Conduction mechanisms in metal/self-assembled monolayer/metal junctions

David Etor[1,2] ✉, *Linzi E. Dodd*[1,3], *Claudio Balocco*[1], *David Wood*[1,3]

[1]*Department of Engineering, Durham University, Durham, DH1 3LE, UK*
[2]*Department of Electrical and Computer Engineering, Baze University, Abuja, 900108, Nigeria*
[3]*Department of Mathematics, Physics and Electrical Engineering, Northumbria University, Newcastle upon Tyne, NE1 8ST, UK*
✉ *E-mail: david.etor@bazeuniversity.edu.ng*

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The conduction mechanisms in metal–insulator–metal junctions where the insulator consists of a self-assembled monolayer are investigated. Temperature dependence measurements from 2.5 to 300 K, show that the conduction is dominated by tunnelling only for temperatures below 20 K, while at higher temperatures surface-limited and bulk-limited mechanisms are observed. The experimental results are explained using a combination of direct (Simmons) tunnelling, Schottky emission, and Poole–Frenkel theory. Further insight is gained through numerical simulations based on the non-equilibrium Green-function formalism.

1. Introduction: The metal–insulator–metal (MIM) diode has attracted significant attention for a variety of high-frequency applications such as detectors, and optical rectennas for electromagnetic energy harvesting [1]. Besides high-speed operation, additional MIM diode requirements for rectenna and detector applications include a small turn-on voltage for a low zero-bias resistance as well as asymmetric and non-linear operation [2]. The ultra-high frequency operation regime desired for these devices requires that the electron transport time between terminals be as short as a few femtoseconds [2]. Based on these operational requirements, very thin (usually 1–4 nm thick) insulators with a large electron affinity are desirable to produce a small energy barrier at the metal-insulator interfaces [3–7]. Existing thin insulator deposition techniques often result in a defective layer, with a large number of pinholes, short-circuiting the diode terminals and drastically reducing yield.

To overcome this problem, we have previously reported the development of a MIM diode in which the insulator self-assembles in a monolayer on a metal surface [8]. The diode uses an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM), which consists of carbon chains strongly packed together with an overall thickness of ~2 nm (thin enough to allow electron tunneling to occur), sandwiched between titanium (Ti) and platinum (Pt) metal electrodes. Due to the nature of self-assembly, a second layer cannot grow on top of the first one, resulting in an extremely uniform thickness over large areas determined by the SAM chemistry [9, 10]. The fabrication process is compatible with large-area roll-to-roll manufacturing. We have also previously reported the fabrication and testing of MIM diodes on a flexible plastic substrate [11] to demonstrate the large-area roll-to-roll manufacturing promise, which the use of OTS dielectric layer presents.

This work investigates the conduction mechanisms, which occur in the Ti/OTS/Pt device at a variety of operating conditions.

2. Conduction mechanisms: The conduction mechanism is responsible for transporting electrons through the dielectric film and gives further insight as to the nature of the dielectric. Conduction mechanisms in MIM diodes fall into two categories of electrode-limited and bulk-limited conduction mechanisms [12]. While the electrode-limited conduction mechanisms depend on the electrical properties of the electrode–dielectric interface, i.e. the height of the barrier located at the electrode–dielectric interface, the bulk-limited conduction mechanisms depend only on the electrical properties of the dielectric [12]. The electrode-limited conduction mechanisms include Schottky (thermionic) emission (SE), direct tunneling (DT) and Fowler–Nordheim tunnelling (FNT). And the bulk-limited conduction mechanisms include Poole–Frenkel emission (PFE) and hopping conduction (HC).

Although it is more desirable for a single conduction mechanism to occur in devices for specific applications throughout the device operation, in reality, a single conduction mechanism does not fully describe the conduction mechanism taking place. Depending on the operating conditions, such as frequency, applied voltage and temperature levels, a combination of conduction mechanisms may be present with one dominating in certain instances.

SE occurs most often in metal–insulator interfaces of MIM structures, especially at relatively high temperatures, and is expressed as [12, 13]

$$J_{\mathrm{SE}} = \left\{A^{*}T^{2}\exp\left[\frac{-q\left(\phi_{B}-\sqrt{qV/4\pi\varepsilon_{i}\varepsilon_{0}}\right)}{k_{B}T}\right]\right\} - \left\{A^{*}T^{2}\exp\left[\frac{-q\left(\phi_{B}+\sqrt{qV/4\pi\varepsilon_{i}\varepsilon_{0}}\right)}{k_{B}T}\right]\right\} \quad (1)$$

where

$$A^{*} = \frac{4\pi q k_{B}^{2} m^{*}}{h^{3}} = \frac{120 m^{*}}{m_{0}}, \quad (2)$$

and A^{*} is the effective Richardson's constant, T is the absolute temperature, m_0 is the free electron mass, m^{*} is the effective electron mass in the dielectric, q is the fundamental electronic charge, $q\Phi_B$ is the Schottky barrier height, k_B is Boltzmann's constant and h is Planck's constant.

Equation (1) can be interpreted as a current density

$$A^{*}T^{2}\exp\left[\frac{-q\left(\phi_{B}-\sqrt{qV/4\pi\varepsilon_{i}\varepsilon_{0}}\right)}{k_{B}T}\right] \quad (3)$$

flowing from metal-1 to metal-2, and another

$$A^{*}T^{2}\exp\left[\frac{-q\left(\phi_{B}+\sqrt{qV/4\pi\varepsilon_{i}\varepsilon_{0}}\right)}{k_{B}T}\right] \quad (4)$$

flowing from metal-2 to metal-1 [13]. Where a typical SE has occurred, the plot of $\ln(J/T^2)$ as a function of $V^{1/2}$ should be linear and is best measured at a high temperature and low voltage [14].

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DT relies on a quantum mechanical effect, where electrons tunnel through the full barrier thickness of a MIM structure even when the applied bias is very small (i.e. $V<\Phi_B$) [12]. The tunnelling of the electrons through the full barrier thickness is made possible by a barrier or insulator that is without defects and is sufficiently thin (typically <4 nm) [3]. In which case, DT would dominate the flow of current in the MIM structure [3, 12, 14]. DT can be measured in a structure by measuring the J–V characteristic of the structure at low temperature (e.g. <30 K) where thermionic emission is sufficiently suppressed, and plotting $\ln(J/V^2)$ as a function of $1/V$. The resultant plot should be linear at points where the applied voltage is very low (i.e. a few mV). The expression for the DT current is [13, 15]

$$J_{\mathrm{DT}} = J_0[\{\phi_B \exp(-A_S\sqrt{\phi_B})\} - \{(\phi_B + V)\exp(-A_S\sqrt{\phi_B + V})\}] \tag{5}$$

where

$$J_0 = \frac{q^2}{2\pi h d_i^2} \tag{6}$$

and

$$A_S = \frac{4\pi d_i\sqrt{2qm^*}}{h} \tag{7}$$

d_i is the thickness of the dielectric film, and all other terms are as defined previously.

As with the SE current density, (3) can be interpreted as a current density

$$J_0[\phi_B \exp(-A_S\sqrt{\phi_B})] \tag{8}$$

flowing from metal-1 to metal-2, and another

$$J_0[(\phi_B + V)\exp(-A_S\sqrt{\phi_B + V})] \tag{9}$$

flowing from metal-2 to metal-1 [13].

FNT is similar to DT, which occur in MIM structures. But unlike the DT where current flows from one electrode to the other through the full dielectric thickness due to a very thin dielectric film, FNT occurs when the insulator thickness is large (>5 nm) and the applied bias is much larger (in volts) than the barrier height $q\Phi_B$. The large applied bias causes the incident electrons on the insulator to have high energy, enough to shrink the thick insulator and penetrate its conduction band [12]. FNT is faster than DT because here the electrons flow through a barrier with a thickness significantly reduced due to the shrinking caused by large bias. The FNT current is expressed by [12]

$$J_{\mathrm{FNT}} = \frac{q^3V^2}{8\pi h\phi_B}\exp\left[\frac{-8\pi(2qm_T^*)^{1/2}}{3hV}\phi_B^{3/2}\right] \tag{10}$$

This current can be measured by measuring the J–V characteristic of the diode at low temperature (e.g. <30 K) where thermionic emission is suppressed, and plotting ln (J/V^2) as a function of $1/V$ [14]. This conduction mechanism dominates the flow of current in a MIM structure if the plot of ln (J/V^2) as a function of $1/V$ is linear at high applied bias [12, 14]. The test for this conduction mechanism is not applicable in this work, as our Ti/OTS/Pt diodes have a small irreversible breakdown voltage (±0.35 V).

PFE is similar to SE, as it is also influenced by thermal excitation of electrons. But rather than electrons overcoming the energy of the barrier at the electrode–dielectric interface and moving into the conduction band of the dielectric, they do so from traps present in the dielectric [16]. This type of conduction mechanism is more often found in defected dielectric films [16–18], and its current density is expressed as [12, 17, 18]

$$J_{\mathrm{PFE}} = CE\exp\left[-\frac{q\phi_T - \sqrt{q^3E/\pi\varepsilon_i\varepsilon_0}}{k_BT}\right] \tag{11}$$

where C is a proportionality constant, and E is the applied electric field. PFE is often observed at high temperature and high applied electric field because the process depends on thermal activation under an electric field [12]. It can be determined from the J–V characteristic of the diode at high temperature, and plotting $\ln(J/V)$ as a function of $V^{1/2}$. The resultant plot should be linear at high applied voltage if the conduction mechanism has occurred [18].

The hopping conduction mechanism is due to the tunnelling effect of trapped electrons in dielectric films hopping from one trap site to another [12]. Unlike in the PFE where the electrons can overcome the trap barrier through thermal activation, the electron energy is lower than the energy of the barrier between adjacent trap sites. However, the electrons can still penetrate through [12]. This is similar to DT but occurs within the dielectric only. Its current density is expressed by [12]

$$J_H = qanv\cdot\exp\left[\frac{qaV - E_a}{k_BT}\right] \tag{12}$$

where a is the mean hopping distance between trap sites, n is the electron concentration in the conduction band of the dielectric, v is the frequency of thermal vibration of electrons at trap sites, and E_a is the activation energy.

3. Ti/OTS/Pt diode fabrication: Fig. 1 (not drawn to scale) shows the basic fabrication process of the Ti/OTS/Pt structure. As in [8], a bilayer of ~25 nm of titanium coated with 100 nm of gold was deposited on a borosilicate glass substrate by e-beam evaporation and lift-off (Fig. 1*a*). After a further photolithographic step, gold was removed by an iodine/iodide wet etching, leaving small regions of titanium exposed (Figs. 1*b* and *c*). After removing the photoresist (Fig. 1*d*), the exposed titanium was coated with OTS (Fig. 1*e*) using techniques as described in [8]. After a further photolithographic step, a thin layer of platinum with a nominal thickness of 40 nm was evaporated on the sample and lifted-off in the unexposed regions, resulting in the definition of small Ti/OTS/Pt junctions (Figs. 1*g* and *h*).

The addition of leads and bonding pads concludes the MIM diode fabrication. An AFM image of a fabricated device can be

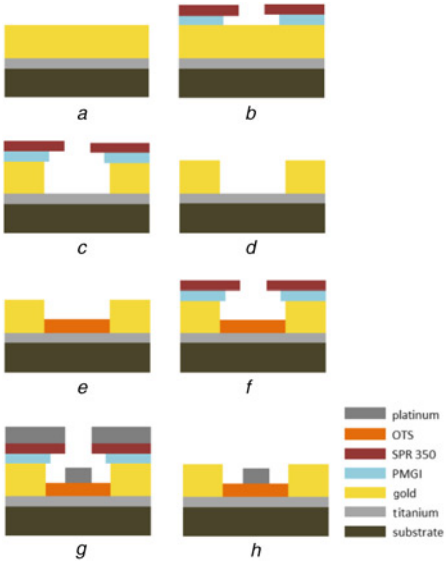

Fig. 1 *Ti/OTS/Pt diode fabrication process. (a) Ti/Au bilayer on the substrate. Photolithographic patterning (b) followed by Au wet etching (c) Photoresist stripping (d) and OTS deposition (e). Photolithographic patterning (f), Pt deposition (g) and lift-off (h)*

seen in the inset of Fig. 2, where the OTS layer is sandwiched between Pt and Ti metal layers at the crossover of two arms which defines the MIM junction. The nominal feature size of the fabricated diode junction is 2×2 μm. The results discussed and the related conclusion made in this work is based on test results from one of seven of these devices, which are very similar.

4. Results and discussions: To determine the conduction mechanism(s) occurring in the Ti/OTS/Pt device, *I-V* measurements were performed on the diodes in the temperature range of 2.5 to 296 K using a closed cycle JANIS SHI-4 optical cryostat. The cryostat was connected to a LakeShore 340 Temperature Controller and an Agilent B2902A (SMU) parameter analyser, and controlled via Matlab-based software. Fig. 2 shows the typical device *I–V* characteristics for a selection of temperatures. The diode current increases with temperature, which is expected, as higher temperatures increase the possibility of thermionic emission being present, resulting in a significant increase in current.

With the result in Fig. 2, it was clear that thermionic emission is significant in the device, but it was worth understanding the device functionality at much lower temperatures. It can be seen in the plot of the current as a function of temperature shown in Fig. 3 that the current is almost constant from a temperature of 2.5 to ~25 K (see inset in Fig. 3).

This suggests that DT was the dominant conduction mechanism occurring in the diode while operating at these temperatures. Fig. 4 further suggested that there were no emission conduction mechanisms occurring in the device at these low temperatures, as the *I–V* characteristics can be seen (Fig. 4) to be temperature independent from 2.5 up to ~20 K.

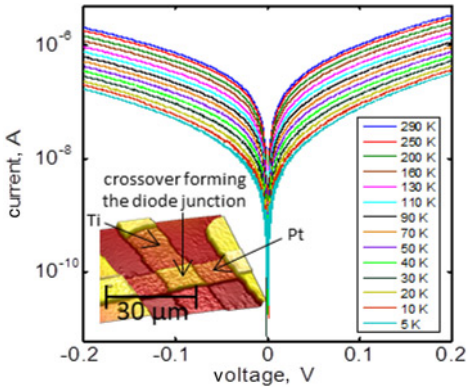

Fig. 2 *I–V characteristics (in log scale) of the Ti/OTS/Pt device for a selection of temperatures. In the inset is an AFM image of a fabricated device*

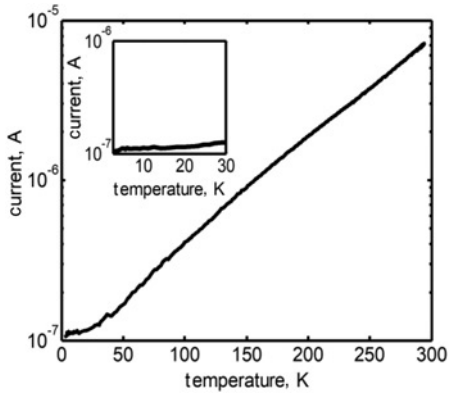

Fig. 3 *Current versus temperature plot for the Ti/OTS/Pt structure at a voltage of 0.2 V*

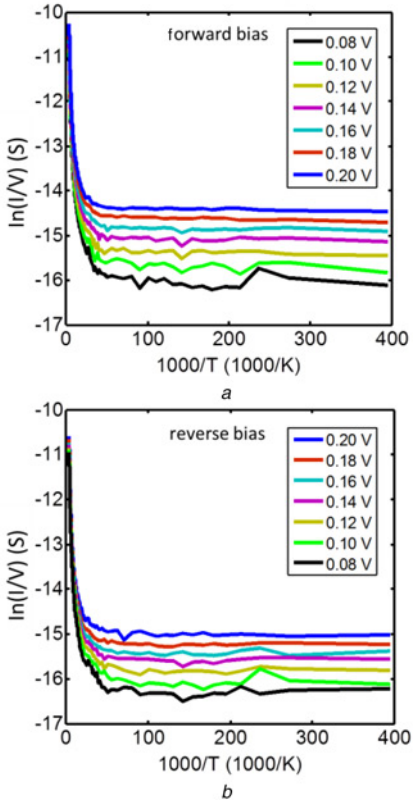

Fig. 4 *I–V characteristics (conductance) versus temperature (2.5–296 K) plot for the Ti/OTS/Pt structure for a selection of voltages*
a Forward bias
b Reverse bias

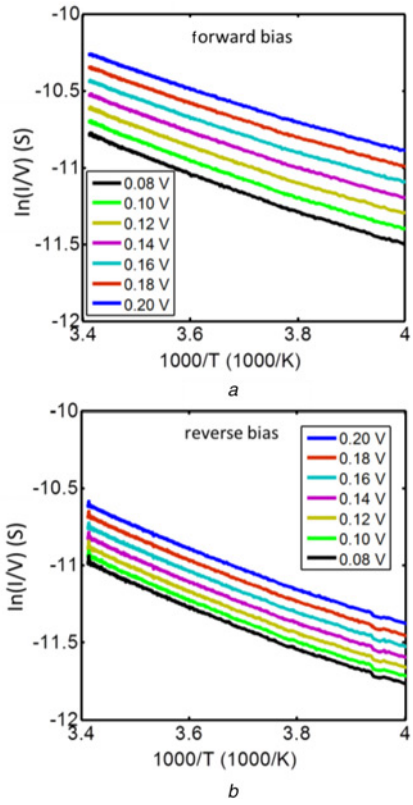

Fig. 5 *I–V characteristics (conductance) versus temperature (250–296 K) plot for the Ti/OTS/Pt structure for a selection of voltages*
a Forward bias
b Reverse bias

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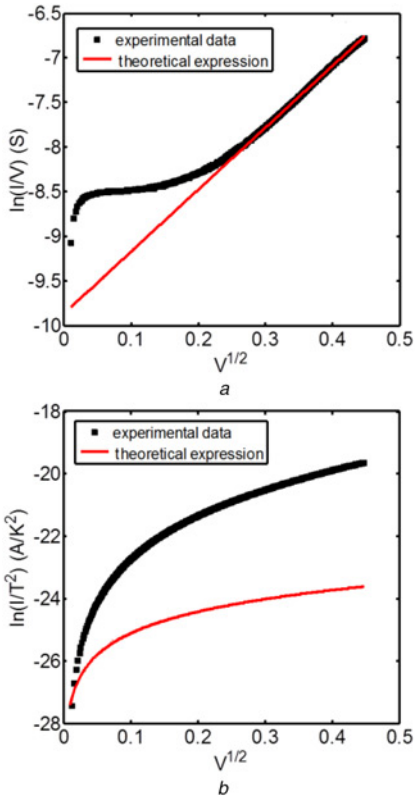

Fig. 6 *Plot of the experimental data and theoretical expressions for*
a Poole–Frenkel emission
b Schottky emission at a temperature of 296 K

However, as can be seen in Fig. 5, at higher temperatures (250 K and above), the *I–V* characteristics were strongly temperature dependent, which suggested that emission conduction mechanisms were taking place in the device and dominated the transport of electrons at these high temperatures.

It is put forward that the emission conduction mechanisms occurring in the device at higher temperatures were either Schottky emission or Poole–Frenkel emission, or a combination of both. To verify these hypotheses, the experimental and theoretical Poole–Frenkel emission expressions were plotted in Fig. 6*a*. In the plot, the experimental data clearly shows that there is more than one regime of conduction mechanisms occurring in the diode, as the theoretical expression only agrees with a certain section of the experimental data.

Experimental and theoretical Schottky emission expressions were also plotted in Fig. 6*b*, with the plot showing a considerable disagreement between the experimental and theoretical data. The results in Figs. 5 and 6 suggest that there is more than one emission conduction mechanism occurring in the diode at temperatures above 25 K, and the process is being dominated by the Poole–Frenkel emission. The accuracy of the theoretical expressions suffered from uncertainty in the value of the OTS barrier height, as the value is not known and it is not available in the literature; a value of 1.33 eV (which resulted in the closest agreement between the experimental and theoretical expressions) was assumed throughout the investigation. It is speculated that the Poole–Frenkel behaviour arises from trap centres located in the SAM layer. This implies that the transport mechanism that would be occurring in the device, as it is, for the applications it could potentially be used for, including rectenna, thermal-energy harvesting, and high-frequency detectors, will be predominantly emission transport mechanisms, as these applications operate at room or higher temperatures.

5. Conclusion: The conduction mechanisms responsible for transporting electrons in the OTS dielectric layer of the Ti/OTS/Pt MIM structure have been investigated. The comparison of experimental and theoretical data showed that, while direct tunnelling conduction mechanism dominates the transport of electrons in the diodes at temperatures of ~25 K and below, Poole–Frenkel takes over at ~25 K and above. As, ideally, it is desirable for the tunnelling conduction mechanisms to dominate the transport of electrons in the structure throughout its potential operation temperatures (as the tunnelling conduction mechanisms transport electrons faster than the emission conduction mechanisms), further work is ongoing to optimise the OTS deposition technique in order to eliminate or significantly reduce the disorder occurring in the OTS SAM as a result of the presence of traps.

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7 References

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