Inductively coupled CH_4/H_2 plasma etching process for mesa delineation of InAs/GaSb type-II superlattice pixels

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An inductively coupled CH_4/H_2 plasma etching process for delineation of InAs/GaSb type-II superlattice pixels is presented. An optimised CH_4/H_2 etch recipe without alternate O_2 plasma cleaning step showed an etch rate as high as 0.11 μm/min that results in smooth vertical sidewalls for the type-II superlattice pixel arrays with 10 μm pitch size and 2.4 μm deep trenches. At 70 K, the dark current density for the mesa etched + SU-8 polymer passivated type-II superlattice photodiodes was found to be 0.11 A/cm^2 at an applied reverse bias voltage of 0.2 V. The activation energy of 13 meV obtained from the Arrhenius plot and a variable area diode array technique showed that the measured dark current is mainly attributed to bulk tunnelling current. This technique of mesa delineation for the type-II superlattice pixel arrays with small pitch size is a viable option in realising next-generation infrared focal plane arrays.

1. Introduction: InAs/GaSb type-II superlattice (T2SL) based infrared focal plane arrays (FPAs) have recently seen rapid advances [1, 2]. The development of next-generation FPAs requires high packing density of detector pixels with small pitch size that creates a need for a mesa delineation technique capable of producing deep and vertical mesa sidewalls. Cl_2-based reactive ion etching (RIE) is widely used for delineation of the T2SL pixels [3]. However, low volatility of $InCl_3$ etch products formed during etching leads to rough surfaces and also results in bevelled sidewall profiles of the T2SL pixels which thus creates challenges for etching deeper structures with smaller inter-pixel width <2 μm [3]. CH_4/H_2 is another RIE chemistry extensively used for InP compounds to realise vertical mirror facet waveguide structures with high aspect ratio [4]. CH_4/H_2 RIE can be effectively used for realising various novel nanostructured devices on InP similar to those designed on Si [5]. Similar to InP, CH_4/H_2 etching of InAs is found to be slow and well controlled, resulting in vertical profiles and smooth etched surfaces [6]. However, for Ga content semiconductors such as GaAs and GaSb, although CH_4/H_2 etching results in mirror smooth etched surfaces and vertical profiles, the etch rate is found to be very low due to the low volatility of Ga-organometallic complexes formed during etching [7]. The etch rate can be increased by using CH_4/H_2 RIE in inductively coupled plasma (ICP) configuration [8]. CH_4/H_2 RIE is also found to be an effective technique for realising high optical quality nanostructures on group-III nitride materials [9]. A major drawback in this chemistry is polymer deposition on the substrate which reduces the etch rate [10]. Therefore, in practice, the etching process is altered with O_2 plasma cleaning in order to remove the polymer layer [4, 10]. Although CH_4/H_2 etching has been studied extensively for bulk semiconductors, to the best of our knowledge, no such studies on InAs/GaSb T2SL structure for delineation of pixel arrays have been reported.

In this Letter, we present a CH_4/H_2 ICP RIE process with and without using an alternate O_2 plasma cleaning step for delineation of the T2SL pixel arrays with pitch size of 10 μm. We found that unlike in InP or GaAs compounds, alternate O_2 plasma cleaning step inhibits etching process for the T2SL structure and leads to rough surfaces. However, a single step CH_4/H_2 ICP RIE recipe without alternate O_2 plasma cleaning step results in perfectly vertical sidewalls of the pixels with smooth etched surfaces. The electrical characterisations of these mesa etched T2SL photodiodes passivated with SU-8 polymer are also presented.

2. Experiments: The InAs/GaSb T2SL layer structure with cutoff wavelength of ~5.5 μm used in this work was grown on an n-type (100) GaSb substrate using solid source molecular beam epitaxy (MBE). The p-i-n detector structure, shown in Fig. 1, consists of the following, bottom to top:

Substrate: n-type GaSb.

n^+ *contact layer*: [10 monolayers (MLs) InAs:Si (1×10^{18} cm^{-3}) + 10 MLs GaSb] repeated 80 times, total 0.506 μm thick superlattice (SL).

Layer to improve carrier transport: (10 MLs InAs + 10 MLs GaSb) repeated 20 times with graded n-doping, total 0.126 μm thick SL.

Undoped absorber layer: (10 MLs InAs + 10 MLs GaSb) repeated 205 times, total 1.3 μm thick SL.

Layer to improve carrier transport: (10 MLs InAs + 10 MLs GaSb) repeated 20 times with graded p-doping, total 0.126 μm thick SL.

p^+ *contact layer*: [10 MLs InAs:Be (1×10^{18} cm^{-3}) + 10 MLs GaSb] repeated 10 times, total 0.063 μm thick SL.

The X-ray diffraction measurement (not shown here) showed that the thickness of one period of the SL, consisting of 10 MLs InAs + 10 MLs GaSb, is 6.33 nm. Dry etching experiments were performed in an Oxford Instruments, PlasmaLab80Plus system by CH_4/H_2 ICP RIE. To study etch profiles, an array of 8 μm square pixels with 2 μm inter-pixel gap was fabricated using 150 nm thick Al etch mask. Al was found to have very high mask selectivity in CH_4/H_2 ICP RIE process and post etch it can be easily removed with commercial developer like Microposit CD26 without affecting the SL structure. The surface morphology of these etched pixels was examined by scanning electron microscope (SEM) and etch depth was measured by optical profiler. To perform electrical characterisations, a variable area diode array (VADA) pattern

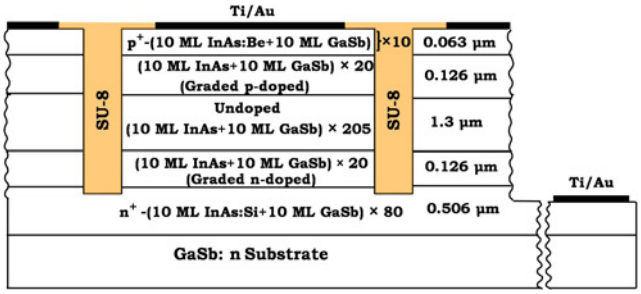

Fig. 1 *Schematic layer structure of the InAs/GaSb T2SL detectors for demonstration of* CH_4/H_2 *ICP RIE etching + SU-8 passivation technique*

with mesa sizes ranging from 55×55 to 400×400 μm^2 with 10 μm inter-pixel gap were similarly processed. The mesa sidewalls were then covered with SU-8 2002 polymer to act as the passivation layer. Subsequently, top p^+ and bottom n^+ ohmic contacts were made using Ti (500 Å)/Au (3500 Å) by e-beam metal evaporation followed by a liftoff process. A schematic of the device structure is shown in Fig. 1. Finally, the devices were gold wire bonded and mounted on a cold finger inside a Helium cryostat for electrical measurement.

3. Results and discussions: Based on the optimised CH_4/H_2 ICP RIE recipes for InP compounds that result in smooth vertical profiles with high aspect ratio [11], we choose our standard etching conditions as CH_4:H_2 = 15 sccm: 40 sccm, RF/ICP power = 200 W/300 W, chamber pressure = 30 mtorr and O_2 plasma clean recipe as O_2 = 100 sccm, RF/ICP power = 200 W/300 W, chamber pressure = 50 mtorr with repeated cycles of 5 min etching + 1 min cleaning. Initial experiments were performed on bulk GaAs using these recipes for four repeated cycles of 5 min etching + 1 min O_2 plasma cleaning. The etched profiles were found to be vertical with mirror smooth surfaces as shown in Fig. 2*a*; however, the etch rate is very low ~18 nm/min as expected for the Ga content semiconductors. The etching was then carried out on the Al masked 8×8 μm^2 T2SL pixel arrays using similar alternate etching + cleaning recipes. However, unlike GaAs etched profiles, the T2SL etched surfaces and pixel sidewalls were found to be very rough as shown in Fig. 2*b* and the T2SL etch rate was found to be ~20 nm/min. This may be attributed to buildup of a native oxide layer when T2SL layer is exposed to O_2 plasma [12]. The surface of GaSb is much more reactive than that of InAs being easily oxidised when exposed to O_2 plasma and forms a native gallium oxide layer. However, non-uniform desorption of the native oxide from the GaSb surface [13] and etch-resistant nature of such oxides may result in non-uniform etching of the underlying T2SL layers in the subsequent etching steps, causing roughness in the etched surfaces and sidewalls. The etch-resistant nature of the oxide layer comes from the fact that the Ga–O bond strength is higher than that of the Ga–Sb bond [14]. This also accounts for the observed low etch rate in the alternate CH_4/H_2 etching + O_2 cleaning process. This is consistent with the result of lower etch rate obtained in the group-III nitride materials etched with O_2 containing plasmas [9]. A single step etching with similar CH_4/H_2 ICP RIE etch recipes without O_2 plasma cleaning step, however, results in much higher etch rate. A variation of T2SL etch rate as well as etch depth as a function of single step etch time is plotted in Fig. 3 along with the fitted curves. The etch rate in Fig. 3 is obtained from the first derivative of the etch depth graph. An interesting observation here is that the etch rate increases linearly with etching time. This can be explained on the basis of the temperature dependence of GaSb etch rate in CH_4/H_2 etching process [6]. It has been observed that GaSb etch rate increases linearly with temperature whereas InAs etch rate is fairly constant over a wide range of

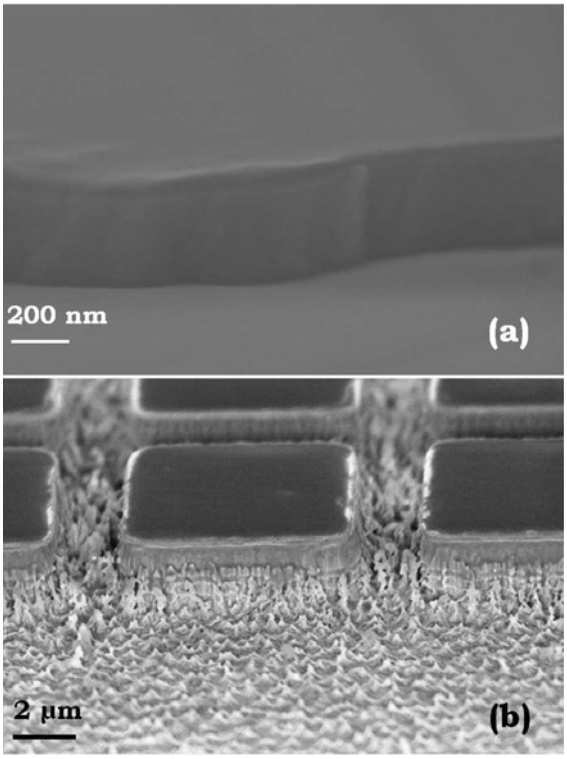

Fig. 2 *SEM image of etched*
a GaAs profile
b T2SL pixel arrays using CH_4/H_2 ICP RIE with CH_4:H_2 ratio 15:40. Four cycles of 5 min etching + 1 min O_2 plasma cleaning are done at RF/ICP power = 200/300 W

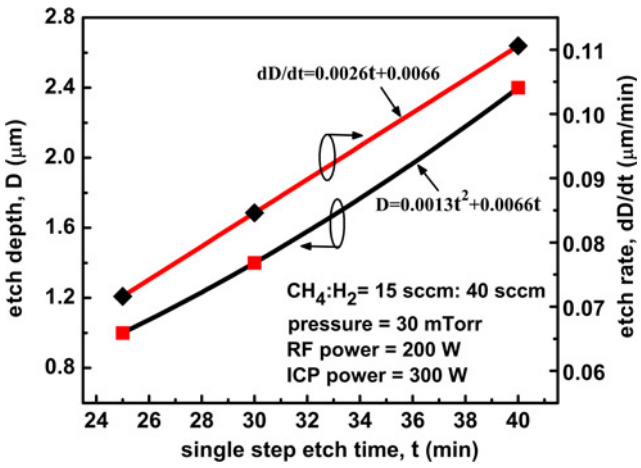

Fig. 3 *Variation of T2SL etch rate and etch depth as a function of single step etch time for a* CH_4/H_2 *ICP RIE process without using alternate* O_2 *plasma cleaning. Here, symbols and lines are shown for experimental and fitted data, respectively*

temperature and GaSb etch rate approaches the InAs etch rate at ~ 125 °C. The temperature dependence of GaSb etch rate thus provides an extra control on defining the InAs/GaSb heterostructure etched profile. The increase in etch rate as observed in Fig. 3 may be due to the increase in GaSb etch rate which may be the result of the rise in sample temperature when the single step etching time increases. The resulting smooth and vertical etched profiles of the T2SL after 40 min of single step etching also suggests that the GaSb etch rate is increased and is equal to that of InAs. In addition, polymer deposition was hardly visible after this etching process. An etch rate as high as 0.11 μm/min was obtained,

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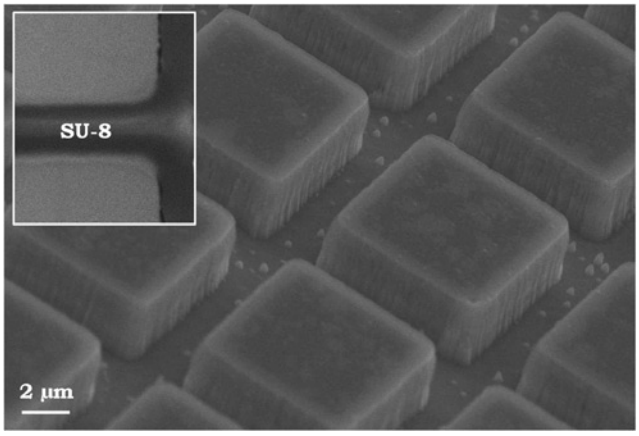

Fig. 4 *SEM image of single step* CH_4/H_2 *ICP RIE etched T2SL pixel arrays of size 8 μm × 8 μm with inter-pixel gap of 2 μm. Inset shows the top view of the mesa etched + SU-8 passivated T2SL photodiodes*

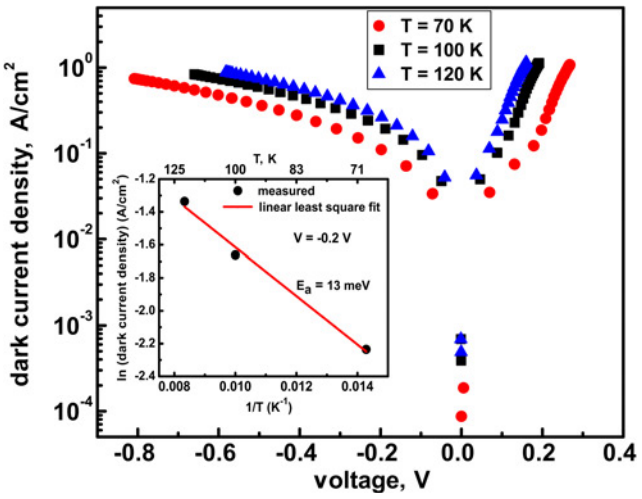

Fig. 5 *Dark current densities as a function of applied voltage for a single step* CH_4/H_2 *ICP RIE etched + SU-8 passivated 400 μm × 400 μm T2SL photodiode measured at different temperatures. Inset shows the Arrhenius plot of log of dark current density as a function of inverse of temperature, at 0.2 V of applied reverse bias*

resulting in an etch depth of ~2.4 μm. This is probably the highest CH_4/H_2 etch rate reported for the T2SL material in the form of such dense pixel arrays. Fig. 4 shows the SEM image of the mesa delineated T2SL pixels with vertical mesa sidewalls. The T2SL etched profile obtained in this work is found to be more vertical than that reported with chlorine-based ICP RIE [15]. The VADA patterns were similarly processed using this single step CH_4/H_2 ICP RIE recipe to etch up to ~1.8 μm (down to middle of the n^+ contact layer) for mesa isolation. This was followed by patterning SU-8 polymer at the device sidewalls as shown in inset of Fig. 4. SU-8 serves as a surface passivation layer for these T2SL detectors [16].

Fig. 5 shows the bias dependent dark current densities for a 400 μm × 400 μm T2SL photodiode in the VADA structure measured at different temperatures. At 70 K, the dark current density was found to be 0.11 A/cm^2 at an applied reverse voltage of 0.2 V which is an order of magnitude higher than the reported result [17]. However, at room temperature, the dark current was found to be very high with nearly non-rectifying characteristics and hence the data are not presented here. The activation energy of 13 meV estimated from the Arrhenius plot, shown in inset of

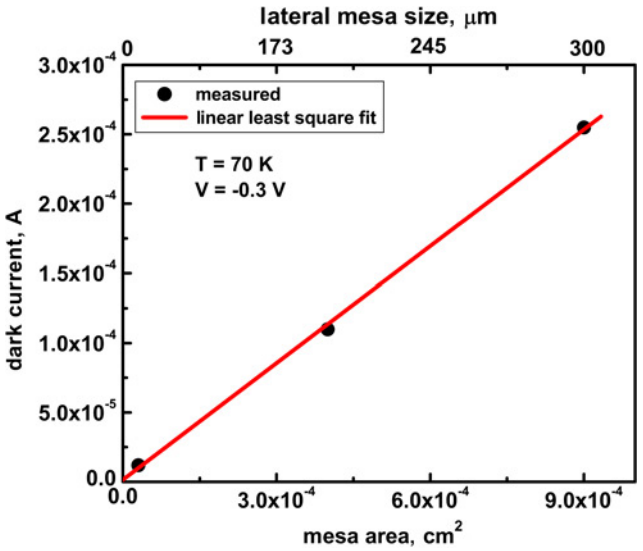

Fig. 6 *70 K reverse dark current versus the mesa area for the* CH_4/H_2 *ICP RIE etched + SU-8 passivated T2SL photodiodes, at 0.3 V of applied reverse bias*

Fig. 5, suggests that the origin of dark current is neither dominated by diffusion process nor by midgap Shockley–Read–Hall centres [18]. This possibly indicates that the dark current is dominated either by tunnelling current or by surface leakage. The bulk and surface contributions in the dark current are investigated by the VADA technique where values of dark current are plotted as a function of mesa area and a linear fit of these data points is performed as shown in Fig. 6. The fitting line intercepts with the origin clearly suggests that the bulk leakages are the dominant dark currents and the surface leakage current is completely suppressed by a combination of CH_4/H_2 ICP RIE and SU-8 passivation. Therefore, the high dark current as obtained in the T2SL photodiodes even at 70 K mainly arises due to tunnelling current which is assisted by high density of traps present in the used SL layers [19] and that can be minimised with the availability of a better SL epitaxial layers.

4. Conclusions: A single step CH_4/H_2 ICP RIE process for delineation of the InAs/GaSb T2SL pixels with pitch size down to 10 μm is presented. Introducing an alternate O_2 plasma cleaning step in the CH_4/H_2 etching results in rough surfaces for the T2SL structure with poor etch rates. An optimised single step CH_4/H_2 ICP RIE recipe without alternate O_2 plasma cleaning showed an etch rate as high as 0.11 μm/min with vertical profiles and smooth etched surfaces of the T2SL array of 8 × 8 μm^2 pixels with 2 μm inter-pixel width. This is probably the highest CH_4/H_2 etch rate reported in this material system. The mesa etched T2SL photodiodes with SU-8 polymer passivation showed a dark current density of 0.11 A/cm^2 at an applied 0.2 V reverse bias which is an order of magnitude higher than previously reported results. The activation energy of 13 meV estimated from the Arrhenius plot and a VADA technique reveals that tunnelling is the dominant dark current component which is mainly assisted by high density of traps present in the used SL layers. It is expected that if this single step CH_4/H_2 ICP RIE + SU-8 passivation technique is used for better epitaxial T2SL layers, the leakage currents of the photodiodes would be much lower. In view of the smooth vertical sidewalls of the T2SL pixels with pitch sizes down to 10 μm and an etch depth up to 2.4 μm achieved in this work, single step CH_4/H_2 ICP RIE appears to be a promising technique in realising next generation T2SL FPAs.

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