Fabrication of QDNVM-based comparator

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This work presents the fabrication of 1 bit comparator circuit based on quantum dot gate non-volatile memory (QDNVM) for both analogue-to-digital and digital-to-analogue signal processing applications. The charge accumulation in the gate region varies the threshold voltage of QDNVM, which can be used as a reference voltage source in a comparator circuit. A simplified comparator circuit can be implemented using the QDNVM. In this work, the authors discuss the fabrication of QDNVM-based comparators in designing analogue-to-digital converters and digital-to-analogue converters.

1. Introduction: In the analogue-to-digital conversion, the analogue signals are quantised in some specific values which are represented by digital bits. In quantisation, the analogue signal is compared with various reference voltages and is represented by different quantised values. This rounding up of the analogue signal to some quantised levels produces quantisation noise [1–4]. The quantisation noise can be reduced as well as the precision of conversion can be increased by designing high-resolution compact comparator [1] circuit. Quantum dot gate non-volatile memory-based (QDNVM) comparator may have some solution. The crossover point of the QDNVM-based comparator can be changed precisely by controlling the threshold voltage of the QDNVM in the comparator circuit. This work shows the fabrication of comparator with QDNVM as a circuit element.

In this work, SiO_x-cladded-Si QDs are used in the gate region of the QDNVM. Various researches are going on the metal nanoparticle. Recent work shows that the threshold voltage shift for metal QDs is more than semiconductor QDs [5, 6]. However, there are some basic issues regarding metal nanoparticle. The major issue is an impurity. Since nanoparticles are highly reactive, they interact with impurities. They are very unstable. So, encapsulation is necessary when they are a fabrication stage. SiO_x-cladded-Si nanoparticles are already encapsulated which prevent them from reacting with other impurities as well as this cladding also used to decrease the charge leakage from the core of the silicon QDs.

2. QDNVM device structure: A QDNVM is similar to a conventional metal–oxide–semiconductor field-effect transistor (MOSFET) having different gate structure. In a QDNVM, SiO_x-cladded-Si QDs are deposited on top of the gate tunnel insulator. On top of QD layers, a silicon nitride (Si_3N_4) is deposited. The QD layer works as a floating gate to store charges and is responsible for the change in the threshold voltage of the device. The cross-sectional schematic representation of the QDNVM structure is shown in Fig. 1. The high-resolution transmission electron micrograph (HRTEM) image of fabricated QDNVM is shown in Fig. 2.

3. Theory of operation: In the QDNVM, the threshold voltage depends on the amount of charge stored in the QDs in the gate region. The threshold voltage of a QDNVM can be represented as $V_{TH}+\Delta V_{TH}$, where ΔV_{TH} is the threshold voltage shift due to charging and discharging of the quantum dots. The self-consistent Schrödinger and Poisson equations solution can be used to predict the threshold voltage shift in the QDNVM [7–10].

The tunnelling of charge carriers changes the flat band voltage (ΔV_{FB}) as well as the threshold voltage (ΔV_{TH}) of the device. The change in threshold voltage for two groups of quantum dot layers can be expressed as below:

$$\begin{aligned}\Delta V_{TH1} &= -\frac{q}{C_{OX}}\int_0^{X_g}\frac{x\rho(x)}{X_g}\,dx \\ &= -\frac{q}{C_{OX}}\left[\sum\frac{X_{QD1}n_1N_{QD1}}{X_g}+\sum\frac{X_{QD2}n_2N_{QD2}}{X_g}\right]\end{aligned} \quad (1)$$

Here, X_{QD1} is the distance of first-layer quantum dot core from the gate contact; X_{QD2} is the distance of second-layer quantum dot core from the gate contact; n_1 is the number of dots in layer 1; n_2 is the number of dots in layer 2; n_3 is the number of dots in layer 1; n_4 is the number of dots in layer 2; N_{QD1} are charges on each SiO_X-cladded-Si quantum dots in the first layer; N_{QD2} are charges on each SiO_X-cladded-Si quantum dots in the second layer; X_g is the distance of the Si–SiO_X interface from the gate; $\rho(x)$ is the charge density; and ΔV_{TH1} is the change in threshold voltage for electrons in layer 1 and layer 2.

According to the device simulation, more than two layers of quantum dots in the gate region do not affect the threshold voltage significantly. The effect of stored charge in the channel is not only dependent on the number of charged QDs but also on their distance from the channel. The effect decreases with distance. As the number of dots is increasing, the threshold voltage will increase for a particular layer of dots. When dots accumulated on top of the other QD layer, the distance of the layer increases as well as the number of dots. The mutual effect controls the threshold voltage.

Initially, in a QDNVM, there is no charge stored in the QDs on top of the gate insulator. The tunnelling of charge carriers from inversion channel to QDs on top of the gate insulator may happen due to various mechanisms such as direct tunnelling, Fowler–Nordheim tunnelling, trap-assisted tunnelling etc. The threshold voltage of the device can be controlled externally by applying different voltages in the control gate. The transfer characteristics (I_D versus V_{GS}) and output characteristics (I_D versus V_{DS}) of fabricated QDNVM (Table 1) are shown in Figs. 3 and 4, respectively. Metal gate shows less resolution for different pulse magnitudes for different durations (Fig. 3*a*). QDs in the gate region of QDNVM show more resolution for different pulse magnitudes for a different duration. In Fig. 3*b*, a 12 V pulse for different durations (20 µS, and others) are applied to

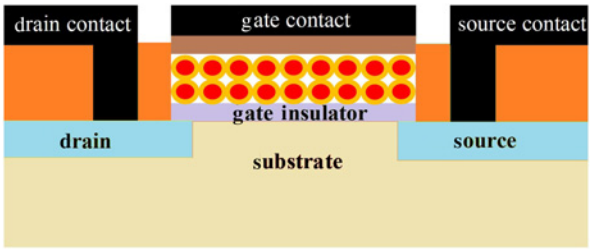

Fig. 1 *Cross-sectional schematic representation of QDNVM*

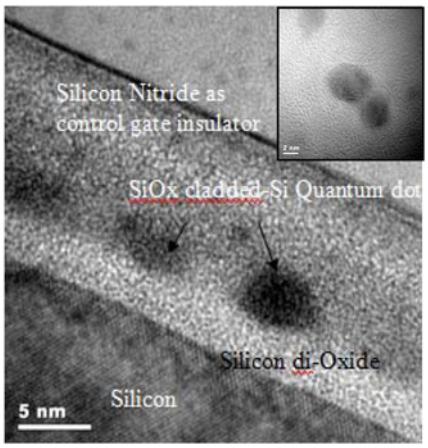

Fig. 2 *HRTEM image at the gate region of QDNVM*

Table 1 Different parameters of a fabricated QDNVM

Parameters	Value
width, W	0.5 μm
length, L	0.5 μm
core diameter of Si-dot	4 nm
SiO_x thickness around the core	1 nm
mobility	600 cm^2/Vs
tunnelling gate insulator (silicon dioxide) thickness	40–50 Å
threshold voltage (V_{TH})	0.7 V
supply voltage (V_{DD})	5.0 V

store the different amounts of charge in the gate region. The threshold voltage of the device before any pulse in the gate region is around 1.00 V. Owing to charging, the threshold voltage of the device changes which is shown in the transfer characteristics. Fig. 3*c* shows that there are not significant changes in the transfer characteristics for more than two QD layers.

4. Fabrication: The fabrication of comparator was performed using conventional silicon fabrication process. In this process, the starting material was P-type Si-wafer. The P-type Si-wafer was cleaned using trichloroethylene, acetone, methanol and de-ionised water. Then, the wafer was processed through radio corporation of america (RCA) cleaning followed by cleaning with piranha solution. After the wafer was cleaned, it is transferred to wet oxidation furnace at 1000°C to grow wet oxide of 1200 Å which acts as a hard mask for the source and the drain diffusion. The source and drain regions were opened using photolithography techniques using source–drain opening mask. A gate region was formed. In the gate region formation, a gate opening mask was used to open the gate between the source and drain and a sacrificial oxide of 400 Å was grown in the gate region. The sacrificial oxide was used to clean the gate region for the following gate process. After growing the sacrificial oxide in the gate region, the gate is reopened to grow the actual gate oxide having thickness 40–50 Å. Quantum dots on top of the gate insulator are deposited using site-specific self-assembly method. In this method, the sample was dipped in a

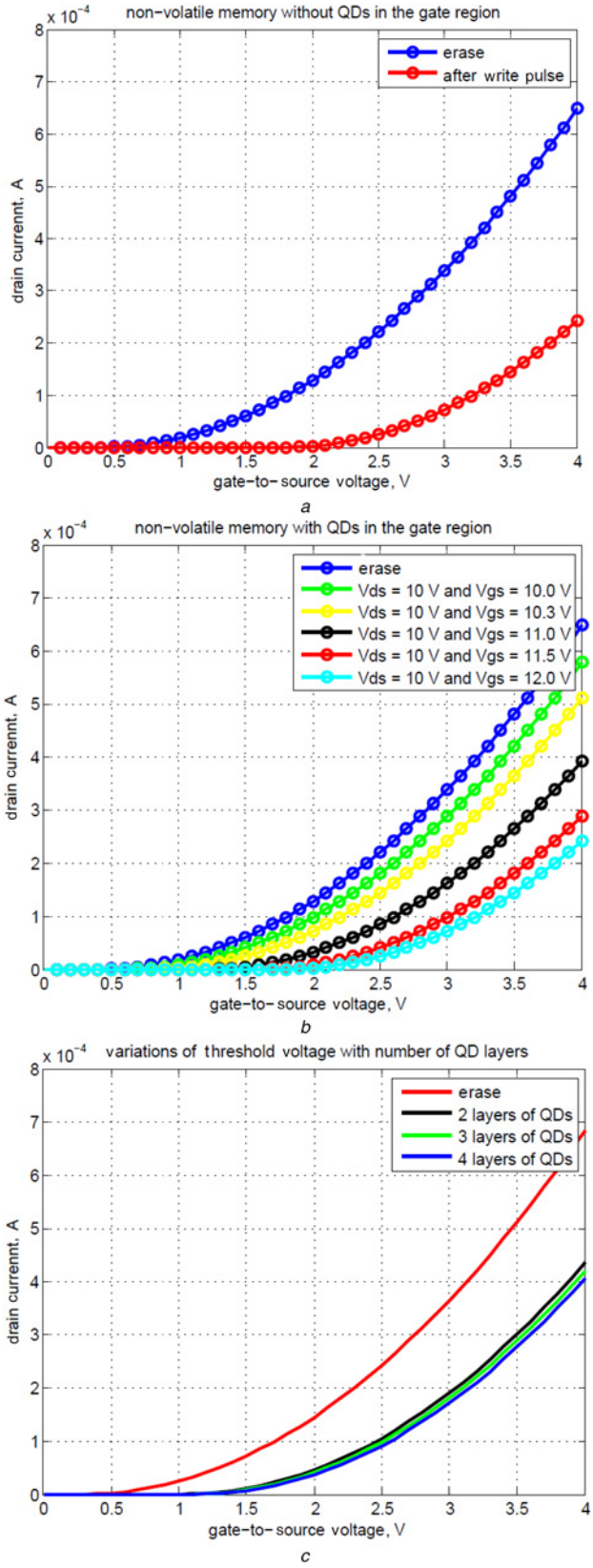

Fig. 3 *Transfer characteristics of*
a NVM with conventional MOSFET
b QDNVM before pulse (BLUE) and after the pulse (RED and others) at the gate terminal
c QDNVM with different numbers of QD layers

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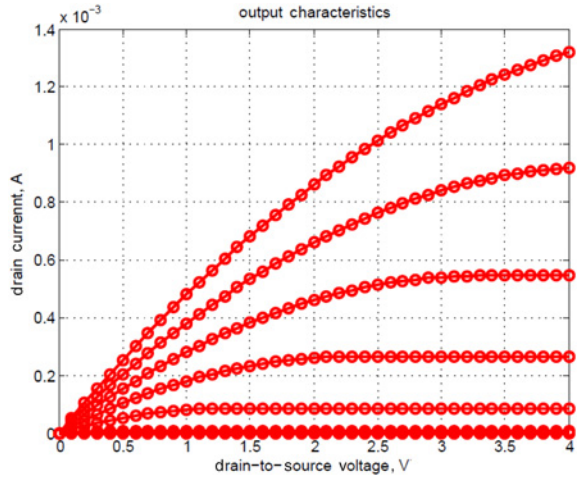

Fig. 4 *Output characteristics of QDNVM*

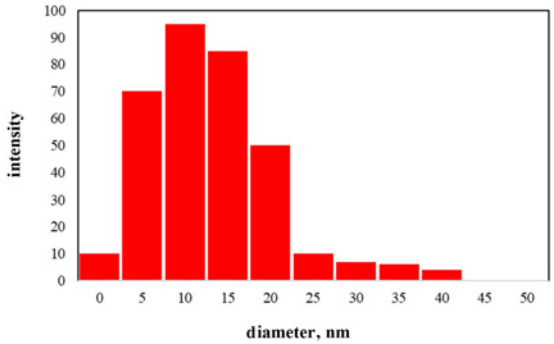

Fig. 5 *DLS of fabricated QDs in the QDNVM*

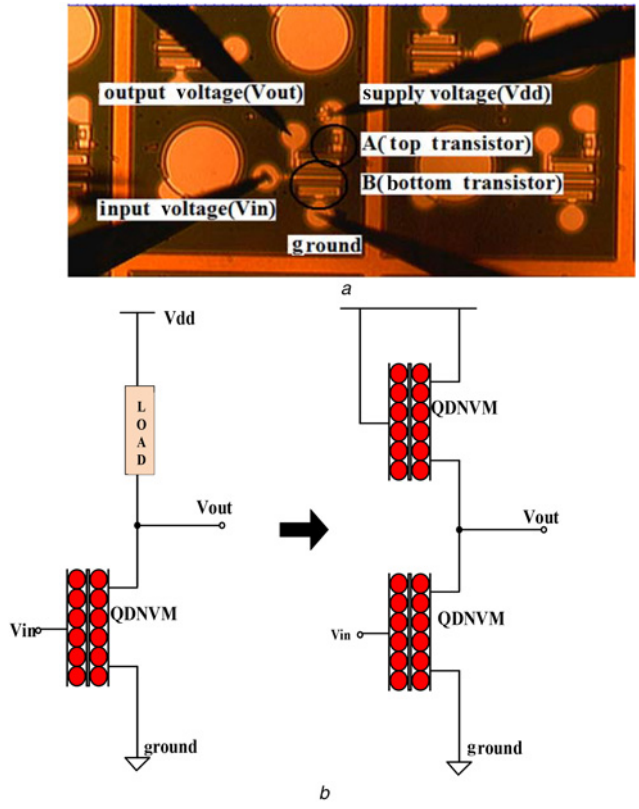

Fig. 6 *Comparator*
a Top view
b Circuit diagram

solution of QDs having PH 5.5 for 5 min to form the quantum dot layer in the gate region. Owing to opposite polarity surface charge in the device, the QDs from QD solution were deposited on top of the gate insulator. The dynamic light scattering (DLS) data shown in Fig. 5 which shows the average QDs diameter is between 10 and 15 nm. A control gate of Si_3N_4 is deposited on top of the quantum dot layer using plasma-enhanced chemical vapour deposition (PECVD) at 250°C. After depositing the gate stack, the final step was to fabricate different contacts. Initially, the source and the drain contact holes were formed by using source–drain contact hole mask which follows thermal evaporation of AuAs as contact material. Then, the device was annealed in the nitrogen–hydrogen environment at 300°C for 1 min to form an ohmic contact. Then, aluminium was evaporated on top of the device and interconnect mask was used to form different contact terminals.

The process flow of the fabrication is as follows:

(i) Clean the silicon wafer.

(ii) Wet oxidation for 1200 Å oxide.

(iii) Open source and drain regions with source and drain opening masks.

(iv) Phosphorous diffusion for source and drain formations.

(v) Open the gate and growth of 400 Å sacrificial oxide for gate cleaning.

(vi) Open gate again to grow gate oxide having thickness 40–50 Å.

(vii) Deposition of QDs in the gate region by using site-specific self-assembly method.

(viii) Deposit Si_3N_4 using PECVD.

(ix) Open source and drain contact hole.

(x) Deposit AuAs using the lift-off method.

(xi) Anneal at 300°C for 1 min in the nitrogen–hydrogen environment.

(xii) Evaporate aluminium on top of the device.

(xiii) Gate contact and metal interconnects are formed.

5. Comparator: In the comparator circuit, the pull-up QDNVM works as a resistive load since the gate and drain are connected. The pull-down QDNVM plays a major role to change the crossover point of the comparator circuit. The fabricated comparator circuit is shown in Fig. 6. The top view is shown in Fig. 6*a* and the circuit diagram is shown in Fig. 6*b*. In Fig. 6*a*, different terminals and

Table 2 Different measured parameters of a fabricated comparator

Parameters	Value
width	0.5 µm
length	0.5 µm
supply voltage (V_{DD})	2.5 V
average current	3.1 µA
propagation delay	1.27 µS
offset voltage	2.42 mV

different transistors are marked. Fig. 6*b* shows the circuit diagram of the fabricated comparator (Table 2) which is an N-channel MOS (NMOS) inverter, where the load of the inverter is replaced by a QDNVM. The driving transistor of the NMOS inverter is also replaced by a QDNVM. When the input is low, the bottom QDNVM is OFF and the output will be high through the load transistor. When the input is high and beyond the threshold voltage of the bottom transistor, the bottom QDNVM is ON and output will be based on the conductivity of the pull-down QDNVM.

The output voltage of the comparator is expressed as

$$V_{\mathrm{OUT}} = V_{\mathrm{DD}} - I_{\mathrm{LOAD}} \times R_{\mathrm{LOAD}} \tag{2}$$

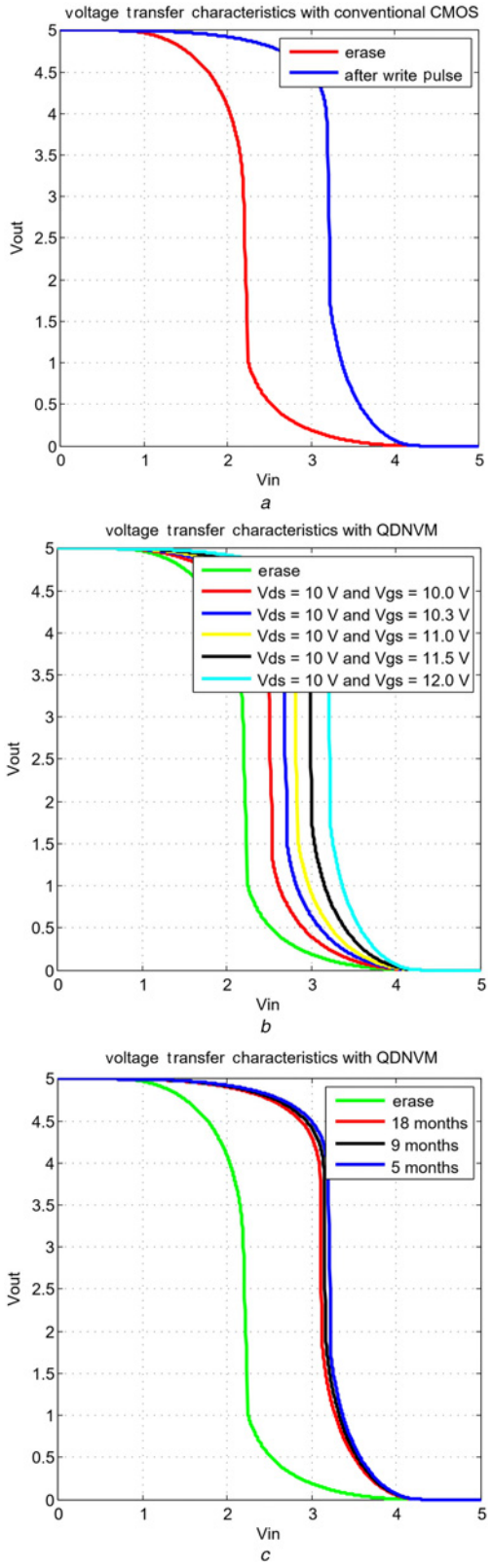

Fig. 7 *Measured comparator transfer characteristics with*
a Conventional MOSFET
b QDNVM
c Retention of charge after a different time frame

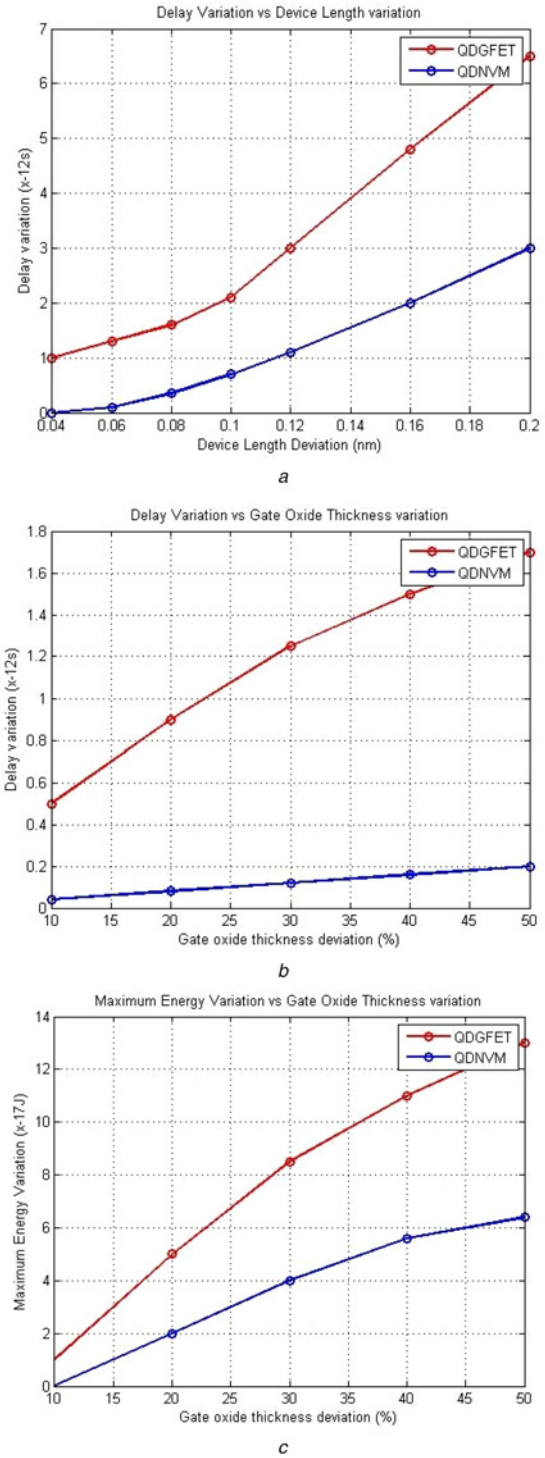

Fig. 8 *Process variation for different technologies*
a Delay variation versus device length variation
b Delay variation versus gate oxide thickness variation
c Maximum energy variation versus gate oxide thickness variation

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I_{LOAD} depends on the threshold voltage of the pull-down QDNVM. As threshold voltage increases, I_{LOAD} decreases and V_{OUT} increases. The opposite will happen when the threshold voltage of pull-down QDNVM will decrease. When programming voltage is applied to the gate terminal of the bottom QDNVM, the charge will be transferred to the QDs in the gate region. The stored charge in the QDs will decrease the effective gate voltage. As a result, the threshold voltage of the lower QDNVM will increase and it will turn on for comparatively higher-input gate voltage. The transfer characteristics of the comparator based on conventional NVM and QDNVM are shown in Figs. 7*a* and *b*, respectively. The resolution of QDNVM-based comparator is more than conventional MOSFET-based comparator because of the discrete charge stored in the QDs in the gate region of the QDNVM. The bottom QDNVM threshold voltage, as well as the comparator crossover point, can be changed precisely using different programming voltages for the bottom QDNVM. This property of the comparator increases the resolution of the analogue-to-digital converter and decreases the quantisation error.

The charge is injected from the channel to the floating gate by hot electron injection mechanism. In this method, 10 V pulse is applied in the drain of the QDNVM ($W/L = 10/3.3$) for 20 µS and a gate–source (V_{GS}) of 12 V which produces a threshold voltage change of around 1.5 V. The device is erased first with 1 µS erase pulse between source and a gate region. Then, the device is programmed with the gate and drain pulse for a different amount of time. The erase and programming are done repeatedly to check the stability of the device. Even after 1.5 years, the device holds the data properly (Fig. 7*c*).

6. Process variations: The QDNVM is a modified version quantum dot gate FET (QDGFET) which is used for ternary logic generation. The presence of Si_3N_4 layer in the gate region of the QDNVM makes their characteristic more stable than QDGFET. In this section, the process variations for different parameters in two different technologies are shown in Fig. 8. The delay variation with device length deviation is shown in Fig. 8*a*, which shows less variation for QDNVM than QDGFET. A similar effect is observable for oxide thickness in the gate region (Fig. 8*b*). The maximum energy variation with gate oxide thickness for different technologies is shown in Fig. 8*c*. The QDNVM devices are less sensitive to process variation than QDGFET. The stable nature of this device is very useful for advanced circuit design and fabrication using QDNVM.

7. Conclusion: In this Letter, the fabrication of compact comparator using QDNVM is demonstrated. The controllable threshold voltage of the QDNVM is very useful to control the crossover point of the designed comparator. Preliminary data shows the reference voltage of the comparator can be controlled by controlling the threshold voltage of the QDNVM in the circuit, which depends on different controllable parameters. The comparator can be fabricated using a conventional CMOS process. Finally, the process variation of the QDNVM shows that they are more stable in silicon process compared with other similar devices. The retention data shows that the comparator behaves similarly even after 1.5 years or 18 months. Successful comparator fabrication with flexible crossover point by using conventional CMOS process will help to design and fabricate other advanced circuits in the future.

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