


Si/SiC heterojunction lateral double-diffused metal oxide semiconductor field effect transistor with breakdown point transfer (BPT) terminal technology

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A novel silicon (Si) on silicon carbide (SiC) lateral double-diffused metal oxide semiconductor field effect transistor with deep drain region is proposed. Its main idea is transferring the breakdown point and utilising the high critical electric field of SiC material to suppress the curvature effect of the drain, which eventually alleviates the trade-off relationship between breakdown voltage (BV) and specific on-resistance ($R_{on,sp}$). Through the TCAD simulation, the results show that the BV is significantly improved from 240 V for conventional Si lateral double-diffused metal oxide semiconductor (LDMOS) to 384 V for the proposed structure with the drift region length of 20 μm , increased by 60%. The figure-of-merit of the conventional Si LDMOS and the Si/SiC LDMOS are 2.04 and 4.26 MW/cm^2 , respectively. It indicates that the proposed structure has better performance than the Si counterpart. The influences of design parameters and interfacial charges on the device performance are also discussed in this work.

1. Introduction: Lateral double-diffused metal oxide semiconductor field effect transistor (MOSFET), whose electrodes are located on the surface of the device, is easier to integrate with other devices and peripheral circuits compared with vertical double-diffused MOSFET [1]. There is a trade-off relationship between specific on-state resistance ($R_{on,sp}$) and breakdown voltage (BV), which sets a silicon (Si) limit on conventional Si lateral double-diffused metal oxide semiconductor (LDMOS) [2]. To further optimise the device performance, the reduced surface field (RESURF) technology and other structures based on it are proposed in order to design high-voltages and low on-resistance Si LDMOS [3–9]. However, efforts of improving Si power devices are always limited by the low critical electric field of Si, which gives an opportunity for the development of silicon carbide (SiC) devices. SiC material has the characteristics of wide bandgap, high-thermal conductivity and a critical electric field about 10 times that of the Si [10]. Nevertheless, SiC power devices suffer from gate oxide reliability and some difficulties in manufacturing processes such as the diffusion of impurity and the realisation of high-quality ohm contact [11]. Moreover, manufacturing SiC devices is much more costly compared with Si devices. The successful fabrication of Si/SiC substrates offers a practical approach to solve these problems [12–16].

Therefore, in this Letter, a Si/SiC LDMOS with a deep drain region is proposed. Compared with the conventional Si LDMOS, the proposed structure combines the advantages of the Si and the SiC materials. The active area of the Si/SiC LDMOS is fabricated by traditional Si manufacturing processes. The SiC substrate is expected to endure high-electric field with breakdown point transfer (BPT) technology [11, 17], and served as a heatsink in a Si-based integrated circuit at the same time [10]. With the deep drain region, the combination of Si and SiC optimises the electric field distribution of the LDMOS, thereby improving the device performance.

2. Device structure and description: The cross-section of the proposed Si/SiC LDMOS with the deep drain region is shown in Fig. 1. Different from the conventional Si LDMOS, the proposed device uses a SiC substrate while the active area of the device is formed in a Si epitaxial layer. Moreover, the doping depth of the drain region is deepened down to the SiC substrate. When the

conventional Si LDMOS is in reverse mode, the curvature effect causes an electric field to crowd around the drain and makes the device break down at the cylindrical edge [18]. After the deep drain region structure is employed, the high-electric field around the cylindrical edge of the drain region is introduced into the SiC substrate so the highest electric field that the device can reach is significantly increased. In this way, the breakdown point is transferred from the cylindrical edge to the n-Si/p-SiC heterojunction, thus the BV of the proposed device is improved. Besides, there is part of the drain region involving in the vertical depletion, which facilitates the improvement of BV as well.

The key processes of fabricating the proposed Si/SiC LDMOS are presented in Fig. 2. The formation of the Si/SiC substrate can be realised by the method in [12] and the simplified wafer-bonding processes are as follows: (a) initial Si & SiC wafers to be bonded; (b) ion implantation to form the drain region in the SiC substrate and epitaxial growth of the Si substrate; (c) wafer bonding and wafer splitting. The remaining key processes are similar to those of the conventional Si LDMOS, which can be summarised as follows: (d) ion implantation to form the P-well and N-drift, (e) ion implantation to form the other part of the drain, (f) gate oxide and field oxide growth and ion implantation to form the source.

In order to investigate the characteristics of the proposed structure, 2D numerical simulations were performed by ISE TCAD. The comparison is made between the conventional Si LDMOS and the Si/SiC LDMOS with a deep drain region. The physical models in the simulation mainly include *mobility (DopingDep HighFieldsat Enormal)*, *EffectiveIntrinsicDensity (OldSlotboom)*, and *recombination (Shockley-Read-Hall (DopingDep) Auger Avalanche (Eparal))*. The device break criterion is specified as the condition when the drain current density exceeds $1 \times 10^{-7} \text{ A}/\mu\text{m}$. The parameters of 4H-SiC are used in the simulation. In Table 1, the optimal key parameters of both the devices are listed.

3. Results and discussion: Fig. 3 shows the potential distribution when the Si LDMOS and the Si/SiC LDMOS break down. Owing to the curvature effect around the drain, the Si LDMOS breaks down at a low BV of 240 V. For the Si/SiC LDMOS, the potential distribution beneath the device surface is more uniform and its potential lines still crowded around the bottom edge of the

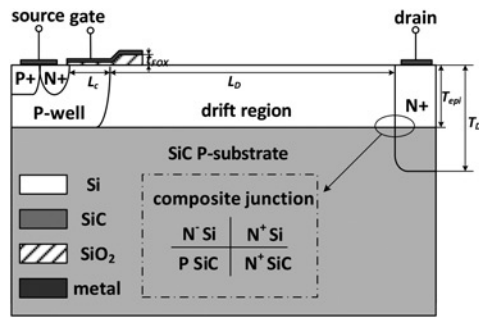


Fig. 1 Cross-section of the proposed Si/SiC LDMOS with the deep drain region

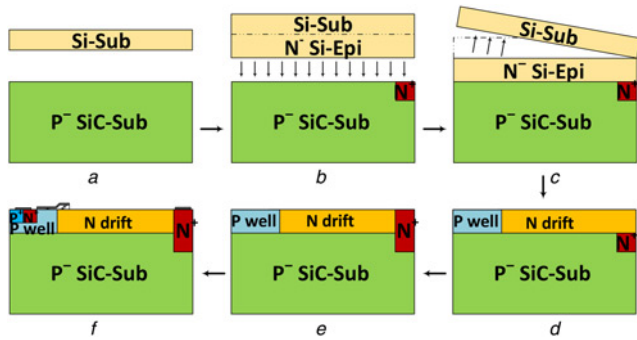


Fig. 2 Simplified key processes of fabricating Si/SiC LDMOS

Table 1 Key parameters used in device simulations

Symbol	Description	Si/SiC LDMOS	Cov. LDMOS
L_C	channel length, μm	2	
L_D	drift region length, μm	20	
t_{OX}	gate oxide thickness, nm	50	
t_{FOX}	field oxide thickness, nm	500	
T_{epi}	epitaxial layer thickness, μm	3	
T_D	drain region depth, μm	6	1
N_D	drift region doping, cm^{-3}	9×10^{15}	1.2×10^{16}
N_{sub}	substrate doping, cm^{-3}	2.8×10^{14}	

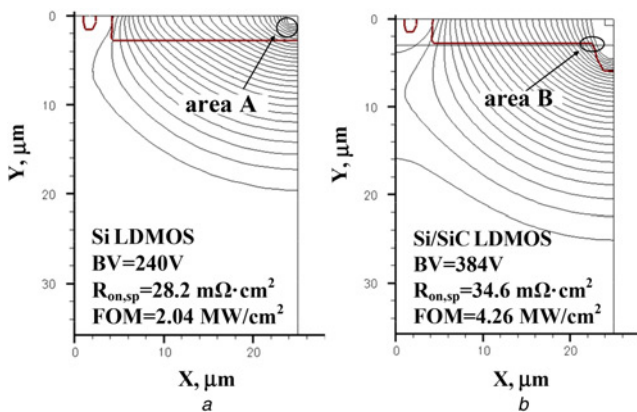


Fig. 3 Potential distribution at breakdown of
a Si LDMOS
b Si/SiC LDMOS. The left side of the devices is the source and the right side is the drain

drain but inside the SiC substrate, shown in area B in Fig. 3b. On the one hand, the introduction of the deep drain region reduces the curvature around the cylindrical edge [18] and the maximum

electric field is transferred from the Si epitaxial layer to the SiC substrate. On the other hand, the depletion area that sustains applied voltage is further extended to the SiC substrate. Therefore, the BV of the proposed LDMOS is significantly improved to 384 V.

The electric field distributions of the optimised Si LDMOS and Si/SiC LDMOS are compared in Fig. 4. Both the devices have U-shaped lateral surface electric field distributions due to the RESURF principle, as shown in Fig. 4a. The proposed structure modulates the electric field contributing to a more uniform and enhanced surface distribution. However, when the reverse voltage reaches BV, the maximum electric field in the SiC substrate has not reached its critical electric field (3.0×10^6 V/cm). Owing to the lower critical electric field of Si (3.5×10^5 V/cm), breakdown points are still inside Si epitaxy and located both around the drain and near the gate field plate. The former contributes more as is discussed in [18].

The drain region depth has an impact on device performance. As is seen in Fig. 4b, with the increased T_D , the vertical electric field peak gets higher, which coincides with the initial growth trend of BV in Fig. 5. The electric field modulation in the proposed structure is mainly related to the extent to which the drain penetrated into the SiC substrate. When T_D is around 3–4 μm , the maximum electric field around the drain is still in the Si epitaxial layer so the electric field modulation effect is not prominent. With T_D increasing, the maximum electric field shifts towards the SiC substrate so the breakdown occurs at a higher voltage. However, when $T_D \geq 6 \mu\text{m}$, there is a slightly downward trend of BV. The shift of both lateral and vertical peaks in Fig. 4 demonstrates that lateral diffusion of the drain becomes more serious with the increased T_D . Since the drain region is intended for ohmic contact, it usually does not participate in depletion. Therefore, the reduction in depletion region results in little improvement in BV although the maximum electric field gets higher with the increased T_D . As is shown in Fig. 5, the Si/SiC LDMOS have the same BV when $T_D = 6$ and 8 μm .

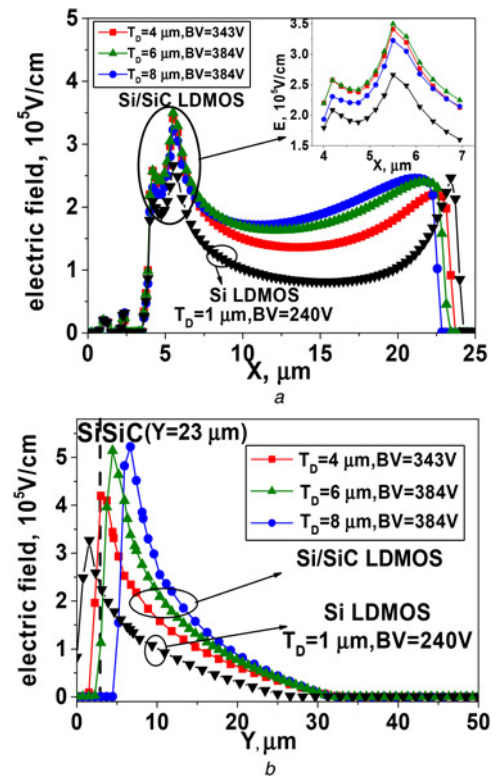


Fig. 4 Electric field distributions of the optimised Si LDMOS and Si/SiC LDMOS

a Optimised lateral electric field
b Optimised vertical electric field distribution as a function of T_D

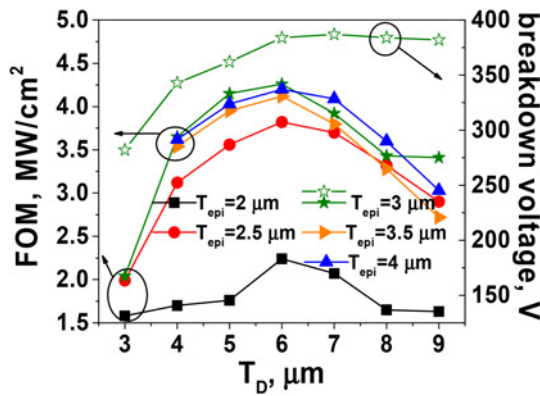


Fig. 5 Variation in FOM and BV with T_D of Si/SiC LDMOS

The influence of T_D can also be assessed by figure of merit ($FOM = BV^2/R_{on,sp}$ [8]). In Fig. 5, when $T_{epi} = 3 \mu m$ and $T_D > 6 \mu m$, FOM declines drastically with T_D . Therefore, a very deep T_D is unnecessary.

The influence of epitaxial layer thickness (T_{epi}) on BV is also investigated. In Fig. 5, when $T_{epi} = 2 \mu m$, the superiority of the proposed structure barely exhibited, but when $T_{epi} \geq 2.5 \mu m$, the FOMs for the same T_D are close. In Fig. 6, for each T_D , the BV of the Si/SiC LDMOS begins to decline after the initial growth reaching an optimal value. As is discussed above, the electric modulation effect of BPT is concerned with the drain region that is inside the SiC substrate, which determines whether the location of the maximum electric field is inside the SiC substrate. In brief, a deeper T_D may imply a larger BV to some degree. Therefore, the variation of BV with the T_{epi} of the Si/SiC LDMOS differs from those of the conventional Si counterpart, since the increased T_{epi} can be treated as the decreased T_D . It indicates that the proposed structure does not require a very thick epitaxial layer to achieve better performance.

For LDMOS, usually, BV increases with the growth of drift region length (L_D) until it reaches a saturated BV, as shown in Fig. 7. The proposed Si/SiC LDMOS has a steeper slope of BV compared with the Si counterpart. Since it can modulate both the lateral and vertical electric field, a more uniform electric field distribution can be obtained. In this way, the saturated BV of LDMOS has been broken by the deep drain region [19]. Although the Si/SiC LDMOS can obtain a higher BV, its $R_{on,sp}$ is slightly larger than the Si counterpart. Moreover, as the L_D increases, $R_{on,sp}$ grows rapidly as well. Therefore, it is important to choose the drift region length reasonably.

According to previous experimental results [20, 21], the Si/SiC interfacial charges are introduced during the direct bonding process. In the simulation, the influence of acceptor-like traps at the Si/SiC interface is investigated in Fig. 8. When the interfacial

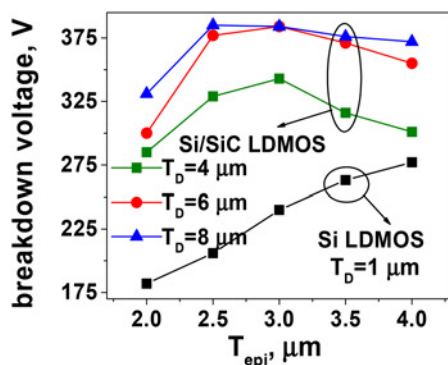


Fig. 6 BV as a function of T_{epi} with different drain region depths

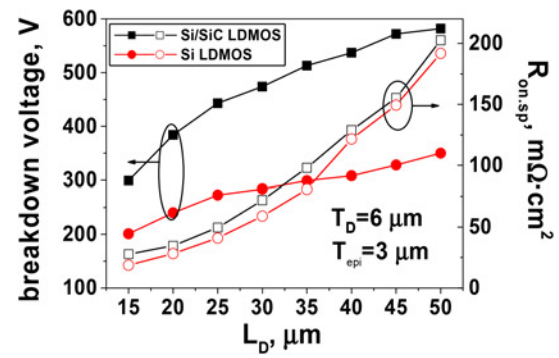


Fig. 7 BV and $R_{on,sp}$ as a function of L_D . $R_{on,sp}$ is achieved @ $V_{gs} = 10 V$, $V_{ds} = 20 V$

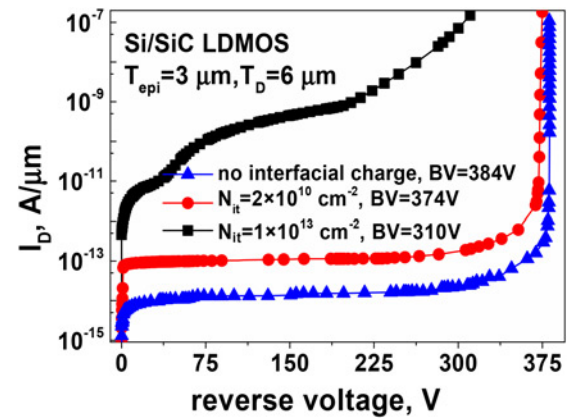


Fig. 8 Reverse I - V characteristics of the Si/SiC LDMOS with different concentrations of interfacial charges

charge is small ($2 \times 10^{10} \text{ cm}^{-2}$), the off-state performance of the proposed Si/SiC LDMOS slightly degrades. However, when $N_{it,acceptor-like} = 1 \times 10^{13} \text{ cm}^{-2}$, BV is reduced from 384 to 310 V and the leakage current is significantly increased. Owing to the trapped electrons, the electric field near the interface is increased, causing the early breakdown and high leakage. Further work should focus on improving the interfacial properties of the bonded Si/SiC wafers.

4. Conclusion: In this Letter, a novel Si/SiC LDMOS with a deep drain region has been proposed. The Si epitaxial layer and SiC substrate are associated with the deep drain region, which facilitates the transfer of breakdown point and modulates electric field distribution at the same time. Compared with the conventional Si LDMOS, the Si/SiC LDMOS alleviates the trade-off between BV and $R_{on,sp}$. The BV is improved from 240 to 384 V with the same drift region length. After analysing the influence of design parameters on the BV, the proposed LDMOS obtains its best performance when $T_D = 6 \mu m$ and $T_{epi} = 3 \mu m$. In addition, the Si/SiC interfacial charge has a negative effect on the device performance. Further improvement of the interfacial quality is needed for the realisation of the Si/SiC LDMOS.

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6 References

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