TCAD simulation of a double L-shaped gate tunnel field-effect transistor with a covered source–channel

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In this work, the authors propose and simulate a double L-shaped gate tunnel field-effect transistor (DLG-TFET) with the covered source–channel. The proposed structure improves the ON-state current by increasing the linear tunnelling area and has excellent subthreshold characteristics. The simulation focuses on the performance improvement of the device under different longitudinal gate length L_g, interlayer silicon thickness T_{si}, gate and source overlap length L_{ov}, and covered source depth L_s. For optimal parameters, the ON-state current of the proposed DLG-TFET increases up to 3.53×10^{-5} A/μm, and the current switch ratio(I_{on}/I_{off}) is 4.28×10^{11} at room temperature, moreover, a minimum subthreshold swing (SSmin) and an average subthreshold swing (SSave) are as low as 32.2 and 52.9 mV/Dec, respectively. Meanwhile, this work uses mixed device-circuit simulations to predict the performance of the inverter circuit implemented with proposed DLG-TFET.

1. Introduction: A tunnelling field-effect transistor (TFET) has become a kind of promising candidate for the ultra-low power consumption applications in the nanoscale circuit because of overcoming a limitation of 60 mV/Dec subthreshold swing (SS) [1–8]. However, band-to-band tunnelling (BTBT) is the main working mechanism in TFETS [9–16], which leads to an inherent disadvantage in terms of ON-state current [17–28].

Different types of structures have been proposed to solve ON-state current issue in recent years, such as L-shaped channel TFET (LTFET) [14, 17], U-shaped channel TFET (UTFET) [1], symmetric tunnel field-effect transistor (S-TFET) [21], U-shaped channel with dual sources TFET (DUTFET) [22], covered source–channel tunnel field-effect transistors (CSC-TFETs) [6], heterojunction tunnel field-effect transistor with T-shaped gate (HTG-TFET) [9], and so on. In general, all these works attempt to improve the ON-state current of TFETs by using new structures [11–15], new materials [12], alloy engineering, or heterojunctions [23].

In this Letter, we propose a novel structure of a double L-shaped gate tunnel field-effect transistor (DLG-TFET) with the covered source–channel to increase the ON-state current in all silicon conditions. Consequently, in theory, the proposed structure can generate higher ON-state current and realise higher I_{on}/I_{off} ratio; at the same time, it retains a steep SS within a large gate voltage range. Synopsys Sentaurus simulation results also show that DLG-TFET has high ON-state current and low OFF-state current and steep SS compared with CSC-TFET. We will discuss details in the following sections, Section 2 presents the basic structure of the new device and simulation models used in this Letter, Section 3 includes the properties of the structure and the optimisation process, Section 4 summarises the Letter and makes some relevant statements.

2. Device structures: As we know, increasing the tunnelling area is an effective method to enhance the ON-state current, both LTFET and UTFET follow this principle by transforming BTBT from point tunnelling to linear tunnelling. Traditional covered source–channel tunnel field-effect transistor (CSC-TFET) with a trench gate structure also exhibits a remarkably increased ON-state current owing to the enhanced tunnelling area, which schematic diagram is shown in Fig. 1*a*, where the tunnelling current varies with T_{si} and L_T. In order to obtain large current, T_{si} should be small (not be <1 nm,) and L_T should be long (has an optimal value), at the same time, the change of L_s has no effect on the current in this structure. Based on the basic CSC-TFET, an optimised structure is proposed in Fig. 1*b*, where an additional depth-controlled L-shaped gate in the body is created to further increase the linear tunnelling current, as a result, the gate that controls the tunnelling current in the new structure resembles two vertically flipped and head to the tail alphabet 'L'. Similar to CSC-TFET, the tunnelling current still varies with T_{si} and L_T, and as expected, the tunnelling current increases with L_s under L_g stays constant and L_s is less than L_g.

The key process steps of the proposed DLG-TFET are as follows: first, the p+ source region is recessed into the Si substrate and is grown by epitaxy. Second, the covered source is realised by implantation. Afterwards, the trench whose edge resembles two vertically flipped and head-to-tail alphabet 'L' is etched, and the gate dielectric and gate conductor are deposited and patterned. Finally, the n+ drain region is formed by ion implantation.

The proposed device is Si-based in the simulation, and the parameters used for simulation are listed in Table 1.

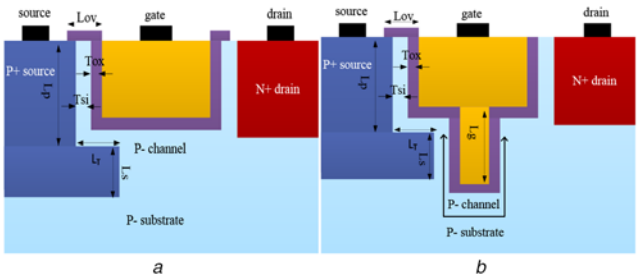

Fig. 1 *Schematic diagram of*
a CSC-TFET
b Proposed DLG-TFET with the covered source–channel

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Table 1 Device parameters used for simulations

longitudinal gate length (L_g)	13–29 nm	depth of covered source (L_s)	15–24 nm
width of covered source (L_T)	14–20 nm	depth of source (L_p)	30 nm
gate oxide thickness (T_{ox})	2 nm	source doping concentration	1×10^{20} cm^{-3}
gate and source overlap region length (L_{ov})	5–23 nm	drain doping concentration	1×10^{18} cm^{-3}
interlayer silicon thickness (T_{si})	2–7 nm	channel doping concentration	1×10^{15} cm^{-3}

Simulations are carried out in Synopsys Sentaurus. To consider the band-to-band tunnelling phenomenon in the case of TFET and the spatial variation of the energy bands, the nonlocal BTBT model is used, Shockley–Read–Hall related to concentration, Fermi statistics, the doping dependent mobility (CONMOB) model and bandgap narrowing (BGN) model are also used.

3. Simulation and discussion: To compare the performance of the proposed device and CSC-TFET, we adopt the same parameters in our simulation. Figs. 2*a* and *b* show the difference of tunnelling area and footprint between CSC-TFET and DLG-TFET. It can be seen obviously that the tunnelling area of DLG-TFET is larger than CSC-TFET due to a double L-shaped gate, resulting in the total current of CSC-TFET is less than DLG-TFET. Fig. 3*a* indicates the total current of CSC-TFET and DLG-TFET at 3 V gate-to-source voltage (V_{gs}) and 2.0 V drain-to-source voltage (V_{ds}), it is not difficult to find that the proposed DLG-TFET has larger ON-state current than CSC-TFET, and ON-state current of DLG-TFET and CSC-TFET are 2.84×10^{-5} and 1.59×10^{-5} A/μm in this condition, respectively. At the same time, we also add the transfer characteristics of LTFET [16] in Fig. 3*a* to provide a contrast with traditional TFETs, it can be found from Fig. 3*a* that the total current of LTFET at 3 V V_{gs} is only 1.48×10^{-6} A/μm.

The comparison of CSC-TFET and DLG-TFET based on Fig. 3*a* is illustrated in Table 2. As can be seen clearly from Table 2 that the I_{on}/I_{off} ratio of DLG-TFET can still be reached to 10^{11}, more importantly, SSmin of DLG-TFET is 41.4 mV/Dec at 0.6 Vgs, and SSave of DLG-TFET extracted from $V_{turn\text{-}on}$ to V_t ($V_{turn\text{-}on}$ is the gate voltage at which tunnelling occurs the first time, and V_t is the gate voltage at which drain current becomes 1×10^8 A/μm) is 55.3 mv/Dec, what's more, I_{off} of DLG-TFET is only 7.96×10^{-17} A/μm. In terms of overall performance, the proposed structure is superior to CSC-TFET, on the one hand, this is because that tunnelling area under ON-state condition is determined by the sum of L_T, L_s and L_p, on the other hand, the small value of OFF-state current and subthreshold swing owes to the large electron diffusion length in the new structure.

Fig. 3*b* shows the transfer characteristics of DLG-TFET with different T_{si}. It can be seen clearly that the maximum ON-state current gradually decreases from 3.53×10^{-5} to 8.06×10^{-6} A/μm with the increase of T_{si} (from 2 to 7 nm), and the transfer characteristics curve starts to display a downward inflection point at 6 nm which

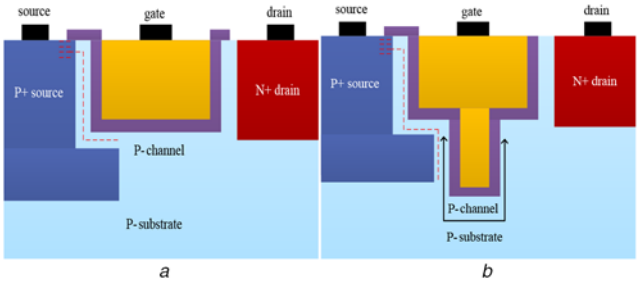

Fig. 2 *Tunnelling area and footprint comparison between*
a CSC-TFET
b DLG-TFET

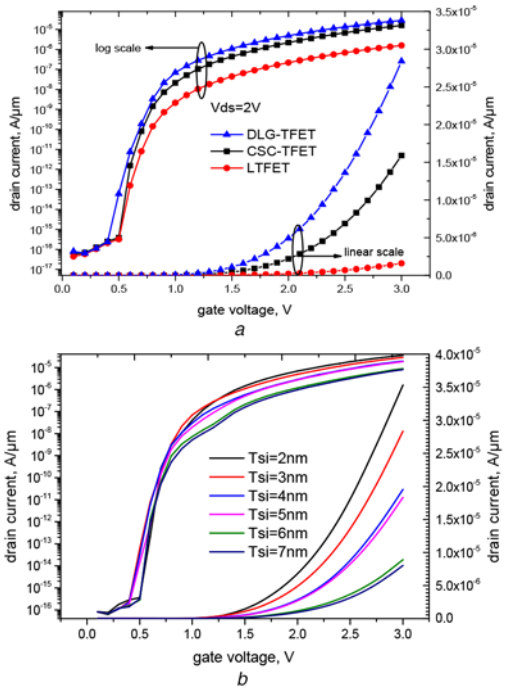

Fig. 3 *Transfer characteristics of*
a Transfer characteristics of LTFET, CSC-TFET and DLG-TFET with the same $L_p = 30$ nm, $L_T = 18$ nm, $L_s = 24$ nm and $T_{si} = 3$ nm
b Transfer characteristics of DLG-TFET with different T_{si}

Table 2 Comparison of CSC-TFET and DLG-TFET

Device	CSC-FET	DLG-TFET
$V_{turn\text{-}on}$, V	0.4	0.4
I_{on}, A/μm	1.59×10^{-5}	2.84×10^{-5}
I_{off}, A/μm	5.46×10^{-17}	7.96×10^{-17}
I_{on}/I_{off}	2.91×10^{11}	3.57×10^{11}
SSmin, mV/Dec	52.7	41.4
SSave, mV/Dec	71	55.3

is not desirable. The reason for the previous, current change in characteristics curve is that the tunnelling probability decreases as T_{si} increases and increasing thickness of interlayer silicon makes depleted region widen between source and channel. By considering the three aspects of maximum ON-state current, SS and OFF-state current, T_{si} is selected 2 nm as the optimal value, and the transfer characteristics curve will obviously deteriorate when T_{si} is larger than 5 nm. The ON-state current and OFF-state current of $T_{si} = 2$ nm are $3.53 \times 10^{-}$ and 8.27×10^{-17} A/μm, respectively, SSave and SSmin are 52.9 and 32.2 mV/Dec, the ratio of I_{on}/I_{off} is 4.28×10^{11}, respectively.

Figs. 4*a* and *b* show the variations of ON-state current, I_{on}/I_{off} ratio, SSave and SSmin with different T_{si}. As depicted in Figs. 4*a* and *b*, the ON-state current decreases from 3.53×10^{-5} to 8.06×10^{-6} A/μm, the ratio of I_{on}/I_{off} decreases from 4.28×10^{11}

to 9.82×10^{10}, the SSave increases from 52.9 to 92 mV/Dec, and SSmin increases from 32.2 to 53 mV/Dec.

Fig. 5*a* shows the influence of L_g on transfer characteristics with keeping $L_s = 15$ nm and $V_{ds} = 2$ V, it can be found through the observation of Fig. 5*a* that the ON-state current of the proposed structure at $L_s = 15$ nm decreases by order of magnitude to 9.43×10^{-6} A/μm when $L_g = 13$ nm, while the ON-state current stays at the order of 10^{-5} A/μm when L_g is >13 nm. Moreover, the ON-state current of DLG-TFET increases with the increase of L_g before 27 nm, and the ON-state current starts to saturate when L_g is larger than 27 nm. The ON-state current of $L_g = 27$ and $L_g = 29$ nm are 1.816×10^{-5} and 1.816×10^{-5} A/μm, respectively, which can be observed from Fig. 5*a* and further explains the fact that the current will be saturated after $L_g = 27$ nm. Fig. 5*b* shows the variation of I_{on} and SSave with different L_g, it can be noticed

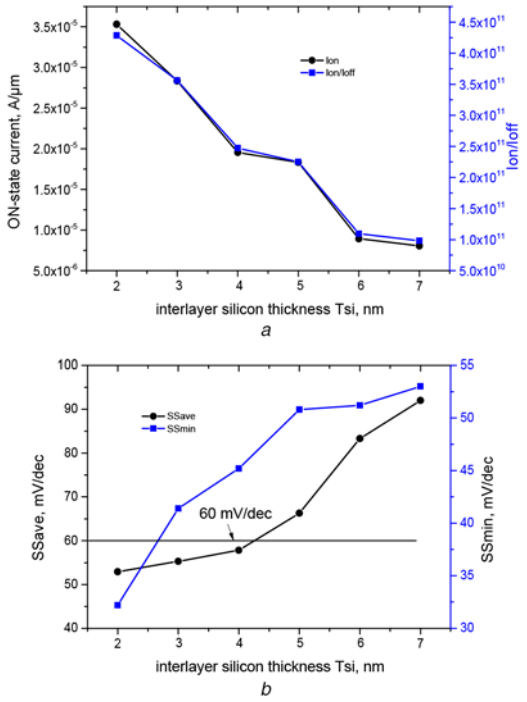

Fig. 4 *Variation of*
a Variation of I_{on} and I_{on}/I_{off} with different T_{si}
b Variation of SSave and SSmin with different T_{si}

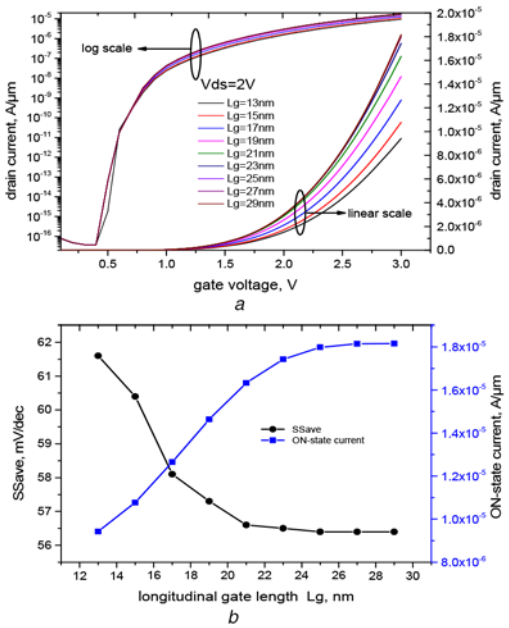

Fig. 5 *Transfer characteristics of*
a Transfer characteristics of DLG-TFET with different L_g
b ON-state current and SSave with different L_g

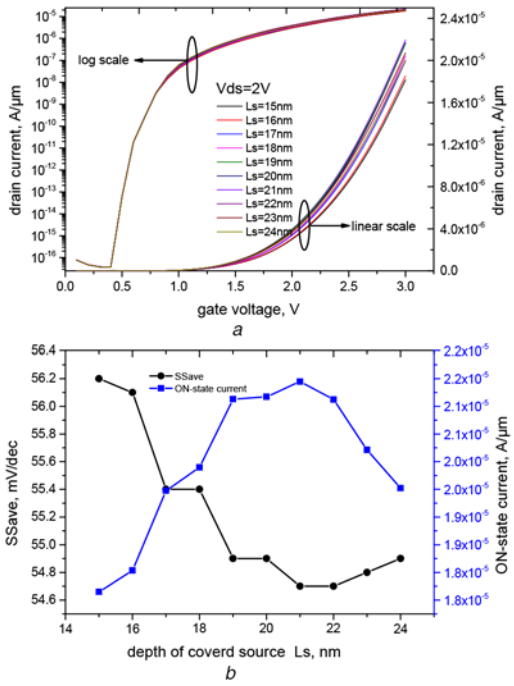

Fig. 6 *Transfer characteristics of*
a Transfer characteristics of DLG-TFET with different L_s
b ON-state current and SSave with different L_s

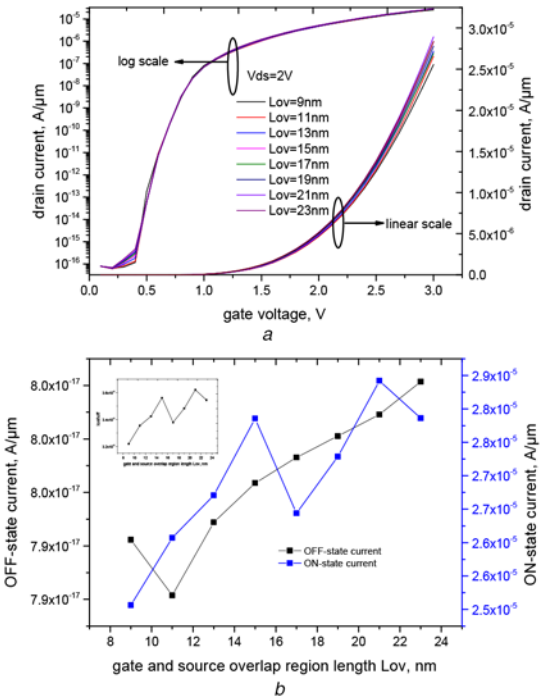

Fig. 7 *Transfer characteristics of*
a Transfer characteristics of DLG-TFET with different L_{ov}
b ON-state current and OFF-state current with different L_{ov}

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clearly in the diagram that I_{on} goes from 9.43×10^{-6} to 1.816×10^{-5} A/μm and SSave becomes greater than 60 mV/Dec when $L_g < 15$ nm and tends to saturate to 56 mV/Dec when $L_g > 19$ nm.

Fig. 6*a* shows the impact of L_s on transfer characteristics with keeping $L_g = 27$ nm and $V_{ds} = 2$ V, it is easy to see that the current of DLG-TFET increases with the increase of L_s before 21 nm, and the current begins to decrease when L_s is larger than 21 nm, this is because that covered source will generate a small amount of current on the left side of its right bottom corner which will get smaller and smaller as the length of L_s approaches or exceeds the length of L_g, this phenomenon is represented by the curves of $L_s = 22$ nm, $L_s = 23$ nm and $L_s = 24$ nm in Fig. 6*a* and affected by the distribution of electric field intensity at the right bottom corner of the covered source. Fig. 6*b* shows the variation of I_{on} and SSave with different L_s, it can be seen clearly in this diagram that the maximum I_{on} and minimum SSave are 2.19×10^{-5} A/μm and 54.7 mV/Dec at $L_s = 21$ nm, I_{on} increases and SSave decreases with the increase of L_s before 21 nm, after that, I_{on} decreases and SSave increases with the increase of L_s.

Fig. 7*a* shows the impact of L_{ov} on transfer characteristics with keeping $L_g = 27$ nm, $L_s = 21$ nm and Vds = 2 V, as can be clearly found from Fig. 7*a* that the SSave is almost unaffected by L_{ov}. However, ON-state current, OFF-state current and I_{on}/I_{off} increase with the increase of L_{ov}, and the maximum ON-state current varies from 2.55×10^{-5} to 2.89×10^{-5} A/μm when L_{ov} changes from 9 to 23 nm. Fig. 7*b* shows the variation of ON-state current, OFF-state current and I_{on}/I_{off} ratio with different L_{ov}, in Fig. 7*b*, it is very clear that ON-state current increases with the increase of L_{ov} on the whole and has a maximum value of 2.89×10^{-5} A/μm at $L_{ov} = 21$ nm and changes periodically every 6 nm because of the double action of transverse electric field and longitudinal electric field. While the OFF-state current has a minimum value at $L_{ov} = 11$ nm and increases with the increase of L_{ov} after $L_{ov} = 11$ nm, the inserted graph in Fig. 7*b* indicates the changes of I_{on}/I_{off} ratio of DLG-TFET which has the same trend with ON-state current and has a maximum value of 3.62×10^{11} at $L_{ov} = 21$ nm.

Finally, it is necessary to verify the circuit-level AC performance of DLG-TFET in order to adapt for logic applications [25–28]. To make a complementary TFET inverter in our simulation, we adopt the same parameters for n-type and p-type DLG-TFETs.

Fig. 8*a* shows the transfer characteristics of n-type and p-type DLG-TFETs with different gate voltages, as can be seen from this figure that maximum current of n-type and p-type DLG-TFETs is 3.53×10^{-5} and 3.12×10^{-5} A/μm at $V_{gs} = 3$ V and $V_{gs} = -3$ V, respectively. Fig. 8*c* shows the transient characteristics curve of an inverter for DLG-TFET which are simulated at different load capacitance (0.01, 0.1, 1 and 10 fF) under an input step signal (V_{in}) with a peak voltage of 1.0 V and arising/falling time of 5 ns. Apparently, overshoot/undershoot voltage will occur on the simulated output signals at the points of input voltage transitions due to the process of capacitor charge and discharge. Moreover, the value of overshoot/undershoot voltage is decided by external load capacitance, it can be observed that overshoot/undershoot voltage increases with the decrease of load capacitance, and internal parasitic capacitance is relatively large on account of two vertically flipped and head to tail L-shaped gate which has an important impact on the overshoot/undershoot voltage, as shown in Fig. 8*b*. Fig. 9*a* shows the variation of overshoot and undershoot voltage as a function of load capacitance, consistent with the previous analysis, whose absolute values decrease as the load capacitance increases from 0.01 to 10 fF.

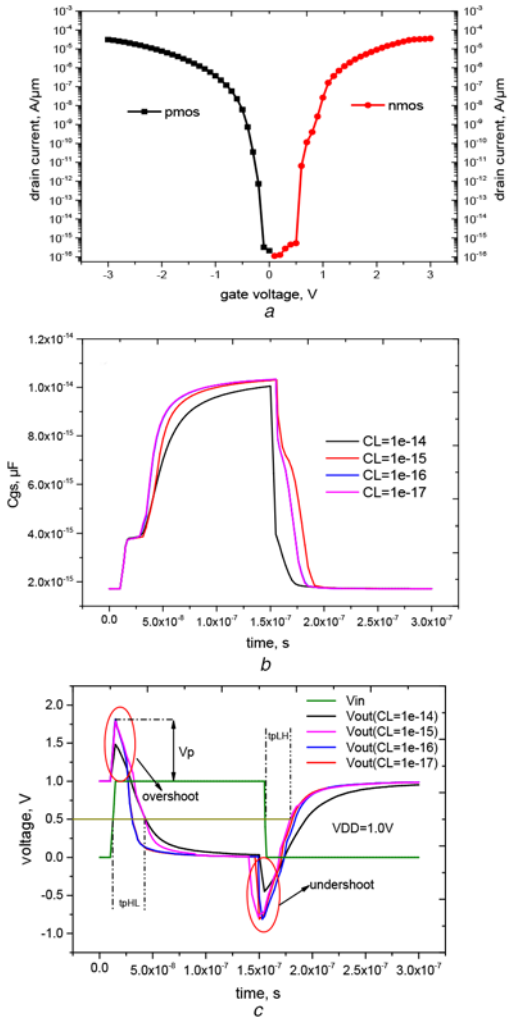

Fig. 8 *Transfer characteristics of*
a Transfer characteristics of n-type and p-type DLG-TFETs with different gate voltages
b Gate-to-source capacitance (C_{gs}) for different load capacitance with different time
c Transient response characteristics of DLG-TFET

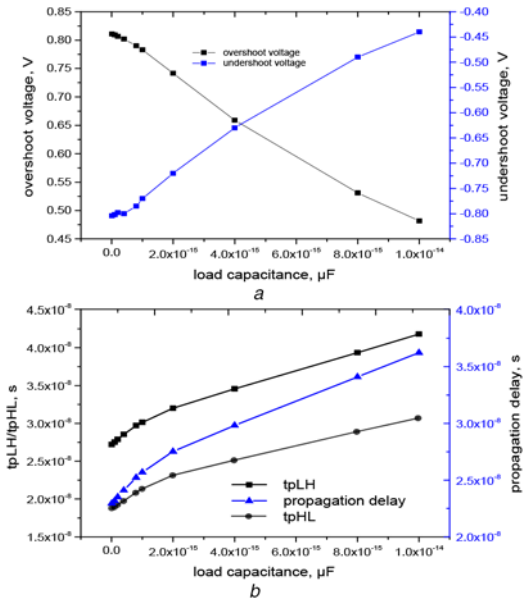

Fig. 9 *Value of*
a Value of overshoot voltage and undershoot voltage
b Value of propagation delay as a function of load capacitance for DLG-TFET

Propagation delay t_P is defined as the average of t_{PHL} and t_{PLH} for the inverter circuit, which is the time interval between 50% of the input voltage and 50% of the output voltage in the transient response as illustrated in Fig. 8*b*. Fig. 9*b* shows the propagation delay as a function of load capacitance for DLG-TFET, as shown in Fig. 9*b* that the DLG-TFET exhibits a propagation delay which decreases with the decrease of load capacitance, and the value of t_P is 3.62×10^{-8} s at 10 fF and 2.29×10^{-8} s at 0.01 fF, respectively.

4. Conclusion: Important conclusions arrived at based on the Letter are the following:

- The proposed DLG-TFET has an ON-state current of 3.53×10^{-5} A/μm, and has an I_{on}/I_{off} current ratio of $\sim 10^{12}$ at room temperature.

- A minimum subthreshold swing SSmin = 32.2 mV/Dec and an average subthreshold swing SSave = 52.9 mV/Dec.

- The transient characteristics of inverter for DLG-TFET are simulated and propagation delay t_P are compared under different load capacitance, our inverter shows overshoot/undershoot voltage on the simulated output signals at the points of input voltage transitions and overshoot/undershoot voltage increases with the decrease of load capacitance, what's more, propagation delay t_P decreases with the decrease of load capacitance, and the value of t_P is 3.62×10^{-8} s at 10 fF and 2.29×10^{-8} s at 0.01 fF, respectively.

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