AC-SJ VDMOS with ultra-low resistance

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An accumulation superjunction (AC-SJ) vertical power metal–oxide–semiconductor field-effect transistor (VDMOS) is proposed and its mechanism is investigated. Different from the conventional VDMOS, a number of carriers are accumulated and modulate the conductivity of the drift region when the AC-SJ VDMOS works in the on-state. The causes of carrier AC and the factors affecting the amount of carrier are analysed. The influences of these factors on the output characteristics are studied by simulation. Simulation results show that the on specific resistance ($R_{on,sp}$) of the AC-SJ VDMOS decreases from 6.64 mΩ cm^2 of the conventional VMOS to 1.53 mΩ cm^2 with the same drift region length of 15 μm. The AC-SJ VDMOS obtains very low $R_{on,sp}$ by accumulating electrons while maintains high breakdown voltage due to SJ theory, thereby breaking the SJ limit in silicon.

1. Introduction: The vertical power metal–oxide–semiconductor field-effect transistor (VDMOS) is a kind of important power semiconductor switching device and has a wide range of applications in power electronic system. An ideal VDMOS device should have a high breakdown voltage (BV) in off-state and a lower specific on-resistance ($R_{on,sp}$) in on-state to minimise conduction loss. However, in the conventional VDMOS device, there is a trade-off between BV and $R_{on,sp}$ called silicon limit: $R_{on,sp} = 5.93 \times 10^{-9} BV^{2.5}$ [1–3]. The trench gate structure is widely used in VDMOS manufacturing because it eliminates the junction field-effect transistor region of the VDMOS [4, 5], thus the resistance of the drift region becomes the dominant resistance in devices. An effective method for reducing the drift resistance is using superjunction (SJ) concept [6]. SJ could assist the depletion between P-pillar and N-pillar by introducing a lateral electric field in the body, thus the doping concentration of the drift region can be increased to reduce the $R_{on,sp.}$ In addition, there is another way to obtain very low drift resistance. The structure of U-shaped groove metal-oxide-semiconductor (UMOS) [7] has been fabricated by utilising deep trench structures. The resistance contribution from the drift region is reduced by the formation of an accumulation (AC) layer on the sidewalls. Moreover, several structures [8, 9] with AC layer are superior to the conventional structures. However, the blocking voltage of UMOS is limited to low voltage (<100 V) by the high electric field created in the gate oxide, which limits the application in medium- and low-voltage areas.

A novel AC-SJ VDMOS is proposed in this Letter to obtain very low $R_{on,sp}$ by utilising the idea of UMOS. The AC-SJ VDMOS extends down to the $N+$ substrate as UMOS. To avoid the breakdown in the bottom of the oxide layer in UMOS, the bottom oxide layer is replaced by PN junction in the proposed structure. There is also an electric potential difference between the oxide layers in the on-state, which accumulates the electrons in the drift region. The accumulated electrons dramatically increase the forward current.

The Sentaurus technology computer aided design (TCAD) [10] has been used to perform the characteristics of the proposed structure. The main physics models are applied mainly including of mobility (the Masetti model and the Canali model), band gap narrowing for Slotboom model, Shockley–Read–Hall, and Auger and Avalanche (Eparal) models for recombination. To verify the correctness of the model, the above models are used to simulate the structure in [11]. The simulation results are in good agreement with the experiments. Therefore, credible results can be obtained when the proposed structure is simulated with the models. The $R_{on,sp}$ of AC-SJ VDMOS is 1.53 mΩ cm^2, whereas the $R_{on,sp}$ of conventional VDMOS is 6.64 mΩ cm^2.

2. Device structure and analysis: Fig. 1*b* shows the schematic cross-section of the proposed AC-SJ VDMOS. The oxide layers extend from the bottom of gate to substrate, which separates N-pillar and P-pillar. There is a thin $N+$ region inside the P-pillar near the substrate, rather than an oxide layer in UMOS. This structure avoids the breakdown in the bottom oxide layer of UMOS. The expansion of the depletion region can undertake high reverse drain voltage. In the on-state, the PN junction (*J*2) maintains the voltage of V_{GD}, which is leading the electric potential in P-pillar to be higher than the electric potential in N-pillar, the potential difference could accumulate electrons to modulate the resistance (*R*1) of the drift region. In the off-state, the PN junction (*J*1) maintains the voltage of V_{DG} for high BV. The key parameters of the 300 V-rate devices in this simulation are listed in Table 1.

When a positive gate voltage is applied, the *J*1 junction is in the forward bias, the *J*2 junction is in the reverse bias, and the potential difference exists on both sides of the oxide layer. Therefore, electrons will be accumulated in the drift region as shown in Fig. 2. When the gate voltage is 0 V, no electrons are accumulated (not shown in this figure). When the gate voltage is 3 V, only a small amount of electrons are generated. With the increase of the gate voltage, the amount of electrons increases gradually and can be calculated by the formula below

$$Q = C_{OX} \times V \tag{1}$$

where C_{OX} is the intermediate oxide capacitor and V is the potential difference between the two sides of the oxide layer. It can be concluded that the thin oxide width should be helpful for better performance. In this simulation, the thickness of 0.1 μm oxide layer is employed for considering about the feasibility of the manufacturing process. When the gate voltage is 9 V, the accumulated surface charge density can even reach the order of 10^{18} cm^{-3}, which significantly reduces the on-resistance of the device.

The accumulated charge is dependent on the potential difference across the oxide layer, so it is related to the drain voltage. Fig. 3*a* shows the potential distribution of the AC-SJ VDMOS at different drain voltages when the gate voltage is 10 V. When the drain voltage is 0 V, electrons are generated along with the entire oxide layer as described above. When the gate voltage increases to

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Table 1 Key parameters for conventional VDMOS and AC-SJ VDMOS

Parameters	Definition	Conventional VDMOS	AC-SJ VDMOS
W, μm	half width of the pitch	4	4
T_{ox}, μm	width of the oxide layer	—	0.1
L_D, μm	length of the drift region	15	15
L_n, μm	length of the bottom $N+$ region	—	1
L_p, μm	length of the bottom P region	—	1
P_{well}, cm^{-3}	doping concentration of P well	5×10^{16}	5×10^{16}
N_n, cm^{-3}	doping concentration of drift region	1.2×10^{15}	6×10^{15}
N_p, cm^{-3}	doping concentration of P-pillar	—	6×10^{15}
$R_{on,sp}$, mΩ cm^2	specific on-resistance	6.64	1.53
BV, V	BV	262	340

40 V, the drain voltage is taken over by the $J2$ junction, and the depletion region gradually expands as the drain voltage increases. As shown in Fig. 3*b*, the dashed line is the potential along the line AA′ on the left-hand side of the oxide layer, whereas the solid line is the potential along the line BB′ on the right-hand side of the oxide layer. The area between the dashed line and solid line is the potential difference across the oxide layer.

It can be seen that the potentials between the drain and depletion line are almost the same, so there are no accumulated electrons in the depletion layer. The potential on the right-hand side of the oxide layer is the gate voltage, and the potential on the left-hand side of the oxide layer is approximately linear, so there exist accumulated electrons. With the increase of drain voltage, the depletion region gradually expands to undertake higher drain voltage. With the increase of drain voltage, the depletion region expands to the gate, the potential difference between the two sides of the oxide layer disappears gradually, and the accumulated charge disappears accordingly.

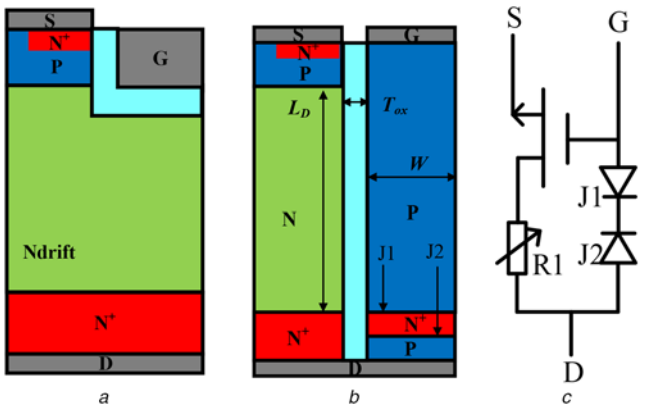

Fig. 1 *Device structure and analysis*
a Schematic cross-sections of the VDMOS structure
b Proposed AC-SJ VDMOS
c Equivalent circuits

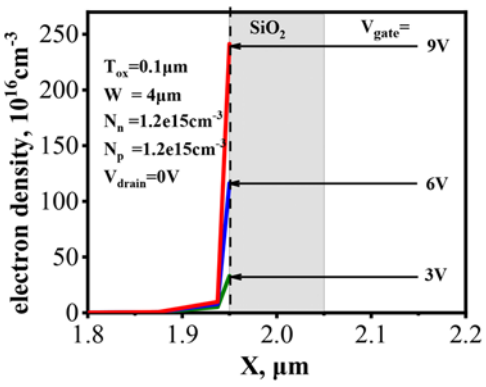

Fig. 2 *Electron density in the AC-SJ VDMOS with different gate biases (at $Y = 10$ μm)*

3. Optimisation results and discussion: Fig. 4 shows the output characteristics of the conventional VDMOS and AC-SJ VDMOS. In the conventional VDMOS, the density of current is determined by the doping concentration of the drift region. The drain current almost remains unchanged with the increase of the gate voltage when the device is turned on. In the AC-SJ VDMOS, the density of electron in drift region contains two parts. One part is generated by doping as conventional VDMOS, and the other part is accumulated by the difference of electron potential. The drain current increases with the increase of the gate voltage. To compare the effect of gate voltage on current clearly, the doping concentration of conventional VDMOS and AC-SJ VDMOS is set at 1.2×10^{15} cm^{-3}. It is noteworthy that the saturation current of AC-SJ VDMOS is still lower than that of conventional VDMOS when the gate voltage is low (3 V). The reason is the reduction of effective drift area. When the gate voltage increases

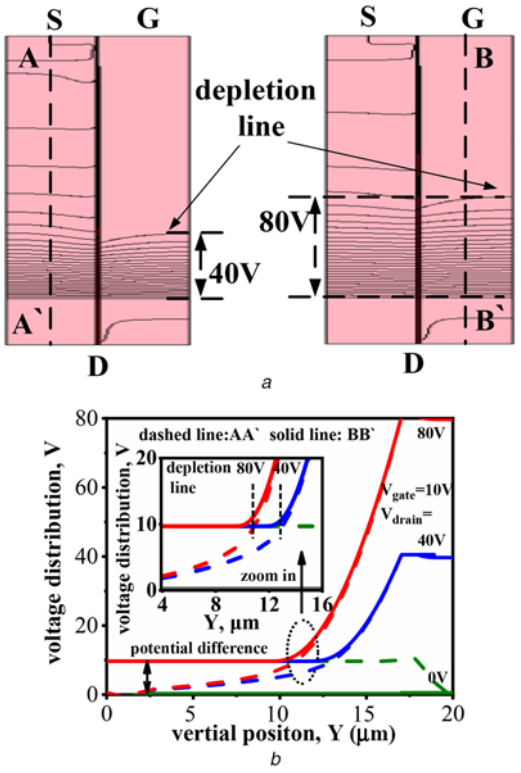

Fig. 3 *Potential distribution*
a Distribution of potential in the on-state
b Potential difference on both sides of the oxide layer

to 10 V, the accumulated electrons increase greatly and the saturation current increases by 30% compared with the conventional VDMOS.

SJ concept introduces lateral electric field in the body to assist the depletion between P-pillar and N-pillar so that the drift can be completely depleted at higher concentrations. Fig. 5 shows the relationship between the BV and $R_{on,sp}$ of the drift region as a function of drift doping concentration. To confirm the optimum concentration range, the calculated figure-of-merit curve is inserted in this figure. It can be seen that the optimum concentration range is 4–7 × 10^{15} cm^{-3}.

The reverse characteristics of the device are almost the same as that of the SJ device, and the $R_{on,sp}$ of the AC-SJ VDMOS is greatly reduced due to the accumulated charge, thus breaking the silicon limit and SJ limit. Fig. 6 compares the simulated

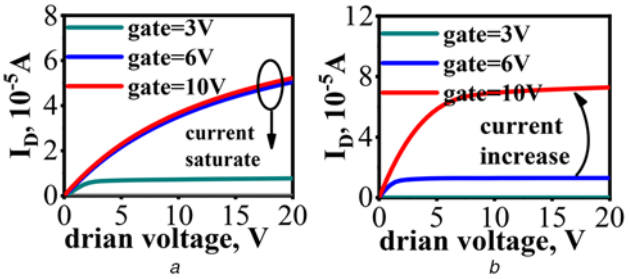

Fig. 4 *Output characteristics for*
a Conventional VDMOS (N_n = 1.2 × 10^{15} cm^{-3})
b AC-SJ VDMOS with same doping concentration ($N_n = N_p$ = 1.2 × 10^{15} cm^{-3})

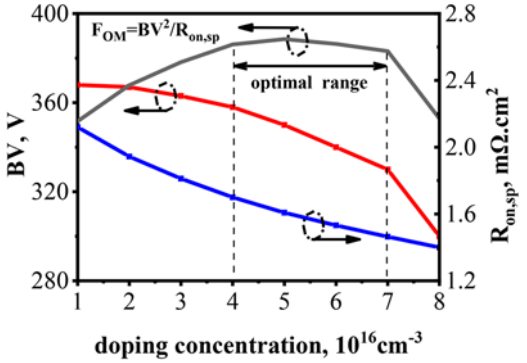

Fig. 5 *Influence of doping concentration ($N_n = N_p$) on BV and $R_{on,sp}$ of the AC-SJ VDMOS*

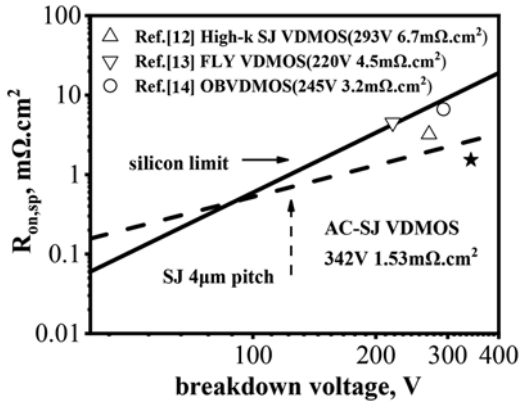

Fig. 6 *BV-$R_{on,sp}$ performance comparison of simulated AC-SJ VDMOS with silicon limit line, SJ silicon limit line and other published devices*

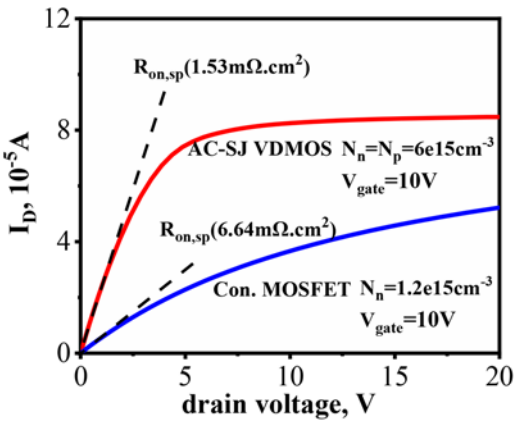

Fig. 7 *Output characteristics for the conventional VDMOS and AC-SJ VDMOS*

BV-$R_{on,sp}$ performance of the AC-SJ VDMOS with silicon limit, SJ silicon limit, and various reported SJ VDMOS structures [7–9]. It is can be seen that the $R_{on,sp}$ of AC-SJ VDMOS is obviously lower than silicon limit, simulated SJ-UMOS, SJ silicon limit, and some reported SJ VDMOS structures.

The output characteristics of the conventional VDMOS and AC-SJ VDMOS obtained by simulations are shown in Fig. 7. The saturation current of the AC-SJ VDMOS is larger than that of the conventional VDMOS. The current density of AC-SJ VDMOS is larger 50% than that of the conventional VDMOS. In addition, the $R_{on,sp}$ of AC-SJ VDMOS is 1.53 mΩ cm^2, whereas the $R_{on,sp}$ of conventional VDMOS is 6.64 mΩ cm^2 with the drift length of 15 μm, which decreases by 75%.

4. Conclusion: In this Letter, a novel AC-SJ VDMOS with ultra-low resistance is proposed. Electrons are accumulated in the walls of the oxide layer in on-state because of the electric potential difference across the oxide layer, which significantly reduces the $R_{on,sp}$. The causes of carrier AC and factors affecting the amount of carrier AC are discussed, and the doping concentration of AC-SJ VDMOS is optimised. Furthermore, the trade-off between BV and $R_{on,sp}$ of the AC-SJ VDMOS is better than SJ device (4 μm pitch), and the results are compared with other reported theory and results. The result shows that the specific on-resistance of AC-SJ VDMOS decreases about 75%, from 6.64 mΩ cm^2 of the conventional VDMOS to 1.53 mΩ cm^2.

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