

Optimal repeater insertion for nano-interconnects in current-mode signalling scheme

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The optimal design of repeaters for current-mode (CM) nano-interconnects is conducted and compared with that for voltage-mode (VM) ones. Both Cu and carbon nanotube (CNT) nano-interconnects are considered and studied, with the contact resistance treated appropriately. In comparison with the VM ones, the CM nano-interconnects can not only demonstrate better electrical performance, but also require fewer repeaters, thereby saving more valuable chip area. In the delay-optimal repeater design of multi-walled CNT interconnects, for instance, the optimal number of repeaters can be reduced by 120% with the implementation of CM signalling scheme.

1. Introduction: With the continuous advancement of CMOS technology, IC feature size is approaching the physical limit but chip area is increasing (due to the increase of functionality) [1]. Unlike transistor scaling, interconnect scaling leads to a dramatic increase in time delay, which has become a decisive factor in designs of high-performance ICs [2]. It is a necessity to explore efficient techniques to improve the electrical performance of interconnects, especially long nano-interconnects.

Current-mode (CM) signal transport techniques, which were proven to provide speed enhancements in SRAM CMOS circuits, have been applied to on-chip global interconnects [3, 4]. It was demonstrated that the CM interconnects exhibit better performance than their voltage-mode (VM) counterparts. Moreover, repeater insertion techniques were usually employed to reduce the time delay [5], and some power-optimal repeater insertion methodologies were also developed [6, 7].

Besides circuit optimisation, there have been great efforts devoting to the alternative conductive materials for interconnect applications. Carbon nanotubes (CNTs), including single-walled CNT bundle (SWCNTB) and multi-walled CNT (MWCNT), have been proposed as a promising interconnect material due to their extraordinary physical properties [8–10]. To further improve the interconnect performance, the CNT interconnects in the CM signalling (CMS) scheme have been proposed and studied [11]. The repeater insertion methodology has also been employed in the design of CNT interconnects to reduce time delay [12–14]. As demonstrated in these studies, both CMS and repeater insertion techniques can significantly reduce the time delay.

However, there still lacks a fundamental study on optimal repeater insertion for the CM interconnects, not to mention the CNT interconnects in the CMS scheme. Although it was indicated that an unrepeatable CM interconnect is superior to a repeated one with uniformly spaced VM drivers [4], the CM interconnects would also suffer from serious performance degradation problem as the interconnect dimensions scale to nanometres. To fill that gap, the optimal repeater insertion in the CM nano-interconnects, which can be made of Cu, SWCNTB, and MWCNT, is studied in this Letter.

This Letter is organised as follows. The circuit models of the CM and VM nano-interconnects are presented in Section 2. In Section 3, the figure-of-merit of the nano-interconnects is defined. The optimal repeater designs are carried out using the particle swarm optimisation (PSO) algorithm. The results are employed to train a back-propagation artificial neural network (ANN) due to its flexibility and high speed. Based on the trained ANN, a comparative analysis

is conducted in Section 4. Finally, some conclusions are drawn in Section 5.

2. Electrical model: Fig. 1a shows the cross-sectional view of typical on-chip interconnect. In the figure, W , H , and T denote the interconnect width, interconnect height, and interlayer dielectric thickness, respectively, S is the spacing between adjacent interconnects, and ϵ_r is the effective dielectric constant of the surrounding dielectric. The related parameters are adopted from ITRS 2013 and listed in Table 1 [1].

In modern ICs, Cu is widely utilised as interconnects due to its low resistivity and high electromigration resistance. To prevent the Cu diffusion into dielectric and subsequently into silicon substrate, as shown in Fig. 1b, a barrier layer should be placed between Cu and the dielectric material. Here, the barrier layer thickness is denoted as T_a , and the effective width and height of the Cu wire are $W_{Cu} (= W - 2T_a)$ and $H_{Cu} (= H - 2T_a)$, respectively. The resistance of the Cu wire can be calculated by $R_{Cu} = \rho_{Cu}L/(W_{Cu}H_{Cu})$, where L is the wire length and ρ_{Cu} is the Cu resistivity. When the wire width scales to below 100 nm, the scattering probabilities of electrons at surface and grain boundary increase dramatically, thereby leading to significantly increased resistivity [2]

$$\rho_{Cu} = \rho_0 \left[\frac{1/3}{1/3 + \alpha/2 + \alpha^2 - \alpha^3 \ln(1 + 1/\alpha)} + \frac{3}{8} c(1-p) \frac{1+AR}{AR} \frac{\lambda_{Cu}}{W_{Cu}} \right] \quad (1)$$

where $\alpha = \lambda_{Cu}R_g/[d_g(1-R_g)]$, $c = 1.2$, AR is the wire aspect ratio, $R_g = 0.22$ is the reflective coefficient at the grain boundary, $\rho_0 = 2.04 \mu\Omega \cdot \text{cm}$ is the bulk resistivity, $p = 0.41$ is the specular parameter of the Cu surface, λ_{Cu} is the mean free path (MFP) of Cu, and d_g is the average distance between grain boundaries that is usually set as W_{Cu} .

The per-unit-length (p.u.l.) capacitance C_{pul} can be extracted using the full-wave electromagnetic simulator (e.g. ANSYS Maxwell). Based on the configuration in Fig. 1a and the geometrical parameters in ITRS [1], C_{pul} is 149.4 pF/m for the 14 nm technology node and 120.3 pF/m for the 7 nm technology node, respectively. As the interconnect width increases, the capacitance is almost kept unchanged because of the constant aspect ratios of wire and via (see Table 1).

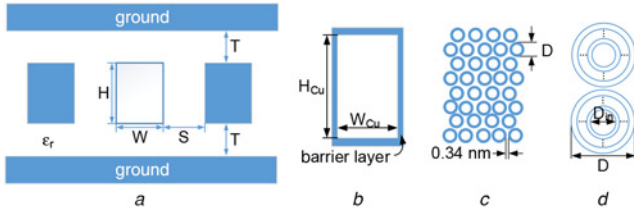


Fig. 1 Schematic of on-chip interconnect

- a Cross-sectional view of typical on-chip interconnect, which can be made of
b Cu
c SWCNTB
d MWCNT

Table 1 Parameters of the global interconnects adopted from ITRS 2013

Technology node	14 nm	7 nm
interconnect width	21.5 nm–1 μm	10.5 nm–1 μm
wire aspect ratio (H/W)	2.34	2.4
via aspect ratio (T/W)	1.5	1.5
effective dielectric constant ϵ_r	2.08	1.65

As mentioned earlier, CNTs have been used as on-chip interconnects as they possess low resistivity and high ampacity. The resistance of an isolated SWCNT is a function of the CNT diameter D , i.e. $R_{\text{CNT}}(D) = 6.45L/D$ [10]. To reduce the resistance, the SWCNTB is used for interconnect applications, as shown in Fig. 1c. In general, about one-third of SWCNTs in the bundle are metallic, i.e. the fraction of metallic SWCNTs in the bundle is $Fm = 1/3$. Various efforts have been made to improve the metallic fraction, and therefore, all metallic SWCNTBs (i.e. $Fm = 1$) are also considered in this Letter. The resistance of SWCNTB is $R_{\text{SWCNTB}} = R_{\text{CNT}}/N$, where N is the number of metallic SWCNTs [8]. For an MWCNT, the innermost diameter D_{in} is set as one half of its outermost diameter, as shown in Fig. 1d. The resistance of MWCNT is $R_{\text{MWCNT}} = 6.45L \cdot [\sum_{i=1}^{N_s} D_i N_{\text{ch},i}]^{-1}$, where N_s is the shell number and $N_{\text{ch},i}$ is the number of conducting channels of i th shell [10]

$$N_{\text{ch},i} = \begin{cases} 2/3, & D_i \leq 6 \text{ nm} \\ 0.0612D_i + 0.425, & D_i > 6 \text{ nm} \end{cases} \quad (2)$$

Different with the Cu wire, the CNT interconnect has metal-CNT contact resistance. For SWCNTB, the contact resistance is $R_c = 3225 + R_{\text{mc}}/(2N)$, and for MWCNT, it is $R_c = [4 \sum_{i=1}^{N_s} (R_{\text{mc}} + 12,900/N_{\text{ch},i})^{-1}]^{-1}$ [14], where R_{mc} is the imperfect contact resistance per channel, and it highly depends on the fabrication process.

As the CNT quantum capacitance is much larger than the electrostatic one, it can be neglected in the simulation. In general, p.u.l. capacitance of SWCNTB is the same as that of the Cu interconnects. However, as shown in Fig. 1d, the aspect ratio of the MWCNT interconnect is fixed as 2, and due to its configuration, the MWCNT interconnect has a smaller capacitance than its Cu counterpart. Based on the full-wave simulation, the p.u.l. the capacitance of the MWCNT interconnect is 129.12 and 102.24 pF/m for the 14 and 7 nm technology nodes, respectively.

3. Figure-of-merit (FoM): Fig. 2 shows a long interconnect inserted with uniformly distributed repeaters. In the figure, R_d is the driver resistance, C_d is the driver capacitance, and R_L and C_L are load resistance and capacitance, respectively. Here,

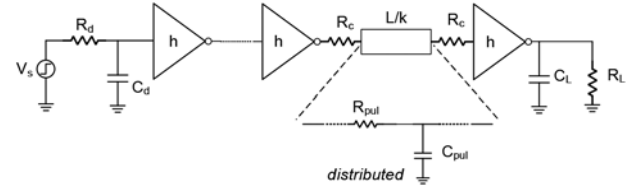


Fig. 2 Long interconnect inserted with uniformly distributed repeaters

nano-interconnect is modelled as resistance-capacitance (RC) distributed circuits [15].

The interconnect is divided into k segments by $k - 1$ repeaters, and each segment has a length of L/k . The repeaters are assumed as h times the minimum size, i.e. $R_d = R_{d0}/h$, $C_d = hC_{d0}$, $R_L = R_{L0}/h$, and $C_L = hC_{L0}$. For the CMS scheme, it is assumed that R_{d0} , C_{d0} and C_{L0} are 30.3 kΩ, 0.15 fF and 0.3 fF at the 14 nm node and 69.7 kΩ, 0.06 fF, and 0.12 fF at the 7 nm node, respectively, with $R_{L0} = R_{d0}$. As shown in Fig. 3, the CM circuit described in [4] is adopted, while for the VM signalling (VMS) scheme, there is no load resistance, i.e. $R_L = \infty$ [16]. Therefore, based on a unified model, the time delay of one segment of interconnect can be calculated by [4]

$$T_{\text{seg}} = \frac{\ln(a/2)R_T C_T}{1 + 1.0058 \ln(a)} \left[\eta_L R_{dT} \left(1 + \frac{1}{2R_{LT}} \right) + \eta_d C_{dT} \right] \times (1 + R_{LT}) + \frac{\eta_L}{2} \left(1 + \frac{1}{3R_{LT}} \right) + \eta_L C_{LT} (1 + R_{dT}) \quad (3)$$

where $a = 1.2 + 0.5\eta_L/R_{LT}$, $\eta_L = R_L/(R_L + R_d + R_T)$, $\eta_d = R_d/(R_L + R_d + R_T)$, $R_{LT} = R_L/R_T$, $R_{dT} = R_d/R_T$, $C_{dT} = C_d/C_T$, $C_{LT} = C_L/C_T$, $R_T = R_{\text{pul}}L/k + R_c$, and $C_T = C_{\text{pul}}L/k$. Here, the metal-CNT contact resistance has been considered in the model. The time delay of the interconnect inserted with $k - 1$ repeaters is $T_{\text{total}} = kT_{\text{seg}}$. Moreover, the energy dissipation of one segment of interconnect in a clock period is [4]

$$P_{\text{seg}} = (\eta_L V_{dd})^2 \left\{ C_L + C_d \left[1 + \frac{2R_T}{R_L} + \left(\frac{R_T}{R_L} \right)^2 \right] + C_T \left[1 + \frac{R_T}{R_L} + \frac{1}{3} \left(\frac{R_T}{R_L} \right)^2 \right] \right\} \quad (4)$$

The total power dissipation P_{total} is proportional to kP_{seg} . With the consideration of both time delay and power dissipation, the FoM of interconnect is defined as $\text{FoM} = k^{p+q} \cdot P_{\text{seg}}^p \cdot T_{\text{seg}}^q$, where p and q are weighting factors.

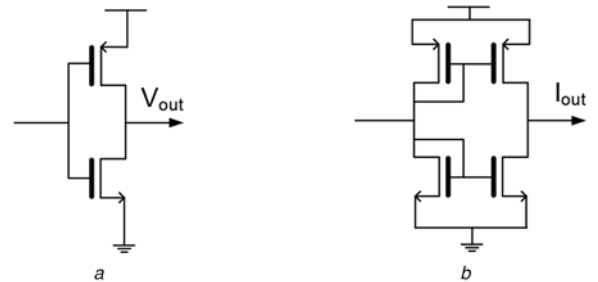


Fig. 3 Voltage and current mode receivers
a VM
b CM

4. Optimal repeater design: Following the optimal repeater design procedure proposed in [14], the PSO algorithm is used to obtain the minimum value of FoM by cooperation and competition of the particles in virtue of its high computational efficiency. To validate the PSO algorithm, the optimal number of repeaters of the Cu, SWCNTB, MWCNT interconnects at the 14 nm and 7 nm technology nodes in the CMS scheme are obtained and compared with those obtained using the genetic algorithm (GA), as shown in Fig. 4. For simplicity, both p and q are set as 1 (i.e., the repeaters are optimised at the target of minimum energy-delay product) and the SWCNT diameter is set as 1 nm. It is evident that the results obtained using the PSO and GA algorithms agree well with each other. As the total FoM is the sum of the FoMs of all segments, the segment length should be optimised at first, independent of L . Therefore, the optimal number of repeaters increases linearly with the length. The CNT nano-interconnects require fewer repeaters due to their smaller resistance, thereby saving more power and chip area [10]. With regard to the optimal repeater size, the Cu interconnect in the VMS scheme at the 14 nm node is taken for example, and the p.u.l. resistance and capacitance of the global level interconnect are $R_{pul} = 94.4 \Omega/\mu\text{m}$ and $C_{pul} = 150 \text{ pF/m}$, respectively. According to [17], the optimal repeater size of the 5000 μm -long Cu interconnect in the VMS scheme can be calculated as $h_{opt} = [R_{d0}C_{pul}/(C_{L0}R_{pul})]^{1/2} = 17.88$. By utilising the PSO algorithm, it is found that the optimal repeater size is about 17, which is consistent with the analytical result.

As low power design is very important in future nanoscale ICs due to the power wall, special attention should be paid to the power consumption in the optimal repeater design. Herein, one can examine the cases with different weights of the power dissipation in FoM by changing p from 0 to 1.5 with q kept as 1. Fig. 5 shows the optimal number of repeaters in the Cu nano-interconnects for different weights of the power dissipation in FoM. It is evident that the CM nano-interconnects require fewer repeaters than its VM counterparts. As the value of p increases, the optimal number of repeaters in the VM nano-interconnects decreases significantly. This is because fewer repeaters can save more power. Differently, the optimal number of repeaters in the CM nano-interconnect has only a slight decrease with the increasing p .

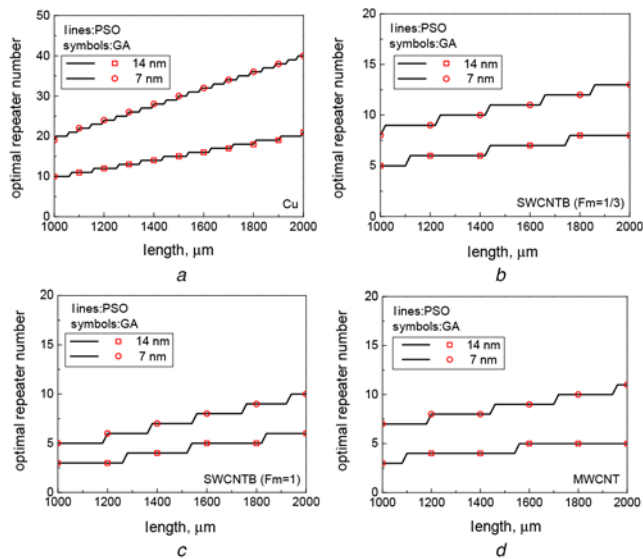


Fig. 4 Optimal numbers of the repeaters
a Cu interconnect
b SWCNTB ($F_m = 1/3$) interconnect
c SWCNTB ($F_m = 1$) interconnect
d MWCNT interconnects

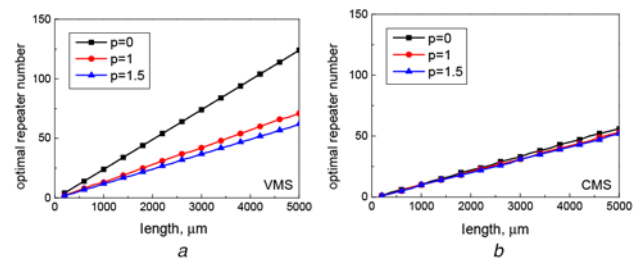


Fig. 5 Optimal number of repeaters in Cu interconnects at the 14 nm technology node
a VMS scheme
b CMS scheme

Moreover, the FoMs of the optimised Cu interconnects in the CMS and VMS schemes are compared. Fig. 6 shows the ratio of FoM between the CM and VM interconnects at the 14 and 7 nm technology nodes. It is evident that the advantages of the CM interconnects are almost unchanged with the scaling of technology. More importantly, as the weight of the power dissipation in FoM increases, the FoM ratio between the CM and VM interconnects decreases significantly. This is because the CM repeater consumes less power than the VM one as $\eta_L < 1$ in the CMS scheme [4]. Moreover, the results imply that the CM nano-interconnect is more superior to its VM counterpart when the power is more emphasised in the IC design.

Then, the optimal repeater size and optimal number of repeaters obtained using the PSO algorithm are used to train a two-layer back-propagation ANN. Here, 70% of the data is used as the training set, whereas the rest is used as the test set [14]. The implementation of the ANN can reduce the computation time significantly. Based on the trained ANNs, the optimal number of repeaters in nano-interconnects can be quickly determined. As discussed earlier, each repeater inserted in the CNT interconnect would bring two metal-nanotube contact resistances. To investigate the influence of contact resistance on the optimal repeater design, Fig. 7 plots the optimal number of repeaters in the CNT interconnects in the VMS and CMS schemes. It is evident that the R_{mc} has negligible influence on the optimal repeater designs in SWCNTB interconnect. As the value of F_m increases, the effective resistance of the SWCNTB interconnect decreases, thereby reducing the demand for repeaters. It can be seen in Figs. 7a and b that the optimal number of repeaters in SWCNTB interconnect decreases dramatically with the increasing value of F_m . Moreover, the CM nano-interconnect requires fewer repeaters than its VM counterpart, and this advantage would be more pronounced as the technology node scales down.

In general, the MWCNT interconnect possesses long MFP but a limited number of conducting channels, implying that it is more susceptible to the variation of R_{mc} than the SWCNTB one. It can be seen in Fig. 7c that the optimal number of repeaters in MWCNT nano-interconnect decreases with the increasing R_{mc} . This is, simply neglecting the contact resistance would overestimate the optimal number of repeaters, thereby degrading the electrical

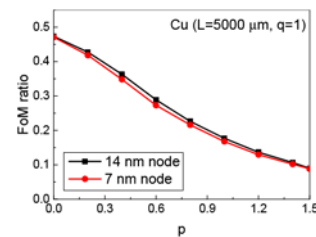


Fig. 6 Ratio of FoMs between CM and VM interconnects as a function of p

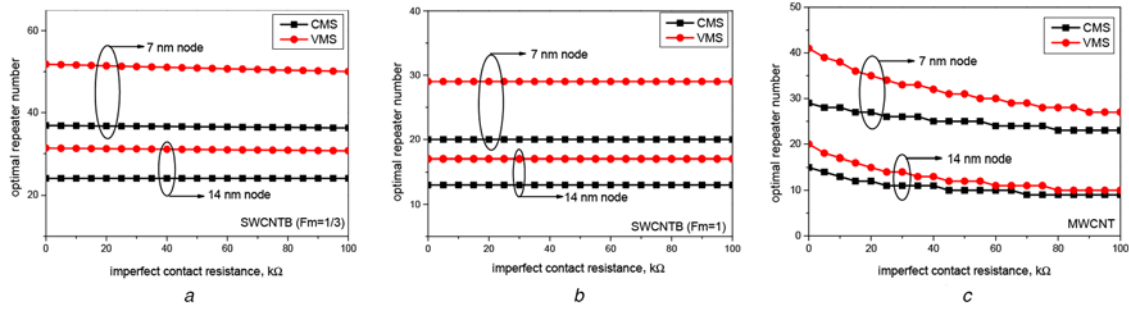


Fig. 7 Optimal number of repeaters in 4000 μm -long interconnect in the VMS and CMS schemes
a SWCNTB ($F_m=1/3$) interconnect
b SWCNTB ($F_m=1$) interconnect
c MWCNT interconnect

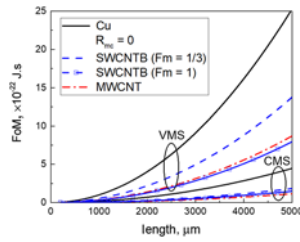


Fig. 8 FoMs of the optimised nano-interconnects

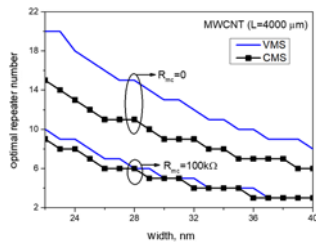


Fig. 9 Optimal number of repeaters in MWCNT interconnect at the 14 nm technology node

performance. Similarly, the CMS scheme can save some chip area since it needs fewer repeaters than the VM one, which becomes more significant with the technology node scaling down.

Fig. 8 shows FoMs of the optimised nano-interconnects at the 14 nm technology node. It is evident that the CM nano-interconnects are superior to their VM counterparts despite the conductor type. It is evident that MWCNT interconnect in the CMS scheme possesses excellent electrical performance and requires few repeaters. Moreover, MWCNT is always metallic and easy to process, indicating that such an interconnect scheme should be pursued for future high-performance ICs. Fig. 9 shows the optimal number of repeaters in the MWCNT interconnect versus the width. Here, the maximum diameter of the MWCNT is assumed as 40 nm. It is evident that as the width increases, the interconnect requires fewer repeaters due to the decreased resistance.

Finally, the ratio of FoMs between the optimised MWCNT and Cu interconnects are plotted in Fig. 10. It is evident that as R_{mc} exceeds a certain value, the ratio of FoMs would become larger than 1, implying that the MWCNT interconnects no longer have advantages over their Cu counterparts. Here, the value of R_{mc} at which the FoMs of the optimised MWCNT and Cu interconnects are equal with each other is defined as the maximum tolerable imperfect contact resistance $R_{mc,max}$, which is found to be independent of the length. In the VMS scheme, $R_{mc,max}$ is about 57 and 180 k Ω at the 14 and 7 nm technology nodes, respectively.

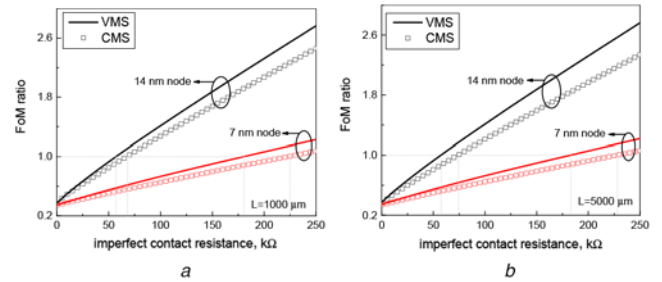


Fig. 10 Ratio of FoMs between MWCNT and Cu interconnects as a function of imperfect contact resistance

a 1000 μm
b 5000 μm

As the contact resistance may increase more than fourfold as the technology scales down from 14 to 7 nm, more advanced technology node has a more stringent requirement on R_{mc} . Moreover, in the CMS scheme, $R_{mc,max}$ increases to 68 and 225 k Ω at the 14 and 7 nm technology nodes, respectively, implying that CM nano-interconnects have a lenient requirement on the contact resistance than their VM counterparts. It should be pointed out that there are still many fundamental issues unsolved. For instance, the tapered buffer insertion techniques should be investigated for nano-interconnects as tapered buffer can drive large capacitive loads, which will be the subjects of our future work.

5. Conclusion: In this work, the optimal repeater design was carried out for the CM nano-interconnects and compared with that for their VM counterparts. Both the Cu and CNT interconnects were modelled, and the metal-nanotube contact resistance was considered and treated appropriately. It was found that the CM nano-interconnects not only have better performance, but also require fewer repeaters than their VM counterparts. As the power dissipation weighs more in FoM, the advantage of the CMS scheme to the VMS one becomes more significant. This is because the CM nano-interconnects consume less power than their VM counterparts due to reduced supply voltage at the receiver. Moreover, it was demonstrated that the optimal number of repeaters in the CM nano-interconnect is insensitive to the weight variation of the power dissipation in FoM.

Furthermore, by comparing their optimal repeater design results, it was found that MWCNT nano-interconnects in the CMS outperform their Cu counterparts. Moreover, MWCNT is easy to process in comparison with SWCNTB as it is always metallic. However, the applications of the MWCNT interconnects are highly depending on the imperfect contact resistance. The advantage of MWCNT is lost as the imperfect contact resistance exceeds a certain value, regardless of the interconnect length. Moreover, the more advanced

technology node has a more severe restriction on the imperfect contact resistance, thereby placing more restriction on the fabrication process. Fortunately, the CMS scheme can alleviate such restriction.

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