Anisotropic transport in tellurene FETs

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Tellurene, a single layer of tellurium, is a new emerging 2D material and a possible candidate for the post-silicon era. It has anisotropic carrier effective mass in zigzag and armchair directions. Therefore, the study of the anisotropic performance of tellurene FETs is a timely topic. In this work, the authors study the transport mechanism and performance metrics of tellurene n-channel and p-channel transistors using a quantum simulation. Heavy carrier mass in the armchair direction effectively blocks the tunnelling current and the transport is governed by thermionic emission over the potential barrier. On the other hand, lighter carrier mass in the zigzag direction results in a mixed tunnelling and thermionic transport mechanism. The n-channel transistor has an on-state current of 894 μA/μm, a sub-threshold slope of 62 mV/dec, a 9.27 mS/μm transconductance, a 0.129 ps delay, and a 0.046 fJ/μm dynamic power loss. The p-channel metrics are, respectively, 852 μA/μm, 62 mV/dec, 9.24 mS/μm, 0.117 ps, and 0.040 fJ/μm. Both the transistors comply with the International Technology Roadmap for Semiconductors 2026 low operating power device requirements.

1. Introduction: In recent years, 2D materials have attracted significant attention due to their unique mechanical, electrical, and optical properties. Tan *et al.* [1] provided a detailed review of recent advances in ultrathin 2D materials along with their synthetic methods, characterisation techniques, and applications. The 2D materials that have been explored in various applications include group III monolayer of borophene [2], group IV monolayer of graphene [3–6] and graphene-like 2D materials [7], silicene [8] and stanene [9, 10], group V monolayer of phosphorene [11], transition metal dichalcogenides [12], and metal chalcogenides such as GaTe [13] and InSe [14]. Very recently, a group VI material called tellurene (single layer of tellurium) has been added to the list. Theoretical studies [15–17] and fabrication [18–20] of tellurium nanostructures have been reported. Its applications in nanoscaled transistors have been demonstrated theoretically [21] and experimentally [22, 23]. Recently, the progress, challenges, and prospects of 2D tellurium have been reviewed in detail [24].

Tellurium has the chiral-chain crystal structure in which the individual chains are stacked together by van der Waals forces. The bulk tellurium is a direct band gap material with a band gap value of 0.38 eV, and its monolayer (tellurene) is also a direct gap [16] or nearly direct gap [15] 2D material. Using first-principles calculations, Zhu *et al.* [15] predicted three structures of tellurene named α, β, and γ phases. These structures were later confirmed by Qiao *et al.* [25]. The tetragonal β-tellurene has anisotropic transport properties along with the zigzag and armchair directions. The β-tellurene has been realised on a graphene substrate [19] and in a substrate-free solution process [23].

The back-gated 7.5 nm thick 2D tellurium FETs fabricated on the high-k dielectric substrate [23] has a high on-state current of 300 mA/mm and an on–off current ratio of 1×10^5 in the long channel limit. In [23], the 100 nm channel device exhibited an on-state current of 550 mA/mm. Zhao *et al.* [26] have fabricated p-type tellurium thin film FET using thermal evaporation. Their 8 nm thin film FET showed an on–off current ratio of 10^4, a sub-threshold slope of 108 mV/dec, and a hole mobility of $35\,cm^2V^{-1}s^{-1}$. The hole mobility of transfer-free direct growth tellurium p-channel FET (pFET) reported by Zhou *et al.* [27] is $707\,cm^2V^{-1}s^{-1}$. Yan *et al.* [28] theoretically investigated the sub-5 nm tellurene FETs and reported that the FETs can satisfy the International Technology Roadmap for Semiconductors (ITRS) requirements at a gate length of 4 nm. The β-tellurene nanoribbon FETs have been theoretically studied using first-principles-based multiscale simulation [21]. Their 20 nm channel length double gate ballistic FETs show an on-state current of 750 μA/μm for hole transport and 1000 μA/μm for electron transport for a 0.8 V gate swing.

In this work, we study the transport mechanism and performance metrics of monolayer β-tellurene n-channel FET (nFET) and pFET. Transport in both zigzag and armchair directions is studied. While transport in the armchair direction is thermionic, it is mixed tunnelling and thermionic in the zigzag direction. Both the nFET and pFET show better performance when transport in the zigzag direction is considered. We benchmark the performance metrics of zigzag nFET and pFET against the ITRS 2026 low operating power (LOP) technology requirements [29], and we found that both the devices fulfil the requirements.

2. Device structure and simulation approach: For 2026 LOP logic, the ITRS predicted device has a physical gate length of 5.8 nm, an effective oxide thickness of 0.5 nm, and a power supply voltage of 0.43 V [29]. In line with the 2026 LOP requirements, we setup our simulation device structure, shown in Fig. 1, with $L_G = 6$ nm, HfO_2 gate dielectric with effective oxide thickness = 0.5 nm, and drain bias $V_D = 0.4$ V. The device has a double gate structure. The undoped channel is a monolayer β-tellurene. For comparison, we also simulated a 3 nm silicon ultrathin body (UTB) channel. That is the same device structure with monolayer tellurene channel replaced by a 3 nm Si UTB.

A 2D Poisson's equation is discretised using the finite difference method and is solved over the entire device domain using a Newton–Raphson method. As the boundary conditions, we fixed voltages on the gate electrodes and set the normal component of electric field to zero at all other boundaries. For monolayer tellurene, we discretise a 1D effective mass Schrodinger's equation using the finite difference scheme for the charge and transmission calculation. Discretisation uses a grid spacing of 0.2 nm. The effective masses are taken from [15], and the values are listed in Table 1, where m_0 is the free electron mass. These values are calculated in [15] using Vienna ab initio simulation package within the projector augmented wave method. The effective masses are extracted from the tellurene band structure [15] (NOT from the bulk tellurium), and the transistors studied in this work operate in low-bias range. Therefore, single-band effective mass approximation is fair enough. For the Si UTB channel, the 2D Schrodinger's equation is discretised using the same grid spacing. The longitudinal

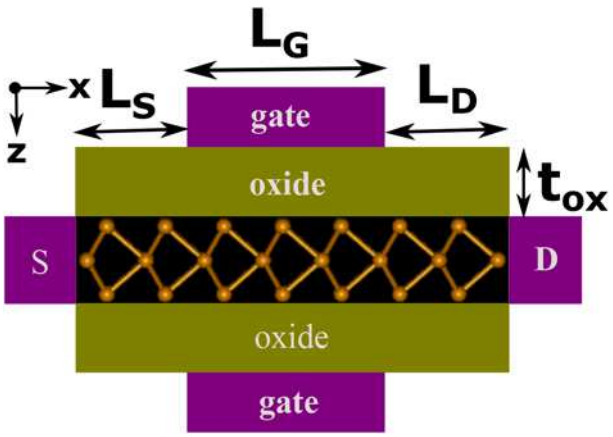

Fig. 1 *Cross-section of the device structure used for simulation. Different dimensions are: $L_G = 6\,nm$, $L_S = 25\,nm$, $L_D = 30\,nm$, and $t_{ox} = 2.37\,nm$. A slightly longer L_D is taken to ensure flat band on drain end*

Table 1 Electron and hole effective masses and mobilities of Te monolayer in zigzag and armchair directions. The data are taken from [15]

Parameter	Zigzag	Armchair
electron mass, m_0	0.19	0.83
electron mobility, $cm^2/V\text{-}s$	100	50
hole mass, m_0	0.11	0.3
hole mobility, $cm^2/V\text{-}s$	450	198

effective mass of $0.98m_0$ and the transverse effective mass of $0.22m_0$ are used for the 3 nm Si UTB. These masses for the 3 nm UTB silicon have been verified against an atomistic $sp^3d^5s^*$ simulation [30].

Electron density is calculated using recursive Green's function algorithm [31]

$$n(x,z) = (n_s n_v)\sqrt{\frac{m_y k_B T}{2\pi\hbar^2}} \cdot \int \frac{dE}{2\pi}\Big[A_S F_{-1/2}(\eta_S) + A_D F_{-1/2}(\eta_D)\Big], \tag{1}$$

where n_s and n_v account for spin and valley degeneracies, k_B is the Boltzmann's constant, T is the temperature in Kelvin, m_y is the effective mass in the width direction, F_j is the Fermi integral of order j, and A_S and A_D are the source and drain spectral functions, respectively. The arguments of Fermi $-1/2$ integrals are $\eta_S = (\mu_S - E)/k_B T$ and $\eta_D = (\mu_D - E)/k_B T$, where μ_S and μ_D are the source and drain Fermi levels, respectively. The density $n(x, z)$ is divided by the grid area to obtain the volume density. Within the self-consistent loop, the drain current is calculated from

$$I_D = \left(\frac{1-r_c}{1+r_c}\right)(n_s n_v)\frac{q}{h}\sqrt{\frac{m_y k_B T}{2\pi\hbar^2}} \cdot \int \frac{dE}{2\pi} T(E)\Big[F_{-1/2}(\eta_S) - F_{-1/2}(\eta_D)\Big], \tag{2}$$

where the transmission coefficient $T(E)$ is calculated using Green's function [31] and the backscattering parameter is calculated from $r_c = \ell/(\ell + \lambda)$. Here ℓ is the critical length, which is the distance from the top of the band to the position where the potential drops by $k_B T$ [32]. The low-field mobility is used to calculate the mean-free path λ [33]

$$\lambda = \frac{2k_B T}{q}\frac{\mu_0}{v_T}\frac{F_0(\eta_{top})}{F_{-1/2}(\eta_{top})}. \tag{3}$$

The argument of Fermi integrals is $\eta_{top} = (\mu_S - E_{Ctop})/k_B T$ and the thermal velocity of electron gas is $v_T = \sqrt{2k_B T/\pi m_t}$. The low-field mobility values for tellurene, taken from [15], are listed in Table 1. For Si UTB, we set low-field mobility to $200\,cm^2\,V^{-1}\,s^{-1}$ [34]. The calculated current is used to update the potentials of internal part of the device, $V^i_{GS} = V_{GS} - I_D R_S$ and $V^i_{DS} = V_{DS} - I_D(R_S + R_D)$. The experimental realisation of metal–tellurene contact is in an early stage. The extracted total contact resistance values of substrate-free solution growth tellurene FETs are 0.67 and 0.82 Ω-mm, respectively, for Pd and Ni contacts [23]. The theoretical first principle calculations [35, 36] show that while Pd and Ni form Schottky contacts, graphene forms nearly ohmic contact to tellurene. In this work, we set the contact resistance value to $R_C = R_S + R_D = 102\,\Omega - \mu m$ as per ITRS 2026 LOP technology requirement [29]. The self-consistent loop started with an initial guess of potential and the potential profile, the carrier density, the current, and the internal voltages are updated in each iteration of the self-consistent loop. The simulation package is our in-house code and it is written in open source programming language Julia [37].

3. Simulation results and discussions: The *I–V* characteristics of nFET for transport in zigzag and armchair directions are shown in Fig. 2. There, the *I–V* characteristics of a silicon double-gate FET are also shown. We set the drain bias to 0.4 V and swing the gate bias over a wide range. Then the voltage axis is shifted to zero corresponds to the off-state current of 5 nA/μm, which is the 2026 ITRS requirement for LOP devices [29]. In the sub-threshold region, the *I–V* characteristics of Te-nFET in both transport directions are identical. However, the above threshold, the current in the zigzag direction is higher. The on-state current for transport in the zigzag direction is 894 μA/μm and for transport in the armchair direction is 675 μA/μm. In both cases, the on-state current is higher than the 2026 LOP requirement of 666 μA/μm. However, Si double-gate FET having an on-state current of 296 μA/μm fails to even meet the requirement. That is tellurene outperforms silicon as the channel material. From here on, we will focus on tellurene-based FETs only. An on-state current of 550 μA/μm has been reported for solution growth tellurium FET [23]. Simulation results reported in the literature for ballistic on-state current are 951 μA/μm for 5 nm Te monolayer FET with a gate swing of 0.64 V [28] and 1000 μA/μm for Te monolayer nanoribbon FET [21] for a gate bias swing of 0.8 V. The sub-threshold swing of both tellurene FETs shown in Fig. 2 is 62 mV/dec. Yan *et al.* [28] used source and drain underlap regions to block off-state tunnelling current and achieved a near-ideal sub-threshold slope of 60 mV/dec for a 5 nm tellurene FET. The electron mass in the zigzag direction is significantly lower resulting in high electron mobility in that direction (see Table 1). Therefore, the on-state current

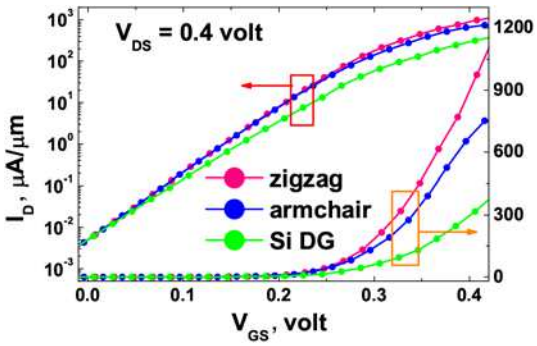

Fig. 2 *I–V characteristics of n-channel silicon double-gate FET and monolayer tellurene FET for transport in zigzag and armchair directions. The left vertical axis is the log scale and the right vertical axis is the linear scale. Rectangles with an arrow indicate the y-axis of the curves*

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in the zigzag direction is also high. However, the sub-threshold current in both transport directions is identical.

For a deeper understanding of the sub-threshold behaviour, we plot, in Fig. 3*a*, the conduction band profile and energy spectrum of off-state current of zigzag tellurene nFET. Here the source Fermi level is the reference energy. The conduction band top is located at 0.319 eV, and the current spectrum, $J(E)$ spreads from 0.07 to 0.62 eV. The area under $J(E)$ from 0.07 to 0.319 eV is the current that flows through the conduction band barrier. That is integration of $J(E)$ from 0.07 to 0.319 eV gives the tunnelling current, which is 41% of the off-state current. This tunnelling mechanism is called intra-band tunnelling, because an electron injects from the source conduction band, tunnels through the channel potential barrier, and reaches the drain conduction band. That is the tunnelling is from the conduction band to the conduction band. Similarly, the area under $J(E)$ from 0.319 to 0.62 eV is the current that flows over the top of the conduction band. That is integration of $J(E)$ from 0.319 to 0.62 eV gives the thermal current or the current that flows over the top of the barrier. This current is 59% of the off-state current. In armchair tellurene nFET, Fig. 3*b*, the conduction band top is located at 0.28 eV and $J(E)$ spreads from 0.19 to 0.607 eV. The tunnelling current that flows in the energy range of 0.19–0.28 eV is 12% of the off-state current. The rest 88% of the off-state current flows over the top of the conduction band in the energy range of 0.28–0.607 eV. Also, note that the off-state conduction band top of armchair nFET is located at lower energy, which increases the thermal component of current. The decomposition of current into tunnelling and thermal parts for transport in zigzag and armchair directions are shown in Fig. 4. Clearly, the transport in the armchair direction is dominated by thermionic emission over

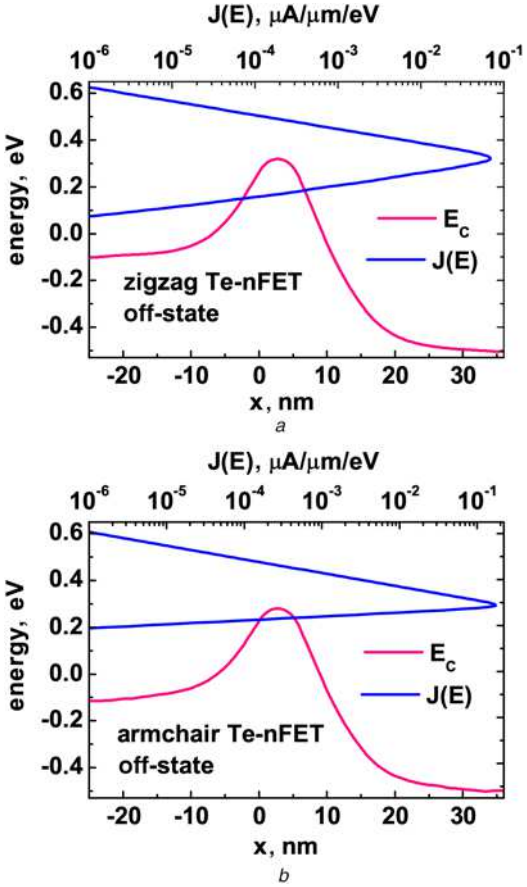

Fig. 3 *Off-state conduction band profile, E_C and energy spectrum of current J(E). Here the source Fermi energy is the reference energy*
a Zigzag tellurene nFET
b Armchair tellurene nFET

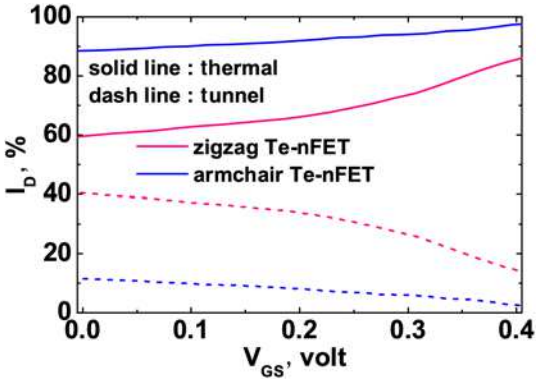

Fig. 4 *Tunnelling and thermal current components versus gate bias for both zigzag and armchair tellurene nFETs*

the entire bias range. The heavy electron mass in the armchair direction effectively blocks the tunnelling current. On the other hand, lighter electrons in the zigzag direction easily tunnel through the channel potential barrier in the off-state. With gate bias, the channel potential barrier reduces, and therefore, the thermionic current increases. The on-state transport mechanism is governed by thermionic emission in both directions. However, the transport in the zigzag direction is mixed tunnelling and thermal in the sub-threshold region for lighter electron mass in that direction.

From Table 1, we see that the hole effective mass is also direction dependent. It is lighter in the zigzag direction but heavier in the armchair direction. As a result, the hole mobility is also anisotropic. To see this anisotropic effect on transport, we plot the *I–V* characteristics of Te-pFET in Fig. 5. Although the current in the zigzag direction is expected to be much higher, it is not the case. We observe a slightly higher current in on-state for transport in the zigzag direction. The on-state current of zigzag pFET is 852 μA/μm and it is 778 μA/μm for armchair pFET. The sub-threshold swing in both cases is 62 mV/dec. The lighter hole mass and higher mobility in the zigzag direction could not bring much benefit to the FET's *I–V* characteristics, and the reason is the excessive tunnelling in the zigzag direction. This is evident from Fig. 6, where the tunnelling and thermal components of current are shown as the function of gate bias. The tunnelling current dominates in zigzag pFET up to $V_{SG} = 0.24$ V. Even in the on-state, the tunnelling current contributes 20% to the total current. That is the high mobility benefit from the lighter effective mass is counterbalanced by a high tunnelling current in the zigzag direction. On the other hand, the current is primarily thermal in the armchair direction.

For both the nFET and pFET, we see that transport in the zigzag direction gives a better on-state performance. We, therefore, evaluate the performance metrics of zigzag nFET and pFET. For this, the

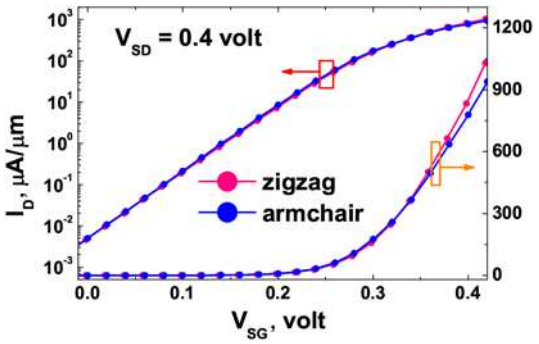

Fig. 5 *I–V characteristics of Te-pFETs for transport in both zigzag and armchair directions. Here $V_{SG} = 0$ is corresponding to the off-state and $V_{SG} = 0.4$ V is corresponding to the on-state. Rectangles with an arrow indicate the y-axis of the curves*

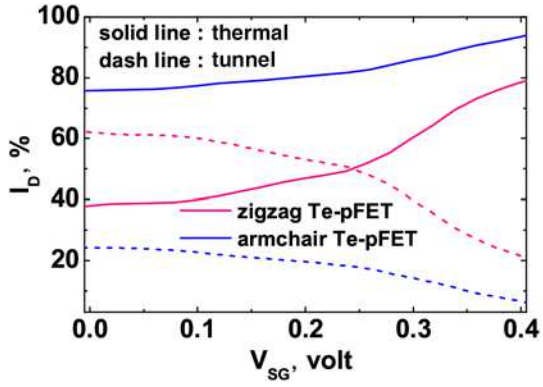

Fig. 6 *Tunnelling and thermal current components versus gate bias for both zigzag and armchair Te-pFETs*

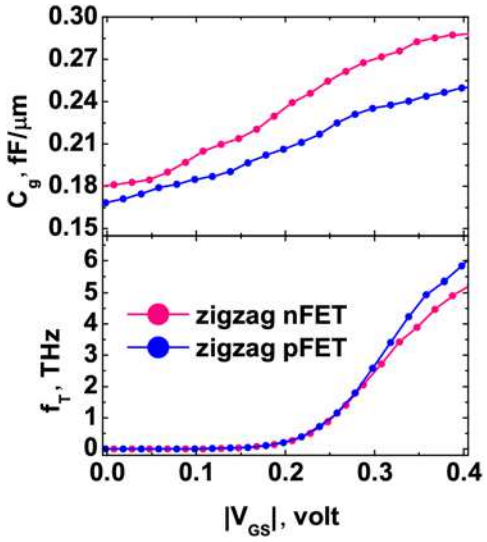

Fig. 7 *Top: gate capacitance versus gate bias. Bottom: cut-off frequency versus gate bias*

Table 2 Benchmarking performance metrics of Te nFET and pFET against ITRS 2026 LOP FET

Parameter	Te nFET	Te pFET	2026 LOP FET
I_{on}, μA/μm	894	852	666
I_{on}/I_{off}	1.79×10^5	1.70×10^5	1.3×10^5
S, mV/dec	62	62	—
g_m, mS/μm	9.27	9.24	—
C_g, fF/μm	0.288	0.249	0.402
τ_s, ps	0.129	0.117	0.26
CV^2, fJ/μm	0.046	0.040	0.07

gate capacitance is calculated by evaluating the flux density emanating from the three sides of the gate metal

$$C_g = \int \frac{\delta D_z}{\delta V_G} dx + \int \frac{\delta D_x}{\delta V_G} dz \quad (4)$$

Here D_z is the flux density along the z-direction (from top to bottom of Fig. 1) and D_x is the flux density along the x-direction (from left to right of Fig. 1). The first integral of (4) is over the bottom line of the gate metal and the second integral takes care of the two sides (facing to source and drain) of the gate metal. The gate capacitance and cut-off (unity current gain) frequency, $f_T = g_m/2\pi C_g$, are shown in Fig. 7. Although the performance metrics are competitive, the nFET has slightly higher gate capacitance and the pFET has slightly better cut-off frequency in the on-state. The performance metrics of the zigzag Te nFET and pFET are benchmarked against the 2026 LOP FET in Table 2. In the table, the delay time is computed from $\tau = C_g V_{DD}/I_{on}$, where $V_{DD} = 0.4$ V in our simulation. Both the nFET and pFET satisfy the 2026 LOP devices requirements. The pFET has slightly better performance in terms of delay and dynamic power indicator while nFET has better on-state current.

4. Conclusion: In conclusion, we have studied the transport physics and performance metrics of monolayer tellurene nFETs and pFETs using a quantum transport simulation. Transport in both zigzag and armchair directions is explored. The transport in the armchair direction for nFETs and pFETs is primarily governed by thermionic emission over the entire bias range. Whereas, electron tunnelling plays a significant role in the sub-threshold region and hole tunnelling dominates in the sub-threshold, and contributes significantly in the above threshold regions in the zigzag direction. Both the nFETs and pFETs show better performance for transport in the zigzag direction, and they meet the ITRS 2026 LOP requirements. The nFET has a slightly higher on-state current and the pFET has a slightly better delay and dynamic power indicator.

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