


An Energy efficient application specific integrated circuit for electrocardiogram feature detection and its potential for ambulatory cardiovascular disease detection

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Published in Healthcare Technology Letters; Received on 27th July 2015; Revised on 5th October 2015; Accepted on 26th October 2015

A novel algorithm based on forward search is developed for real-time electrocardiogram (ECG) signal processing and implemented in application specific integrated circuit (ASIC) for QRS complex related cardiovascular disease diagnosis. The authors have evaluated their algorithm using MIT-BIH database and achieve sensitivity of 99.86% and specificity of 99.93% for QRS complex peak detection. In this Letter, Physionet PTB diagnostic ECG database is used for QRS complex related disease detection. An ASIC for cardiovascular disease detection is fabricated using 130-nm CMOS high-speed process technology. The area of the ASIC is 0.5 mm^2 . The power dissipation is $1.73 \mu\text{W}$ at the operating frequency of 1 kHz with a supply voltage of 0.6 V. The output from the ASIC is fed to their Android application that generates diagnostic report and can be sent to a cardiologist through email. Their ASIC result shows average failed detection rate of 0.16% for six leads data of 290 patients in PTB diagnostic ECG database. They also have implemented a low-leakage version of their ASIC. The ASIC dissipates only 45 pJ with a supply voltage of 0.9 V. Their proposed ASIC is most suitable for energy efficient telemetry cardiovascular disease detection system.

1. Introduction: Wearable electrocardiogram (ECG) monitoring and diagnostic systems are developed for cardiovascular disease detection. For disease detection in [1, 2] ECG signal processing [3–5] is carried out using smartphone. Li *et al.* [6] had demonstrated that ECG signal processing algorithm execution in ASIC (in 45-nm technology operating at 100–222.2 MHz) results in 20 times faster runtime and lower (1/2871 times) energy dissipation as compared to the case when the same ECG signal processing algorithm is executed in a smartphone operating at 1.5 GHz. We propose an energy and area efficient QRS ASIC which detects RR interval and QRS duration to detect arrhythmia [7], which includes bradycardia, tachycardia, premature ventricular contraction beat, couplet beat, fusion beat and escape beat.

Our ASIC is based on our forward search region (FSR) technique [8] to detect QRS complex peak. In addition, we detect *R* peak value, *Q* peak value, *S* peak value and secondary *R* peak value to detect hypertrophy [9]. Also, we detect *R* wave duration and *S* wave duration which are needed to detect right bundle branch block [9].

To detect the above mentioned cardiovascular diseases, we verified our QRS ASIC using Physionet PTB diagnostic ECG database [10, 11]. The data from each ECG lead is processed in our ASIC to obtain *R–R* interval and QRS complex parameters, which includes QRS duration, *R* wave duration, *S* wave duration, *R* peak value, *Q* peak value, *S* peak value and secondary *R* peak value. The output from our ASIC can be used to detect arrhythmia, ventricular hypertrophy and bundle branch block besides *R–R* interval and its variability. The outputs of the ASIC are fed to an Android smartphone. We have developed an Android app which reads ASIC outputs and generates the disease diagnostic report. We have processed the ECG data from six leads sequentially in our QRS ASIC. Using six QRS ASICs, a parallel system can be realised to obtain *R–R* interval and QRS complex parameters.

Our QRS ASIC is fabricated in UMC high speed 130-nm technology with chip area of $1 \times 0.5 \text{ mm}^2$ and power dissipation of $1.73 \mu\text{W}$. Our QRS ASIC design using UMC low leakage 130-nm technology achieves power dissipation of 45 nW. To the best of our knowledge, our ASIC is the first hardware realisation that together with our Android app detects arrhythmia, ventricular

hypertrophy and bundle branch block besides *R–R* interval and its variability. Earlier ASICs could only detect *R–R* interval and its variability.

This paper is organised as follows. Section 2 presents software algorithm details for QRS ASIC design. Sections 3 and 4 present QRS ASIC architecture along with experiment results.

2. Software algorithm: For area and energy efficient ASIC implementation, we develop software algorithm with low computational overhead and very low failed detection rate (FDR) (0.16%). Fig. 1 shows three phases of the disease diagnostic algorithm proposed in this Letter. In the first two phases, we calculate QRS complex parameters. Based on this, we detect QRS complex related cardiovascular diseases during phase 3.

The digitised ECG signal is passed through a bandpass filter (bandwidth: 2–40 Hz [12]). The bandpass filter removes power line interference and baseline wander. Our QRS ASIC is designed to operate at 250 Hz sampling frequency so that memory requirement for the bandpass filter becomes small [7]. Next, we took square of ECG_FILT signal in filtered ECG signal processing block. The signal processing inside filtered ECG signal processing block is shown on the right of Fig. 1. For cardiac patients with myocardial infarction and bundle branch block, QRS complex has small slope. For slope-based QRS complex peak detection [3, 4], this yields very low output voltage in pre-processing stage and QRS complex peak remains undetected.

To make our algorithm independent of QRS complex slope, we obtain an envelope signal (ECG_ENV) which captures all the peaks of squared signal (ECG_SQR). The peaks are found based on zero-crossing of three-point derivative of the squared signal. Next, this envelope is passed through a 64 point exponential weighted moving average filter [13]. The moving average signal (ECG_AVG) is obtained based on recent sample rather than storing all samples in first in first out memory. This results in smaller silicon area for ASIC design. The moving average filter output peaks correspond to QRS complex peak. The low-pass filter (LPF) (8 Hz) is used to remove noise from moving average filter output. This LPF output is represented by LPF signal as shown in Fig. 1. The division operation of the LPF in ASIC

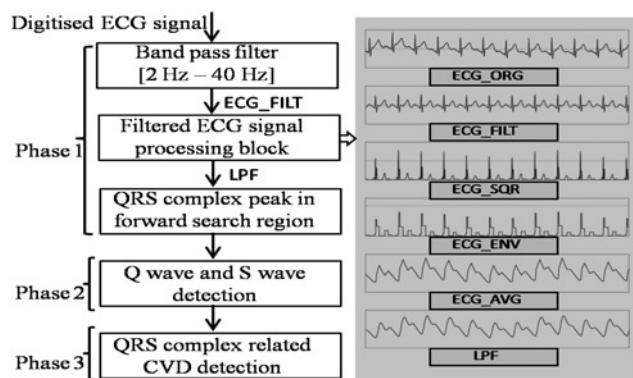


Fig. 1 Flowchart of software algorithm

design is performed using shift operation as the cut-off frequency 8 Hz is a multiple of 2^n .

The signal processing from the filtered ECG signal to the LPF output introduces a time delay D_0 as shown in Fig. 2a. In this Letter, we use forward search which starts from the current peak to the next peak of the LPF output. The window from the current peak to the next peak of the LPF output is called forward search region as shown in Fig. 2a. This forward search does not require memory which makes its ASIC implementation faster, low power and area efficient. Before we start the forward search, we ignored first 2 s of the filtered ECG signal in order to avoid initial transient as shown in Fig. 2a. We find the absolute value of the peak in the filtered ECG signal in each FSR. For detecting the real QRS complex peak in a FSR, we use a threshold value. After initial 2 s marked as ITR (initial threshold region), the first four FSRs are used to determine the initial value of the threshold and used for detecting QRS complex peak in the FSR starting at time T_0 shown in Fig. 2a. The threshold value used in a forward region is the average of the absolute maximum value of peaks in the previous four FSRs. Note that the threshold value is adaptive and depends on the ECG signal in the past four FSRs.

The filtered ECG signal contains real QRS complex peak, tall T wave and tall P wave. The choice of four FSRs ensures at least two real QRS complex peak values are included for calculating the adaptive threshold value. This way, the adaptive threshold value is always higher than the maximum P wave peak value [9]. This ensures that detected peaks are real QRS complex peaks and tall T wave peaks. When a peak is found in filtered ECG signal within an FSR, we have initially selected the peak as a valid peak if its amplitude is greater than the adaptive threshold. In Fig. 2a, valid peaks are marked with filled circles (for real QRS complex peak) and filled rectangles (for tall T wave peak). The tall T waves are detected based on refractory period criteria [14] and QT duration [15]. Let the time interval between the current valid peak and the previous valid peak be $tp-p$. Later, we determine if the current valid peak is a QRS complex peak based on the following three conditions:

- As per physiology, the next QRS complex peak occurs only after the refractory period from the current QRS complex peak is over. The range of mean effective refractory period is from 250 to 300 ms [14]. If $250 \text{ ms} \leq tp-p \leq 300 \text{ ms}$, we compare the current peak magnitude with the previous peak magnitude and select the larger peak as the QRS complex peak. For example, the peak at time T_3 is due to the QRS complex peak and the peak at time T_4 is due to T wave peak as shown in Fig. 2a. Since the QRS complex is always larger than the T wave peak, T wave peak at T_4 marked as multiplication sign in Fig. 2a, is rejected and for the FSR T_3 to T_4 , the peak at T_3 is identified as the valid QRS complex peak.
- To reduce the false detection of T wave peak as a QRS complex peak, we use QT duration. For a normal QT duration of 400 ms [15], QR duration is 40 ms [15] and hence the QRS complex peak to T wave end duration is 360 ms. Therefore, when $300 \text{ ms} \leq tp-p \leq 360 \text{ ms}$, to differentiate a real QRS complex peak from a tall T wave, we determine the ratio of the slope of the rising edge of the two peaks and compare it

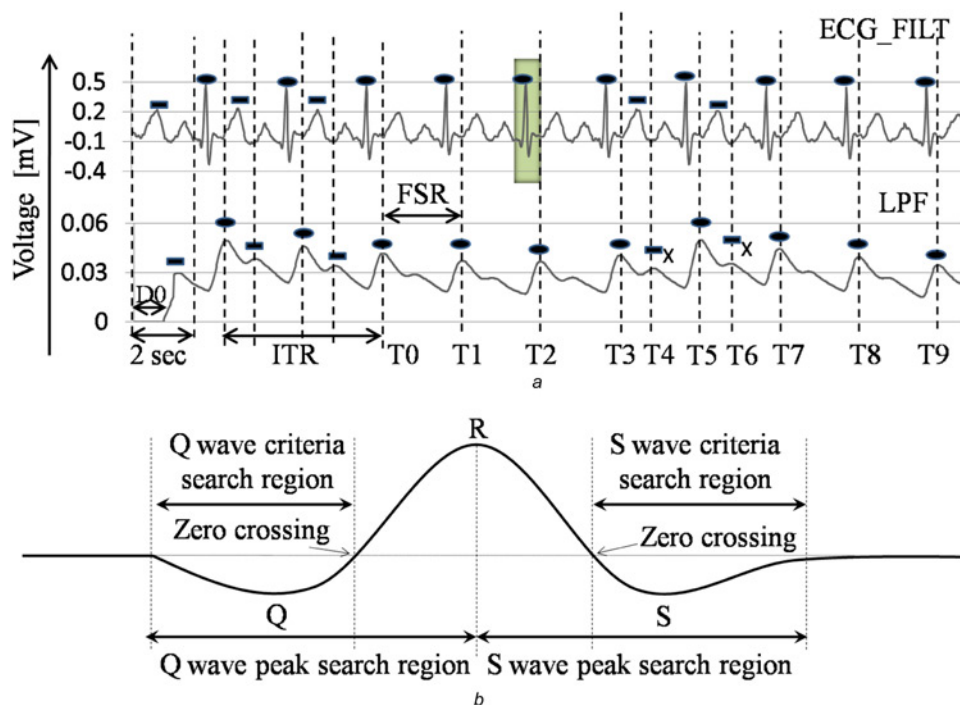


Fig. 2 Forward search concept to find peak of QRS complex

a Forward search region for QRS complex peak

b Forward search region for Q wave peak and S wave peak

to a slope ratio threshold value. If the ratio of the slope is less than the slope ratio threshold value, the current valid peak is identified as a tall T wave peak. The slope ratio threshold is taken as 0.375. This number is derived based on the ratio of minimum slope of rising edge of QRS complex and maximum slope of rising edge of T wave. The slope of rising edge of QRS complex is $16.67 \mu\text{V/ms}$ for the QRS complex duration of 120 ms and the QRS complex peak of 1 mV. The slope of rising edge of T wave is $6.25 \mu\text{V/ms}$ for T wave duration of 160 ms and T wave peak of 0.5 mV [9]. For example, we have a peak due to the QRS complex at time T_5 and peak due to T wave at time T_6 in Fig. 2a and $300 \text{ ms} \leq tp-p \leq 360 \text{ ms}$. The ratio of slope of filtered ECG signal at time T_6 and that at time T_5 is calculated. As this ratio is less than the slope ratio threshold value, the peak at time T_6 is identified as T wave and not a QRS complex peak.

- (iii) If $tp-p > 360 \text{ ms}$, the current valid peak is a valid QRS complex peak. For example, the peaks at T_0 – T_3 , T_5 and T_7 – T_9 in Fig. 2a are selected as valid QRS complex peaks based on this criterion.

There are three main advantages of using forward search scheme as follows: (i) the peak of the filtered ECG signal is automatically detected within each FSR; (ii) there is no need to store filtered ECG samples in memory. For example, the existing literature [3–5] used search back when a QRS complex peak is missed. This search back technique requires memory (SRAM) for ASIC implementation. This leads to increased power dissipation and requires

more silicon area; and (iii) the number of false detections of T wave and P wave peaks as the QRS complex peak reduces significantly. Consequently, we obtain better sensitivity, specificity and FDR. The performance of our algorithm is discussed in Section 4.

2.1. Q wave and S wave detection: We define two FSRs as the S wave peak search region and the Q wave peak search region as shown in Fig. 2b. These search regions are 80 ms duration from the QRS complex peak as shown. There are two criteria to detect Q wave peak in the Q wave peak search region. In the first criteria, Q wave peak is recognised as either a zero slope or a change in sign in the slope of the waveform. In the second criteria, Q wave peak is recognised if three consecutive samples of filtered ECG signal have slopes greater than a slope threshold value. This threshold is taken as one-eighth of the smaller magnitude of the maximum positive and the maximum negative slopes in the QRS complex. If either or both of the criteria are met, the sample point closest to the QRS complex peak is recognised as a Q wave peak. Using the same method, the S wave peak is detected after the QRS complex peak.

2.2. Disease detection criteria: Our objective was to detect arrhythmia, hypertrophy, bundle branch block and intraventricular conduction delay. The arrhythmia detection is based on R – R interval and QRS duration as given in [7]. The left and right ventricular hypertrophy are detected based on scoring criteria as given in [9]. The QRS axis is required to detect hypertrophy. The QRS axis is calculated using the expression given by Mcfarlane and Lawrie [16]. The left bundle branch block [9] is detected

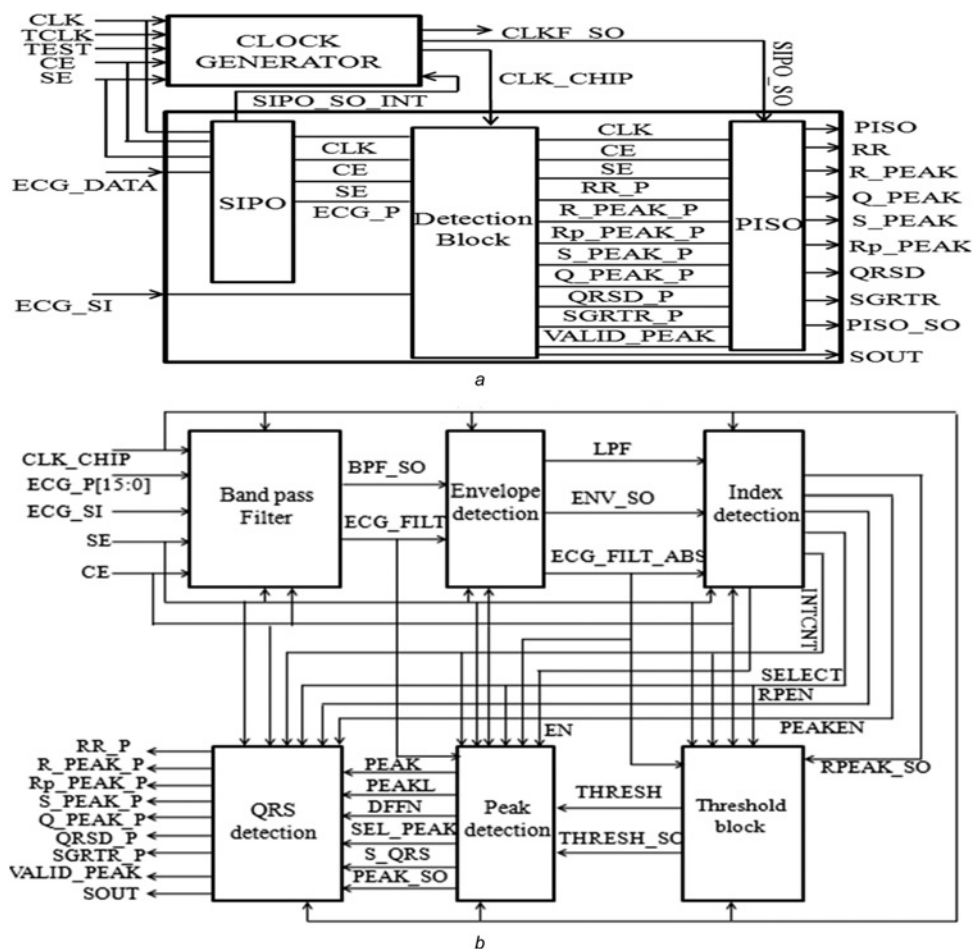


Fig. 3 ASIC block diagram
a ASIC architecture
b Detection block architecture

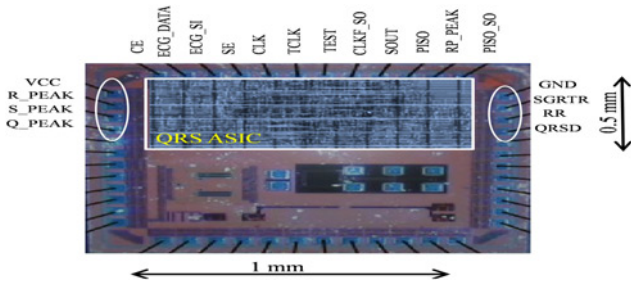


Fig. 4 ASIC fabricated in 130-nm CMOS technology

based on the two conditions. (i) QRS duration in lead I, lead II and lead avL should be equal to or greater than 120 ms; and (ii) Q wave must be absent in lead I and V6. The right bundle branch block [9] is detected based on the three conditions. (i) QRS duration in lead I, lead II and lead avL should be equal to or greater than 120 ms; (ii) In lead V1, secondary R wave amplitude should be greater than or equal to R wave; and (iii) S wave duration should be greater than R wave in lead I or lead II or lead V6. The intraventricular conduction delay [9] is detected if QRS duration is greater than 120 ms. These detection criteria are used in our Android application as explained in Section 4.

3. QRS ASIC design: Our QRS ASIC architecture is based on the algorithm as discussed in the previous section. The ASIC is designed for a single ECG lead and operates at external clock and serial ECG data. The ASIC has four blocks namely as clock generator, SIPO, detection block and PISO as shown in Fig. 3a. We have used a four bit counter to generate a divide by 16 internal clock (CLK_CHIP) inside clock generator. This counter is triggered at the negative edge of the external clock. The most significant bit of this four bit counter is used to drive the internal clock (CLK_CHIP) as shown in Fig. 3a. The incoming serial ECG data is converted into 16 bit parallel ECG data (ECG_P) inside SIPO block. The detection block is operated at the internally generated clock (CLK_CHIP). The signal processing steps of phases 1 and 2 of our algorithm are processed inside the detection block. The parallel 16 bits outputs from the detection block have QRS complex parameters such as R - R interval (RR_P), QRS duration (QRS_P), R wave peak (R_PEAK_P), Q wave peak (Q_PEAK_P), S wave peak (S_PEAK_P), and secondary R wave peak (Rp_PEAK_P). A logic high on signal SGRTR_P indicates whether S wave duration is greater than R wave duration. A logic high on signal VALID_PEAK indicates that 16 bits parallel outputs are valid to convert into serial output by parallel in serial output (PISO) block at the negative edge of PISO signal.

This chip can be operated in normal, scan and test mode. To increase testability of the ASIC, test mode and scan mode are provided. Apart from this, for checking purpose the internally generated clock waveform is available at the output pin CLKF_SO. For scan mode, clock generator scan flip flops are triggered at the rising edge of external clock. The signal SIPO_SO is input to PISO block where this signal is passed through all

Table 2 Disease detection performance for 290 patients in PTB diagnostic ECG database

Disease	Total patients	TP	FN	FP	FDR, %	Se, %	Sp, %
BBB	15	15	0	2	0.69	100.00	99.32
hypertrophy	7	5	2	1	1.03	99.32	99.66
dysrhythmia	14	14	0	1	0.34	100.00	99.66

BBB: bundle branch block

scanned flip flops which are triggered at the rising edge of external clock. The output PISO_SO represents scan output of all flip flops triggered by the external clock. Similarly, there exists another scan path from signal ECG_SI to SOUT for all flip flops triggered at the rising edge of internal clock (CLK_CHIP) inside detection block.

The 16-bit ECG data is filtered using the bandpass filter inside the detection block as shown in Fig. 3b. The output of the bandpass filter is input to the envelope detection block where we perform square operation, envelope detection, 64 point moving average and low-pass filtering. The square of filtered ECG signal data (16 bits) is obtained using the array multiplier. The squared signal width is 33 bits, where the 33rd bit represents the sign bit. The peaks in the envelope signal (ECG_ENV) are found based on the zero-crossing of 33-bit squared signal data as mentioned in Section 1. The zero-crossings are detected based on the sign bit of three-point derivative of the squared signal. The three-point derivative signal is obtained by using a 33-bit subtractor circuit. This signal processing corresponds to filtered ECG signal processing block shown in Fig. 1. The peak of the LPF output is found in the index detection block. The enable signal (EN) is generated in the index detection block after initial 2 s and the ITR for adaptive threshold calculation. This signal represents time T_0 as shown in Fig. 2a. This is to make sure that we have a valid adaptive threshold after first 2 s and the ITR. When a peak is detected in the LPF output, the signal SELECT is sent to threshold block, peak detection block and QRS detection block. This signal represents time stamp (T_0 , T_1 , T_2 etc.) shown in Fig. 2a. The QRS detection block detects QRS complex parameters based on QRS complex peak location (PEAKL). The QRS detection block is enabled only after receiving S_QRS signal, which is generated based on gating of SELECT and EN signals. This gating reduces ASIC dynamic power significantly.

The RTL implementation of the ASIC was written in Verilog hardware description language. The gate level netlist was generated by Synopsys design compiler. The placement and routing was performed using Cadence chip encounter. The post layout simulations were verified using Mentor Modelsim. The static timing analysis was performed using Synopsys Primitime. The Cadence chip encounter generated design netlist and design GDSII file. The cadence virtuoso generated schematic and layout view based on this design netlist and GDSII file. The output pads were added manually and routed. The physical verification of final GDSII file is performed using Mentor Calibre tool. The core area of ASIC is $1 \times 0.5 \text{ mm}^2$ as shown in Fig. 4. The bottom area of the chip is used by other research teams.

Table 1 Algorithm comparison for MIT-BIH arrhythmia database

Algorithm	Total beats	TP	FP	FN	FDR, %	Se, %	Sp, %
this work	109,496	109,329	80	167	0.23	99.85	99.93
[3]	109,267	108,927	248	340	0.54	99.69	99.77
algorithm 1 [17]	110,050	109,548	376	341	0.65	99.69	99.66
algorithm 2 [17]	110,050	109,615	386	288	0.61	99.74	99.65
[18]	109,428	109,208	153	220	0.34	99.80	99.86

For algorithms 1 and 2 [17], FP and FN includes shifted false negative errors and shifted false positive errors, respectively

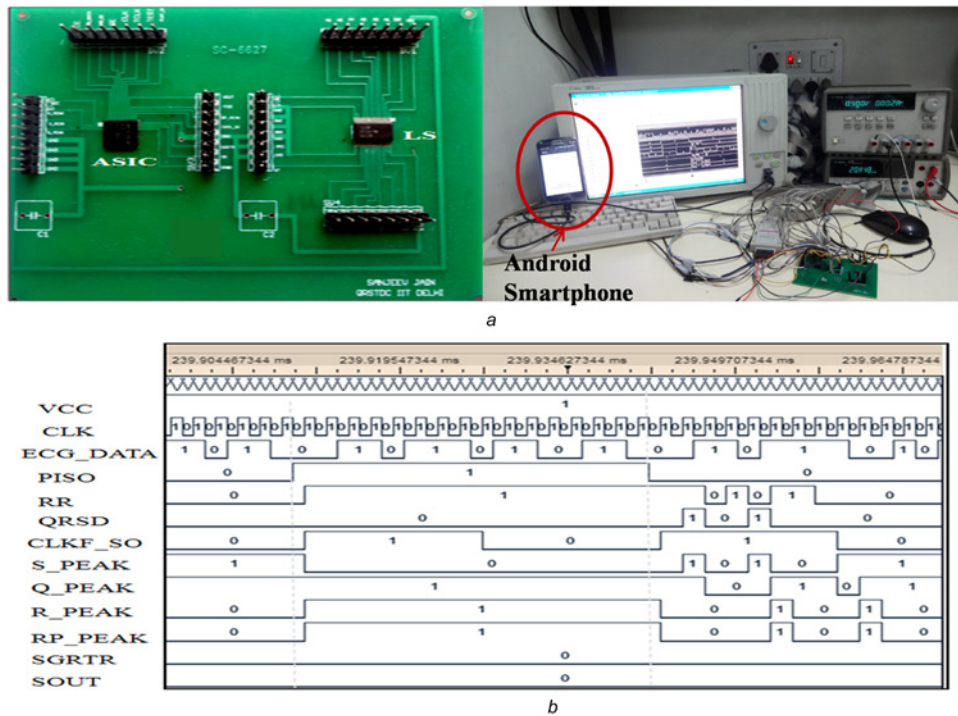


Fig. 5 ASIC testchip setup
a Printed circuit board and testchip setup
b Testchip waveform

4. Experiment results: Our objective is to detect the QRS complex related cardiovascular diseases using six ECG lead data as explained in Section 2. To benchmark our algorithm with the existing QRS complex peak detection algorithm [3, 17, 18], we also evaluated our algorithm using lead II data of MIT-BIH arrhythmia database [10, 11]. In Table 1, our results are compared with those of Hamilton algorithm [3] and Christov algorithm [17]. Both of these algorithms are based on derivative approach and use adaptive thresholds. Table 1 also includes comparison with a wavelet-based algorithm [18] that used multiscale threshold approach.

Martinez *et al.* [18] have compared the performance of their algorithm with other algorithms (see Table 2 in [18]). For brevity, we have not included algorithm comparisons that are already given in Table 2 in [18]. Note that total beats reported in [17] are

higher as compared to other reported works as well as our work. The higher number of total beats in [17] is for record 213 and record 231. The total number of beats detected by our algorithm for record 213 and record 231 match the number of beats given in MIT-BIH arrhythmia *R-R* interval database. In Table 1, we have included our algorithm's performance comparison with the existing algorithms on all three parameters viz sensitivity, specificity and FDR. Note that the data in Table 1 consists of all annotated beats of MIT-BIH arrhythmia database except ventricular flutter waves of record 207. The sensitivity and specificity of our algorithm are 99.85 and 99.93%, respectively. The FDR of our algorithm is 32% lower as compared to wavelet-based algorithm [18] that offers the best FDR in the literature.

Our QRS ASIC is tested for PTB diagnostic ECG database for six leads (I, II, avL, V1, V3 and V6). The sampling frequency of

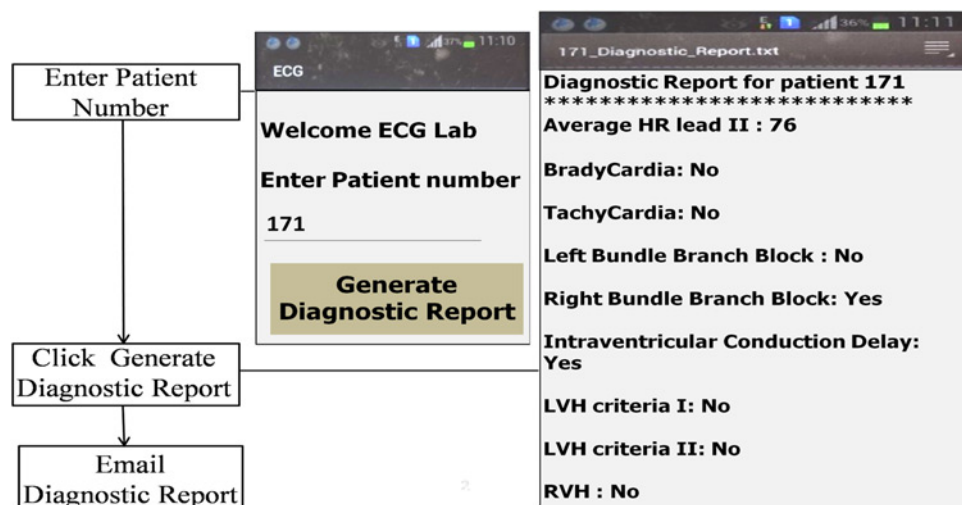


Fig. 6 Android application to process ASIC output

Table 3 ASIC comparison

Ref	Tech, μm	Area, mm^2	Leakage power, μW	Dynamic power, nW	Power, μW	Energy	Supply Voltage, V	Frequency, kHz	Simulation/ measurement	Database	Se, %	Sp, %	FDR, %	Function ^a
this work (HS)	0.13	0.22	0.762	1.85	0.764	0.76 nJ	0.6	1	measurement	PTB	99.93	99.92	0.16	1
										MITDB	99.85	99.93	0.23	
		0.5	1.728	4.5	1.73	1.74 nJ	0.6	1	measurement	PTB	99.93	99.92	0.16	3
this work (LL)	0.13	0.22	0.018	1.79	0.02	18 pJ	0.9	1	simulation	PTB	99.93	99.92	0.16	1
										MITDB	99.85	99.93	0.23	
		0.5	0.041	4.25	0.045	45 pJ	0.9	1	simulation	PTB	99.93	99.92	0.16	3
[19]	0.13	0.016	NA ^b	NA	0.447	NA	1.2	5	simulation	MITDB	99.89	99.4	1.71	2
[20]	0.35	1.2	NA	NA	13.6	NA	3	1	measurement	MITDB	99.9	99.91	0.196	1
[21]	0.18	1.2	NA	NA	9	NA	1.1	32	measurement	MITDB	99.8	99.86	0.35	1
[22]	0.35	1.11	NA	NA	0.83	NA	1.8	0.3	measurement	MITDB	99.31	99.7	0.99	1
[23]	0.09	7.03	NA	NA	NA	13 pJ	0.4	1K	measurement	NA	NA	NA	NA	1
[24]	0.065	0.02	NA	NA	NA	0.88 pJ	0.33	20	measurement	NA	NA	NA	NA	1
[25]	0.18	0.68	NA	NA	2.21	NA	NA	0.5	measurement	MITDB	95.65	99.36	4.97	1
[26]	0.5	9	0.013	NA	10	NA	5	1K	measurement	PTB	NA	NA	NA	2
[27]	0.18	1.1	NA	NA	176	NA	1.8	1K	measurement	MITDB	99.63	99.89	0.48	1
[28]	0.13	5.98	NA	NA	2.6	NA	3.3	475	simulation	NA	NA	NA	NA	1
[29]	0.13	1	0.0678	46.7	0.114	114.5 pJ ^c	1.2	1	simulation	NA	NA	NA	NA	1

^aFunction: (1) QRS complex peak detection; (2) RR interval and variability; and (3) QRS complex parameters for cardiovascular disease detection which include R–R interval, QRS duration, R peak, Q peak, S peak, secondary R peak, R wave duration and S wave duration

^bNA: Not available. The authors have not reported these parameters for their work

^cEnergy is calculated based on dynamic power and leakage power as given in [29]

six leads ECG data is 1000 Hz for this database. These signals are downsampled to 250 Hz using MATLAB. The ASIC testchip setup includes a printed circuit board as shown at the left of Fig. 5a.

The complete testchip setup is shown on the right of Fig. 5a which includes a power supply, the printed circuit board, a computer with Agilent pattern generator, logic analyser and a smartphone. The input signal information is read by Agilent pattern generator, which generates inputs for our ASIC. The minimum voltage level of ASIC inputs from Agilent pattern generator is 2.5 V. The maximum operation voltage of our ASIC is 1.8 V. Therefore, we use level shifter (LS) in printed circuit board to convert input voltages from higher voltages (3.3–2.5 V) to lower voltages (1.8–0.6 V). The ASIC outputs are processed by logic analyser and displayed in the waveform window as shown in Fig. 5b for lead II of patient record 207 of PTB diagnostic ECG database. Therefore, the cardiac events (phases 1 and 2 of our software algorithm) are detected by our ASIC. We process six ECG leads data sequentially using our ASIC. The outputs of ASIC for six leads are stored in six CSV files in logic analyser. The Android phone is connected through USB cable to receive these CSV files as shown in Fig. 5a.

An Android application is developed which reads data from six CSV files and process disease detection criteria as explained in Section 2.2. This Android application has three steps to send cardiovascular disease diagnostic report to a cardiologist through email services available on Android smartphone. The three steps are shown in Fig. 6. Once a user enters a patient number, android application reads six CSV files and generates a diagnostic report based on coded disease detection criteria.

We have also executed our algorithm on an Android phone having 1.2 GHz processor and 1 GB RAM. The execution time for phases 1 and 2 of our algorithm for 2 min single lead data is 8 s. The execution time in our ASIC is 0.48 s for a clock frequency of 1 MHz. Therefore, the ASIC is 16.67 times faster with a 1200 times slower clock. For arrhythmia detection [7], the ECG recording of 24–48 h is processed offline for diagnosis. If we process 48 h ECG data in an Android phone, the execution time is 3.2 h for a single lead if data is segmented in 2 min interval. Our QRS ASIC can process this data in 11.52 min for a single lead.

Table 2 shows the disease detection performance of our QRS ASIC for 290 patients in Physionet PTB diagnostic ECG database. In this database, there are 15 patients with bundle branch block, 7 patients with hypertrophy and 14 patients with dysrhythmia (generally known as arrhythmia [9]). The remaining patients of this database have other diseases not covered in this Letter. The sensitivity and specificity for each disease are obtained based on total 290 patients of this database. We achieve 100% sensitivity for bundle branch block and dysrhythmia. The FDR for hypertrophy is 1.03 as we detect ventricular hypertrophy in five patients out of seven patients. The two patient records patient159/s0390lre and patient250/s0485_re do not have ventricular hypertrophy.

Table 3 summarises the comparison of our ASIC with published ASICs and SOC's from the point of view of area, leakage power, dynamic power, total power, total energy, sensitivity (Se), specificity (Sp), FDR and its function. We have listed both dynamic power and leakage power dissipation in Table 3. The dynamic power, leakage power and total power dissipation are obtained using Synopsys PrimePower tool for Physionet PTB diagnostic ECG database. The energy dissipation is also listed. Our ASIC for cardiovascular disease detection is fabricated using 130-nm CMOS high speed process technology. In our ASIC, 0.22 mm² is devoted for QRS complex peak detection. The total area of the ASIC is 0.5 mm². The dynamic power dissipation is 4.5 nW at the operating frequency of 1 kHz with a supply voltage of 0.6 V. We have also implemented a low leakage version of our ASIC. The ASIC dissipates only 45 pJ with a supply voltage of 0.9 V. Our ASIC besides detecting QRS complex peak detects QRS complex parameters (*R*–*R* interval, QRS duration, *R* peak, *Q*

peak, *S* peak, secondary *R* wave peak, *R* wave duration and *S* wave duration) and consumes only 45 pJ.

The existing ASICs and SOC's [19–29] detect QRS complex peak. Some of these [19, 26] additionally detect RR interval variability. To compare the performance of our implementation with the existing work [19–29], we have also determined the area, leakage power, dynamic power, total power, total energy required in our ASIC for detecting QRS complex peak. The ASICs reported in [20, 21, 25–28] consumes much larger power as compared to the ASICs reported in [23, 24, 29]. The ASIC in [29] used UMC 130-nm low leakage standard cells with sleep transistors. The energy dissipated in [29] is 114.5 pJ. Our low leakage implementation when operated at the same supply voltage of 1.2 V and at operating frequency of 1 kHz, the energy dissipation is 35.2 pJ. The supply voltages for ASICs reported in [23, 24] are 0.4 and 0.33 V, respectively. If our ASIC is implemented in 90-nm or 65-nm technology as in [23, 24], we expect to get comparable energy dissipation for the QRS complex peak detection.

Simplification of ADC and processor design by using 7 bits digital signal processing results in least area in [19], but results in large FDR of 1.71. The larger FDR is not acceptable for cardiovascular disease detection system. The next lowest area is achieved in [24] using 65-nm CMOS process technology, which is the same design as [29] in 130-nm technology. The ASIC area in [29] is larger than our implementation for the QRS complex peak detection. Note that for the QRS complex peak detection for MIT-BIH arrhythmia database, our implementation achieves very low FDR. The average FDR in our ASIC is 0.16% for six leads of PTB diagnostic ECG database which is quite satisfactory.

5. Conclusions: A cardiovascular disease detection algorithm based on forward search is presented in this paper. For QRS complex peak detection, our algorithm achieves sensitivity of 99.86% and specificity of 99.93% for MIT-BIH database. Based on the forward search algorithm an ASIC with low energy dissipation and small area is implemented. The ASIC is fabricated using UMC 130-nm high speed standard cells and dissipates 1.74 nJ with a supply voltage of 0.6 V for clock frequency of 1 kHz. The average FDR in our ASIC is 0.16% for six leads data of 290 patients in PTB diagnostic ECG database. The low leakage implementation of proposed ASIC dissipates only 45 pJ with a supply voltage of 0.9 V. Our proposed ASIC is an energy efficient device for telemetry cardiovascular disease detection system. The cardiovascular disease detection criteria have been coded into Android app. Based on QRS complex parameters obtained from ASIC, the Android app generates user friendly diagnostic report, which can be sent to a cardiologist via email facility available on Android smartphone.

6. Conflict of interest: The authors have a patent pending 'QRS Complex Identification in Electrocardiogram Signals', US patent office application number: 14/573,037.

7. Acknowledgment: The authors acknowledge Ravi Informatics for soldering the packaged IC on PCB. The authors also thank Texas Instruments (India) Pvt Ltd for providing SN74AVC8T245, a voltage level shifter IC which they have used to interface their chip with a Logic Analyzer.

8 References

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