

**DESIGN AND ANALYSIS OF HIGH POWER AND LOW
HARMONIC RF FRONT END FOR MULTI BAND WIRELESS
APPLICATION**

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**DESIGN AND ANALYSIS OF HIGH POWER AND LOW
HARMONIC RF FRONT END FOR MULTI BAND WIRELESS
APPLICATION**

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TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	iii
LIST OF TABLES	viii
LIST OF FIGURES	ix
LIST OF SYMBOLS AND ABBREVIATIONS	xvi
SUMMARY	xvii
CHAPTER 1	1
CHAPTER 2	7
2.1. Impedance Transform Methods	9
2.2. Multi-Stacked FETs	11
2.3. LC Resonator Circuits	12
2.4. Substrate body tuning technique in CMOS high power switch	14
CHAPTER 3	17
3.1. A High Power CMOS SP4T Switch Using a Switched Resonator for Dual Band Application	18
3.1.1. Switched Resonator at Receiver Switch	19
3.1.1.1 Dual mode operation of the switched resonator	20
3.1.1.2 Dual band operation of the switched resonator	23
3.1.2. Simulation Results	25
3.1.3. Measurement Data and Design Issue	26
3.2. A High Power CMOS Switch Using Multi Gate Structure	28
3.2.1. Multi-Gate Device in RF and Digital Circuits	28

3.2.2.	RF CMOS Switch Device – Four port device	29
3.2.3.	High Power SPDT switch Design	32
3.2.4.	RF Switch Measurement	34
3.2.5.	Summary	37
3.3.	A High Power CMOS Switch Using Substrate Body-Switching in Multi-Stack Structure	39
3.3.1.	Method of Power-Handling Improvement	40
3.3.2.	SP4T Switch Design and Measurement Data	45
3.3.3.	Summary	49
CHAPTER 4		50
4.1.	Introduction.	50
4.2.	A Novel Multi-Stack Device Structure and its Analysis for High Power CMOS Switch Design.	53
4.2.1.	High power Switch Design.	53
4.2.1.1.	Operation of Conventional Multi-Stack Structure Switch	54
4.2.1.2.	Operation of Proposed Multi-Stack Structure	56
4.2.1.3.	Measurement Results	60
4.2.1.4.	Summary	63
4.3.	A High Power CMOS Switch using a Novel Adaptive Voltage Swing Distribution Method in Multi-Stack FETs	64
4.3.1.	Analysis of Voltage Swing Behavior in the CMOS Switch	64
4.3.1.1	A Single CMOS Switch with Resistive Body Floating Technique	65

4.3.1.2	A Multi-Stack CMOS Switch with Resistive Body Floating Technique	69
4.3.1.3	Operation of the Adaptive Voltage Swing Distribution Method in the Multi-Stack FET Structure	70
4.3.2.	SPDT Switch Using A Novel Adaptive Voltage Distribution Method in the Multi-Stack FETs	75
4.3.3.	Experimental Results	79
4.3.3.1	Power-Handling Capability in the Series-Shunt Configuration	80
4.3.3.2	S-parameter Measurement	81
4.3.3.3	Measured 0.3 dB Compression Point	82
4.3.3.4	Second and Third Harmonics	85
4.3.4.	Summary	86
4.4.	Layout Consideration of the CMOS switch in the Multi-Stack Structure	88
4.4.1.	Equivalent Circuit Model considering the Substrate Junction Diodes	88
4.4.2.	Measurement Results	92
4.5.	High Power Switch Design using Feed-Forward Capacitor	95
4.5.1.	Feed Forward Capacitor Method	95
4.5.2.	Measurement Results	100
4.5.3.	Summary	103
CHAPTER 5		105
5.1.	Design of multi band and multi mode GaAs switch with CMOS driver	106
5.1.1.	Measurement data of the SP7T switch using GaAs pHEMT technology	109
5.2.	Layout Consideration of the SPMT switch Design	113

5.3. Design of multi band and multi mode GaAs switch with integrated driver	116
5.4. Design switch IC of multi band and multi mode GaAs switch with integrated driver	117
CHAPTER 6	121
REFERENCES	126
PUBLICATIONS	128
VITA	130

LIST OF TABLES

	Page
Table 1: Performance of the GaAs SP9T switch: Insertion loss	110
Table 2: Performance of the GaAs SP9T switch: Harmonic performance	110
Table 3: Insertion losses of the SP7T switch	111
Table 4: Return losses of the SP7T switch	111
Table 5: Harmonic performance of the SP7T switch	111
Table 6: Insertion loss of the SP7T switch	119
Table 7: Harmonic performance of the SP7T switch	119

LIST OF FIGURES

Fig. 1.1. The prospect of GSM/UMTS cellular phone market.	2
Fig. 1.2. Prospect of the antenna switch market	3
Fig. 1.3 Functional building blocks of the RF-transceiver architecture.	4
Fig. 1.4. Voltage swing behavior in a CMOS switch (a)., (b) Small signal input, and (c) Large signal input	5
Fig. 2.1. Simplified series shunt switch	7
Fig. 2.2. Voltage swing at the drain and gate terminal at the OFF-state switch.	8
Fig. 2.3. (a) SPDT switch diagram, (b) Impedance diagram of the simplified SPDT switch with Tx ON state.	10
Fig. 2.4. SPDT switch structure using three stacked FETs	11
Fig. 2.5. Basic operation of LC resonant switch circuits in the receive switch	13
Fig. 2.6. Voltage swing at each node in the CMOS switch with body floating technique.	15
Fig. 2.7. (a) CMOS switch. (b) CMOS switch with body floating using LC resonant tank (c) CMOS switch using body floating technique using Deep N-well process.	16
Fig. 3.1. Basic operation of LC resonator at receiver switch.	19
Fig. 3.2. SP4T switch using switched resonator at Tx mode.	21
Fig. 3.3. SP4T switch using switched resonator at Rx mode.	22
Fig. 3.4. Performance comparison by L1/L2 ratio	22
Fig. 3.5. (a) multi stacked switch at TX path (b) Simplified equivalent model of switch with signal flow.	24
Fig. 3.6. Receiver switch simulation results.	25

Fig. 3.7. Transmit switch simulation results: Power handling capability and Isolation from Ant to Rx.	26
Fig. 3.8. Layout of SP4T CMOS switch using switched resonator with 1.7 mm by 0.9 mm dimension.	27
Fig. 3.9. .1 dB compression point of the CMOS switch at 1.9 GHz.	27
Fig. 3.10. Basic schematic and layout of multi-gate structure	29
Fig. 3.11. Equivalent model of three stacked FETs with body floating technique.	30
Fig. 3.12. Equivalent model of triple gate transistor	30
Fig. 3.13. Cross-sectional view of the triple gate transistor.	31
Fig. 3.14. Cross-sectional view of the dual gate transistor.	32
Fig. 3.15. Schematic of SPDT switch using the triple gate structure at the Rx switch.	33
Fig. 3.16. Tx insertion loss and isolation of SPDT switch using the triple gate structure in the Rx switch.	34
Fig. 3.17. Insertion loss and isolation of the SPDT switch using the triple gate structure in case of a Rx mode operation.	35
Fig. 3.18. 1dB compression point of the triple gate FET and the dual gate FET at 1.9 GHz.	36
Fig. 3.19. S-parameter performance of the test structure of the dual gate.	36
Fig. 3.20. Photograph of multi-gate structure (a) SPDT switch using a triple gate (b) dual gate test structure.	38
Fig. 3.21. Basic concept of substrate body-switching (a) schematic of Rx switch (b) body-switch turning on when Tx mode switch is in ON state (c) body-switch turning off when Tx switch is in OFF state.	39

Fig. 3.22. Voltage swing at each parasitic capacitor. CGD and CGS (Pin=30 dBm).	41
Fig. 3.23. Equivalent circuit models of (a) the switch with body grounded and (b) the switch with body floating, both in OFF state.	42
Fig. 3.24. Schematic of SP4T switch using body switching technique.	45
Fig. 3.25. Photograph of the SP4T switch using body switching technique	46
Fig. 3.26. Measurement data of the Tx switch performance.	47
Fig. 3.27. P1dB performance of the TX switch.	47
Fig. 3.28. Measurement data of Rx switch performance. Insertion loss improvement by body-switch operation.	48
Fig. 4.1. Equivalent lumped element model of the conventional multi-stack structure.	54
Fig. 4.2. Voltage swing dividing of conventional multi-stack switch in OFF state (24 dBm input power).	56
Fig. 4.3. Proposed multi stack structure CMOS switch.	57
Fig. 4.4. Equivalent lumped element model of the proposed structure in the OFF-state.	57
Fig. 4.5. Voltage swing of the proposed multi-stack structure.(24 dBm input power).	58
Fig. 4.6. Leakage current of the conventional multi-stack structure and the proposed multi-stack structure in OFF state.	60
Fig. 4.7. Photographs of test structures. (a) Conventional structure and (b) proposed structure.	61
Fig. 4.8. .Measured isolation of test structures with respect to input power level at 900 MHz.	62
Fig. 4.9. The measurement-data comparison of the isolation and the insertion loss between the conventional structure and the proposed structure.	62

Fig. 4.10. Cross-sectional view of an NMOS transistor in a deep N-well structure.	65
Fig. 4.11. Equivalent circuit models of a CMOS switch using resistive body floating technique (a) in ON-state and (b) in OFF-state.	66
Fig. 4.12. Voltage swing behavior simulation of a single NMOS switch with resistive body floating technique (a) in ON-state and (b) in OFF-state.	68
Fig. 4.13. (a) Conventional multi stack FETs (b) the multi stack FETs using adaptive voltage swing distribution with substrate body switching technique.	70
Fig. 4.14. Impedance variation of conventional multi-stack FETs and proposed multi-stack FETs according to the input power level.	71
Fig. 4.15. Equivalent circuit model of the proposed multi-stack FETs using the adaptive voltage swing distribution in Fig. 4.13 (b).	72
Fig. 4.16. Simulation of adaptive voltage swing of the proposed multi-stack structure in a SPDT switch.(30 dBm input power).	73
Fig. 4.17. Simulation of VGS and VGD at each node in the equivalent circuit model shown in Fig.7 (30 dBm input power).	74
Fig. 4.18. Two different kinds of four stacked SPDT switch configurations using the adaptive voltage swing distribution method. (a) Type A, and (b) Type B. (Size of the device: Tx FET W/L:1.5mm/0.35 μ m, Rx FET:700 μ m/0.35 μ m. Resistors: 10K ohm).	75
Fig. 4.19. Voltage swing simulation of the structure of type-A in Fig. 10 (a) (30 dBm input power).	77
Fig. 4.20. Voltage swing simulation of the structure of type-B in Fig. 10 (b) (30 dBm input power).	77

Fig. 4.21. Voltage difference simulation between gate and source at M4 in type-A and type-B in Fig.10 (28 dBm and 33.5 dBm input power level).	78
Fig. 4.22. Micro-photograph of the fabricated SPDT switches (a) type-A in Fig. 10 (a) and (b) type-B in Fig. 10 (b). (size of the switches : 1000 um X 400 um)	80
Fig. 4.23. Measured power handling capability of the Rx switches(OFF state) using series-shunt configuration at 1.9 GHz.(ANT-input port, Tx-output port(series ON) and Rx-grounded(shunt-OFF state))	81
Fig. 4.24. Measured S-parameters of Tx switch.	82
Fig. 4.25. Measured S-parameters of Rx switch.	83
Fig. 4.26. Measured 0.3 dB compression point of the type-A and type-B structure in an SPDT configuration at 1.9 GHz.	84
Fig. 4.27. Measured the second and third harmonics of the type-A structure, and the type-B structure, respectively, at 1.9GHz.	86
Fig. 4.28. (a) the cross sectional view of the NMOS device and (b) equivalent circuit model of the NMOS device considering the substrate junction diodes and capacitors.	89
Fig. 4.29. Equivalent-circuit model of the four-stacked CMOS switch in Fig. 4.18 (b) with consideration of the substrate-junction diodes.	90
Fig. 4.30. Proposed equivalent-circuit model of the four-stacked CMOS switch.	91
Fig. 4.31. Layout of the CMOS switch employing the individual bias resistor at the each N-well of the device	92
Fig. 4.32. 1 dB compression point and the second and the third harmonics.	93
Fig. 4.33. Channel formation of the OFF-state device	96
Fig. 4.34. Schematic of the SPDT switch using the feed forward capacitor.	97

Fig. 4.35. Voltage swing difference between source and drain in Fig. 4.34	98
Fig. 4.36. Voltage swing (a) at source, (b) gate, (c) drain and gate and (d) source and gate.	98
Fig. 4.37. Safe voltage swing region of the switch device.	100
Fig. 4.38. Photograph of the CMOS switch using the Feed-forward capacitor	101
Fig. 4.39. Measured S-parameters of Tx switch	101
Fig. 4.40. Measured Rx switch performance. (S-parameters)	102
Fig. 4.41. 1dB compression point of the SPDT switch according to the value of the feed-forward capacitors (1.9GHz).	103
Fig. 5.1.(a). Microphotograph of the commercial products of GaAs SP8T switch, and (b). Schematic of the GaAs SP8T switch.	106
Fig. 5.2. Different version of SP9T switch designs for the multi mode and multi band operation.	107
Fig. 5.3. Photograph of the SP7T switch assembled on the COB	110
Fig. 5.4. (a) SPDT switch with series shunt configuration. (b) M2 and M3 in ON state , M1 and M4 in OFF state , and (c) impedance matching configuration.	113
Fig. 5.5. Schematic of the inverter core implemented in E/D mode p-HEMT process.	114
Fig. 5.6. Schematic of the SP7T switch with decoder integrated	116
Fig. 5.7. (a) multi-stack FETs and (b) multi-gate FET	117
Fig. 5.8. Notch filter implementation at the antenna pad	118

LIST OF SYMBOLS AND ABBREVIATIONS

IC	Integrated Chip
GaAs	Gallium Arsenide
CMOS	complimentary-metal-oxide-semiconductor
ASM	antenna switch module
GSM	Global System for Mobile communications
UMTS	Universal Mobile Telecommunications System
GPRS	global packet radio service
EDGE	Enhanced Data rates for GSM Evolution
RF	radio frequency
PAs	power amplifiers
LNAs	low noise amplifiers
VCOs	voltage controlled oscillators
PCS	personal communication systems
FETs	field-effect transistors
LC	Inductors and Capacitors
SPDT	Single pole double throw
SP7T	Single pole seven throw
SP9T	Single pole nine throws
SPMT	Single pole multi throws
Tx	Transmit
Rx	Receive
SOI	Silicon on Insulator
P1dB	1 dB compression point
RL	Return Loss
IL	Insertion Loss
Iso	Isolation
pHEMT	Pseudomorphic High Electron Mobility Transistors

SUMMARY

The objective of this research is to demonstrate the feasibility of the implementation of low-cost, small-size, and high power RF front ends using CMOS technology which has been known not to be suitable for high-power applications due to its material characteristic. One part of this research focuses on developing GaAs switches for multi band and multi mode high power applications.

The development of RF front end switches for high power applications using CMOS technology is challenging in that the characteristics of CMOS technology such as low breakdown voltages, slow electron mobility and existence of substrate junction diodes are limiting power handling capability of CMOS technology. Various topologies of CMOS switches have been employed in implementing high power RF front end CMOS switches in order to overcome material limitations of CMOS technology in high power applications. Based on measurement data such as power handling capability and S-parameters of fabricated CMOS switches, the feasibility of use of CMOS technology in high power RF antenna switch design has been studied, and novel methods of designing CMOS switches to improve the power handling capability without compensating S-parameter performance are proposed. As a part of this research, multi-band and multi-mode power switches using GaAs technology are fabricated and tested for use of the commercial applications such as handsets covering GSM, PCS/DCS, and UMTS bands. Current commercial RF switch products demand small size, low cost and low voltage control as the number of wireless standards integrated in a single application increases. This research provides a solution for commercial products which can meet all the specifications as well as needs required in the wireless market.

CHAPTER 1

INTRODUCTION

The explosive growth of wireless communication was due to the huge success of cellular phones with the public. When wireless technology belonged to captive markets like the military, broad-casting stations, and the maritime or aircraft industry, the most important factor was not size and cost, but performance of the technology[1]. The necessities of reduced size and low cost accompanied the rapid growth of the number of mobile telecommunication users. The demand of small size for wireless communication products has accelerated development of the integrated chip (IC) industry. Most of the ICs in hand-held applications had been implemented using the gallium arsenide (GaAs) process in the early stage of the cell phone booming era. However, the necessity of low cost and integration with digital circuitry has boosted research on the transition from GaAs technology to complimentary-metal-oxide-semiconductor (CMOS) technology[2, 3]. However, the physical limitation of the characteristics of CMOS technology prevents the CMOS process from being applied to high-power applications. Consequently, design of new circuitry is required to overcome this problem. This chapter introduces the economic and technological motivation for designing high power CMOS switches. This chapter begins with an overview of the market data regarding the wireless communication industry. Subsequently, the direction of the antenna switch module (ASM) market is illustrated. The necessity of the integration of the antenna switch in ‘On-chip’ is discussed. Finally, the last section outlines the organization of the dissertation.

Fig. 1.1 shows the prospect of the Global System for Mobile communications (GSM) and the Universal Mobile Telecommunications System (UMTS) market.

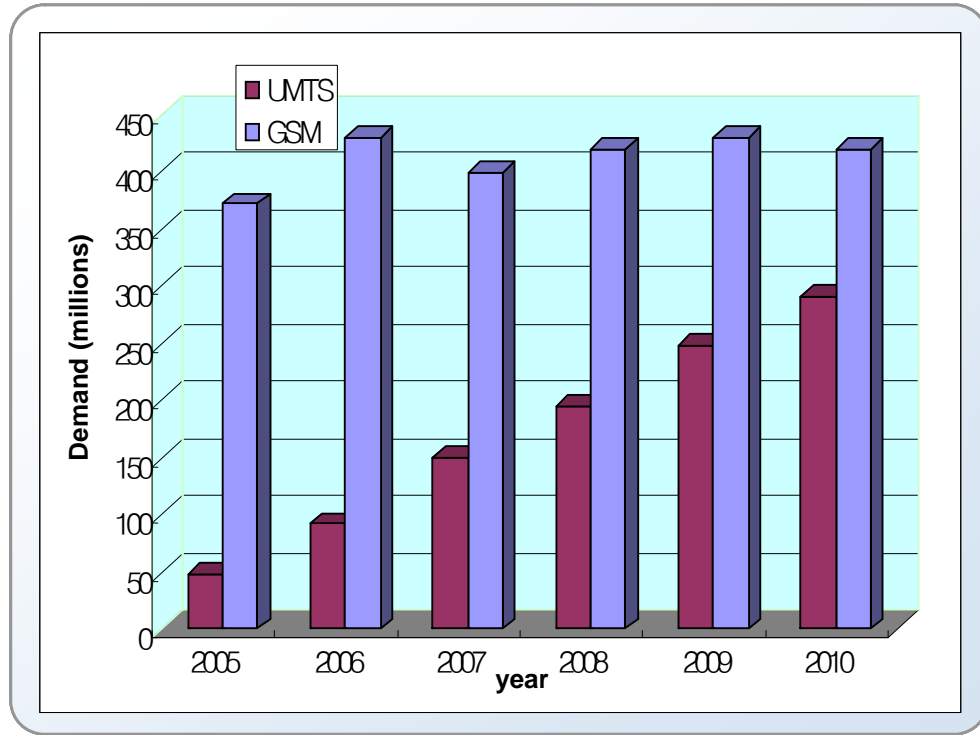


Fig. 1.1. The prospect of GSM/UMTS cellular phone market.

A cellular phone is one of the major marketable products for wireless communication industry. For the last decade, the GSM market leads the wireless communication industry by its explosive growth. However, referring to Fig. 1.1, the GSM market approaches some saturation point. In the meanwhile, the market for UMTS expects significant growth within a couple of years from now. Therefore, the cellular phone providers started to introduce new model of the next-generation wireless telephone that integrates the next generation wireless standard in one application. The wireless standards are following; GSM, global packet radio service (GPRS), enhanced data rates for GSM evolution (EDGE) and UMTS. Fig. 1.2 shows the prospect of the antenna switch market according to the cellular phone market[4].

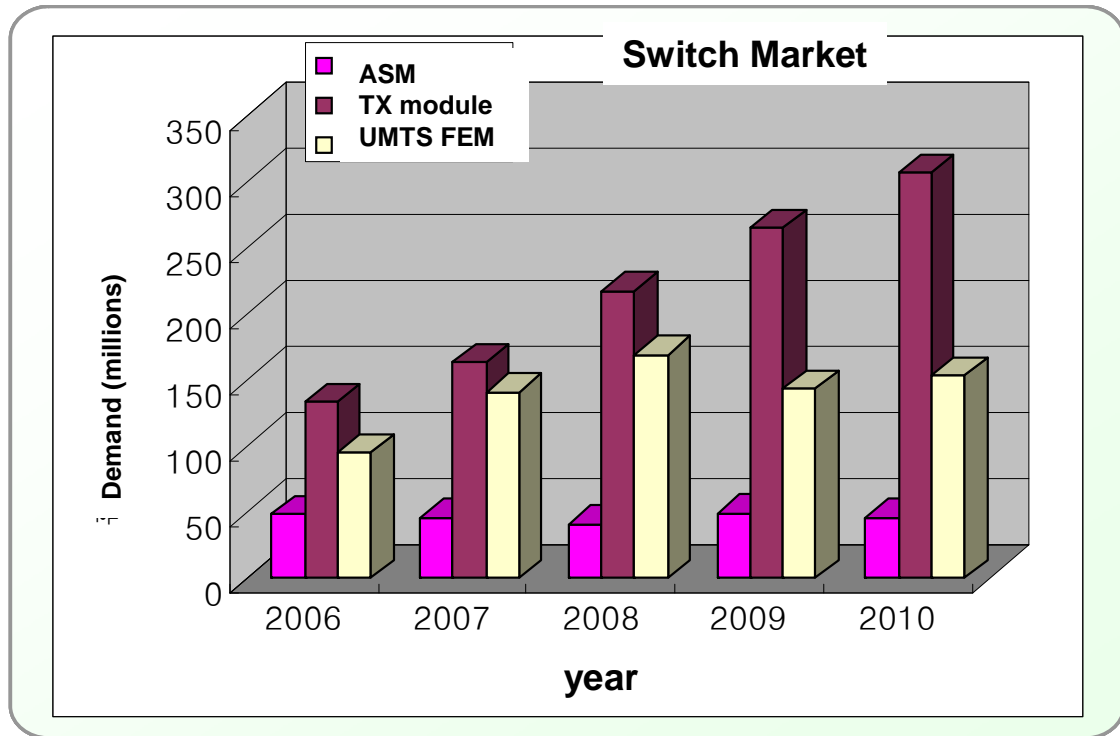


Fig. 1.2. Prospect of the antenna switch market

As the different types of wireless standards become integrated into one application, the radio frequency (RF) circuits such as power amplifiers (PAs) and low noise amplifiers (LNAs) need to be designed to cover each wireless standard at each frequency. However, there might be only one antenna switch required per wireless telephone unless a different type of antenna is used. Therefore, the antenna switch has to meet all the specifications from all the different wireless communication standards. Hence, the multi-throw antenna switch might be necessary.

Fig. 1.3 illustrates the functional building blocks of the wireless communication system. Most of the building blocks are designed using CMOS technology. The performance of the CMOS device at high frequency reaches the point where the integration of RF circuits such as voltage-controlled oscillators (VCOs), mixers and

LNAs is allowed with decent performance. PAs and antenna switches are the only remaining blocks to use high power devices such as GaAs.

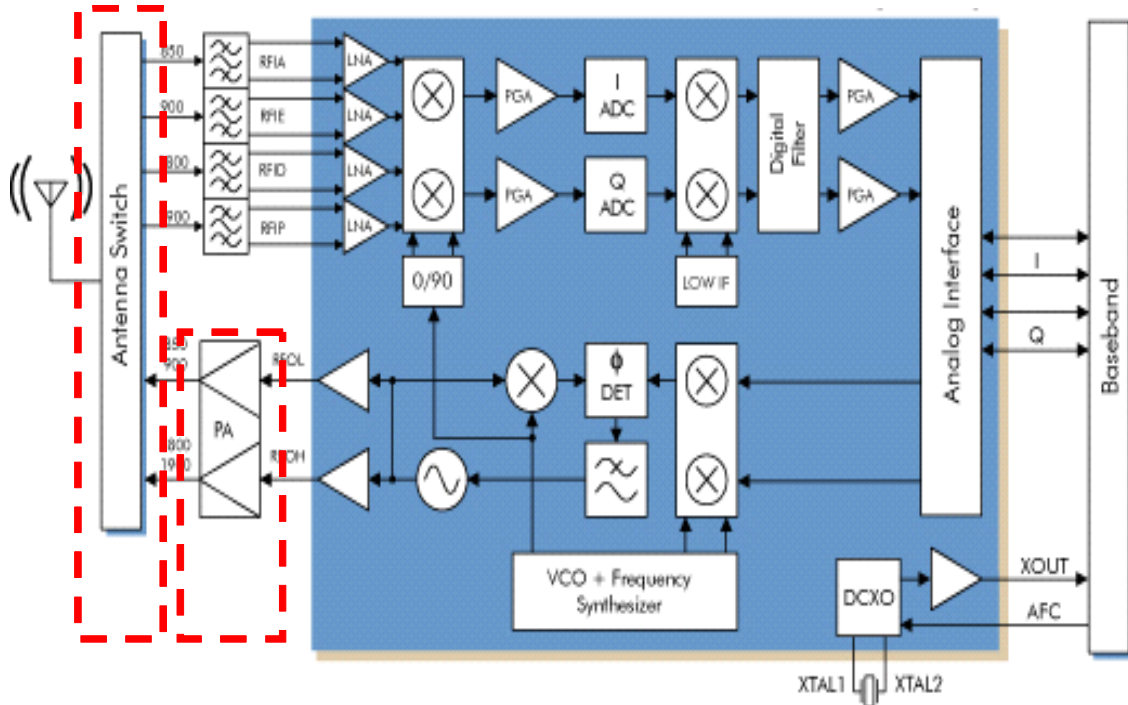


Fig. 1.3 Functional building blocks of the RF-transceiver architecture.

However, recent research shows the feasibility of designing PAs in a standard 0.18 μm CMOS process to meet the specifications for GSM and personal communication systems (PCS). If the antenna switch can be integrated in the CMOS technology, it can be possible to integrate all of the RF transceiver building blocks in one single die. This can provide benefits with respect to the performance of the IC, saving manufacturing costs, optimizing power and the reducing design complexity. If the integration of all the blocks in one chip is allowed, the number of the passive components can be significantly reduced. This can save manufacturing costs by minimizing the overall size of the product. Also, power loss due to the inter-connection between the building blocks designed in two different dies can decrease. When considering the reliability issues, the single chip

design can support a better solution. Eliminating impedance matching blocks is another benefit of integrating all the RF function blocks in one die.

However, the CMOS technology is basically introduced to produce digital circuits. This means that it is challenging to design RF circuits using CMOS technology to deal with high power signals.

There is one critical factor with the CMOS switch to limit the power handling capability, which is the existence of substrate junction diodes in the substrate body. As can be seen in Fig. 1.4, voltage swing at the load port is not a significant problem until negative voltage swing reaches threshold voltage of the junction diode, as shown in Fig. 1.4(b).

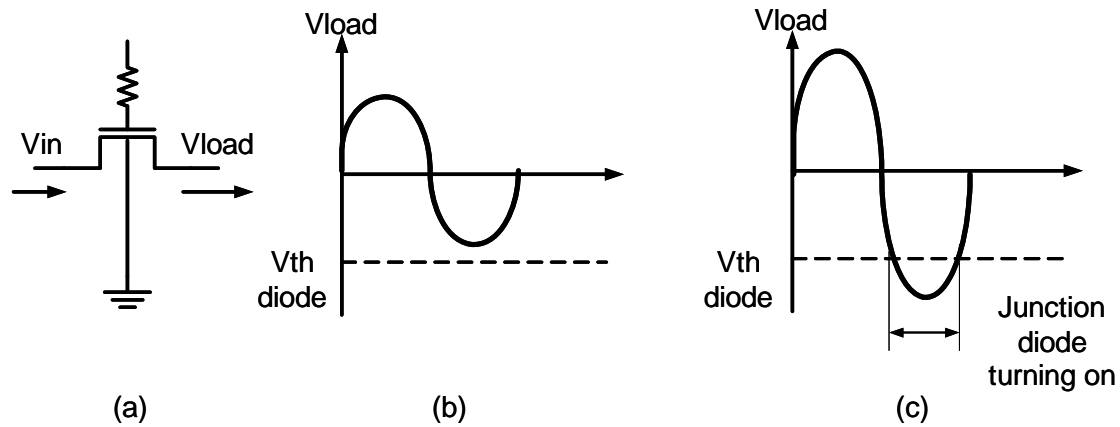


Fig. 1.4. Voltage swing behavior in a CMOS switch (a)., (b) Small signal input, and (c) Large signal input

Once the negative voltage swing reaches the threshold voltage of the switch, as shown in Fig. 1.4(c), the substrate junction diode turns on so that distortion of the input signal might occur. Besides this phenomenon, low breakdown voltage between source and drain as well as low gate-oxide breakdown voltage, which is decided by the type of device chosen also limit the power-handling capability of the CMOS switch.

This dissertation aims for designing high-power switches using CMOS technology by employing various techniques and introducing new design techniques to integrate multi-wireless applications in one antenna switch design. Chapter 2. presents various types of RF switches to implement high-power antenna switches and introduce a critical technique to design high-power switches using CMOS technology. This technique is employed in every switch in the subsequent chapters. Chapter 3 introduces initial designs of the high-power CMOS switch. In this chapter, the various techniques introduced in the Chapter 2 are applied to the CMOS switches. The feasibility of applying these techniques to the CMOS switch is tested. Chapter 4 introduces a novel technique to realize design of high-power switch using CMOS technology. This technique is called an adaptive voltage swing distribution method in the multi-stack field-effect transistors (FETs). Chapter 5 demonstrates the design of the high power low harmonic switches in multi-wireless standards using GaAs technology. Finally, the conclusion and future works are summarized in Chapter 6.

CHAPTER 2

RF SWITCHES

For many years, various types of switches with high power-handling capability have been researched and implemented[5]. The maximum power-handling capability of a switch depends on the maximum voltage swing that can be safely applied to the OFF-state switch at an antenna port as well as the maximum current flow limit in the ON-state switch[6]. The latter can easily be solved by increasing the size of the device in the ON-state path, which is, however, accompanied by degraded isolation performance. The former becomes the main issue in designing high-power switches. There have been three different kinds of methods to improve high power-handling capability: stacked FET transistors, impedance transformer[7], and LC resonators[8].

First, the simple theory of OFF-state power blocking capability is introduced in Fig. 2.1.

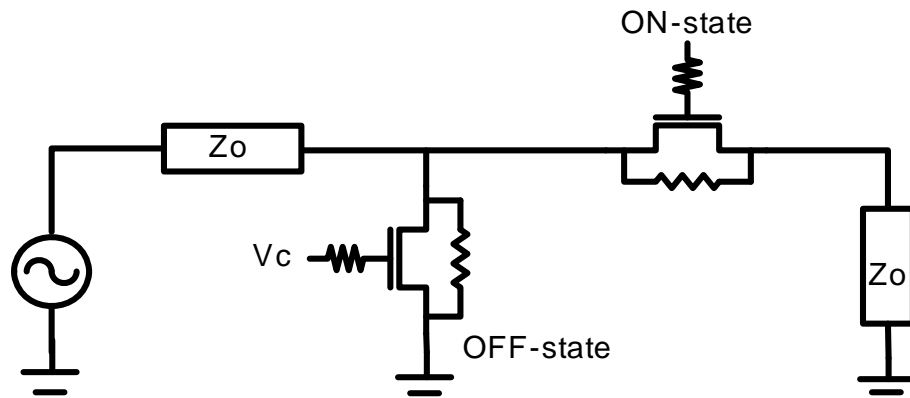


Fig. 2.1. Simplified series shunt switch

When an RF signal is applied across the shunt FET connected to the Z_o , a portion of RF voltage is shown in the drain and the gate of the OFF-state of the switch. The gate terminal is RF open because of high impedance resistor at the gate.

When the drain-gate and the source-gate impedance are equal, half of the voltage swing can be observed at the drain-gate terminal.

For a positive half cycle shown in Fig. 2.2, the total gate voltage should not fall below the pinch-off voltage V_p . If V_c is the dc control voltage,

$$-V_c + \frac{V_{\max}}{2} = -V_p. \quad (2)$$

Also

$$V_{\max} + V_c - \frac{V_{\max}}{2} = V_B, \quad (3)$$

where V_B is the gate-drain breakdown voltage.

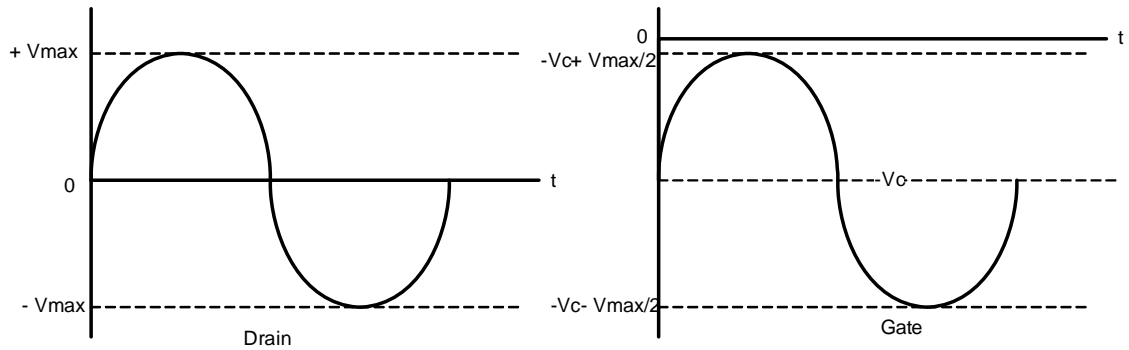


Fig. 2.2. Voltage swing at the drain and gate terminal at the OFF-state switch.

So, the maximum allowable drain voltage and gate bias control voltage can be expressed as

$$V_{\max} = V_B - V_p \quad (4)$$

$$V_C = \frac{V_B + V_P}{2} . \quad (5)$$

The maximum power that can be transmitted for the shunt OFF-state switch can be calculated:

$$P_{\max} = \frac{1}{2} \times \frac{V_{\max}^2}{Z_0} = \frac{1}{2} \times \frac{(V_B - V_P)^2}{Z_0} . \quad (6)$$

When the series FET switch is in the ON-state, there is no gate-drain voltage difference.

The maximum power deliverable through the ON-state switch is

$$P_{\max} = \frac{1}{2} I_{ds}^2 Z_0 . \quad (7)$$

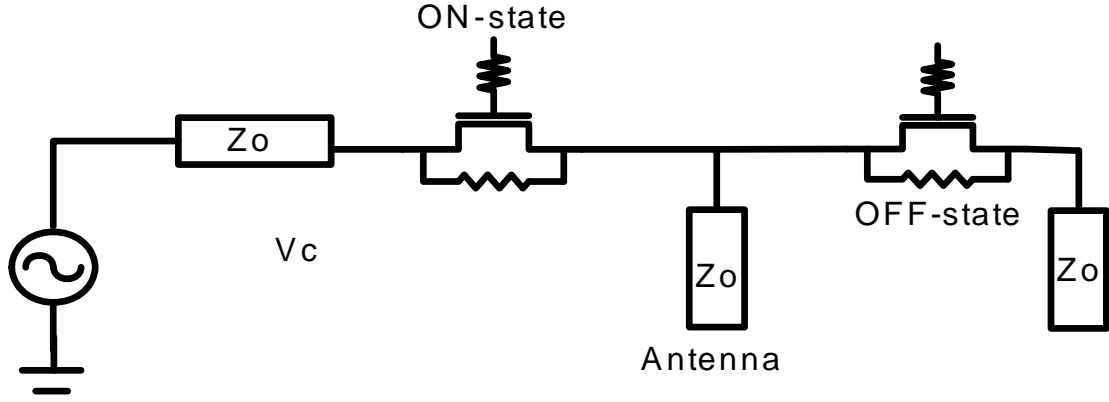
The drain-source current can be handled by the overall size of the device. Considering the breakdown voltages of the devices, the high power operation requirement, and the maximum power delivery, the size of the FETs are decided.

Another method for implementation of the high-power switch at the OFF-state switch needs to be applied according to the maximum transmit-power required. The other method can be either the impedance-transformation or the LC resonator structure.

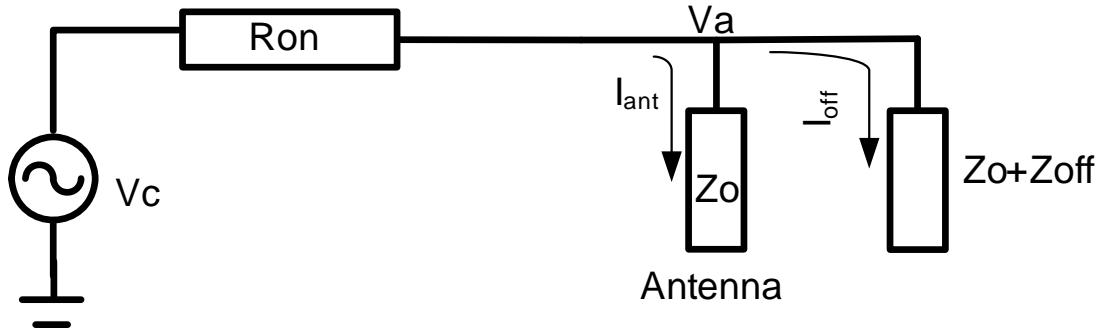
2.1. Impedance Transform Methods

Ideally, the OFF-state switch should not pass any leakage current so that all the power transmitted from the Tx switch can be delivered only toward the antenna. However, in reality, the OFF-state switch has finite impedance so that there might be leakage currents toward the OFF-state switch. Fig. 2.3. (a) SPDT switch diagram, (b) Impedance diagram of the simplified SPDT switch with Tx ON state.

As the size of the FET increases, the impedance of the OFF-state switch decreases. Eventually, the larger size FET can produce larger leakage current than the small size FET.



(a) SPDT switch



(b) Impedance of Tx mode SPDT

Fig. 2.3. (a) SPDT switch diagram, (b) Impedance diagram of the simplified SPDT switch with Tx ON state.

$$P_{loss} = \frac{1}{2} I_{total}^2 R_{on} + \frac{1}{2} I_{off}^2 (Z_o + Z_{off}) \quad . \quad (8)$$

$$P_{del} = \frac{1}{2} I_{ant}^2 Z_{ant} = \frac{1}{2} \frac{V_a^2}{Z_{ant}} \quad . \quad (9)$$

$$P_{total} = P_{del} + P_{loss} \quad . \quad (10)$$

As can be seen in Fig. 2.3, there are two main power loss sources in the circuit. One is transmit-path loss of ON-state and the other is leakage loss in the receive path of OFF-state. Simply, reducing the R_{on} value and increasing the Z_{off} value are one of design targets. However, these values are limited because of the isolation and insertion loss issues

An alternative way to improve power-delivery capability is to control the impedance of the antenna port. As described above, the level of the power delivered to the antenna is related to current I_{ant} , and Z_{ant} . This approach is accompanied by the necessity of an impedance matching network between switch and antenna.

2.2. Multi-Stacked FETs

The power handling capability of FET switches is improved by stacking FETs at OFF-state path and enlarging gate periphery as shown in Fig. 2.4.

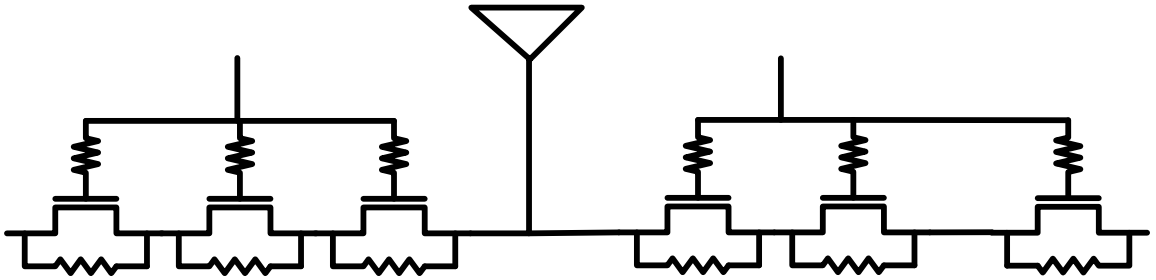


Fig. 2.4. SPDT switch structure using three stacked FETs

By stacking transistors at the OFF-state path, the RF voltage swing at the OFF-state path can be evenly divided within the stacked FETs, so that the power-handling capability increases approximately by the square of the number of FETs stacked in series.

$$P_{del} = \frac{[N(V_B - V_P)]^2}{2Z_0} \quad (11)$$

As the number of stacked transistors increases, the power-handling capability can be improved. However, the stacked FETs switch can create higher insertion loss than a single FET switch. Therefore, the size of the FETs has to be large enough to minimize the R_{on} to achieve the low insertion loss.

This configuration is very popular in commercial applications because of its advantages such as small size, wide bandwidth, and high power handling capability. The multi-gate FETs structure is originated from the multi-stack structure. By taking out the drain and the source contacts of the multi-stack FETs, overall size of the device can be dramatically reduced. Also removing unnecessary drain/source contacts, the insertion loss of the multi-gate device becomes lower than that of the multi-stack FETs.

Nevertheless, the multi-stack FETs and the multi-gate FETs cannot provide the high enough power required in the application by itself. Therefore, the voltage boosting method associated with DC/DC converters and the feed-forward method is necessary to apply this structure to the high power applications.

2.3. LC Resonator Switch

Even though the techniques described above have relevant high-power handling capabilities, there are some drawbacks such as large die area of the impedance matching technique and requirement of the high control voltage for the multi-stacked FETs. Actually, a high power operation in multi-band applications requires increasing the number of branches and level of supply voltages. These result in using external circuits

such as DC/DC converters, switch control logic circuits, and charge pump. A novel technique is proposed to resolve this additional complexity of the system, which is called an LC resonant switch. This structure does need neither the high breakdown-voltage device nor the high supply-voltage circuit.

There are many configurations introduced so far about the LC resonant circuit structure[9]. The basic operation theory is described in Fig. 2.5.

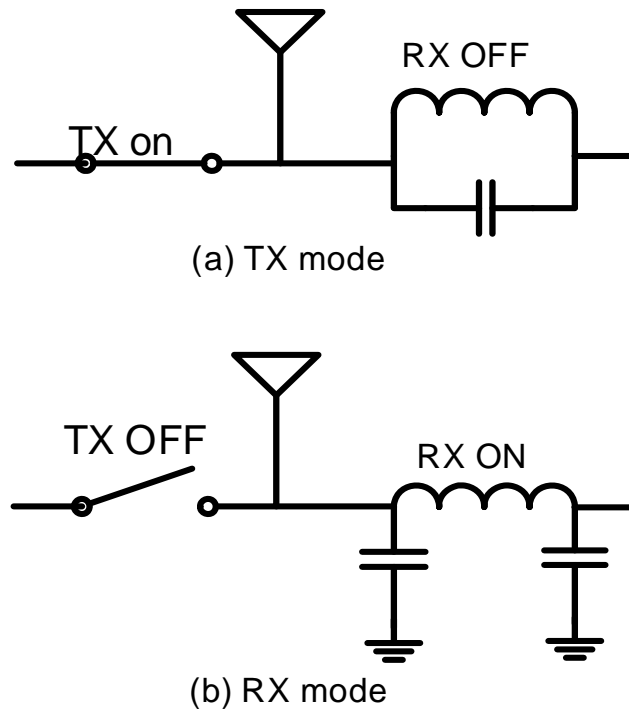


Fig. 2.5. Basic operation of LC resonant switch circuits in the receive switch

As can be seen in Fig. 2.5, the LC resonant circuit can operate in one of dual modes: either the LC parallel resonator at the Tx mode or the LC low-pass filter at the Rx mode.

An appropriate combination of switches and on-chip passive components such as inductors and capacitors can create many different configurations of LC resonant circuits. Basically, in the Tx mode, the combination of an inductor, capacitors, and switches generates an LC parallel resonator at the Rx path to block the high voltage swing at the

antenna port. In the Rx mode, the combination of LC and a couple of switches can form a low-pass filter or a impedance matching network at the Rx path to generate a signal path from the antenna to the receiver circuits in the Rx path.

Depending on the operation of either the Tx or Rx mode, the preferred inductor values vary. In the Tx mode, inductors are acting as an RF choke to block signals from the antenna to the receiver blocks. However, the inductor used as the RF choke acts as a signal path at the Rx path in case of the Rx mode, so the value of the inductor needs to be as small as possible to guarantee low insertion loss. So, a high Q inductor is required to meet different demands in both the Tx mode and the Rx mode. An on-chip inductor has limited Q values less than 20 for GaAs technology and 6-7 for 0.18 μm CMOS technology. This limited Q value is one of the drawbacks in this configuration. Also, the use of inductors on a chip results in increasing the overall size of the die area. So this configuration might not be suitable for the compact design.

The most critical problem of this configuration is narrow band operation. An RF high power signal can be blocked only at the LC resonant frequency. This phenomenon limits the bandwidth. This structure cannot be used in multi-band operation.

Also, in the case of the CMOS technology, this structure can only be applied to the limited frequencies between 2 GHz and 6GHz, where the Q of inductor shows peak values.

2.4. Substrate body tuning technique in CMOS high power switch

Compared to the GaAs process, CMOS technology has a critical disadvantage in terms of the power-handling capability because of the existence of junction diodes between the drain or source and the body substrate. As mentioned earlier, when the peak-

to-peak value of a small signal voltage swing is smaller than the threshold voltage of the junction diodes, the existence of the junction diodes doesn't affect the power-handling capability of the CMOS switch. However, once the level of the input voltage swing exceeds the threshold voltage of the substrate junction diodes, the input signal starts to be distorted, which can limit the power handling capability of the CMOS switch, as shown in Fig. 2.6. Without resolving this issue, the CMOS switch cannot be used for high power applications.

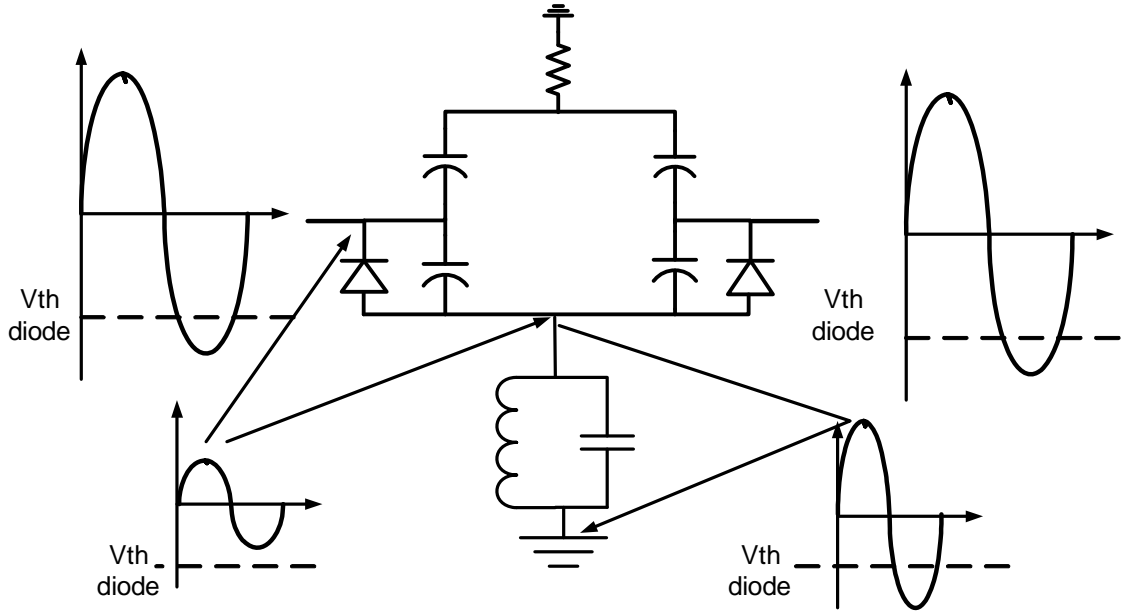


Fig. 2.6. Voltage swing at each node in the CMOS switch with body floating technique.

Fig. 2.7 shows configurations of the body floating technique implemented in the CMOS technology[10]. As can be seen in Fig. 2.7 (b), a LC resonator is connected at the substrate bulk port in the NMOS device. This LC parallel resonator provides very high impedance to the bulk port at the resonance frequency so that the portion of the impedance of the junction diode and the junction capacitor becomes relatively small in the overall impedance between the source port and ground. When the voltage swing of the large signal applied to the switch exceeds the turn-on voltage of the junction diode,

voltage level between the source or the drain and the bulk port is divided by the ratio of the impedance between the LC parallel resonator and the junction capacitors. Consequently, only a smaller portion of voltage swing is applied to the junction diode so that the junction diode does not turn on even at the large signal negative voltage swing.

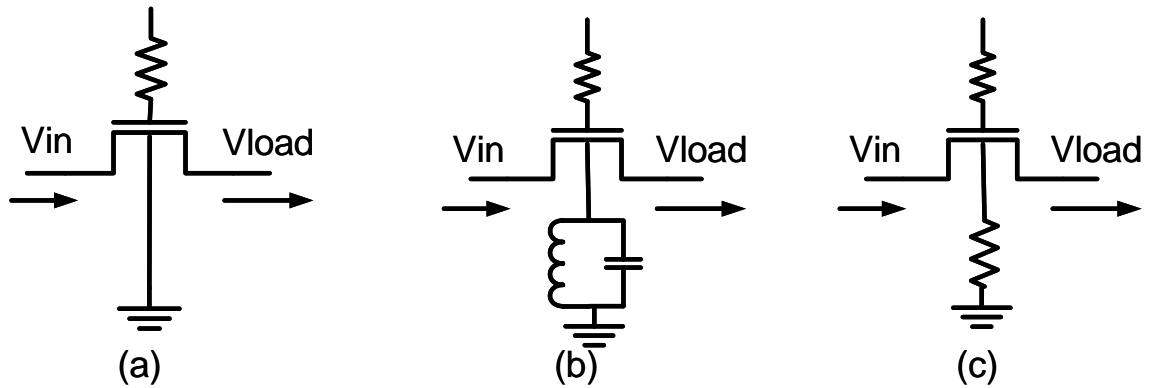


Fig. 2.7. (a) CMOS switch. (b) CMOS switch with body floating using LC resonant tank (c) CMOS switch using body floating technique using Deep N-well process.

However, this can be only effective at the certain frequency where LC component resonates. The main reason for using LC resonator as high impedance provider instead of a high value resistor is latch-up effect. However, this problem can be resolved if the body floating technique is implemented in the triple-well NMOS device. The triple-well NMOS devices can provide perfect isolation between the substrate body of one device and the other device so that this structure is immune to the latch-up effect. The configuration of the body floating technique implemented in the triple-well NMOS device is shown in the Fig. 2.7(c).

The body floating technique[11] becomes fundamental technique in the high-power CMOS switch implementation because this can prevent junction diodes from turning on in the large signal input. However, there are still remaining issues such as junction diode breakdown voltage and channel formation of the OFF-state devices.

CHAPTER 3

VARIOUS TECHNIQUES TO IMPLEMENT HIGH POWER CMOS SWITCHES

In the last two decades, many different kinds of techniques were developed to implement high power switches in GaAs processes and SOI CMOS process[12]. Those techniques include multi-stack FETs, multi gate FETs, LC resonator type switches and an impedance transformer. These techniques have their own pros and cons. For example, LC resonator type switch can provide very high power-handling capability while it requires very large die area. Also performance of the LC resonator type switch depends on the Q-factor of the inductor. The multi-stack FETs can have small size and a relative low insertion loss. However, the power-handling capability of the multi-gate FETs is not high enough for watt-level high power applications. A voltage-boosting method using a DC/DC converter should be associated with the multi-stack FETs to provide high power-handling capability. The main advantage of the multi-gate FETs is even smaller size than the multi-stack FETs. The relatively low power-handling capability of the multi-gate FETs becomes its main disadvantage.

In spite of all these matters, these structures described above are still commercially available and some of them are popularly used in association with supplementary methods to overcome its disadvantages.

In this chapter, CMOS switches employing the techniques used in GaAs process [13]to design a high power switch are introduced; for example, the LC resonator type

switch, multi-gate FETs and multi-stack FETs with body-switching techniques. All these switches are associated with the body- floating technique that is essential in designing a high power CMOS switch.

Measurement data of the CMOS switches are presented at the end of each section. The power handling capability of CMOS switches in this chapter still remains around one watt input power. Also there are issues to be resolved in each design. The issues are following; large die area, low Q factor, voltage swing at the substrate, leakage current control, and high insertion loss. All these matters are discussed in the conclusion of the each section[14].

3.1 A High Power CMOS SP4T Switch Using a Switched Resonator for Dual Band Applications

A novel dual-band CMOS single pole four throw (SP4T) switch with P1dB of higher than 29 dBm is designed to operate at 0.9 GHz and 1.8 GHz. In the receiver (Rx) switch path, a carefully designed switched resonator is incorporated to block high-power RF signals from the power amplifier at the transmit (Tx) path as well as to maintain a low insertion loss of the Rx switch simultaneously. In the Tx switch devices, a body-substrate tuning technique is applied to support high power delivery to the antenna port. Extended simulation results demonstrate more than 31 dBm of P1dB at both low and high bands as well as 0.9 dB and 1.4 dB of the insertion loss at 900 MHz and 1.9 GHz, respectively. This section also demonstrates the feasibilities of CMOS integration of RF front-end switch modules for modern wireless communication applications.

3.1.1 Switched Resonator At Receiver Switch

As well known, maximum transmit power is mainly limited by the voltage swing at a node of off-state switch because of the possible damage to the device from breakdown. Given this limitation, transmitter switch may have high power operation depending on the quality of endurance to breakdown of receiver switch at off-state. Besides, most of LC resonant receiver switches introduced so far have disadvantages such as capability of a single band operation only and trade-off relationship between insertion loss of the Rx switch and maximum transmit power of the Tx switch.

LC resonant circuits illustrating two different modes are shown in Fig. 3.1.

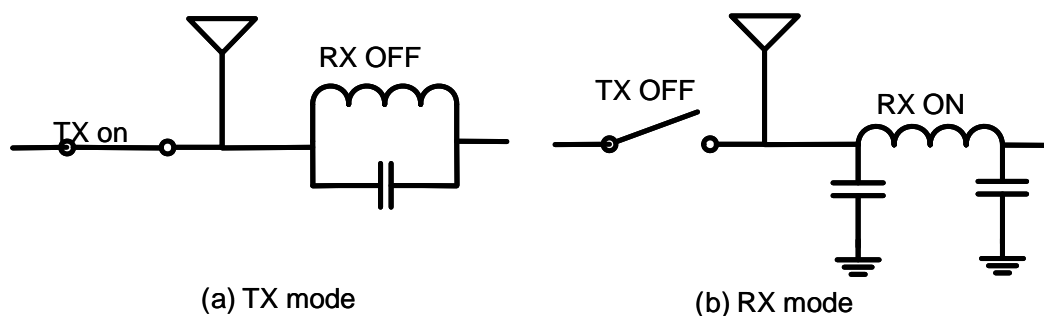


Fig. 3.1. Basic operation of LC resonator at receiver switch.

The preferred inductor value in a Tx mode operation is normally different from the one in a Rx mode operation. This is because maximum transmitting power can be obtained by using a large inductor value, which might be greater than 5nH depending on operating frequency, to prevent the signal power from flowing toward the receiver switch. On the contrary, the ON-state Rx switch needs the inductor value as small as possible at the operating frequency to reduce the attenuation as little as possible. Therefore, the structure of the switched resonator can be a solution to meet contradictory requirements of the Tx and Rx modes at the same time by providing variation of the inductor values.

Besides the capability of the dual mode operation by the switched inductor, it is possible for the switched resonator to provide capability of a multi-band operation.

In this section, the validity of using switched LC resonant circuit is verified by designing CMOS SP4T switch. The possibility of satisfying the contradictory demands regarding the value of the inductor of the Rx switch from the Tx mode and the Rx mode operation is demonstrated by the simulation results and the measurement data.

3.1.1.1 Dual mode operation of the switched resonator

Another beauty of the switched LC resonator is that the dual mode operation is made possible with the different functionality of the switched resonator in different modes. In the Tx mode operation, its primary functionality becomes an LC parallel resonator to block high power signals from the antenna port to the receiver switches to protect the Rx blocks. However, its main function is to deliver signals from the antenna to the Rx blocks with maintenance of insertion loss as small as possible by forming an LC lowpass filter in case of the Rx mode operation.

Fig. 3.2 shows the Tx mode operation of an SP4T switch using the LC resonator. In this mode, switches M3 and M4 are closed to form an LC parallel resonator to block the Tx signal. At the same time, M5, M6 and M7 are open to provide high impedance at point A. Also, M8 and M9 are closed to bypass leakage signals to ground to protect LNA resulting in high isolation. The power-handling capability of the transmit switch can be decided by the impedance of the LC parallel resonator and source to drain breakdown voltage of cascaded switches M5 and M6.

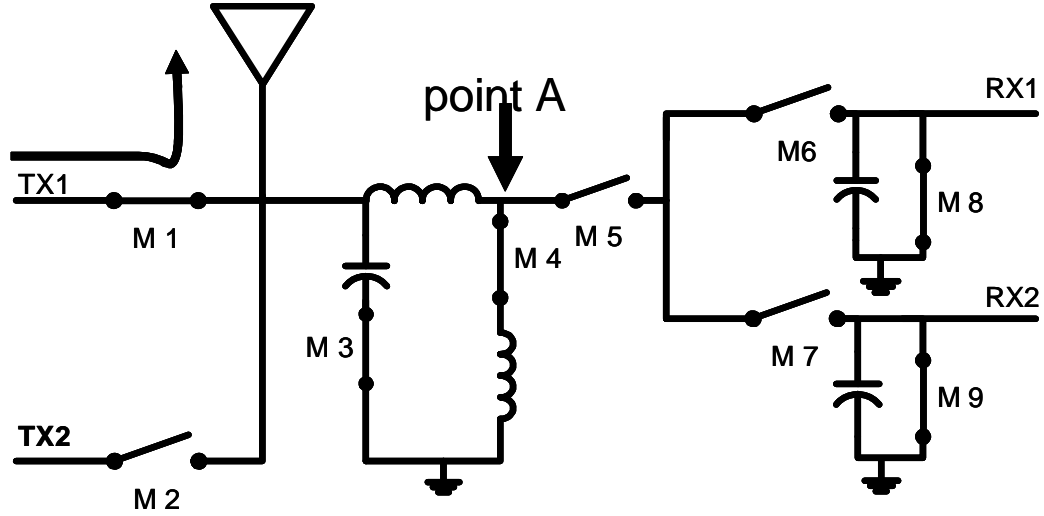


Fig. 3.2. SP4T switch using switched resonator at Tx mode.

Fig. 3.3 shows the Rx mode operation of the SP4T switch using the LC lowpass filter mode of switched resonator. In this mode, switch M4 and M3 are open so that only L1 is used to provide low inductor value. Also M5 and M6 (M7) are closed and M8 (M9) is open to provide LC lowpass filter response at Rx1 (Rx2) path. If low insertion loss is the only consideration of the design, the inductor L1 value has to be as small as possible to reduce insertion loss. However, ratio of inductor value of the L1 and L2 is related to power handling capability at the Tx mode. When M4 is closed, the voltage swing at M4 is decided by the L1 and L2 ratio. If L1 is too small, then larger voltage swing than source-to-drain breakdown voltage of M5 and M6 can be applied to M5, M6, and M7, resulting in device failure. So compromise has to be made by a careful selection of inductor value, L1 to get optimum voltage swing for Tx mode and low insertion loss for Rx mode, this is one of the design considerations of switched resonator. Fig. 3.4 shows performance comparison depending on the L1/L2 ratio. As can be seen, P1dB increases as L1 value increases. However, insertion loss at Rx path becomes higher at that point.

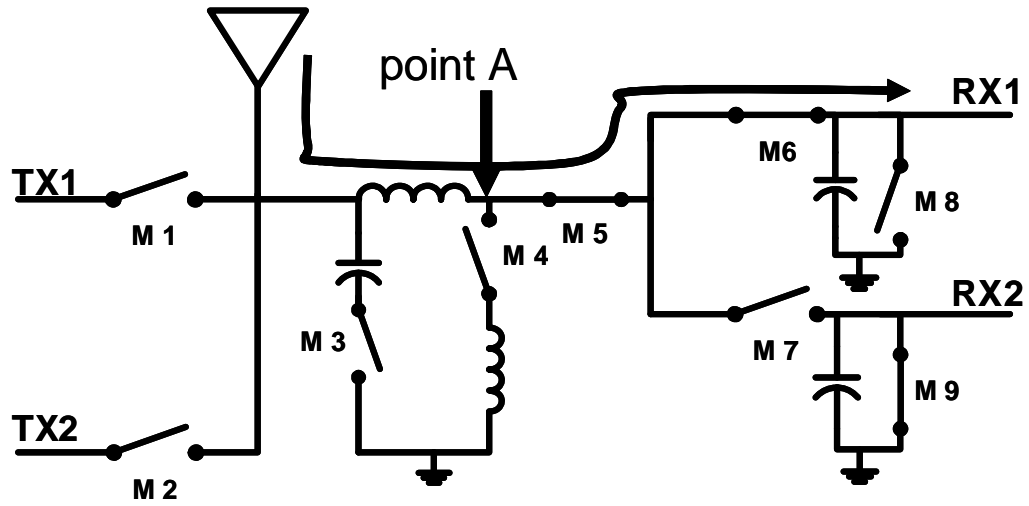


Fig. 3.3. SP4T switch using switched resonator at Rx mode.

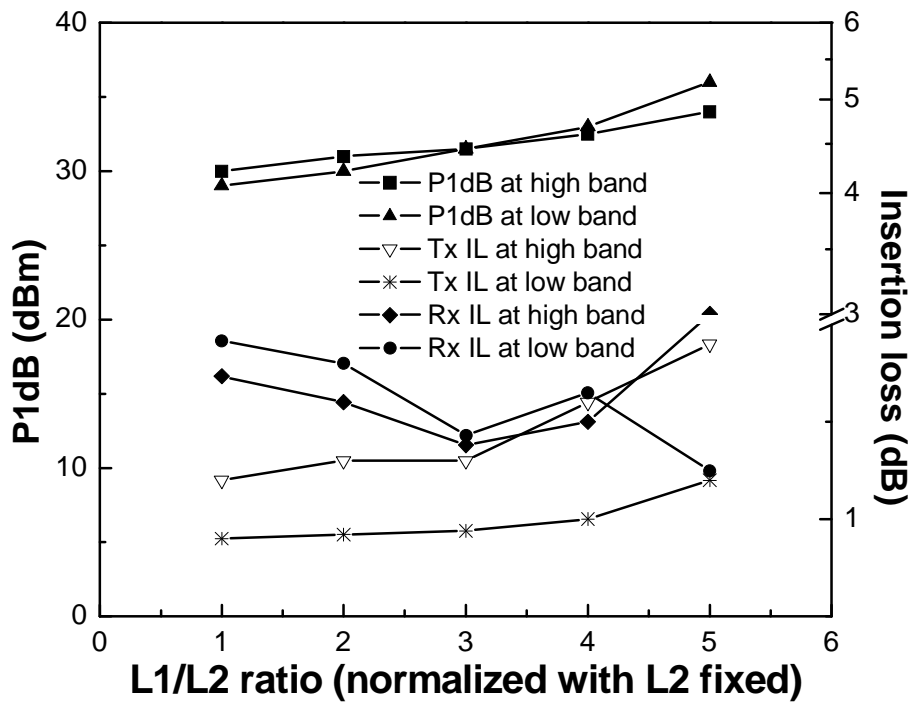


Fig. 3.4. Performance comparison by L1/L2 ratio

The insertion loss of the Rx switch can get lower if the small value of L1 is chosen. However, this can also cause the lower the 1 dB compression point of the Tx switch.

Furthermore, L_1 plus L_2 value need to be fixed at the operating frequency. Therefore there is an optimum ratio of L_1 and L_2 , which is 3.5 nH and 8.5 nH when the target frequencies are 900 MHz and 1.8 GHz.

3.1.1.2. Dual band operation of the switched resonator

An SP4T switch is designed for a multi band operation. Basically, the receiver switch has to secure dedicated signal paths from antenna to LNA for different frequencies. However, as the number of signal paths at the antenna increases, the power handling capability of the transmit switch can drop accordingly. Key design issue at a single pole multi throw switch is to decrease the number of signal branch attached to the antenna. As can be seen in Fig. 3.3, receiver switches of Rx1 and Rx2 shares one LC parallel resonator at the antenna port. This LC parallel resonator should block transmitter signal from Tx1 and Tx2 at dual band frequencies. Instead of designing switched resonator which has two switched transmission zeros at dual-bands, the switched LC resonator proposed has one transmission zero at 1.5 GHz with wide bandwidth characteristic. Simulation results shows 13 dB, 25 dB and 14 dB return loss at 900 MHz, 1.5 GHz that is located between two bands and 1.9 GHz, respectively.

Fig. 3.5 (a) shows Tx switch structure representing M1 in Tx1 path and M2 in Tx2 path in Fig. 3.2. When M1 in Tx1 path is closed to transmit signals, M2 in Tx2 path has to be open so that off-state M2 at Tx2 path has to have high power blocking capability. When blocking high power signal, high stress of voltage between two switch ends can be built up, which may result in breakdown of the devices.

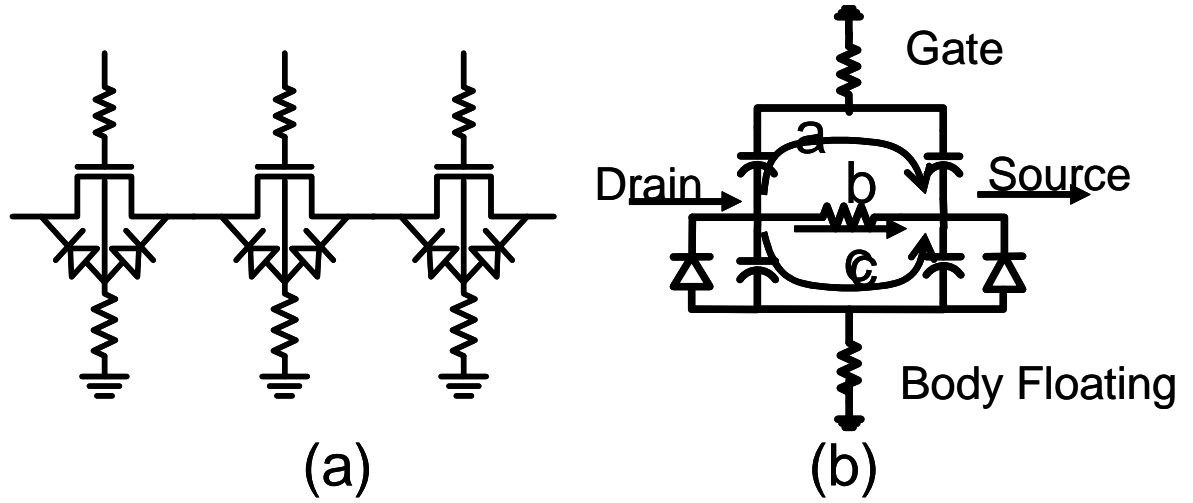


Fig. 3.5. (a) multi stacked switch at TX path (b) Simplified equivalent model of switch with signal flow.

By stacking the transistors used in the switch device, source-to-drain breakdown voltage can be increased by sharing the stress voltage among multiple transistors in stacked structure. However, increasing the number of transistors may result in higher insertion loss in the Tx switch, which necessitates another optimization of design parameters.

Also, a body floating technique to ensure negative voltage swing is employed to reduce the insertion loss of signal power. This technique is feasible by employing deep N-well process that is very common in present processing techniques, by use of a deep N-well, the device becomes immune to latch up in spite of connecting high value resistor between the body of the device and substrate.

Fig. 3.5 (b) shows signal flow of on-stage single switch device. Simulation result with this floating body device shows that body floating resistor can improve insertion loss by blocking leakage current to substrate ground. Without this body floating technique, as the size of a transistor increases, parasitic capacitance value becomes high

Therefore the source-to-body and drain-to-body parasitic capacitors start to establish the path of signal power insertion loss, since the body is grounded, signal path C in Fig. 3.5(b) is bypassed to the ground, which results in degraded insertion loss. However, with body floating technique, the path of signal power loss is broken to minimize the insertion power loss.

3.1.2 Simulation Results

Fig. 3.6 and Fig. 3.7 show simulation results of the SP4T switch using the switched LC resonator.

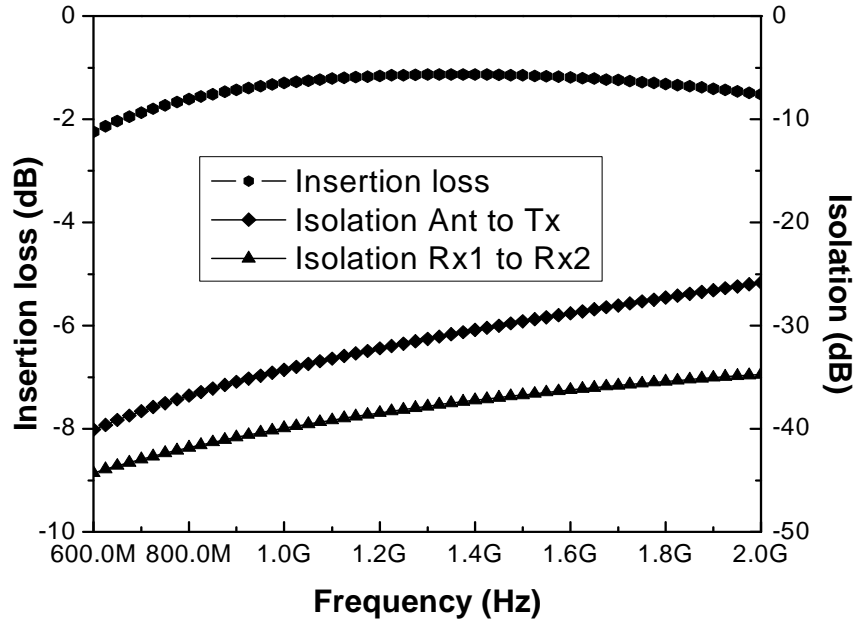


Fig. 3.6. Receiver switch simulation results.

Simulation results meet the demand of the high power handling capability at both bands. The switched resonator and stacked transistors at receiver path provide high isolation at Tx mode from antenna to Rx. So receiver circuits like LNA can be protected from the Tx

high power signal. Also When the Rx1 mode is in operation, isolation between Rx1 and Rx2 is high enough to prevent signals from one path from leaking to the other path. Fig. 3.8 show the layout of the SP4T switch using switched LC resonator.

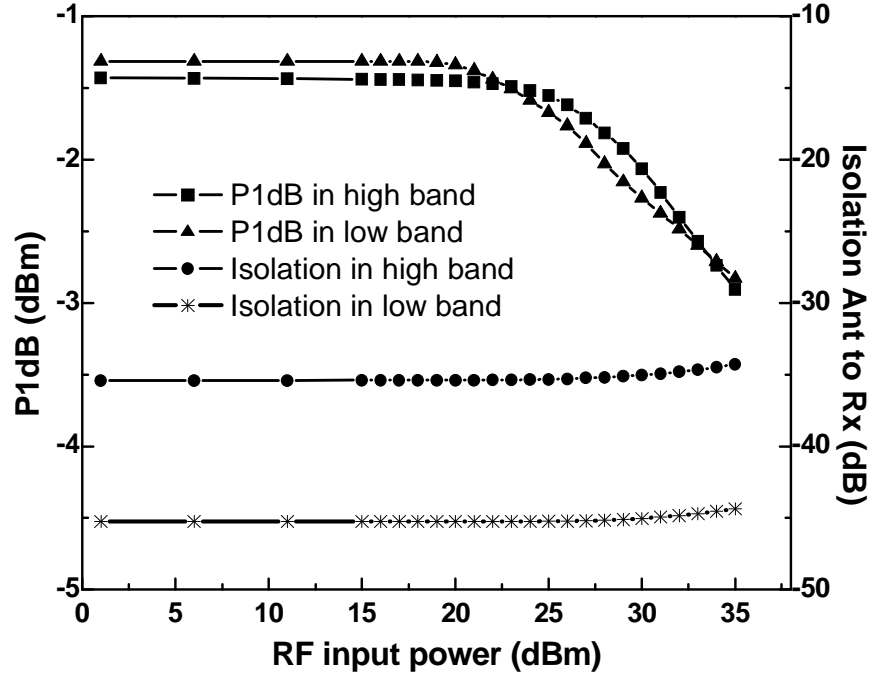


Fig. 3.7. Transmit switch simulation results: Power handling capability and Isolation from Ant to Rx.

3.1.3. Measurement Data and Design Issue

Fig. 3.9 shows the measured power-handling capability of the proposed structure at 1.9 GHz. The 1 dB compression point was obtained at 29 dBm input power.

When we implement this type of switch in a standard 0.18 μm CMOS process, the Q-factor of the inductor might play a very important role to determine the insertion loss of the Rx switch and the power-handling capability of the Tx switch. Since the 0.18 μm standard CMOS process employs Alumina as a metal process, Q-factor at this process might be lower than that of the 0.13 μm CMOS process, where Cu is used as a metal

process. However, the breakdown voltage of the device at 0.13 μm process is lower than that of the 0.18 μm process so that the 0.13 μm process can not be a good candidate for high power switch design just because of the high Q value. Another possibility to implement this structure at the CMOS technology is to employ the high Q process for the inductor value and then combine the CMOS switch with the high Q process. The detailed design method is discussed in the future work.

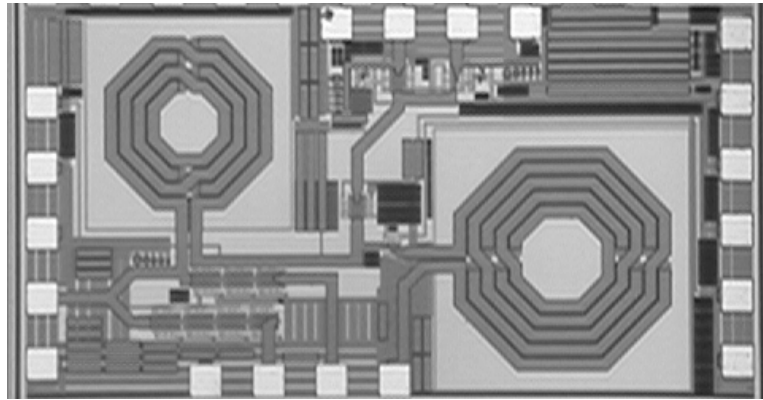


Fig. 3.8. Layout of SP4T CMOS switch using switched resonator with 1.7 mm by 0.9 mm dimension.

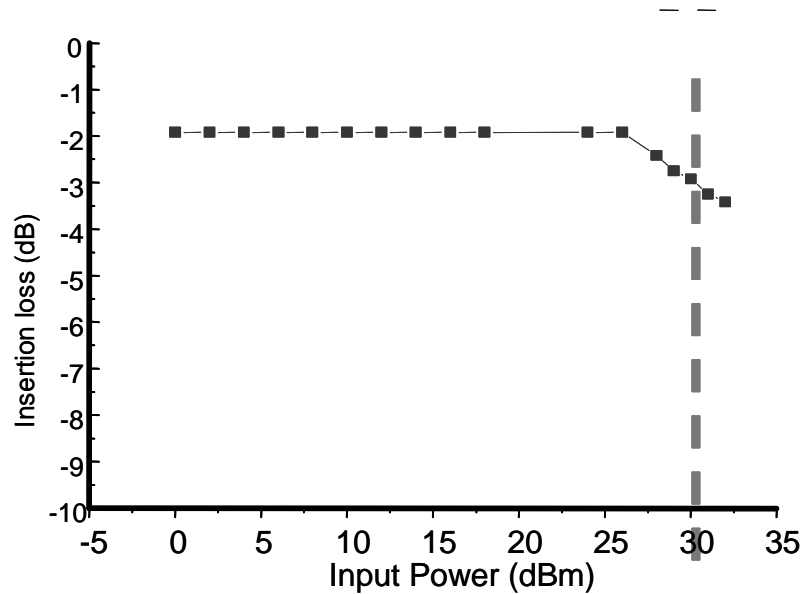


Fig. 3.9. 1 dB compression point of the CMOS switch at 1.9 GHz.

3.2. A High Power CMOS Switch Using Multi Gate Structure

A novel CMOS high power RF switch using the multi-gate structure is designed, implemented, and characterized in a standard 0.18-um triple-well CMOS process. The receive switch incorporates the multi-gate structure to provide high power- handling capability of the transmit switch. In addition, the RF switch with the multi-gate structure reduces insertion loss more than the one with the stacked FETs by reducing parasitic capacitance of the devices. Both a triple-gate NMOS switch and a dual-gate NMOS switch were fabricated and their performance are compared. Experimental data show that the SPDT switch exhibits 26 dBm of P1dB with the triple gate structure, and 24 dBm of P1dB with the dual gate structure at 900 MHz and 1.9 GHz. The multi-gate switch demonstrates 0.2 dB lower insertion loss than the multi-stacked switch. The size of the fabricated switch die is also minimized by employing the compact multi-gate layout structure. Compared to the multi-stacked structure using an RF NMOS device in a standard CMOS process, the die size of the triple gate and the dual gate is reduced up to 50 % in both cases[15].

3.2.1. Multi-Gate Device in RF and Digital Circuits

Multi-gate devices have been introduced in many RF circuits using GaAs MESFET and p-HEMT technology [9, 16, 17] as well as in digital circuits using CMOS technology[18, 19]. Fig. 3.10 shows the basic schematic and layout of multi gate FETs and stacked FETs.

In digital circuits, layout of the multi-gate FETs can have smaller perimeter by sharing active area (N+) than that of multi-stacked FETs. In turn, this reduces contribution of

junction capacitance as the one of the sources of leakage currents to the substrate. Therefore, faster switching speed of the device can be obtained [19]. In RF circuits, GaAs devices such as MESFET and p-HEMT have employed multi-gate structures mainly for high power switch devices. In the case of CMOS circuits, mixers and LNAs uses multi-gate structures to achieve low noise and high linearity performance [20].

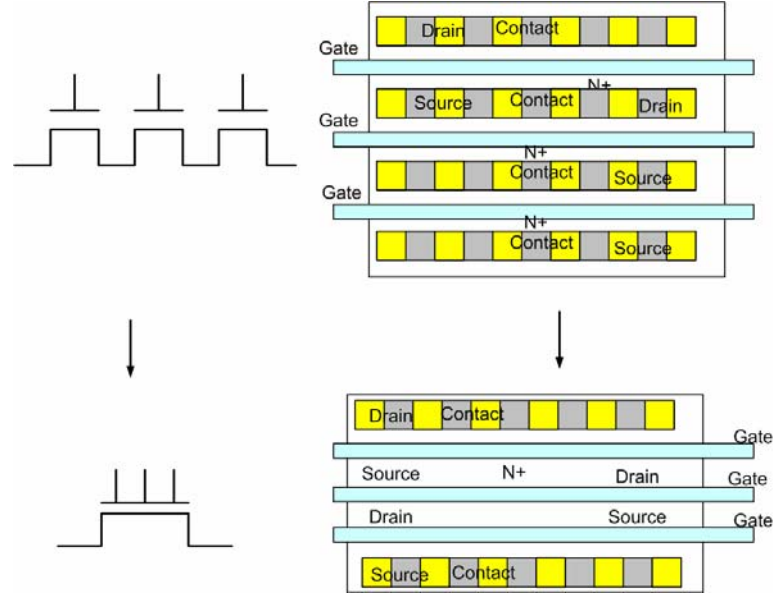


Fig. 3.10. Basic schematic and layout of multi-gate structure

3.2.2. RF CMOS Switch Device – Four port device

Basically the devices used in commercial applications with multi gate FETs such as GaAs switches, CMOS digital circuits, and RF CMOS mixers can be expressed as three port devices[21-23]. However the CMOS device for high power RF switches is a 4-port device which has separate bulk connections. One of the characteristics of the CMOS devices to limit power-handling capability is a low breakdown voltage. Source/Drain-to-gate breakdown, source-to-drain breakdown, and source/drain-to-substrate junction breakdown are main factors to limit the power handling capability in CMOS devices. Among those, the existence of source/drain-to-substrate junction diode does not allow

negative voltage swing, because junction diodes turn on once the negative voltage swing becomes larger than the turn on voltage of the substrate junction diodes. The body floating technique [11] is introduced to resolve this problem.

The presence of parasitic junction capacitors and junction diodes causes that the equivalent circuit model of multi-gate devices of the CMOS technology becomes differently from that of GaAs devices and digital CMOS circuits. Fig. 3.11 shows equivalent lumped element circuit model of three stacked CMOS FETs used in high power switch applications [24]. Fig. 3.12 shows the equivalent lumped element model of a triple gate CMOS device.

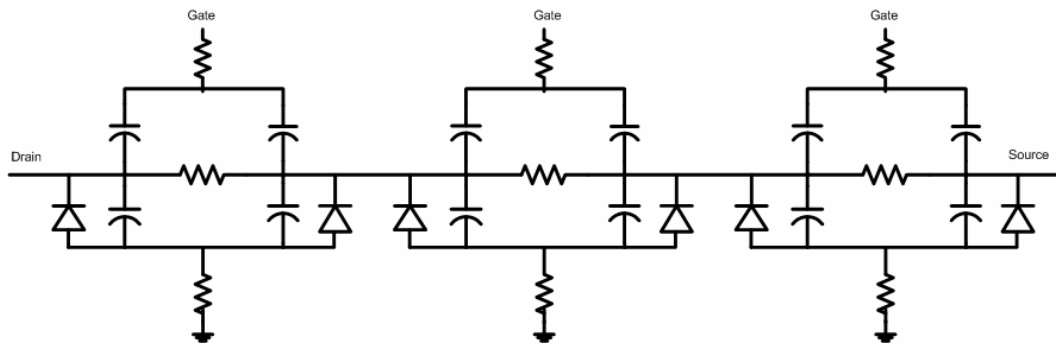


Fig. 3.11. Equivalent model of three stacked FETs with body floating technique.

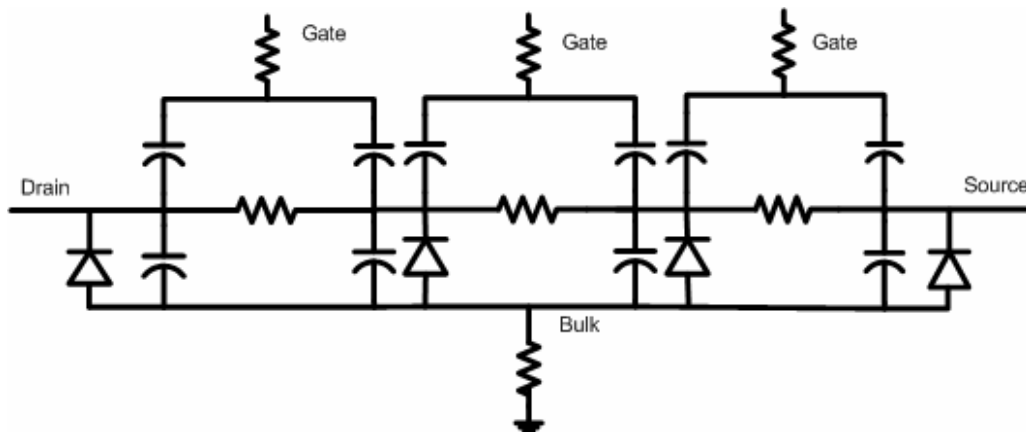


Fig. 3.12. Equivalent model of triple gate transistor

As can be seen in Fig. 3.12 a multi-gate structure can have a smaller junction capacitance than a stacked structure by sharing drain and source connections. Fig. 3.13. and Fig. 3.14. show cross-sectional view of the triple gate transistor and the dual gate transistor of the NMOS device in deep N-well process, respectively.

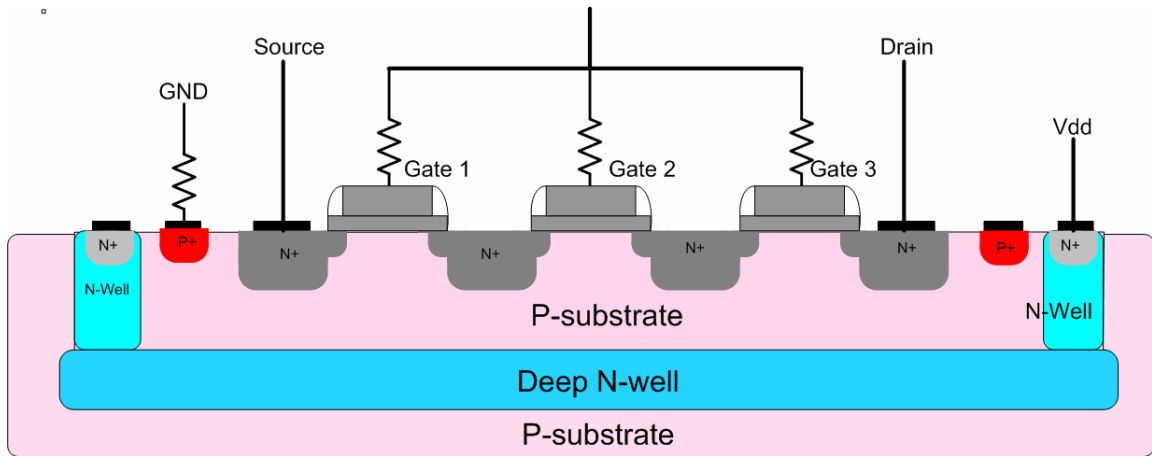


Fig. 3.13. Cross-sectional view of the triple gate transistor.

Both of the triple gate device and the dual gate device are implemented in p-substrate surrounded by deep N-well and N-well structures. When employing the body floating technique, isolation of substrate has to be secure. Otherwise, latch-up might happen so that the leakage current to the substrate increases. Therefore, a lower 1dB compression point of transmit power can be caused. One of advantages of the multi-gate structure is smaller junction capacitance which can provide lower insertion loss. As the size of the device increases in RF CMOS switch applications to achieve high power delivery and low insertion loss, the parasitic capacitance in the junction can not be negligible in both ON-state and OFF-state. Smaller junction capacitance of the multi-gate structure can improve insertion loss by minimizing leakage current to the substrate body.

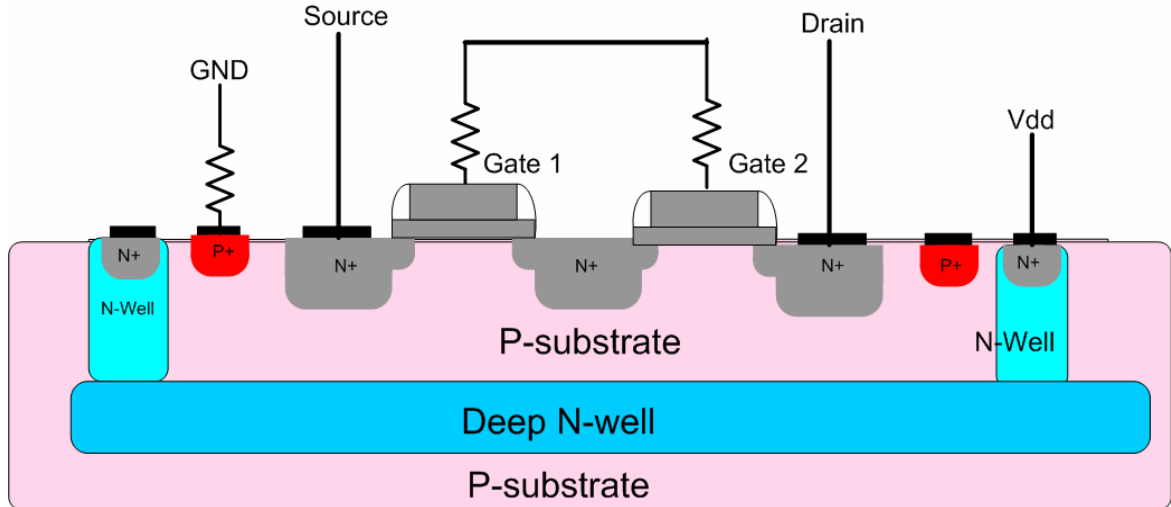


Fig. 3.14. Cross-sectional view of the dual gate transistor.

Considering designing CMOS switches using a standard 0.18 μm RF CMOS process, p-substrate guard rings and N-well guard rings of the NMOS device increase the overall size of the device. Integrating multi-stack transistors in a single body substrate enables a dramatic size reduction of the multi-gate structure. Compared to the size reduction of GaAs p-HEMT multi-gate, where a multi-gate switch can achieve 67% reduction from a stacked FETs switches, the size of RF CMOS multi-gate device can be reduced up to 50 % from the stacked CMOS FET device in both dual gate devices and triple gate devices.

3.2.3. High Power SPDT switch Design

In switch operations, high power-handling capability is decided mainly by both voltage swing limitation of the OFF device and maximum current limitation of the ON-state device. A high power SPDT switch needs to have a large gate width for large current flow of the Tx switch in ON-state and a large gate length for the allowance of high voltage swing at the Rx switch in OFF-state. There have been many methods

introduced in designing Rx switches for high power switches; for example, LC resonator switches [24], multi stack switches, and impedance transformation methods [25]. Multi gate switch design is one of the approaches in those techniques. By cascading transistor at the Rx switch, large voltage swing at the antenna port can be divided to each device. Cascaded switches can reduce the burden of low breakdown voltage of CMOS devices between source/drain-to-gate and source-to-drain. Fig. 3.15 shows the schematic of an SPDT switch using the triple gate structure at the Rx switch. In order to maximize power performance, a shunt arm at the Tx switch was not incorporated.

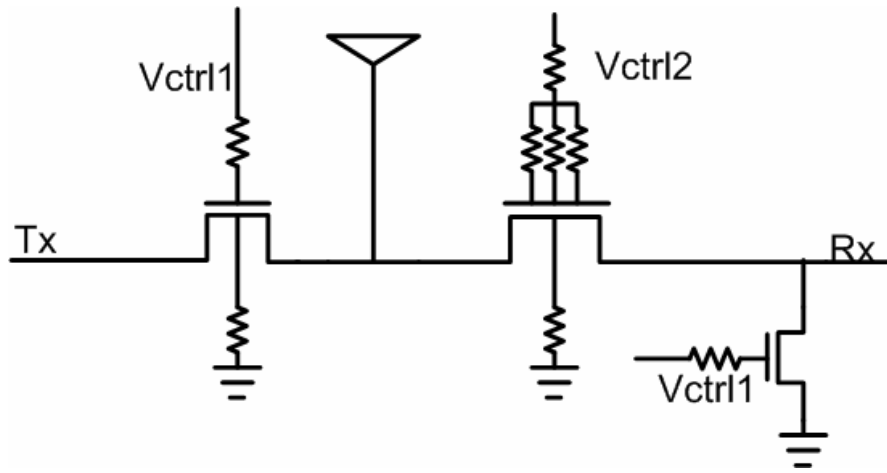


Fig. 3.15. Schematic of SPDT switch using the triple gate structure at the Rx switch.

The size of the Tx switch was chosen using DC characteristics to handle large current. The Rx switch utilizes the triple gate transistor to maximize voltage swing at the antenna port. As the number of gates in the transistor increases, the power handling capability of the Rx switch also increases. However, an increased number of gates of the Rx switch can cause higher insertion loss. Insertion loss can be improved by reducing gate length, increasing gate width, or increasing the control voltage supplied to the gate. However, increasing gate width causes the lowering of OFF state impedance. This, in turn, causes

to lower the P1dB compression point because of increased leakage currents toward the OFF-state device. Also the isolation performance of the device in OFF-state can be degraded. The multi gate structure has a smaller junction parasitic capacitance than the multi stack structure. Therefore the effect of leakage current on P1dB compression point can be alleviated in the multi-gate structure. The gate length with thick gate-oxide provided by the commercial 0.18-um CMOS process was chosen to maximize gate-to-drain/source breakdown voltage.

3.2.4. RF Switch Measurement

Fig. 3.16 and Fig. 3.17 represent the performance of an SPDT switch using a triple gate transistor in the case of the Tx mode operation and the Rx mode operation, respectively.

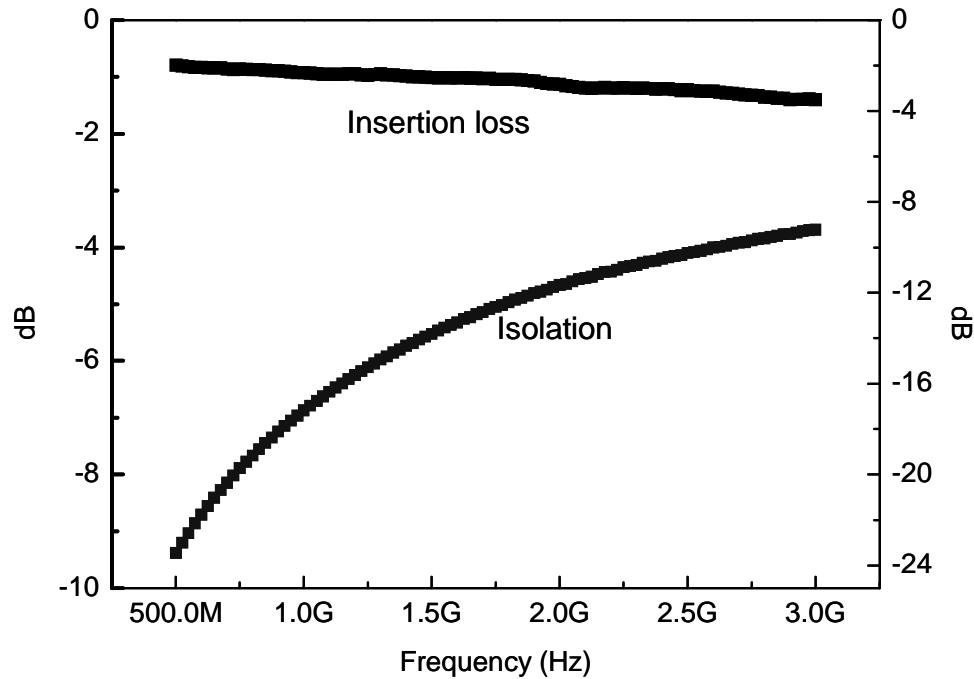


Fig. 3.16. Tx insertion loss and isolation of SPDT switch using the triple gate structure in the Rx switch.

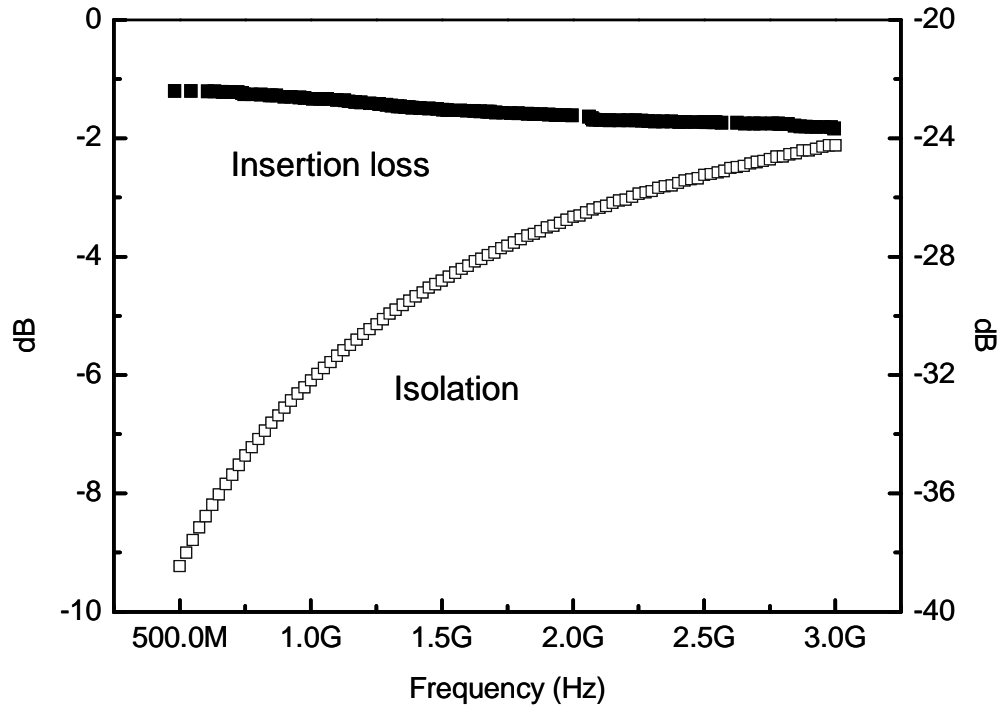


Fig. 3.17. Insertion loss and isolation of the SPDT switch using the triple gate structure in case of a Rx mode operation.

A standard RF CMOS process does provide neither the device model nor the circuit model of the multi gate structure. Simulation of the SPDT switch using the multi gate structure was performed by cascading transistors with all the bulk ports connected to single resistor to implement the body floating technique. Therefore, all the devices in the multi gate configuration can share one substrate. Measurement data show that insertion loss of the Tx switch is less than -1 dB up to 2 GHz, and insertion loss of the Rx switch, where the triple gate structure was implemented, is less than -2 dB up to 2GHz. The insertion loss at the Rx switch is mainly dominated by leakage currents toward the OFF-state device of the Tx switch. A single transistor with large perimeter at the Tx switch does not have high enough isolation because of parasitic capacitance. Lower isolation performance of the Tx switch means larger leakage current. That is one of the reasons

why the Rx switch can have higher insertion loss than the Tx switch. Fig. 3.18 shows the P1dB compression point of the SPDT switch using triple gate and dual gate test structure.

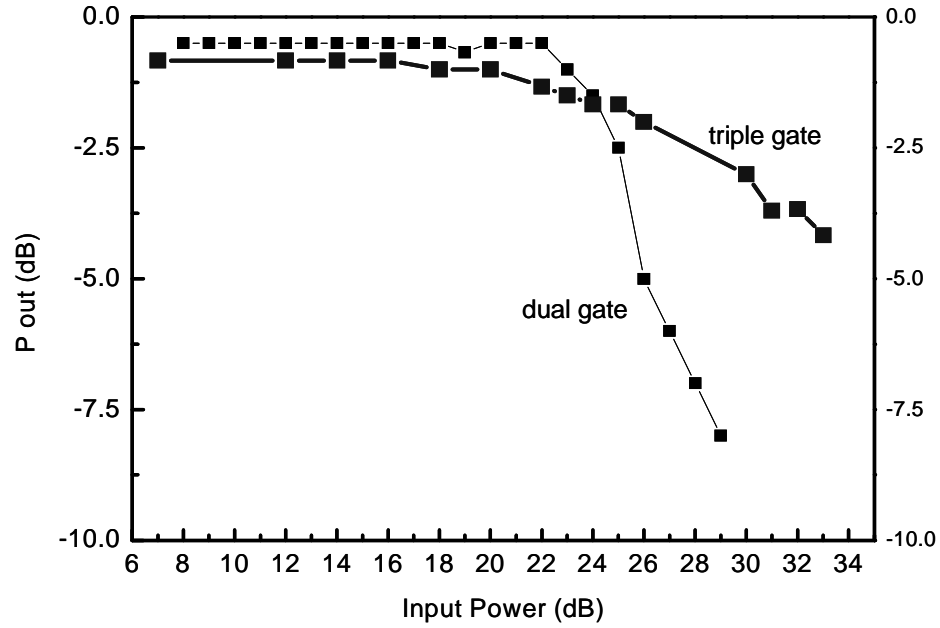


Fig. 3.18. 1dB compression point of the triple gate FET and the dual gate FET at 1.9 GHz.

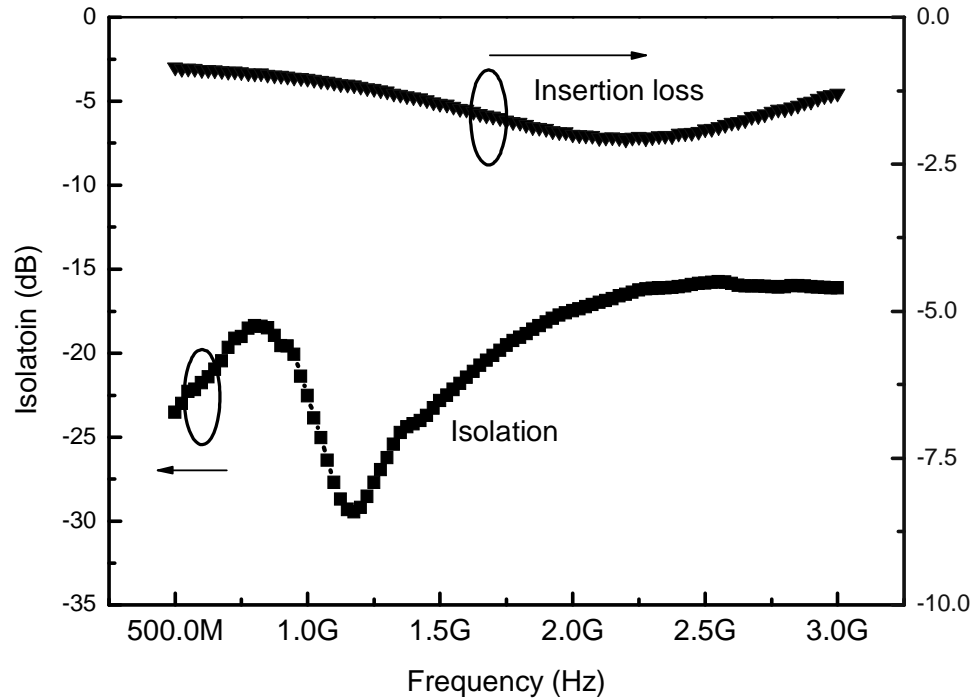


Fig. 3.19. S-parameter performance of the test structure of the dual gate.

As can be seen, the compression point of the triple gate is observed around 27 dBm at 1.9 GHz.

A dual gate test structure was implemented to compare the performance of that structure with that of the triple gate structure. The dual gate device has power-handling capability of 24 dBm of P1 dB with 1.5 dB loss up to 2 GHz. Fig. 3.19 shows the S-parameter performance of the dual gate test structure. Fig. 3.20 shows photograph of the SPDT switch using the triple gate structure at the Rx switch and the test structure using the dual gate structure.

3.2.5. Summary

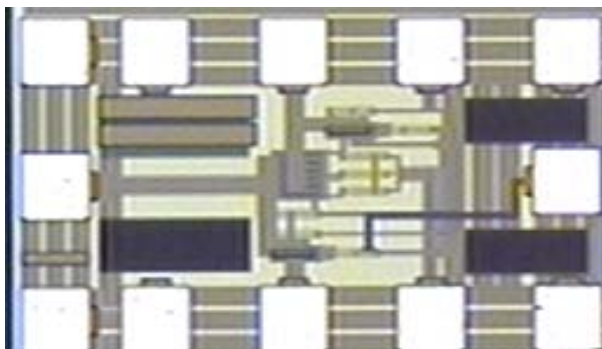
An SPDT switch using the triple gate structure and a test structure of the dual gate are designed and implemented. Experimental data demonstrate that P1dB of 27 dBm and 24 dBm at 1.9 GHz were achieved from the triple gate structure and the dual gate structure, respectively. S-parameter measurements show that the dual gate and the triple gate have less than 1.5 dB and 2 dB insertion loss up to 2 GHz. The size of the SPDT switch using the triple gate was dramatically reduced. Compared to the case of using an RF CMOS device for cascaded transistors, overall die area of the triple gate structure and dual gate structure can be saved up to 50 %.

Even though the multi gate structure FETs provide advantages of the reduced size and lower insertion loss over the multi stacked FETs, the former has the critical disadvantage of the lower 1 dB compression than the latter.

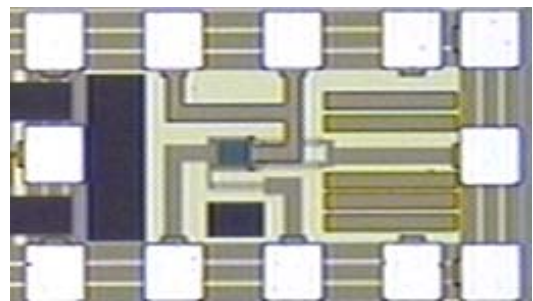
The power-handling capability of the CMOS switch can not be explained without consideration of the voltage swing at the bulk port. A conventional multi-gate structure

and multi stack structure of the GaAs switch only need to consider voltage swing at source/drain and gate to design high power switch. However, the CMOS switch using body floating technique has one more factor to limit power-handling capability that is the voltage swing between source/drain port and bulk port. In case of the multi-stack FETs, all the switch devices have its own body-floating resistor at the bulk port. This can ensure another voltage-swing dividing mechanism between the drain/source port and the bulk port of the switch device in OFF state. However, the multi-gate switches in the CMOS technology share one body floating resistor. Therefore, the voltage swing at an input port of a multi-gate switch device in OFF state cannot be divided in a same fashion as that of the multi-stack switch devices. The mechanism of the voltage swing dividing at the multi-gate switch is not so much effective as that of the multi-stack switches.

To the conclusion, the multi-gate structure switch can be a good candidate for applications with medium-power level, where the power level needs to be smaller than 0.5 W. Nevertheless, small size and lower insertion loss are main advantages of the multi-gate switch devices.



(a) SPDT switch using triple gate structure



(b) Dual gate test structure

Fig. 3.20. Photograph of multi-gate structure (a) SPDT switch using a triple gate (b) dual gate test structure.

3.3. A High Power CMOS Switch Using Substrate Body-Switching in Multi-Stack Structure

In this section, the substrate body-switching technique is introduced as a novel method for improving the 1dB compression point in a CMOS high-power switch using a standard CMOS 0.18 μm process. The substrate body-switching technique employs a switch (M4) at the bulk port of one of the cascaded NMOS switch devices (M3), as shown in Fig. 3.21 (a). All the switches in the Fig. 3.21 are implemented in the deep N-well.

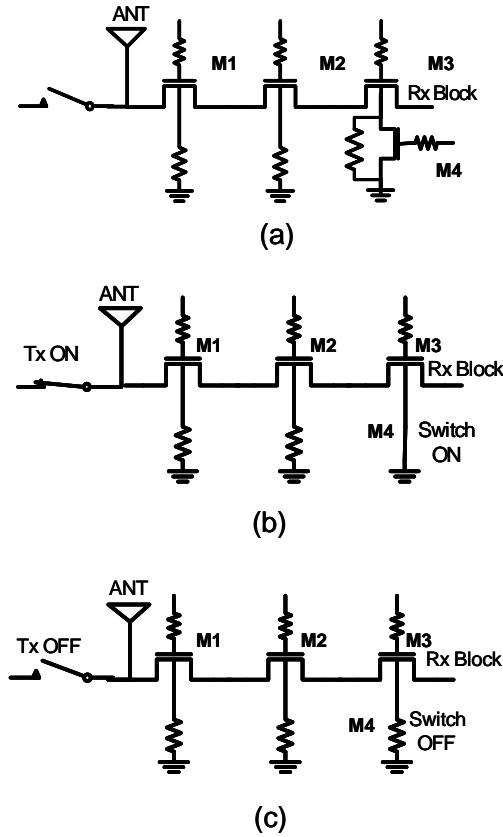


Fig. 3.21. Basic concept of substrate body-switching (a) schematic of Rx switch (b) body-switch turning on when Tx mode switch is in ON state (c) body-switch turning off when Tx switch is in OFF state.

A Tx-mode operation of the switch prefers the bulk port to be grounded to enhance power-handling capability of the Tx switch. However, an Rx-mode operation of

the switch requires the bulk port to be connected to high-impedance capacitors to maintain a low insertion loss of the Rx switch. Therefore, the switch operation is necessary at the bulk port of one of cascaded NMOS devices in a receiver switch. Experimental results show that the switch employing the body-switching technique can improve power-handling capability by 2.5 dB compared to the switch using the cascaded structure with the body-floating technique.

3.3.1. Method of Power-Handling Improvement

The power-handling capability of an RF switch is determined by both maximum current flows in the ON-state device at the Tx switch and maximum voltage swing in the OFF-state device at the Rx switch [5]. Several methods to increase the power-handling capability were introduced in chapter 1: LC resonator circuits [5], multi-stack FETs, and impedance transformation [5] are well-known methods for high-power RF switch design. The multi-stack structure of the Rx switch divides the voltage swing from the antenna port into each OFF-state stacked switch; thus resulting in reducing the burden of gate-to-drain/source breakdown voltage and source-to-drain breakdown voltage. The voltage swing level at the antenna port is one of the factors limiting the power-handling capability of the RF switch [26]. A multi-stacked FET scheme, as shown in Fig. 3.21, is chosen as the method to increase power-handling capability of the RF switch. Three thick gate-oxide devices with 0.35 μ m gate length were stacked to increase the power-handling capability.

Considering the voltage-dividing mechanism by parasitic capacitors in OFF state devices [26], the gate-oxide breakdown voltage of the devices, which is 6.8 V for thick

oxide devices[27], plays a key role in determining power-handling capability. Theoretically, considering voltage dividing by multi-stack FETs, the maximum voltage swing allowance of the three stacked thick gate-oxide FETs in OFF state in a 0.18 μm standard CMOS technology is 20.4 V. The maximum power-handling capability, P_{max} , of the multi -stack switch follows equation (1), where N is the number of the stacked devices, and Z_{ANT} is impedance of the antenna.

$$P_{\text{max}} = \left[N \times (V_{\text{GD}} - V_{\text{threshold}}) \right]^2 / 2Z_{\text{ANT}} \dots\dots\dots(1)$$

As shown in Fig. 3.22, the voltage swing level at C_{GD} and C_{GS} of each stacked FET in OFF state with 30 dBm input power remains under the gate-oxide breakdown voltage of each device. Therefore, the voltage swing of 30 dBm input at the antenna port is durable in the three- stacked FET scheme.

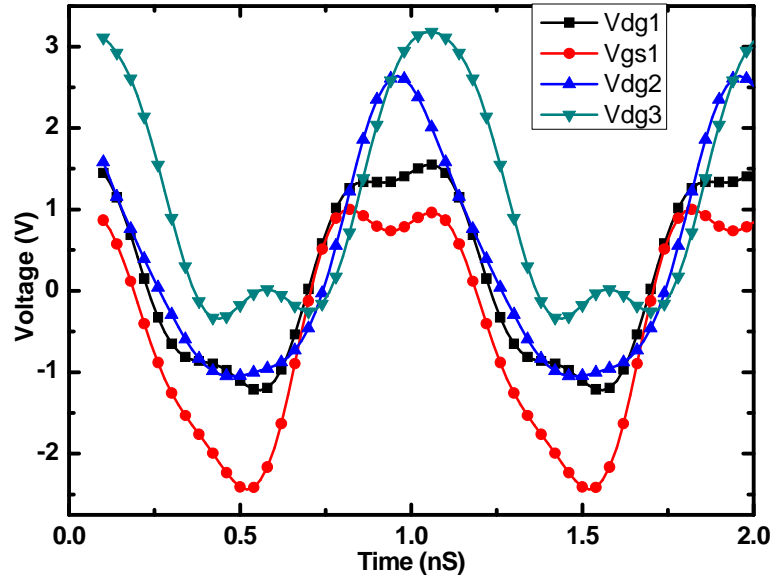


Fig. 3.22. Voltage swing at each parasitic capacitor. CGD and CGS (Pin=30 dBm).

To further increase the power-handling capability in a Tx-mode operation and to improve the insertion loss in an Rx-mode operation, we propose the body-switching

technique. The body-switching technique is associated with the body-floating technique by applying the body switch in parallel with the body-floating resistor to one of the multi-stacked RF switches. The device with the body switch needs to be located close to the Rx blocks to minimize the effects of the voltage distortion at the antenna port, as shown in Fig. 3.21. Fig. 3.23 presents the equivalent circuit model of the switch (M3) in Fig. 3.21.

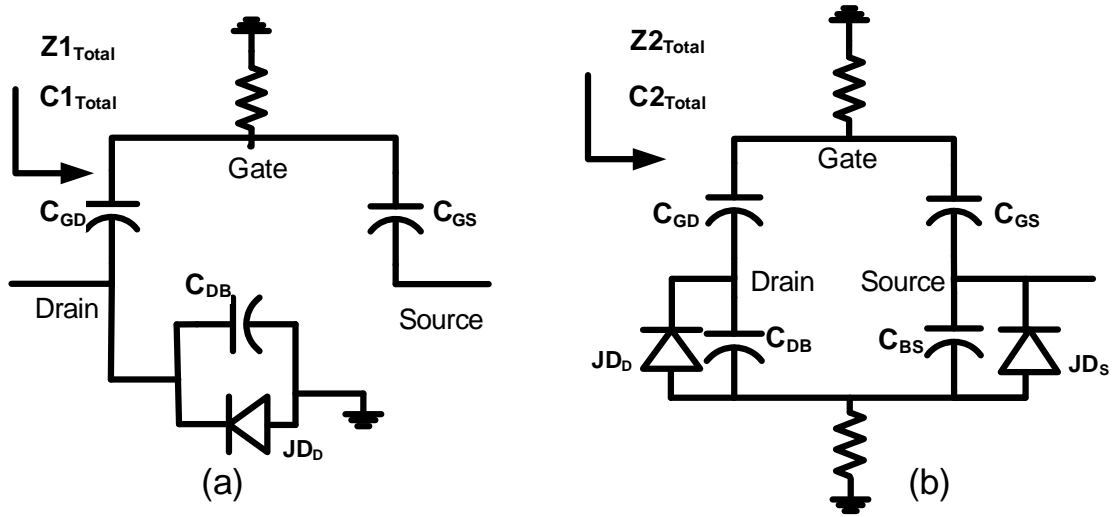


Fig. 3.23. Equivalent circuit models of (a) the switch with body grounded and (b) the switch with body floating, both in OFF state.

Equation (2) and (3) explain the total capacitance and impedance of the equivalent circuit model in Fig. 3.23. $C1_{Total}$ and $Z1_{Total}$ is capacitance and impedance of the body grounded switch, respectively, in Fig. 3.23 (a). $C2_{Total}$ and $Z2_{Total}$ is capacitance and impedance of the body-floating switch, respectively, in Fig. 3.23 (b).

$$C1_{Total} = (C_{GD} // C_{GS}) + C_{DB}$$

$$C2_{Total} = (C_{GD} // C_{GS}) + (C_{BS} // C_{DB}) \dots\dots\dots(2)$$

$$1/(j\omega C1_{Total}) \approx Z1_{Total} < Z2_{Total} \approx 1/(j\omega C2_{Total}) \dots\dots\dots(3)$$

In the Tx-mode operation, the body switch turns ON so that the bulk port can be grounded. Depending on the operation of the body switch, the equivalent circuit model of the switch with the body switch (M4) in Fig. 3.21 is differently described as shown in Fig. 3.23. Because the impedance of the OFF-state switch device depends on the total capacitance of the switch device, $Z1_{Total}$ is smaller than $Z2_{Total}$ in a small signal operation, as shown in equation (2) and (3). When the device ($W=512\text{ }\mu\text{m}$, $L=0.35\text{ }\mu\text{m}$) is used, the $C1_{Total}$ and $C2_{Total}$ is 3.98 pF and 1.98 pF respectively. In a large signal operation, as the negative voltage swing increases at the antenna port, the voltage difference between the source and the gate becomes larger than the threshold voltage of the transistor. Therefore the switch devices in OFF state at the Rx path start to form channels so that undesirable leakage current flows from the antenna port to the Rx blocks in the case of the high-negative voltage swing. However, when the substrate switch (M4) is ON at the last stage in the multi-stacked structure in the Rx switch, the channel formation in the last device is prevented by the junction diode operation. When the negative voltage swing is applied to the Rx switch with the body-switch ON, one of the junction diodes close to the Rx block turns on. As a result, the voltage drop caused by the junction diode turning on between the body port and the drain port prevents the channel formation. The turned-on junction diode fixes the voltage at the source port of the switch device (M4) to zero so that the switch device with the body grounded does not form a channel in the negative voltage swing. Because one of the channel formations in the multi-stack FETs caused by the negative voltage swing at the antenna port is disabled, overall leakage current at the antenna port can be significantly reduced.

There is a tendency for the negative voltage swing to be distorted at the switch device (M3) with the body grounded (M4) because of the turned-on junction diode. As stated earlier, the voltage swing at the antenna port is divided by the number of stacked switch devices. Therefore, the distorted voltage swing caused by the negative voltage swing is only a fraction of the overall voltage swing at the antenna port. Instead, leakage currents of the OFF state devices are significantly reduced. Therefore, the power-handling capability of the Tx switch using the body-switching technique can be improved by 2.5 dB at 31.5 dBm input power.

In the Rx-mode operation, the body switch turns off to take advantage of the body-floating technique. As the periphery of the device increases, the insertion loss of the ON-state Rx device depends more on parasitic capacitance than the ON resistance. If the body switch turns off, the high impedance of the OFF-state device can provide a similar effect as the body-floating technique. The switch with the body-floating technique can have lower insertion loss than that with the body port grounded, because the switch with the body-floating technique reduces leakage currents into the substrate. This is the main reason why the switch operation is needed at one of the bulk ports of the device in the Rx switches. The ON state of the body switch helps enhancement of the power-handling capability in the Tx-mode operation. The OFF state of the body switch enables the Rx switch to maintain low-insertion loss by reducing leakage currents toward the substrate.

3.3.2. SP4T Switch Design and Measurement Data

An SP4T CMOS switch is designed and implemented. The measurement data demonstrate that the body-switching technique is a very effective method of improving power-handling capability without compromising insertion loss performance. All the switches of the SP4T CMOS switch have employed the body-floating technique in a three-stacked FETs scheme. The body-switching technique is applied to one of the Rx switch devices, as shown in Fig. 3.24. The body-switching technique can be applied only to the Rx switch. Any NMOS devices in Tx switches cannot have a switch operation at the bulk port since the bulk port can look at the high voltage swing according to the body-floating technique. In that case, the power-handling capability of the switch is decided by the switch connected to the bulk port.

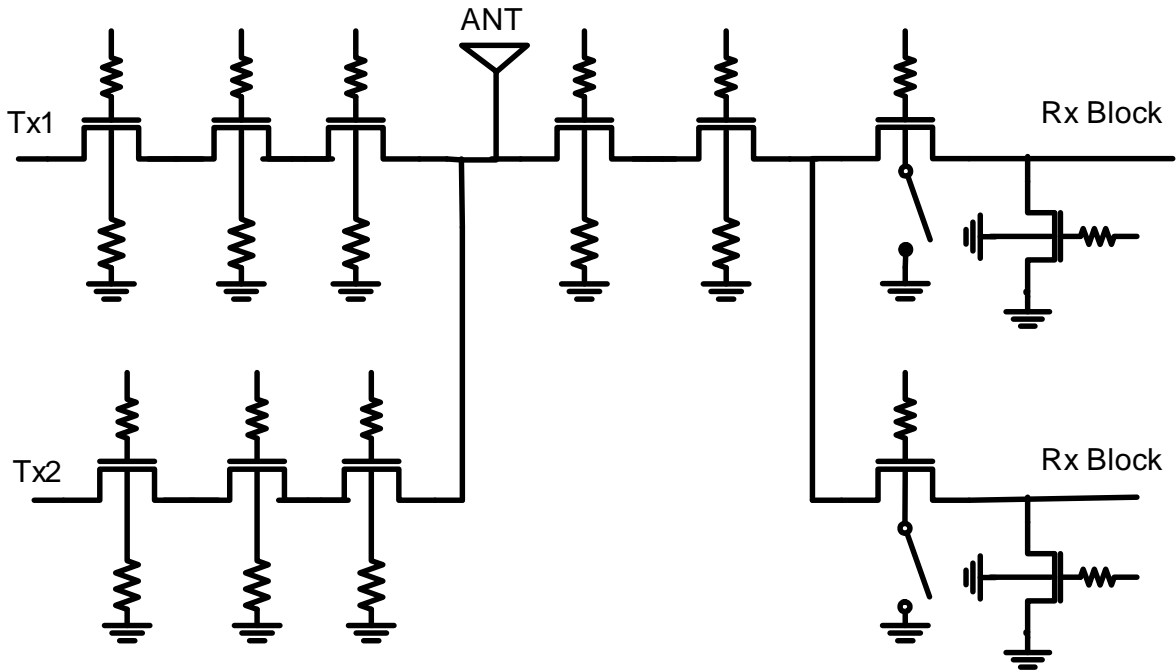


Fig. 3.24. Schematic of SP4T switch using body switching technique.

Tx switches do not have shunt devices to maximize power-handling capability, because those shunt devices increase leakage currents and the breakdown voltage of the shunt devices degrades the overall power-handling capability performance. However, this configuration might compensate the insertion loss of the Rx switch because of the degraded isolation of the Tx switch when the antenna receives the signal. The fabricated IC is assembled on a PCB to measure the power performance with supply of the high power signal, as shown in Fig. 3.25. The PCB is made of FR-4 material, which has a 4.3 dielectric constant and a 0.03 tangent loss. Even though the overall size of the IC is 900 μm by 600 μm that is mainly dominated by the number of the RF and DC pads, the actual area of the SP4T switch is 700 μm by 300 μm .

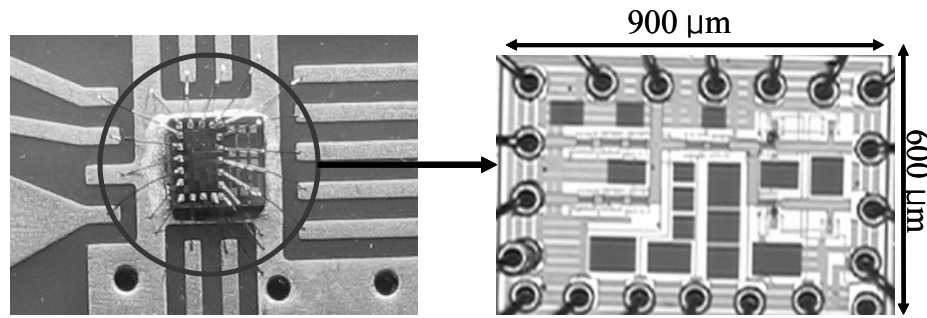


Fig. 3.25. Photograph of the SP4T switch using body switching technique

The S-parameter measurement of the fabricated switch in a Tx-mode operation is shown in Fig. 3.26. The results of the return loss demonstrate that the switch can have good input/output matching by using the inductance of the bond wire and capacitance of the device even though no shunt devices are incorporated in Tx switches. The measurement results of the 1dB compression point, as shown in Fig. 3.27, demonstrates that the structure with the body switch ON has a P 1dB 2.5 dB higher than the one with the body switch OFF.

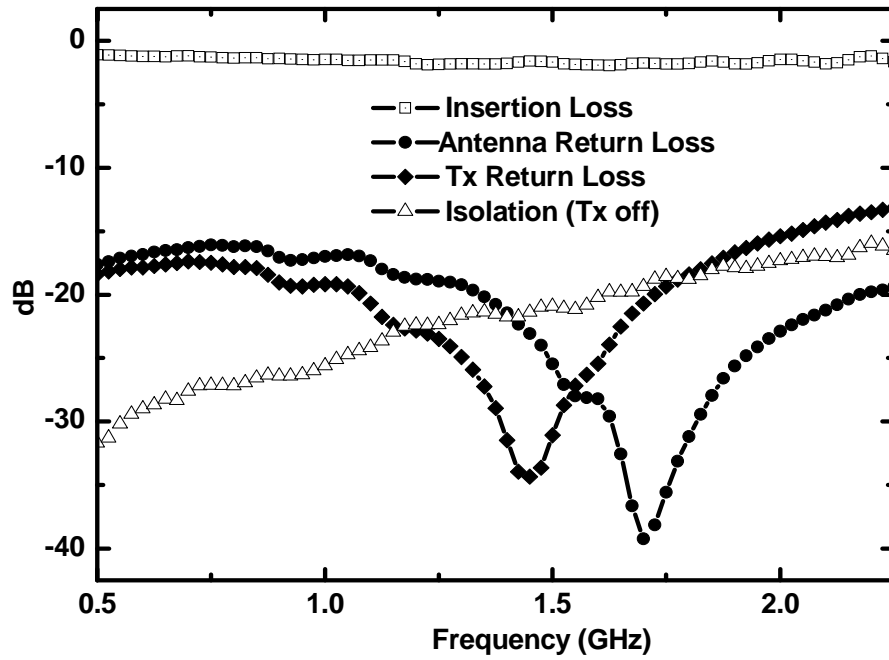


Fig. 3.26. Measurement data of the Tx switch performance.

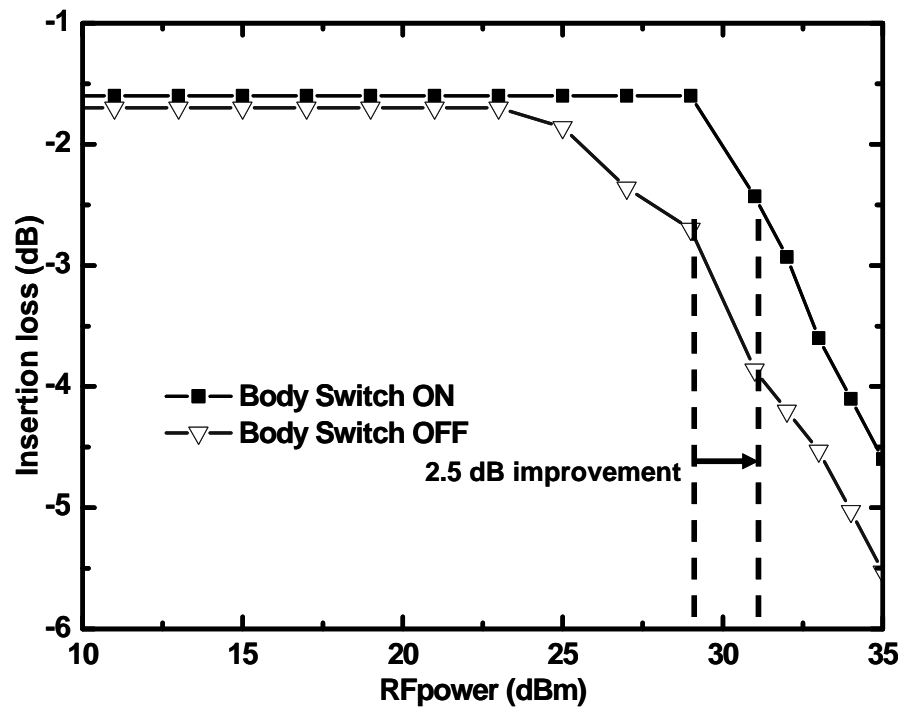


Fig. 3.27. P1dB performance of the TX switch.

The substrate body-switches are in OFF state when the Rx switches are receiving signals from the antenna port. The measurement results of the S-parameter of the Rx switch are shown in Fig. 3.28, where the insertion loss of the Rx switch with the body switch OFF is lower than the one with body switch ON.

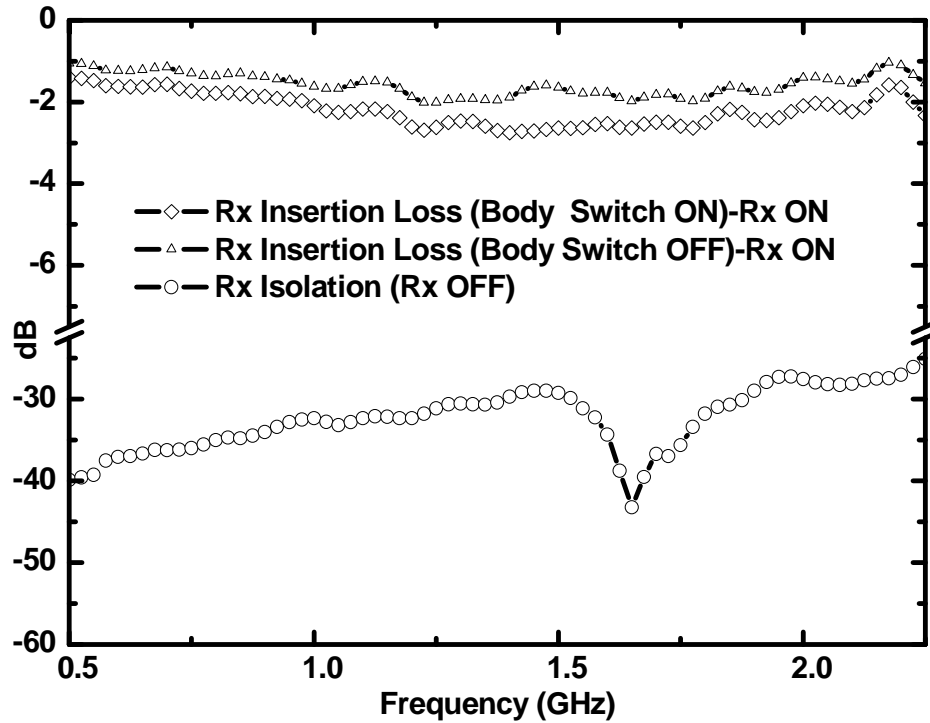


Fig. 3.28. Measurement data of Rx switch performance. Insertion loss improvement by body-switch operation.

These data demonstrate the main advantage of the body switch operation. As the size of each device in the multi-stack FET switch increases to minimize the insertion loss, the parasitic capacitors between device ports, such as source-to-body-to-drain and source-to-gate-to-drain, act as signal paths along with the ON-state resistance. In the multi-stacked switch, the switch with the floating body (the body switch OFF) has a lower insertion loss than the one with the body grounded (the body switch ON) by having one more signal paths between the source-to-body and body-to-drain.

3.3.3. Summary

A high-power CMOS RF switch using the substrate body-switching technique is proposed. The body switch at the bulk port in one of the multi-stacked Rx switches turns on to maximize the power-handling capability in the Tx-mode operation and turns off to minimize the insertion loss in the Rx-mode operation. The experimental data demonstrate the improvement of the power-handling capability by 2.5 dB of P_{1dB} in the Tx-mode operation as well as the enhancement of the insertion loss up to 1.0 dB in the Rx mode operation by using the proposed body-switch operation.

CHAPTER 4.

RF CMOS SWITCH USING ADAPTIVE VOLTAGE SWING DISTRIBUTION METHOD IN MULTI-STACK FETS

4.1. Introduction

Recent research and commercial products in the wireless communication industry show that modern silicon technology can be utilized in designing high frequency circuits[28]. In particular, radio frequency (RF) circuit designers utilize a standard CMOS process in implementing receiver circuits such as low noise amplifiers (LNAs), voltage controlled oscillators (VCOs), variable gain amplifiers (VGAs), and mixers, while some key blocks such as power amplifiers (PAs) and antenna switches are still manufactured by non cost-effective GaAs-based high power processes in commercial products. However, the advantages of a CMOS process such as low cost and high integration capability spur the development of high-power handling devices in a standard CMOS process. In spite of not being commercially available yet, many efforts have been made to achieve high power CMOS PA design [29-31] and some of them show comparable performance with their counterpart, GaAs power amplifiers. However, the design of antenna switches using a standard CMOS process for high-power applications still suffers from the material characteristics of CMOS technology such as low mobility, low breakdown voltage, and parasitic capacitance[32] . Most of all, the existence of junction diodes in Si-substrate that do not allow negative voltage swing is the main drawback of CMOS switches in high power operations[32-34]. This challenging issue has been resolved by employing the body-floating techniques[8-9]. The LC resonant type body-

floating technique[10] was demonstrated in a digital CMOS process, showing 28 dBm of P1dB at 2.4 GHz and 5 GHz operation, and the resistive body floating technique [11] was implemented in a deep N-well CMOS process to demonstrate 21.5 dBm of P1dB at 2.4 GHz. The resistive body-floating technique has advantages such as small size, wideband operation and latch-up free phenomenon. Most of recent CMOS switch designs employ this technique. Another approach to enhance power handling capability has been attempted by using negative supply voltage to the body substrate [35], resulting in 26 dBm of P1dB. The power handling capability was also improved by designing a differential switch [36], which has 30 dBm of P1dB in wide bandwidths. The methods described above have drawbacks such as necessity of negative voltage and power combining in the antenna port, etc. There have been many other attempts to achieve a high power CMOS switch using voltage level shift [37, 38], and an impedance transformer network [38]. However none of them succeeded in obtaining watt-level power handling capability.

In this section, a watt-level high power CMOS switch is reported. This switch is fabricated on a standard 0.18- μ m CMOS process. A multi-stack FET scheme is chosen as a fundamental method of high-power operation [5]. The proposed method of adaptive voltage swing distribution in multi-stack FETs in the OFF state incorporates the resistive body-floating technique. The proposed structure utilizes a combination of drain-to-body junction diodes and drain-to-body junction capacitors as well as the parasitic capacitors between gate and drain/source to adaptively distribute voltage swing at the antenna port toward the OFF-state FET depending on the voltage swing level. As a result undesirable channel formation in the OFF-state FETs can be prevented. The experimental data of the

SPDT switch based on the proposed structure demonstrate that a 0.3 dB compression point can be obtained at 33.5 dBm input power at 1.9 GHz. This is the best power handling capability of CMOS switches in a standard 0.18- μ m CMOS process ever reported. Also, the power handling capability of the proposed structure using the series shunt configuration, where the Tx switch and Rx switch are used as series and shunt respectively, is expressed.

This chapter begins with the introduction to the fundamental theory of the adaptive voltage swing method in the multi-stack FETs. Specifically, the voltage-swing behavior between each port of the device in the multi-stack FETs is fully analyzed. Measurement data of the proposed structure is compared to that of the conventional structure in terms of the isolation performance according to the input power sweep. In Section 4.3, the design of the single pole double throw (SPDT) switch using the adaptive voltage swing distribution method is introduced. A description is given to the behavior of the voltage swing at a single CMOS switch using the resistive body-floating technique. Analysis of the voltage-swing distribution mechanism in the CMOS multi-stack FETs in OFF state is also discussed. Also, a principal analysis[39] of the proposed adaptive voltage swing distribution method is introduced with detailed explanation of voltage swing behavior at each node of the multi stack FET. Experimental results are discussed with comparison between two implemented switches, where the superiority of the proposed design in terms of reduction of the voltage stress on one of the stacked FETs is explained in relation to the gate oxide breakdown voltage of the switch device.

4.2. A Novel Multi-Stack Device Structure and its Analysis for High Power CMOS Switch Design.

In this section, the operation of a multi-stack structure in a high power CMOS switch is characterized. The inspiration from this analysis encourages a proposal of a new method to improve power handling capability in CMOS switch design. The proposed structure incorporates a source or drain connection with a bulk port in a multi stack NMOS switch using a standard CMOS 0.18 μm process, still employing a body floating technique. This structure is designed and tested for the purpose of high power CMOS switch devices.

4.2.1. High power Switch Design

Power-handling capability of the switch is limited by both maximum current flow in the ON device at the Tx switch and maximum voltage swing in the OFF device at the Rx switch. The current limitation in the Tx switch can be resolved by increasing size of the device. The voltage swing limitation at antenna port can be resolved by employing high-power switch design schemes: LC resonator circuits, multi-stack FETs and impedance transformation[7] are well known methods for high-power RF switch design. Among these high-power design methods, the multi-stack FET method was incorporated because of its compact design capability. The multi-stack FETs scheme in the Rx switch enhances the power-handling capability of the Tx switch by increasing voltage swing level at the antenna port. The overall voltage swing at the antenna port can be divided by the number of stacked transistors. Basically, the power-handling capability of the Tx switch can be improved at the cost of the Rx switch insertion loss. However, the voltage dividing principle in GaAs FET switch design does not directly apply to the CMOS FET

switch design, because the secondary voltage dividing is affected by parasitic junction diodes and junction capacitors. Meanwhile, the primary voltage dividing is determined by gate-to-drain and gate-to-source junction capacitors.

4.2.1.1. Operation of Conventional Multi-Stack Structure Switch

As shown in Fig. 4.1, a lumped element model of the multi stack FET switch devices in OFF-state consists of a series of gate-to-drain and source-to-gate parasitic capacitors, a series connection of drain-to-bulk and bulk-to-source junction capacitors and a back-to-back connection of drain-to-bulk and bulk-to-source junction diodes. The voltage swing division in the path which consists of junction diodes and junction capacitors follows a different fashion from the division in the path made up of drain-to-gate-to-source capacitors, according to the case of positive voltage swing or negative voltage swing as well as to the level of the input power at the antenna port.

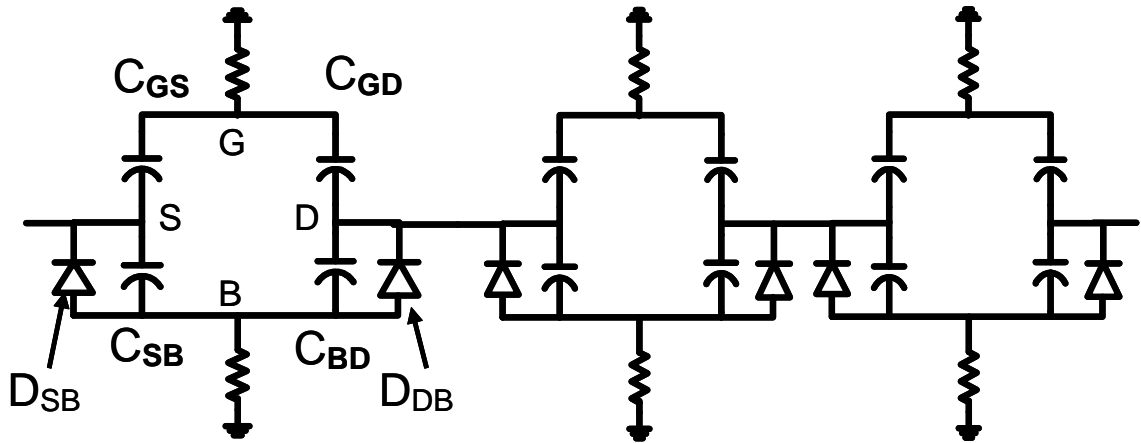


Fig. 4.1. Equivalent lumped element model of the conventional multi-stack structure.

With a small signal input, the leakage current in the receiver switch is determined by impedance of the multi-stack structure in OFF state, whereas channel formation of the switch in OFF state is the main contributor of leakage current with large signal input. In

the case of positive voltage swing, V_{SB} and V_{BD} , the voltages between source-to-bulk-to-drain are unequally divided, while V_{SG} and V_{GD} , the voltages between drain-to-gate-to-source are equally divided. V_{BD} voltage between the bulk and the drain drops as much as threshold voltage of junction diode D_{BD} so that V_{BD} is getting smaller than V_{SB} as the input power increases. This, in turn, results in uneven junction capacitor values C_{BD} and C_{SB} , which follows equation (1) [7].

$$C_{junction} = \sqrt{\frac{\epsilon_{si} q N_a}{2 \times (\psi_{built_in} + V_{applied_to_junction})}} \dots\dots\dots (1)$$

This principle also can be applied to the case of negative voltage swing, where V_{SB} is smaller than V_{DB} shown in Fig. 4.2. However, the main reason for the leakage current in the large signal input is different from the one in the small signal input. In case of negative RF cycle, V_{GS} increases as the voltage swing increase. Once the V_{GS} crosses the threshold voltage of the device, the device tends to form a channel temporarily so that unexpected leakage current flows in the OFF state device. This undesirable channel formation in the OFF state device lowers overall impedance of the receiver switch so that power handling capability of the transmit switch diminishes. Apart from channel formation by the enlarged voltage differences between the gate and the source, overall leakage current can be augmented by junction diode turn-on-current both in negative voltage swing and in positive voltage swing.

Also one of junction diodes that does not turn on can provide an issue of reverse breakdown as the voltage difference in nodes S, B, and D in Fig. 4.2 increases. These

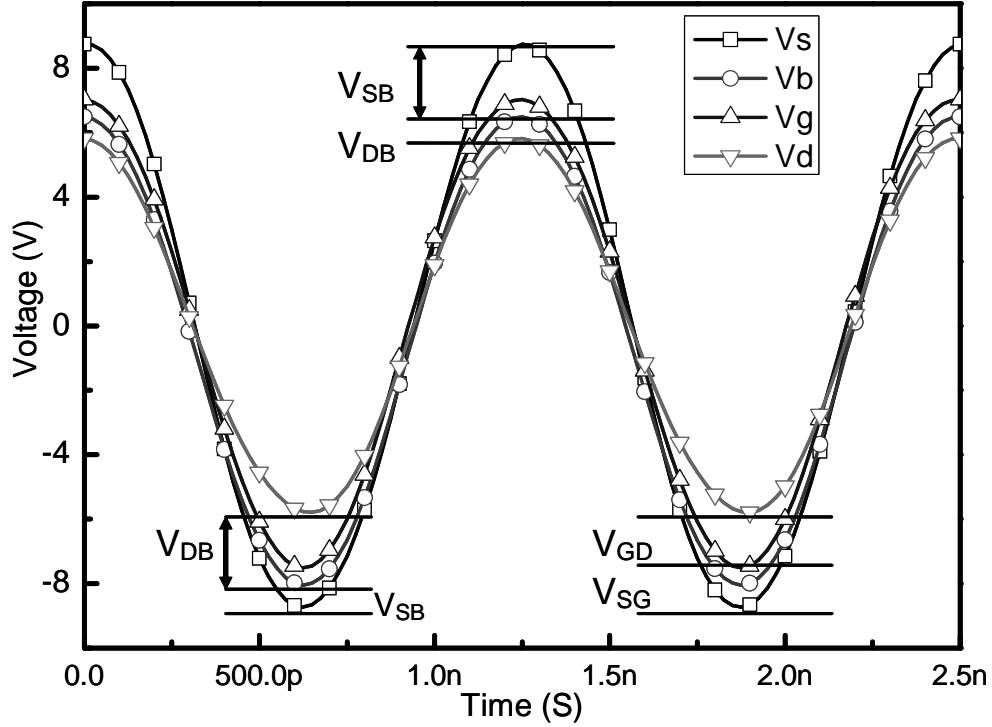


Fig. 4.2. Voltage swing dividing of conventional multi-stack switch in OFF state (24 dBm input power).

phenomena are the primary reasons why a CMOS switch even in a multi-stack structure can have a limitation in terms of power-handling capability.

4.2.1.2. Operation of Proposed Multi-Stack Structure

Fig. 4.3 presents a schematic of the proposed multi-stack structure of the high-power CMOS switch. Fig. 4.4. shows the equivalent circuit model of the proposed structure in the OFF state. Differently from the structure in the prior art, bulk ports of the first two switch devices toward the antenna side in this proposed multi-stack structure tie up with the source as shown in Fig. 4.3.

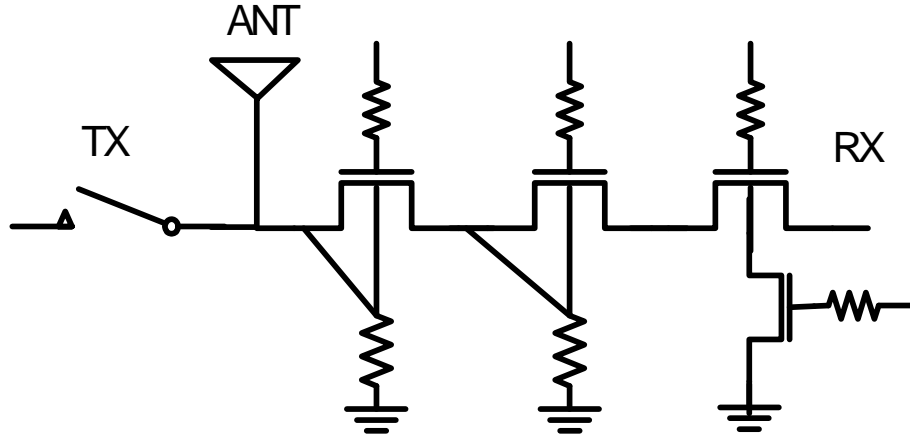


Fig. 4.3. Proposed multi stack structure CMOS switch.

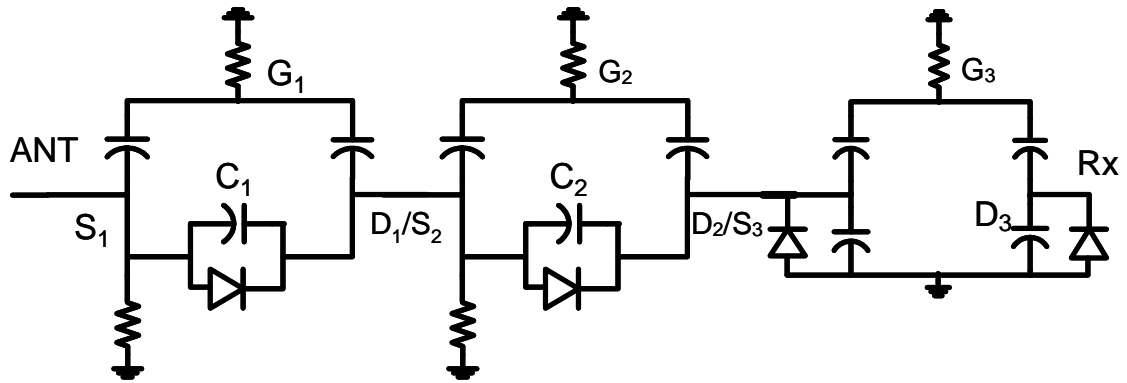


Fig. 4.4. Equivalent lumped element model of the proposed structure in the OFF-state.

The last switch among multi-stack NMOS switches, which is closest to the receiver blocks, can have a body switch at the bulk port.

Compared to the structure shown in Fig. 4.1, the proposed structure has lower impedance in OFF state in case of small signal input. A disabled junction capacitor leads to the reduction of impedance in the OFF-state device. However, with a large signal input, the impedance of the proposed structure is higher than that of the conventional multi-stack structure.

In the case of the large voltage swing, voltage-dividing behavior in the positive cycle is totally different from that in the negative voltage swing. The shape of the voltage swing between each device in Fig. 4.4 is shown in Fig. 4.5.

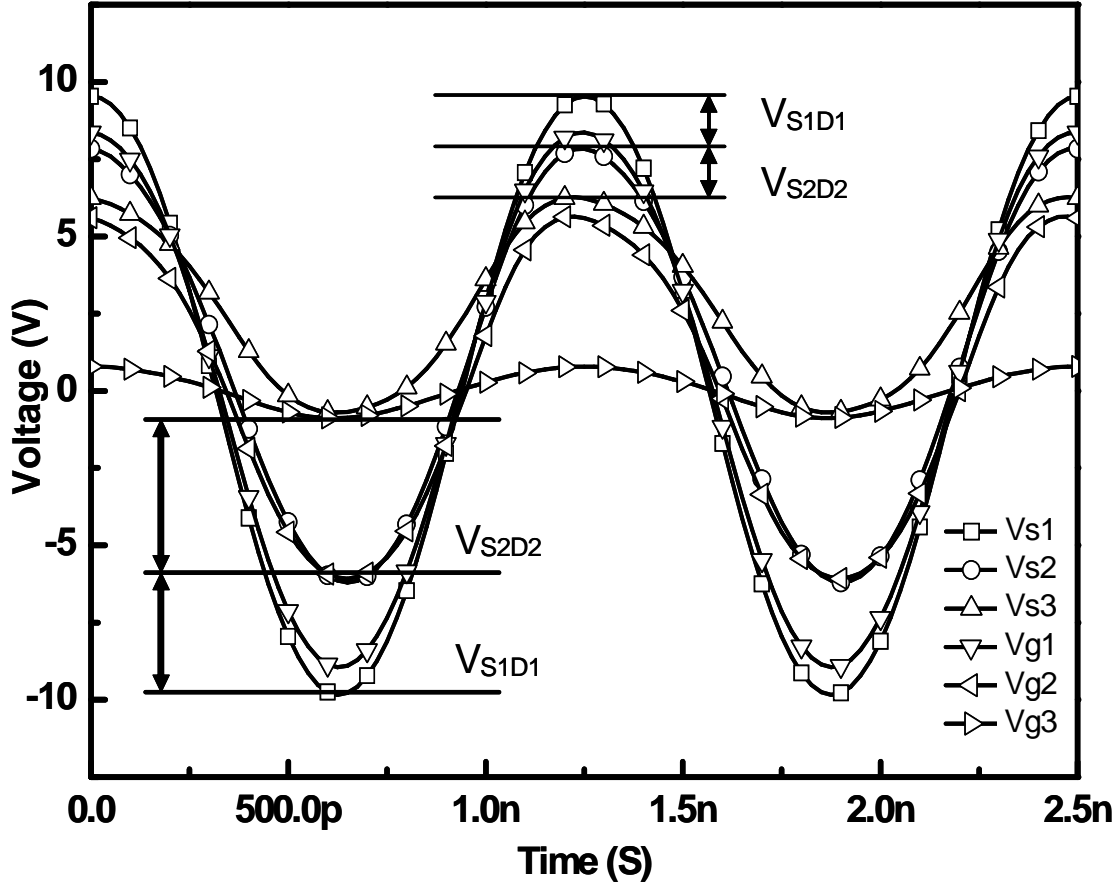


Fig. 4.5. Voltage swing of the proposed multi-stack structure.(24 dBm input power).

In the case of positive voltage swing, V_{S1D1} and V_{S2D2} , as shown in Fig. 4.5, can be fixed by junction diode threshold voltage. However, in the negative voltage swing, the voltage splitting between V_{S1D1} and V_{S2D2} is determined by the ratio of junction capacitor C_1 to C_2 and the impedance of the last device in OFF state. This voltage swing appears as though the DC level of each voltage swing at nodes D1/S2 and D2/S3 is shifted up, which can be one of methods to improve power handling capability in high power GaAs

switch design. Interestingly, the primary voltage swing dividing mechanism through the series path consisting of drain-to-gate-to-source links in the proposed structure follows the same fashion as the voltage swing at each gate port in the structure shown in Fig. 4.1, because DC level at the gate port in each device is fixed by the control voltage of the switch device which is zero in OFF state. Meanwhile, the DC level of the voltage swing at point D_1 and point D_2 in Fig. 5 is decided by the ratio of junction capacitors.

From Fig. 4.5, V_{S2} and V_{S3} , voltages at point S_2 and point S_3 in Fig. 4.4, are higher than gate voltages V_{G1} and V_{G2} in the case of negative voltage swing so that channel formation in OFF state devices does not occur. Also in the case of positive voltage swing, V_{S2} and V_{S3} voltages at point S_2 and point S_3 are higher than gate voltages V_{G1} and V_{G2} , respectively, so the channel of the device in the OFF state is not created, either. As a result, even if the voltage swing level increases at the antenna port, the proposed multi-stack structure can have higher OFF-state impedance than the conventional multi-stack structure by preventing channel creation of the device in OFF-state. The reason for the last device having different structures compared to the other devices is that if the bulk port of that device is connected to S_3 , the DC voltage at the point S_1 , S_2 and S_3 is fixed by the threshold voltage of the junction diodes so that voltage dividing at each device follows the same trends as voltage dividing in the conventional structure cases. Fig. 4.6 shows the leakage current of the conventional multi-stack structure and the proposed multi-stack structure in the OFF state. The reduced leakage current of the OFF-state device in the proposed structure is due to the suppressed channel formation.

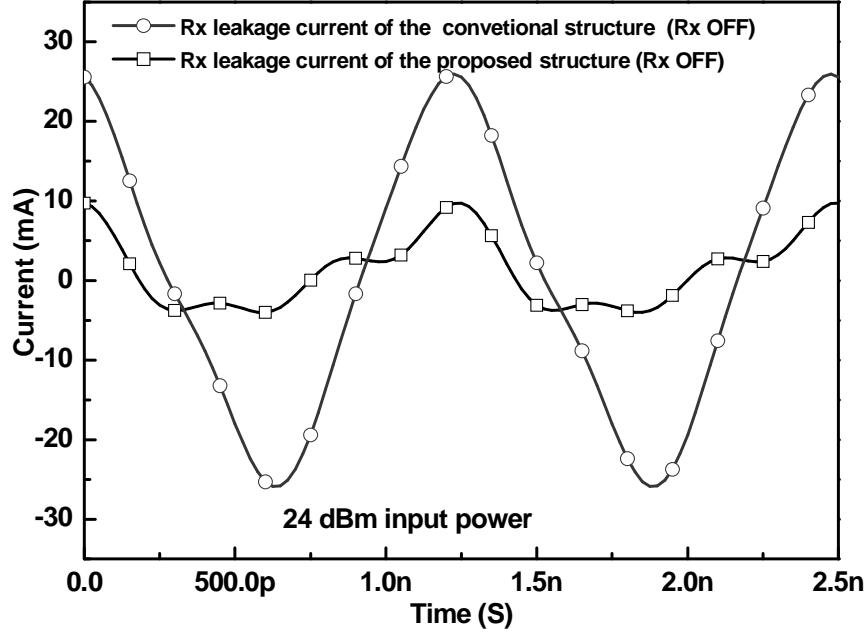


Fig. 4.6. Leakage current of the conventional multi-stack structure and the proposed multi-stack structure in OFF state.

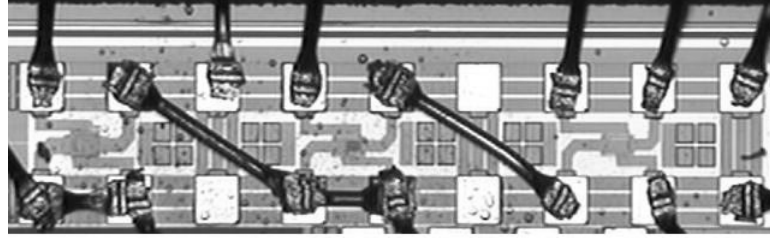
4.2.1.3. Measurement Results

The novel multi-stack structures in the CMOS switch are implemented by connecting CMOS switches located in a row using bond wire for high power characterizations. All the structures are assembled and measured on Chip-On-Board (COB) to apply high power input to the test structure. The photographs of the conventional multi-stack structure and the proposed multi-stack structure are shown in Fig. 4.7 (a) and (b), respectively.

First, isolation of the each structure in OFF state was measured with respect to the input power level to verify the improvement of high power handling capability of the proposed structures. As shown in Fig. 4.8, the measured power isolation levels of each multi stack structures vary according to the input power level.



(a)



(b)

Fig. 4.7. Photographs of test structures. (a) Conventional structure and (b) proposed structure.

As expected from the simulation results, the structure using the conventional multi-stack has a lower knee input power level (transition point of isolation level) than the one of the proposed structure. The alteration of isolation in OFF-state device with respect to power level can result in the increase of power-handling capability of the switch device in ON state. Therefore, the proposed structure demonstrates higher power-handling capability.

Fig. 4.9 shows the isolation level of the test structures in OFF state at a small signal input and the insertion loss in ON state according to the body-switch operation. As explained, the proposed structure has lower impedance at a small signal input than the conventional structure because of the disabled junction capacitors.

This fact results in lower isolation in a small signal input than that of the conventional structure. However, the low isolation performance can be extended to higher input power level.

In the case of ON state, disabling one of the junction capacitors and junction diodes does not affect the performance of the insertion loss because of equal potentials between all the sources and drains.

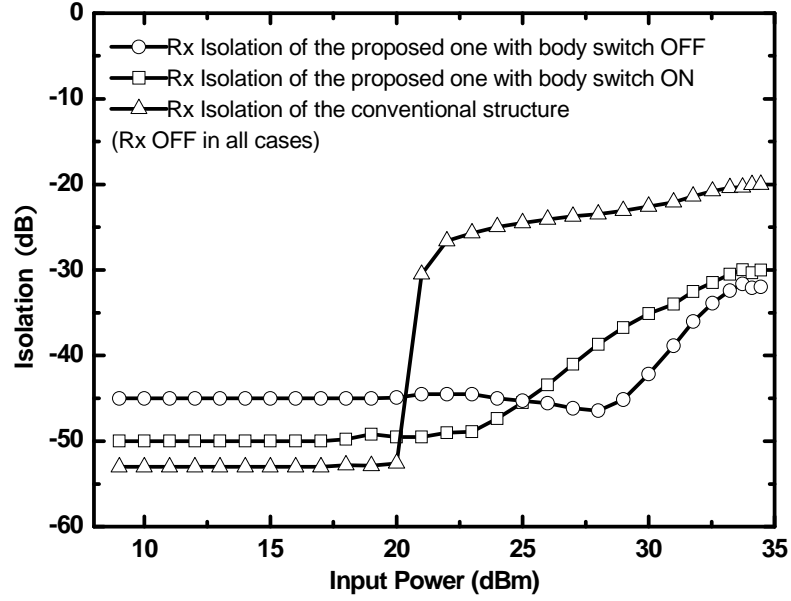


Fig. 4.8. .Measured isolation of test structures with respect to input power level at 900 MHz.

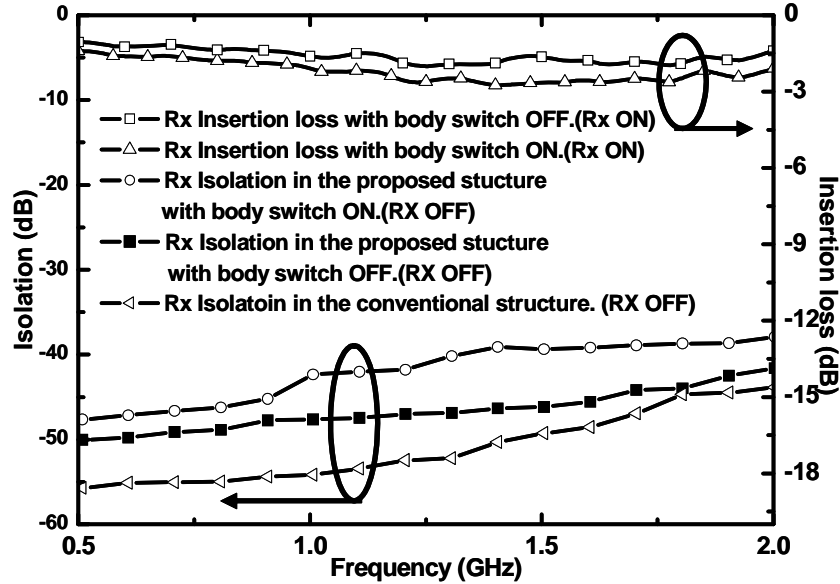


Fig. 4.9. The measurement-data comparison of the isolation and the insertion loss between the conventional structure and the proposed structure.

The power handling capability can be improved more by connecting the bulk port of the last switch device to the ground. However, the insertion loss can be minimized when the last device is in the body floating state by blocking the leakage current from flowing toward the ground. The trade off between the power-handling capability and the insertion loss can be resolved by applying the body- switching technique [40]. The insertion losses in Fig. 4.9 were measured by applying the body-switching technique.

4.2.1.4.. Summary

A novel CMOS switch structure using multi-stacked NMOS devices for the purpose of a high-power CMOS switch design is proposed, fully analyzed, and characterized. The novel body-floating technique of the multi-stacked structure enables the voltage dividing between each device in a different fashion from the structure using the previously proposed body-floating technique. The novel structure prevents the channel formation of the device in OFF state so that the level of the isolation can be maintained consistency to the higher power input level. Therefore, this structure enables the further improvement of power handling capability of the CMOS switch.

4.3. A High Power CMOS Switch using a Novel Adaptive Voltage Swing

Distribution Method in Multi-Stack FETs

A high power CMOS switch using a novel adaptive voltage swing distribution method in a multi-stack FET scheme is proposed. The proposed adaptive voltage swing distribution method in the multi-stack FETs is effective in preventing unwanted channel formation of the OFF state FETs even in the case of using a low-control voltage. This, in turn, increases the power-handling capability in a large signal operation. In the proposed CMOS switch, the behavior of the voltage swing in the OFF-state multi-stack FETs shows difference with respect to the level of the input voltage swing. The characteristics of the voltage-swing distribution method and a leakage channel formation in the CMOS switch is fully analyzed by applying the novel adaptive voltage swing distribution method to a three-stacked NMOS Rx switch fabricated in a standard 0.18- μm triple well CMOS process. In addition, two different kinds of CMOS T/R switches are fabricated and fully characterized to verify the proposed technique in terms of power-handling capability associated with the resolution of voltage stress issues on one of the stacked FETs. The measured data of the proposed design shows a 0.3 dB compression point at the 33.5 dBm input at 1.9 GHz. The insertion loss of the Tx switch and the Rx switch are 1.6 dB and 1.9 dB, respectively, at 1.9 GHz. The isolation of the Tx switch and the Rx switch is around 20 dB and 30 dB, respectively, at 1.9 GHz.

4.3.1. Analysis of Voltage Swing Behavior in the CMOS Switch

The voltage swing behaviors at each node of the CMOS switches in case of both the single device and the multi-stack devices are analyzed.

It is essential for all the devices to be fabricated in the triple-well process of the CMOS technology.

4.3.1.1 A Single CMOS Switch with Resistive Body Floating Technique

Fig. 4.10 shows a cross sectional view of the individual NMOS switch. One of the biggest concerns in employing the resistive body floating technique is a latch-up phenomenon. When a PMOS device is fabricated along with an NMOS device in the same substrate, a group of parasitic bipolar transistors is formed [3]. If a resistor with a large value is connected to the bulk port on p-substrate, undesirable leakage current toward the substrate increases.

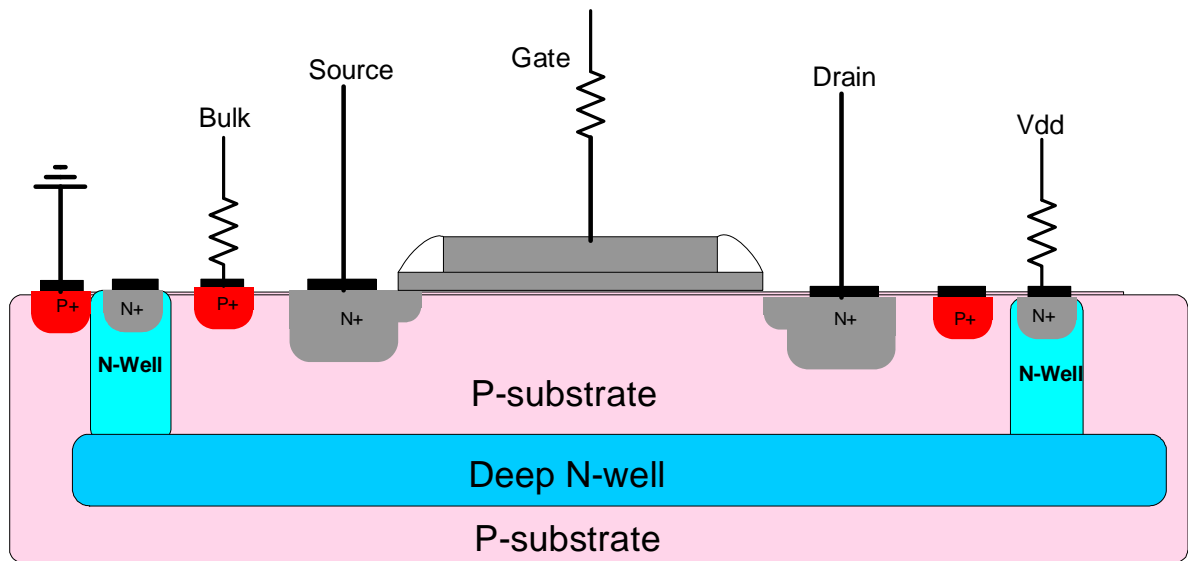


Fig. 4.10. Cross-sectional view of an NMOS transistor in a deep N-well structure.

Also this configuration is a prerequisite to employ a multi-stack FET scheme with the resistive body floating technique. Each bulk port of the multi-stacked CMOS FETs in OFF state has its own voltage swing behavior based on the voltage-dividing mechanism. Therefore, each device in the multi-stack FETs with the body-floating technique has to have its own substrate to prevent interference among divided voltage-swing signals at

each bulk port. To avoid this phenomenon, it is essential to fabricate each NMOS device inside individual deep N-well in the resistive body floating technique where a p-substrate inside an N-well is connected to a high value resistor and the N-well substrate is biased to V_{dd} through another high-value resistor to maintain isolation and reject interference between devices. Fig. 4.11 shows equivalent circuit models of an NMOS switch device with the resistive body floating technique in ON state (a) and OFF state (b). The resistive body floating technique is to prevent junction diodes from being forward biased in ON state. However, it is notable that the behavior of voltage swing at the NMOS switch shows different fashions when it is in ON and OFF state.

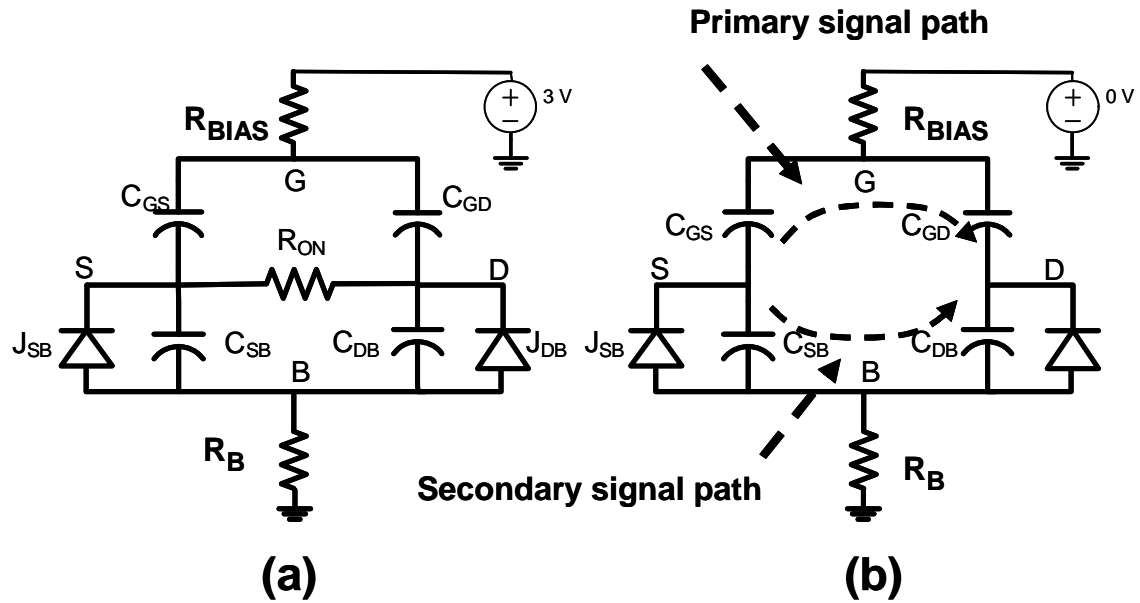


Fig. 4.11. Equivalent circuit models of a CMOS switch using resistive body floating technique (a) in ON-state and (b) in OFF-state.

Fig. 4.12 shows voltage swing waveforms between each port of the NMOS switch device in both (a) ON and (b) OFF state. When a large-voltage swing signal is applied to the NMOS switch in ON state, the voltage swing is divided according to the ratio

between the impedance of junction parasitic components and the resistance of the body floating component. Therefore, only a small amount of the voltage swing is applied to the junction diodes, J_{SB} and J_{DB} . Hence, the junction diodes are not forward-biased, as shown in Fig. 4.12(a) (V_{SB} in ON state).

In the case of ON state, V_{DS} is assumed to be equal due to the small turn-on resistance value of R_{ON} while there is voltage difference between source and drain in OFF state. In OFF state, the body floating resistor, R_B , and bias resistor, R_{BIAS} , operate as open circuits due to its high impedance. Voltage swing behavior of the switching device in OFF state is revealed in a different fashion from that of the ON state device, according to either small signal or large signal as well as either negative voltage swing or positive voltage swing. In the case of small signal operation, where voltage swing level is less than the turn on voltage of the junction diodes, J_{SB} and J_{DB} , voltage swing level at each port is decided by total impedance of the parasitic parameters. At each port, voltage swing is equally distributed and the leakage current toward the OFF-state device is estimated by total impedance of the OFF-state device. However, as the voltage swing level reaches the turn-on voltage of the junction diodes, which is referred as large signal input, the voltage swing behavior can be expressed by the voltage division scheme through both a primary signal path and secondary signal path as shown in Fig. 4.11. Primary voltage dividing follows the conventional voltage dividing principle of GaAs switches, while the secondary voltage swing is affected by parasitic junction diodes and junction capacitors. The voltage swing at V_{SB} and V_{BD} in Fig. 4.12 have an upper limit and lower limit, respectively, due to forward-biased junction diodes, J_{SB} and J_{DB} , at the peak point of the voltage swing.

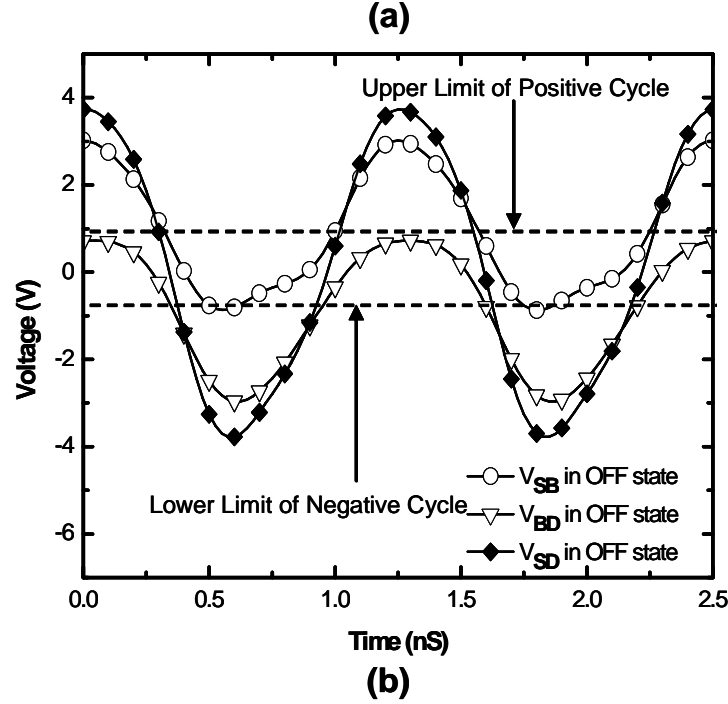
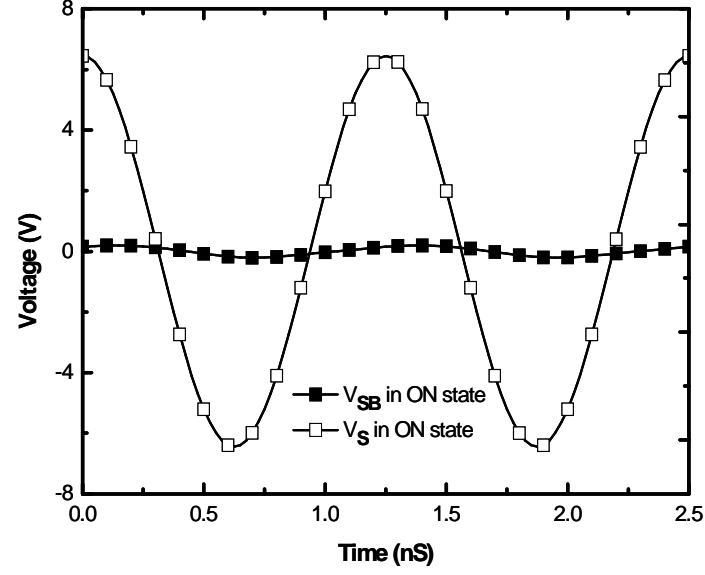


Fig. 4.12. Voltage swing behavior simulation of a single NMOS switch with resistive body floating technique (a) in ON-state and (b) in OFF-state.

In other words, the voltage swing of V_{SB} has a limitation of the negative cycle where the junction diode J_{SB} is forward-biased, while that of V_{DB} has a positive cycle limitation where the junction diode, J_{SD} , is forward-biased. This is a unique phenomenon of bulk CMOS switches which cannot be observed in GaAs switches.

4.3.1.2 A Multi-Stack CMOS Switch with Resistive Body Floating Technique

The multi-stack FET scheme is the most common method in high-power RF switch design due to its additional advantages such as wide bandwidth, small size, and the ease in handling small signal performances [26]. The multi-stack FETs help to reduce the voltage swing burden of each switch device in OFF state. The maximum power handling capability of the multi-stack FETs depends on the number of stacked devices where the breakdown voltages of V_{GD} and V_{GS} play a key role. However, the increase of the number of stacked devices causes degradation of the insertion loss due to the increasing R_{ON} in a series connection.

Fig. 4.13 shows the conventional multi-stack FETs scheme(a) and the proposed structure using the adaptive-voltage-swing-distribution method(b). The main cause of limiting power-handling capability in the multi-stack FETs structure is undesirable channel formation in the OFF-state device in the event of a large signal input. When the control voltage of the switch device is as low as 3.3V or 1.8V for ON state and as 0V for OFF state, this issue becomes more critical. The voltage boosting method in the drain and source port is commonly used in commercial GaAs switch applications to prevent channel formation in the OFF-state device.

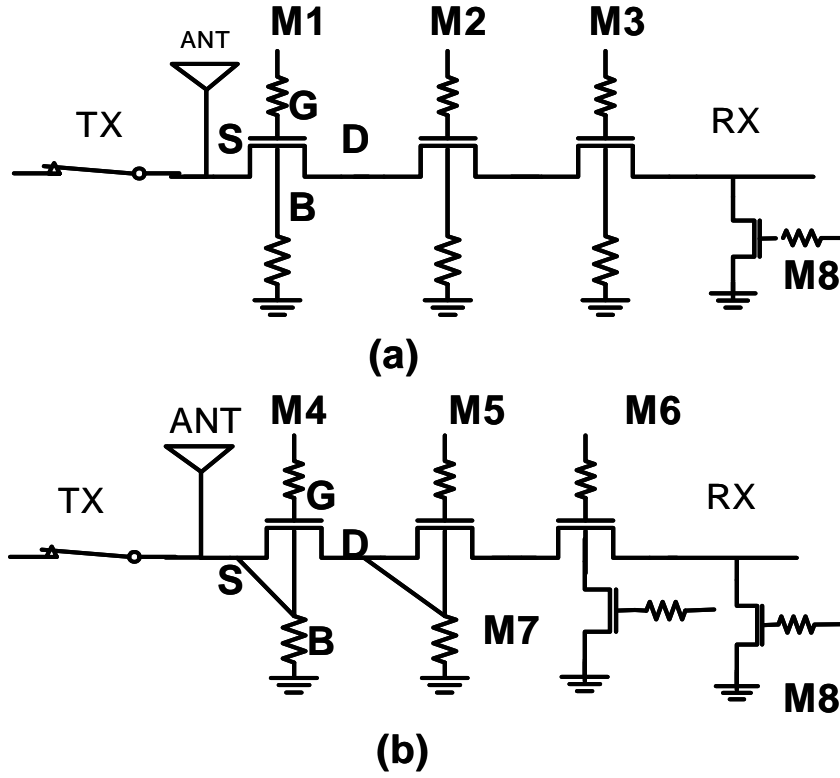


Fig. 4.13. (a) Conventional multi stack FETs (b) the multi stack FETs using adaptive voltage swing distribution with substrate body switching technique.

The proposed switch structure provides a novel method of preventing channel formation in CMOS switches without using any external components. The fundamental voltage behavior is described in detail in the following section.

4.3.1.3 Operation of the Adaptive Voltage Swing Distribution Method in the Multi-Stack FET Structure

Differently from the conventional structure in the prior art as shown in Fig. 4.7(a), bulk ports of the first two switch devices (M4, M5) in the proposed multi-stack structure are connected to the source as shown in Fig. 4.7 (b). The third switch device (M6), which is placed closest to the receiver blocks, has a body switch (M7) at the bulk port. The

operation of the M7 switch is described in [40]. All the resistors connected to FETs in Fig. 4.13 are 10 K ohm to provide high isolation.

Compared to the conventional structure, the proposed structure has lower impedance in OFF-state in the event of small signal input because a disabled junction capacitor leads to the reduction of impedance.

With a large signal input, the impedance of the proposed structure is higher than that of the conventional multi-stack structure. Fig. 4.14 shows the variations of the impedance in both the conventional structure and proposed structure according to input power.

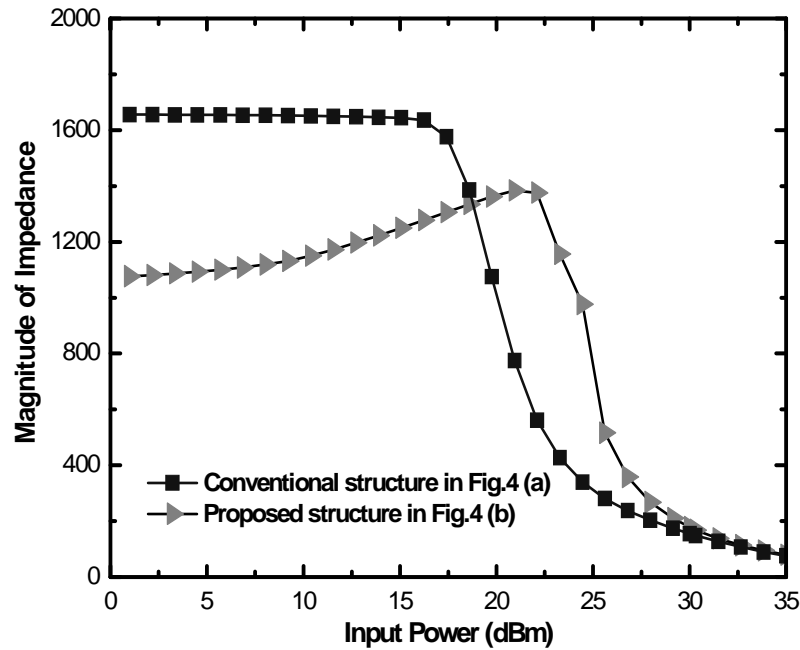


Fig. 4.14. Impedance variation of conventional multi-stack FETs and proposed multi-stack FETs according to the input power level.

As described in Equations (1) and (2) in chapter 3.3, the total impedance of the conventional structure at small signal input is higher than that of the proposed structure due to large capacitance in the small signal input. However, the transition of the impedance occurs as the input power increases.

Fig. 4.15 shows the equivalent circuit model of the proposed three-stacked switch devices in OFF state.

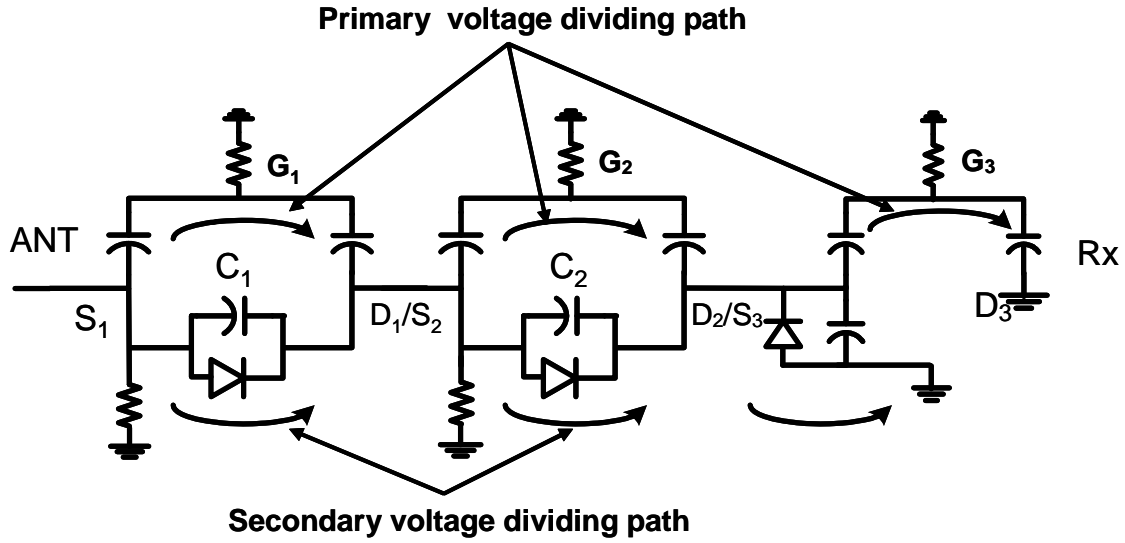


Fig. 4.15. Equivalent circuit model of the proposed multi-stack FETs using the adaptive voltage swing distribution in Fig. 4.13 (b).

In the event of a large voltage swing, the voltage dividing behavior during the positive cycle is totally different from that during negative voltage swing. The voltage swing waveforms between each device in the SPDT configuration are shown in Fig. 4.16. In the case of positive voltage swing, V_{S1D1} and V_{S2D2} , as shown in Fig. 4.16, are fixed by the junction diode turn-on voltage. However, in the negative voltage swing case, the voltage splitting between V_{S1D1} and V_{S2D2} is determined by both the ratio of junction capacitor C_1 to C_2 and the impedance of the last device in OFF state[39].

The method of preventing channel formation in the proposed structure is described in [39]. Basically, the channel is not created in OFF state FET if either the source voltage is higher than the gate voltage or the voltage difference between the gate and the source is smaller than the threshold voltage of the device.

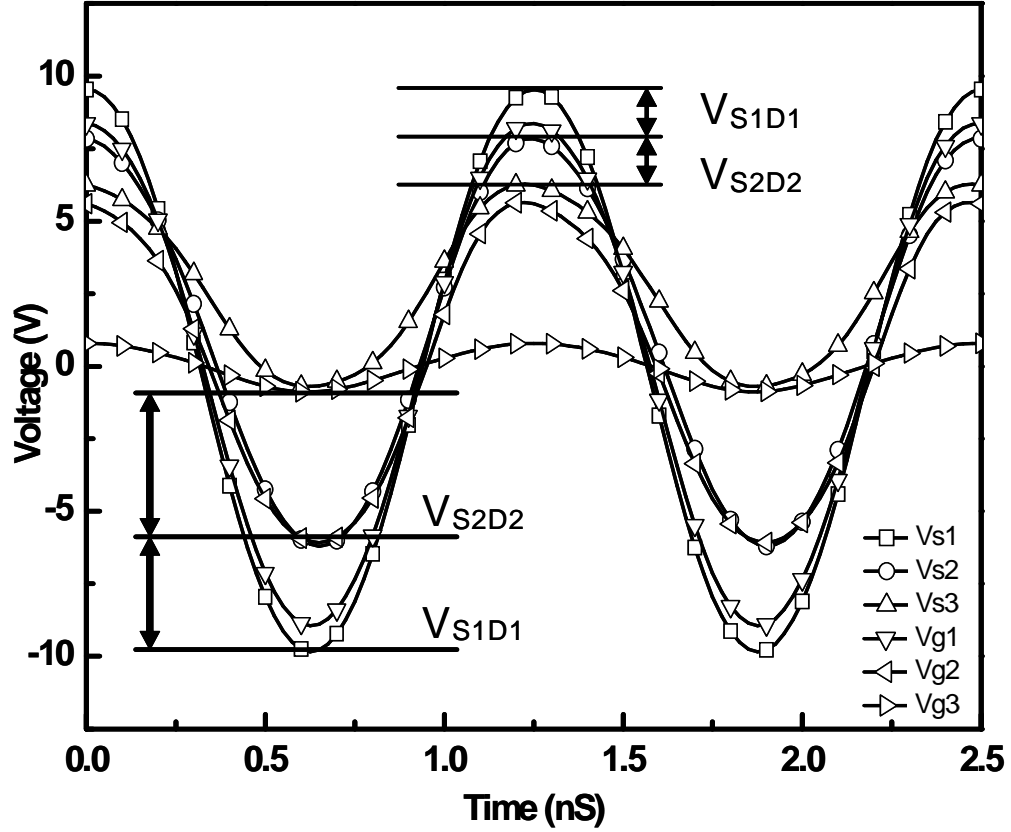


Fig. 4.16. Simulation of adaptive voltage swing of the proposed multi-stack structure in a SPDT switch.(30 dBm input power).

Fig. 4.17 shows the voltage difference between either the source or the drain and the gate at each device. In Fig. 4.17, dashed lines demonstrate voltage difference between the source and the gate while the Fig. 4.15 solid lines indicate the voltage difference between the drain and the gate as shown in. The former explains channel formation in the case of the negative cycle of voltage swing. In the same manner, the latter show channel formation in case of the positive cycle of the voltage swing. As can be seen in Fig. 4.17, neither of the voltage difference in dashed line and solid line becomes higher than threshold voltage of the CMOS FET.

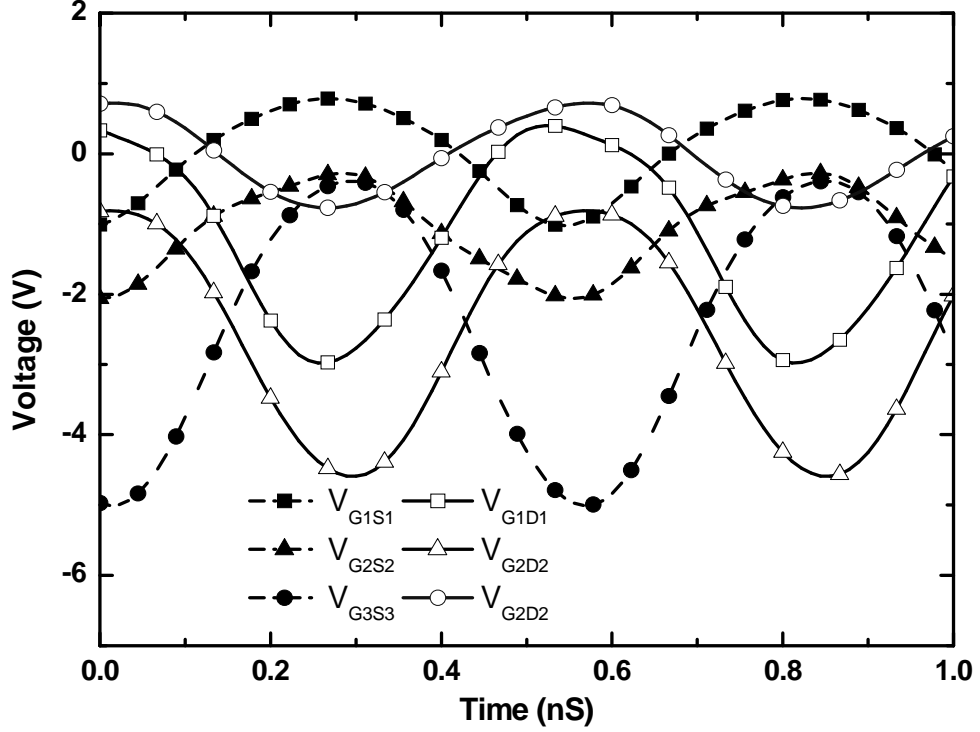


Fig. 4.17. Simulation of VGS and VGD at each node in the equivalent circuit model shown in Fig.7 (30 dBm input power).

Experimental data comparing performance between the conventional and the proposed structures have been reported in the prior works [39, 40]. Isolation performance with respect to the input power level demonstrates that the proposed structure helps to prevent unwanted channel formation in large signal input so that the isolation level from the proposed structure is lower than in that of the conventional structure. The measurement results in [39] indeed reveal a good agreement with simulation results as shown in Fig. 4.14, where the impedance variation between the two structures is compared with respect to the input power level.

4.3.2. SPDT Switch Using A Novel Adaptive Voltage Distribution Method In the Multi-Stack FETs

SPDT CMOS switches using a novel adaptive voltage swing distribution method in multi-stack FETs are implemented. In order to further increase power handling capability of the switch, four NMOS devices are series connected to form a multi-stack FET scheme in Rx switches, as shown in Fig. 4.18.

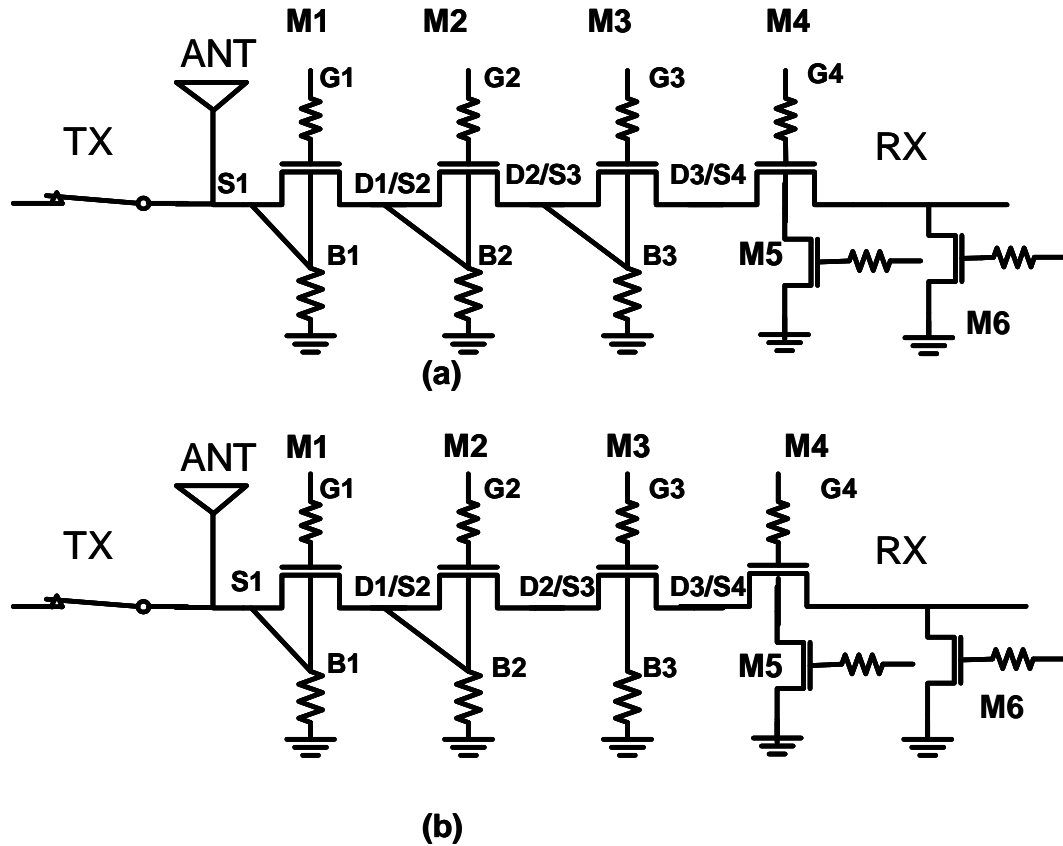


Fig. 4.18. Two different kinds of four stacked SPDT switch configurations using the adaptive voltage swing distribution method. (a) Type A, and (b) Type B. (Size of the device: Tx FET W/L:1.5mm/0.35 μ m, Rx FET:700 μ m/0.35 μ m. Resistors: 10K ohm).

Tx switches are also implemented using four multi-stack devices to increase the isolation of Tx switches from Rx switches in receive mode. All of the switch devices in the multi-stack FET utilize thick gate-oxide devices with 0.35- μ m gate length. This

causes higher insertion loss in ON-state. However, it is inevitable to choose them in the high power CMOS switch implementation because the thick gate oxide device has a gate oxide breakdown voltage of around 6.8V while a thin gate oxide device has 4.2V. In the layout, all of the switch devices in the multi-stack FET scheme need to be fabricated inside individual deep N-wells. The deep N-well structure ensures total isolation of each p-substrate of the NMOS switch device, in which the voltage potential varies with the voltage dividing mechanism of the multi-stack structure.

Two different kinds of SPDT switches, type-A and type-B, are fabricated, as shown in Fig. 4.18(a) and Fig. 4.18(b). Basically, the Rx switches follow a similar structure as the proposed switch in the previous section. One difference between the two switches is the existence of the connection of source and bulk in the device at M3 in the Rx switch. The structure shown in Fig. 4.18(a) follows the method proposed in the previous section so that M1, M2, and M3 have source and bulk connection while M3 in Fig. 4.18(b) does not have source-bulk connection. Fig. 4.19 and Fig. 4.20 show voltage swing waveforms at each source port of the type-A switch and type-B switch, respectively. Voltage swing behavior of the type-A switch follows exactly in the same fashion as the proposed switch in Fig. 4.13 (b). The upper voltage swing difference in the positive cycle is determined by the turn-on voltage of the junction diode, which is forward biased due to voltage differences between each source port. Meanwhile, the negative voltage swing distribution between each source port is determined by the parasitic junction capacitor. Therefore, the overall voltage swings are shifted up and no channel of the OFF-state device can be formed because voltage difference between either

a source or a drain and a gate always stays under the threshold voltage of the switch device.

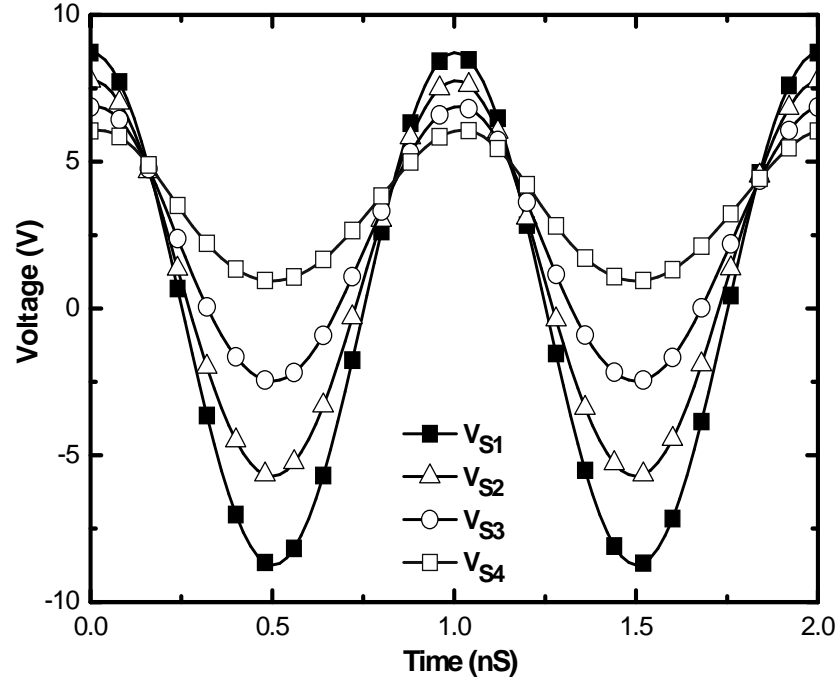


Fig. 4.19. Voltage swing simulation of the structure of type-A in Fig. 10 (a) (30 dBm input power).

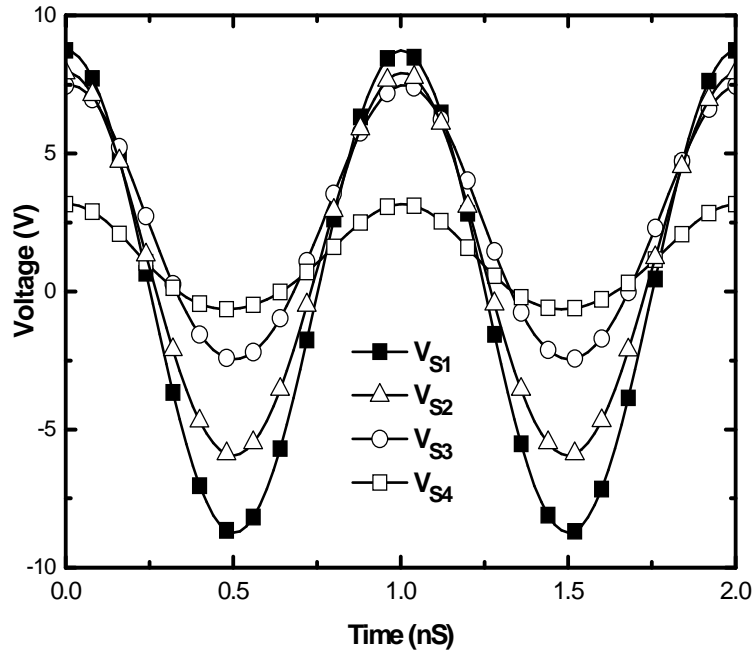


Fig. 4.20. Voltage swing simulation of the structure of type-B in Fig. 10 (b) (30 dBm input power).

The voltage swing in Fig. 4.20 follows in a similar fashion as that of Fig. 4.19, except that V_{S4} in Fig. 4.20 does not follow the same trend as explained above. Instead, V_{S4} in Fig. 4.20 is decided by impedance of the OFF-state device which has an equivalent circuit shown in Fig. 4.15 (a). As a result, positive voltage peak of the V_{S4} in Fig. 4.20 is unbound by the turn-on voltage of the parasitic junction diode. Even in this case, undesirable channel formation of the switch device in OFF state does not occur because V_{G4S4} at M4 still remains under the threshold voltage of the switch device. However, type-A and type-B show significant difference in terms of power handling capability. In order to clarify this issue, Fig. 4.21 shows V_{G4S4} at M4 both in type-A and type-B.

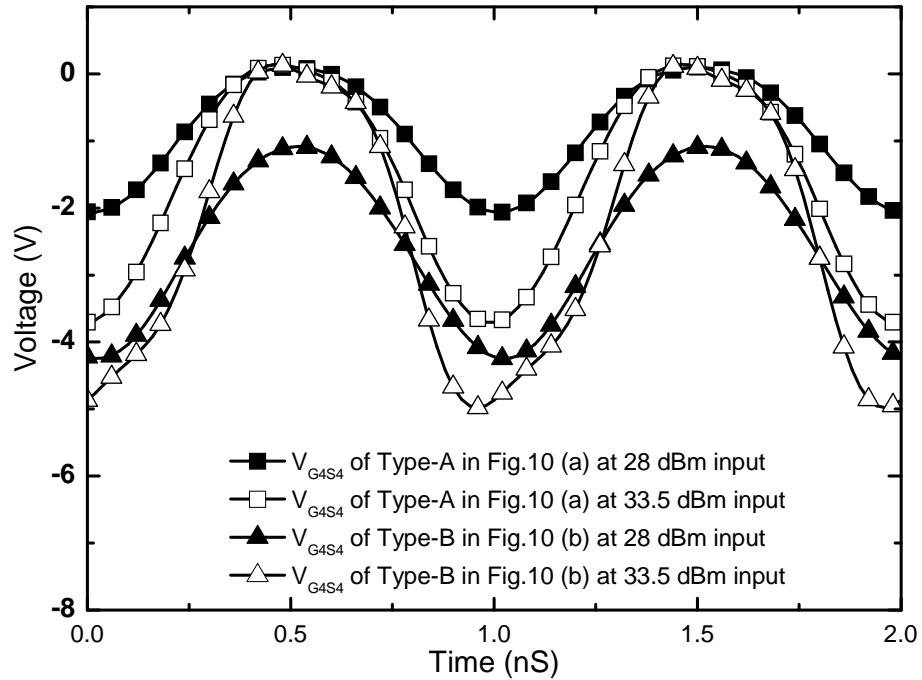


Fig. 4.21. Voltage difference simulation between gate and source at M4 in type-A and type-B in Fig.10 (28 dBm and 33.5 dBm input power level).

As noticed in Fig. 4.19 and Fig. 4.20, the behavior of V_{S4} in type-A and type-B are different from each other. This, in turn, results in different behavior of V_{G4S4} shown in Fig. 4.21. The adaptive voltage swing distribution method is very effective with respect

to preventing channel formation in OFF-state FETs. Nevertheless, the voltage shift-up in a source port results in more voltage stress in the last device in multi-stack FETs. Once the voltage difference between the source and the gate in the last device reaches the gate oxide breakdown voltage, degradation of the power handling capability begins. In other words, if all the stacked devices have source-bulk connections as shown in Fig. 4.18(a), the last device will take all the voltage stress burdens descended from the first three devices. The structure in type-B can resolve this breakdown problem without compromising the prevention of a leakage channel formation in OFF-state device. As the number of devices used in multi-stacked FETs increases, the high power CMOS switch incorporating the proposed methods of channel formation prevention needs to combine conventional voltage distribution methods in conjunction with the novel method of adaptive voltage distribution proposed in this paper. Another advantage of the proposed method is that the first device in RX switch devices is less voltage-stressed by the voltage dividing mechanism than in the conventional multi-stack FETs, where the first device in multi-stack FETs can usually see the highest voltage swing at the antenna port.

It is notable that all the distortion of linearity and degradation of power handling capability are generally limited by the breakdown voltage of the device. Nevertheless, the time variant signal's reaching into the breakdown region of the device does not result in total destruction of the device.

4.3.3. Experimental Results

SPDT switches using adaptive voltage swing distribution methods are fabricated and fully characterized. Fig. 4.22(a) and (b) show microphotographs of the type-A

structure and type-B structure as shown in Fig. 4.18(a) and (b), respectively. The effective die area of the fabricated SPDT switch is 0.16 mm^2 and the overall size of the chip including pads is 0.4 mm^2 in both chips for the type-A and the type-B.

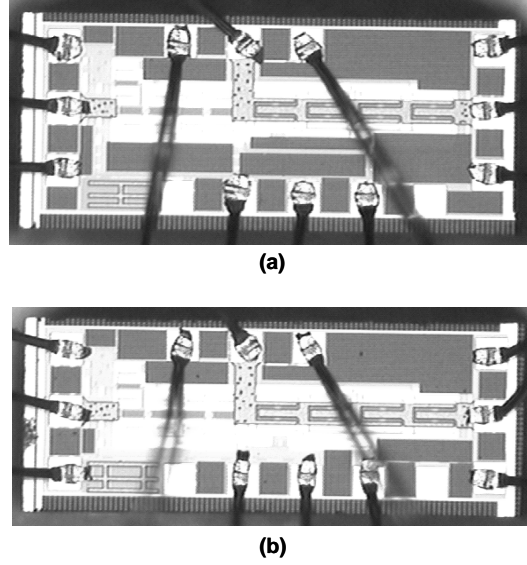


Fig. 4.22. Micro-photograph of the fabricated SPDT switches (a) type-A in Fig. 10 (a) and (b) type-B in Fig. 10 (b). (size of the switches : $1000 \text{ um} \times 400 \text{ um}$)

Please note that the size and the facade of the both chips look identical because the only difference structure is the bulk source connection in one of the multi-stack structures in the Rx switch. In order to supply a high-power RF signal to the fabricated switches, both chips are assembled and characterized on chip-on-board (COB) configuration. All of the control voltages were directly supplied from external DC power supplies.

4.3.3.1 Power-Handling Capability in the Series-Shunt Configuration

The power-handling capability of the type-A structure and the type-B structure is measured and compared with the series-shunt configuration to verify the power-handling capability of the Rx switch itself. In this configuration, the input power is directly applied

to the antenna port so that the test structures can receive the pure single tone of the input signal without any degraded signals from the insertion loss of Tx switches and without any distortion signals such as the second and third harmonics. Fig. 4.23 shows the input power compression point of the type-A and type-B structure.

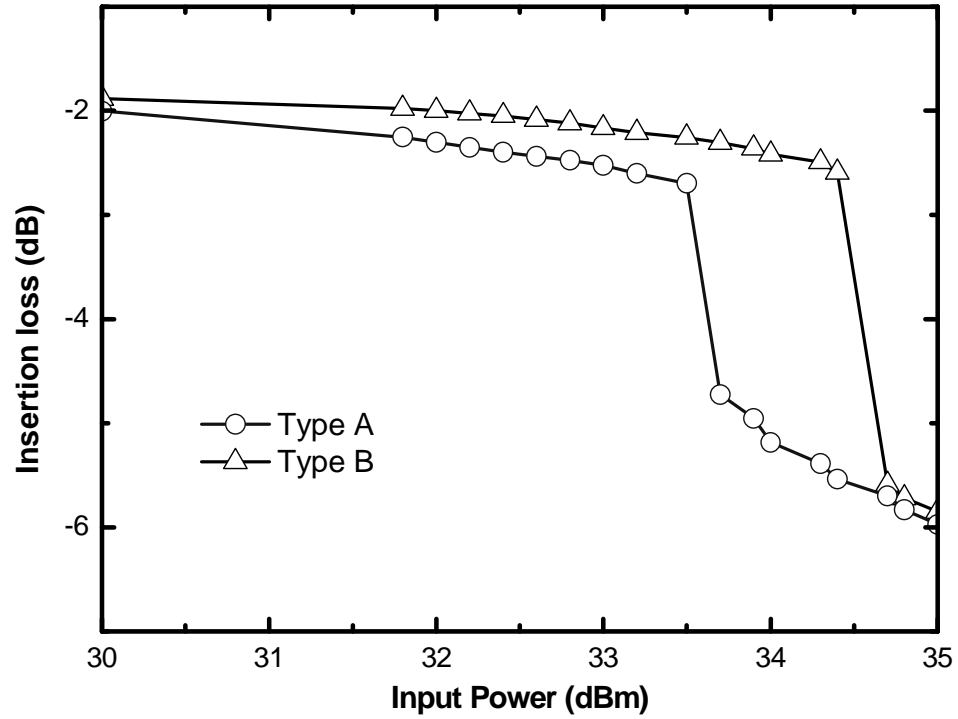


Fig. 4.23. Measured power handling capability of the Rx switches(OFF state) using series-shunt configuration at 1.9 GHz.(ANT-input port, Tx-output port(series ON) and Rx-grounded(shunt-OFF state))

As expected, the type-B structure has a higher input power compression point than the type-A structure due to the breakdown immunity. The input power compression point graph of the type-B structure demonstrates an unprecedented power handling capability of the CMOS switch. Because there is no degradation of insertion loss, the input power level in the graph can indicate the power handling capability of the proposed type-A and type-B structure itself.

4.3.3.2 S-parameter Measurement

Fig. 4.24 shows measured S-parameters of the Tx switches. Even though the four devices are stacked, the insertion loss of the switches reveals decent performances of 1.2 dB at 900 MHz and 1.5 dB loss at 1.9 GHz after de-embedding COB loss.

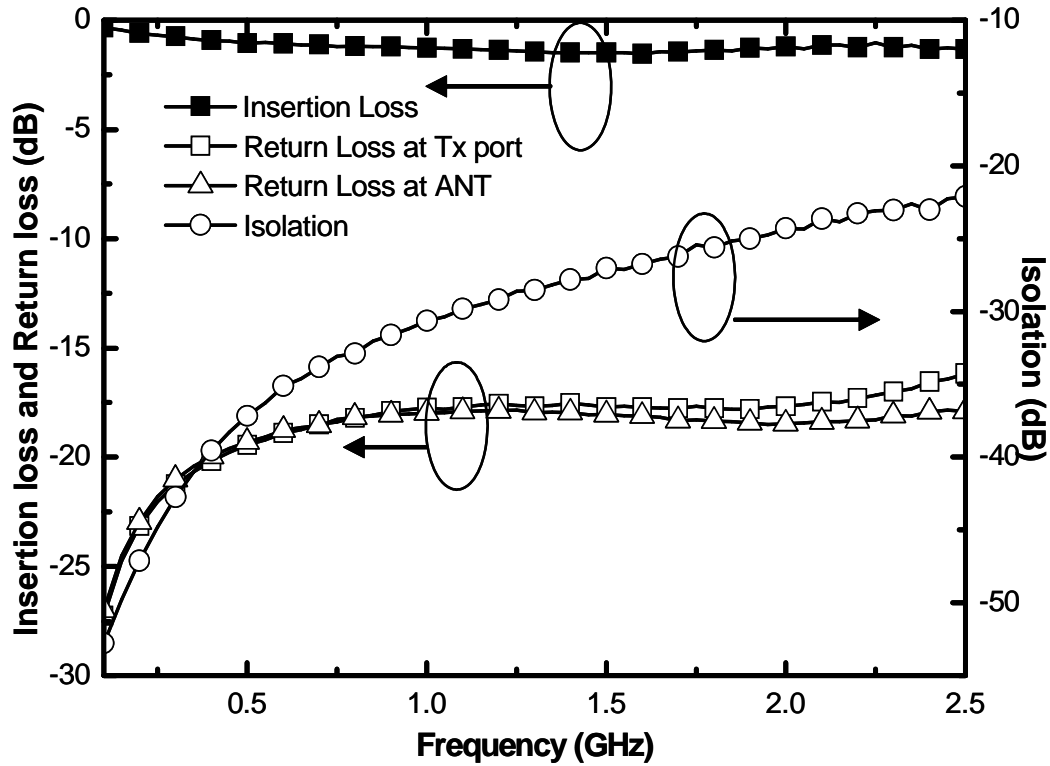


Fig. 4.24. Measured S-parameters of Tx switch.

The return loss of the Tx switch is -17 dB at the Tx port and -19 dB at the antenna port. The return loss can be improved by manipulating the length of the wire bond to provide better impedance matching. Once the return loss can be improved up to -20 dB, mismatch loss can be improved by 0.1 dB. Without any shunt devices in the Tx switches, the isolation shows decent performance such as -22 dB at 1.9 GHz because of the sufficient number of stacked FETs. In a small-signal operation in switch, isolation and insertion loss are always in a trade-off relationship because of the parasitic capacitors.

Fig. 4.25 shows the measured S-parameters of the Rx switches. All of the S-parameters are also measured in COB. The insertion loss of the Rx switches is measured as 1.5 dB at 900 MHz and 1.9 dB at 1.9 GHz, respectively, after de-embedding COB loss.

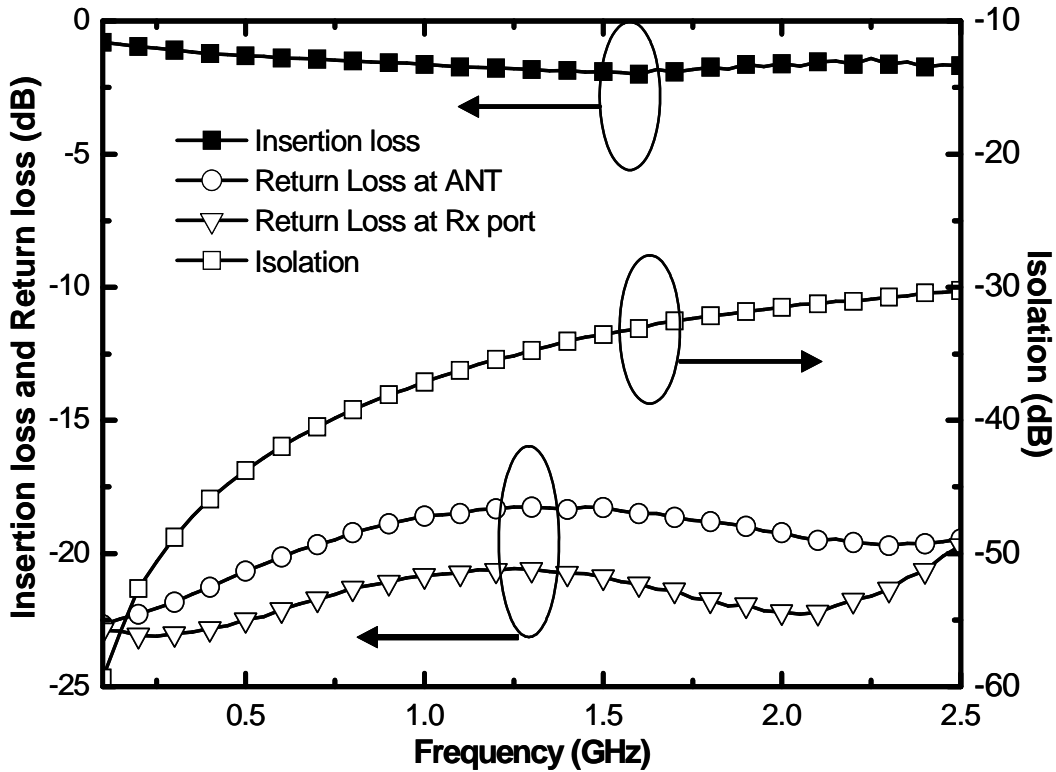


Fig. 4.25. Measured S-parameters of Rx switch.

Because the device size in the Rx switches is smaller than that of the Tx switches, it is natural for the Rx switches to have a higher insertion loss. Also the better isolation performance can be expected from the Rx switches because of its smaller size than the Tx switch. The return loss of the Rx switch shows -20 dB at the antenna port and -22 dB at the Rx port, respectively. This results from the OFF state capacitance difference between the Tx switch and Rx switch. Basically, there is no notable difference between the type-A structure and type-B structure in terms of small signal performance. Therefore, the measured S-parameters of the type-B structure are reported.

4.3.3.3 Measured 0.3 dB Compression Point

Normally, most of the previous CMOS switch works tend to report P1dB as standard power handling capability of the device; however, we would like to report a 0.3dB compression point as a criterion of power handling capability of the device. This is not only because a 0.3dB compression point is more practical in an industrial point of view, but also because P1dB is less meaningful in the event of a sudden drop in the power compression point before the compression reaches 1dB point. **Fig. 4.26** shows the measured 0.3 dB compression point of the type A-structure and the type-B structure.

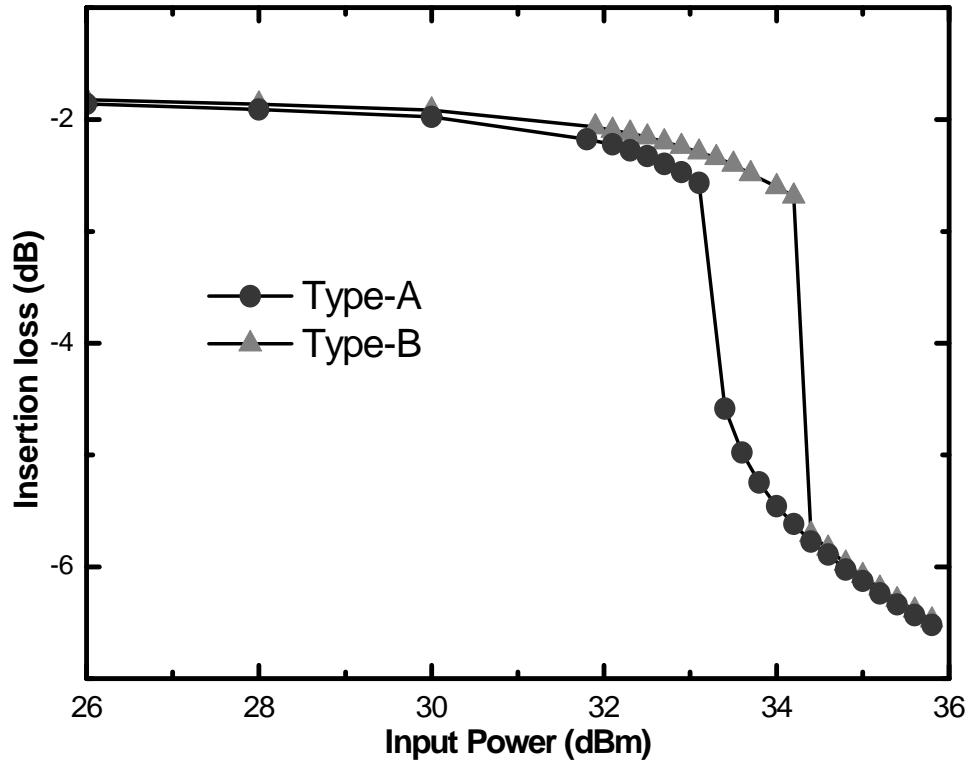


Fig. 4.26. Measured 0.3 dB compression point of the type-A and type-B structure in an SPDT configuration at 1.9 GHz.

According to the experimental data, 33.5 dBm of input power can be observed as input 0.3dB compression point of the type-B structure, which is 1.5 dB higher than that of

the type-A structure. Input power handling capability of higher than 2W in the CMOS switch in a standard 0.18- μm CMOS process is the best performance ever reported.

Compared to the input power compression point shown in the series-shunt configuration shown in Fig. 4.23, the SPDT switch configuration has a relatively low compression point. Considering the insertion loss of the Tx switch and 0.3 dB degradation due to the compression point, the actual power delivered at the antenna port is said to be around 31.5dBm. As explained earlier, the nature of input power between the series-shunt configuration and the SPDT configuration is different in that the former received only the fundamental signal while the latter might have high harmonic level in addition to the fundamental signal. This issue needs to be specially considered when the CMOS power amplifier is integrated in the same substrate as the CMOS switch.

4.3.3.4 Second and Third Harmonics

Fig. 4.27 shows the second and third harmonic performance of the type-A and the type-B structure at 1.9 GHz operation. Experimental harmonics data are collected from the spectrum analyzer by connecting the 20-dB coupler directly to the antenna port of the switch and then using the high pass filter to filter out fundamental frequencies to minimize spurious signals in the spectrum analyzer.

As shown in Fig. 4.27, the second harmonic and third harmonic have -46 dBc and -60 dBc at 33 dBm input. The second and third harmonic performances demonstrate a sudden transition point where the 0.3dB compression points show a rapid drop as well. The sudden transition point in the harmonic performance of the type-B structure is observed in higher input power than that of the type-A structure.

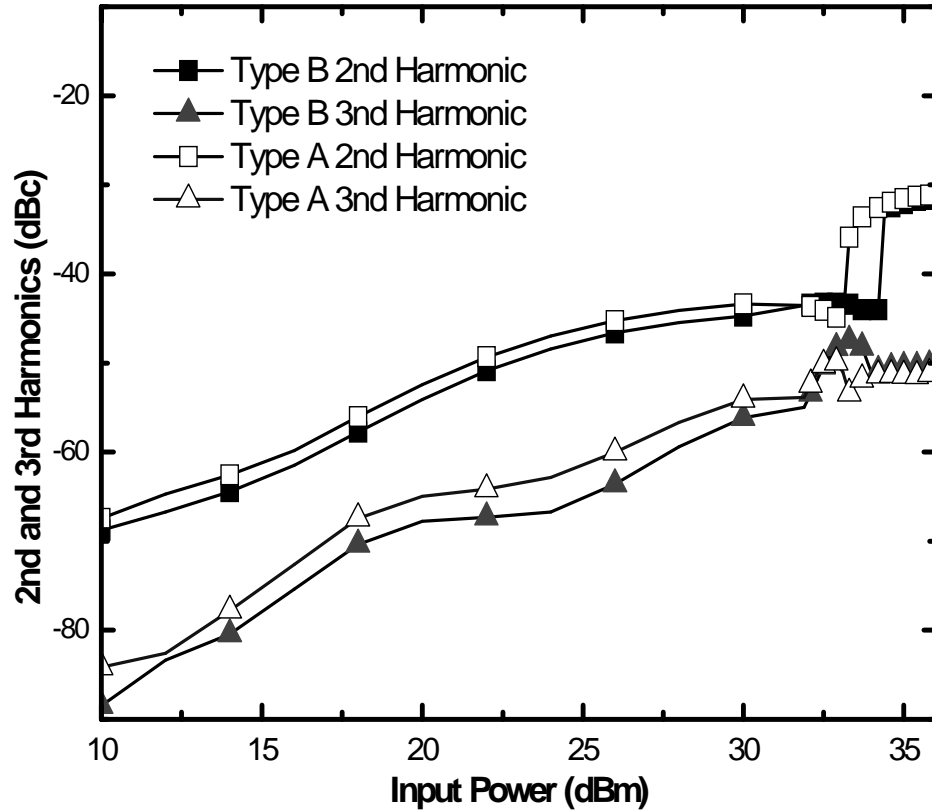


Fig. 4.27. Measured the second and third harmonics of the type-A structure, and the type-B structure, respectively, at 1.9GHz.

4.3.4. Summary

A high power CMOS switch using a novel adaptive voltage swing distribution method in a multi stack FET scheme has been developed. The biggest obstacle to implement high power switches in the multi-stack FET scheme with low control voltage, such as 3.3V/0V is the undesirable channel formation of the device in OFF-state when a large signal voltage swing is applied. The novel adaptive voltage swing distribution method is proposed as a solution for leakage channel formation prevention. This method does not require external components such as feed forward capacitors or DC/DC converters to boost up bias voltage at the drain/source port. This novel method utilizes substrate junction diodes to prevent channel from being formed in OFF-state devices.

Two different types of SPDT CMOS switches employing this novel method in four NMOS multi-stack FET schemes are designed, implemented, and fully characterized to demonstrate the outstanding performance of the proposed CMOS switch. In order to address the reliability issue regarding voltage stress on a particular device in multi stack FETs, one of the fabricated switches follows the exact same fashion as the proposed one in [14], while the other has a combination of a conventional structure and the proposed structure. The latter structure can show better performance of relieving voltage stress in one of the multi-stack FETs. The four multi-stack FETs employing the novel adaptive voltage swing distribution method shows an input 0.3dB compression power handling capability of 34.2 dBm for a series-shunt configuration and 33.5 dBm for an SPDT configuration at 1.9 GHz operation. These are the highest power-handling capability of a CMOS switch using a standard CMOS process ever reported. The size of the fabricated switch is 0.16 mm^2 . The S-parameter measured results reveal good return loss at both the antenna port and Tx/Rx port. The insertion loss is 1.5 dB at the Tx switch and 1.9 dB at the Rx switch. This amount of the value of the insertion loss is a nature of multi-stack FET schemes. From the experimental data, we conclude that the novel adaptive voltage swing distribution method can be a promising candidate for the implementation of watt-level high power switches in a standard CMOS process.

4.4. Layout Consideration of the CMOS switch in the Multi-Stack Structure

The adaptive voltage swing distribution method was introduced as a novel method to improve power-handling capability of the CMOS switch using the multi-stack structure in the previous section.

The main idea of the method is to inhibit the channel formation of the OFF-state device by distributing the voltage swing level at the antenna port toward the each device unequally. The voltage swing at the antenna port is distributed primarily by the parasitic capacitors between the source-gate-drain as well as secondarily by the junction capacitors and the junction diodes. The measurement data in the section 4.3.3.3 verifies the effectiveness of the proposed method. However, the sudden drop point at Fig. 4.26 cannot be explained very well using the equivalent circuit model presented in Fig. 4.15.

In this section, the layout consideration of the CMOS switch is discussed when the switch is designed using the multi-stack structure with the body-floating technique.

4.4.1. Equivalent Circuit Model considering the Substrate Junction Diodes

Basically, BSIM3 models, which is provided by the TSMC, do not include the substrate the substrate junction diode and parasitic junction capacitors between the deep N-well and the p-substrate. It is not necessary that the model has to have all the parasitic parameters between the p-substrate and the N-well. The primary purpose of the deep N-well in the triple well CMOS process is to provide the high isolation between the devices. Employing this structure can improve the noise performance of the circuits and reduce the interference between the devices.

Fig. 4.28 demonstrate the cross sectional view of the NMOS device and the equivalent circuit model considering the substrate junction diode and capacitors.

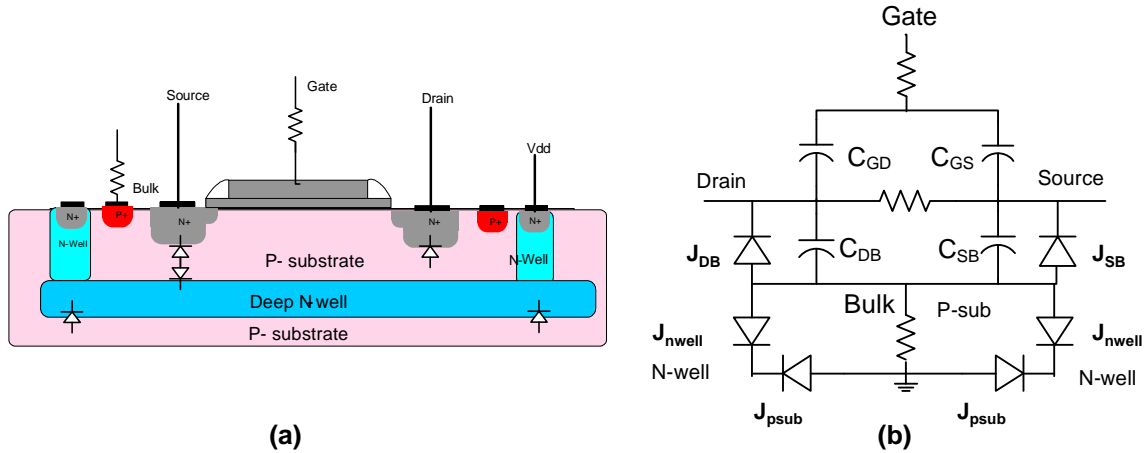


Fig. 4.28. (a) the cross sectional view of the NMOS device and (b) equivalent circuit model of the NMOS device considering the substrate junction diodes and capacitors.

When the triple well CMOS process is used in designing the circuits which have a common-source configuration, n+ contacts at the N-well go to the VDD and the p+ contacts at the substrate are bound to the ground. Therefore all the substrate junction diodes are disabled.

All the switch designs in the previous sections employ this configuration. However, special care need to be taken when the high-power CMOS switch is implemented using the multi-stack structure.

Fig. 4.29 demonstrates the equivalent circuit model of the structure in Fig. 4.18(b) in OFF state, considering the substrate junction diodes. Differently from the previous one in Fig. 4.15 , this equivalent model considers the substrate junction diodes such as J_{nwell} and J_{p-sub}.in Fig. 4.28(b). When a large signal voltage is applied to the OFF-state multi-stack FETs with the adaptive voltage swing distribution methods, voltage swing is divided at each port of the each device. If the N-well port from all the devices is directly connected to the VDD, serious voltage distortion can happen in the OFF-state device.

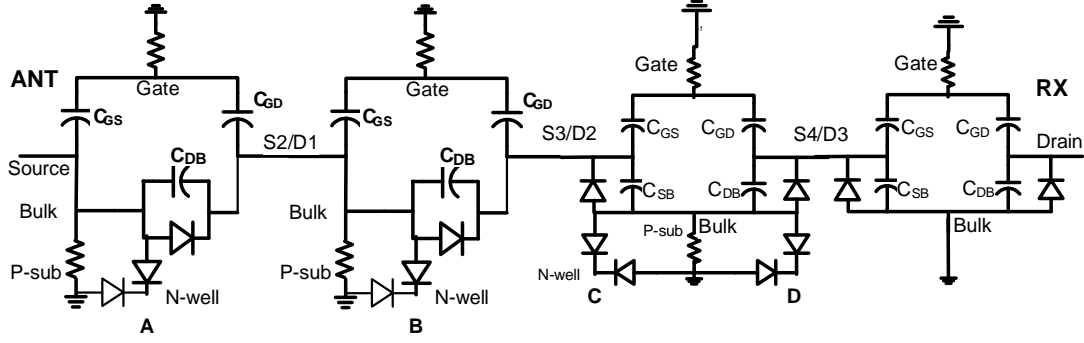


Fig. 4.29. Equivalent-circuit model of the four-stacked CMOS switch in Fig. 4.18 (b) with consideration of the substrate-junction diodes.

As you can see, the voltage swing level between the point A and point B in Fig. 4.29 should be different from each other, as overall voltage swing at antenna port is distributed toward each device according to the impedance of the each device in OFF state. Voltage swing level of the point A is higher than that of the point B, and Voltage swing level B is higher than that of the point C, and so on. Voltage swing level at point A can distort the voltage swing level at point B if point A and point B are combined together. For example, when the voltage level at each source of the device at Fig. 4.29 is determined by the voltage-dividing mechanism, the voltage levels at the point B, C and D have the same voltage as the point A. Therefore, there is an opportunity that the voltage of the point B can be much higher than that of the source port S2 in Fig. 4.29. This can contribute the degradation of the linearity of the CMOS switch by breaking the principle of the voltage swing distribution. For this reason, N-well port in each device in the Rx switches should have its own high value resistor connected before it is combined at VDD port. This can provide better isolation performance of one device from another device and guarantee the operation of the N-well diodes and p-sub diodes at each device to stay in safe region by supporting the N-well and the p-substrate floating.

Fig. 4.30 presents the equivalent circuit model of the four-stacked switch implemented in the CMOS process using the triple-well process. Fig. 4.31 shows the layout of the CMOS switch employing the individual bias resistor at the each N-well of the device

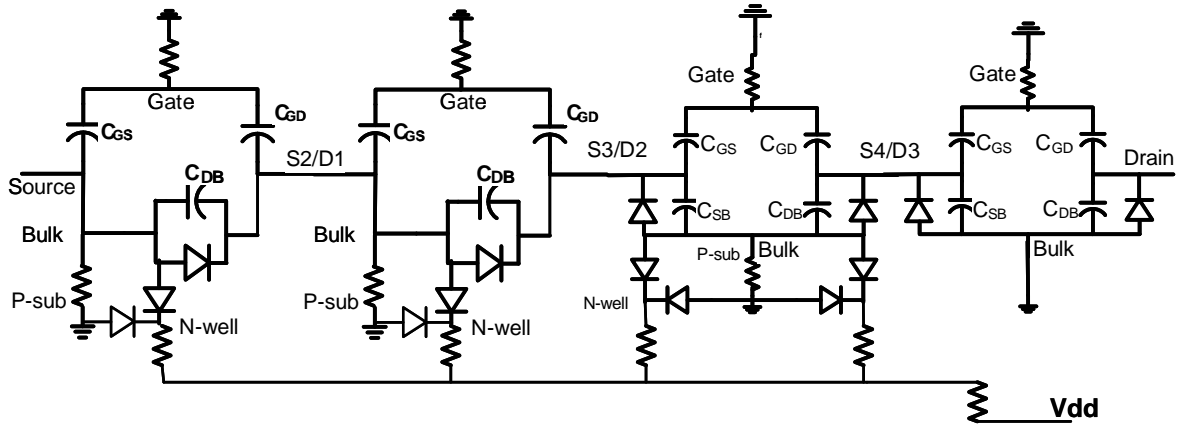


Fig. 4.30. Proposed equivalent-circuit model of the four-stacked CMOS switch.

As is well-known, the schematic model of the NMOS device in the deep N-well provided by the foundry service is a four port device which consists of source, drain, gate and bulk. Therefore, the circuit simulation does not explain all the effects caused by the substrate junction capacitor and junction diodes. When it comes to the large-signal operation, it gets worse. This could be one of the reasons for the degraded power-handling capability of the device, compared to the simulation results.

Also, the switch designed using the model of the four port device cannot explain the harmonic performance of the CMOS switch, because the substrate junction diode can be a dominant source to generate harmonics as the power of the supply signal is getting high.

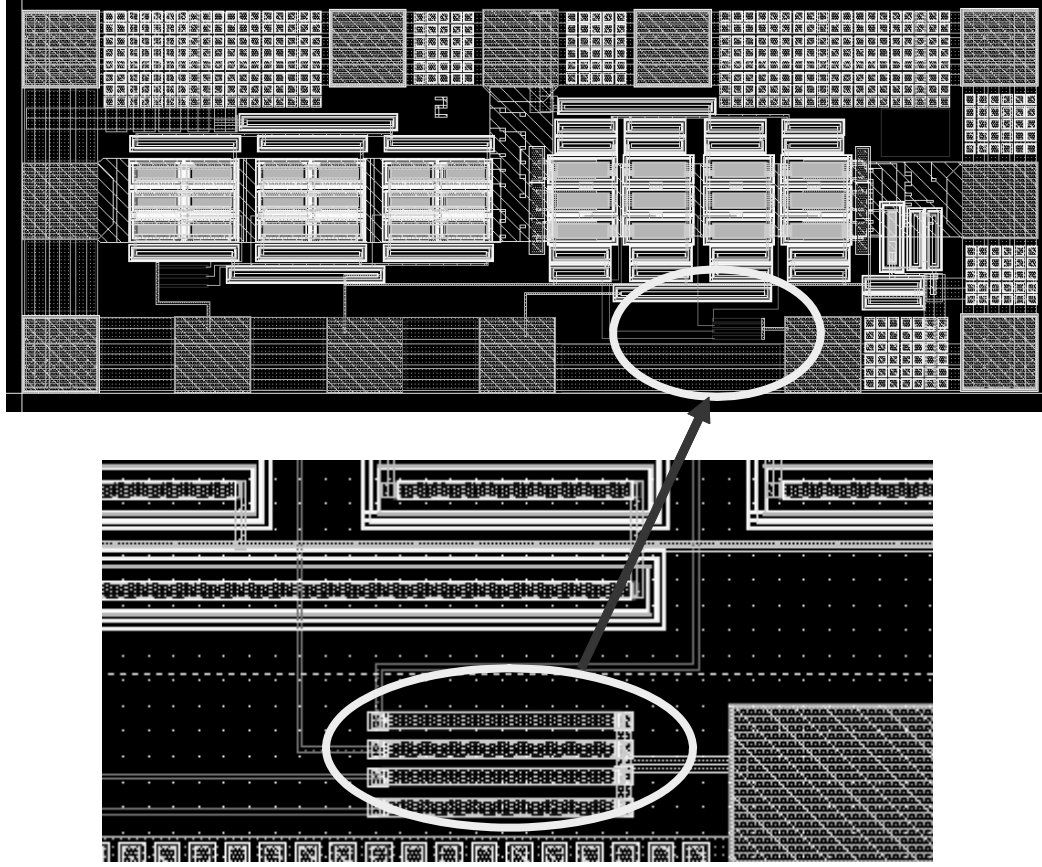


Fig. 4.31. Layout of the CMOS switch employing the individual bias resistor at the each N-well of the device

4.4.2. Measurement Results

A SPDT switch using the adaptive voltage swing distribution method was designed and tested. As shown Fig. 4.31, the N-well body of the each switch device in the multi-stack structure is connected to an individual resistor to ensure the isolated voltage swing at the bulk port of the switch device. Also, the N-well body resistors at the Rx switch need to be separated from those at the Tx switches to provide isolation between the Tx substrate and the Rx substrate. Fig. 4.32. demonstrates the power-handling capability of the SPDT switch fabricated considering the N-well body isolation.

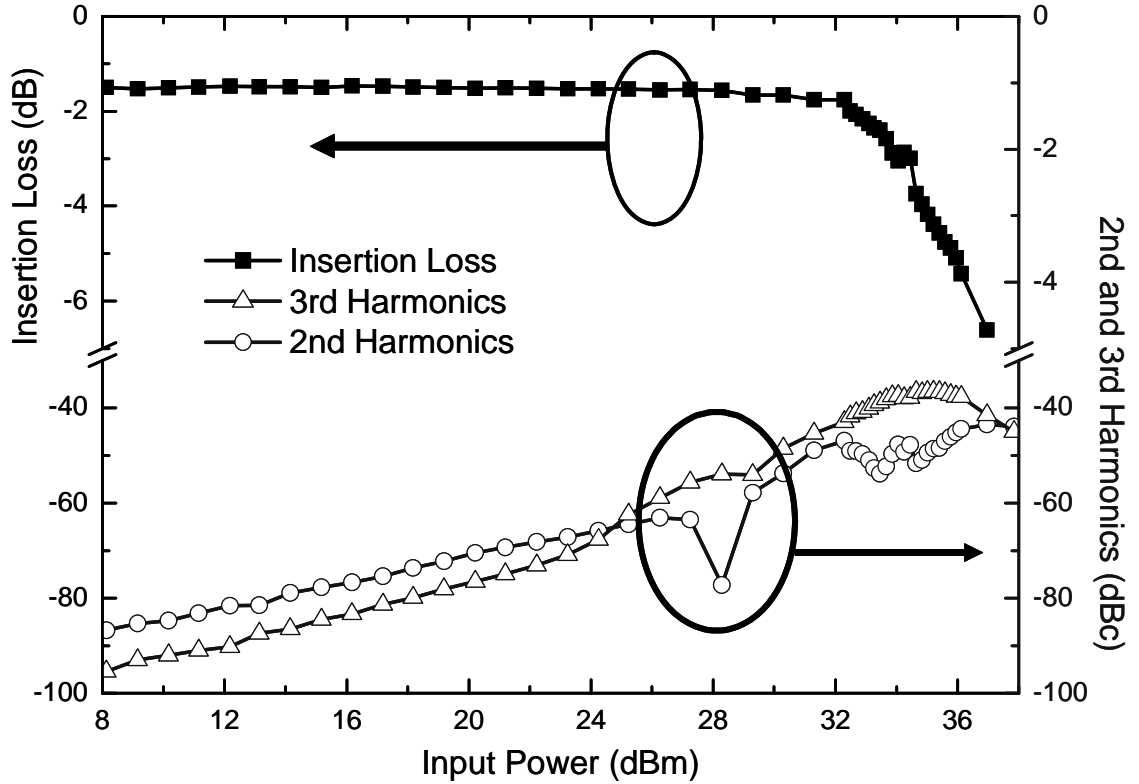


Fig. 4.32. 1 dB compression point and the second and the third harmonics.

As can be seen in Fig. 4.32, the power-saturation point of the switch is depressed in a different fashion from that of the switch in Fig. 4.26. The most important difference between Fig. 4.26 and Fig. 4.32 is that there is no sudden drop point at the 1 dB compression point at Fig. 4.32. This result matches the theory regarding the voltage swing at the N-well body port of the each device. Also, the power-handling capability slightly improves in the new design. Also, the harmonic performance of the CMOS switch with consideration of the voltage swing at the N-well presents the enhancement at the low input power. The third harmonics remains under the -70 dBc until the input power reaches 1 watt. However, as the input power level approaches the saturation point of the switch, the harmonic performance becomes higher.

The harmonic performance is explained using the relationship between the voltage swing in the OFF-state device and the breakdown voltage of the switch device. As the voltage swing reaches the breakdown voltage of the device, the distortion at the voltage swing is caused so that generating the harmonics is initiated. This is a general theory regarding the generation of the harmonics in the case of GaAs switches. However, in the case of the CMOS switch design, the substrate junction diodes can work as another source of the harmonic generation. Only four port-device models are available in the circuit simulation. Hence this kind of the result regarding the harmonic performance cannot be observed in the circuit simulation. Designing a new circuit model which can cover all the substrate effect in the case of a large-signal operation could remain as a future work.

4.5. High Power Switch Design using Feed-Forward Capacitor

In this section, design of high power CMOS switch using method of the Feed Forward capacitor is introduced in association with the body-floating technique.

The method of the feed-forward capacitor is well known method in designing the high power GaAs switch, where the control voltage is very low. This method does not require the external circuitry such as DC/DC converters to provide high power-handling capability. Since one of the requirements of the recent commercial products is low supply voltage, the feed forward capacitor method is getting popular.

The feed-forward capacitor method is applied to the high power CMOS switch design. SPDT switches using different sizes of the capacitors to apply the feed forward method were designed and tested.

This section starts with the explanation of the feed-forward capacitor method. The maximum power-handling capability of the feed-forward capacitor method is discussed with respect to the threshold voltage and the breakdown voltage of the device. The measurement data present the variation of the power-handling capability of the CMOS switch using the feed-forward method according to capacitor values.

4.5.1. Feed Forward Capacitor Method

The linearity of the switch is decided by current limit, voltage limit and breakdown voltage limit of the device. When the control voltage of the switch becomes as low as 3 V, the voltage limit is the biggest contributor. As the voltage swing at the antenna port reaches the voltage level higher than the control voltage, the voltage

difference between the negative voltage peak and the control voltage becomes higher than the threshold voltage of the device so that the device in OFF state turns on.

Fig. 4.33 shows the principle of the channel formation of the OFF state device according to the voltage swing supplied.

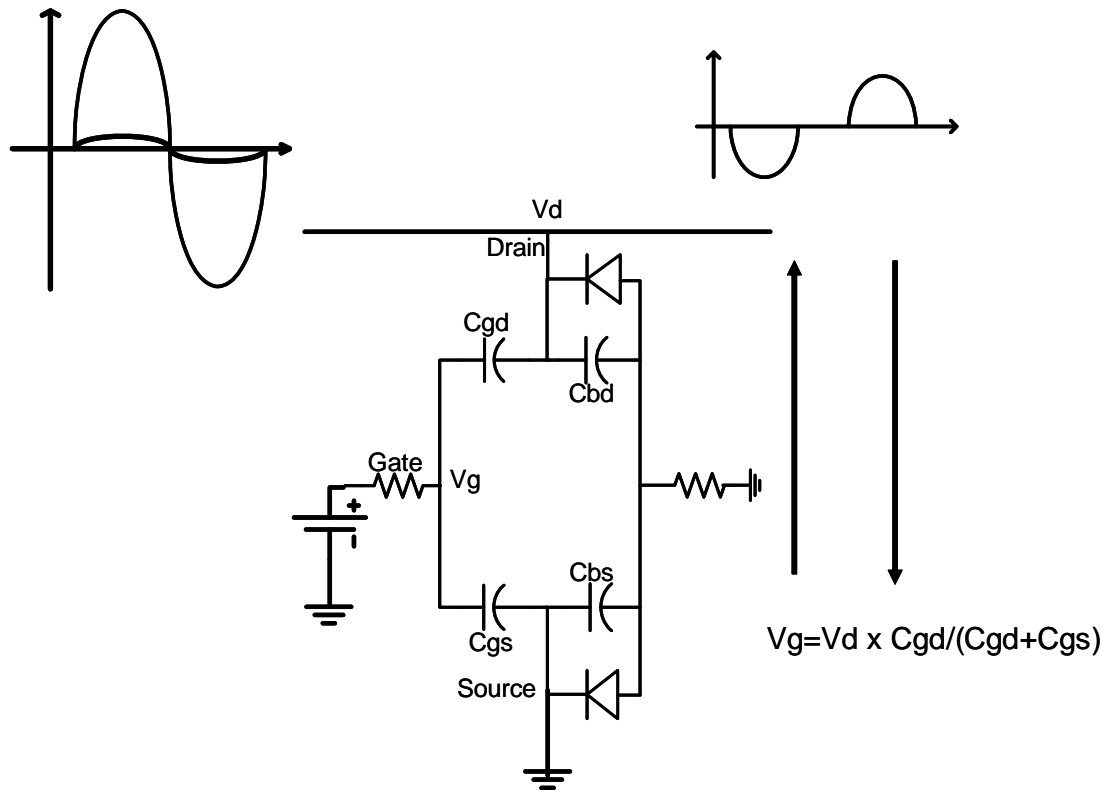


Fig. 4.33. Channel formation of the OFF-state device

Voltage swing at the drain port is divided by the ratio of the C_{gd} and C_{gs} . Since the values of the C_{gd} and C_{gs} are equal, V_{dg} and V_{gs} are equally distributed. In case of the positive cycle of the device, the V_g is higher than the V_s . The voltage difference at V_{gs} becomes the threshold voltage of the device so that current of the device starts to flow from drain to source, as the voltage swing level increases. In case of the negative cycle of the voltage swing, V_g can be higher than V_d so that the current can flow from the source to the drain. The feed-forward capacitor is an external capacitor added between gate and

source/drain to prevent leakage current from flowing. Adding the external capacitor between the drain and the gate, the voltage swing can be unequally divided. The peak value of the voltage swing at the feed-forward capacitor becomes lower than the threshold voltage of the device, because the impedance at that point becomes small because of the large capacitor value.

Fig. 4.34 shows the schematic of the CMOS switch using feed forward capacitors.

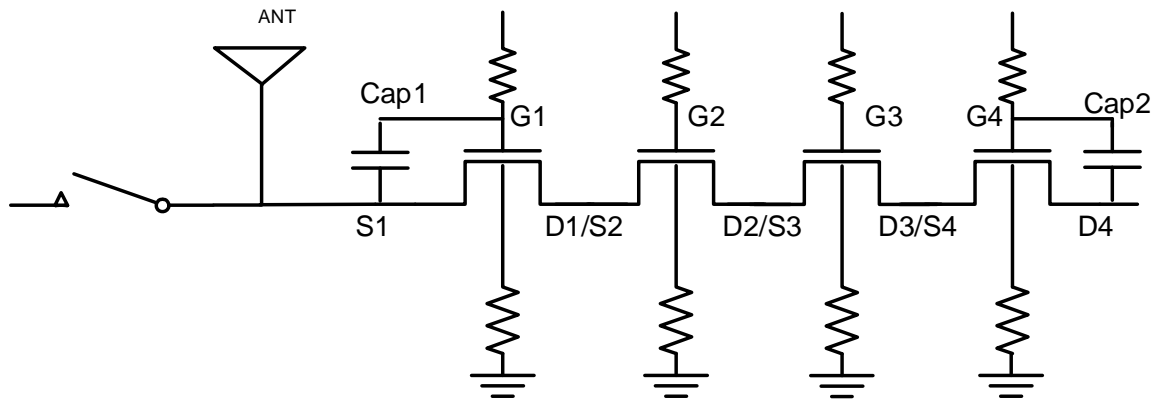


Fig. 4.34. Schematic of the SPDT switch using the feed forward capacitor.

The feed-forward capacitor is employed in the multi-gate structure or multi-stack structure. Fig. 4.35 shows the voltage swing difference between the source and the drain at Fig. 4.34. As can be seen, the voltage swings of V_{s1d1} and V_{s4d4} are smaller than those of V_{s2d2} and V_{s3d3} .

This is because the impedances of the device, M1 and M4 are smaller than those of the M2 and M3 because of the additional capacitors, Cap1 and Cap2. Fig. 4.36 shows the voltage swing at each source/drain port and each gate port as well as the voltage difference between the source and the gate.

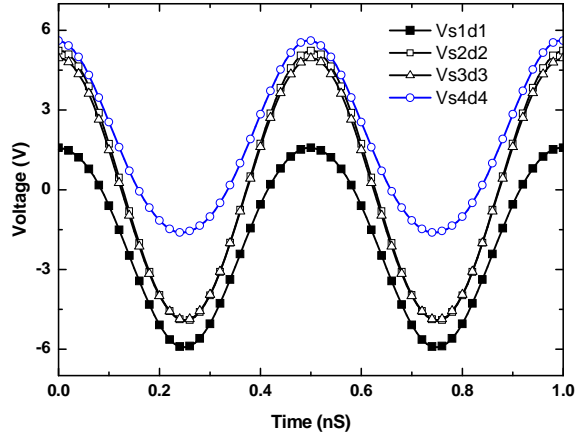


Fig. 4.35. Voltage swing difference between source and drain in Fig. 4.34

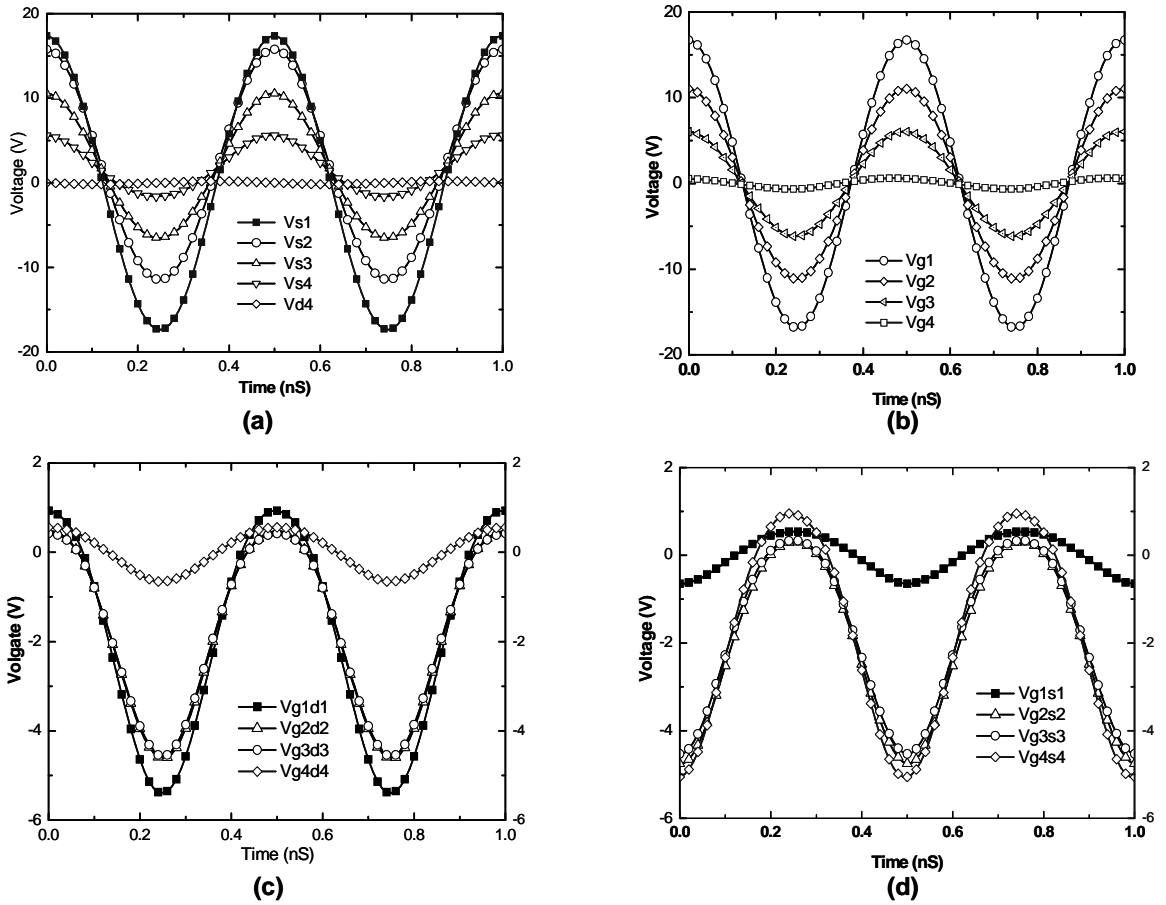


Fig. 4.36. Voltage swing (a) at source, (b) gate, (c) drain and gate and (d) source and gate.

As can be seen in Fig. 4.36(b), the voltage swing at the gate port is divided simply by the parasitic capacitors between the gate and the drain/source of the device. However, the Fig.

4.36(a) presents that half wave rectification caused by the parasitic diode pulls up the voltage swing at the S2 in Fig. 2. As a result, Fig. 4.36(c) and Fig. 4.36(d) illustrate all the voltage level between drain/source and the gate stay below the threshold voltage of the device. Therefore, high power handling capability of the switch in Fig. 4.34 can be obtained. The voltage swing level at the V_{g4d4} at Fig. 4.36(c) and V_{s1g1} at Fig. 4.36(d) is decided by the value of the capacitors, Cap 1 and 2 in Fig. 4.34. As the values of the capacitors increase, the voltage swings, V_{g4d4} and V_{s1g1} decrease. Large values of the capacitors, Cap1 and Cap2 reduce voltage stress at the devices, M1 and M4. However, this may bring another issue of the breakdown voltage stress at M2 and M3 in Fig. 4.34. Fig. 4.37 illustrates the safe region of the voltage swing at the device without breaking linearity of the switch. The threshold voltage of the device is called an upper region of the device for safe voltage swing. Lower limit of the device to ensure the linearity of the switch is determined by the breakdown voltage of the device. Since the upper limit is decided by the threshold voltage of the device, the lower limit can be claimed as the threshold voltage from the breakdown voltage of the device. For example, the thick gate-oxide device in a 0.18 μm standard process, which has a 0.6 V threshold voltage and a 6.8 V gate-oxide breakdown voltage has a 0.6 V upper limit and -6.2 V lower limit for the safe region without any distortion at the voltage swing.

Therefore, the four-stacked switch with the feed-forward capacitors in Fig. 4.34 can theoretically have 39 V peak-to-peak voltage swing allowance. This is equivalent as 37 dBm input power at the antenna port.

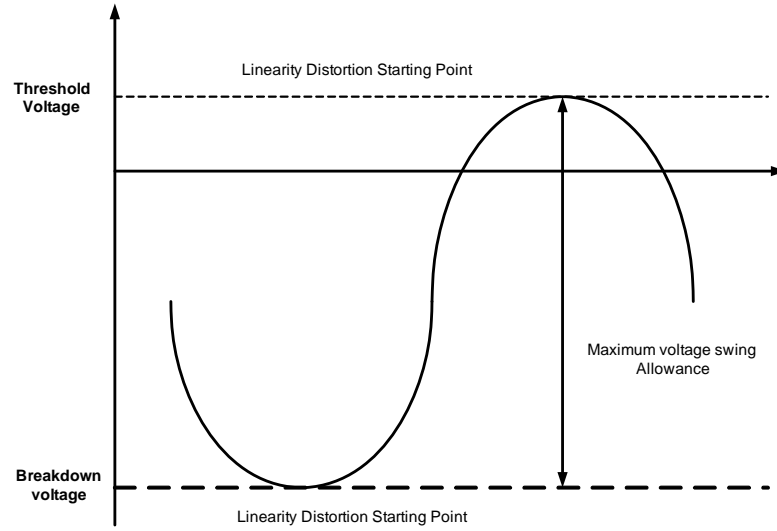


Fig. 4.37. Safe voltage swing region of the switch device.

However, if the value of the capacitor C_{p1} is so small that the voltage swing at V_{s1g1} and V_{d4g4} becomes larger than the threshold voltage of the device, the linearity of the switch can be distorted.

4.5.2. Measurement Results

An SPDT switch using the feed-forward capacitor is fabricated using a standard 0.18 μm CMOS process with triple well structure. Four-multi stacked FETs with feed forward capacitors are used in the Rx switch. All the FETs employ the body-floating technique to ensure negative voltage swing at the device. Also, thick gate-oxide devices are chosen to increase the power-handling capability. Five different values of the feed forward capacitors are implemented to compare the linearity performance accordingly. The capacitor values of 0.5 pF, 1.5 pF, 2 pF, 2.5 pF and 3 pF are chosen. The gate width of the device in the Tx and Rx switch is 2 mm. Fig. 4.38 shows the photograph of the CMOS switch fabricated. Fig. 4.39 and Fig. 4.40 show small signal measurement results of the Tx switch and the Rx switch, respectively.



Fig. 4.38. Photograph of the CMOS switch using the Feed-forward capacitor

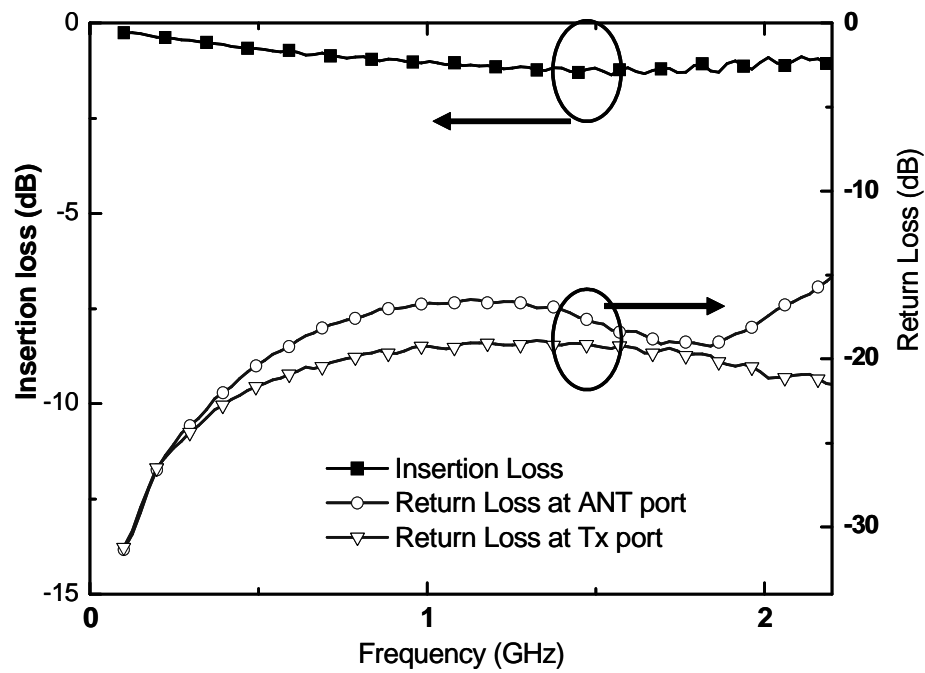


Fig. 4.39. Measured S-parameters of Tx switch

Tx switch provides 1 dB insertion loss and 1.4 dB insertion loss at 900 MHz and 1.9 GHz, respectively. The Rx switch has the 1.4 dB insertion loss at 900 MHz and 1.8 dB insertion loss at 1.9 GHz. The isolation performance of the Rx switch provides -35 dB at 1.9 GHz. However, return loss at ANT port reveals that there is a room for improvement

of impedance matching at the antenna port. Improvement of the insertion loss is also expected from the impedance matching.

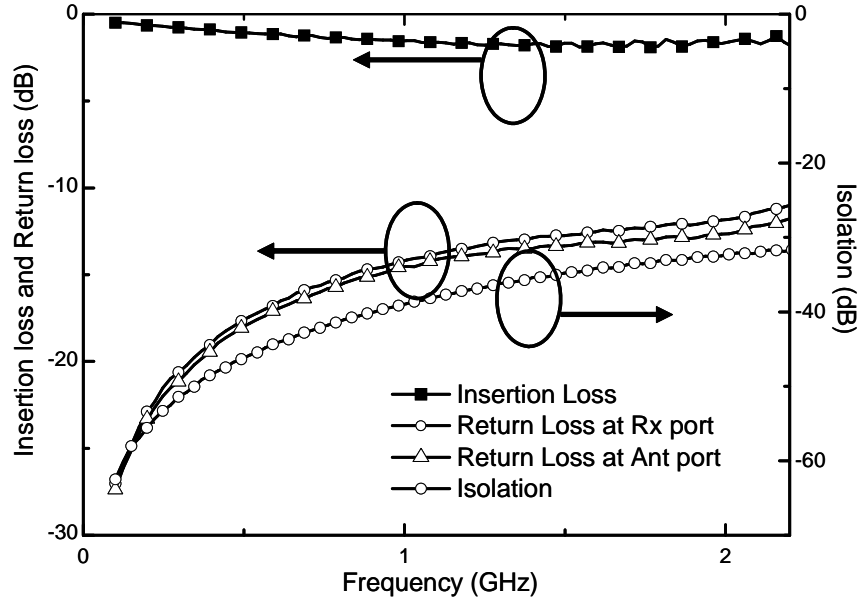


Fig. 4.40. Measured Rx switch performance. (S-parameters)

Fig. 4.41 presents the power handling capability of the switch fabricated according to the value of the feed-forward capacitors. The highest power-handling capability of the switch was observed at 35.2 dBm input power from the 2pF feed forward capacitor. 34.5 dBm, 33.8 dBm and 33.1 dBm of 1 dB compression point are obtained from 2.5 pF and 3 pF, 1.5 pF and 0.5 pF of the feed-forward capacitors. Since the individual resistor is connected to the each N-well of the each switch device in the Rx switch, there is no sudden drop point of 1 dB compression point observed in the previous section. The small value of the capacitor such as 0.5 pF cannot have the high enough power handling capability, because the peak voltage of the V_{slg1} and V_{dlg1} at Fig. 2 can be higher than threshold voltage, as stated in the previous section. On the other hand, 3pF value of the feed-forward capacitor shows retreat of the linearity compared to the 2

pF of the feed-forward capacitor. This is caused by the voltage swing at M2 and M3 in Fig.2 reaching the breakdown voltage of the device at the lower input power.

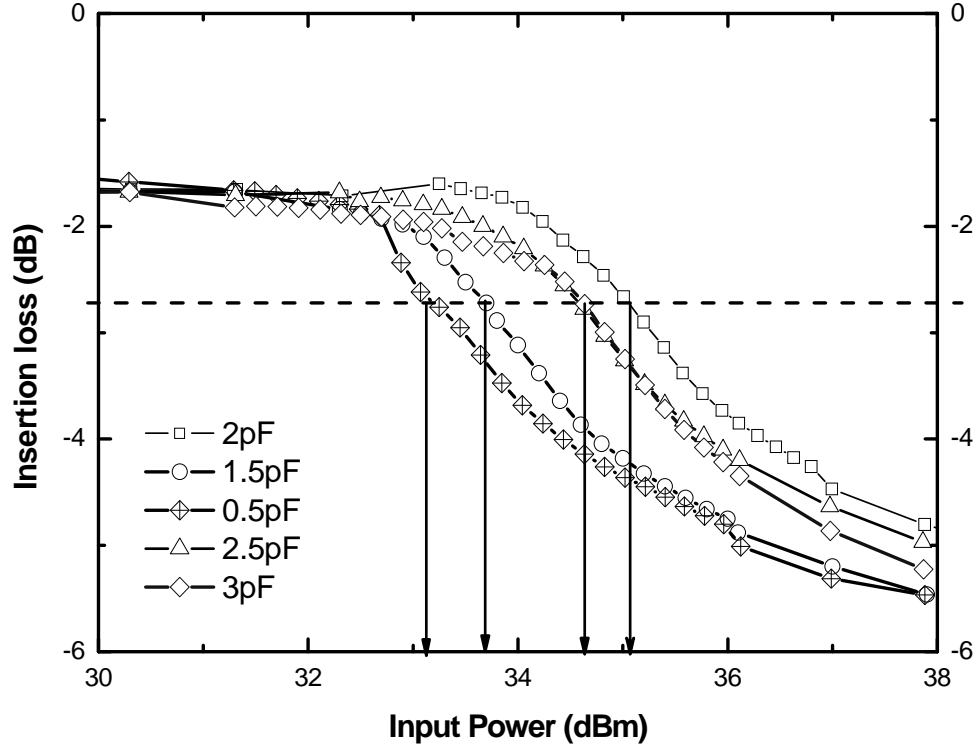


Fig. 4.41. 1dB compression point of the SPDT switch according to the value of the feed-forward capacitors (1.9GHz).

4.5.3. Summary

SPDT switches using the feed-forward capacitors are fabricated and tested. The measured S-parameter shows 1 dB and 1.4 dB insertion loss at 900 MHz and 1.9 GHz, respectively, in the Tx switch. The Rx switch provides 1.4 dB and 1.8 dB insertion loss at 900 MHz and 1.9 GHz. The 1 dB compression point of the switch is observed at 35.2 dBm input power at 1.9 GHz. This level of power handling capability shows a possibility of integration of the CMOS switch with the high power CMOS power amplifiers so that a fully integrated CMOS RF front-end circuit can be achieved.

CHAPTER 5.

MULTI MODE AND MULTI BAND SWITCH DESIGN USING GaAs E/D-MODE p-HEMT PROCESS

Even though there have been made lots of efforts to achieve low cost, small size switch design using CMOS technology, GaAs switches commercially prevail in most of high-power applications.

The current issues in designing the high-power switch using a GaAs process[41] are requirement of low cost, low control voltages, small size, and the complexity of integration with various wireless communication standards. As the demand for integrating different standards in one chip increases, the design of the GaAs switch is getting complicated considering power-handling capability, isolation, low insertion losses, low-harmonic performance, and return losses. The complexity of the design in a limited area to achieve low cost causes degraded performance of the switch. The high insertion loss of the switch is due to the increase of leakage current by branches in OFF state as well as the impedance mismatch caused by the parasitic capacitors. Also the power-handling capability regarding the second and third harmonics[6, 42] could be one of the issues related to the linearity. As the number of the branch at the antenna port increases, the classic theory of the linearity of the switch is not valid any more. Except from the voltage dividing theory, special care of leakage current toward the OFF-state branch needs to be taken.

In this section, the design of single-pole-multi-throw (SPMT) high power switches using the GaAs 0.5 μm E/D mode pHEMT process is introduced. This GaAs

switch is implemented based on the specification of the switch which is commercially available in multi-band and multi-mode application. The performance of the fabricated switch is compared to the commercial product, and design strategy will be discussed.

5.1.Design of multi band and multi mode GaAs switch with CMOS driver.

Based on the description provided in the previous chapter, configuration of the stacked FETs was chosen to design a SP9T switch. Modifying of gate periphery is not available in process provided by TriQuint so that gate length is fixed at 0.5 μm . The SP9T switch will cover EGSM, PCS/DCS and UMTS bands. The highest power that the switch needs to deliver is 35 dBm of EGSM.

A single D-mode pHEMT FET can transmit only 30 dBm so that a multi-stacked FET structure needs to be employed to transmit 35 dBm. The three-stacked transistors are chosen to maximize the transmit power as well as to minimize the insertion loss.

Fig. 5.1 shows the schematic and micro photograph of a commercial SP8T switch that is used as a reference design of the multi-band and multi-mode GaAs switch.

As can be seen, an antenna port is shared by four Tx branches and one Rx branch. Even though four Rx branches are needed to cover 850/900 MHz and 1800/1900 MHz bands, these branches share one three stacked branch at the antenna port. As described in the previous chapter, increasing the number of branches at the antenna port can deteriorate power-handling capability and harmonic performance of the switch.

The reference switch was designed for four Tx paths. Each Tx path was assigned for EGSM, PCS/DCS, and UMTS bands. All the transmit power paths have three-stacked FETs, which are not necessary for UMTS bands because the UMTS bands have only to

transmit 28 dBm input power. Also four different operating frequencies of the Rx bands are delivered through one three-stacked branch in Rx switches. This idea can help reduce the leakage current at the antenna port because of the decreased number of the branch. However, this can increase insertion loss because of the large leakage current toward all the other Rx paths, when one of the Rx paths is ON-state.

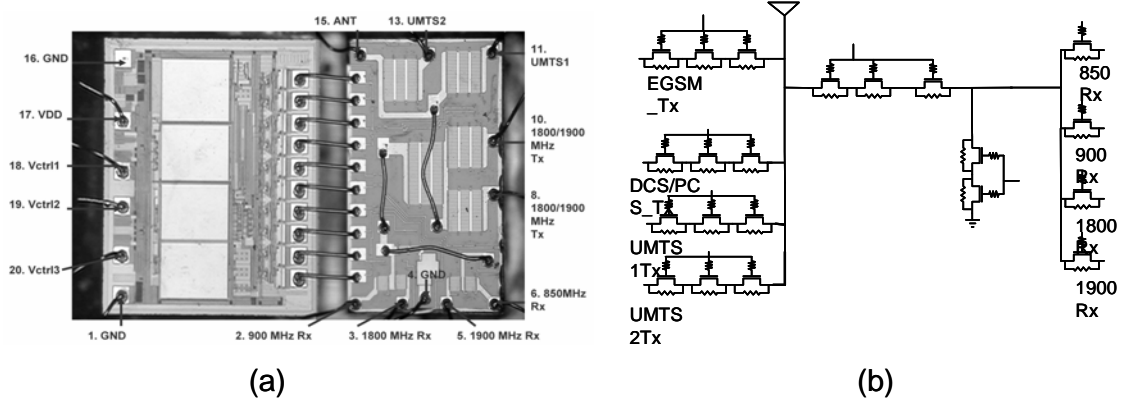


Fig. 5.1.(a). Microphotograph of the commercial products of GaAs SP8T switch, and (b). Schematic of the GaAs SP8T switch.

As can be seen in Fig. 5.1(a), the commercial product is using CMOS technology to realize a DC/DC converter and digital logic circuit. This is one of methods to realize high power GaAs switch with multi stack FETs structure. The DC/DC converter generates high DC voltages such as 8 V for a biasing voltage and 9 V for control voltages. GaAs FETs have more margins in terms of AC voltage swing in case of the large signal input to prevent the channel or the harmonic source from forming in OFF state devices, which could be the limitation of the linearity of the switch. Also only positive voltages can be used because the DC/DC converter and the digital logic circuit are implemented in silicon based technology. Generating negative voltage to increase the linearity of the GaAs switch can provide one advantage that is no necessity of the DC block capacitor in the system, because the voltage level at the input and the output ports of the switch is AC

ground. This could be an effective method to reduce assembly cost of the switch module. However, the triple well structure of CMOS technology would be pre-requisite to implement the negative voltage generator as the switch driver.

Fig. 5.2. shows different versions of SP9T switches.

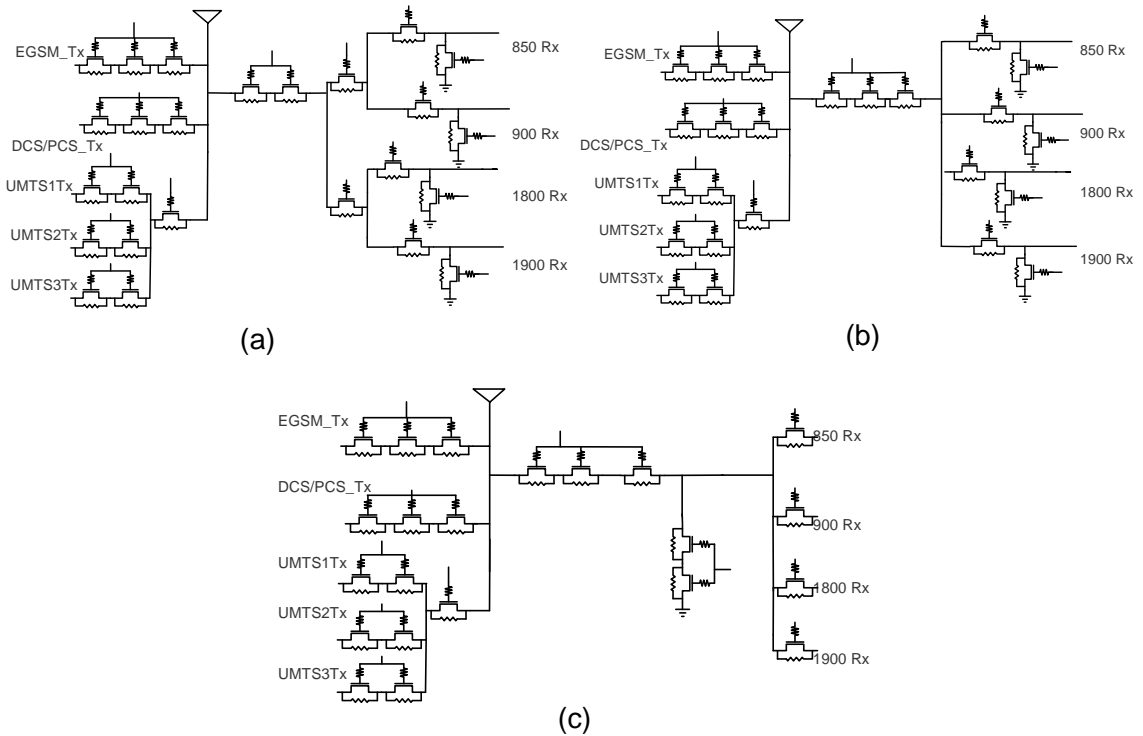


Fig. 5.2. Different version of SP9T switch designs for the multi mode and multi band operation.

Differently from the reference design shown in Fig. 5.1, UMTS bands in Fig. 5.2 share one main large device at the antenna port and utilize two stacked FETs structure for each band. The proposed structure has advantages such as reducing the overall size of the layout, and providing high power-handling capabilities with the minimal number of stacked FETs for UMTS bands

Each Rx switches at all the versions has different configuration from each other. Simple simulation results show that insertion loss caused by the parasitic capacitors

because of the three OFF-state switches is almost 3.5 times bigger than insertion loss of single ON-stage FET.

Optimization of Rx switches is focused on reducing leakage currents toward OFF state switches for another frequency band. There is one shunt device in the Rx switch to provide the isolation performance among switches.

When Tx mode is in operation, shunt FETs at the Rx mode need to be ON state to bypass leaking power to ground to protect the receiver blocks. The location of shunt device in each configuration can vary to observe the best performance in terms of improving isolation as well as insertion loss at each Rx path.

The size of device also varies depending on the operating frequencies. The size of the device in higher band operation is a little bit larger than that of the device in a low band operation to maintain not only high isolation, but also low insertion losses by reducing the leakage current. Smaller device has higher OFF-state impedance than larger device; in other words smaller device has better isolation performance than larger device.

5.1.1. Measurement data of the SP9T switch using GaAs p-HEMT technology

Table 1 and Table 2 shows performance comparison between the commercial product and multi band and multi mode switch GaAs switch manufactured.

As can be seen, most of data meet the specification. However, insertion losses in high band and the second-harmonic performances in the GSM and DCS/PCS bands still need to be improved. The insertion loss can be improved by controlling matching network which can be changed by the length of the bond wire.

Table 1 Performance of the GaAs SP9T switch: Insertion loss

Item	Frequency (MHz)	Pin (dBm)	ON pass	OFF pass	TQS Measurement					NEC SP8T	Unit
					ver.1	ver.2	COB Loss	Ver.1 – COB IL	Ver.2 – COB IL		
Insertion loss	1710-2170	28	UMTS1-ANT		1.5	1.6-1.9	0.8-0.9	0.6	0.7	0.55	dB
	824-894	28	UMTS2-ANT		0.53	0.53	0.2-0.3	0.23	0.23	0.3	dB
	2100	28	UMTS3-ANT		2.3	3.1	0.9-1.2	1.1	1.9	N/A	dB
	824-915	35	850/900 Tx-ANT		0.5	0.5	0.2-0.3	0.3	0.3	0.3	dB
	1710-1910	33	1800/1900Tx-ANT		1.9	1.16	0.6-0.7	1.2	0.46	0.45	dB
	869-894	0	850 Rx-ANT		0.78	0.67	0.2-0.3	0.48	0.37	0.6	dB
	925-960	0	900 Rx-ANT		0.78	0.67	0.25-0.3	0.48	0.37	0.6	dB
	1805-1880	0	1800 Rx-ANT		2.4	2.1	0.65-0.85	1.55	1.25	0.85	dB
	1930-1990	0	1900 Rx-ANT		2.4	2.5	0.75-0.85	1.55	1.65	0.85	dB

Table 2 Performance of the GaAs SP9T switch: Harmonic performance

Item	Frequency (MHz)	Pin (dBm)	ON pass	TQS Measurement			Unit
				Ver.1	Ver.2	Spec Min/Max	
2nd Harmonic	3420-3960	28	UMTS1-ANT	-72	-70	-68/80	dBc
	1648-1698	28	UMTS2-ANT	-70	-70	-68/80	dBc
	4200	28	UMTS3-ANT	-72	-72	-68/80	dBc
	1648-1830	34	850/900	-62	-60	-68/80	dBc
	3420-3820	33	1800/1900	-64	-60	-68/80	dBc
3rd Harmonic	5130-5940	28	UMTS1-ANT	-86	-82	-68/80	dBc
	2472-2547	28	UMTS2-ANT	-83	-82	-68/80	dBc
	6300	28	UMTS3-ANT	-86	-82	-68/80	dBc
	2472-2745	34	850/900Tx-ANT	-82	-79	-68/80	dBc
	5130-5730	33	1800/1900Tx-ANT	-82	-79	-68/80	dBc

However, the second harmonic performance still remains as issue to be resolved.

The simulation data of 2nd harmonics shows good matching with specifications. However, the model used in simulation does not cover all the harmonic simulations in all the power

levels. This harmonic performance issue can be resolved by increasing the number of stacked FETs and controlling size of the device. Also matching network improvement might affect the harmonic performance. As stated earlier, the SP9T switch has two more branches at the antenna port to cover two UMTS bands. This can increase overall leakage current of the system. Increased leakage current toward OFF state device can affect the linearity of the Tx switch.

Fig. 5.3 shows the photograph of the SP7T switch, that has the same structure as the design version 1. in the Table 1. Since this is SP7T switch, the leakage current at the antenna port is significantly less than that of the SP9T switch. Table 3, Table 4, and Table 5 show the performance of SP7T switch.

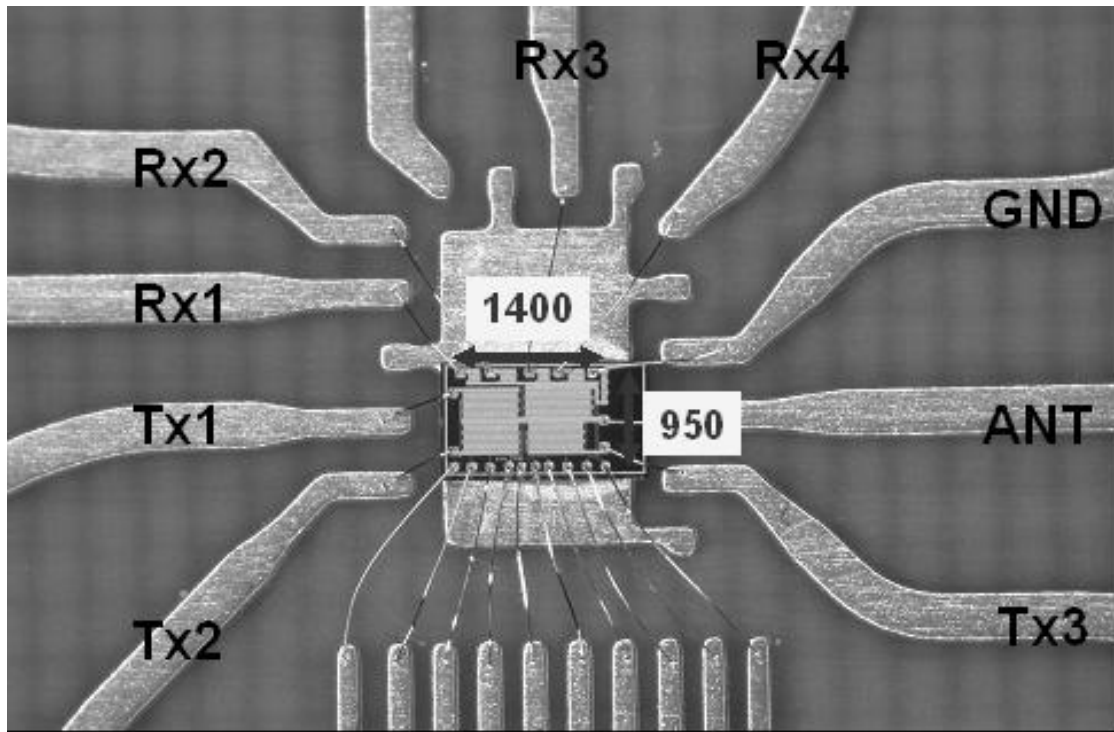


Fig. 5.3. Photograph of the SP7T switch assembled on the COB

Table 3 Insertion losses of the SP7T switch

Parameter	Condition	Pin (dBm)	Typ.	Max.	SP7T	Unit
Insertion Loss	Ant-UMTS 2100	28	0.55	0.7	0.45	dB
	Ant-850/900Tx	35	0.3	0.45	0.4	dB
	Ant-1800/1900Tx	33	0.45	0.6	0.45	dB
	Ant-850Rx	0	0.6	0.75	0.9	dB
	Ant-900Rx	0	0.6	0.75	0.85	dB
	Ant-1800Rx	0	0.85	1.0	1.45	dB
	Ant-1900Rx	0	0.85	1.0	1.45	dB

Table 4. Return losses of the SP7T switch

Parameter	Condition	Min.	Typ.	Max.	SP7T (ANT / ON Port)	Unit
Return Loss	UMTS 2100	20	-	-	17 / 22	dB
	850/900Tx	20	-	-	21 / 21	dB
	1800/1900Tx	20	-	-	22 / 21	dB
	850Rx	20	-	-	17 / 15	dB
	900Rx	20	-	-	17 / 15	dB
	1800Rx	20	-	-	12 / 11	dB
	1900Rx	20	-	-	12 / 11	dB

Table 5. Harmonic performance of the SP7T switch

Parameter	Condition (Pin dBm)	Min.	Typ.	SP7T	Unit
2nd harmonics	UMTS 2100 (28 dBm)	68	80	74	dBc
	850/900Tx (35 dBm)	70	80	74	dBc
	1800/1900Tx (33 dBm)	68	80	72.9	dBc
3rd harmonics	UMTS 2100 (28 dBm)	68	80	79.69	dBc
	850/900Tx (35 dBm)	70	80	87.69	dBc
	1800/1900Tx (33 dBm)	68	80	84	dBc

The second harmonic performance in the SP7T switch design is dramatically improved. The only difference between the SP7T and SP9T switch design is the reduced number of the branch at the antenna port. As a result, the layout consideration to reduce the leakage current toward the OFF-state device needs to be seriously taken into. Normally, it is said that there are three major causes to determine the harmonic performance of the switch device. First, the maximum current of the device can limit the linearity. This can be resolved by increasing size of the device. Second, pinch-off voltage and breakdown voltage limit the power handling capability of the switch. Once, any of these rules first reach the limit, the generation of the harmonics initiates.

5.2.Layout consideration of the SPMT switch design.

As you can see Table 3 and Table 4, the insertion loss of the multi port switch is higher in the high band than in the low band operation. This is caused by the parasitic capacitors of the OFF-state device connected in shunt. Fig. 5.4 illustrates the series-shunt configuration in the SPDT switch. Basically, the switch is represented as R_{on} resistor in ON state and C_{off} capacitor in OFF state as can be seen in Fig. 5.4 (b). Therefore, when the M2 is in ON state, there is a capacitor between the antenna port and the Rx path. Also, the antenna port looks at the other capacitor caused by the M1 in OFF state.

As the size of the device increases, the size of the capacitors also becomes large. In the case of the single pole multi throw switches, the size of the parasitic capacitor next to the antenna port becomes a few pF. Even in the case of the Rx path of the SP7T switch, when a Rx switch is in ON state, there must be three other switches in OFF state so that there are a large values of parasitic capacitors connected to the series path.

An inductance of the bond wire between the RF pad and the pad on COB can cancel out the capacitance of the shunt devices. There might be a chance to use internal bond wires to cancel out capacitance of the OFF-state device. There are a couple of inner wires in Fig. 5.1 (a).

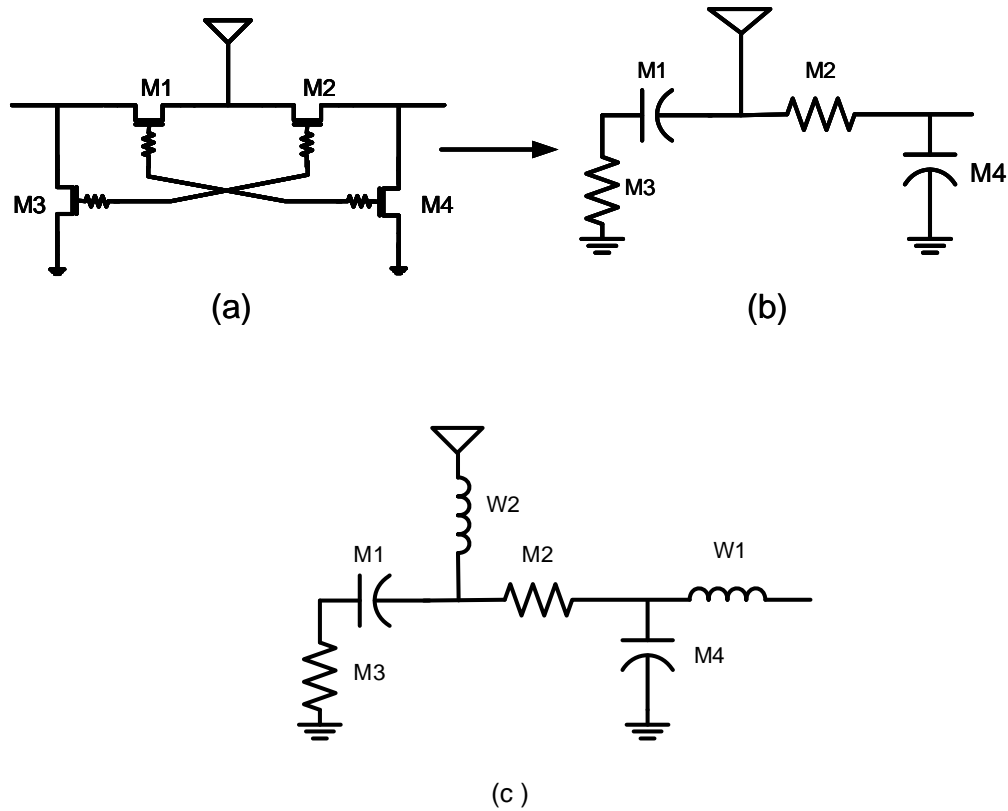


Fig. 5.4. (a) SPDT switch with series shunt configuration. (b) M2 and M3 in ON state , M1 and M4 in OFF state , and (c) impedance matching configuration.

The primary function of the inner wires is to cancel out the capacitance and improve impedance matching. However, when it comes to the issue of the yield, using inner wire connection of the IC can drop the yield in mass production. If a spiral inductor is used instead of the inner bond wire, the yield problem can be resolved. However, this can cause another drawback such as large die area.

5.3.Design of multi band and multi mode GaAs switch with integrated driver

One of the bottlenecks in integrating digital control circuits with GaAs switch IC core was that GaAs process does not have NMOS and PMOS as CMOS process has. Most of digital circuits consist of combination of PMOS and NMOS. However, E/D mode pHEMT process enables to build up digital logic circuit in GaAs process. Normally, depletion mode pHEMT is used for high power circuit implementation due to higher breakdown voltage than enhancement mode pHEMT.

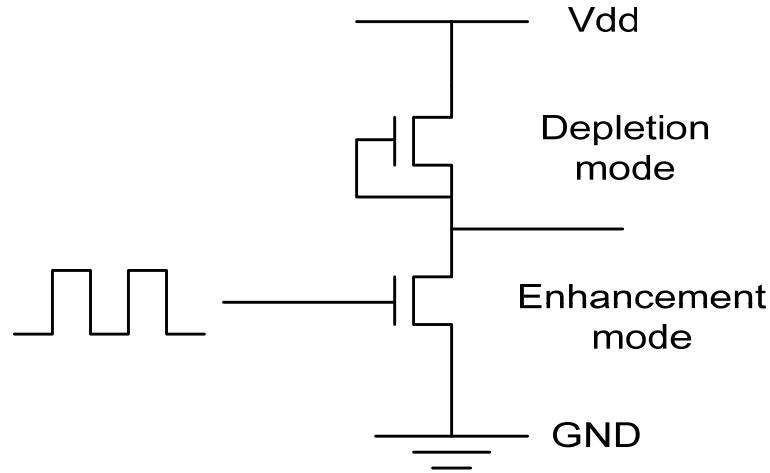


Fig. 5.5. Schematic of the inverter core implemented in E/D mode p-HEMT process.

Fig. 5.5 shows example of the inverter designed using depletion mode pHEMT and enhancement mode pHEMT. Using this configuration, digital logic circuit can be integrated in the GaAs switch core IC.

However, another problem emerges as the digital control circuit can be integrated in GaAs process. Most of wireless communication products uses dc power supply around 3-4 V. However, the specification of the power handling capability and low harmonic performance of the GaAs switch has been ensured by using high supply voltages such as 8 or 9 V so that they need to have a charge pump realized by Si-based technology which

integrate digital logic circuit at the same time. If the digital logic circuit is integrated in the GaAs circuit, high voltage supply would be no more option for the high power handling capability and low harmonic performance. Also, recent wireless communication products demands low control voltage usage. As a result, feed forward technique would be necessary for the purpose of low voltage usage as control voltages.

5.4.Design Switch IC of multi band and multi mode GaAs switch with integrated driver

The proposed GaAs switch in multi band and multi mode operation is designed using feed forward technique with digital control circuit integration. The cost would be the biggest issue in the industrial point of view when it comes to the commercialization. Considering the manufacturing cost, the size of the die should be limited by 2 mm by 2 mm for the single pole nine throw switch design. This can limit the optimization of the size of the devices used in GaAs switch and performance of the switch. Regarding the specification of the GaAs switch design on target to meet in the proposed work, the GaAs switch should have less than 0.6 dB and 1.2 dB insertion loss in low band and high band respectively in Tx mode as well as Rx mode. Also all the harmonic performance should be below -68 dBc in all bands, while all the other specifications need to remain same as the previous work.

Fig. 5.6 shows the schematic of the GaAs switch IC core for single pole seven throw. The SP7T switch design has three Tx switches and four Rx switches. Frequency bands of Tx switches are 900MHz, 1900MHz, and 2100 MHz. Frequency bands of Rx switches are 850MHz, 900MHz, 1800MHz and 1900MHz. This SP7T structure can be described

as a combination of two SP4T switches. At the antenna port, one SP4T switch controls in-and- out signals with high power-handling capability.

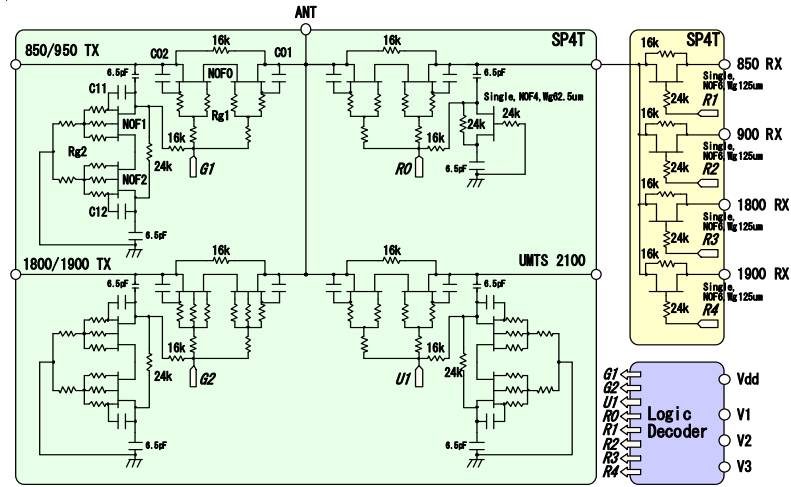


Fig. 5.6. Schematic of the SP7T switch with decoder integrated

The size of the SP4T switch at the antenna port needs to be big enough to flow large current and minimize insertion loss at the Rx path. One of the branches in the SP4T switch is used as the Rx path. Four Rx branches are sharing one big device to receive signals from the antenna port. Therefore, there is another SP4T switch for Rx signal paths. The size of the SP4T switch in Rx switches needs to control low insertion loss of the each Rx path and high isolation between the Rx paths. The power-handling capability is not a big issue for Rx SP4T switch. Therefore, the size of the Rx switches does not have to be large enough to transmit high power currents. Also, the Rx switches do not have to employ multi-stack FETs or any other scheme to allow high voltage swing.

Metal0-to-metal1 capacitors are implanted as feed-forward capacitors under the RF signal paths to reduce the overall size.

Since the size reduction is one of the key design points, multi-gate transistors are employed instead of multi-stack FETs. However, there is a drawback in the multi-gate

FETs in terms of the linearity, compared to the multi-stack FETs. The second harmonic performance of the multi-gate FETs is better than that of the multi-stack FETs. However, the third harmonic performance of the multi-gate FETs is worse than that of the multi-stack FETs. Fig. 5.7 shows the simple schematic of the multi-gate FET and multi-stack FETs.

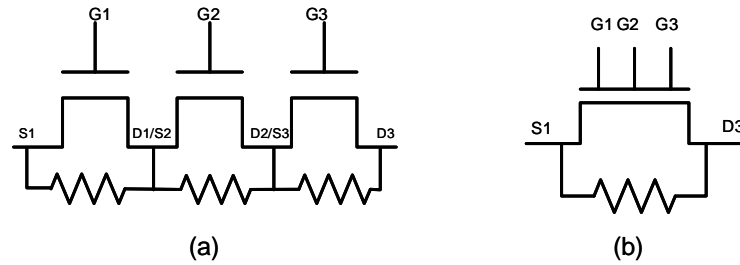


Fig. 5.7. (a) multi-stack FETs and (b) multi-gate FET

Multi-stack FETs has a bias resistor to connect source and drain at each device. Therefore, the voltage level at the source and the drain is always consistent. However, the multi-gate FET can not have those connections because of no existence of source/drain ports between devices. This causes degraded third harmonic performance. However, the degraded third harmonic problem can be easily canceled out at the antenna port.

Fig. 7 shows an example of the notch filter to cancel out the third harmonics. The metal-to-metal capacitor is integrated to the antenna pad. Then, there is a bond wire connected to the ground. This can form LC series resonator at the third harmonic frequency. The third harmonics can be grounded through the LC series resonator so that the third harmonic performance can be improved.

However, this approach can decrease the yield of the product. Therefore, another approach to reduce the third harmonic performance needs to be devised.

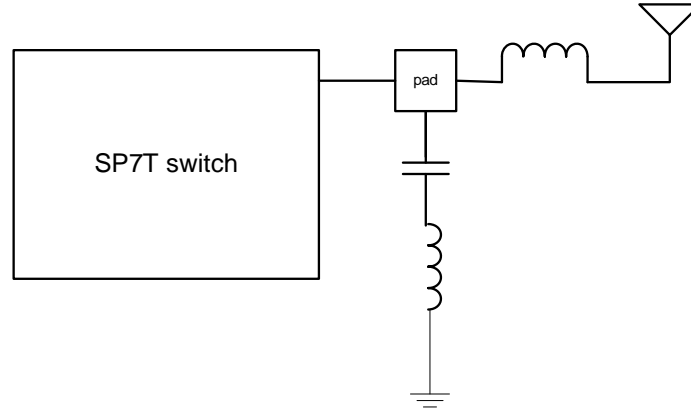


Fig. 5.8. Notch filter implementation at the antenna pad

Table 6. Insertion loss of the SP7T switch

Parameter	Condition	Pin (dBm)	Typ.	Max.	Meas.	Unit
Insertion Loss	Ant-UMTS 2100	28	0.55	0.7	0.58	dB
	Ant-850/900Tx	35	0.3	0.45	0.39 / 0.38	dB
	Ant-1800/1900Tx	33	0.45	0.6	0.54 / 0.59	dB
	Ant-850Rx	0	0.6	0.75	0.73	dB
	Ant-900Rx	0	0.6	0.75	0.63	dB
	Ant-1800Rx	0	0.85	1.0	0.93	dB
	Ant-1900Rx	0	0.85	1.0	0.97	dB

Table 7. Harmonic Performance of the SP7T switch

Parameter	Condition	Min.	Typ.	Meas.	Unit
2nd harmonics 2fo	UMTS 2100	68	80	89.9	dBc
	850/900Tx	70	80	80.6	dBc
	1800/1900Tx	68	80	82.8	dBc
3rd harmonics 3fo	UMTS 2100	68	80	69.2	dBc
	850/900Tx	70	80	76.5	dBc
	1800/1900Tx	68	80	70.0	dBc

As can be seen in Table 6 and Table 7, insertion losses meet all the specifications. However, the third harmonic performance still needs to be improved. The improvement of the third harmonic performance remains as future work.

CHAPTER 6

CONCLUSTIONS

Mobile wireless devices using CMOS technology have experienced unprecedented growth of wireless communication in the last decade. This trend is expected to continue in another next decades. The demands for low cost, small size and integration of the functional building blocks into one die drives recent researches of the circuits using CMOS technology in various areas. Recent achievement of the integration of the functional building blocks of the RF systems in CMOS technology satisfies an industry standard and enables CMOS technology to become leading technology in the mobile wireless communication. All these achievement can be referred to be accomplished in a small signal domain. This means all the successful achievements has been done in the area which only deals with a small signal. However, enormous efforts are made to achieve another level of integration functional blocks in a large signal domain. CMOS power amplifier could be a good example. Since CMOS process has been known as a technology for digital circuits, it is challenging to integrate large signal circuits in the process of which has limitation such as low breakdown voltage. The recent research reports that the performance of the CMOS power amplifier is getting close to the industry standard. Another achievement is about to be accomplished in a large signal domain in modern wireless industry. Design of the high power CMOS switch can contribute in a similar fashion as the CMOS power amplifier does in the modern wireless communication system.

Chapter 2 studies conventional techniques to implement high power switches. Impedance matching network and LC resonator circuits using passive component increase power handling capability of the switch. However, it requires large area. Also the narrowband operation is serious disadvantage of these configurations. Multi gate FETs and multi-stack FETs are very popular method because of its small size and wideband operation. However, the power handling capability of these configurations is not as high as the LC resonator circuits. Therefore, the feed-forward method or external voltage boosting method such as DC/DC converter is commonly accompanied with these configurations. The body-floating technique is a key factor to implement high power CMOS switch in a standard process. This technique ensures the negative voltage swing at the CMOS switch.

Chapter 3 presents employing the conventional configurations introduced in the chapter 2 in the CMOS technology. The performance of each configuration is measured and characterized. The LC resonator type CMOS switch provides the high power handling capability with relative high insertion loss because of low Q value of the CMOS process. The multi gate structure is very effective method in terms of size reduction. However, sharing one substrate of the multi-gate structure limits power-handling capability of the device. The substrate body switching technique is introduced at multi-stack FETs. This technique demonstrates improvement of the power-handling capability. However, the channel formation of the multi-stack FETs in OFF state still remains a bottleneck to improve linearity.

Chapter 4 introduces a novel method to prevent channel formation of the device in OFF state. This is called the adaptive voltage swing distribution method in the multi

stack FETs. The size of the switch using this method is same as the switch using a conventional multi stack structure with body floating technique. The power handling capability from this configuration is achieved around 2 W in terms of 0.3 dB compression point. The layout optimization from this configuration is presented. After considering the voltage swing effect at the N-well of the NMOS device using triple well process, the problem of the sudden drop point of the 0.3 dB compression point is resolved. Another method to prevent channel formation of the device in OFF state is introduced. This is called the feed forward capacitor. The power handling capability from this configuration is obtained at 35 dBm 1 dB compression point.

Chapter 5 depicts design of the single pole multi throw switch using GaAs process. Various design approaches were introduced to reduce leakage current at the multi throw switch. The linearity of the switch reveals lower than -68 dBc at the second and the third harmonics in case of the SP7T switch design.

Even though a watt level power handling capability is achieved in the CMOS switch, additional works remains to improve the performance of the CMOS switch.

First, the impedance matching of the CMOS switches needs to be improved. The high insertion loss around 1.9 dB at 1.9 GHz is mainly caused by mismatched impedance of the device. As the size of the device increases, the value of the parasitic capacitors of the device in OFF state increases, too. Therefore, a technique to cancel out the capacitance is required without compensation of the insertion loss. Improving the impedance matching may lead to further improvement of the linearity of the switch.

The power handling capability of the CMOS switch can increase with special care in the layout. The current layout can have more parasitic capacitance and resistance. Also

the substrate of the device contributes the degraded power handling capability of the device. Also, the harmonic performance of the CMOS switch is still far behind the industry standard. Theoretically, the second harmonics and the third harmonics should be in the stable region if the voltage swing stays the safe region as stated in the section 4. However, the measurement results show the harmonics of the CMOS switch shows the transit point in the early stage of the input power. This can be related to the leakage current toward the device. Actually, the single pole multi throw switch shows degraded harmonic performance when the volume of the leakage currents increases even in the case the voltage swing level satisfies the upper limit and lower limit of the safe voltage swing region in a device.

Second, since 2 W level power handling capability of the CMOS switch is obtained, it is possible to integrate the CMOS power amplifier and the CMOS switch in one die for PCS/DCS applications. Also, LNA can be integrated too. A lot of issues can occur when the CMOS power amplifier is integrated with the CMOS switch in one die. The CMOS power amplifier can generate certain amount of heat in the substrate. This can deteriorate the performance of the CMOS switch. Also, the harmonics from the CMOS PA directly feeds to the switch. From the experience of the measurement, it can be expected that harmonics can degrade the linearity of the CMOS switch.

Currently, the CMOS power amplifiers employ integrated passive device to provide high Q transformer to combine the powers. Low pass filters and impedance matching networks can be designed using this high Q process. Also, the high Q inductor from the IPD process can help design of LNAs.

Finally, the device modeling for the switch design[43] is absolutely necessary in large signal operation. The circuit model consists of four port; drain, source, gate and bulk. However, in case of the switch operation, there are two more ports to consider, that are an N-well port of the NMOS device and the p+-pick up. All phenomenon created by the voltage swing operation in the substrate are not explained in the circuit simulation. Therefore, six port device needs to be proposed for designing high power CMOS switches. Also, the breakdown behavior of the junction diodes is not included in the circuit model. This effect must be included in the new large-signal model.

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