Integrated Input/Output Interconnection and Packaging for GSI

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2006

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Integrated Input/Output Interconnection and Packaging for GSI

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Acknowledgement

I would like to thank Prof. James D. Meindl for his guidance, inspiration, and support throughout my Ph.D. study. I am also very grateful to Prof. Sunk-Kyu Lim, Prof. Brouno Frazier, and for their time to review my dissertation. Thanks are also extended to Prof. Yogendra Joshi, Prof. Paul Kohl, Dr. Xiaojin Wei, and Dr. Paul Joseph for their great help. I would also like to express my gratitude to Jennifer Tatham Root for her continuous help and support during my dissertation years. My dissertation benefited so much from discussion and collaboration with my fellow GSI group members. Particularly, I would like to thank Dr. Muhannad Bakir for his help and insights. I would like to thank Deepak Sekar for a lot of discussion and help. In addition, thanks are extended to Dr. Kevin Martin, Joel Pikarsky, Gary Spinner, and cleanroom staff.

I would like to thank my parents, my wife, and my sisters, for their understanding and endless support. I also want to thank my wonderful daughter, Ashley Y. Dang.

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Summary

As IC technology advances toward gigascale integration (GSI), the performance of an IC chip will be limited by its interconnection capability. The bottlenecks in chip-package interfacing are mainly from thermal-mechanical mismatch, input/output (I/O) communication bandwidth, power distribution, and heat dissipation. Through wafer-level batch processing, novel integrated interconnects can be used to enable GSI packaging with high I/O density, high reliability, and high performance at low cost.

In this research, a set of integrated I/O interconnection and packaging technologies are investigated. MEMS-based sea-of-leads (SoL) compliant interconnects are demonstrated to be promising to eliminate the need for underfill between a Si chip and organic packaging substrate. Wafer-level packaging with the compliant interconnects can largely reduce the impact on the fragile low-k interlevel dielectric (ILD) films. The technology feasibility of the SoL MEMS I/O interconnects is demonstrated by process integration, assembly, and reliability assessment. To achieve the high power dissipation with compact form factor, integrated thermal-fluidic I/O interconnects and CMOS compatible microchannels are developed to enable a prototype on-chip microfluidic heat sink. In addition, highly integrated electrical and optical interconnects based on dual-mode polymer pillars are fabricated, assembled and tested as a potential solution to the I/O bandwidth bottleneck. The resulting integrated I/O interconnection and packaging technologies are compatible with back-end-of-the-line (BEOL) wafer processing and conventional flip-chip assembly.

Chapter 1. Introduction and Background

In recent decades, improvements in the computing performance of integrated circuits (ICs) have been mainly accomplished through increasing the number of transistors, as Moore's Law indicates. However, as IC technology advances toward gigascale integration (GSI), the performance of an IC chip will be limited primarily by interconnects [1.1, 1.2]. In particular, input/output interconnection (or I/O interfacing) is becoming a serious bottleneck, which includes power/signal I/Os and thermal dissipation paths, as illustrated in Figure 1.1. According to the International Technology Roadmap of Semiconductors (ITRS) [1.3], there are significant technical and economical challenges for die-to-package interfacing in future IC systems.

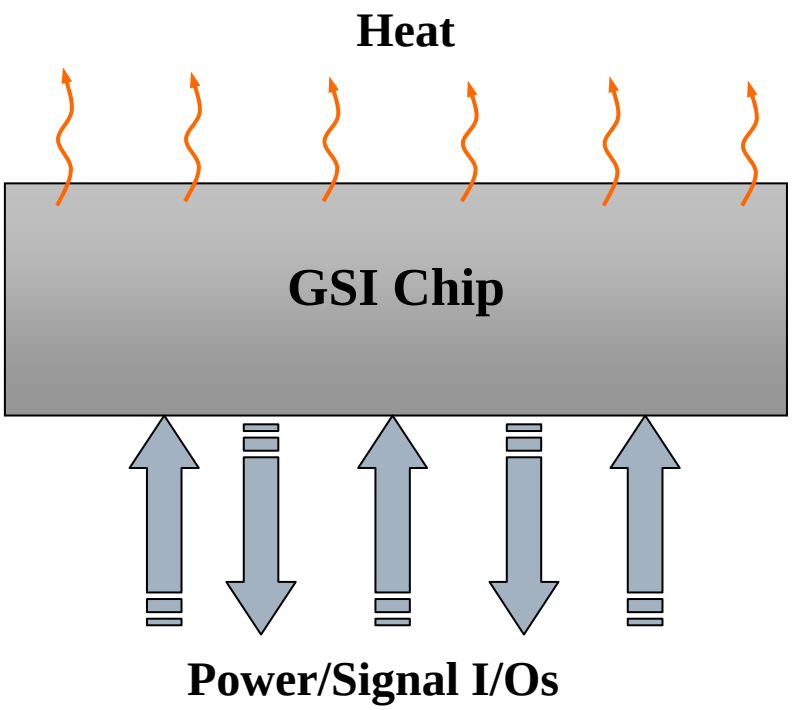


Figure 1.1: Schematic of chip-package I/O interfacing for a GSI chip.

First, the projected increase of pin count demands area array interconnection technologies that can continuously scale down in pitch and dimensions. Meanwhile, the application of the low-k interlevel dielectrics (ILD) raises more reliability issues because the mechanical strength of the porous low-k dielectric materials is weak enough to cause the delamination of bonding pads under thermal-mechanical stress [1.4-1.8]. To overcome these challenges, wafer-level packaging with compliant intermediate interconnects must be developed to reduce the impact on the fragile chip surface.

Second, the reliability and performance of interconnects and transistors greatly depend on the operating temperature. Chip cooling will become more critical as the chip power density increases. The ITRS projects that the power density of a single chip package will reach 108 W/cm^2 for cost performance applications in 2018 [1.3]. This requirement may exceed the heat removal limit of conventional forced-air heat sinks. Thus, microfluidic cooling is being considered as an ultimate solution because of a significantly higher heat transfer coefficient [1.9–1.11]. Liquid cooling also promises to lower operating temperatures, which can potentially improve the computing performance of microelectronic systems [1.12]. In particular, an on-chip microchannel heat sink can eliminate thermal interface related problems and represents the highest level of integration for liquid cooling. However, novel fabrication approaches for CMOS-compatible microchannels and thermal-fluidic I/O interconnection and packaging still need to be explored to implement chip-level microfluidic cooling.

Third, high bandwidth chip-board communication calls for optical interconnection. While planar optical waveguides have been extensively studied and used for “in-plane” signal transmission [1.13], more challenges exist for the integration of compatible high-density “out-of-plane” optical I/O interconnects because of their manufacturing complexity in fabrication,

packaging, alignment, and assembly [1.3, 1.14, 1.15]. Therefore, novel integrated optical I/O interconnection approaches must be developed.

In this chapter, conventional chip I/O interconnection technologies are briefly reviewed and the compliant wafer-level I/O interconnection technologies are compared and summarized. In addition, advanced chip cooling technologies are reviewed and the concept of integrated microfluidic cooling is presented. Finally, integrated electrical, optical, and thermal-fluidic I/Os are identified as useful enabling interconnection and packaging technologies for future generation gigascale integrated circuit systems.

1.1. Area Array Chip-to-Package Interconnection

Primarily because of their low melting temperature, solder alloys have a long history of use as I/O interconnections for ICs. By evaporation, electroplating, or screen printing through certain masks, very small volumes of solder can be deposited for use as high-density electrical interconnects in the form of area arrays with low-cost batch processing. The most typical example is the C4 (controlled collapse chip connection) flip-chip packages.

1.1.1. C4 Flip-chip Interconnection

Flip-chip packaging was first introduced by IBM in the 1960s and ceramic substrates with low coefficient of thermal expansion (CTE) have been used for decades without any reliability issues associated with the C4 joints [1.16]. Since the early 1990s, organic package substrates have rapidly emerged as an alternative to ceramic substrates for IC packages because of lower cost and higher performance [1.17]. However, organic laminate materials have an effective CTE of around 17 ppm, which is much higher than that of Si (~3 ppm). Because of this CTE mismatch, a large thermal-mechanical strain is induced on the solder joints under thermal excursion. To enhance the thermal-mechanical reliability of the solder joints, underfill is required

for organic flip-chip packages, as illustrated in Figure 1.2. The underfill is a mixture of epoxy and ceramic fillers and is normally applied by the capillary effect in the gap between a Si chip and a package substrate. Once cured, the underfill mechanically couples a Si chip with its mounting substrate.

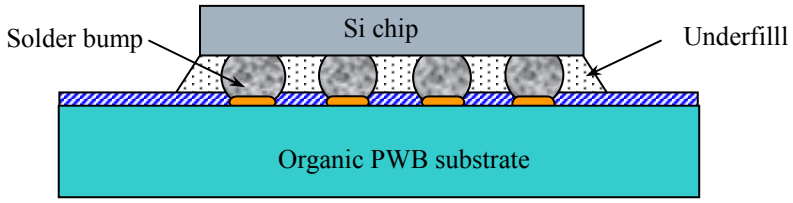


Figure 1.2: Schematic of a flip-chip on an organic PWB substrate with underfill.

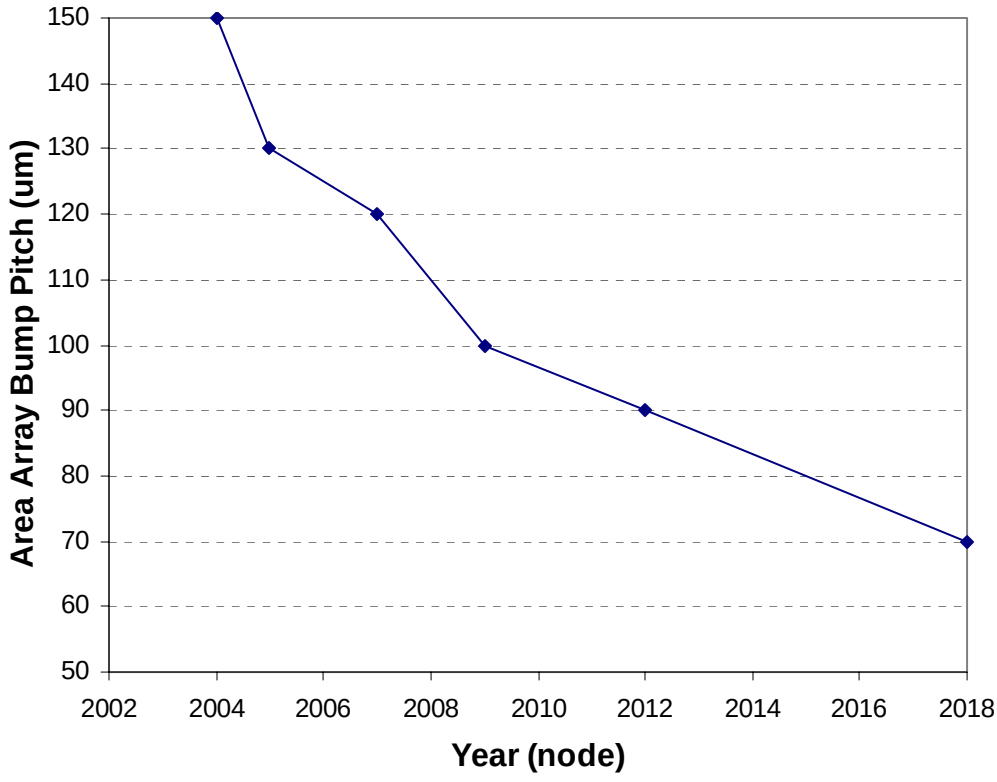


Figure 1.3: ITRS projection of area array bump pitch vs. technology node [1.3].

As projected by the ITRS, chip-to-package interconnect pitch will continue to scale down to provide very high I/O density (Figure 1.3). Thus, dimensions of the C4 solder joints in flip-chip packages must be reduced. With smaller solder joints, the thermal-mechanical strain (dimensionless) increases rapidly due to the reduced stand-off height according to [1.17]:

$$Strain = \frac{Displacement(m)}{Height(m)} \tag{1.1}$$

Meanwhile, the chip-package gap will become smaller and the spacing between solder joints will become tighter. The conventional capillary underfilling process, therefore, is expected to be more difficult and slow. The cost of underfill materials will increase because of these requirements. In addition, the application of underfill also raises other problems such as poor reworkability and electrical performance degradation [1.18-1.20].

Another challenge for conventional flip-chip packages is the application of the low-k interlevel dielectric (ILD). It is well known that low-k ILD materials are being widely pursued to reduce the RC delays of on-chip interconnect networks. Typical low-k materials are either organic films or hybrid organic/inorganic silicate films made by CVD or spin-on processes [1.4, 1.5]. Most low-k ILD materials are porous and mechanically fragile. Thus, chip-to-package interaction can cause critical reliability issues. Wang [1.6] and Mercado [1.7] have recently studied the impact of flip-chip packaging on the Cu/low-k interconnect structure. They concluded that although underfill is beneficial to the reliability of the solder joints, the strong coupling between the chip and the package substrate leads to a large local deformation in the on-chip Cu/low-k interconnects under thermal excursion. As illustrated in Figure 1.4, the local deformation can ultimately induce cracks or interfacial delamination in the Cu/low-k

interconnects because of the weak mechanical strength and poor adhesion of the low-k materials [1.5-1.8]. Therefore, flip-chip packaging of advanced low-k ICs is becoming more complex.

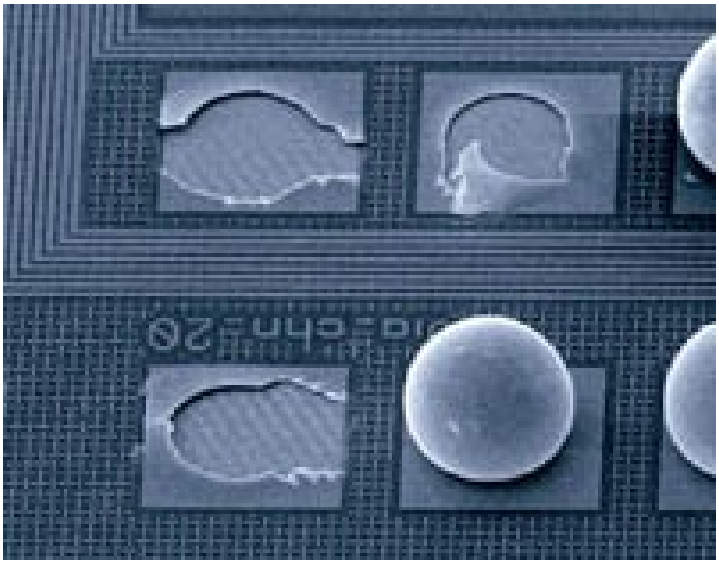


Figure 1.4: Illustration of delamination of chip pads under thermal-mechanical stress in the low-k interconnect systems [1.5].

1.1.2. Compliant Wafer-Level Chip I/O Interconnection

The ITRS suggests that wafer-level packaging (WLP) offers a promising solution to reduce packaging costs. In the past five years, many types of wafer-level packages have been developed, and they can be mainly divided into two categories: rigid types and compliant types. The rigid WLPs are essentially redistributed flip chips, which, therefore either require underfill or can only be used for low I/O count applications [1.21]. In contrast, the compliant WLPs use flexible links as the I/O interconnects, which can compensate for the CTE mismatch between the Si chip and organic substrate. Thus, a compliant WLP does not require underfill after assembly. In addition, the compliant WLPs provide another important advantage, especially for low-k IC packaging since the compliant I/O interconnects provide low-stress interfacing between the chip and substrate and thus reduce the impact of packaging and assembly processes on the low-k ILD.

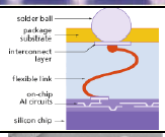
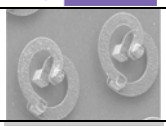
Table 1.1 lists several compliant WLP technologies that have been studied in recent years [1.22-1.33]. FormFactor's WOW^{TM} technology utilizes a wire-bonder to fabricate microsprings for WLPs and has shown good reliability [1.22]. However, wire bonding is inherently a serial operation and is time consuming for high I/O count applications. Tessera's WAVE^{TM} technology uses wafer-level batch fabrication, but involves transient-liquid-phase (TLP) Cu bonding and injection encapsulation processes at wafer level, which are not commonly available in back-end-of-line (BEOL) facilities [1.23]; The helix-type interconnects are monolithically fabricated [1.24, 1.25], but their process requires multiple electroplating steps and a long RIE etch-back process of the thick-film photoresist.

Compared to these compliant interconnect technologies, sea-of-leads (SoL) technology extends BEOL processes to provide high I/O density chip interconnection. The concept of SoL was developed by Bakir [1.28-1.33] based on Patel's work on a CWLP prototype [1.26, 1.27]. Substantial effort has been invested in developing processes and characterization [1.30 – 1.32]. In particular, a "slippery type" SoL promises to offer the maximum effective x-y compliance in that the restriction from adhesion with the polymer film can be eliminated since the leads are released [1.28, 1.30]. Such a SoL structure is essentially a MEMS interconnect that has spring-like behavior for high thermal mechanical reliability.

A simple method to release the leads is undercut etching the adhesion layer underneath the narrow portion of the electroplated leads. However, such a process involves wet etching, which requires careful design of the lead dimensions and a timed etching process to avoid detaching the leads from the chip pads. Another promising approach is to use a lift-off method with a sacrificial layer, which has a long history of use in fabricating MEMS structures such as cantilevers and actuators [1.34, 1.35]. Nevertheless, many technical issues in lead releasing,

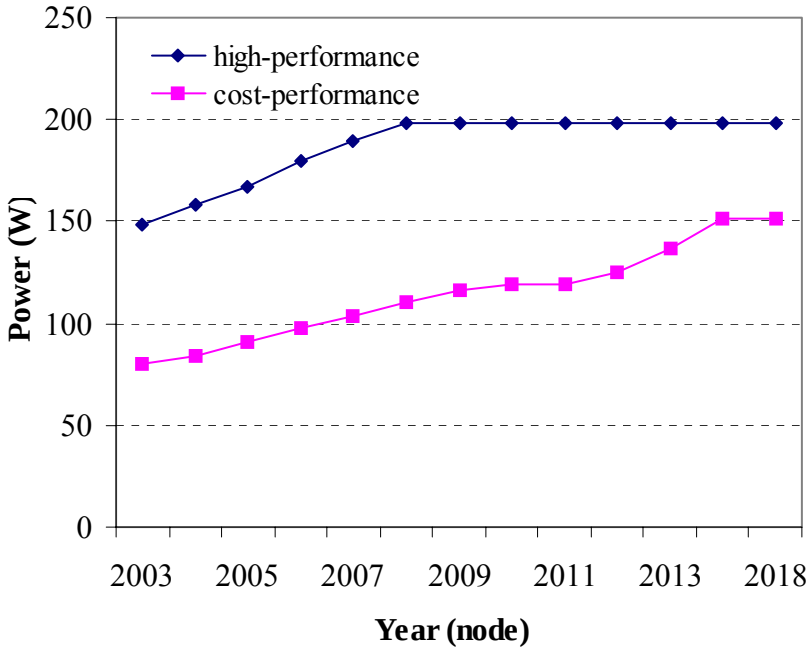
bumping, and assembly need to be investigated. A full set of manufacturable processes is yet to be developed and basic reliability performance should be assessed. In addition, the structural design guidelines need to be developed based on the trade-offs between mechanical compliance and electrical parasitic parameters for certain geometries or dimensions.

Table 1.1: Summary of various compliant chip I/O interconnect technologies [1.22-1.33].

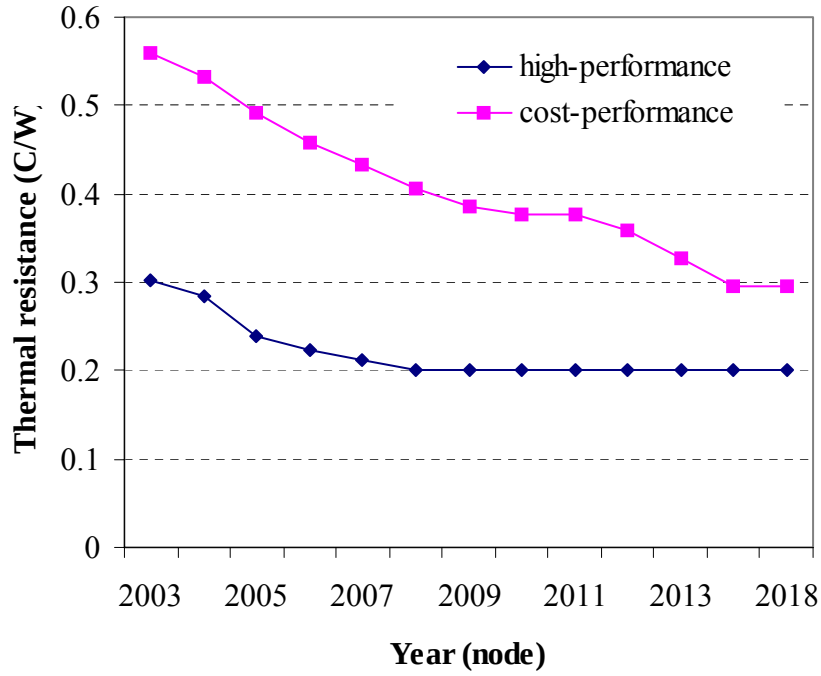
Technology and company name	Illustration	Attributes	Status	References
MOST® (Form Factor)		Au wire bonding technology Serial fabrication Pitch & size limited by tools	Commercial	[Novitsky et al. 2000]
µBGA® and WAVE® (Tessera)		TLP Cu bonding technolgy Batch fabrication Elastomer encapsulating	Commercial	[V. Solberg et al 2000]
β-Helix and G-Helix Interconnects (ME., GIT)		Lithographic batch fabrication Multi-layer free-standing structure	R&D	[Zhu et al. 2002 and 2003]
Sea-of-leads (SoL) Interconnects (ECE., GIT)		Lithographic batch fabrication CMOS compatible processes	R&D	[Patel et al. 2000] [Bakir et al. 2002 and 2003]

1.2. Advanced Chip Cooling

The heat generated by ICs must be removed by natural convection or enhanced convention. While natural convention is usually sufficient for low-power ICs, extra components, such as heat spreaders, heat sinks, and fans, are often necessary to cool the high-power ICs. The thermal resistance between a chip and the ambient is typically used as a metric for cooling technologies, which is defined as the ratio of the temperature difference to the amount of power that is removed. Figure 1.5 plots the ITRS projection of chip power, as well as the calculated junction-ambient thermal resistance for high-performance and cost-performance applications.



(a)



(b)

Figure 1.5: ITRS projection of (a) power dissipation (b) calculated thermal resistance (junction to ambient) of a single chip package for high performance and cost performance applications.

According to the ITRS, the power dissipation will reach 151 W and 198 W for cost performance and high-performance applications, respectively, in 2018. To keep the junction temperature below 85 °C in a local ambient of 45 °C, the required thermal resistance may be as low as 0.2 °C/W. However, the thermal resistance of typical air-cooled heat sinks is normally higher than 0.3 °C/W [1.36]. Meanwhile, the thermal resistance at the interfaces between the components in a conventional flip-chip package can account for a significant portion of its overall thermal resistance. Thus, a manufacturable packaging solution is not available to remove the high heat flux in future generation GSI chips using conventional air-cooled heat sinks.

In addition, the non-uniform power dissipation across a chip often results in hot spots, which exacerbate the cooling issues. Complex systems involving three-dimensional (3-D) and/or optical integration raise even more challenges in thermal management. For instance, stacking chips means higher power for the same footprint area. Optoelectronic devices, such as semiconductor lasers, are usually operated at a much higher power density than CMOS devices [1.37], and they have a much narrower tolerance for temperature variation because of the wavelength shift [1.38].

1.2.1. Limitations of Air-cooled Heat Sinks

Figure 1.6 illustrates a typical schematic of the air-cooled heat sink used in a flip-chip package. A large area is usually needed for a heat spreader and a high profile is required for the heat sink fins. With increasing power dissipation of the microprocessors, the necessary volume and the overall weight of the heat sink increases continuously to provide a larger overall heat exchanging surface area, which is becoming a major bottleneck in miniaturization of the high-performance microelectronic systems [1.39].

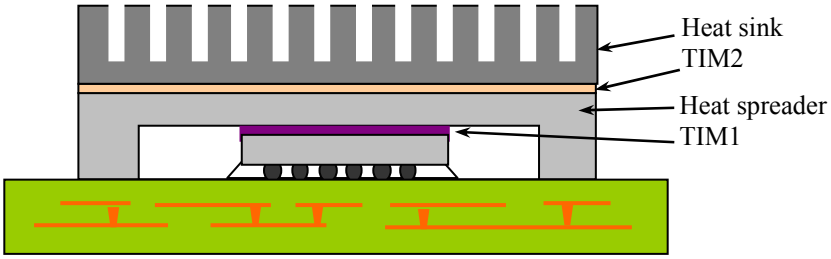


Figure 1.6: Schematic of a conventional forced-air heat sink for a typical flip-chip package.

The thermal resistance of the downward thermal paths (through the package substrate underneath a chip) is usually much higher than that of the upward thermal paths (through the heat sink above a chip) [1.11, 1.27]. Therefore, the overall thermal resistance R_{th} (ºC/W) is mainly dominated by the upward path and can be estimated as follows:

$$R_{th} \approx R_{Si} + R_{TIM} + R_{sp} + R_{\sin k} \tag{1.1}$$

where R_{Si}, R_{TIM}, R_{sp}, and R_{sink} are the thermal resistance (ºC/W) of the Si chip itself; the thermal interface materials (TIMs), the heat spreader, and the heat sink with fins.

Table 1.2 summarizes the material properties and the typical thermal resistance values for the components that are commonly present in the upward thermal path for a flip-chip package. Because of its large thermal conductivity and small thickness, the thermal resistance of the Si chip is usually small (R_{chip}~0.01 ºC/W) because of its small thickness (t_{chip}~ 7×10^{-4}m) and a relatively large thermal conductivity (k_{Si}~150 W/ºC-m). A heat spreader is normally a solid metal plate (typically Al or Cu), which is critical for spreading the heat flux from a small chip area, A_{chip} (m^2), to a relatively larger area (A_{sp}> $9\times A_{chip}$). A heat sink consists of a structure made of multiple high-aspect ratio fins that provide a large area for heat dissipation into air. A fan is usually used to improve the air flow velocity around the heat sink area. The thermal resistance of a heat sink is determined by its convective heat transfer coefficient, h_{conv} (W/ºC-m^2), and the heat

exchanging area of the fins, A_{fins} (m^2). In addition, suitable thermal interface materials (TIMs) must be carefully selected. A small thickness of the TIMs, t_{TIM} (m), and a large thermal conductivity, k_{TIM} (W/ºC-m), are critical for a low thermal resistance at the interfaces between components. Otherwise, the interfacial thermal resistance may account for a large portion of the overall thermal resistance.

Table 1.2: Summary of the thermal resistance of the components in a typical flip-chip package for microprocessors [1.11, 1.27, 1.36, 1.39-1.42].

Component	**Materials**	**Thermal conductivity *k* (W/ºC-m)**	**Thermal resistance (ºC/W)**	
			Expression	**Typical value**
Chip	Si	150	$R_{chip}=t_{chip}/(k_{Si}\times A_{chip})$	~0.01
Heat Spreader	Al	210	$R_{spreader}=t_{sp}/(k_{sp}\times A_{sp})$	~0.1
	Cu	400		
	SiC	120-300		
	Diamond	1200		
Heat Sink with Fins	Al	210	$R_{conv}=1/(h_{conv}\times A_{fins})$	~0.3
	Cu	400		
Thermal Interface Material (TIMs)	Grease	3-5	$R_{TIM}=t_{TIM}/(k_{TIM}\times A_{TIM})$	~0.1
	Gel	3-4		
	Phase change film (PCM)	0.5-5		
	Solder	30-50		

Conventional TIMs that are suitable for IC packages include various types of thermal greases. Although these materials are readily available, there are many issues involved in their selection, such as thermal resistance at low contact pressure and performance degradation

because of "pump-out" or "dry-out" during operation. Gel-like TIMs suffer from fewer concerns with degradation, but the problem of messy assembly remains [1.11]. Phase change materials (PCM) and low melting temperature solder alloys represent the latest TIM technologies [1.11, 1.39]. These materials behave like liquids at the operating temperature and can fill the air gaps at the interfaces, which provides a minimum effective thickness by allowing the mating surfaces to come into contact [1.11]. Nevertheless, a considerable pressure (up to tens of psi) must be maintained in order to ensure a low contact thermal resistance between components no matter which type of TIM is used. Taking into account all the components, the overall thermal resistance of an air-cooled flip-chip package can be much higher than the required thermal resistance projected by the ITRS for future generation ICs. In summary, the fundamental barriers to heat dissipation in conventional flip-chip packages mainly arise from physical limits of the forced-air heat transfer mechanism, material properties of the heat spreader, and imperfect thermal interfaces between the components [1.10, 1.11]. Therefore, novel cooling mechanisms and packaging approaches are urgently needed.

1.2.2. Liquid Cooling and Microfluidic Heat Sinks

Gurrum et al. [1.36] estimated the achievable convection thermal resistance, R_{conv} (ºC/W), as a function of heat transfer coefficient, h_{conv} (W/ºC-m^2), based on pure convection for various cooling mechanisms by the following equation:

$$R_{conv} = 1/(h_{conv} \cdot A) \tag{1.2}$$

where A (m^2) represents the heat exchanging area.

As shown in Figure 1.7, single-phase liquid cooling or two-phase liquid cooling can offer heat transfer coefficients that are two orders of magnitude higher than what is achievable with air-cooling mechanisms. The low thermal resistance projected by the ITRS for the cost-

performance and high-performance single chip packages in 2018 will only be possible if single-phase or two-phase liquid cooling is used [1.3]. Liquid cooling further promises to enable operations at lower temperatures, which would be beneficial to the computing performance of most systems simply due to the increased charge carrier mobility of the semiconductors, decreased electrical resistance, and improved electromigration lifetime for the interconnects [1.12].

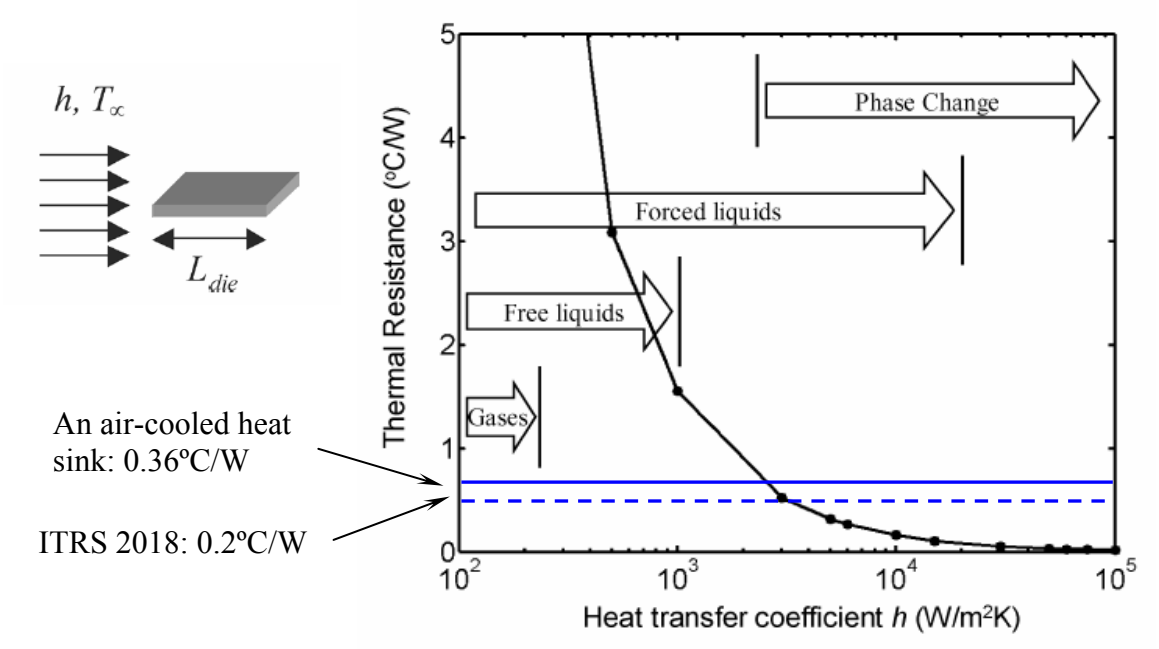
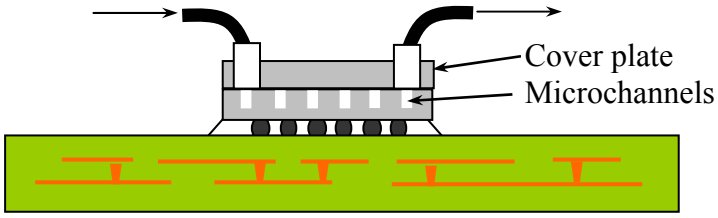


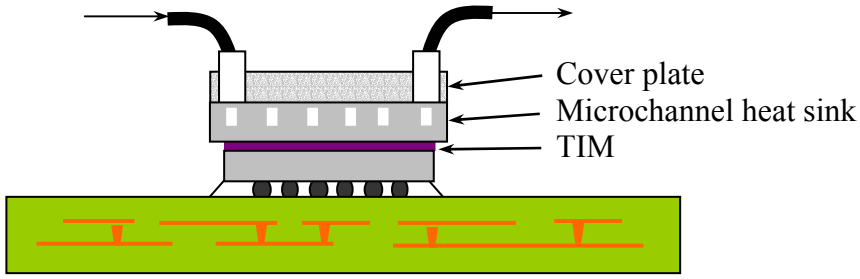
Figure 1.7: Plot of achievable thermal resistance as a function of heat transfer coefficient for the forced air, free liquid cooling, forced liquid cooling and phase-change cooling [1.36]. (The blue solid line represents the thermal-resistance of a typical forced air-cooled heat sink and the blue dotted line represents the ITRS projection for a high-performance chip in 2018 [1.3])

Many liquid cooling approaches have already been employed to cool chips. For example, the electronic chips may be directly immersed in a pool of inert dielectric liquid [1.43]. Other examples include the thermosyphons and heat pipes, where a liquid evaporates with applied heat and condenses elsewhere, in a closed system, to dissipate that heat [1.44, 1.45]. These techniques

are usually bulky and are inherently unsuitable for today's compact, and highly integrated systems. In contrast, it is well-known that microfluidic heat transfer can provide exceptionally high heat transfer efficiencies and low thermal resistances [1.9, 1.36]. In 1982, Tuckerman and Pease [1.9] first studied a microchannel heat sink directly integrated into a Si chip, demonstrating that a heat flux as high as 790 W/cm^2 can be removed and a thermal resistance as low as 0.09 °C/W can be achieved with single-phase liquid cooling. Since then, microfluidic heat sinks have been extensively studied [1.46-1.49].



(a)



(b)

Figure 1.8: Schematic of typical microchannel heat sinks in literature (a) the microchannel heat sink is integrated as part of a Si chip [1.9, 1.48] (b) the microchannel heat sink is fabricated separately and attached onto the back side of a chip with a TIM [1.46, 1.49].

As illustrated in Figure 1.8(a), with on-chip microfluidic access, direct hot spot cooling becomes possible since all the thermal interfaces are eliminated. An integrated microfluidic heat sink can also significantly reduce the IC package area and space, which is desirable for the rapidly growing applications of multi-chip and 3-D integration [1.50, 1.51]. Because of these

benefits, microfluidic cooling has recently received increasing interest from major semiconductor manufacturers including Intel and IBM [1.52, 1.53]. However, many technical challenges still remain. For example, in conventional fabrication methods for microchannels, the deep trenches are enclosed by direct wafer bonding (glass or Si), which requires ultra smooth/clean bonding interfaces, high pressure, and high temperature (350 ºC~1000 ºC) and/or high voltage (500 V~1000 V) [1.54, 1.55]. These processing conditions are not very friendly to CMOS wafers. As a result, most microchannel heat sinks that have been reported in literature [1.46, 1.49] are fabricated separately and attached on the back side of a chip, as shown in Figure 1.8(b). Using this approach, the high-performance TIMs are still a limiting factor [1.49].

Another challenge of using a back-side microchannel heat sink is associated with the fluidic interconnection, because compatible fluidic paths are not available in conventional IC packages. While it is relatively easy to manually connect two tubes at the back side of a single chip, the fluidic interconnection of multi chip packages can be a significant challenge, as illustrated in Figure 1.9. Therefore, an integrated packaging scheme with thermal-fluidic interconnection capabilities is needed.

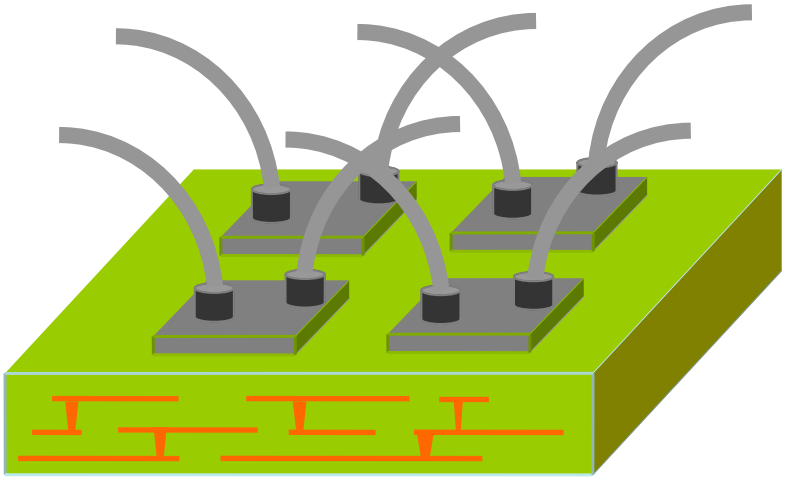
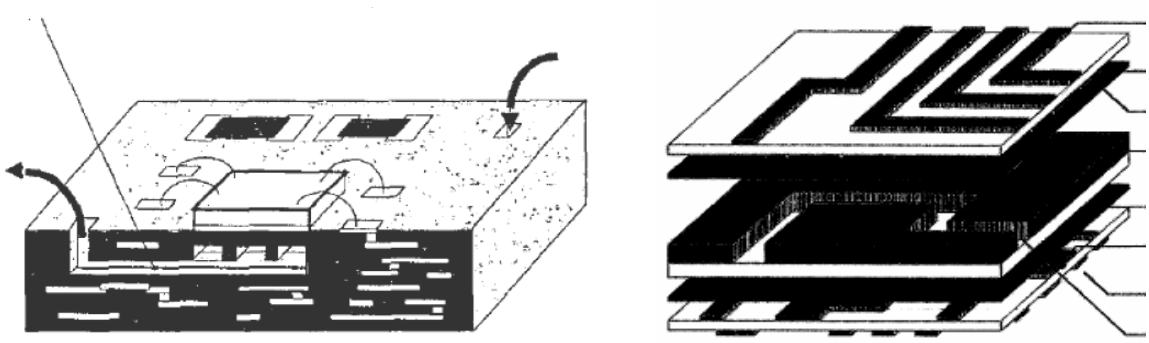


Figure 1.9: The conceived schematic for a multi chip system with the chip-level liquid cooled heat sink and individual tubing at the back side of each chip.

1.2.3. Opportunity of the Integrated Thermal-fluidic Packaging

In addition to the liquid cooling at the back side of a chip, board-level liquid cooling has also been studied [1.50, 1.56, 1.57]. As shown in Figure 1.10(a), Bauer et al. [1.56] described a concept of integrating a channel system directly into the ceramic multilayer wiring board based on low-temperature co-fired ceramic technology (LTCC). With such a module, dissipation of a heat flux of 50W/cm^2 from the chip area to a remote heat sink has been demonstrated. Ilgen [1.58] further reported a fabrication method for thermal-fluidic channels based on the low-cost FR-4 organic laminate technology, as illustrated in Figure 1.10(b). These technologies are especially useful to reduce the necessary heat sink space above the packages.



(a) (b)

Figure 1.10: Examples of board-level fluidic channels for heat dissipation: (a) thermal-fluidic channels in LTCC board [1.56] and (b) thermal-fluidic channels in FR-4 organic board [1.58].

Meanwhile, the use of novel micro-pumping technologies such as electro-kinetic pumps [1.59, 1.60] offers the opportunity of compact pumps integrated directly within the printed wiring boards. While these technologies are helpful for cooling the substrates to a certain extent, the thermal resistance of most board materials is intrinsically high, particularly for the low-cost organic boards. An on-chip microchannel heat sink is still necessary for effective direct cooling

of the high power chips. Considering these technologies, there is an opportunity to implement an integrated thermal-fluidic packaging scheme that utilizes both chip-level and board-level cooling systems. Several key technologies should be developed to enable compact packaging of GSI chips with thermal-fluidic heat dissipation capabilities. Low-temperature CMOS compatible processes are needed for on-chip microchannels. Novel thermal-fluidic chip I/O interconnects and compatible assembly approaches are required for the massive fluidic interconnection with board-level fluidic systems.

1.3. Integrated Electrical, Optical and Thermal-fluidic I/O Interconnections

Another concern at the chip-package interface is the off-chip communication bandwidth. According to the ITRS projections, the off-chip frequency will reach 56.8 GHz in 2018 [1.3], which poses a significant challenge for electrical I/O interconnection because of increased levels of cross-talk and signal loss [1.2]. Optical interconnection offers a promising solution, with higher I/O bandwidth, smaller global delay, lower crosstalk, and better clock distribution [1.64-1.66]. A great deal of progress has been achieved in the integration of novel optoelectronic devices and optical waveguides in recent years. For instance, SiGe-based photodetectors and III-V compound semiconductor VCSEL arrays can be used for high speed optical clock distribution to reduce jitter and skew [1.64]. Polymer-based planar waveguide technologies, along with the use of mirror-based or grating-based couplers, will enable interconnection of these optical components at low cost [1.65]. Monolithic [1.66], heterogeneous [1.67], or polylithic [1.68] integration approaches may be used. Nevertheless, high-density area array optical interconnection is still a major challenge because of the difficulties of alignment, coupling, and assembly [1.3]. The sea-of-polymer-pillars (SoPP) technology developed by Bakir [1.69-1.74] offers a feasible means to overcome these issues. Using either air cladding or metal coating, the

polymer pillar based interconnects act as surface-normal optical waveguides as well as electrical pins, as shown in Figure 1.11. The compliant nature of the low-modulus polymer facilitates a low-stress interconnection between the chip and package substrate. The fabrication of polymer pillars is a low-temperature wafer-level batch operation, involving only spin coating of the polymer film, soft baking, UV exposure through a mask, hard baking and spray developing. The optical transmission properties of the polymer pillars [1.69] and process integration of polymers on optical devices such as photodectors [1.72] and slant mirrors [1.71] have been reported. The potential I/O density of SoPP exceeds 10^5 /cm^2.

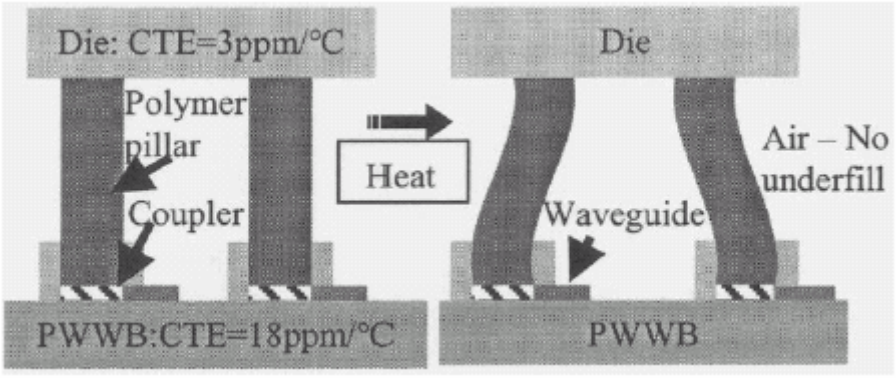


Figure 1.11: Schematic illustrating how the polymer pillars compensate for the CTE mismatch between the board and the die and maintain optical alignment during thermal cycling [1.71].

In particular, when coated with metal cladding, the polymer pillars can deliver simultaneous electrical and optical signals, which represents the highest integration level of electrical and optical I/O interconnects [1.73, 1.74]. However, the corresponding fabrication and assembly techniques must be investigated more thoroughly before this novel interconnection approach can be implemented. Furthermore, as discussed previously, effective cooling

techniques for future generation high power chips may require the use of on-chip microfluidic heat sinks, which means that compatible and highly integrated electrical, optical and thermal-fluidic I/O interconnects must be developed and explored for GSI chips.

1.4. Summary of Research Goals

The objective of this research is to develop a set of integrated I/O interconnection and packaging technologies for future GSI chips with high performance, high I/O count, and high power dissipation. To eliminate the need for underfill and reduce the impact of packaging on the fragile Cu/low-k ILD system, the MEMS-based sea-of-leads (SoL) compliant interconnects are studied through fabrication, process integration, and assembly. Preliminary reliability testing and failure analysis are performed and optimal design guidelines are developed for SoL interconnects based on 3-D finite element modeling (FEM) and numerical analysis. To provide high heat dissipation capabilities with micro-scale transport, novel low-temperature CMOS compatible processes and chip-board thermal-fluidic I/O interconnects are developed to enable chip-scale cooling schemes. To provide simultaneous electrical and optical interconnections, the process integration and assembly of dual-mode polymer pillar-based interconnects are demonstrated. The resulting technologies will ultimately enable wafer-level packaging of GSI chips with integrated electrical, thermal-fluidic, and optical I/O interconnections.

1.5. Organization of the Dissertation

The organization of the research in this thesis is described as follows:

- Chapter 2 describes the results in fabrication, assembly, reliability testing, and failure analysis of the MEMS-based SoL I/O interconnects for compliant electrical interconnection.

- Chapter 3 discusses the modeling and simulation results for characterization and optimization of the structural design for the SoL interconnects.
- Chapter 4 primarily describes the low-temperature CMOS compatible methods for fabricating on-chip microchannel heat sinks, the concept of integrated thermal-fluidic I/O interconnects, the prototype chip-scale thermal-fluidic I/O configurations, and assembly methods.
- Chapter 5 discusses thermal/fluidic analysis and testing results of the on-chip microhannel heat sinks, and the hydraulic requirements for meeting the ITRS projected heat dissipation needs.
- Chapter 6 presents the fabrication, assembly and testing results of the "dual-mode" polymer pillars as highly integrated electrical and optical interconnects. Then the integrated electrical, optical, thermal-fluidic I/O interconnects are presented based on the polymer pillar technology. The integrated I/O interconnections are identified as the enabling packaging technologies for the future generation GSI chips.
- Chapter 7 presents the conclusion and future work.

Chapter 2. Implementation of the MEMS-based Sea-of-Leads Interconnects

2.1. Introduction

In most wafer-level packaging technologies, the chip I/O interconnects are usually built onto/through a polymer elastomer, which acts as a stress buffer layer. Thus, the compliance of these interconnects is mainly determined by the mechanical property of the polymer elastomer since the interconnects are mechanically coupled with it. In contrast, the MEMS-based SoL interconnects are partially released from the surface of the wafer, thus, mechanically decoupling the deformation of the chip and the package substrate. However, there are many fabrication and integration issues associated with the "free-standing" nature of the MEMS-based interconnects.

This chapter will first describe two methods to produce MEMS-based SoL interconnects. In addition, the fabrication processes of SoL are reconciled with back-end-of-the-line (BEOL) processes for the integration with two conventional wafer bumping approaches: the masked evaporation (collaboration with IBM) and the electroplating through photolithography. The fabrication methods represent an extension of the previous work of Bakir [2.1, 2.2] on the so-called "partially slippery SoL." In addition, technology feasibility of the SoL MEMS interconnects is demonstrated through a full procedure of integration, assembly, thermal-mechanical reliability testing, and failure analysis.

2.2. Integration of the MEMS-based SoL with an IBM Bumping Process

Since SoL compliant interconnection technology was reported, it has received interest from major semiconductor manufactures such as Intel and IBM. In the past, integration of "non-slippery" SoL interconnects with an Intel chip has been investigated and reported [2.3, 2.4], with

focus on the fabrication and bumping of non-released leads. In this work, process integration of the MEMS-based SoL with an IBM bumping processes was studied.

2.2.1. Lead Releasing by Undercut of the Adhesion Layer

A simple process to release the electroplated metallic interconnects is to undercut the adhesion layer underneath the structure, as indicated in [2.1]. Figure 2.1 illustrates this concept. An etch window opening is first defined by photoresist to control the etching area. The undercut then proceeds through the window, as indicated by the arrows. Due to the isotropic nature of wet etching, the undercut will exceed the area of the etch window. If the etching reaches the anchoring point of a lead, its adhesion with the pad will be affected and the whole lead may be detached from the substrate. A destructive "peeling" test with a sharp probe needle was performed under a microscope, which can reveal whether a lead has been successfully released.

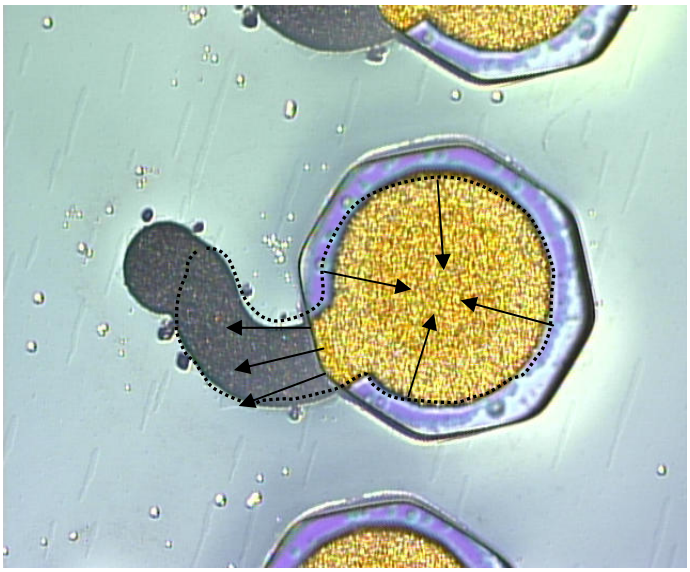
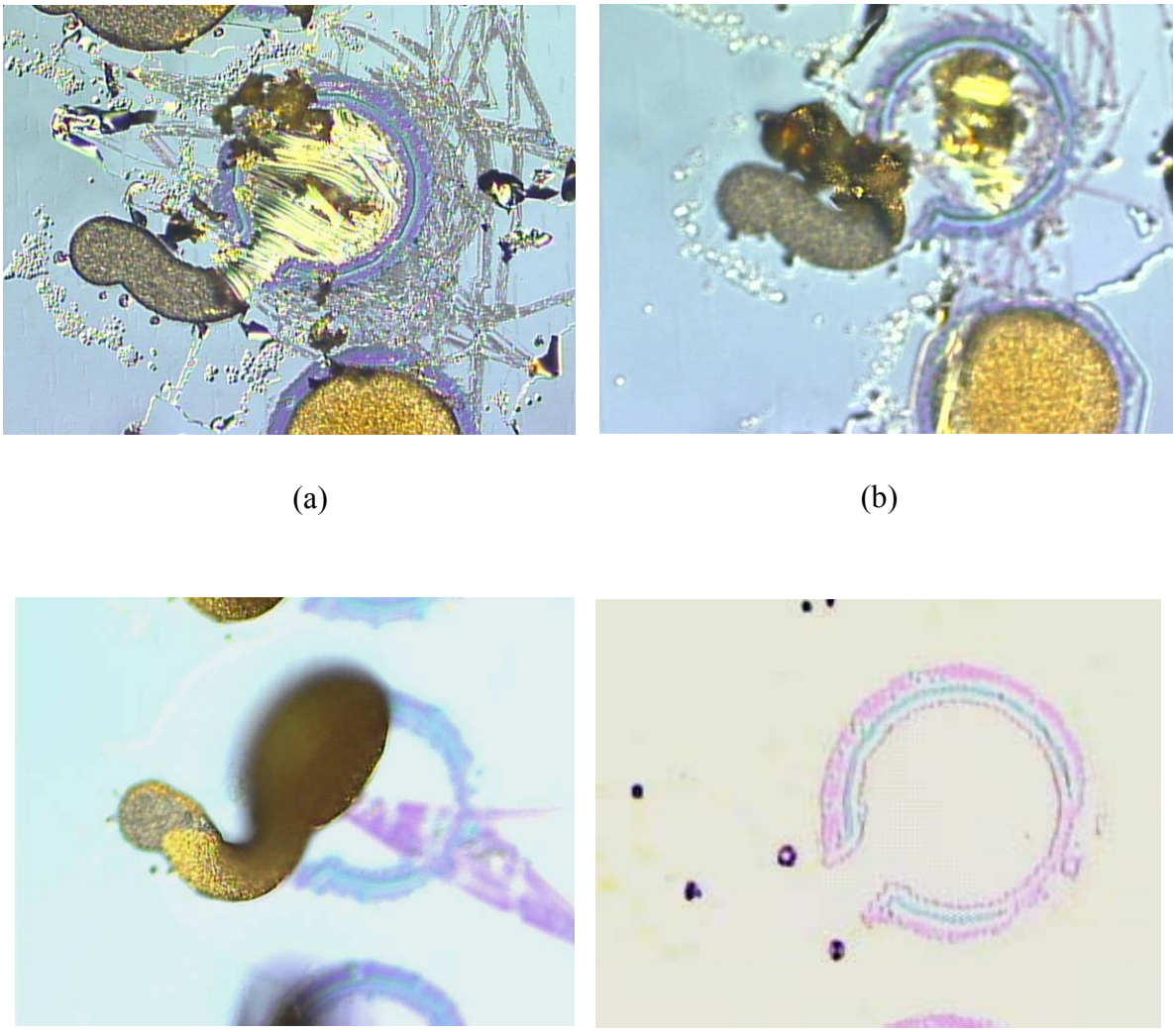


Figure 2.1: Optical micrograph of the electroplated metal leads to be released by controlled undercut etching: an etch window is defined by photoresist to control the undercut progress.

Figure 2.2 shows optical micrographs of the scratched leads that are in various conditions including (a) non-etching, (b) non-uniform etching, (c) good etching, and (c) lead detaching due to over-etching.



(a) (b)

(c) (d)

Figure 2.2: Optical micrographs of the electroplated metal leads in various conditions (a) leads can not be peeled without enough undercut etching, (b) leads are not released because of non-uniform undercut etching, (c) successful releasing resulted from a good undercut etching, (d) detaching due to the over-etching.

In this study, the adhesion (seed) layer for the electroplated leads is Ti/Cu/Ti (300Å/2000Å/300Å). In order to release the leads, the Cu film is undercut and an Al etchant (type A) was used as the Cu etchant since it is a readily available commercial product. However, it was known that the etching rate and uniformity of most etchants significantly depend on the temperature. Thus, experiments were conducted to establish optimal etching conditions such as temperature and time as summarized in Table 2.1.

Table 2.1: Summary of the results of Cu undercut etching experiments with Al etchant (type A) at various temperatures for different etching time.

<table>
<tr><td rowspan="2">25 °C</td><td>15mins</td><td>30mins</td><td>45mins</td><td>60mins</td><td>90mins</td><td>180mins</td></tr>
<tr><td>No peeling</td><td>No peeling</td><td>No peeling</td><td>No peeling</td><td>No peeling</td><td>No peeling</td></tr>
<tr><td rowspan="2">50 °C</td><td>15mins</td><td>30 mins</td><td colspan="2">45mins</td><td colspan="2">60mins</td></tr>
<tr><td>No peeling</td><td>No peeling</td><td colspan="2">Most leads can be partially peeled up;7 Leads missing</td><td colspan="2">Most leads can be partially peeled up;9 Leads missing</td></tr>
<tr><td rowspan="2">58 °C</td><td>15mins</td><td colspan="3">30 mins</td><td colspan="2">60mins</td></tr>
<tr><td>—</td><td colspan="3">All leads can be peeled up; none of the leads is missing</td><td colspan="2">—</td></tr>
</table>

During the experiments, large dice (2 cm× 2 cm) with electroplated leads were put in the agitated Al etchant at various temperatures for various lengths of etching time. At 25 ºC, the undercut etching is very slow, and none of the leads could be peeled up even after 180 mins. At 50 ºC, while the etching rate is increased, etching uniformity is not good enough and an optimal etching time could not be determined for lead releasing without detaching any of the leads. At 58 ºC, both etching rate and uniformity are improved and all the leads can be peeled up after 30mins without detaching of any leads.

In practice, uniform undercut etching across a whole wafer is more challenging. Some other chemicals that are usually used at room temperature, such as the diluted nitric acid, can

eliminate the need for temperature control. In addition, a paddle cell should be used to provide continuous and uniform agitation for a large wafer.

2.2.2. Integration with Wafer Bumping Processes through Masked Evaporation

For assembly of a chip onto a next-level package substrate, a controlled amount of solder must be deposited onto the metal leads through bumping processes. Evaporation through a Molybdenum (Mo) mask is a conventional method to bump a wafer, as it is simple and has a long history of use [2.5].

Figure 2.3 shows the bumping process flow for the SoL interconnects. Upon completion of the lead releasing (Figure 2.3a), a standard BLM (Bump Level Metallurgy) or namely Under Bump Metallurgy (UBM) layer is first deposited onto the end of the leads by evaporation through a Mo mask (Figure 2.3b). A layer of Ti/SiO_2 (1000Å/1000Å) is then deposited as a barrier for the C4 solder bumps. The Ti layer is deposited by DC sputter and the SiO_2 layer is deposited by PECVD. The Ti/SiO_2 layers are patterned and etched in a ring shape to confine the C4 land (Figure 2.3c). A layer of electroless Ni/Au is then coated above the BLM as a good wetting base for the C4 bumps (Figure 2.3d). The next step is to deposit C4 solder bumps through another masked evaporation step (Figure 2.3e). Finally, the C4 solder bumps will be reflowed to form the solder ball in spherical shape (Figure 2.3f).

During the experiments, a technical issue associated with the masked evaporation approach was discovered and illustrated in Figure 2.4. After evaporation, the C4 solder bump is still in contact with the Mo mask. As a result, when the Mo mask is separated from the wafer, some of the leads are easily deformed and damaged because the leads have been released before the bumping processes (Figure 2.5).

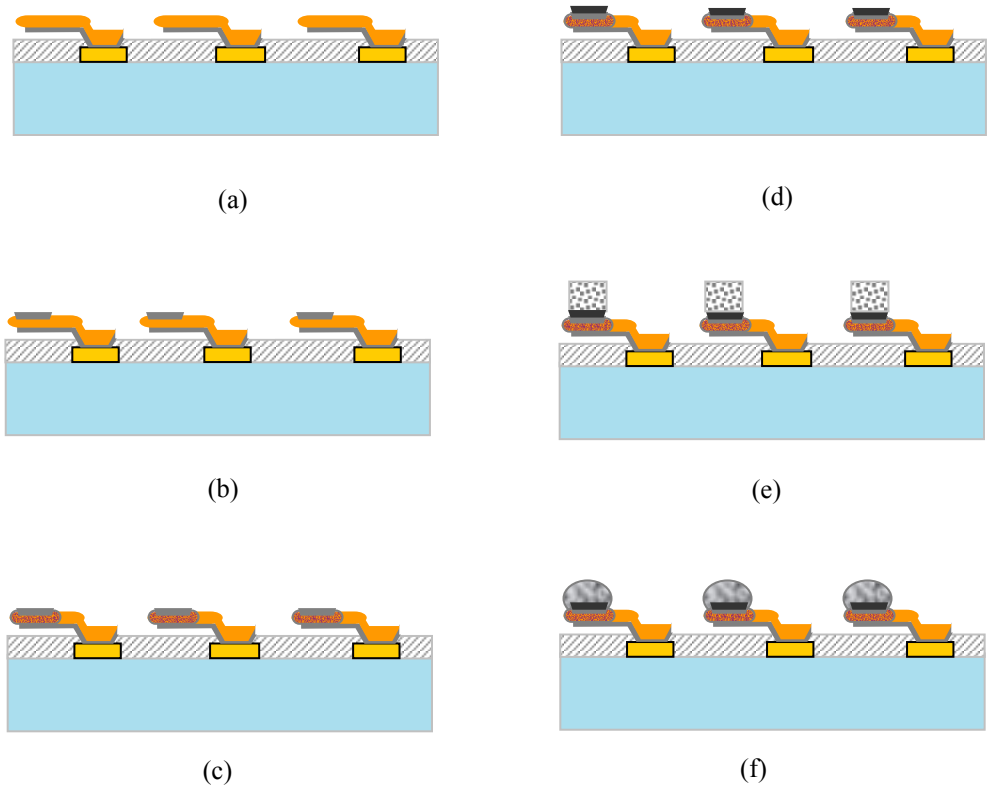


Figure 2.3: Schematic of the process integration with evaporation wafer bumping processes after lead releasing: (a) Begins with the released leads, (b) Deposit BLM through evaporation, (c) Deposit and pattern the Ti/SiO_2 ring, (d) Electroless plating of Ni/Au, (e) Deposit C4 bumps through evaporation, (f) Solder reflow

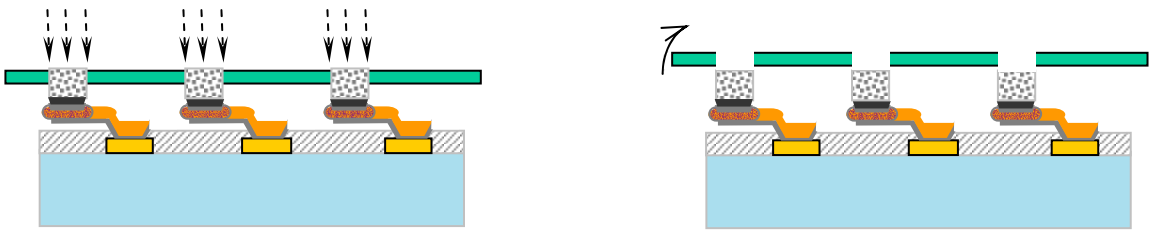


Figure 2.4: Illustration of the mask removal issue for the C4 bump evaporation processes.

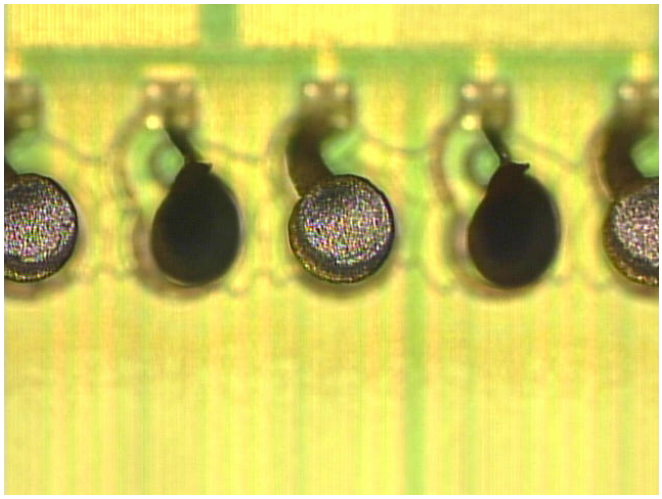


Figure 2.5: Optical micrograph of the damaged leads caused by the Mo mask

To avoid this problem, a “release last” approach has been proposed during the research collaboration with IBM. The sequence of the steps in the process flow can be simply altered such that the leads are bumped before they are released. By this means, the leads are not flexible during the bumping operation and will not be damaged. Upon completion of the bumping processes, the under etching is performed to release the leads, as describe above. Nevertheless, the releasing method by undercut etching requires a careful design of the lead dimensions and a timed etching process to avoid detaching the leads from the chip pads. In practice, precise control of the wet etching undercut rate across a Si wafer is difficult, especially when a Si wafer moves into the 300 mm regime.

Thus, the fabrication processes of the MEMS type SoL should be reconciled for alternative manufacturing approaches. For instance, the MEMS leads may be released in a better controlled manner and different bumping processes may be used. Next section will discuss the lead releasing by a sacrificial layer method and the lead bumping through an electroplating method.

2.3. Process Reconciling for the Processes with a Sacrificial Layer Method and Electroplating Wafer Bumping

When the leads are released through undercut wet etching in the previous section, over-etching can not be completely avoided and it can result in poor adhesion between a lead with the surface of a chip pad. As illustrated in Figure 2.6, such a lead can be easily detached and the manufacturing yield may be reduced. In contrast, a "lift-off" method with a patterned sacrificial layer can offer an effective solution to the lead releasing. As for the C4 solder bumping, electroplating is becoming more popular in the semiconductor industry because it is more cost-effective than evaporation for fine pitch applications with high volume manufacturing [2.5, 2.6]. Therefore, the fabrication processes of the SoL MEMS interconnects must be reconciled for wafer bumping by electroplating approaches.

2.3.1. Lead Releasing by a Sacrificial Layer

Sacrificial films are commonly used for fabricating MEMS structures such as cantilevers and actuators as illustrated in Figure 2.7 [2.7, 2.8]. The key to a successful releasing with a high manufacturing yield is the easy removal of the sacrificial film without damaging the wanted structures after the process is completed.

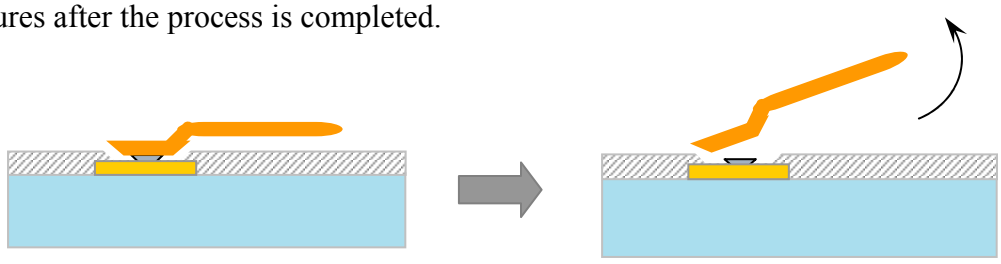


Figure 2.6: Illustration of the lead detaching problem with undercut wet etching approaches. (wet etching undercuts the anchoring portion of a lead)

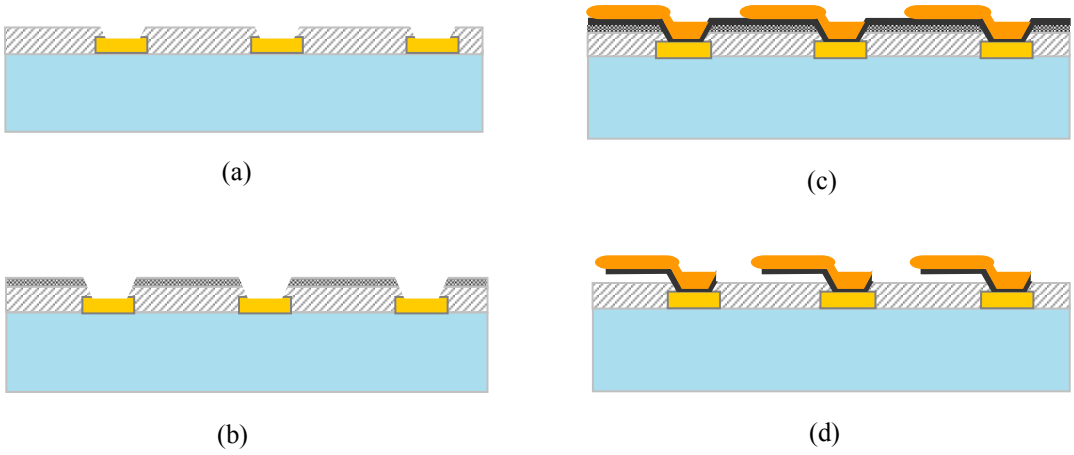


Figure 2.7: Illustration of lead releasing with a sacrificial layer (since the adhesion layer is not affect during releasing step, lead detaching is not a problem)

In this work, three types of sacrificial materials were investigated, as summarized in Table 2.2. They are thin-film Al layer, photoresist, and thermally decomposable polymer material such as polycarbonate (PC) [2.9]. Various removal methods are needed for the different sacrificial materials including selective etching, dissolving with solvents, or heat treatment.

Table 2.2: Summary of the sacrificial materials for lead releasing

Sacrificial Material	**Al thin film**	**Photoresist (Shipley 1827)**	**Decomposable Polymer (Unity 200)**
Deposition method	DC Sputtering, Evaporation etc.	Spin coating	Spin-coating
Removal method	Selective etching with diluted NaOH	Dissolving with solvents or stripper	Heat treatment at ~170ºC~200ºC

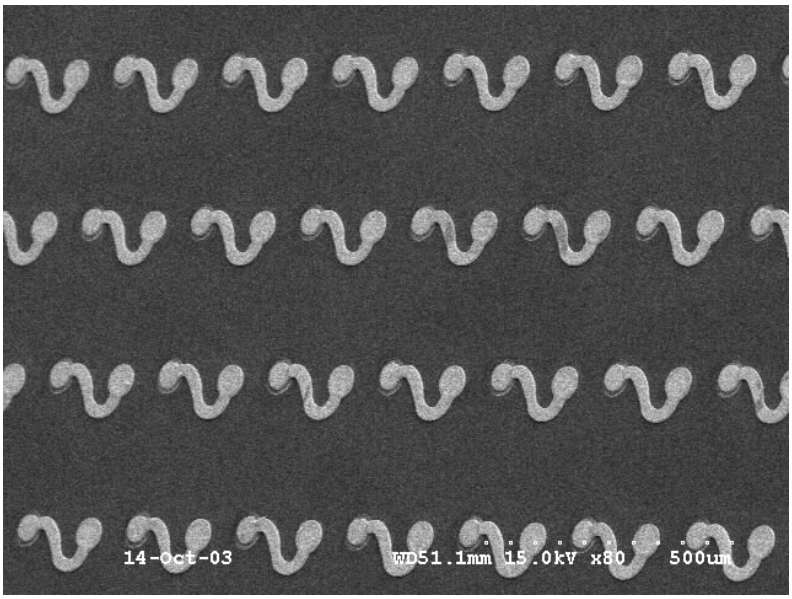
The thin film Al can be deposited by DC sputtering or evaporation and it can be selectively etched by diluted NaOH solution (wt. 10%), which is fairly benign to the electroplated leads (Au or Cu) and their underneath adhesion layer (the Ti/Cu/Ti stack).

Experiments show that it takes approximately 30 mins to complete the selective etching of Al film (~2 μm thick) in the lateral direction (undercut for a distance of 40 μm).

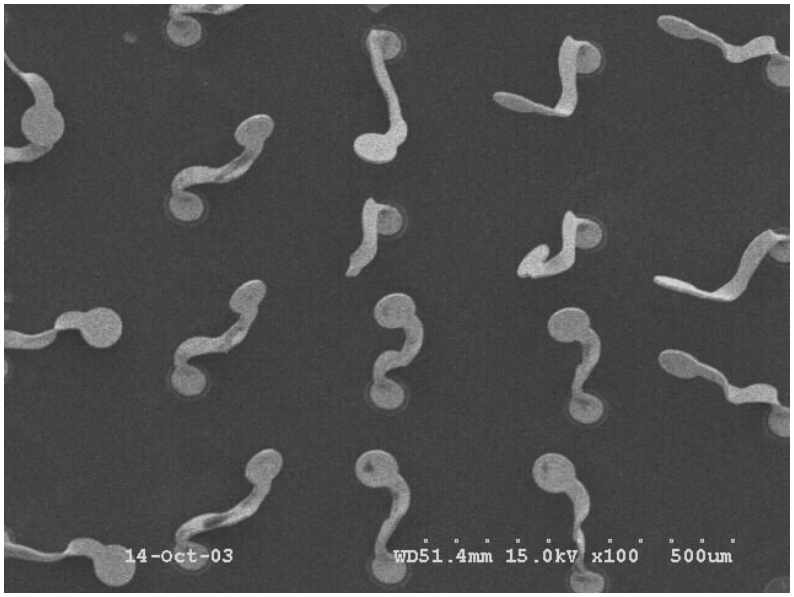
When a photoresist is used as the sacrificial layer, it can be easily removed by solvents or dedicated remover solution. The releasing process takes less than 20 min. Since several photolithographic processing steps are needed following the deposition of the sacrificial layer, a photoresist must be carefully selected as a sacrificial layer. Otherwise, it may seriously deform during the following lithographic steps. In this work, a 2 μm thick Shipley 1827 photoresist was deposited at a spin speed of 3000 rpm. After it was developed, an extra long hard-bake (~10 mins) was performed at 120ºC to ensure that it is well cured before the seed layer is applied. Otherwise, potential out-gassing or deformation may occur in its following processing steps.

The third type of sacrificial material is a low-temperature decomposable polymer, Unity 200P (Promerus LLC.). It can be spin-coated and photodefined with deep UV. Isopropanol (IPA) solution was used as the developing and cleaning agent [2.9]. After the fabrication processes of the SoL interconnects are completed and the seed layer is removed, Unity 200P can be decomposed at 170ºC in a N_2 purged oven.

Once the sacrificial layer is removed, the electroplated metallic interconnects are partially released from the surface of the wafer and become mechanically compliant. A destructive peeling test has been performed to confirm success of the releasing process. Figure 2.8(a) is SEM photograph of metal leads after removal of the sacrificial layer. Figure 2.8(b) shows the SEM micrographfor an area tested with an adhesive tape, which clearly indicates that the metal leads have been released from the underlying passivation surface. Most importantly, none of the leads were detached because the via end of the leads is still well anchored at the chip pads.



(a)



(b)

Figure 2.8: SEM photograph of MEMS leads after the release process: (a) metal leads after removal of sacrificial layer and (b) an area after destructive peeling test with an adhesive tape, which clearly confirms that leads are flexible but well-anchored.

2.3.2. Integration with Wafer Bumping Process by Electroplating

Based on the above approach, the integration of the SoL MEMS interconnects with BEOL processes has been reconciled during a wafer-level packaging procedure. Figure 2.9 shows an optical micrograph of the on-chip interconnects that were used to mimic the top interconnect layers in BEOL wafers. The test pads were designed in a way to form daisy chains when cascaded with board-level interconnects. The Ti/Cu (300Å/5000Å) pads were deposited using a DC-sputter and the SiO_2 passivation film (5000 Å) was deposited with PECVD at 250°C. The vias were etched by Buffered Oxide Etchant (6:1).

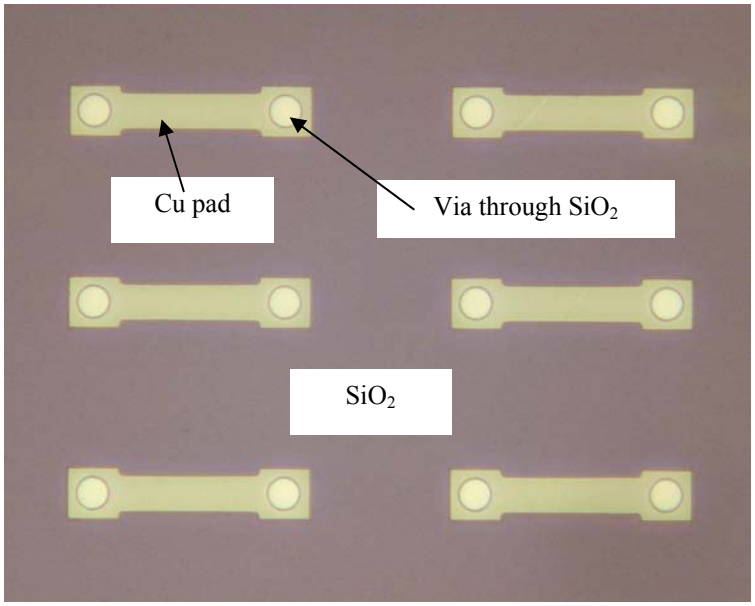


Figure 2.9: Optical photograph of the on-chip interconnects, which include Cu pads covered by SiO2 passivation. The vias have a diameter of 50μm and a pitch of 325μm.

As illustrated in Figure 2.10, the overall process flow is designed to be compatible with wafer bumping by electroplating and only requires three additional masking steps compared to standard C4 bumping processes. A sacrificial layer was first deposited and patterned with the via mask (Figure 2.10b). After the via is cleaned by acid, the wafer is dried and a seed layer of Ti/Cu

(300Å/2000Å) was immediately deposited (Figure 2.10c), which provides electrical continuity across a wafer. If the seed layer Cu layer is left exposed to air for too long, the metal pad surface (Cu) inside the vias can be oxidized thereby degrading the adhesion. Metal leads were then electroplated in a photoresist mold (NR9-8000, Futurrex, Inc.) defined by another masking step (Figure 2.10d). In this work, Au leads were used for a better corrosion resistance and fatigue resistance compared to other metal such as Cu and Ni. The seed layer also acts as a strong adhesion layer between the electroplated leads and the underneath pads. A solder barrier/dam was then deposited over the metal leads and patterned such that it does not restrict the displacement of the leads (Figure 2.10e). After that, a thicker photoresist is used to define the bump area at the end of each lead. At a spin speed of 750 rpm, a 35 μm thick NR9-8000P photoresist is coated to cover the electroplated leads (~ 10μm). After development, a descum process was performed in a reactive-ion-etcher (RIE) to remove potential photoresist residue. Next, a 2 μm Ni layer was electroplated as the BLM (or UBM) and followed by Sn60Pb40 solder bump plating (Figure 2.10f). The Ni surface must be cleaned by acid *immediately* before the solder plating step to remove native oxide, as described above. In this manner, a clean interface between the UBM and the solder alloy is ensured, which is critical for excellent wetting during reflow. Another important feature of this process flow is that the three sequential electroplating steps share the same seed layer such that the number of operation steps is reduced. After the photoresist was stripped, the seed layer was etched and the sacrificial layer was removed (Figure 2.10g). After reflow with aid of a liquid flux (RMA#5, Indium Corp.), solder bumps with spherical shape were formed onto the MEMS leads (Figure 2.10h).

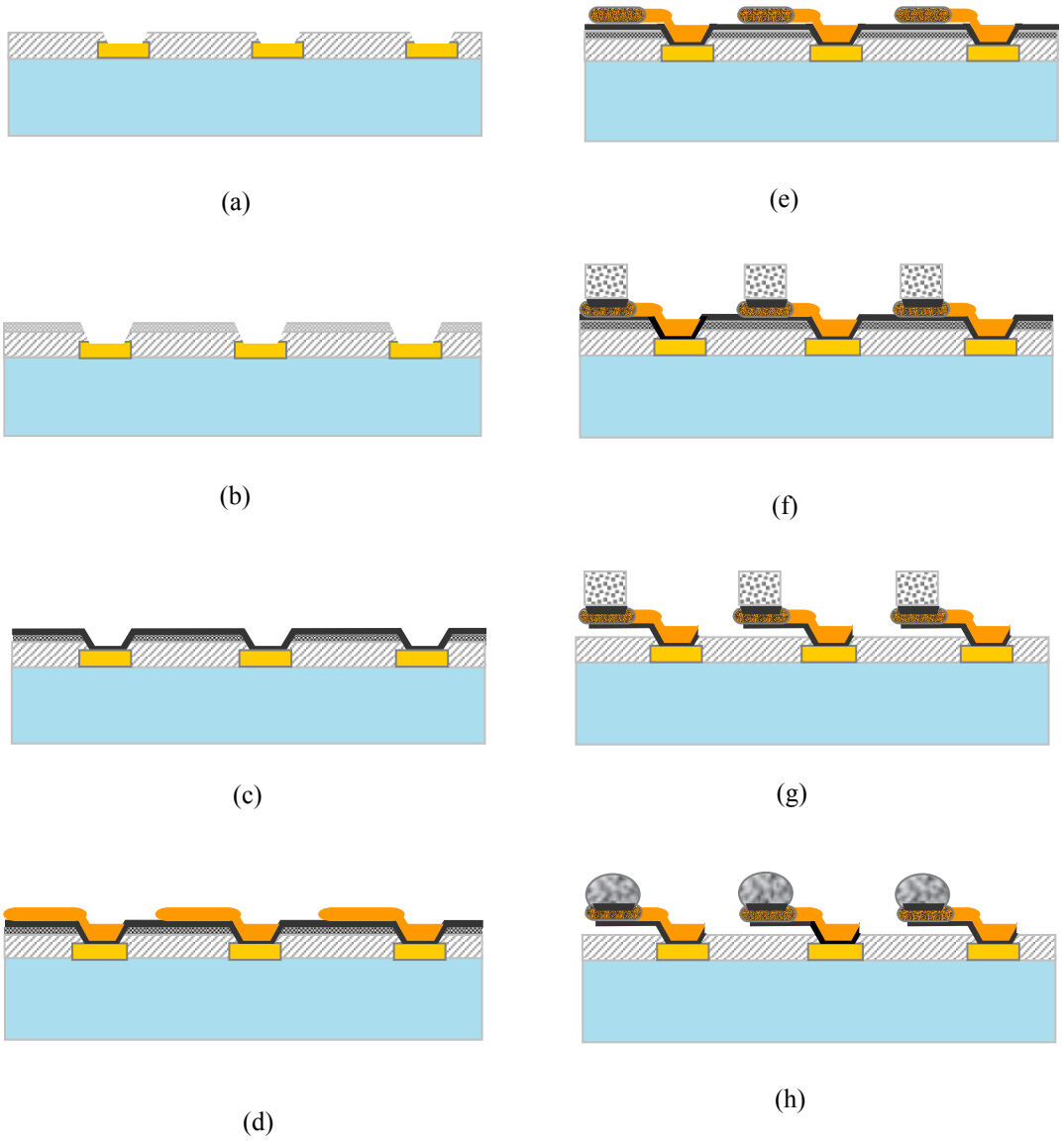


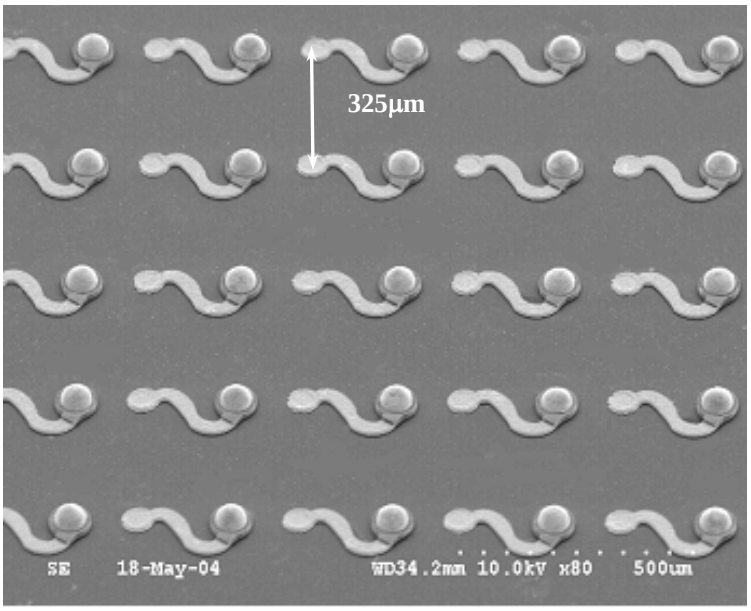
Figure 2.10: Illustration of the integration of SoL MEMS interconnects onto a BEOL wafer and bumping of the SoL interconnects through electroplating: (a) BEOL process completes, (b) deposition of a sacrificial layer, (c) deposition of a seed layer, (d) Patterning and plating of leads (e) deposit and pattern the solder dam, (f) Pattern and electroplate UBM and solder bumps, (g) Remove the seed/sacrificial layer, (h) Reflow of solder.

Figure 2.11a shows SEM micrograph of the completed SoL interconnects on the test wafer and the perspective view of the microstructure of a SoL interconnect is shown in Figure 2.11b. A releasing gap left by the sacrificial layer is clearly visible below the Au lead. The solder bumps were effectively confined at the tip of the leads by a solder dam (Figure 2.11b). The solder dam is formed using a photodefinable dielectric polymer (Avatrel 2195P, Promerus LLC.), which can be cured at as low as 160ºC and has a glass transition temperature larger than 250ºC. Without such a barrier, a solder bump can easily wick the metal leads during reflow, as illustrated in Figure 2.12. This is a very critical issue to all types of compliant leads and the solder dam can be a universal solution technique.

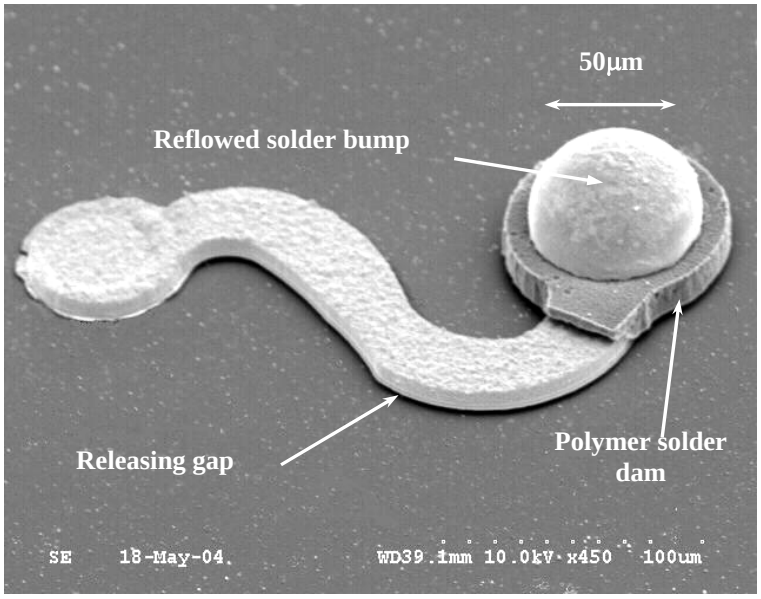
Another important element of the bumped SoL interconnects is the UBM. A well known reliability issue in conventional C4 technology is the excessive growth of Cu-Sn intermetallics during reflow, storage and operation at elevated temperature [2.10 - 2.12]. Therefore, it is desirable to apply a Ni-based UBM for SoL because Ni-Sn intermetallics provide a stable bonding interface and grow at a relatively slower rate [2.10]. The soldered Ni UBM can be revealed when the solder bump is removed by hot air as shown in Figure 2.13. The unique solder dam structure also effectively protects the edge of the leads from being wicked by the solder.

As summarized in

Table 2.3, the total stand-off height of a completed interconnect is 46.5 μm approximately, which includes the gap between a lead and the chip passivation, the thickness of a lead, the thickness of a solder dam, the thickness of the Ni UBM, and the final solder bump height. For the present geometry and dimensions, the overall calculated resistance of a SoL interconnect is 48.07 mΩ including the resistances of the lead, the UBM, and the solder bump.



(a) overview



(b) perspective view

Figure 2.11: SEM photographs of the completed SoL MEMS interconnects (h_{gap}~2µm; t_{lead}~7µm; t_{UBM}~3.5µm; h_{bump}~25µm; overall height~42.5µm).

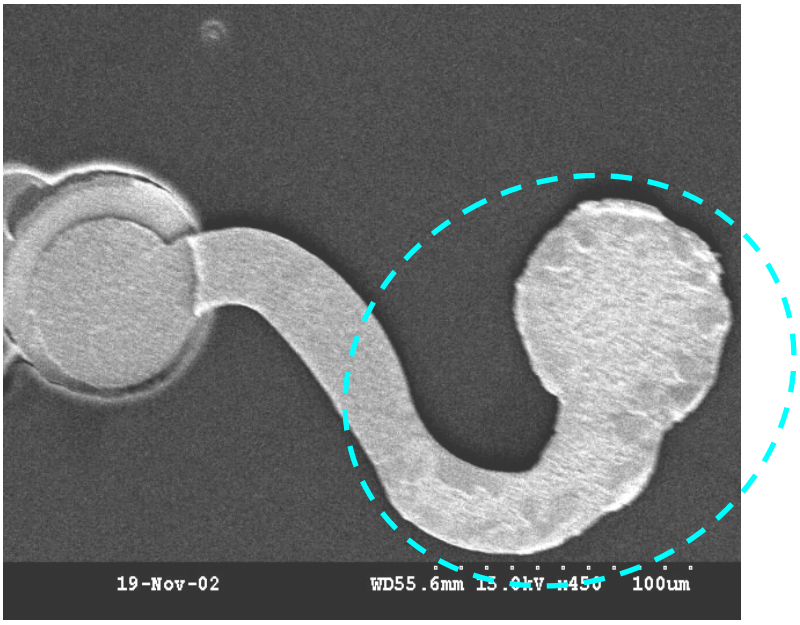


Figure 2.12: Illustration of the importance of a solder dam on a SoL MEMS interconnect (without such a solder dam, wicking can easily occur during solder reflow process)

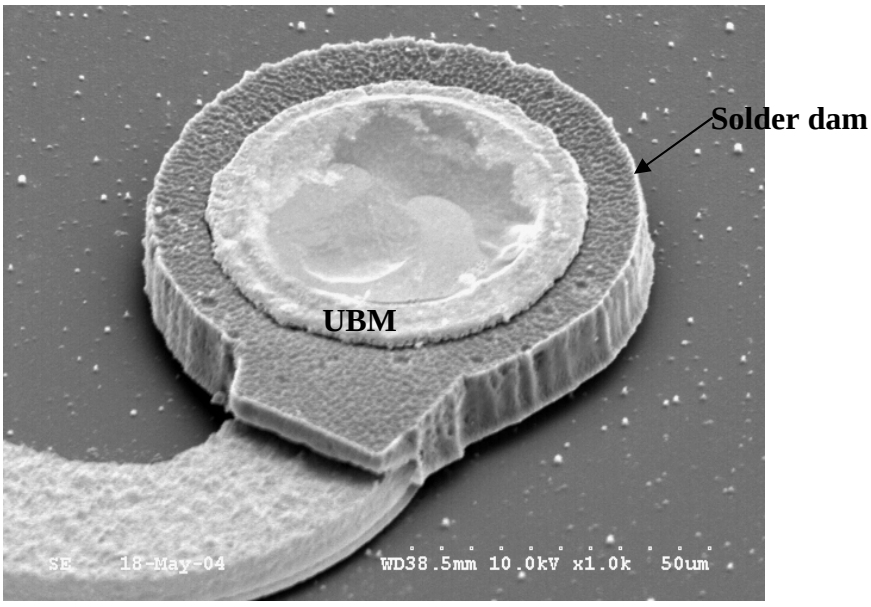


Figure 2.13: SEM photograph of the soldered Ni UBM revealed by hot air.

Table 2.3: Stand-off height and calculated resistance of a completed SoL interconnect

Parameter	Releasing Gap	Au lead	Solder dam	Ni UBM	Reflowed solder bump	Overall
Thickness (μm)	~2	~7	~5	2.5	~30	~46.5
Resistance (mΩ)	—	~28	—	~0.07	~20	~48.07

2.4. Assembly of SoL MEMS Interconnects by Flip-Chip Bonding

Although the highly compliant interconnects are desirable in terms of reliability, a great challenge is to protect them from damage before assembly. Particularly, high-pressure DI water during dicing can lift off or deform the compliant leads excessively in some areas if the leads are not protected (Figure 2.14).

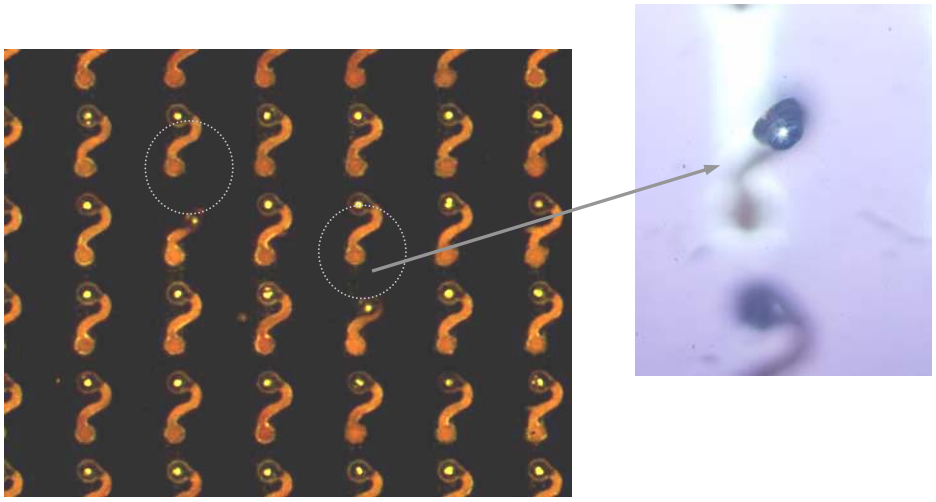
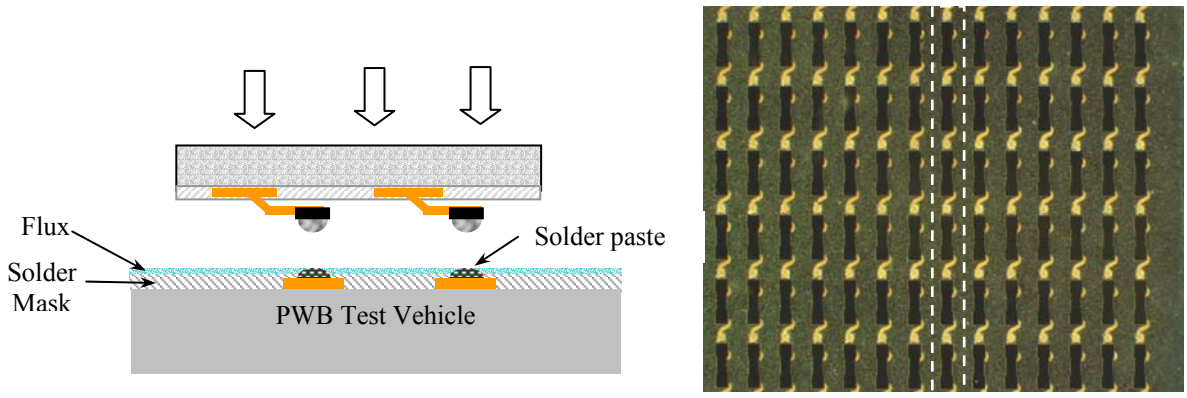


Figure 2.14: Illustration of a handling issue during the dicing process with high pressure DI water: the SoL MEMS interconnects may be lifted up by localized high-pressure impact.

An effective approach to avoid this problem is to encapsulate the leads with dissolvable polymer film such as photoresist before wafer dicing. This approach is commonly used for MEMS wafer when the surface is sensitive to the dicing dust or high-pressure water flow in the dicing process. In this work, NR9-8000 photoresist was used as the encapsulant and it can be easily removed by solvents such as Aceton during the post-dicing clean operation. Direct blow with high-pressure nitrogen should also be avoided during the drying process.

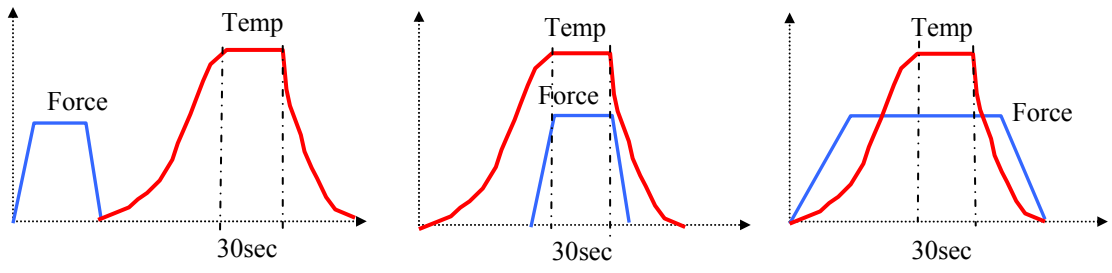
After the SoL chips were diced and cleaned, the next step is assembly. Also because of the nature of compliant interconnects, assembly of SoL chips requires more attention. In this study, thermal-compression bonding was used to compensate for the non-planarity of the PWB and the C4 bumps. A flip-chip bonder with high alignment accuracy was used (RD Automation Inc, Model MA-10). As illustrated in Figure 2.15, the Cu pads were pre-coated with solder and a thin layer of flux was then applied on the test vehicle for a better wettability.



(a) (b)

Figure 2.15: Illustration of thermal compression chip bonding experiments: (a) fluxing of PWB pads and placement of a chip with compression (b) an inspection view through a glass PWB substrate reveals the daisy chains cascaded.

The liquid flux (RMA#5, Indium Corp.) was used and the flux residue was cleaned by solvents (Acetone and Trichloroethylene). The major concerns during bonding include lead wicking by solder under excessive compression and misalignment due to displacement of the "slippery" MEMS leads. A transparent glass substrate was first used to fabricate the test vehicles for the purpose of easy inspection. From the back side of the glass substrate, the cascaded Au leads can be clearly observed, which confirms that no wicking occurred during the compression bonding. It was relatively easy to bond the test chips onto the glass substrates. While a glass test vehicle is useful for inspection of assembly, its CTE is close to that of the Si chips. To perform the thermal-mechanical reliability test, organic PWB substrates have to be used. Therefore, a test vehicle was built with the low-cost FR-4 laminate. Bonding experiments with various profiles (temperature, force, and reflow time) were conducted to find an optimized bonding process using the FR-4 test vehicle. As illustrated in Figure 2.16, during the bonding, a compression force was loaded on the SoL chip and both the chip and the substrate were heated to the peak reflow temperature (220°C). Three bonding profiles have been experimented and evaluated based on the yield of working test structure (the daisy chains).



(a). poor bonding yield (b). poor bonding yield (c). good bonding yield

Figure 2.16: Illustration of various thermal compression bonding profiles. (a) the temperature is increased after the compression force is released (b) the temperature is increased before a

compression force is loaded (c) the temperature is increased after the compression force is applied and the load is released while the temperature drops below the melting point

Profile A is similar to a conventional pick-and-place approach, in which a compression force is only loaded before reflow. In profile B, a compression force is loaded only during the peak reflow temperature segment. In profile C, a compression force is loaded before the temperature reaches the peak value and the load is maintained until the temperature drops below the melting point of the solder (~183ºC). The bonding yield was relatively low with the bonding profile A or B. This may be due to that neither of the two profiles can ensure a close contact between the solder bumps and bonding pads through the entire procedure. Because of the small dimensions of the solder bumps (diameter < 80 μm; height < 50 μm), it is difficult to achieve good joining at all the pads simultaneously. Under the profile C, the position of a chip is dynamically adjusted to maintain the compression force and the contact throughout the heating and cooling processes. As a result, excellent bonding yield was obtained for most test chips.

Figure 2.17 shows the cross-sectional view of the test board, in which the Cu lines (18 μm thick) are covered by a soldermask layer (~25 μm thick). It can also be seen that planarity of a typical organic PWB is not excellent, which is a well known challenge for the assembly of fine-pitch IC packages.

Multiple SoL chips have been bonded on the test vehicle, as shown in Figure 2.18. Since the FR4 laminate is not transparent, X-ray microscopy was used to inspect the alignment of the bonded leads on the Cu pads of the test vehicle upon completion of assembly. Electrical continuity test also confirms that joining is successful for the daisy chains and no shorting is detected between adjacent leads.

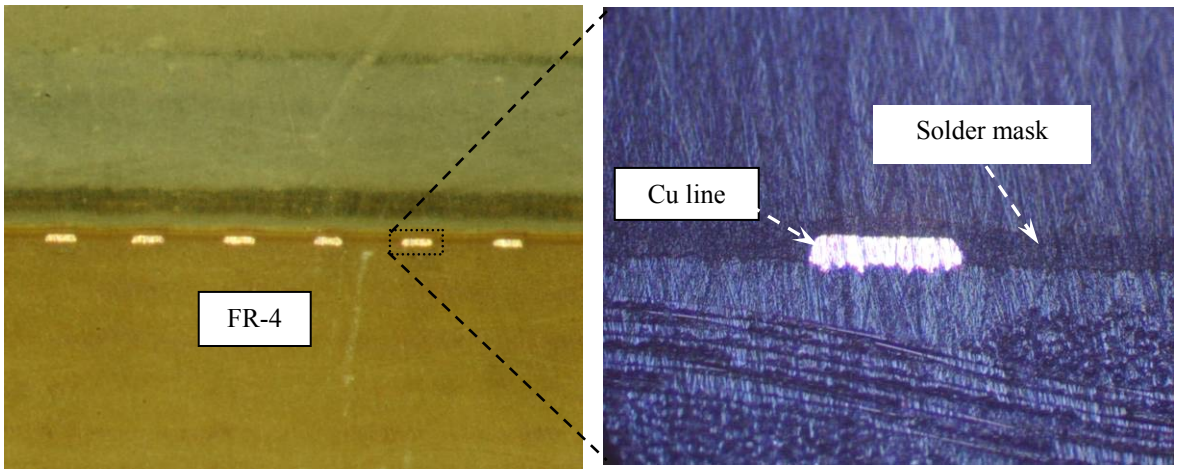


Figure 2.17: Cross-sectional view of the test board with 18μm Cu lines covered by a layer of Avatrel 2195 dielectric polymer as the solder mask.

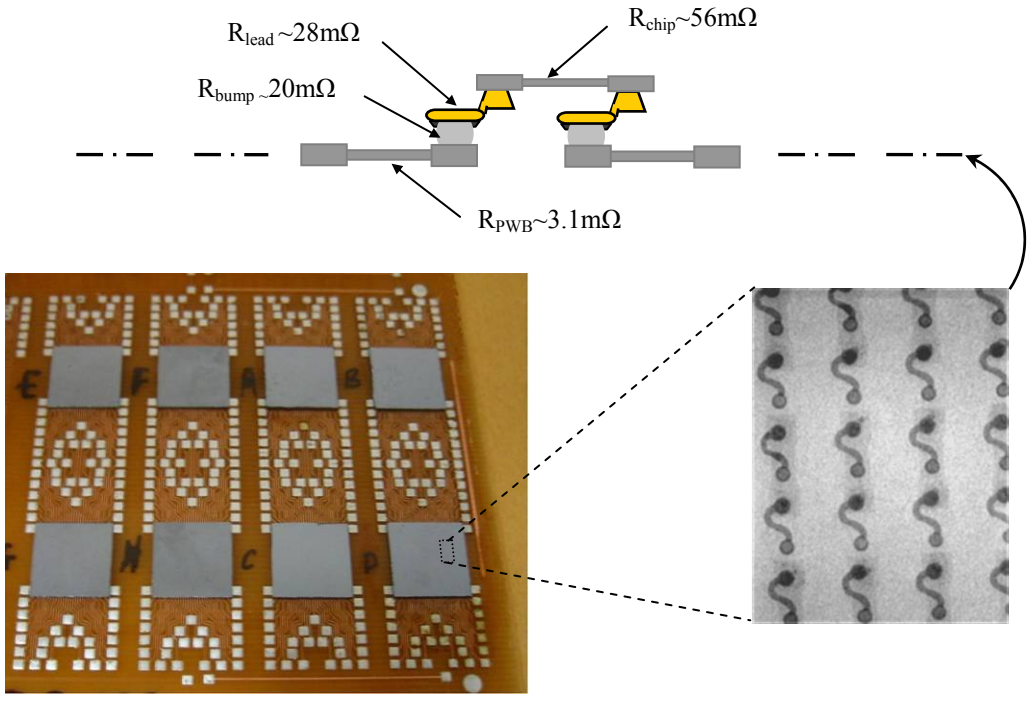


Figure 2.18: Overview of eight SoL chips bonded on the FR-4 test vehicle and X-ray microscopy that shows successful joining of compliant interconnects.

Figure 2.19 shows the cross-sectional view of a typical a solder joint between a lead and a Cu pad on the substrate from an as-bonded sample. Uniform interface can be observed at the boundary between the solder and the Ni-UBM. Meanwhile, an obvious intermetallic compound (IMC) layer is observed at the solder-Cu pad boundary.

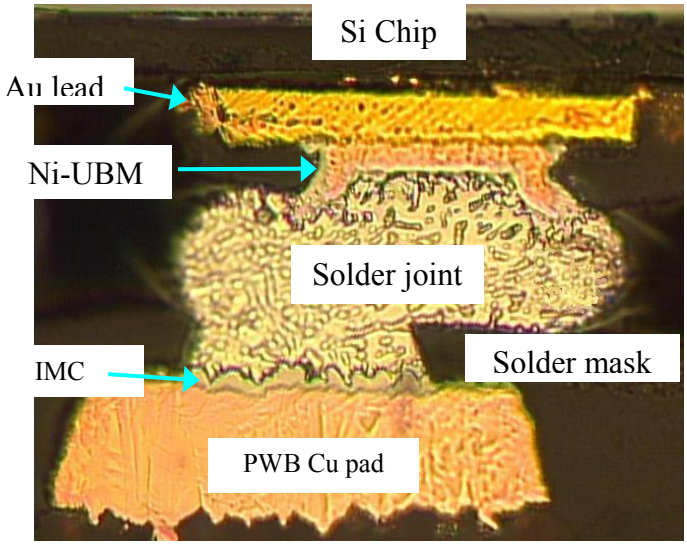


Figure 2.19: The cross-sectional view of a solder joint between a slippery lead and a Cu pad on the PWB substrate.

2.5. Thermal-mechanical Reliability Study

The test chips are 1cm×1cm in size and each chip contains 31 parallel daisy chains at pitch of 325μm as the test structure. Each daisy chain consists of 30 leads and solder joints cascaded between the chip and the board. Fifty-four functional chains were tested in total and the average measured resistance of the chains in the as-bonded samples is 2.52Ω, which agrees with the estimated value (~2.3Ω) based on the circuit components in Figure 2.18. The SoL test vehicles were then subjected to thermal cycling between 0°C-100°C for the accelerated

temperature cycling test based on JEDEC Standard (Condition J of JESD 22-A104-B). The dwell time at the upper and lower zones is 15 minutes respectively with two cycles per hour. As shown in Figure 2.20, the change in resistance of the daisy chains was measured periodically to detect a failure, which is defined as an increase of 15% in the measured resistance on a daisy chain.

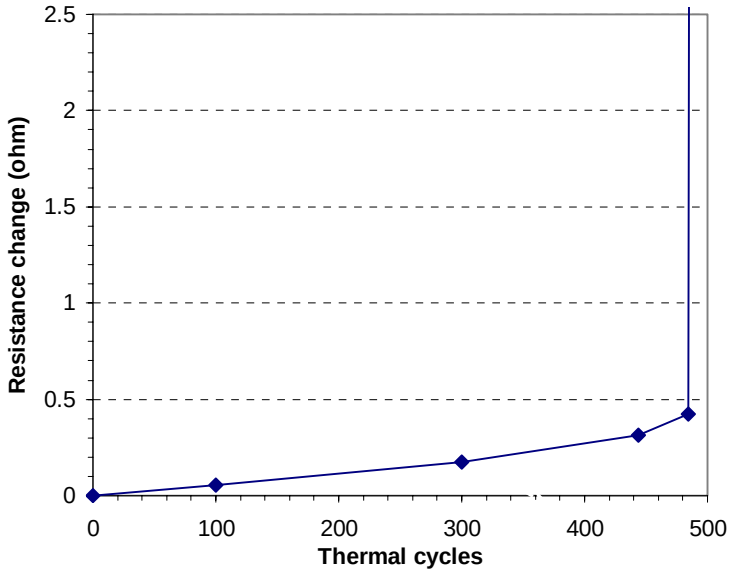


Figure 2.20: Resistance change on a daisy chain during the thermal cycling test.

The accumulative percentage failure rate was recorded for all the functional daisy chains and plotted as a function of the number of the thermal cycles (Figure 2.21). Around 13% of test chains failed after the first 100 cycles and all the test chains failed after 523 thermal cycles. The trend of failure rate agrees approximately with that of the "weibull distribution," which is commonly used for assessment of the thermal-mechanical reliability of solder based interconnects [2.13, 2.14]. In addition, it was noticed that the test chains located closer to the edges of the chips tend to fail earlier than these chains close to the center of the chips. This is understandable because the induced displacement on each lead is proportional to its distance

from the neutral position (DNP) and a larger global mismatch is expected at the chip edges due to a larger DNP.

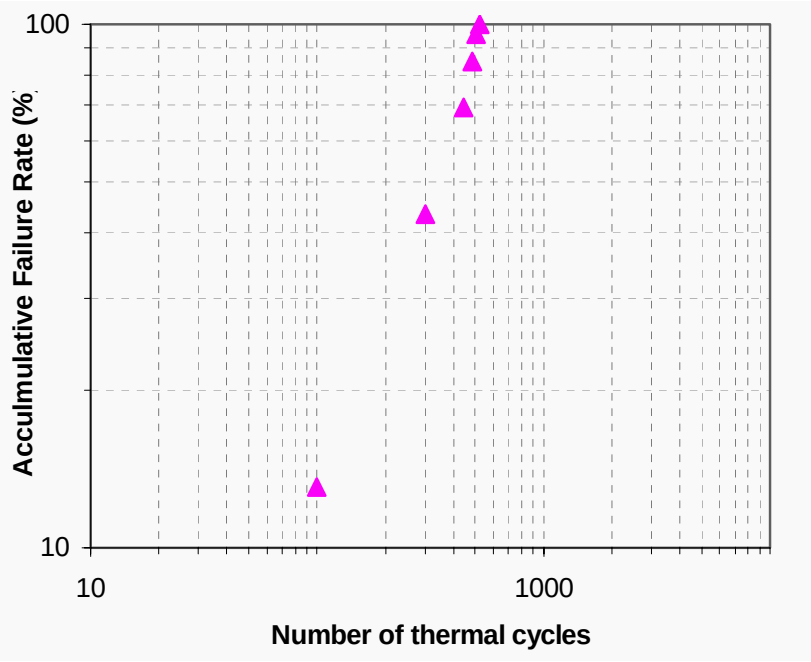


Figure 2.21: Accumulative failure rate as a function of number of thermal cycles

To further investigate the main failure mechanism of the SoL compliant interconnects, a failed chip was removed by heating the substrate to the reflow temperature, as illustrated Figure 2.22. Since there was no underfill, the chip can be easily detached by a piece of polyimide Kapton tape once heated up. By this means, the solder was melted first and the interconnects were preserved for inspection. As expected, the Au leads were not broken during the thermal cycling test because of the compliant nature of the slippery SoL. Therefore, the failure most likely occurred at the solder joints. To reveal the failure at the solder joints, the failed samples were mounted in epoxy and cross-sectional polishing was performed in two directions as shown in Figure 2.23.

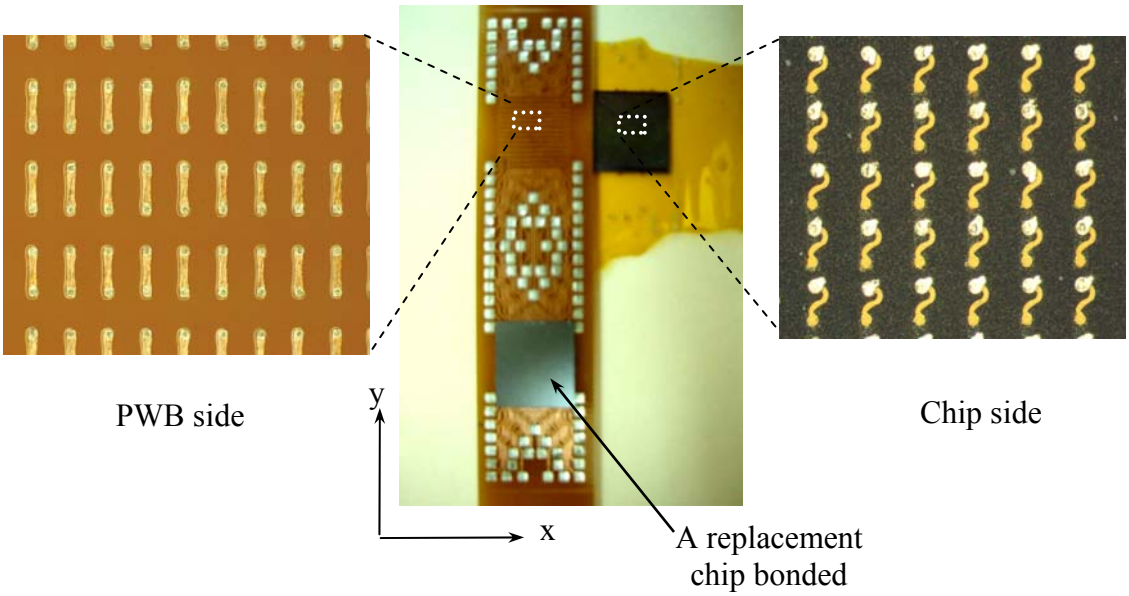
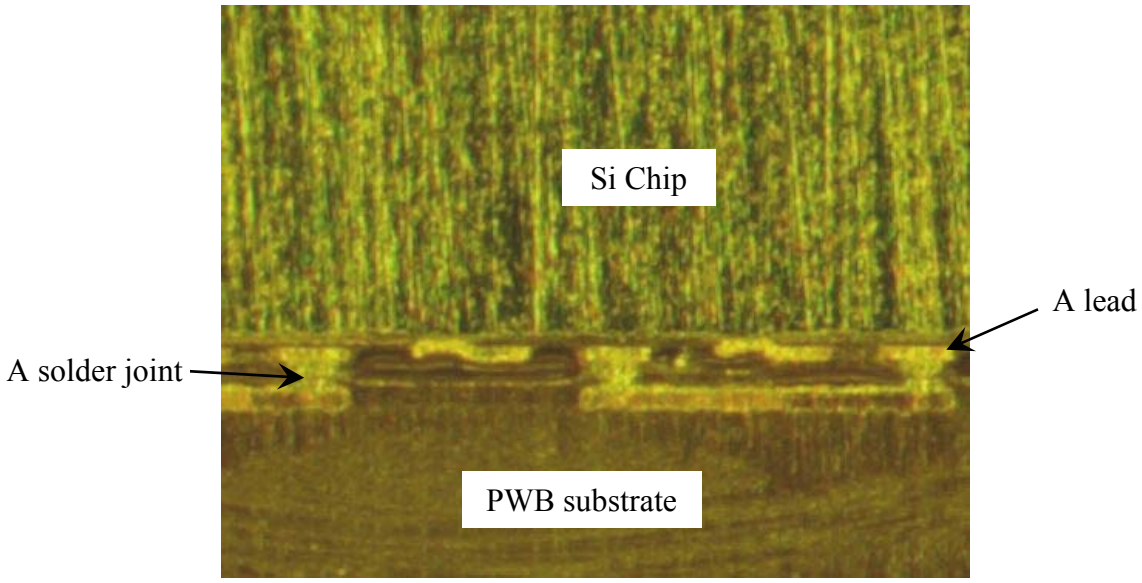
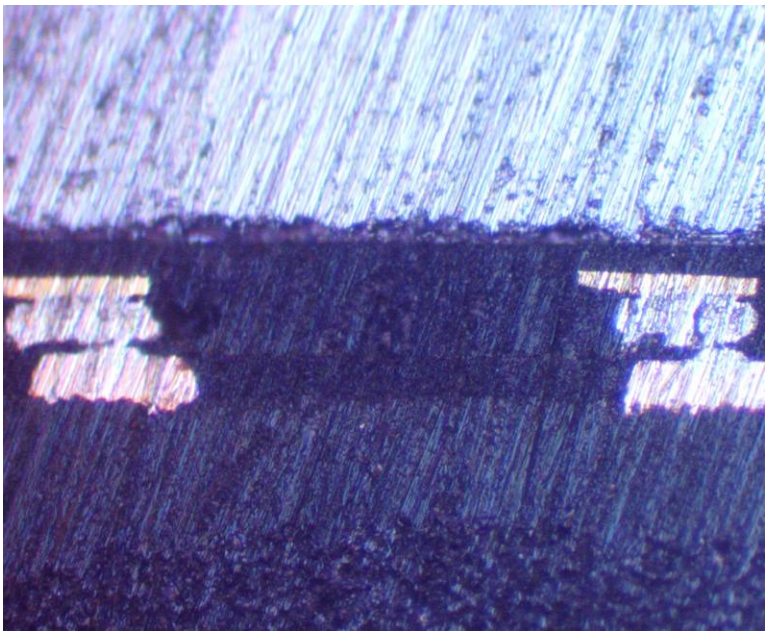


Figure 2.22: Illustration of failure observation by removal of a failed chip at high temperature: The top view of the PWB side shows the clean bonding pads after removal of a failed chip, and the micrograph of the failed chip confirms that the failure was not a result of the broken leads; the bonded replacement chip indicates that the reworkability becomes possible since no underfill was used.

It can be seen that failure is mainly caused by cracking near the boundary between a solder joint and a Cu pad on the PWB. An important reason of such a failure is the excessive growth of Sn-Cu IMC close to the PWB Cu pads. As mentioned above, an obvious layer of IMC was observed in the as-bonded solder joint (Figure 2.19). Since there was no effective barrier over the Cu pads on our present FR-4 board, IMC can grow at elevated temperature and result in a brittle joint close to the solder-Cu boundary. A solution to this issue is to use proper board finishes such as Ni that can act as a diffusion barrier, as suggested in literature [2.10]. Unfortunately, the Ni electroless plating process was not available for the in-house PWB fabrication processes at the time of experiments.



(a)



(b)

Figure 2.23: Failure observation by polishing of the failed sample in two directions: (a) polished in longitude (x) direction along the lead orientation, (b) polished in transverse (y) direction perpendicular to the lead orientation.

Another issue is the poor design of solder mask opening on the test board. Recall from Figure 2.19, we can observe sharp solder mask edges at the lower portion of the solder joint, which may introduce stress concentration. This issue would be resolved if the soldering is defined by the PWB pads (namely non-solder mask defined soldering). Because of these reasons, we conclude that the main failure mechanism of this specific experiment is the early failure of the non-ideal solder joints.

2.6. Summary

This chapter described the implementation of MEMS-based SoL compliant I/O interconnects. The key fabrication steps include the lead releasing and bumping processes. While undercut etching is a simple approach to release the electroplated leads, it is difficult to apply these processes to a large wafer because of the non-uniformity in wet etching. Therefore, a thin-film sacrificial layer was introduced for the releasing of the electroplated leads with easier control and better yield. The overall process was reconciled for the compatibility with the BEOL and the electroplating wafer bumping.

Masked evaporation or electroplating through photolithography may be used for bumping the MEMS leads. When evaporation is used, leads should not be released until the bumping processes are completed to avoid damage by the removal of the Mo mask. For the electroplating wafer bumping, process integration issues have been addressed with three mask steps in addition to the conventional C4 processes. Bonding experiments indicate that compression force is critical for the assembly because of the small dimensions of the solder bumps on the MEMS leads. Using a flip-chip bonder, the test chips with the SoL interconnects were assembled on the low-cost organic PWB test vehicles without use of any underfill. In the preliminary reliability test, the SoL MEMS interconnects have survived more than 500 thermal cycles without use of

underfill, which represents a promising improvement over a regular C4 solder interconnection. Failure analysis revealed that the main failure mechanism of the tested samples is in the solder joints instead of the compliant leads. Reliability of the SoL MEMS interconnects can be further improved by optimization of chip-package co-design. For example, for a given I/O pitch, the lead geometry can be redesigned and the lead orientation may be rearranged to improve the effective mechanical compliance. Therefore, the optimization of structural design will be discussed in the following chapter. Full reliability potential of the MEMS-based SoL can only be better understood upon application of optimized board metallurgies, a proper design of solder mask opening, and optimized lead geometries and orientation, etc. Nevertheless, for the first time, technology feasibility of the SoL MEMS interconnects has been demonstrated through a full procedure of fabrication, assembly and reliability assessment.

Chapter 3. Structural Characterization for SoL MEMS Interconnects

3.1. Introduction

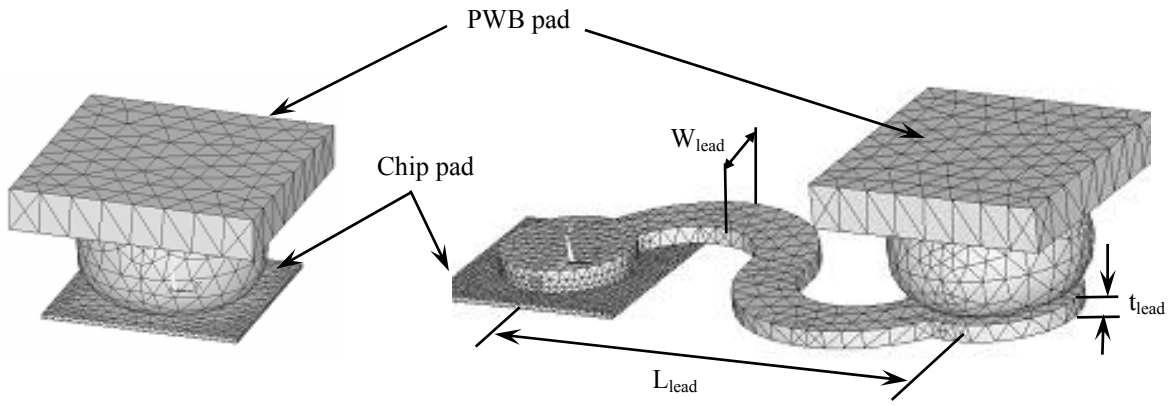
In conventional flip-chip packages, underfill is beneficial to the reliability of chip-package interconnects (C4 solder joints) since it strongly couples the chip with the package substrate. However, such a strong mechanical coupling between the two surfaces means that the deformation of the organic package substrate can induce a large shear force on the chip surface [3.1]. This raises reliability issues when the mechanically weak low-k interlevel dielectrics (ILDs) are used. The low-k materials have intrinsically lower modulus, lower fracture toughness, and poorer adhesion compared to conventional dielectric materials [3.2, 3.3]. For instance, the modulus of the commonly used low-k films is less than 10 GPa, compared with 70 GPa for SiO_2. Thus, delamination and cracking may occur easily in the Cu/low-k interconnect structures under the thermal-mechanical stress. In contrast, when the MEMS I/O interconnects are used without underfill, chip surface is mechanically decoupled from the deformation of the package substrate [3.4 – 3.8]. Since the MEMS leads become the only mechanical and electrical links between chip and package substrate, the properties of the leads determine the chip-package interaction. While the key feature of SoL interconnects is their mechanical compliance from the "spring-like" geometries, the long curved interconnect path will increase the electrical parasitics such as resistance and inductance. Therefore, structural design optimization should include the trade-off between mechanical compliance and electrical characteristics.

This chapter will first discuss the mechanical benefits of the SoL MEMS interconnects through micromechanical finite element modeling (FEM). Package weight analysis is then discussed considering the mass of typical heat sinks. Furthermore, with an "S-shape" lead as an

example, the structural effects on the mechanical compliance are simulated. The electrical characteristics are also estimated through numerical simulation. Based on the results of the analysis, general guidelines are developed and proposed for structural design optimization of the SoL MEMS interconnects.

3.2. Micromechanical Finite Element Modeling

As shown in Figure 3.1, three-dimensional (3-D) finite element models were first built to compare a C4 solder joint with SoL MEMS interconnect. In the models, the on-chip pad is 2 μm thick, while the PWB pad is 9 μm thick. Solder joints have a collapsed spherical shape because of the compression force during the flip-chip bonding process. SoL interconnects consists of a MEMS lead and a solder joint. A solder joint is 30 μm in height and the contact area on the pads or the leads is 55 μm in diameter. The lead dimension are as follows: W_{lead}=25 μm; L_{lead}=190 μm; t_{lead}= 7.5 μm.



(a) C4 solder joint

(b) SoL MEMS interconnect

Figure 3.1: The meshed 3D FEM models of a C4 solder joint and a compliant lead based on SoL between a chip pad and a PWB pad. (chip pad: 80μm×80μm×2μm; PWB pad: 100μm×100μm×9μm; W_{lead}=25 μm; L_{lead}=190 μm; t_{lead}= 7.5 μm)

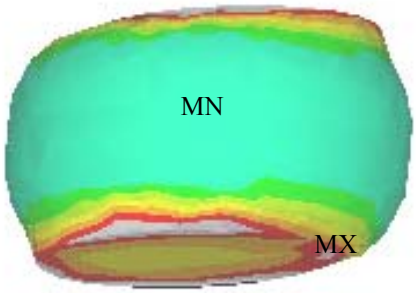
The materials models used to represent the behavior of the various components in the FEM models are listed in Table 3.1. The time independent plastic behavior of both Cu and Au were represented utilizing a classical bilinear kinematic hardening rule, while 60Sn40Pb solder was represented utilizing a multilinear kinematic hardening rule [3.5, 3.9]. The creep behavior of the solder was not modeled for simplification.

Table 3.1: Material properties for the FEM [3.5, 3.9].

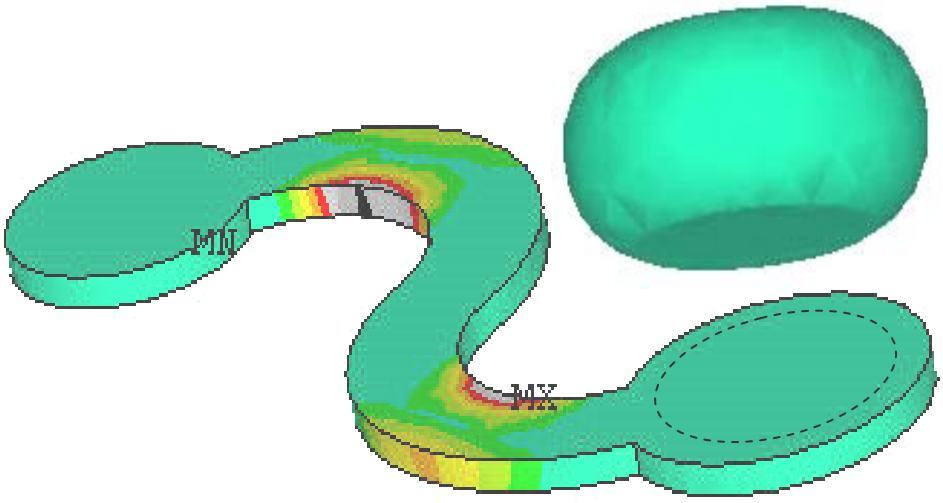
Materials	Components	Material Model	Modulus (GPa)	Poisson's ratio
Cu	Chip pad, PWB pad, MEMS lead	Bilinear kinematic hardening rule	121	0.3
Au	MEMS lead	Bilinear kinematic hardening rule	64	0.42
60Sn40Pb	Solder joint	Multilinear kinematic hardening rule	<30.685 (nonlinear)	0.4

3.2.1. Mechanical Benefits of the SoL MEMS Interconnects

Using ANSYS, the relative shear displacement between a chip pad and its counterpart pad on the package substrate was simulated for a single C4 solder joint and a MEMS lead. During the simulation, the bonding pad at the chip side was constrained, while a displacement was applied on the PWB Cu pad. Due to the difference in geometry, mechanical structure, and material properties, the mechanical response from the displacement is significantly different for a C4 solder joint and a MEMS lead. As shown in Figure 3.2, with a C4 solder joint as the interconnect, both sides of the joint are strained and the maximum plastic strain is located at the solder-pad interface at the chip side. In contrast, when a MEMS lead is used as the interconnect, no significant deformation occurs in the solder joint, while the maximum plastic strain is located in the curved areas of the lead.



(a)



(b)

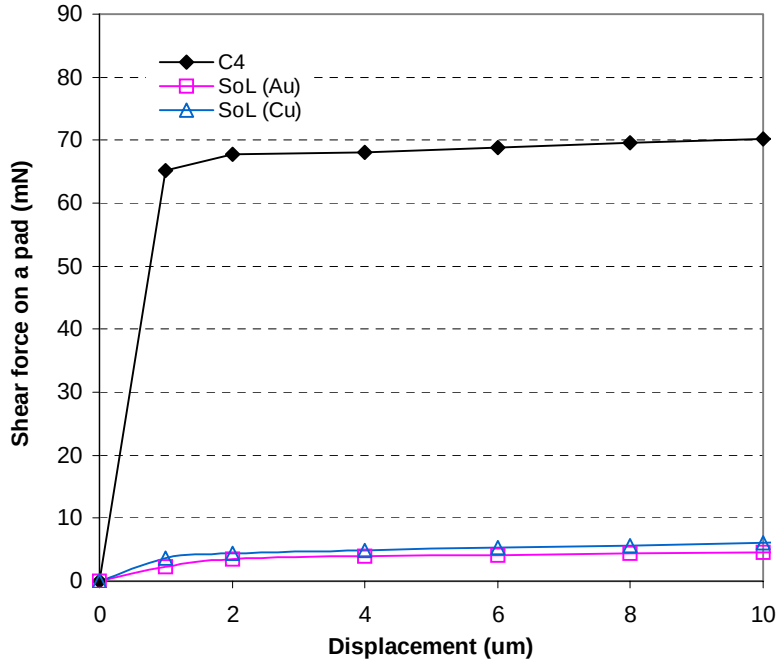
Figure 3.2: Von-mises plastic strain distribution caused by an in-plane displacement between a chip pad and a PWB pad (a) with a C4 solder joint as the I/O interconnect or (b) with a MEMS lead with a C4 solder joint as the I/O interconnect (The lead dimensions are: W_{lead}=25 μm; L_{lead}=190 μm; t_{lead}= 7.5 μm)

The maximum plastic strain is plotted as a function of the relative displacement for the two types of interconnects, as shown in Figure 3.3a. As expected, the level of the maximum plastic strain induced in a MEMS interconnect is 10x smaller than that induced in a regular C4 solder joint. In general, the thermal-mechanical fatigue life, N_f (cycles), for a metallic interconnect is related to the plastic shear strain range, $\Delta\gamma$ (dimensionless), during the thermal cycling according to the Coffin-Manson relation [3.10]:

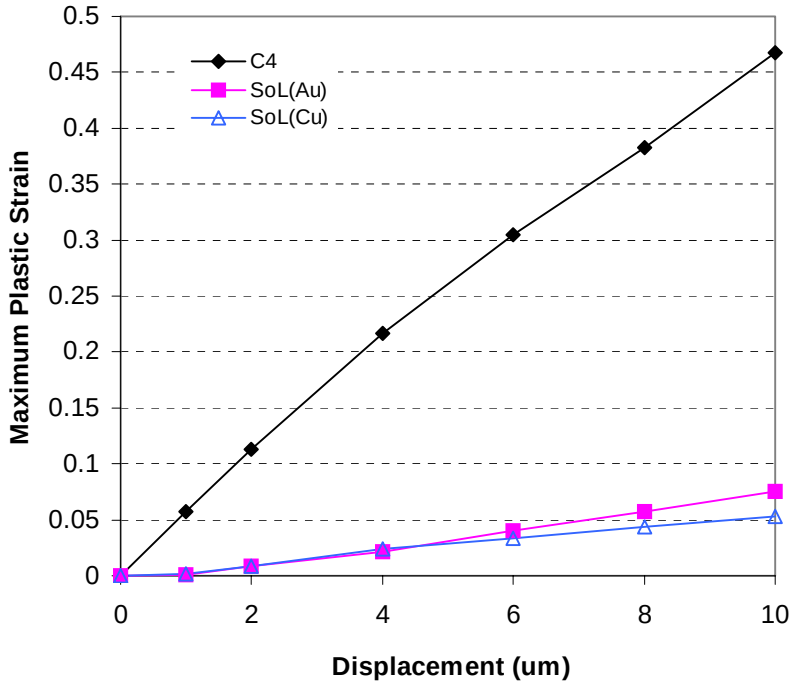
$$N_f = C\,(\Delta\gamma)^{\beta} \tag{3.1}$$

where C and β (<0) are the dimensionless material constants. Thus, a smaller plastic strain range leads to a longer fatigue life time. Although comprehensive models are required to predict the fatigue life in practice, SoL compliant interconnects are obviously promising to offer higher reliability when underfill is not used since the induced plastic strain can be further minimized through structural optimization.

Figure 3.3b illustrated the calculated shear force resulted from the deformation of an interconnect as a function of the in-plane displacement between an on-chip pad and its counterpart pad on PWB substrate. The level of the shear force loaded on a chip pad from a C4 solder joint is more than ten-times higher than that from a MEMS lead, which clearly indicates an important benefit for the mechanically fragile low-k ILD. A Cu lead induces slightly higher force than an Au lead due to its larger modulus. On the other hand, it can be seen that the linear range of the force-displacement curve is much shorter for a C4 solder joint than that for a SoL MEMS interconnect. This also means that a plastic deformation rapidly occurs in a C4 solder joint once the displacement is applied.



(a)



(b)

Figure 3.3: Mechanical response as a function of the relative displacement for a C4 solder joint or a SoL MEMS interconnect as the chip-package interconnect: (a) the maximum von-mises plastic strain (b) the induced shear force on a pad.

3.2.2. Package Weight Supportability Issues

In practice, a heat sink may be used for a microprocessor package depending on the applications. Low-cost, hand-held, and memory applications usually do not require a heat sink, while cost-performance and high performance applications often require a large heat spreader/a forced-air heat sink with high aspect ratio fins because of the high power dissipation. With the MEMS leads as the chip-to-package interconnects, the entire weight of a die as well as a heat sink will be loaded onto and distributed across all the MEMS leads since underfill is eliminated. Such a load will result in a vertical deformation on a lead to a certain degree and its effect on the compliance of the structure must be considered.

Using ANSYS, the vertical deformation of a lead was simulated under a downward compression force. Assuming an approximately even distribution of the overall package weight onto all the leads, the downward compression force on the individual leads is inversely proportional to the total number of the leads for a given overall load. As illustrated in Figure 3.4, the induced vertical deformation increases linearly as a function of the load for a large range. Meanwhile, the more leads are used, the less vertical deformation is induced on each lead since a smaller load is present. If the vertical deformation is larger than the gap beneath a lead, a friction will occur between a lead and the chip surface and mechanical compliance of the leads may be affected. Simulation results for several cases including various loads (from 0.5 g~ 41 g) and lead densities (1000 leads/cm^2 or 2500 leads/cm^2) are summarized in Table 3.2. Without a heat sink, the weight of a bare die causes a vertical deformation less than 0.24 μm even for a low I/O count, which is negligible for the height of the gap beneath a lead (>2 μm). Considering a bare die and a small heat spreader (~ 1.6 g), the maximum resulting vertical deflection on a MEMS lead is around 0.8μm, which is still smaller than the gap beneath a lead. However, considering a larger

heat sink (~ 41 g) for high power dissipations, the minimum simulated vertical deformation is larger than the gap beneath a lead.

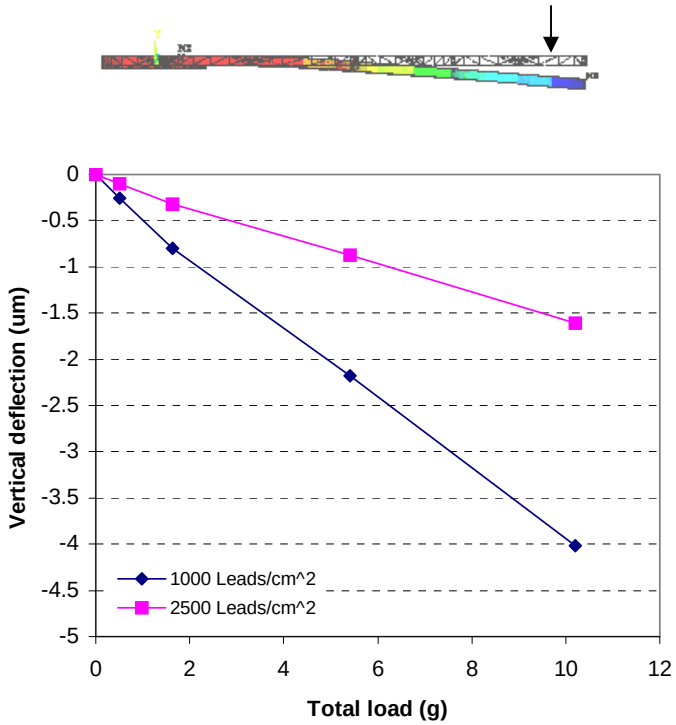
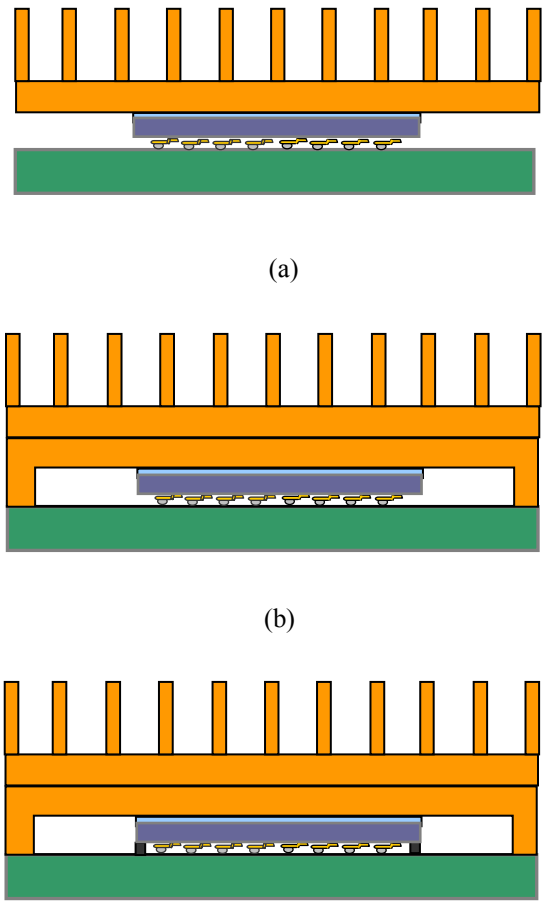


Figure 3.4: FEM simulation of vertical deflection of the MEMS leads under package weight. (The lead dimensions are: W_{lead}=25 μm; L_{lead}=190 μm; t_{lead}= 7.5 μm)

Table 3.2: Summary of vertical deformation for several package weight cases [3.9]

Case	Approximate weight (gram)	# of leads (cm^{-2})	Force on a lead (N)	Vertical Deformation (μm)
Bare die (1cm×1cm×0.05cm)	~0.5	1000	0.005	0.24
		2500	0.002	0.07
Bare Die + small Al spreader (1cm×1cm×0.6cm)	~1.6	1000	0.016	0.8
		2500	0.006	0.36
Bare Die + large Al heat sink (5cm×5cm×0.6cm)	~41	1000	0.41	20.2 (>> the gap below a lead)
		2500	0.164	16.3 (>> the gap below a lead)

This implies that a serious friction can occur between a lead and the chip surface and the effective compliance of the MEMS leads may be significantly affected. As illustrated in Figure 3.5a, a worst case can occur if a heat sink is directly loaded onto the back-side of a SoL chip. If a heat spreader has a mounting base as illustrated in Figure 3.5b, the compression force loaded on the leads can be largely reduced. Another solution is to incorporate certain spacers between a SoL chip and the mounting substrate as illustrated in Figure 3.5c.



(a)

(b)

(c)

Figure 3.5: Illustration of package weight support issues with a large forced-air heat sink: (a) a heat sink directly on a die is the worst case, (b) a heat spreader with mounting base on a substrate can reduce the impact on the MEMS leads, (c) spacers can be used to support the package weight.

3.3. Structural Effects

The mechanical and electrical characteristics of a MEMS lead are determined by its geometry and dimensions for a given material. An "S-shape" or "quasi S-shape" is commonly used for compliant interconnects and usually show the spring-like behaviors [3.4 - 3.9, 3.11]. The length and arc radius of a lead are constrained by the available chip area for I/O interconnects and the area array I/O pitch. For a given length and arc radius, the primary structural variables are the width and thickness and will be used for the discussion of design optimization in this section. Their influence on the electrical parasitics such as DC resistance and inductance will also be evaluated.

3.3.1. Structural Effect on Mechanical Compliance

The most important mechanical property of a compliant lead is its compliance. The compliance is usually defined as the ratio of the displacement to the applied force for a certain direction. Although the out-of-plane compliance is important to enable wafer-level probing or to compensate for package substrate warpage, the in-plane compliance is more critical to compensate for the CTE mismatch, and therefore, has been often used to evaluate effectiveness of the compliant interconnects [3.9]. Based on the FEM simulation results for an "S-shape" lead, the dependence of its compliance on its width and thickness is shown in Figure 3.6. The simulated thickness (t) of a lead ranges from 2.5 μm to 15 μm and the lead width (w) ranges from 15 μm to 30 μm. As expected, the compliance of an "S-shape" lead increases when its thickness and width are reduced mainly because of the decrease in the cross-sectional area (A = w×t) of the lead.

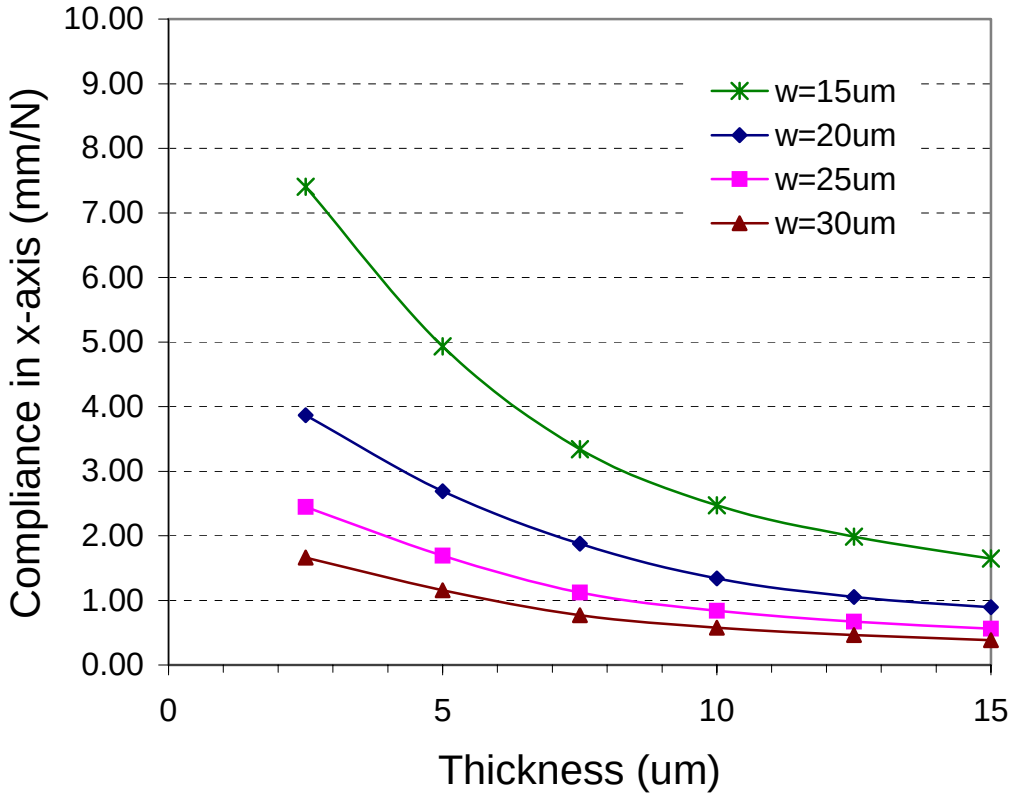


Figure 3.6: Effect of dimensions on the mechanical compliance of the "S-shape" leads. (The dimensions are same as those in Figure 3.1)

In addition, due to the non-symmetrical geometries of most compliant leads, their mechanical response is also a function of the direction of the displacement. As a result, their compliance may vary significantly at different directions. Figure 3.7 illustrates the effect of displacement direction on the compliance of a lead. The simulation results indicate that the compliance of an "S-shape" lead in their transverse direction (Y direction) is the highest while its compliance in the longitudinal direction (X direction) is the smallest. The ratio of its compliance in the two directions is more than 200% and increases rapidly when the lead thickness decreases. Therefore, the orientation of a MEMS lead should be carefully considered to ensure a larger compliance to be effective along the direction of the displacement during the design. In practice,

the in-plane displacement caused by CTE mismatch is usually in the direction of a contour line away from the center of the chip. Although it is not possible to arrange each individual lead in its optimal orientation, it is desirable to avoid an orientation that gives the least compliance for the MEMS leads during the mask design.

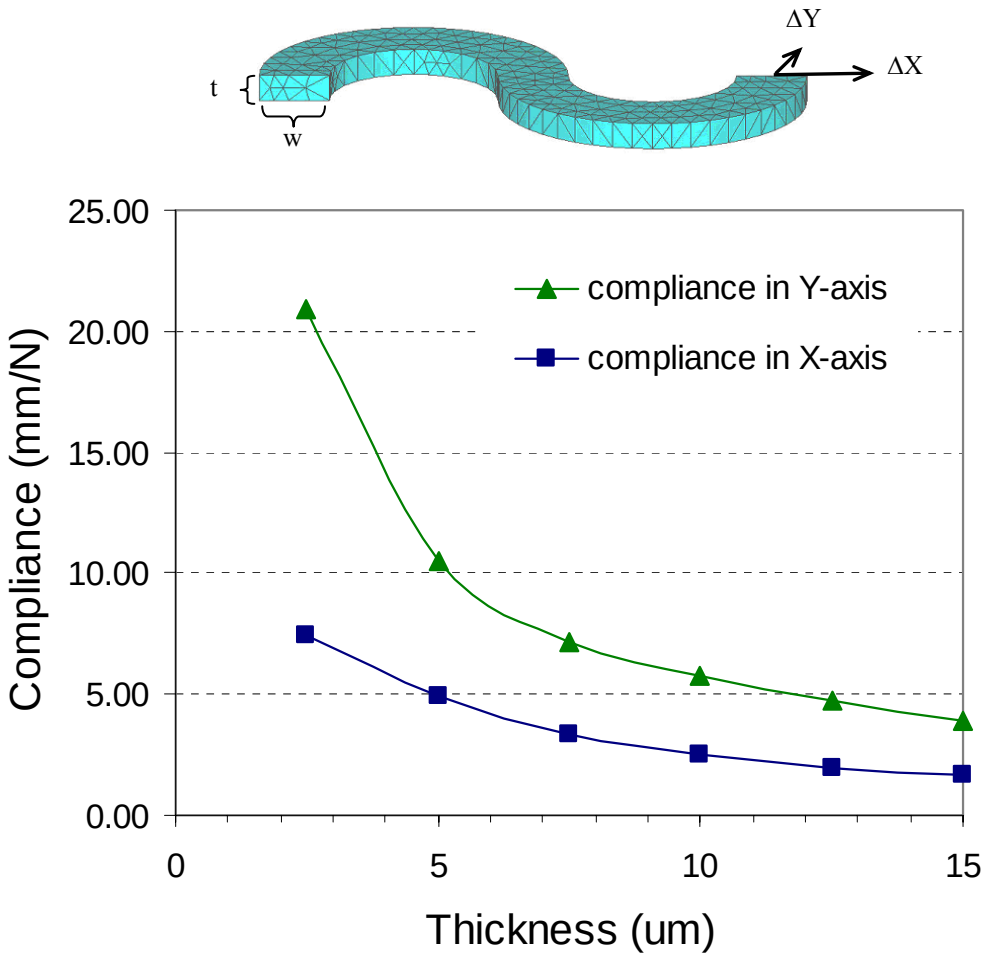


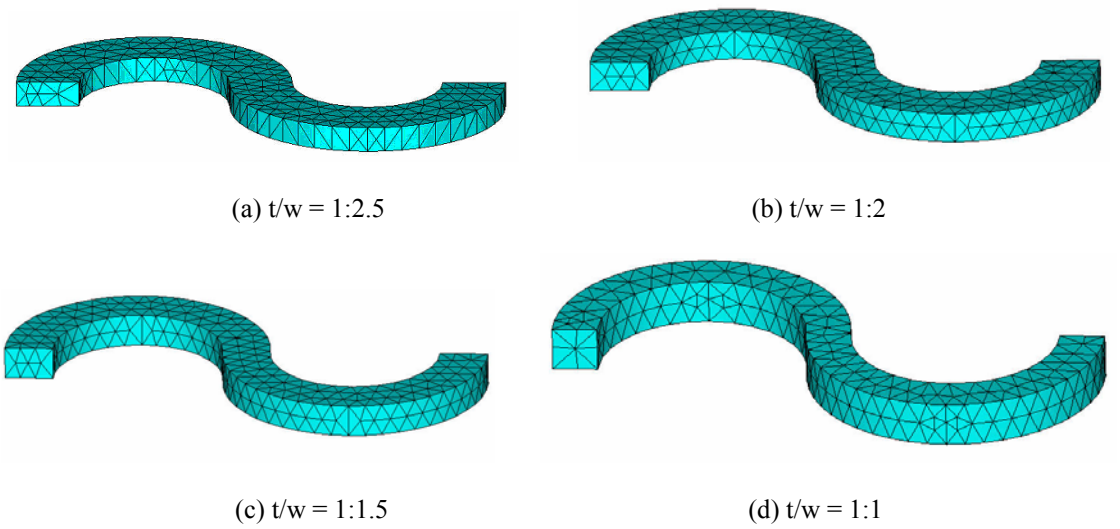
Figure 3.7: Directional effect of the in-plane compliance based on FEM simulation. (The dimensions are same as those in Figure 3.1)

3.3.2. Effect of Lead Aspect Ratio (t/w) on Mechanical Compliance

There is little room in terms of the design window for the arc radius once the I/O pitch is fixed based on the available chip area for each I/O. However, the aspect ratio (t/w) may vary

significantly, for a given cross-sectional area, as illustrated in Figure 3.8. The variation of aspect ratio obviously influences the compliance of a MEMS lead. Figure 3.9 shows that the in-plane compliance increases with an increase of the aspect ratio, while the out-of-plane compliance decreases with increasing aspect ratio.

This is understandable considering the directional effect of the two types of compliance: the in-plane compliance increases when a lead is "narrower" in horizontal direction and the out-of-plane compliance decreases when a lead is "thicker" in vertical direction. Nevertheless, as described in the previous chapter, the negative photoresist was used to define the mold for the electroplating of the metal leads. In general, it is relatively easier to process the photoresist for the features with smaller aspect ratios. Taking NR9-8000 as an instance, the defined cavities with high aspect ratio are difficult to be developed by the developer and slant sidewalls are often observed. Thus, the maximum lead aspect ratio considered in this work is approximately 1:1, which also offers a reasonable balance between the in-plane and out-of-plane compliances.



(a) t/w = 1:2.5 (b) t/w = 1:2

(c) t/w = 1:1.5 (d) t/w = 1:1

Figure 3.8: FEM model of "S-shape" leads with various aspect ratios (A = w×t = constant for a constant resistance)

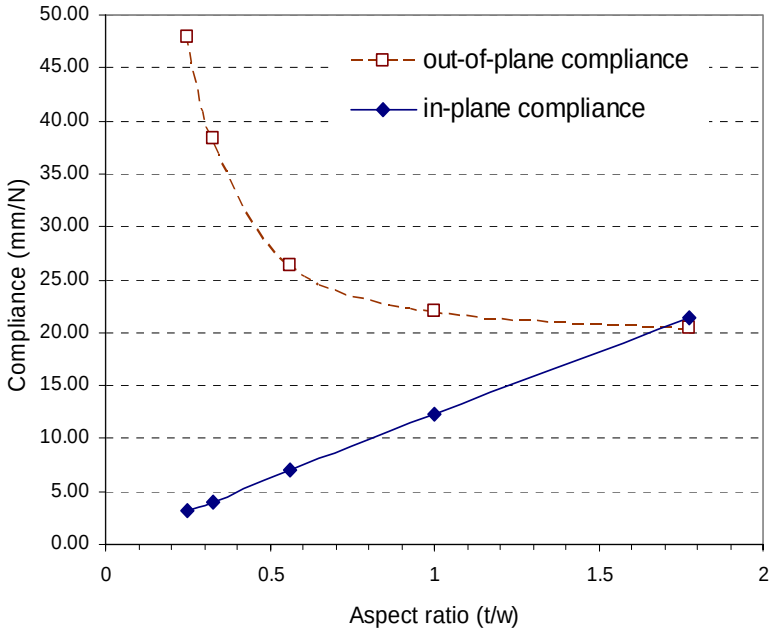


Figure 3.9: Effect of aspect ratio on the mechanical compliance of the "S-shape" leads. (A = w×t = constant for a constant resistance)

3.3.3. Structural Effect on Electrical Parasitics

The geometry of a lead also determines its electrical parasitics including resistance (R), capacitance (C) and inductance (L). The capacitance of a SoL interconnect is usually very small (10^{-3}-10^{-2} pF) because of the following reasons [3.9, 3.11]: First, as illustrate in Figure 3.10, a lead has very small surface area parallel with the on-chip wires due to the relatively short length and small width. Second, the SoL MEMS interconnects are surrounded by air in space, which is an excellent insulating material with low relative dielectric constant.

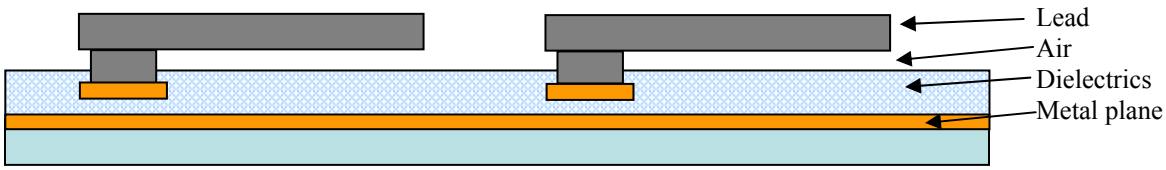


Figure 3.10: Schematic diagram of the SoL interconnects relative to the nearest metal level/ground plane for the approximate calculation of capacitance [3.11].

In contrast, resistance and inductance of a lead need to be carefully considered because a high mechanical compliance requires a smaller cross-sectional area and a larger arc radius for a lead, which may result in large resistance and inductance. Resistance can be simply calculated based on the resistivity and geometries. Calculation of inductance involves definition of a loop, which consists of self-inductance and mutual inductance [3.12]. The previous study of Patel [3.11] concluded that the self-inductance of a lead is usually larger than the mutual inductance (2.6 ~5 X) for two adjacent leads. In addition, the self-inductance of a conductor is highly dependent on its geometries, while the mutual inductance between two adjacent conductors mainly depends on their relative positions [3.12, 3.13]. Thus, structural/geometric effect was only investigated for the self-inductance in this study.

To calculate the resistance and inductance for the leads, a simulation model is created using a three-dimensional (3-D) parameter extractor software called *Raphael*, a CAD tool offered by Technology Modeling Associates (TMA Inc.,). As illustrated in Figure 3.11, the inductance, L (henry), of a loop that is formed by a pair of shorted leads equals to the sum of their self-inductance (L_1 and L_2) subtracted by the 2X of their mutual inductance, M (henry), according to [3.12, 3.13]:

$$L = L_1 + L_2 - 2M \tag{3.1}$$

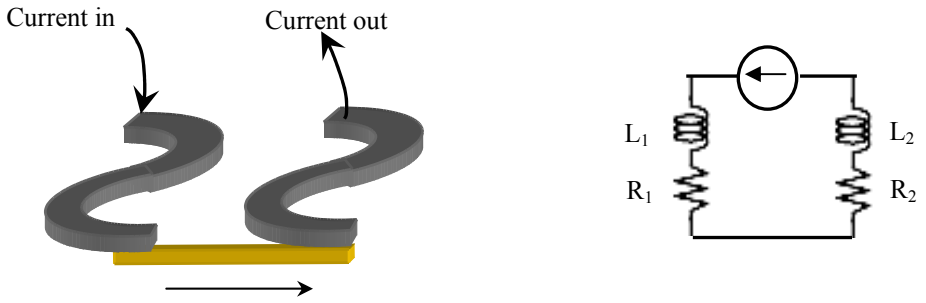


Figure 3.11: Schematic diagram of a pair of shorted SoL interconnects that form a loop for the inductance calculation using *Raphael* (a shorting between the two leads was created in the model; arc radius: ~ 30 μm; resistivity of Cu ~ 1.7×10^{-8} Ω·m).

In Figure 3.11, when the second lead is shorted ($L_2 = 0$ henry, $R_2 = 0$ Ω), the calculated overall inductance becomes the self-conductance of a single lead:

$$L = L_1 \tag{3.2}$$

The calculated resistance and the self-inductance of a Cu lead are plotted as a function of its thickness and width in Figure 3.12 and Figure 3.13 respectively. As expected, both resistance and self-inductance of a lead increase as its width or thickness decreases. For a given lead width, the resistance decreases rapidly when the lead thickness increases because of the change in the cross-sectional area of a lead (A = w×t). A low resistance (< 50 mΩ) can be obtained with a lead thickness larger than 5μm for the lead width ranging from 15 μm to 30 μm. In contrast, the self-inductance decreases steadily when the lead thickness increases. For example, the self-inductance of a lead (15 μm wide) is reduced from 0.11 nH to 0.09 nH (reduction of ~ 18%) when its thickness increases from 2.5 μm to 15 μm.

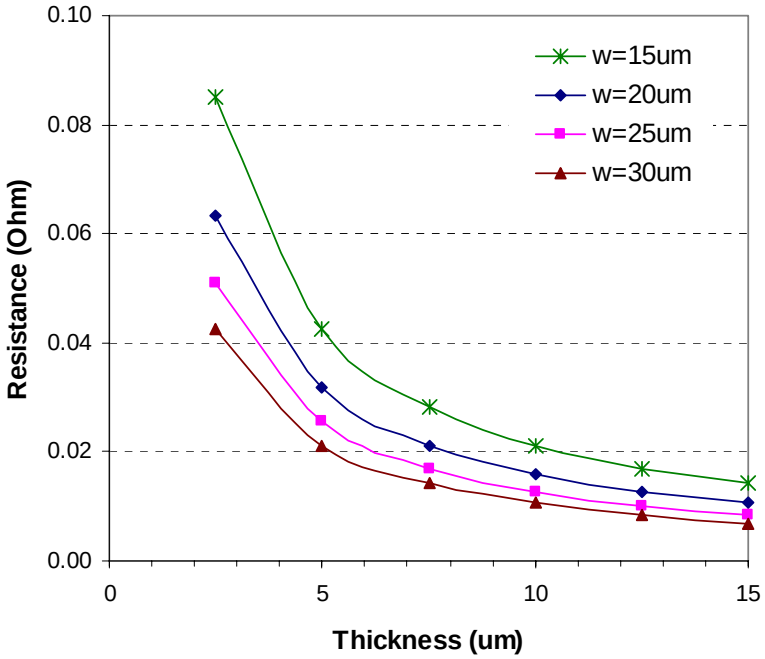


Figure 3.12: Resistance of an "S-shape" lead as a function of the lead thickness and width with a given arc radius of 30 μm and a lead length of 190 μm.

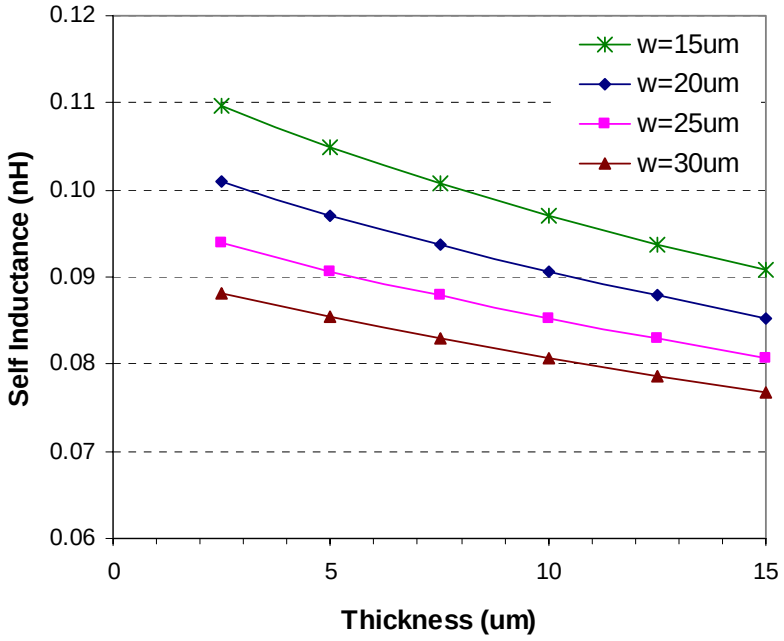


Figure 3.13: Self-inductance of an "S-shape" lead as a function of the lead thickness and width with a given arc radius of 30 μm and a lead length of 190 μm (Frequency ~ 1 GHz).

Since the self-inductance is a more complex function of the geometries and dimensions [3.12], its dependence on the aspect ratio (t/w) was also studied. Figure 3.14 shows the calculated self-inductance as a function of the aspect ratio (t/w) for cross-sectional area of 100 μm^2 and 225 μm^2 respectively. The constant cross-section area was used to maintain a constant DC resistance for each case. Obviously, the self-inductance is smaller when the lead cross-sectional area is larger. For a given lead cross-sectional area, the maximum self-inductance is observed for an aspect ratio of 1:1 and is reduced by ~ 8.6% when an aspect ratio of 0.25:1 is used.

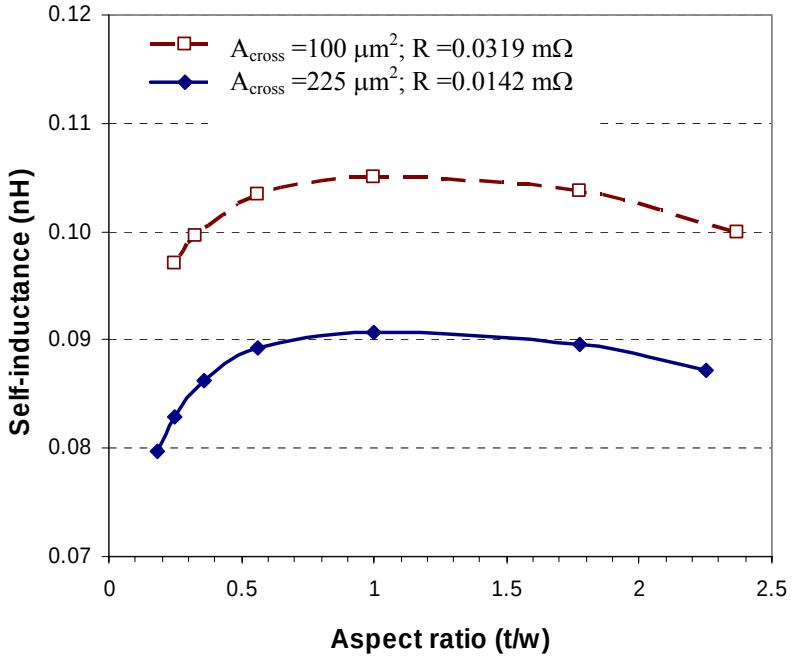


Figure 3.14: Self-inductance of an "S-shape" lead as a function of the aspect ratio (t/w) for various lead cross-section areas with a given arc radius of 30 μm and a lead length of 190 μm.

3.4. General Design Guidelines

Based on the above analysis of mechanical compliance and electrical parasitics of the SoL MEMS interconnects, several general design guidelines are proposed as below:

1. The distance between a SoL chip and its package substrate must be maintained by certain spacers considering the vertical deformation of the MEMS leads under a large weight of a heat sink.
2. The MEMS leads should be orientated properly such that the displacement during thermal excursion is closer to their transverse direction because the magnitude of in-plane compliance is the maximum in the transverse direction and is the minimum in the longitudinal direction.

3. The trade-off between in-plane and out-of-plane compliance need to be considered for the aspect ratio (w/t) of the leads during the structural design.

4. The requirements for mechanical compliance and electrical parasitics are opposing in terms of the cross-sectional area. In general, a larger cross-sectional area means better DC resistance, better current carrying capability, and smaller self-inductance but a smaller mechanical compliance.

3.5. Summary

In this chapter, FEM simulation was performed to illustrate the mechanical benefits of MEMS leads as the compliant I/O interconnects. The results indicate that a SoL MEMS interconnect induces much smaller shear force on a chip pad compared to that from a C4 solder joint, which means a smaller impact on chips with mechanically fragile low-K dielectrics. The need for underfill can be eliminated by SoL MEMS interconnects since the compliant leads can compensate for the CTE mismatch. The influence from the package weight (heat sink) was also analyzed based on the vertical deformation of the MEMS leads. Furthermore, structural effects on the mechanical compliance and electrical parasitics were studied through simulation and several general design guidelines were proposed.

Chapter 4. Fabrication of an On-Chip Microchannel Heat Sink and Assembly with Thermal-fluidic I/O Interconnects

4.1. Introduction

Heat dissipation in microprocessors will reach a level that necessitates chip-scale liquid cooling in the future. In comparison to the bulky forced-air heat sinks for the conventional microprocessor packages, ultra small form factors can be realized by integrating the microfluidic heat sink directly into an IC chip. In addition, liquid cooling at the microscopic level offers a higher heat transfer efficiency than that of the forced-air cooling mechanism. Meanwhile, the complex thermal interface related issues can be completely eliminated when the heat sink is a part of the chip. As illustrated in Figure 4.1, a prototype on-chip microchannel heat sink has been proposed to be integrated inside a wafer-level chip-scale package and cooled by liquids directly [4.1, 4.2].

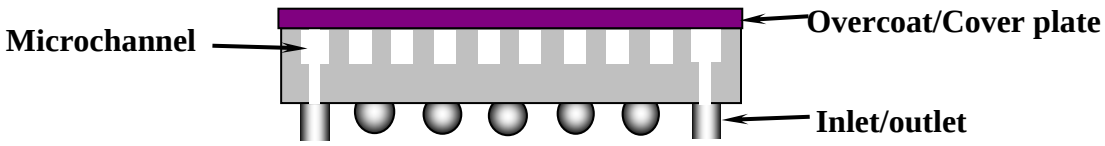


Figure 4.1: Schematic illustration of a microchannel heat sink integrated directly on a flip chip with thermal-fluidic inlets/outlets for the cooling liquid.

In this chapter, novel processes are developed to fabricate microfluidic cooling channels at wafer level. Through-wafer vias and micro-pipes are then proposed as novel thermal-fluidic I/O interconnects. The wafer-level integration processes are described and the issues associated with fluidic interconnection are then addressed for conventional flip-chip assembly with underfill. The board-assisted fluid delivery is also introduced to enable compact packages, especially for the multi-chip systems with high power dissipation.

4.2. CMOS Compatible Fabrication of On-chip Microfluidic Channels

By definition, any channels with dimensions less than 1 mm and greater than 1 μm can be called microchannels. Currently, most microchannels fall into the range of 30 to 300 μm. [4.3] Microchannels can be fabricated using micromachining, molding, or embossing in a variety of materials, such as Si, glass, metals or polymers [4.4 – 4.6]. The most important feature of the microchannels is their large surface-to-volume ratio, which leads to a high rate of heat transfer (or heat transfer coefficient). In addition, the microchannels can be integrated close to the microelectronic components to enable compact heat sinks. Microchannel heat sinking was first proposed for very large scale integrated (VLSI) electronic component in 1980s. Tuckerman and Pease studied chip cooling with an on-chip microfluidic heat sink and demonstrated that a heat flux of ~790W/cm^2 can be removed with a temperature rise of 71°C [4.7]. This translates into a thermal resistance as low as 0.09ºC/W. Following this landmark work, numerous studies have been carried out to implement on-chip microchannel cooling [4.8-4.10].

However, fabrication is a major challenge for the implementation of microchannel heat sinks. Conventional microchannel fabrication methods usually utilize direct wafer bonding. Field-assist bonding (anodic bonding) is the most common bonding technique for high-quality bonding of Si wafers, which requires ultra smooth/clean bonding interfaces, high pressure, and high temperature (350 ºC~1000 ºC) and high voltage (500 V~1000 V) [4.11, 4.12]. These processing conditions are not very friendly to back-end-of-the-line (BEOL) wafers, where CMOS devices and on-chip interconnects are completed. Therefore, CMOS compatible processes are necessary for fabrication of on-chip microchannels following BEOL processing. Two approaches have been studied in this work: one is the intermediate bonding of a cover plate using a polymer glue (Avatrel 2195P, Promerus, LLC) at low temperature (<200ºC); another is a

monolithic process using a sacrificial polymer that can be thermally decomposed at low temperatures (<200 ºC).

4.2.1. Microchannels Enclosed by Glue Bonding

The first approach is relatively simple and requires only a thin glue layer on the cover plate (Figure 4.2). Deep trenches (h > 100 μm) are first etched into the back-side of a Si wafer using the "Bosch Process" in an inductively-coupled-plasma (ICP) etcher. Prior to bonding, a thin layer of SiO_2 (~2000Å) is deposited at the back-side of the Si wafer with plasma-enhanced chemical vapor deposition (PECVD) to improve the adhesion with polymers. The polymer glue is applied onto a cover plate by spin-coating and a soft-bake step is performed at 100 ºC for 5 minutes to remove the solvents. The cover plate is then flipped over and is placed onto the back-side of the Si wafer with pre-etched trenches. Under a compression force (4 kg) in an oven, the two surfaces are kept in good contact and the glue is cured under a controlled temperature profile. The curing time at a peak temperature of 160 ºC is 2 hrs.

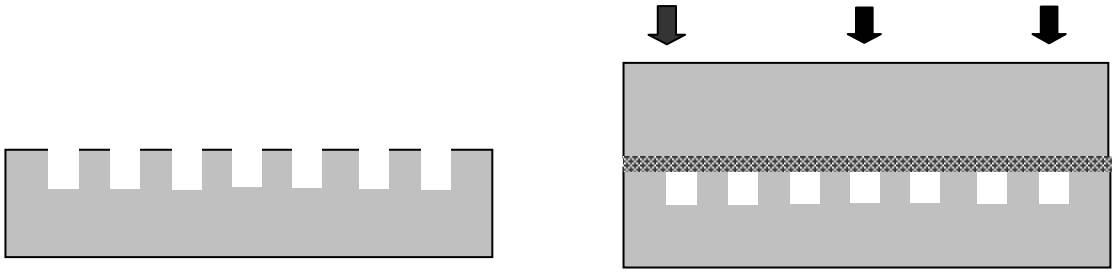


Figure 4.2: Schematic illustration of a low-temperature process of micrchannel fabrication in Si wafer with glue bonding (a) Trench etching and surface cleaning (b) curing of the glue layer under compression.

A strong bond is then formed between the cover plate and the Si wafer by the cured glue. The cover-plate is either a Si wafer or a Pyrex glass wafer, which has a CTE of 2.8 to match with

that of the Si substrate. To reduce the overall thickness of the final package, the cover-plate may be mechanically thinned by grinding.

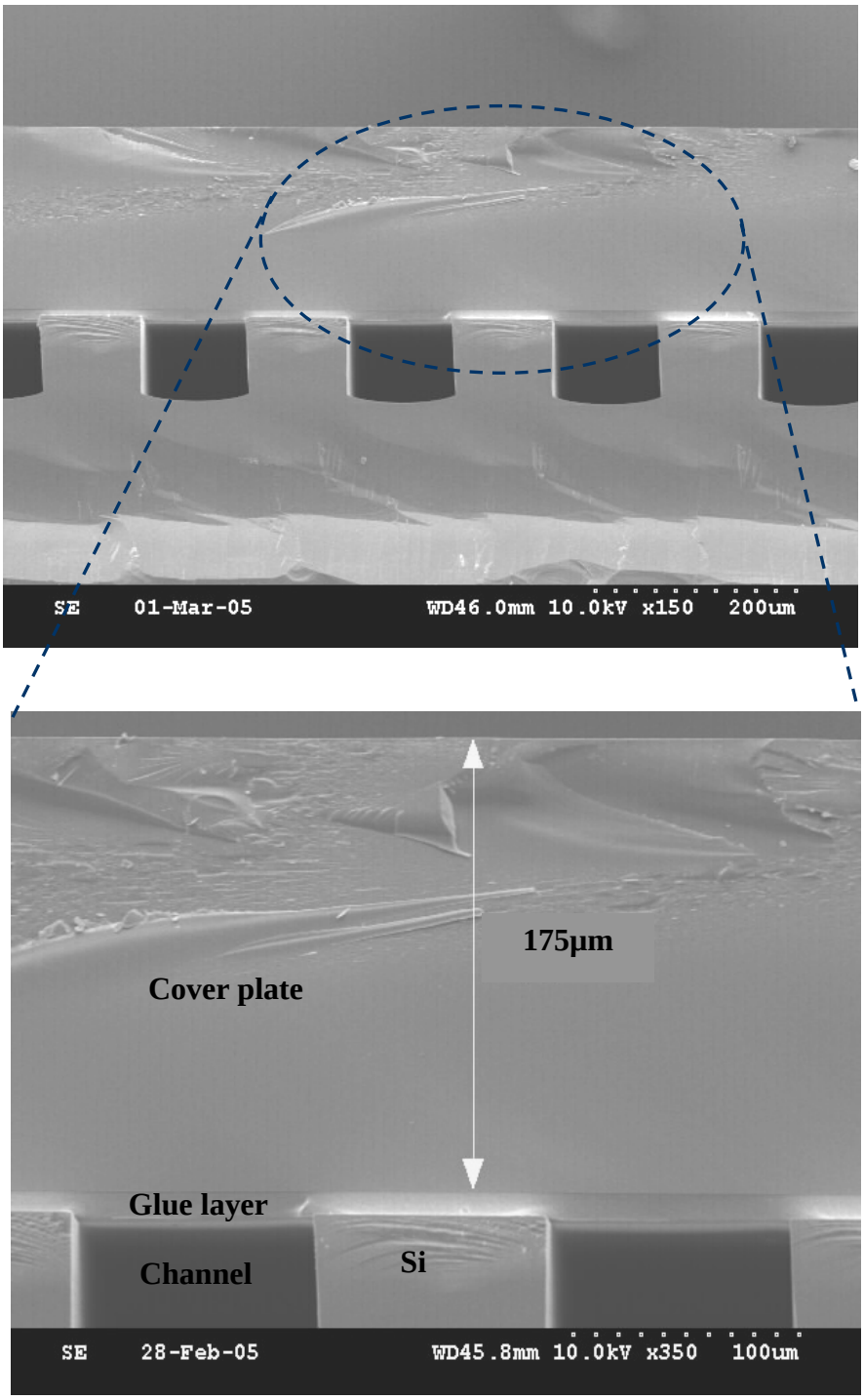


Figure 4.3: Cross-sectional SEM photographs of microchannels enclosed by glue bonding of a glass cover plate.

Figure 4.3 shows cross-sectional SEM images of the bonded microchannels, which reveal a uniform bonding interface between the cover plate and the top surface of the trench. It can be seen that the polymer slightly sag into the trenches because of wetting and the compression force.

4.2.2. Monolithic Fabrication of Microfluidic Channels using a Sacrificial Polymer

The second approach is novel and involves trench filling with a sacrificial polymer by spin-coating, surface planarization through mechanical polishing, over-coating with a layered structure, and decomposition of the sacrificial polymer by heat treatment, as shown in

Figure 4.4.

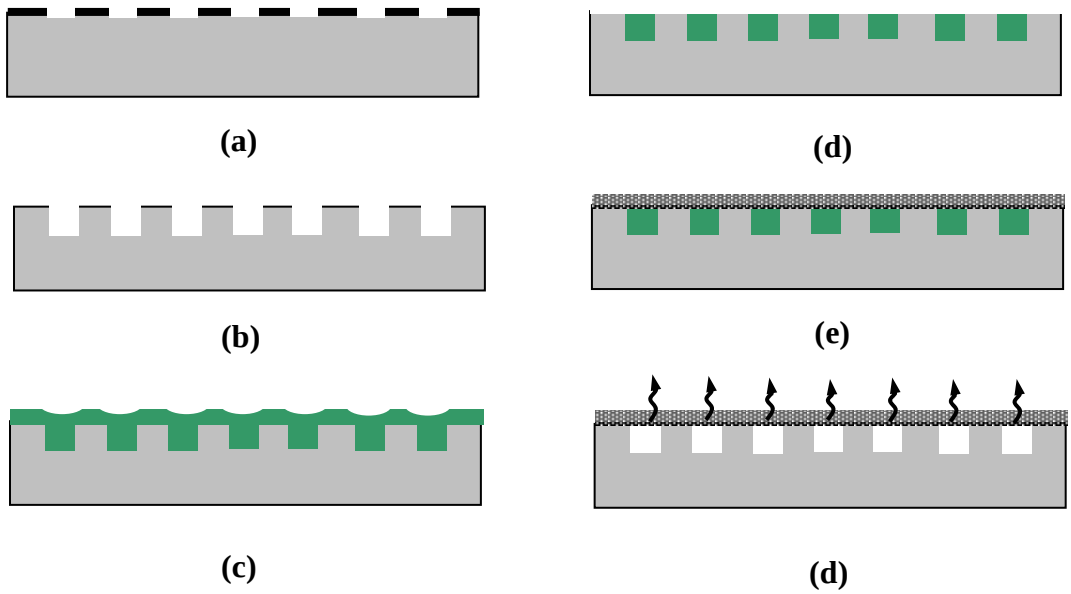


Figure 4.4: Schematic illustration of low-temperature monolithic process of micrchannel fabrication in Si wafer through a sacrificial polymer and an overcoat. (a) Trench patterning(b) Trench etching and surface cleaning (c) Trench refilling by spin-coat (d) Polishing and descum (e) Over-coating with a layered structure (a porous SiO2 layer and a polymer layer) (f) Sacrificial polymer decomposition and overcoat curing.

Without the need for wafer bonding, this approach is monolithic and compatible with common wafer processing techniques. For instance, the spin coating and polishing operations are easily available in standard BEOL facilities. Another advantage is the resulting thin package profile since a thin overcoat layer can be readily obtained. Depending on the spin-coating speed, the thickness of a polymer overcoat may be as thin as tens of micrometers. Two key elements in this novel approach are the sacrificial polymer and the layer overcoat structure.

4.2.2.1. Trench Filling with a Sacrificial Polymer

Since the target depth of the Si trenches is large (≥100μm), sacrificial polymer materials and the required spin-coating conditions need to be carefully selected to achieve optimal filling effect. Two formulas of the sacrificial polymer (Unity 200, Promerus, LLC.) are available for this work. One is the low-viscosity type, and the other is the high-viscosity type.

Figure 4.5 and Figure 4.6 show the experimental results of deep trench filling with two types of sacrificial materials at various conditions. In general, a slower spin speed can result in a thicker coating layer, which means a better coverage of the trenches. However, spin speed of less than 500 rpm leads to poor coating uniformity across a wafer. The trench filling (or coverage) also depends on the viscosity of the polymer. A low-viscosity sacrificial polymer contains a large portion of solvent and shows poor trench filling effect. Although the low-viscosity polymer seems to easily fill up the deep trenches while it is in the liquid state, the volume is largely reduced after soft bake (shrinking effect).

As shown in Figure 4.5, even with a slow spin speed (800rpm), the 100μm deep trenches can only be filled by 20% after three spin steps. Therefore, the low-viscosity is not suitable for deep trenches because the spin-coating and baking processes have to be repeated multiple times

for a complete coverage. In contrast, with the high-viscosity type material, the 100 μm deep trenches can be covered by nearly 100% after 1 spin step at 1500 rpm, as shown in Figure 4.6.

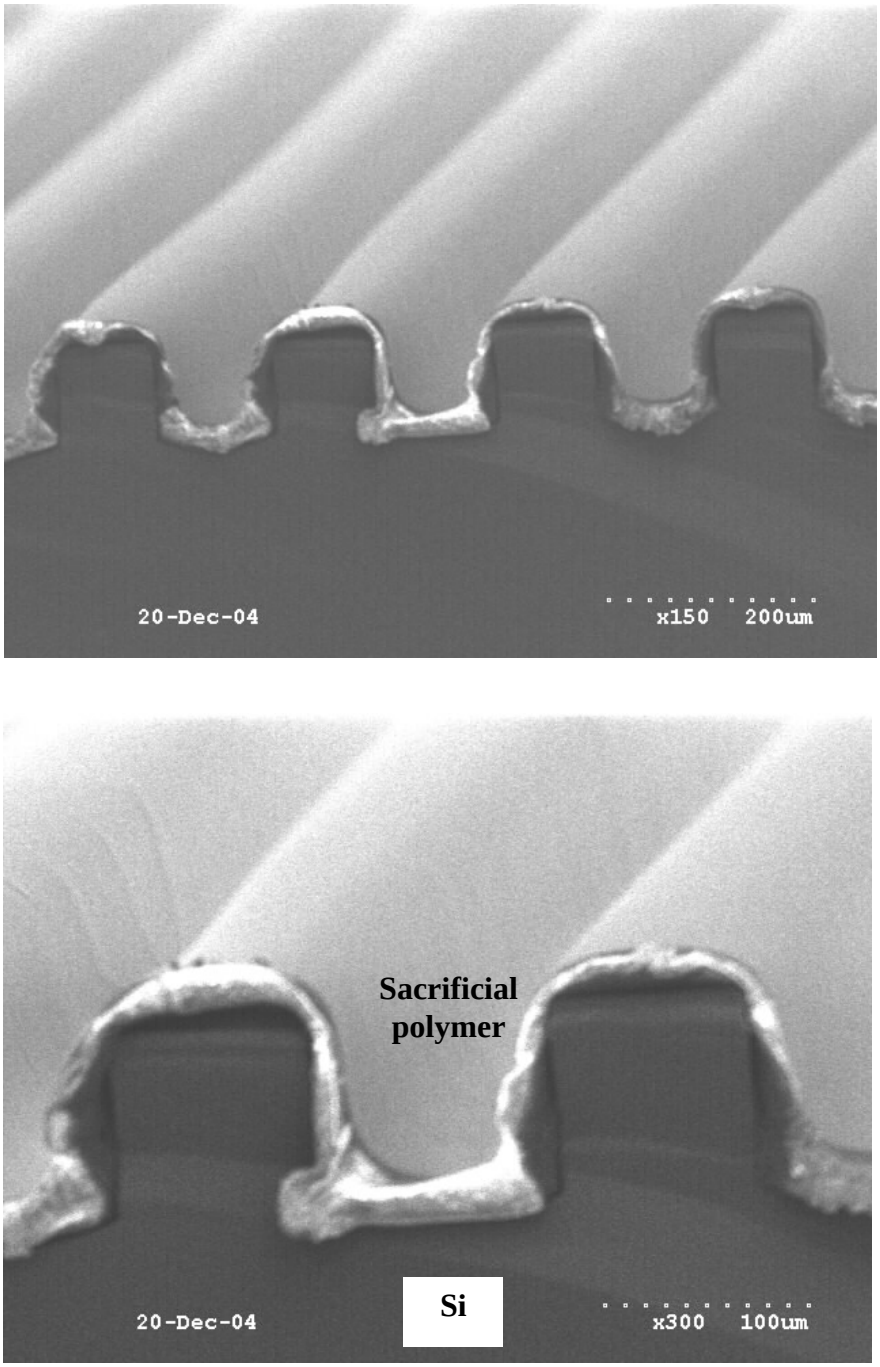


Figure 4.5: Cross-sectional SEM phototgraphs of the deep trenches after filling with low-viscosity sacrificial polymer (after 3 spins at 800rpm).

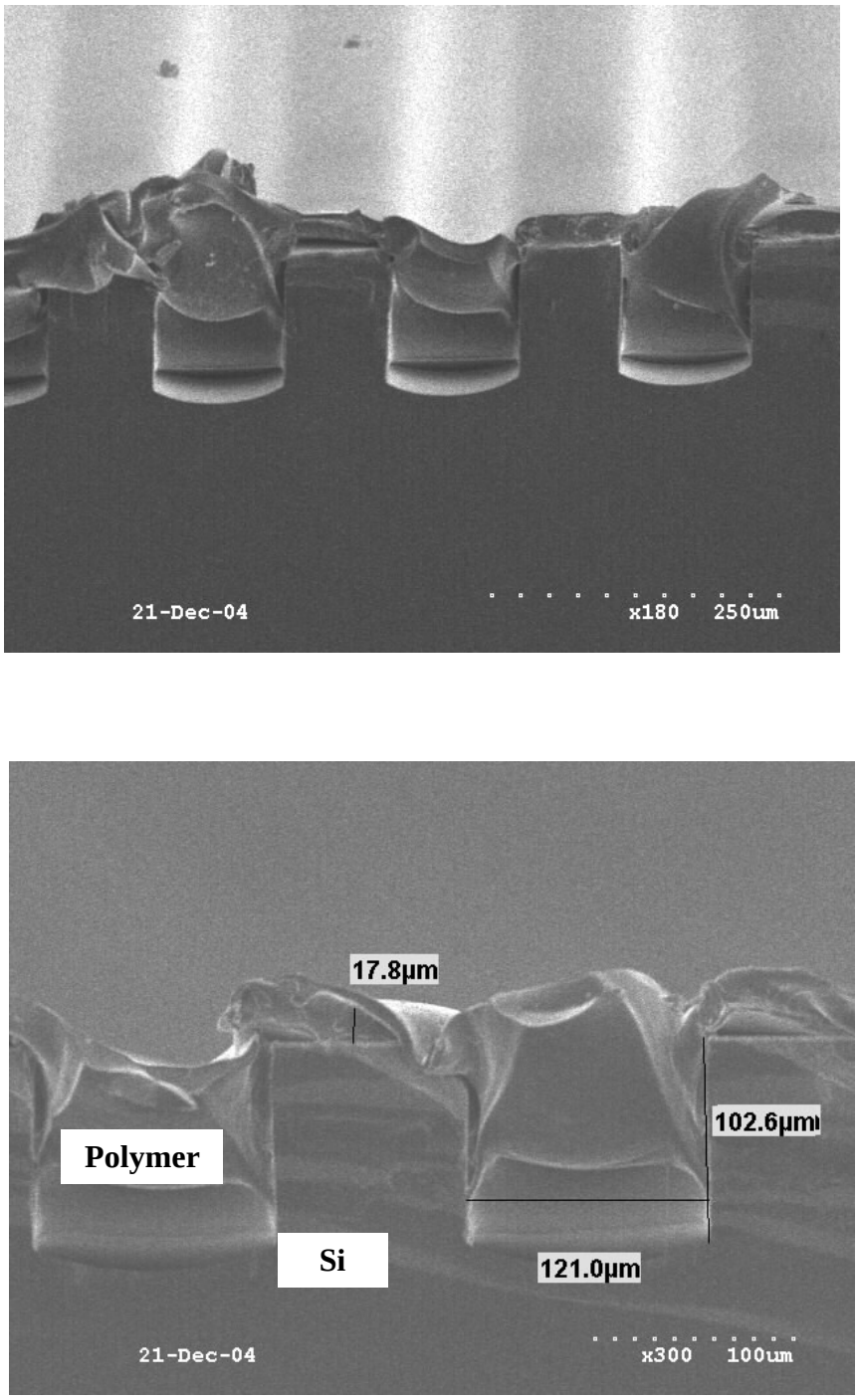
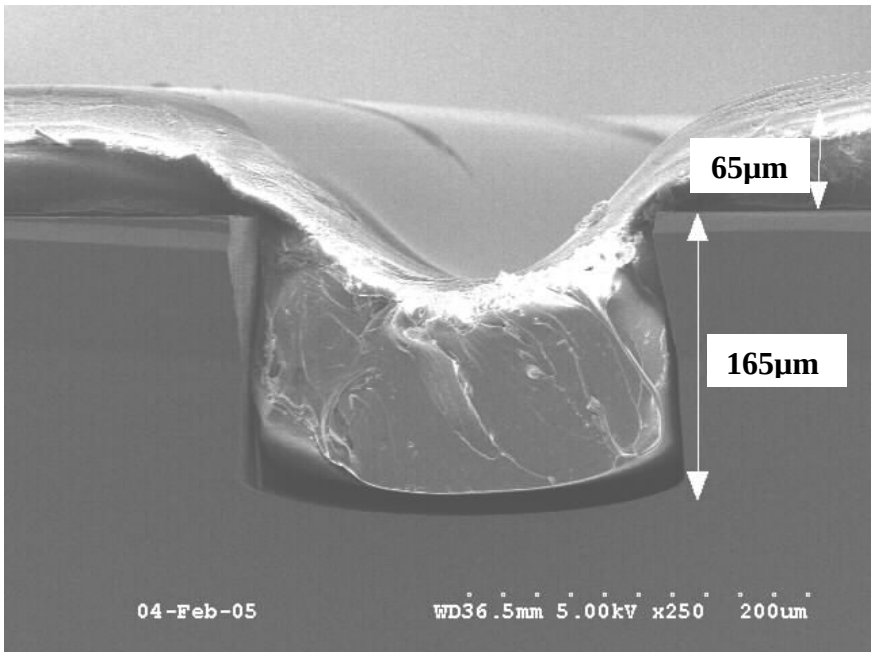


Figure 4.6: Cross-sectional SEM phototgraphs of the deep trenches after filling high-viscosity sacrificial polymer (1 spin at 1500rpm)

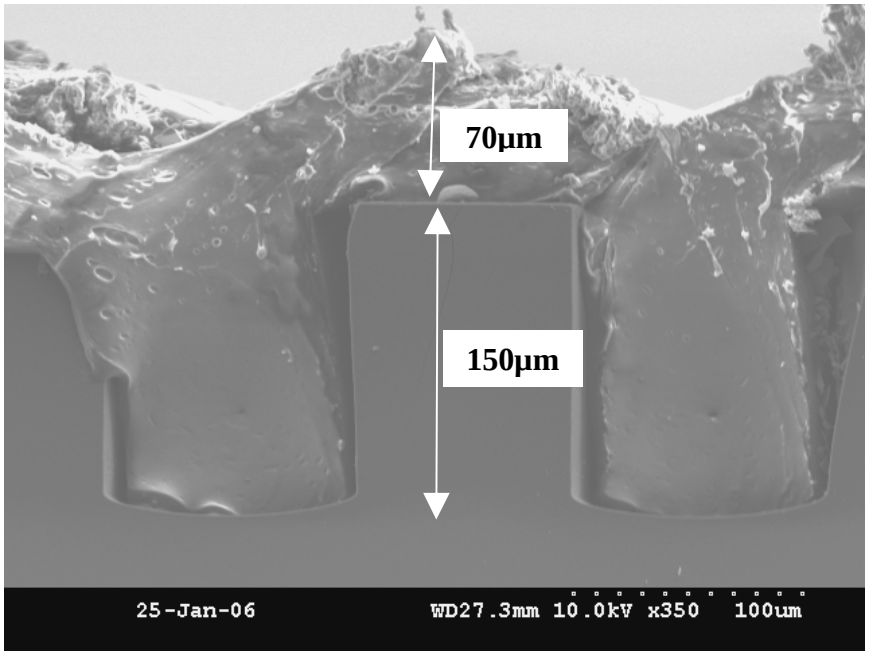
The reason is because there is only a little amount of solvent in the high-viscosity polymer and the volume shrinkage during soft-bake is small. Therefore, the high-viscosity type sacrificial polymer is more desirable for the trench filling process. For deeper channels, the spin speed should be further reduced or the spin step may be repeated. For instance, with a spin speed of 1000 rpm, channels as deep as 160 μm can be filled up, as illustrated in Figure 4.7. Furthermore, the trench filling effect is also related to the aspect ratio of the trenches when the same type polymer is used. As shown in Figure 4.7a, the "sagging effect" is more obvious for wider channels with a smaller aspect ratio (h/w). In contrast, the sacrificial polymer tends to "pile up" above the substrate during spreading and spin coating for those densely populated channels with a higher aspect ratio (Figure 4.7b). Such an effect is beneficial to the coverage of the densely populated channels with high aspect-ratios, which are desirable for a larger heat exchanging surface area. Nevertheless, trenches as deep as 250 μm should be filled by at least two spin-coating steps to ensure a good coverage. Results of trench filling experiments for various channel depths are summarized in Table 4.1.

Table 4.1 Processing conditions for trench filling with high-viscosity polymer for various channel dimensions.

Channel Height (μm)	**Channel Width (μm)**	**Spin speed (rpm)**	**Number of coating steps**	**Coverage**	**"Pile-up" thickness (μm)**
~30	~100	2000	1	> 100%	~12
~100	~100	1500	1	> 100%	~17
~100	~120	1500	1	> 100%	~17
~150	~100	1000	1	> 100%	~70
~170	~250	1000	1	< 90%	~65
~200	~100	1000	2	> 100%	~ 100



(a)



(b)

Figure 4.7: Cross-sectional SEM phototgraphs of the deep trenches with various aspect ratios after filling with the high-viscosity sacrificial polymer at 1000 rpm. (a) aspect ratio (h/w) is ~ 0.66 (b) aspect ratio (h/w) is ~ 1.5.

4.2.2.2. Surface Planarization with Mechanical Polishing

As described above, the spin-coating process not only fills up the trenches but also builds up an extra layer of the sacrificial polymer above the wafer surface. The extra polymer film becomes thicker when the spin-coating step is repeated and must be removed before over-coating. SiC grinding paper (Struers Inc.,) with various particle sizes is used for mechanical polishing. A constant pressure must be evenly applied onto a sample during polishing process to ensure a uniform and flat surface. Otherwise, polymer can be "pulled" out of the trench since it is much softer than the Si surface, as illustrated in Figure 4.8.

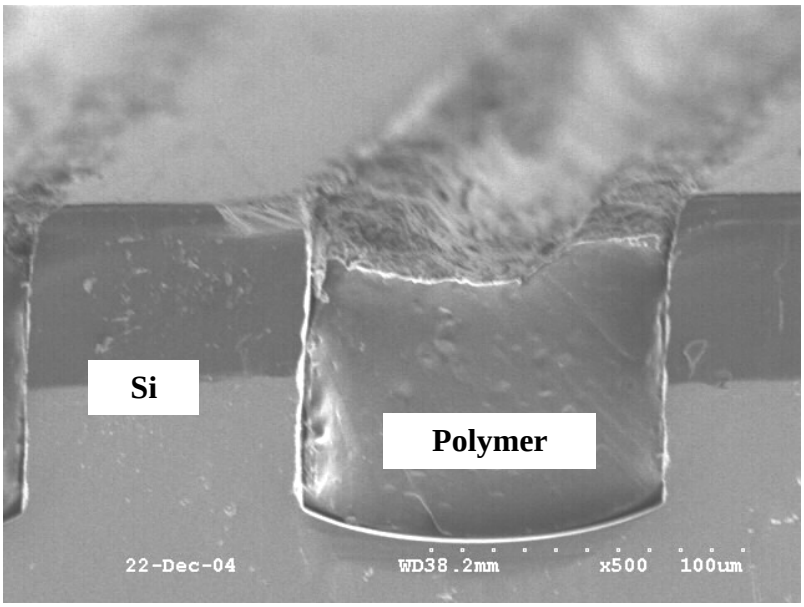


Figure 4.8: Cross-sectional SEM phototgraphs of the deep trenches after mechanical polishing: (The polymer inside the trenches was partially "pulled" out during polishing)

To reduce such an effect, experiments were performed to optimize the polishing processes. A good polishing sequence for the filled samples should begin with rough polishing paper and end with fine polishing paper to reduce overall polishing time and improve the smoothness. For a "pile-up" thickness of ~100 μm, the following steps are suggested: grinding

with a polishing paper of #320 for 30 mins, followed by grinding paper of #800 for 30 mins, and followed by grinding paper of #1200 for 10 mins. Figure 4.9 shows the overview and cross-sectional images of the samples polished with improved processes. Much flatter surfaces can be observed at the top of the sacrificial polymer. It should be pointed out that the mechanical polishing approach was used for the reason of easy availability in this work. The commonly used chemical mechanical polishing (CMP) in semiconductor manufacturing can potentially offer better polishing effectiveness and efficiency.

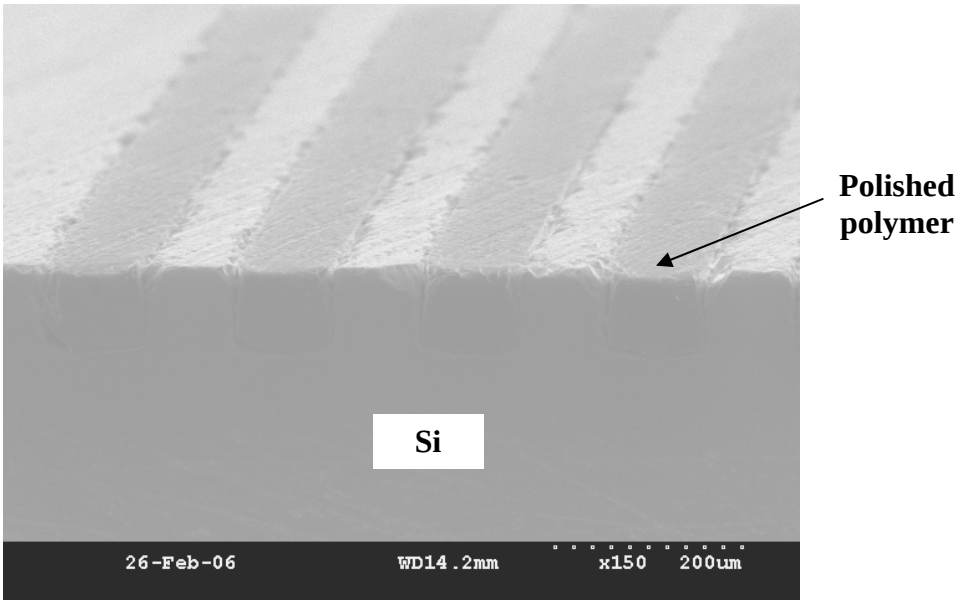


Figure 4.9: Cross-sectional SEM photograph revealing the flatness of the polished polymer surface.

4.2.2.3. Overcoating and Decomposition Processes

After the extra polymer above the substrate surface is removed by mechanical polishing, the trenches must be covered with an overcoat to form the enclosed microchannels. A layered

overcoat was applied to meet two requirements: the permeability during decomposition of the sacrificial polymer and the hermeticity after curing of the structural polymer. A SiO_2 thin film (1~2 μm) was first deposited with PECVD at low temperature (~150 °C) and a thicker layer of Avatrel 2195P was then spin-coated and cured as the structural polymer (~25 μm). Since the SiO_2 film is porous, it allows permeation of the gaseous products from decomposition of the sacrificial polymer. The SiO_2 also plays an important role in maintaining the structure integrity of the overcoat by preventing "sagging" of the above structural polymer. In fact, decomposition of the sacrificial polymer and curing of the structural polymer occur simultaneously during a heat treatment in a program-controlled oven. The temperature profiles are summarized in Table 4.2 for the two versions of sacrificial polymers: Unity 200 and Unity 200P. The major difference between the two types of sacrificial polymer is that the Unity 200P contains the photo-acid-generator and can be decomposed at lower temperatures (≤ 200 °C), while the Unity 200 can only be composed at higher temperatures (≥ 230 °C) [4.5].

Table 4.2 Heat treatment temperature profiles of Unity 200P and Unity 200NP in a nitrogen-purged oven.

Sacrificial Polymer	Step 1	Step 2	Step 3	Step 4
Unity 200P	Ramp to 130 °C (3 °C/min)	Ramp to 170 °C (1 °C/min)	Dwell at 170 °C for 2hrs	Cool with the oven
Unity 200NP	Ramp to 230 °C (3 °C/min)	Ramp to 260 °C (1 °C/min)	Dwell at 260 °C for 2hrs	Cool with the oven

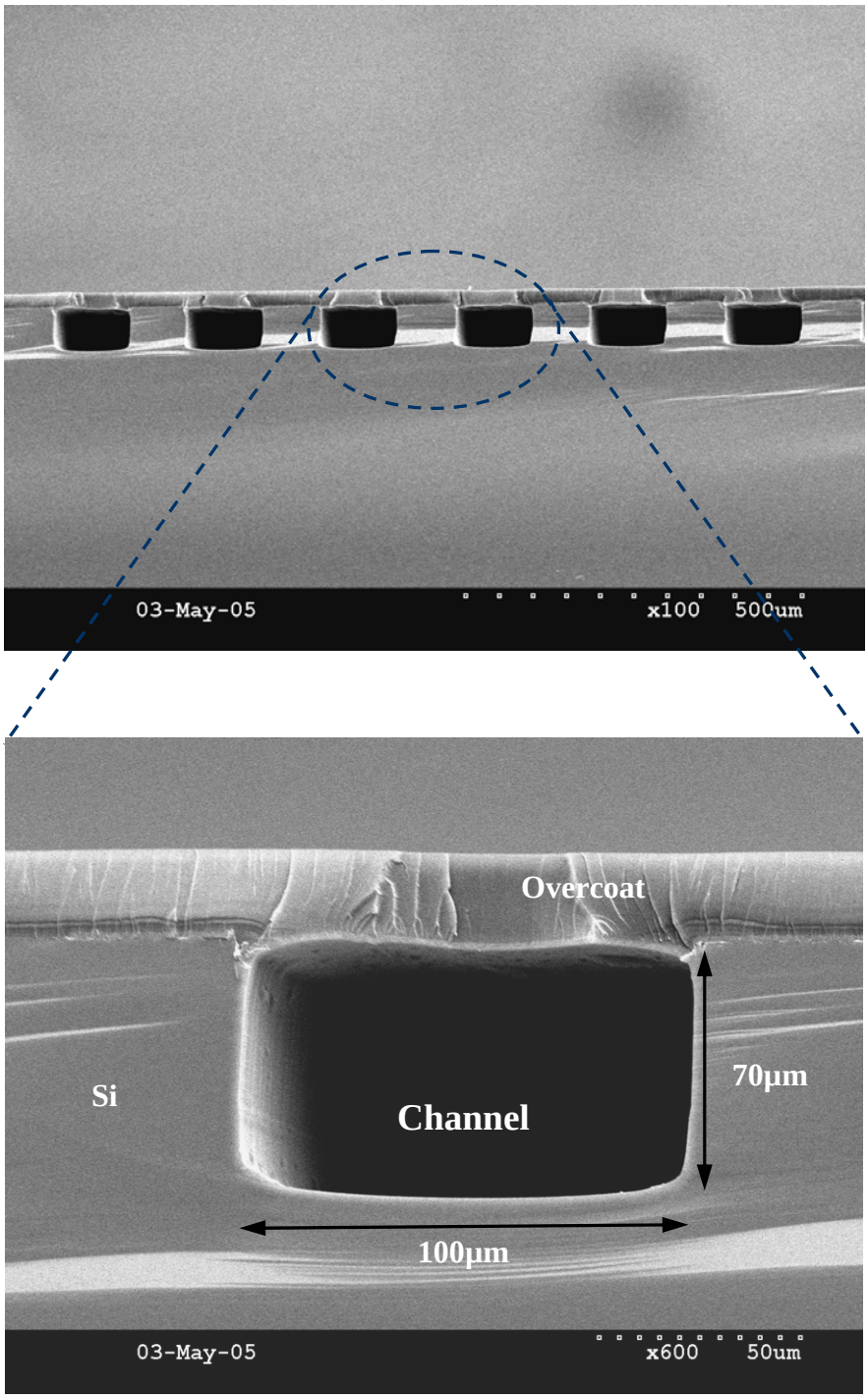


Figure 4.10: Cross-sectional SEM photographs of completed microfluidic channels enclosed by a layered overcoat after decomposition and curing.

Figure 4.10 shows the cross-sectional SEM images of the completed microchannels after the heat treatment. As expected, the sacrificial polymer inside the trench was completely removed during the decomposition and an excellent interface can be observed between the layered overcoat and the substrate. Meanwhile, the structural integrity (flatness and adhesion) of the overcoat is maintained. To further increase the mechanical strength and hermeticity of the mcircochannels, an additional overcoat layer can be easily applied. As shown in Figure 4.11, after a second layer of overcoat is applied and cured, the top surface of the polymer based microchannels is still flat with an increased thickness (~50 μm in total).

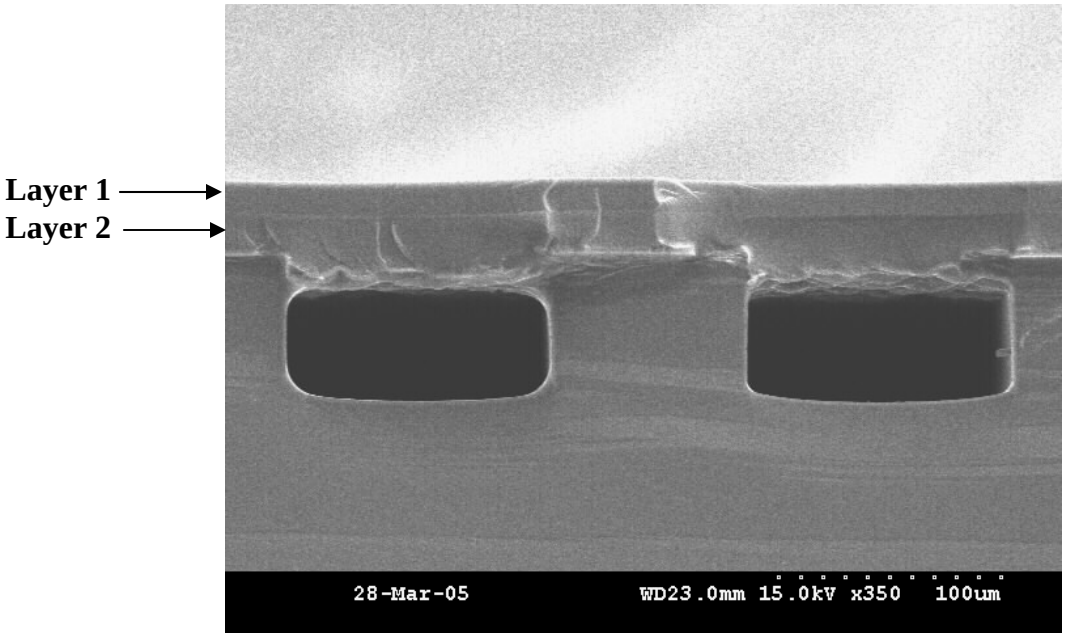


Figure 4.11: Cross-sectional SEM photograph of completed microfluidic channels enclosed by two layers of polymer overcoat.

In addition to the dielectric polymer, many other materials may also be used as water-proof coating, such as metal layers deposited by DC-sputtering and electro/electroless plating, or spin-on glass, etc.

4.2.3. Testing of the Polymer-capped Microchannels

The important requirements for the overcoat layers include strong adhesion, good hermeticity, and high mechanical strength under high pressure, which are critical for the reliability of the microchannels. Table 4.3 lists the basic physical properties of several dielectric polymers that are commonly used for wafer-level packaging. In this work, Avatrel 2195P (Promerus, LLC.) was used as the overcoat polymer because it has been known as a low-stress dielectric polymer in various packaging applications for several years [4.13 - 4.15]. Compared with other candidate polymers, Avatrel 2195P has the following advantages: it can be cured at low temperature and has a relatively high T_g; it is compatible with a variety of commonly used passivation films, such as SiO_2 and Si_3N_4, with good adhesion. More importantly, its moisture absorption rate is relatively low (< 0.1 % at 100% R.H.).

Table 4.3. Physical properties of various dielectric polymers used in wafer-level packaging applications [4.13, 4.16, 4.17].

Polymer	**CTE (ppm)**	**Tensile modulus (GPa)**	**T_g (°C)**	**Moisture absorption rate**	**Curing temperature (°C)**
Avatrel	~50	0.5	250~350	< 0.1 %	~160
Polyimide	~20	50	~430	2-3 %	~300
Su-8	~42	4.7	>200	0.3%	~160
BCB	~52	2.9	~350	~ 0.23 %	~250

4.2.3.1. Fluidic Characterization

As a new technique to fabricate the microfluidic channels, success of the thermal decomposition must be first confirmed with fluidic testing. The simplest test for fluidic continuity is to drive a fluid through the micrchannels using a syringe pump, as illustrated in Figure 4.12. In this work, DI water was used as the testing fluid. Soft plastic tubing and plastic tubes were used to connect the polymer-capped microfluidic channels with the test set-up. A two-parts epoxy glue was used to seal the connection. Once a sample passes the fluidic continuity and leakage check, a closed fluidic loop driven by a small mechanical pump is used to continuously test the hermeticity and strength of the polymer overcoat under high-pressure, as shown in Figure 4.13. In this set-up, a pressure transmitter (0~100 psi, Omega Engineering, INC.) was connected between the inlet and outlet to test the pressure drop dynamically. The measured data was collected by a software (Datalogger). Figure 4.14 shows the optical micrograph of a test sample, which consists of the monolithically fabricated microchannels that are aligned with fluidic manifolds. Although the polymer overcoat is only 30 μm in thickness, the microchannels can withstand a pressure of 2.5 atm (35 psi) during the continuous testing. No delamination or cracking was observed after a test for three hours.

The relation between the pressure drop and the flow rate on a single microchannel can be derived for fully developed laminar flow based on the classic hydraulic equations [4.18, 4.19]:

$$\Delta P = 4f\frac{L_c}{D_h}\frac{\rho v^2}{2} = 2f\,\mathrm{Re}\frac{L_c}{D_c^2}v\mu \tag{4.1}$$

$$\mathrm{Re} = \frac{\rho v D_h}{\mu} \tag{4.2}$$

where f (dimensionless) is the friction factor of the flow, L_c is channel length (m), D_h is the hydraulic diameter (m) of a microchannel, ρ is the density (kg/m^3) of a fluid, v (m/s) is the

velocity of the flow, and μ is the dynamic viscosity (Pa·s) of the working fluid. The hydraulic diameter, D_h (m), of a microchannel with a rectangular cross-section can be calculated as follows [4.18, 4.19]:

$$D_h = \frac{2W_c H_c}{W_c + H_c} \tag{4.3}$$

The friction factor, f (dimensionless), is related to the Reynolds number, Re (dimensionless), and the product of the two terms is usually a constant determined by the geometry and dimensions. For rectangular channels [4.3]:

$$f\,\mathrm{Re} = 24[1 - 1.3553\alpha + 1.9467\alpha^2 - 1.7012\alpha^3 + 0.9564\alpha^4 - 0.2537\alpha^5] \tag{4.4}$$

where α is the reciprocal of channel aspect ratio (if $W_c<H_c$, $\alpha=W_c/H_c$ and $H_c<W_c$, $\alpha=W_c/H_c$)

Taking into account the dimensions and the number of channels (n_c), the average fluidic velocity in multiple parallel microchannels is determined by the overall flow rate, $\dot{V}$ (m^3/s), based on:

$$v = \frac{\dot{V}}{n_c W_c H_c} \tag{4.5}$$

The pressure drop is then correlated to the physical properties of the fluid, the characteristics of the flow, and the geometries of the microchannel according to:

$$\Delta P = 2f\,\mathrm{Re}\frac{L_c}{D_h^2}v\mu = \frac{1}{2}f \cdot \mathrm{Re} \cdot L_c \cdot \frac{\mu \cdot \dot{V}(1 + W_c / H_c)^2}{n \cdot H_c \cdot W_c^3} \tag{4.6}$$

The overall pressure drop across the parallel rectangular microchannels should increase linearly with increasing flow rate for a given working fluid. The pressure drop is also inversely proportional to the number of microchannels for given channel dimensions. The number of microchannels is determined by the chip size and pitch of the microchannels if the channels are evenly distributed.



Figure 4.12: Fluidic continuity testing set-up for the microchannels (a syringe pump is used)

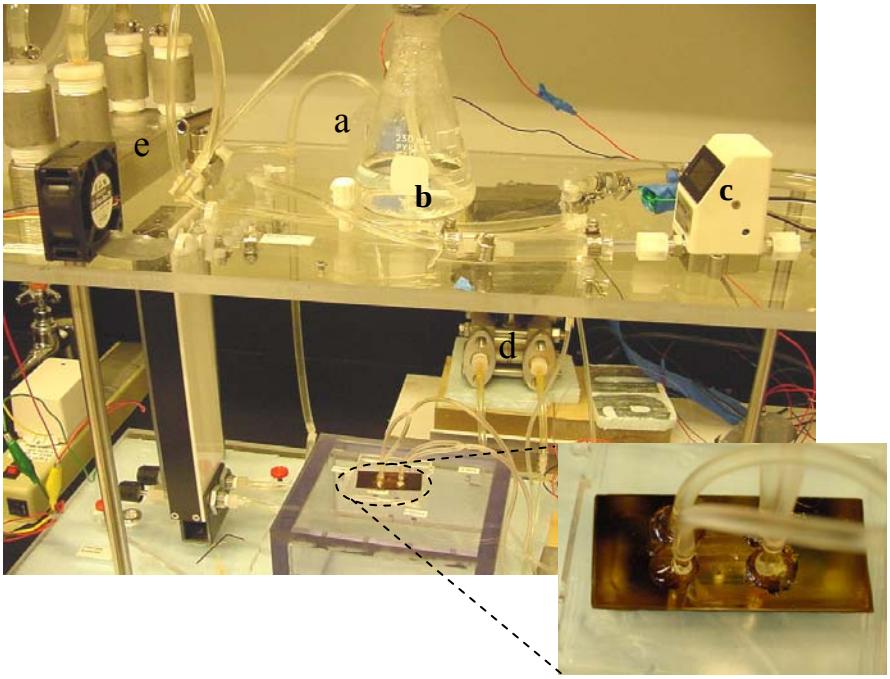


Figure 4.13: The test set-up for continuous high-pressure fluidic testing. (The key components include: (a) the mini pump, (b) DI water reservoir, (c) digital flow rate meter, (d) pressure sensor. (e) heat exchanging metal block with cold water.

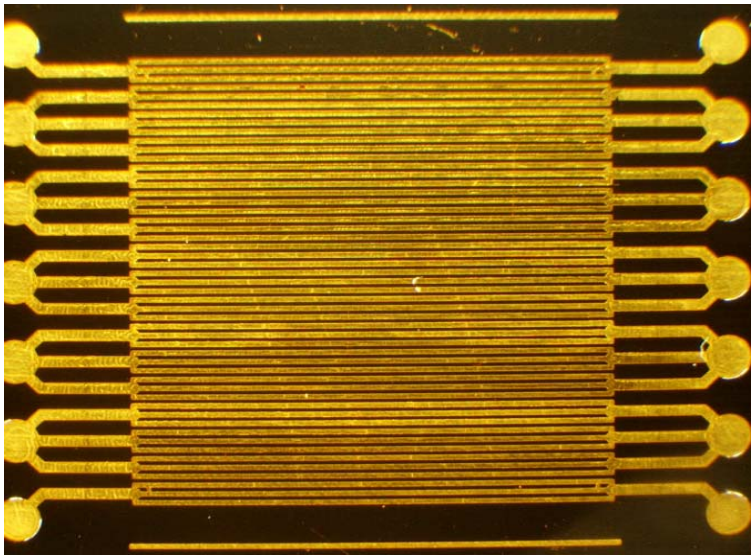


Figure 4.14: Overview of the test sample with monolithically fabricated microchannels. The large channels serve as the manifolds and the liquid flow splits into multiple small channels.

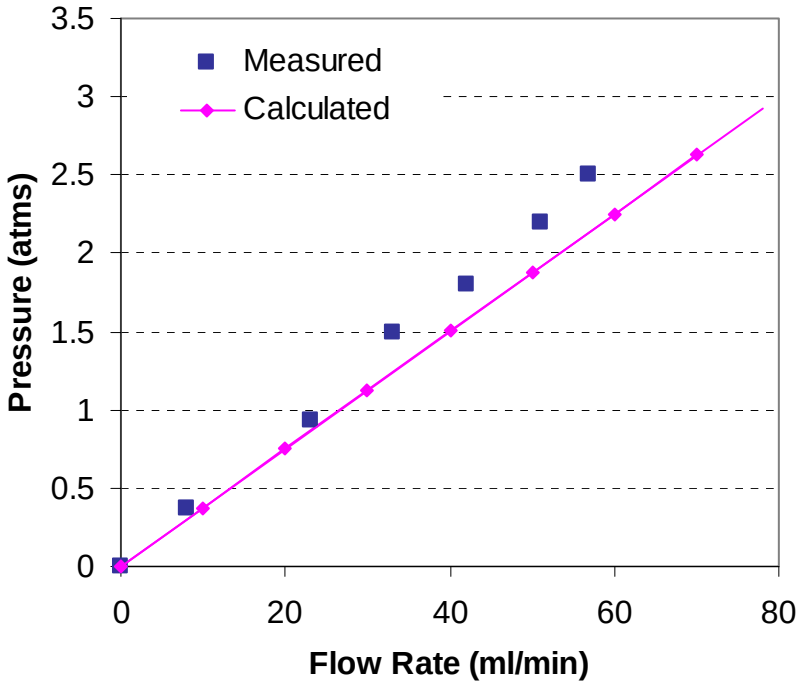


Figure 4.15: Flow rate as a function of the pressure drop for DI water in 18 microchannels. The measured data are close to the theoretical values calculated using Equation 4.6 (the parameters are: n_c ~18, μ~ 8.54×10^{-4} Pa·s, L_c ~ 1cm, W_c~100 μm and H_c ~ 70 μm).

Figure 4.15 illustrates the measured flow rate as a function of pressure drop for the 18 microchannels, which are linked with manifolds connected by two pairs of inlets/outlets. The theoretical values are also calculated using Equation 4.6. (n_c ~18, μ~ 8.54×10^{-4} Pa·s, L_c ~ 1cm, W_c~100 μm and H_c ~ 70 μm) and plotted for the purpose of reference. As shown in Figure 4.15, the measured data closely agrees with the trend of the theoretical plot, although there is a small deviation. The deviation between the measured results and calculated results is relatively small at low pressures. As the flow rate increases, the deviation becomes more obvious and is up to 15.7 % at the pressure of flow rate of 75 ml/min (measured pressure is ~2.5 atms). Such deviation may be introduced by non-ideal flow paths because of the tubing, the path of the manifolds, and the turning or splitting of the liquid flow, etc. In addition, under current experimental conditions, the physical dimensions along the fluidic paths are not perfectly uniform and are difficult to measure precisely.

4.2.3.2. Thermal cycling testing

Another reliability concern of the polymer-capped microchannels is the interfacial integrity of the layered overcoat during thermal stressing. The overcoat polymer, Avatrel 2195P, reportedly has good adhesion with various substrates and a low residual stress [4.13]. A thermal-cycling test was performed for the microchannels that were tested with high-pressure flow described above. To clearly observe the failure at interfaces, the sample with the microchannels was cleaved before they were placed in the thermal-cycling test chamber.

Figure 4.16 shows the cross-sectional SEM images of the microchannels after 1000 thermal cycles based on JEDEC Standard (Condition J of JESD 22-A104-B, 0-100°C, 3 cycles per hour). The high magnification image reveals that the adhesion between the overcoat polymer

and the Si substrate did not degrade and no cracking or delamination occurred under the thermal stressing.

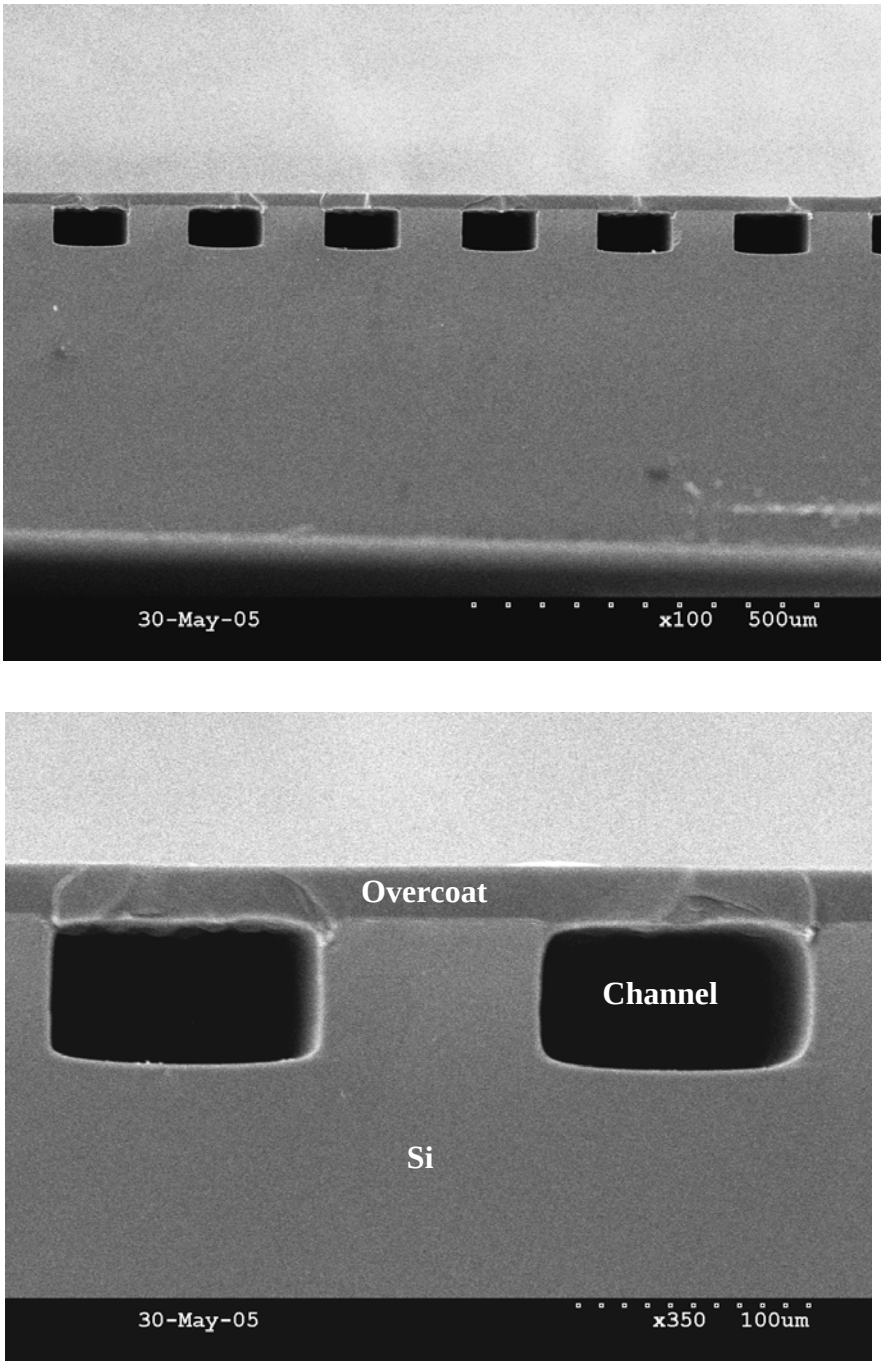


Figure 4.16: Cross-sectional SEM photographs microchannels with a polymer-capped overcoat after 1000 thermal cycles.

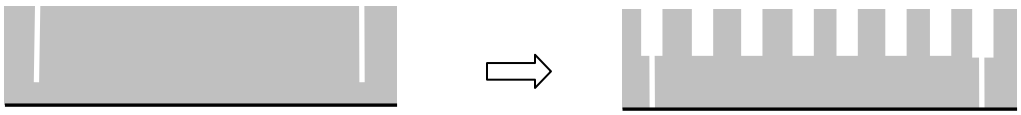
For single-phase liquid cooling, a sufficient flow rate must be maintained and the temperature rises are usually in the range of tens of degrees [4.20, 4.21]. Therefore, these polymer-capped microchannels are promising for use as microfluidic heat sinks in microelectronic systems, although more comprehensive reliability tests are needed. Moreover, as mentioned previously, an advantage of this type of microchannels is that, if needed, additional coatings may be easily applied to enhance their hermeticity and mechanical strength.

4.3. Fabrication of Integrated Thermal-fluidic I/O Interconnects

In addition to the microfluidic channels, a feasible thermal-fluidic interconnection approach is needed to implement an integrated packaging scheme for on-chip microfluidic cooling. In this section, the concept of the thermal-fluidic I/Os is introduced to enable chip-to-board fluidic connection, which includes thermal-fluidic through-vias as well as micro-pipe fluidic inlets/outlets.

4.3.1. Thermal-fluidic Through-vias

A two-step Si etching can be performed to fabricate the necessary through-vias and the heat-exchanging microchannels at the back-side of the Si chips. As shown in Figure 4.17a, in the first masking step, vias are defined through the photoresist and etched partially into the Si wafer. Trenches are then patterned and etched using the second masking step Figure 4.17b.



(a) (b)

Figure 4.17: Schematic illustration of a two-step Si etching process for thermal-fluidic vias and microchannels.

The vias obtained in the first etch step are aligned with the trenches such that the deep vias are further etched simultaneously while the trenches are formed. Si etching is stopped by the SiO_2 passivation film on the front-side of the wafer. In this manner, through-chip vias are produced to achieve fluidic interconnection from the front-side of a chip to its back-side. Nevertheless, the progress of the Si etching must be carefully controlled to ensure the desired depths for both vias and trenches and to avoid a tapered via bottom caused by over-etching. To determine whether or not the vias have been etched through the Si wafer (the overall thickness is ~ 375 μm), the samples must be carefully inspected. A simple method is to use an optical microscope to check the bottom of the vias. If the etching is complete, the color of the bottom surface of via should be from the SiO_2 film, which can be easily distinguished from the bright metallic-like color of the etched Si. A negative photoresist, NR5-8000, was used as the hard-mask for the ICP etching, which shows a etch selectivity larger than 50:1. In this work, ~12 μm thick photoresist (spin condition: 1000 rpm/500rpm/s/50s) was used. During the ICP etching, a RF power of ~18 W was applied and the Si etch rate of the Bosch process is typically 0.6 μm/cycle. However, the etch rate decreases as the vias become deeper. Therefore, based on experiments, the actually etch time was 350 cycles for the first etch step to reach via depth of ~175 μm, and the second etch step takes another 450 cycles to form trench depth of ~200 μm. The photoresist was removed in RR4 remover at 110 °C after the etching was completed. The cleaning must be thorough because residue may be trapped inside the microchannels and vias. In case some polymeric residues are observed, a short descum in a reactive ion etcher (RIE) is necessary and very effective.

Figure 4.18 shows the SEM images of the back-side of the wafer after Si etching. With such a two-step etching method, the depth of the trenches is determined by the time of the second

etching step, as mentioned above. The through-vias are well aligned with the completed trenches, as shown in the side view in Figure 4.19. After the Si vias are etched through, the thin film of SiO_2 at the front-side of a via is visible through the vias.

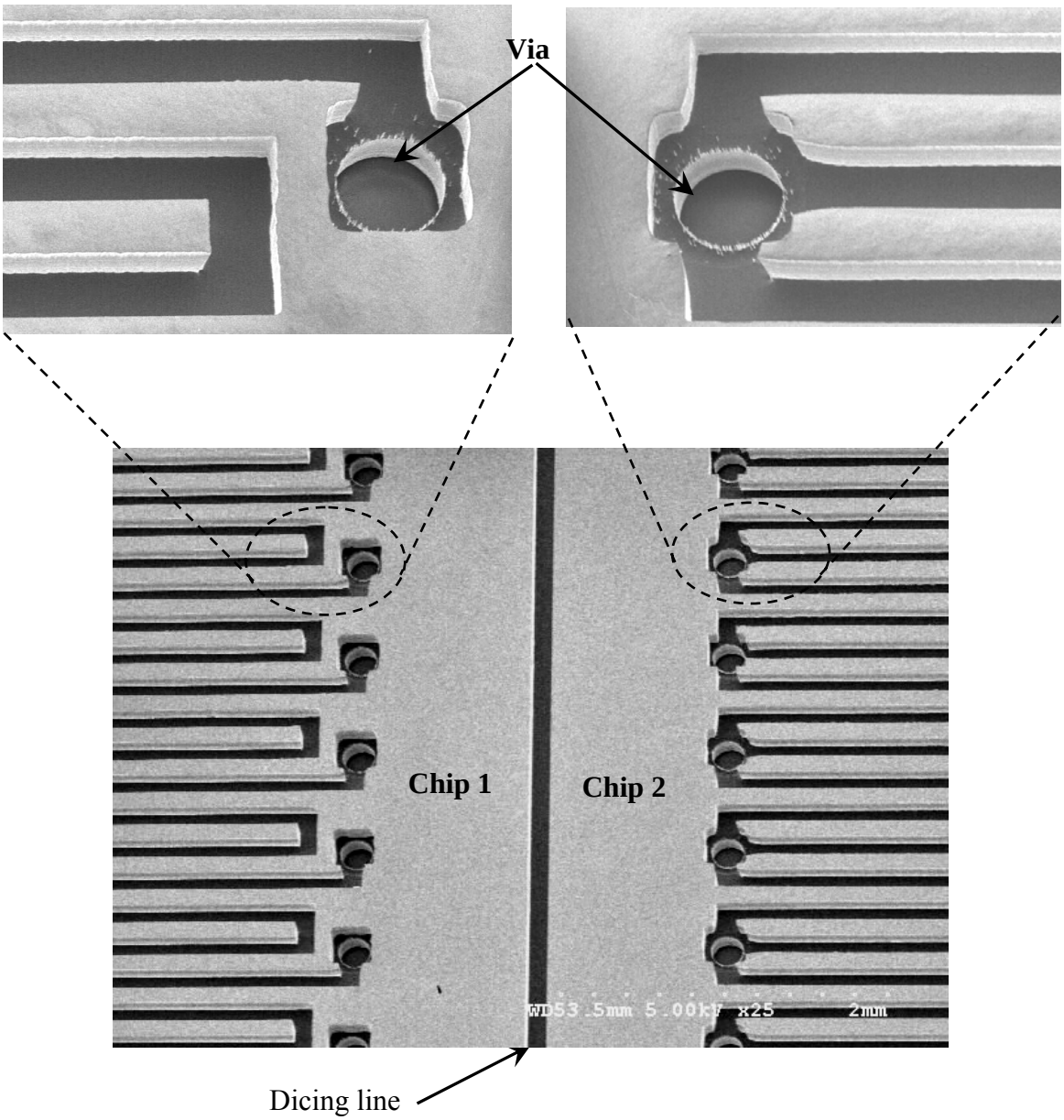


Figure 4.18: SEM photographs of microfluidic channel arrays at the back-side of a wafer. The through-wafer vias (D_{via}=100μm; t_{wafer}=375μm) are located close to the edge of the chips and aligned with the microchannels. Various channel patterns may be used such as the straight lines and the serpentine lines.

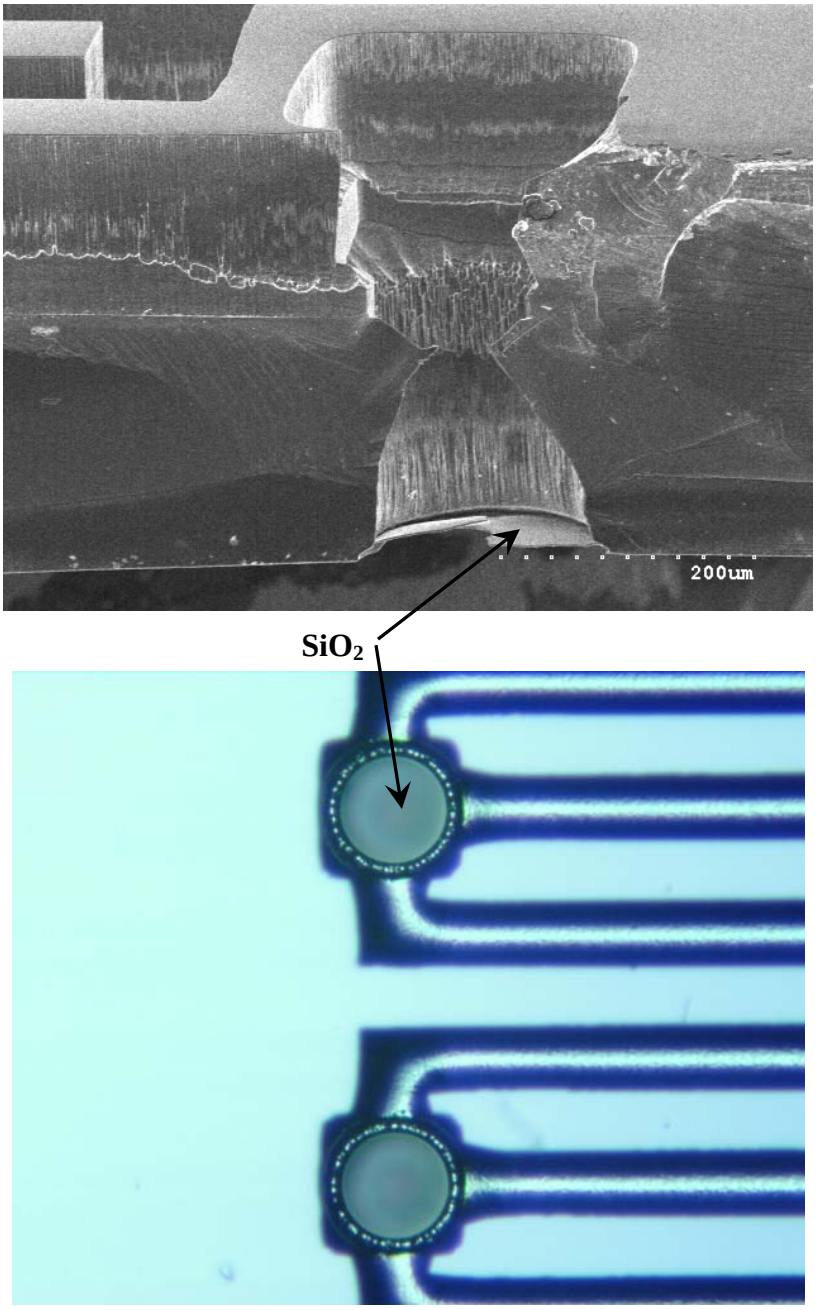


Figure 4.19: SEM and Optical micrographs of the through-vias with SiO_2 film as the etch-stop layer. After Si etching is complete, the color of the SiO_2 can be observed an distinguished during optical inspection.

4.3.2. Trench Filling Issues with the Presence of the Through-vias

If the microchannels are formed with the method of sacrificial polymer, the filling process becomes a challenge due to presence of the deep vias inside these trenches. For instance, although the 200 μm deep trenches can be well filled up with a two-steps spin coating of high-viscosity sacrificial polymer, the through-chip vias can not be completely covered. Voids have been observed inside the through-vias after planarization by mechanical polishing, as revealed in Figure 4.20. This can be resolved by an extra step of spin coating. In addition, the soft bake sequence is also critical to avoid air bubbles trapped inside the through-vias. It was observed that more air bubbles are trapped if the wafer was placed on the hotplate immediately after the spinning. The main reason is that it takes some time for the high-viscosity polymer to flow into the vias. Once the polymer is heated up, it dries quickly before the "via filling process" completes. Therefore, the wafer was intentionally left still for 5~10 mins at room temperature after each spin coating step, which effectively resolves the issue of air bubbles.

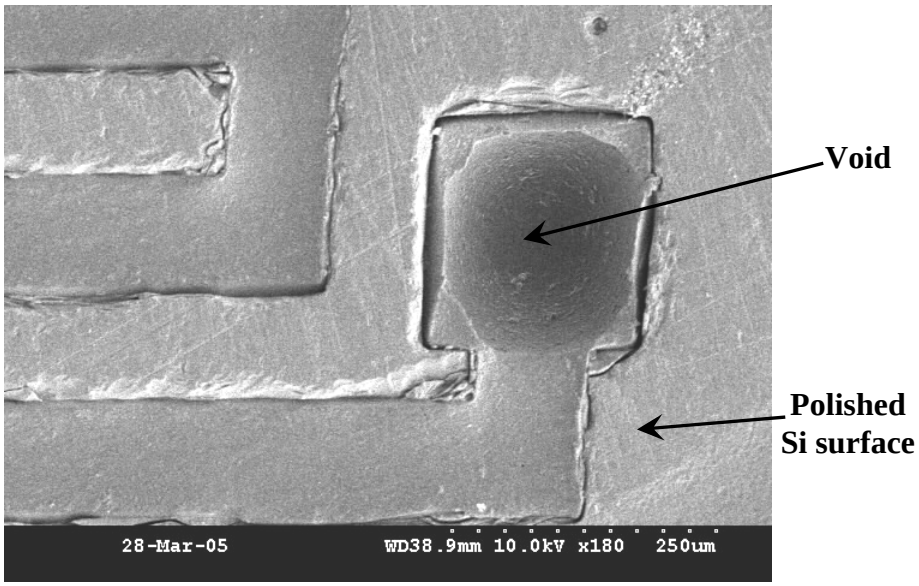


Figure 4.20: SEM image of a poorly filled through-via (filled with two-steps spin coating of high-viscosity sacrificial polymer at 1500 rpm).

Figure 4.21 shows the successfully filled trenches and through-vias after the mechanical polishing. It can be seen that the surface of the sacrificial polymer inside the through-vias becomes flat after the mechanical polishing.

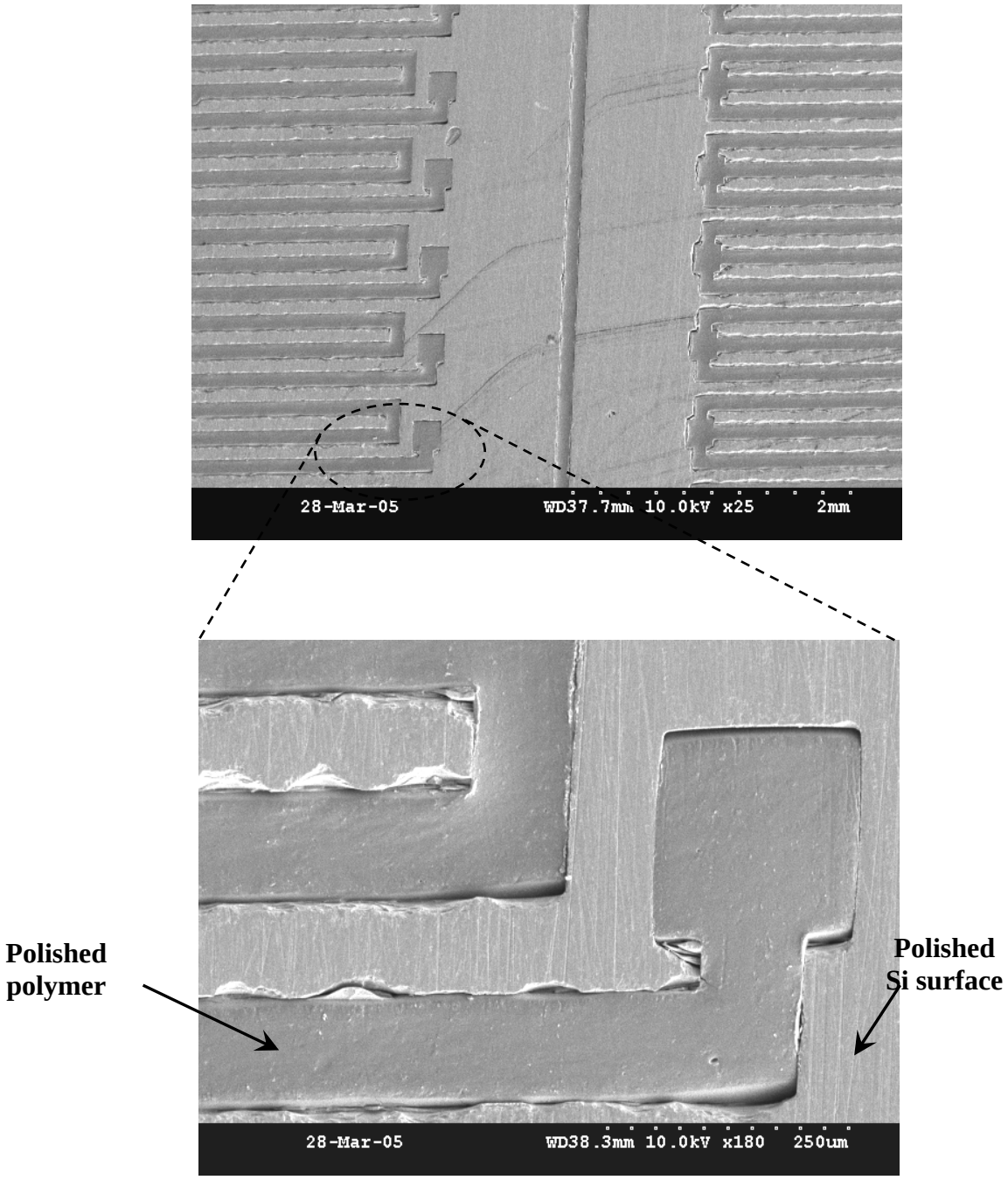


Figure 4.21: SEM photographs of the well-filled deep trenches with through-vias (The surface of sacrificial polymer is planarized after the mechanical polishing.

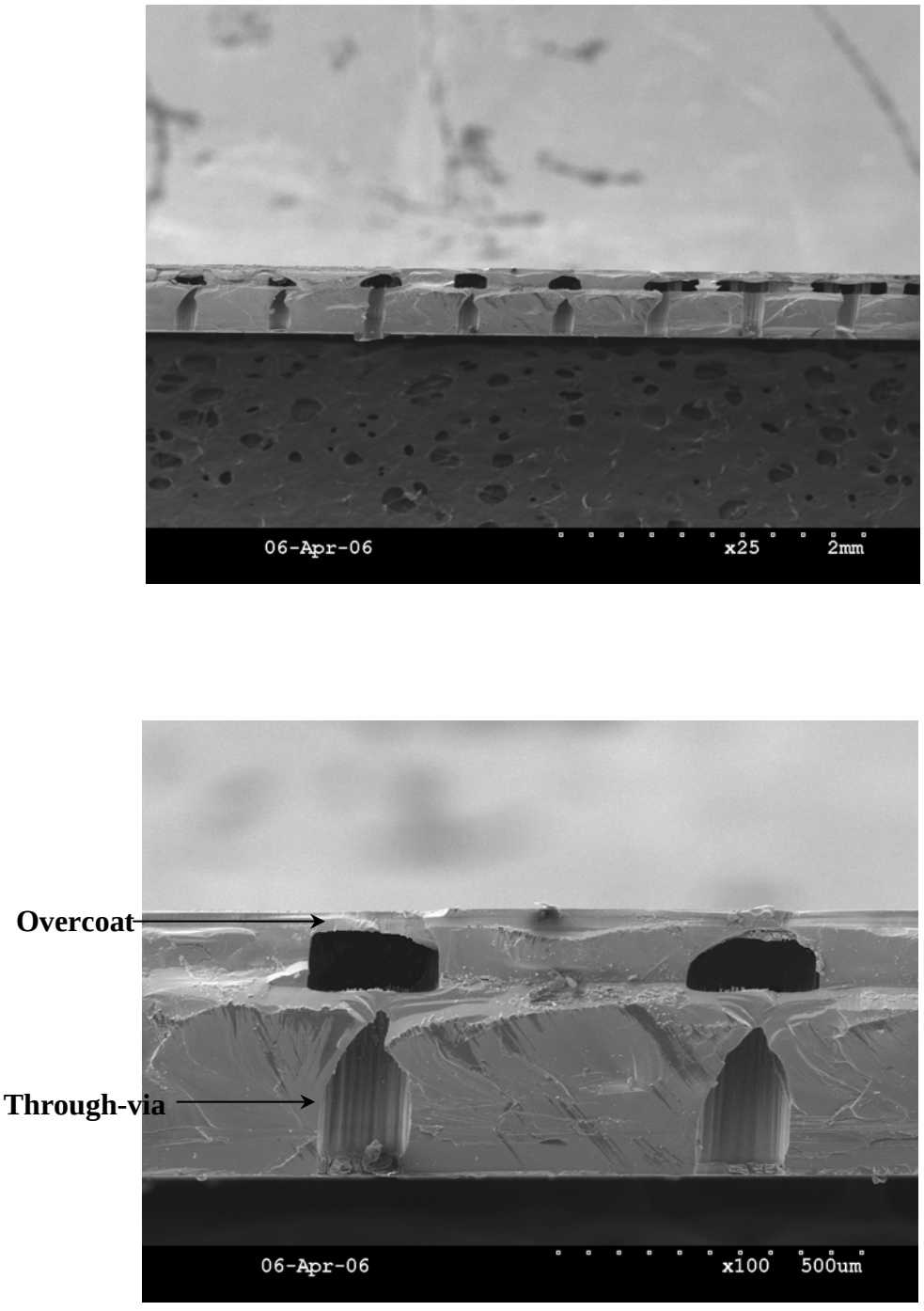


Figure 4.22: Cross-sectional view of the microchannels when the sample is cleaved at the edge to expose the through-vias.

4.3.3. Integrated Electrical/Thermal-fluidic I/O Interconnects

To connect the on-chip microfluidic channels and board-level fluidic networks, micro-pipes are needed as the thermal-fluidic inlets/outlets. They must be compatible with high density electrical interconnects for both fabrication and assembly.

4.3.3.1. Micro-pipe Fluidic Inlets/Outlets

Using photoimageable polymer such as Avatrel 2195P, high-aspect ratio micro-pipes can be easily fabricated as fluidic inlets/outlets, as shown in Figure 4.23. The micro-pipe inlets/outlets can be placed at the chip surface in the form of arrays. Based on this approach, wafer-level thermal-fluidic I/Os become possible and can be used to deliver the working fluid directly into the on-chip microchannels from board-level fluidic systems. The shape of the polymer micro-pipes may be modified through heat treatment above the T_g of the polymer. Since Avatrel 2195P has a T_g of approximately 250 °C (as mentioned previously), the polymer structure deforms if heated up to this temperature.

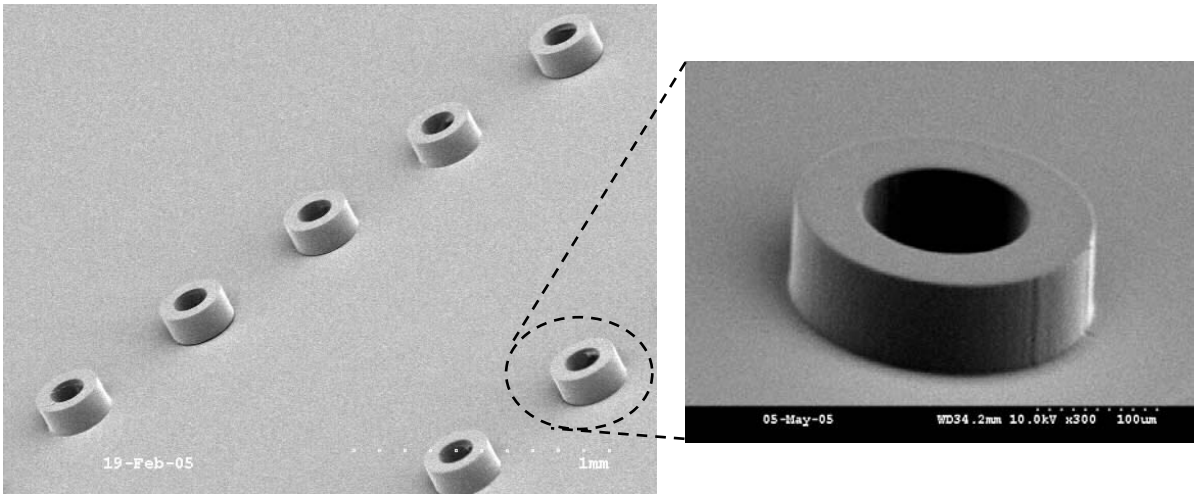
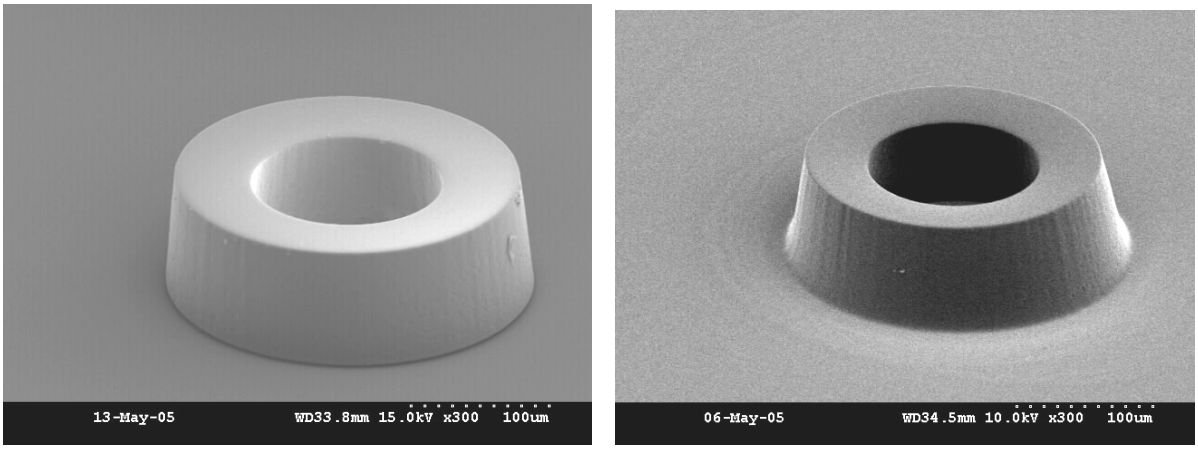


Figure 4.23: SEM photographs of the polymer micro-pipes made of Avatrel 2195P, which were cured at 160 °C.

Figure 4.24 shows the slight deformation of the polymer micro-pipe after heat treatment at 260 °C and 280 °C, respectively. In practice, such a tapered shape may be desirable to assist connection of the micro-pipes with orifices on the board. Furthermore, the polymer micro-pipes can be metallized to improve the mechanical strength.



(a) **(b)**

Figure 4.24: SEM photographs of the tapered polymer micro-pipes that were treated above the T_g of the polymer. (a) treated for 1 hour at 260 °C (b) treated for 1 hour at 280 °C.

4.3.3.2. Integrated Electrical/Thermal-fluidic I/O Interconnects

To be incorporated in high performance IC packages, the micro-pipe thermal-fluidic I/Os must be integrated with area-array electrical interconnects. A key to the process compatibility with conventional C4 solder bumps is the processing temperature. While the melting temperature and reflow temperature of the conventional eutectic SnPb are ~ 183 °C and ~ 220 °C respectively, Avatrel 2195P, can be cured at a relatively low temperature (~160 °C). Thus, the fabrication processes of the two distinct types of I/O interconnects can be compatible if the processing sequences are carefully designed. Figure 4.25 shows SEM images of a row of micro-pipes fabricated along with an area array of C4 solder bumps at the wafer level.

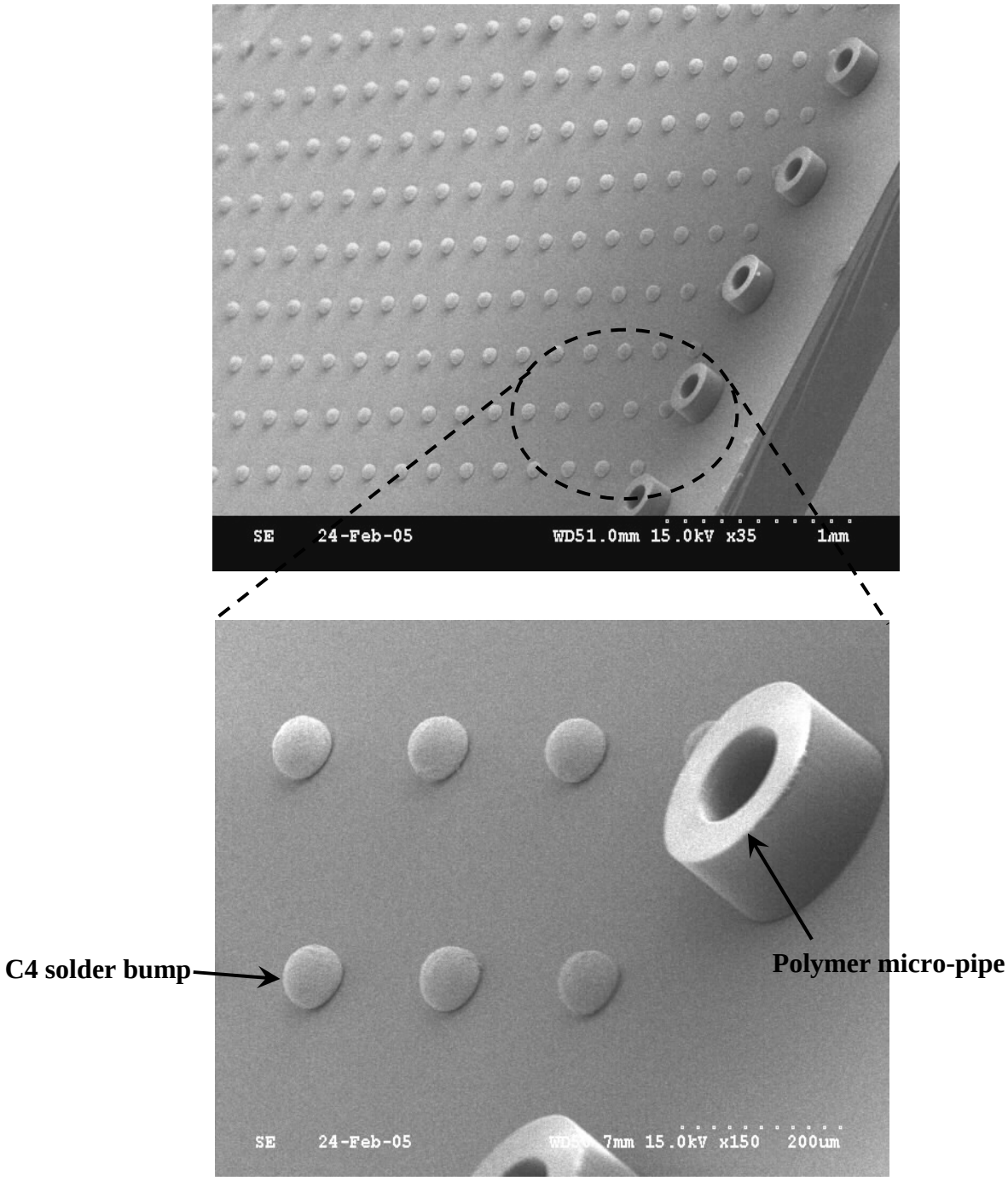


Figure 4.25: SEM photographs of a row of micro-polymer pipes as the fluidic interconnects and the area-array solder bumps for as high density electrical interconnects.

The C4 solder bumps were first deposited through electroplating and then reflowed at 200 °C. After cleaning, the polymer micro-pipes were formed through a simple photopatterning with a thick film of Avatrel 2195P. The inner diameter and the outer diameter of a polymer pipe are 100μm and 250μm, respectively, and its height is approximately 100μm. The solder bumps are 65μm in height and 80μm in diameter approximately. The micro-pipes are intentionally designed to be taller than the solder bumps because they will be partially inserted into orifices (vias), while the solder bumps will be in contact with Cu pads on the top of a board during the assembly.

4.4. Wafer-level Integration of the Microchannel Heat Sink

Using the monolithic microchannels and the thermal-fluidic I/Os described above, a fabrication process is proposed for the on-chip microfluidic heat sink at wafer-level, as shown in Figure 4.26. The process begins following the completion of semiconductor BEOL process (Figure 4.26a). The above described two-step Si etching process is used to fabricate the necessary through-vias and the heat-exchanging microchannels at the back-side of the Si chips. As shown in Figure 4.26b, in the first masking step, vias are defined through the photoresist and etched partially into the Si wafer. Trenches are then patterned and etched using the second masking step (Figure 4.26c). As mentioned above, the color of the SiO_2 film can be easily distinguished from that of the bottom of the etched Si vias and can be used as an indicator of completion of through-via etching. The trenches are then filled with a sacrificial polymer by spin-coating, as shown in Figure 4.26d. The extra polymer built above the surface is removed by the mechanical polishing (Figure 4.26e). The layered overcoat (~1μm porous SiO_2 and ~30μm structural polymer) is then deposited above the trenches (Figure 4.26f). The porous SiO_2 was deposited in PECVD at 110 °C.

Next, the wafer is flipped and the processing at the front-side continues. A polymer passivation layer is first coated and patterned to open the vias for both fluidic paths and electrical paths (Figure 4.26g). Using the approach described above, the sacrificial polymer is decomposed in a nitrogen-purged furnace at low temperatures (≤200ºC), by which the overcoat polymer is cured simultaneously and becomes watertight (Figure 4.26h). After that, the front-side of the wafer is ready for conventional solder bumping process to fabricate the chip-to-package electrical interconnection. For this step, NR9-8000 photoresist with a thickness of ~34 μm (spin speed: 750 rpm) is used as the mold for electroplating. Controlled volume of solder is then electroplated through the photoresist (Figure 4.26i). After reflow with the aid of a liquid flux, spherical solder bumps are formed. So far, Sn60Pb40 solder has been used due to easy availability and its excellent wettability, which usually requires a peak reflow temperature of 220ºC. If necessary, other solders including the widely pursued Pb-free solders such as SnCu, SnAg or SnAgCu may also be usedd using the similar electroplating processes in response to the global transition to Pb-free electronics manufacturing.

Finally, arrays of micro-pipes are fabricated using a thick layer of Avatrel 2195P as the fluidic I/O interconnects between a chip and package-level fluidic networks (Figure 4.26j). The micro-pipes must be designed to be aligned with the through-chip fluidic vias in order to connect with the micrchannels at the back-side. The passivation layer inside the pipes can be easily opened by wet etching (Buffered Oxide Etchant or namely BOE 6:1) to allow fluidic circulation. Since residual BOE may be left inside the channels, the wafer should be soaked in the DI water for at least 10 mins and thoroughly rinsed. A nitrogen purged oven is used to dry the wafer. After that, the wafer is ready for dicing.

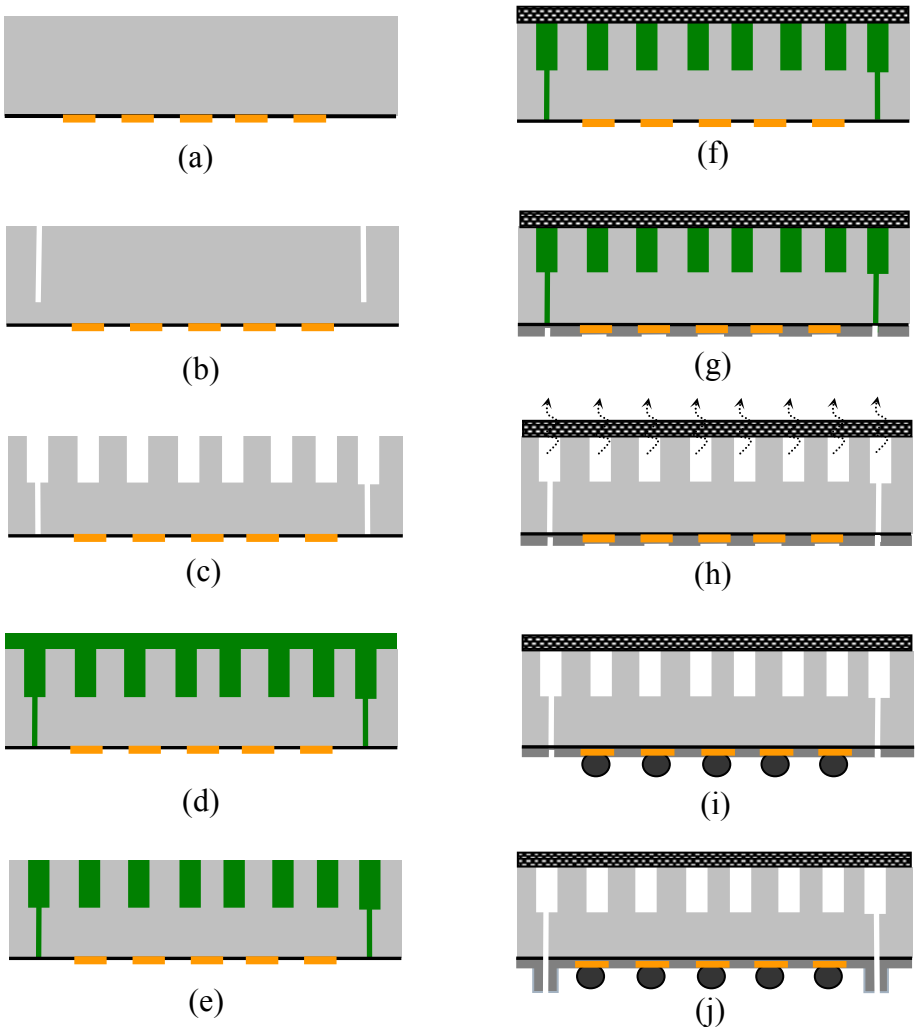


Figure 4.26: Schematic of the fabrication processes for the microfluidic channels with through-chip vias: (a) The process begins after the competition of BEOL process, (b) through-vias are patterned and partially etched, (c) trenches are patterned and etched, by which the through-via etching is completed simultaneously, (d) trenches and vias are filled with a high-viscosity sacrificial polymer, (e) the polymer "pile-up" is removed by mechanical polishing, (f) the layered overcoat is deposited and partially cured, (g) a polymer passivation is deposited and pattern at the front-side, (h) heat treatment is performed to decompose the sacrificial polymer and cure the overcoat polymer, (i) solder bumps are deposited at the front-side by bumping processing, (j) polymer pipes are fabricated by a thick photoimageable dielectric polymer.

4.5. Chip-to-board Thermal-fluidic I/O Interconnection

To distribute the working fluid into on-chip fluidic system, fluidic I/O interconnection must be achieved during assembly. For compact microelectronic systems with board-level fluidic delivery, suitable thermal-fluidic I/O configurations must be investigated. This section will first introduce the assembly method for the "microfluidic flip chips" with primary focus on the compatibility with conventional flip-chip bonding and chip encapsulation [4.2]. Integrated fluidic I/O interconnection schemes will then be discussed.

4.5.1. Assembly of "Microfluidic Flip Chips"

The basic concept of the thermal-fluidic I/O assembly is illustrated in Figure 4.27. With a precision flip-chip bonder, a compression force is applied after the chip and the package substrate are aligned. Since the polymer pipes are usually taller than the solder bumps, a portion of the polymer pipes will be inserted into the orifices, when the solder balls come into contact with the metal pad on the substrate. Once reflowed, metallurgical joining will be formed by the solder bumps and a chip is then mechanically bonded with the board substrate. The micro-pipes are designed to have the same diameter as that of the orifices. However, since Avatrel 2195P is a negative tone photo-polymer, the diameter of the micro-pipes is usually slightly larger than that of the orifices. Therefore, the micro-pipes are actually "squeezed" into the orifices during bonding, which is beneficial to the fluidic connection.

To ensure hermetic sealing of the micro-pipes, a void-free polymer should be applied at the chip-edge after assembly, which is the same as the conventional underfilling process. In this work, a liquid epoxy mixed with ultra fine ceramic powder (Fast cure Acrylic kit, Buehler, Ltd) was used. After curing of the underfill (~1 hour at 60 °C), the polymer pipes are joined with the orifices and the hermetic fluidic path between the chip and the board is formed.

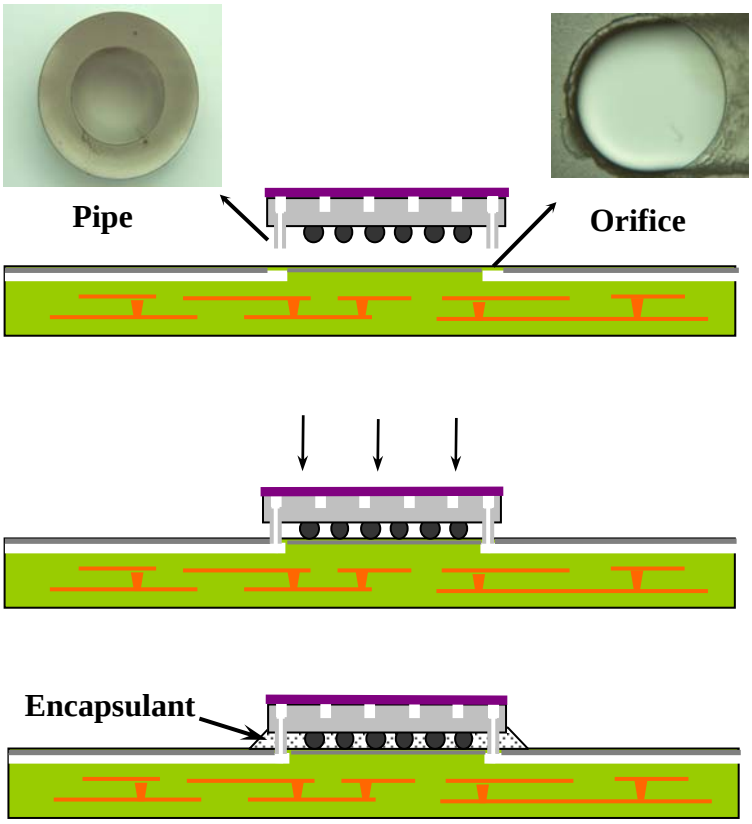


Figure 4.27: Schematic of the assembly process of a "microfluidic flip chip" (a) alignment (b) bonding through compression and heating (c) encapsulation with underfill

Figure 4.28 shows the photograph of the precision flip-chip bonder with an alignment accuracy of this bonder is around ~ 2 μm. With the thermal-compression capability, chips can be bonded with controlled temperature-force profiles using the bonder. To illustrate the feasibility of the fluidic I/O assembly, bonding experiments were first performed with a "microfluidic flip chip." During the bonding, both chip and the substrate were heated to 150 °C after the alignment. A compression force (200 g) was then applied to bring them into contact. While the temperature was increased to the reflow temperature (220 °C), the compression force was maintained at a constant value.

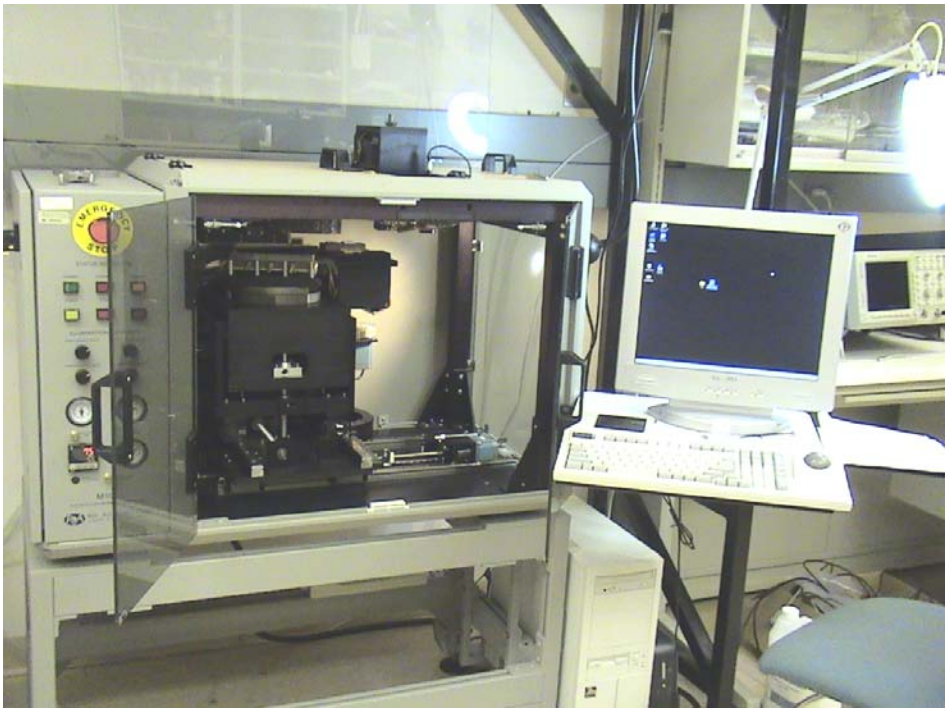


Figure 4.28: Photograph of the precision flip-chip bonder (R&D Automation, Model M-10)

Figure 4.29 shows several "microfluidic flip chips" bonded onto a glass substrate. For the purpose of simplicity, the microchannels on the chip were enclosed by glue bonding of a Si cover plate. The manifold channels on the substrate were fabricated simply using a photoimageable sacrificial polymer. Avatrel 2195 was used as the overcoat and vias were patterned through the overcoat to serve as the orifices. Fluidic continuity has been successfully demonstrated as described below. A plastic tube was connected with a manifold branch on the substrate and DI water was driven by a syringe pump and flowed through 3 board-level channels, passed through the micro-pipes as well as the corresponding 9 on-chip microchannels (3×3=9), and returns to the board-level channels. The liquid droplet can be clearly seen at the end of the board-level channels in a magnified view.

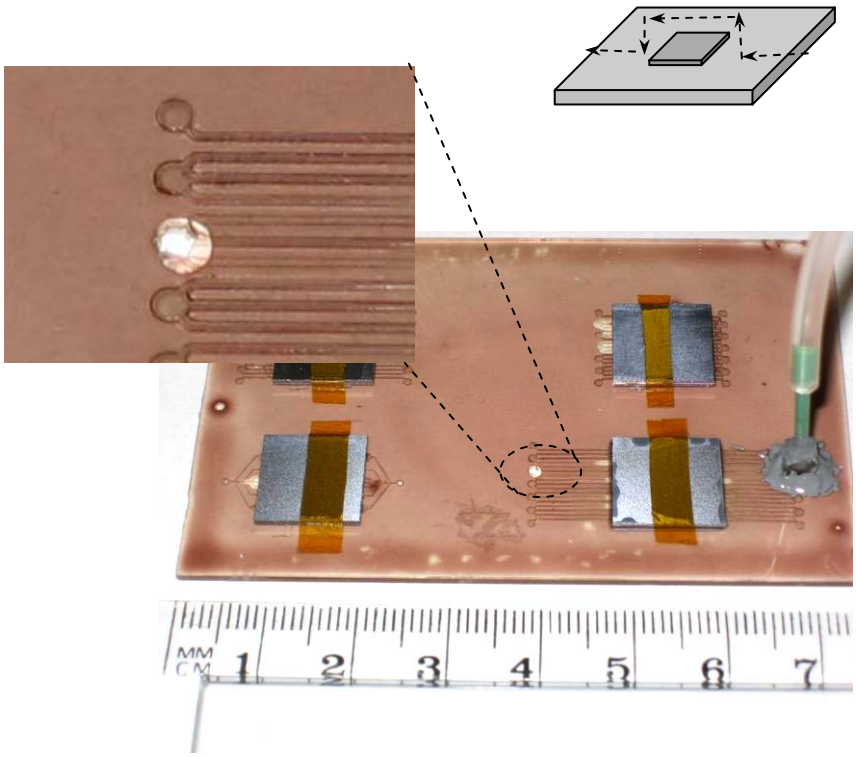
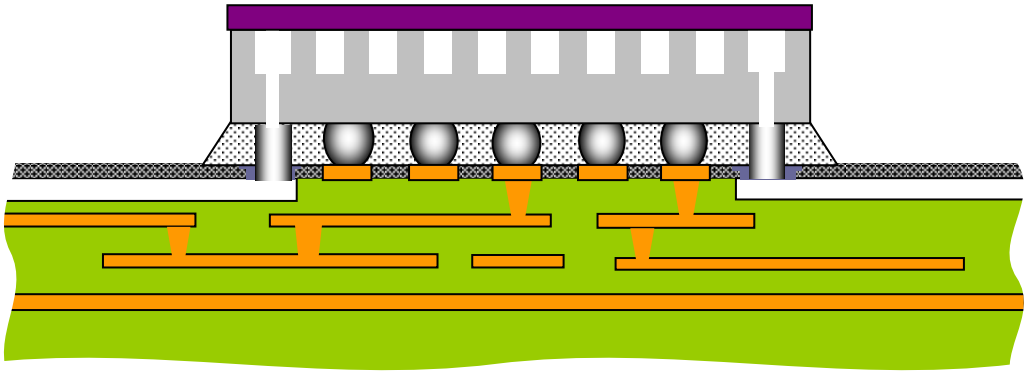


Figure 4.29: Optical micrographs of "microfluidic flip-chips" bonded onto a glass substrate with embedded channels to distribute the working fluid. The chip has 51 parallel microchannels (h ~ 100μm) at its back-side and enclosed with a glass cover plated using the glue bonding approach. The flow direction is illustrated by the arrows.

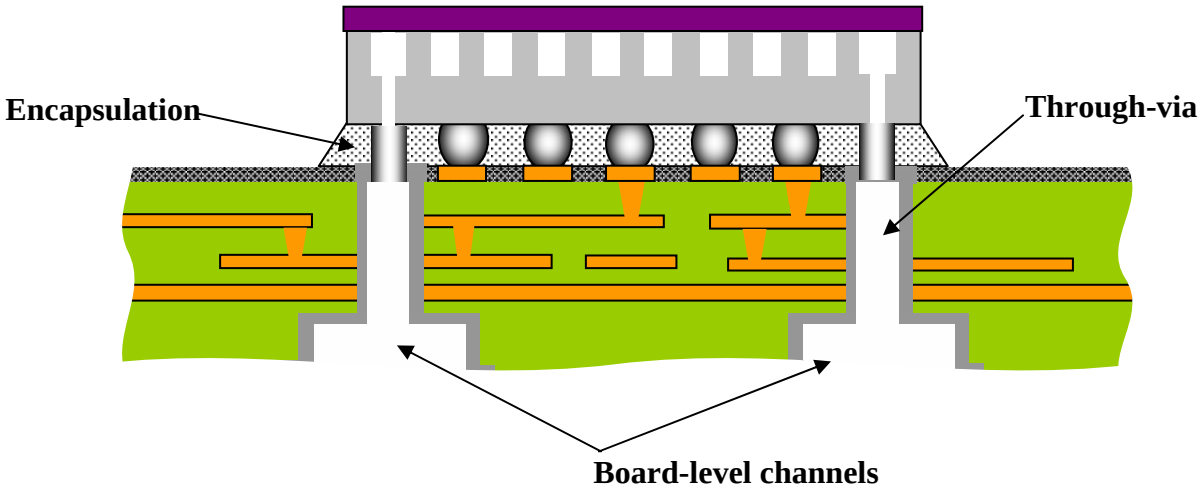
4.5.2. Integrated Thermal-fluidic I/O Configurations

Upon success of the above experiments, two integrated thermal-fluidic I/O configurations were proposed to enable the on-chip microchannel heat sink, as illustrated in Figure 4.30. In I/O configuration (a), the manifold channels must be embedded at the front-side of the board substrate and orifices must be opened through the overcoat. Although a photoimageable version of the sacrificial polymer, Unity 200P, can be used to pattern the board-level channels directly, the height of the channels is directly determined by the thickness of the sacrificial polymer that can be processed. Another challenge for this scheme is that the available area at the front-side of

the mounting substrate is limited. To solve these problems, I/O configuration (b) is proposed, in which the manifold channels are embedded inside the multi-layer board or fabricated at the opposite side of the board and through-holes are utilized for fluidic distribution.



(a)



(b)

Figure 4.30: Schematic of two integrated thermal-fluidic I/O configurations to enable the on-chip microchannel heat sinks: (a) manifold channels are located at the front-side of the board, (b) manifold channels are located at the back-side of the board and large through-holes are used to connect with the micro-pipes.

Fortunately, the through-holes are commonly available in printed circuit boards (PCBs) and the channels can be fabricated with a variety of methods. For instance, the channels can be simply embedded or enclosed through the multi-layer lamination process in the standard PCB fabrication [4.22, 4.23].

In this work, test substrates were mainly fabricated for the integrated I/O configuration (b) for the purpose of simplicity. Figure 4.31 shows the photographs of the front-side of the test substrate, where peripheral arrays of vias are fabricated through the Si substrate and aligned with the electrical paths. The Cu lines with a thickness of ~ 8 μm were first patterned and electroplated. After the seed layer was etched, a polymer passivation layer was applied to serve as the solder mask for the Cu pads. Since the over-coating polymer (Avatrel 2195P) is photoimageable, vias were easily opened for both fluidic and electrical paths to accommodate the micro-pipe inlets/outlets and solder bumps on the test chips respectively.

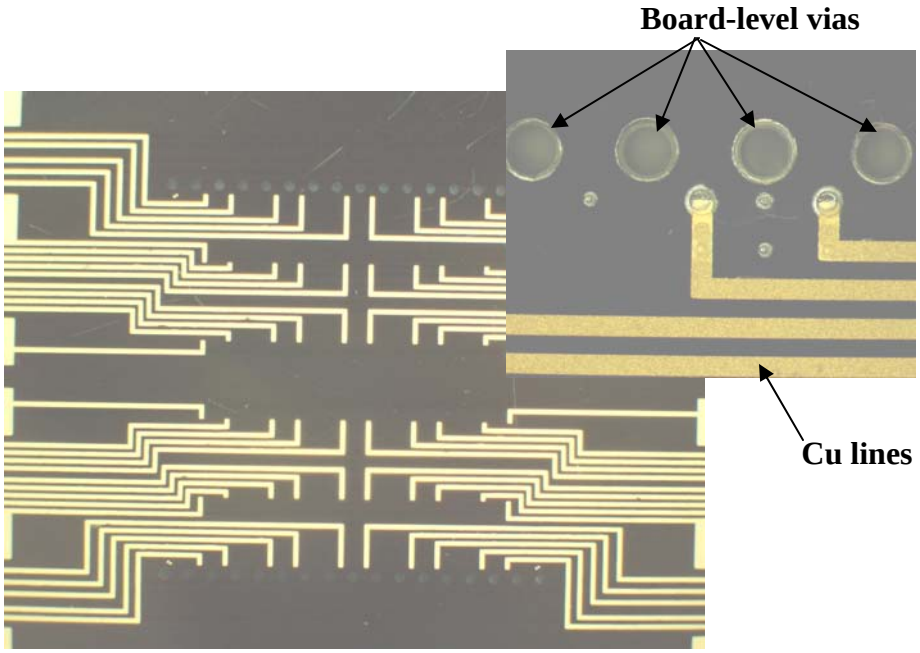


Figure 4.31: Optical photographs of the test board substrates with metal lines at the front-side and through-vias for the thermal-fluidic I/O configuration (b) in Figure 4.30.

As illustrated in Figure 4.32, a test chip with microchannels enclosed by glue bonding of a transparent cover plate (Pyrex glass) was bonded on a Si substrate equipped with fluidic vias (D_{via} =250 μm). The sample was then mounted onto a carrier wafer using an epoxy as the glue. Thin wafer pieces (375 μm thick) were placed and glued between the test substrate and the mounting wafer, which forms cavities with a height of more than 375 μm as the fluidic paths to connect with through-vias on the test substrate. Both fluidic continuity and electrical continuity were tested successfully. Since the cover plate is *transparent,* visual inspection can be easily performed when DI water is passed through the microchannels. Flowing liquid droplets have been observed in all the microchannels and recorded by a digital video recorder, which indicates a high yield of fluidic interconnection.

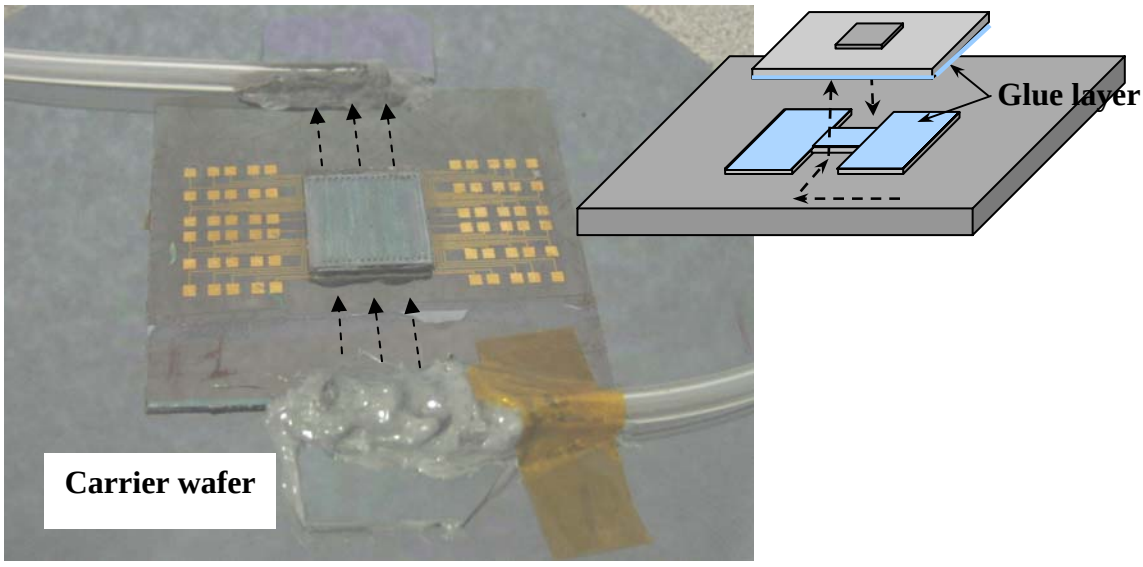


Figure 4.32 Photograph of a test chip bonded onto a test substrate that is mounted onto a carrier wafer. Thin wafer pieces (375 μm thick) were placed and glued between the substrate and the mounting wafer to form the fluidic paths connecting with the through-vias. The flow direction is illustrated by the arrows.

4.5.3. Fabrication of Channel Networks on Low-cost Organic Board Substrates

Bauer et al. [4.22] and Ilgen [4.23] have demonstrated that thermal-fluidic channel networks can be implemented inside LTCC substrates and FR-4 laminates, respectively. Both approaches used lamination processes. In this work, fabrication of fluidic channels using low-cost FR-4 laminates was also demonstrated because the decomposition temperature of the photoimageable version of the sacrificial polymer, Unity 200P, can be as low as 170 ˚C. Figure 4.33 shows the patterned manifold channels with Unity 200P, and Figure 4.34 shows the cross-sectional view of the channels obtained after over-coating with Avatrel 2195P and decomposition at 180 ˚C. Furthermore, as shown in Figure 4.35, a row of tiny orifices can be easily defined at the end of the manifold channels through the Avatrel 2195P over-coat layer, which will accommodate polymer micro-pipe I/Os at a chip.

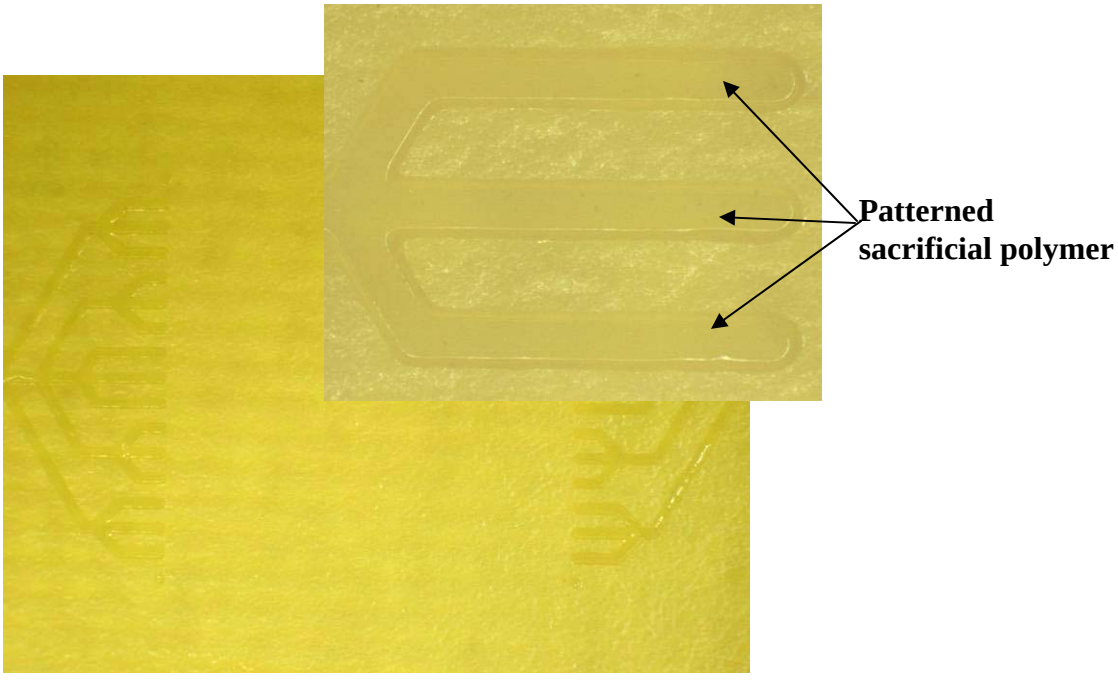


Figure 4.33: Optical micrographs of channels directly patterned with a photoimageable sacrificial polymer (Unity 200P)

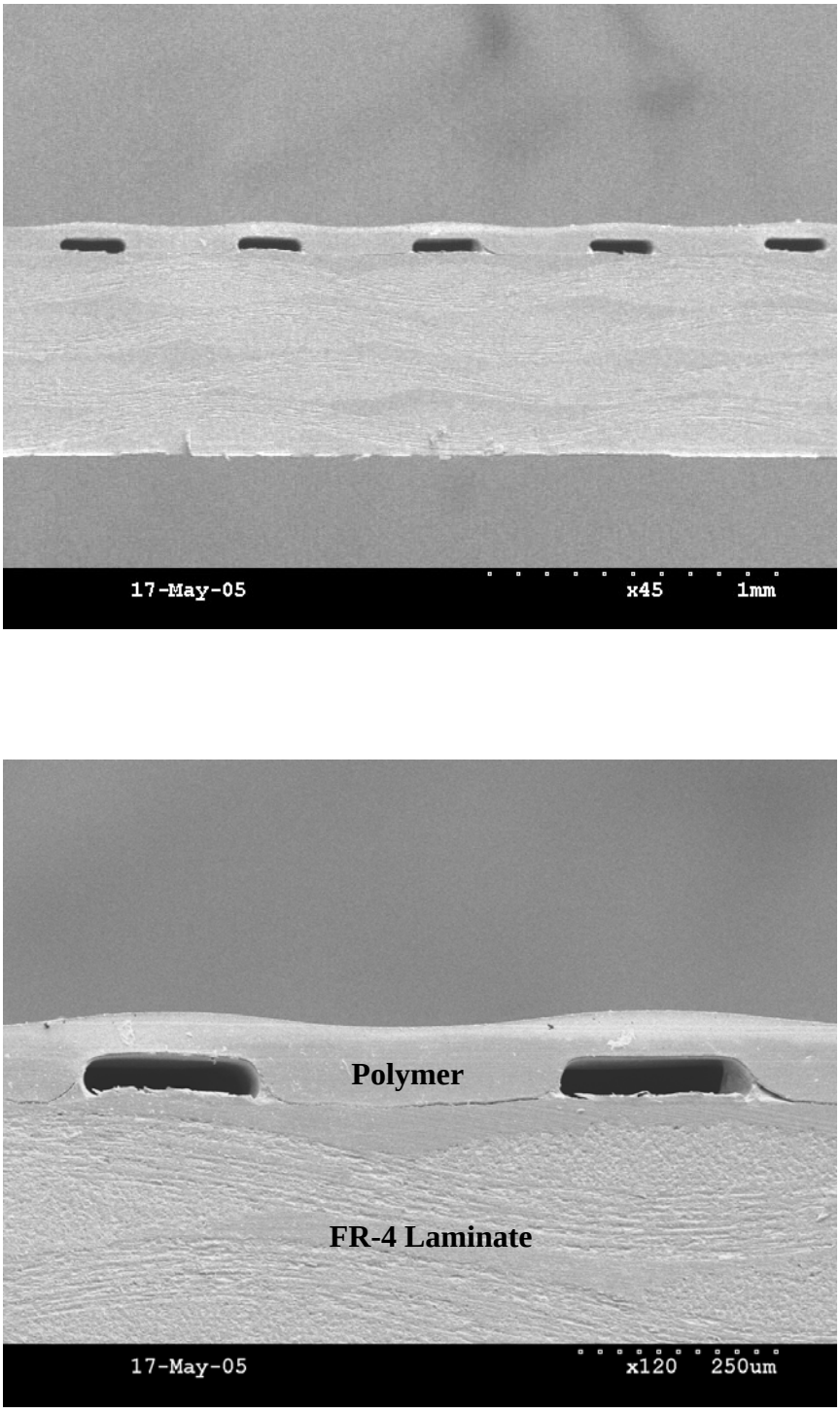


Figure 4.34: Cross-sectional SEM photographs of fluidic channels encapsulated by an overcoat polymer based on FR-4 laminate.

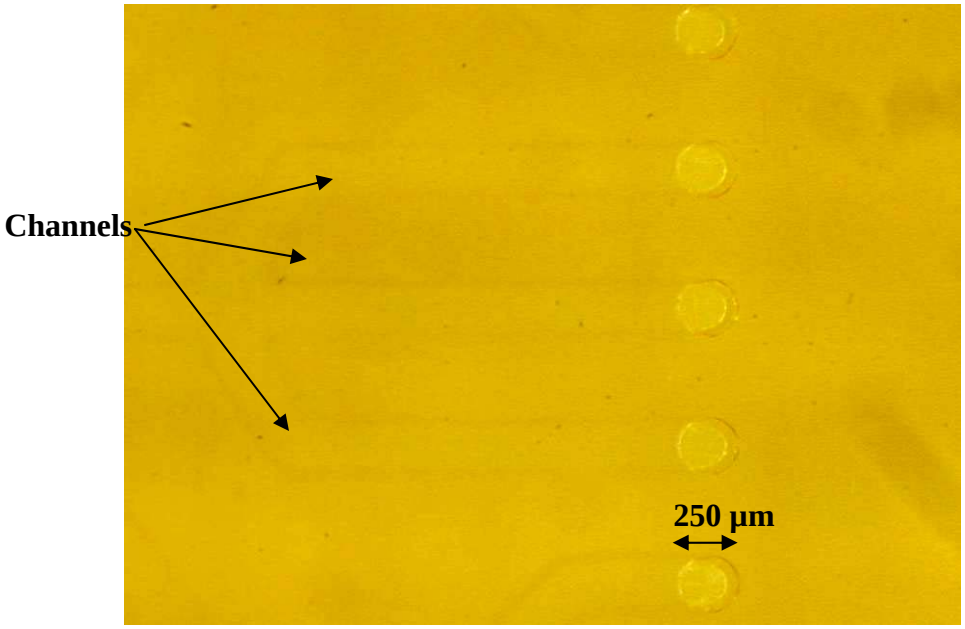


Figure 4.35: Optical micrographs of a row of tiny orifices defined through the Avatrel 2195P over-coat layer. The orifices are aligned with fluidic channels.

4.6. Summary

This chapter primarily described low-temperature CMOS compatible processes for on-chip microchannels as well as assembly with the thermal-fluidic I/O interconnects. Two processes were described for the fabrication of microchannels with use of glue-bonding or a thermally-decomposable sacrificial polymer.

The glue bonding approach is relatively simple but requires an additional cover-plate. The polymer-capped monolithic microchannels can result in a thin package profile and can potentially enable a highly integrated microfluidic systems. Through-Si vias and polymer micro-pipes were then introduced as the thermal-fluidic I/O interconnects.

For the approach with the sacrificial polymer, trench filling is the key challenge for the implementation of deep channels, particularly for the trenches with the presence of the through-

Si vias. Since the content of solvent in the sacrificial polymer is inversely proportional with its viscosity, the low-viscosity polymer has a poorer coverage after the soft bake. Thus, experiments were performed to resolve this issue using a high-viscosity type sacrificial polymer, thus enabling the use of deep Si trenches, which are desirable for better heat transfer. The monolithic microchannels were tested with continuous water flow under high pressure (up to 2.5 atms). No cracking, leakage or delamination was observed during the testing. Thermal-cycling tests also indicated excellent structural integrity at the interface between the layered overcoat and the Si substrate. In summary, by means of the low-temperature CMOS compatible processes, an on-chip microchannel heat sink has been fabricated at the backside of a test wafer as part of wafer-level packaging. Such a chip-scale cooling scheme can completely eliminate the thermal interface related issues.

In addition, fabrication of the fluidic channels using various package substrates was demonstrated to enable board-assisted coolant delivery. Since the Avatrel 2195P is photoimageable, orifices were fabricated through the overcoat simply by photodefination. Assembly experiments verified the feasibility of the chip-to-board fluidic I/O interconnection. An underfilling process was performed to enhance the hermetic sealing of the polymer micro-pipes, which is compatible with the conventional flip-chip assembly. Finally, for the first time to the author's best knowledge, thermal-fluidic interconnection was successfully demonstrated between the board-level fluidic channels and on-chip microchannels along with simultaneous area array electrical interconnection.

Chapter 5. Thermal-fluidic Characterization of an Integrated Microchannel Heat Sink for GSI

5.1. Introduction

The previous chapter discussed the major issues in fabrication, interconnection and assembly of a chip with integrated microchannel heat sink and thermal-fluidic I/O interconnects. Compared to conventional forced-air heat sinks, such an integrated heat sink presents a dramatic change in chip I/O interconnection and packaging. While chip-scale microfluidic cooling promises significant performance improvement (thermal resistance as low as 0.09 *°C/W*) [5.1], many challenges exist in terms of hydraulic and reliability requirements. This motivates the investigation of the cooling benefits and hydraulic challenges (pressure drop, pumping power etc.,) for the prototype on-chip microchannel heat sink through numerical analysis. The ITRS projected power dissipation requirements and "hot-spot" cooling will be also discussed. Finally, integration of thin-film heaters/thermometers will be described and the chip-scale cooling operation will be demonstrated through thermal-fluidic measurement.

5.2. Thermal Resistance Analysis for an On-chip Microchannel Heat Sink

The principles of on-chip microchannel heat sink was first studied by Tuckerman and Pease in 1981 [5.1]. More advanced closed form models were also developed and can be found in [5.2]. It is generally accepted that the thermal resistance of a microchannel heat sink usually includes three physical contributions [5.1-5.3]:

$$R_{th} = R_{cond} + R_{conv} + R_{heat} \tag{5.1}$$

The first term, R_{cond}, is determined by the thermal conductivity, k_{Si} (W/m-°C), the distance between the bottom surface of a channel and the integrated circuits at the front side, t (m), and the chip area, A_{chip} (m^2):

$$R_{cond} = \frac{t}{k_{Si} A_{chip}} \tag{5.2}$$

Since the microchannels are embedded deep inside the Si chip, t is very small, as illustrated in Figure 5.1. Combined with the large thermal conductivity of Si (k_{Si} ~ 150 W/m-°C), R_{cond} can be easily reduced below **0.007** $^oC/W$ assuming t ~ 100 μm.

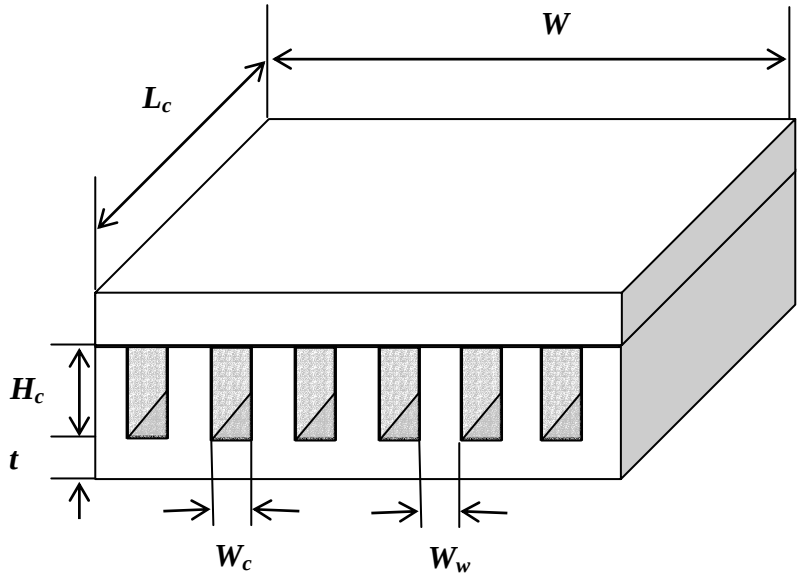


Figure 5.1: Schematic illustration of an on-chip microchannel heat sink

The second term, R_{conv}, depends on the convective heat transfer coefficient h (W/ºC-m^2) and the overall area of "cooling" surfaces of the channels, $A_{channels}$ (m^2).

$$R_{conv} = \frac{1}{hA_{channels}} \tag{5.3}$$

where the surface area of the channels is determined by the channel width, W_c (m), the channel length, L_c (m), channel height, H_c (m), and the number of channels, n_c according to:

$$A_{channels} = n_c \cdot L_c \cdot (2H_c + W_c) \tag{5.4}$$

With DI water at a laminar flow [5.1-5.4], the convective heat transfer coefficient h can be estimated from Equation (5.1).

$$h = \frac{k_f Nu_{fd}}{D_h} \tag{5.5}$$

where k_f (W/ºC-m) is the fluid thermal conductivity and D_h (m) is the hydraulic diameter (or namely characteristic width, [5.1]) of a channel, as mentioned in the Chapter 4:

$$D_h = \frac{2W_c H_c}{H_c + W_c} \tag{5.6}$$

Nu_{fd} is the Nusselt number of the fluid, which represents a *dimensionless* heat transfer coefficient. With water as the working fluid and for a fully developed temperature profile, the Nusselt number can be calculated as [5.2]:

$$Nu_{fd} = 8.235\left(1 - 1.883\alpha + 3.767\alpha^2 - 5.814\alpha^3 + 5.361\alpha^4 - 2\alpha^5\right) \tag{5.7}$$

where α is the ratio of channel width to the channel height (W_c/H_c). Based on the above equations, an ultra high heat transfer coefficient in the order of 10^5 *W*/ºC-m^2 can be easily obtained, which is more than *1000*x higher than that of conventional forced-air cooling mechanisms [5.1]. Combined with the relatively large overall surface area available for heat exchanging, R_{conv} can be further reduced below **0.065** ºC/W through optimization of the channel geometries [5.1, 5.2].

The third component, R_{heat}, equals to the ratio of the temperature rise between inlets and outlets, $\Delta T_{inlet/outlet}$(°C), to the heat flux (or power) Q (W). The temperature rise, $\Delta T_{inlet/outlet}$, is determined by the caloric heating of the working fluid according to:

$$\Delta T_{inlet/outlet} = \frac{Q}{\dot{V} \cdot \rho \cdot C_p} \tag{5.8}$$

where $\dot{V}$ (ml/min) is the liquid flow rate, ρ (g/ml) is the density and C_p (J/°C-g) is the specific heat capacity of the working fluid. As a result, R_{heat}, is inversely proportional to the liquid flow rate $\dot{V}$ for a given fluid:

$$R_{heat} = \frac{\Delta T_{inlet/outle}}{Q} = \frac{1}{\dot{V} \cdot \rho \cdot C_p} \tag{5.9}$$

The above analysis reveals that the first and second terms are determined once the relevant materials and the structural geometries are chosen. The third term, R_{heat}, is the only term related to the flow rate. Since the first term, R_{cond}, is relatively small, the overall thermal resistance, R_{th}, is usually dominated by the second term, R_{conv}, and the third term, R_{heat}, depending on the channel dimensions and flow rate. Table 5.1 summarizes the achievable thermal resistance for chip-level microchannel heat sinks reported in literature [5.1, 5.3, 5.5 – 5.7]. It can be seen that the overall thermal resistance of an on-chip microchannel heat sink can be as low as **0.09 ºC/W** (for a unit area of 1 cm^2) with optimized channel geometries and sufficient flow rate.

Table 5.1 Summary of achievable thermal resistance of single-phase on-chip microchannel heat sinks reported in literature [5.1, 5.3, 5.5 – 5.7]

Source	R_{th}(ºC-cm^2/W)	W_{ch} (μm)	H_{ch} (μm)	Heat flux tested (W/cm^2)	Flow rate (ml/min)
Tuckerman, et al., (1981)	0.09	50	302	790	~ 516
Lee, et al., (2002)	0.1	53	215	108.6	~ 496
Wei, (2004)	0.1	54 ~ 61	243~284	70	~350
IBM, (2005)	0.105	75	195	300	~2,300
Intel, (2005)	0.32	300	180	58	150
	0.09	65	295	58	110
	0.09	61	272	58	98

5.3. Benefits of Microchannel Liquid Cooling

As discussed above, compared with the conventional forced-air heat sinks ($R_{j\text{-}a}$ >> 0.3 ºC/W) [5.8, 5.9], an on-chip microchannel heat sink can offer an ultra low thermal resistance (as low as ~ 0.09 ºC/W). Such a small thermal resistance means that ultra high power density in small heating areas ("hot spots") can be cooled efficiently and quickly. Liquid cooling also promises the potential for low-temperature operation that can largely improve the performance of the transistors and interconnects.

5.3.1. Benefits of Integrated Thermal-fluidic Heat Sink for Cooling of "Hot Spots"

The heat generated from microprocessors is generally non-uniform as a result of the non-uniform power distribution. Multiple "hot spots" usually exist in any microprocessor, which are defined as the chip area with localized power density more than 300 W/cm^2 [5.10]. Over-heating at these "hot spots" can lead to early failure of the devices. Unfortunately, the isotropic nature of conventional heat spreaders makes them not effective for cooling the "hot spots", as illustrated in Figure 5.2. For the multi-core microprocessors, the number of "hot spots" may increase and cooling of the "hot spots" becomes a more challenging task for thermal management.

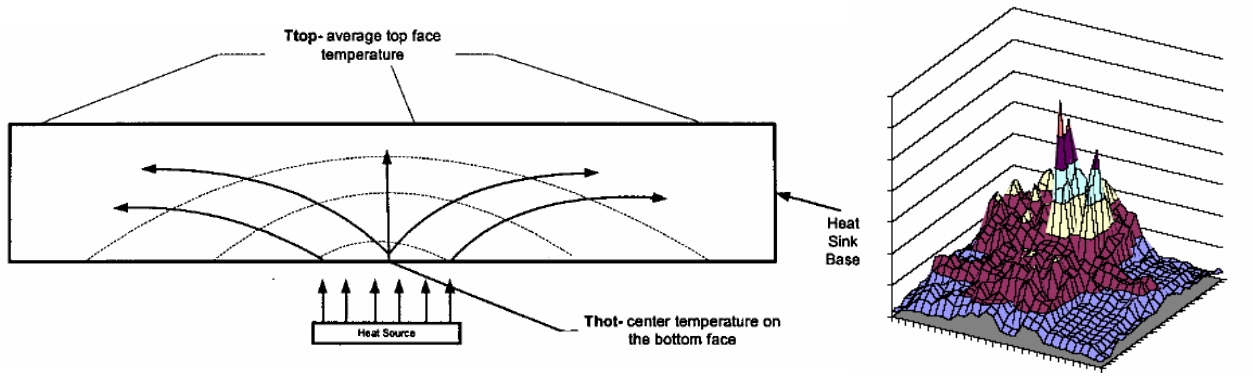


Figure 5.2: Schematic illustration of (a) the isotropic heat spreading with conventional heat sink and (b) the non-uniform power density distribution in microprocessors [5.10]

To solve this problem, various "future cooling technologies" have been evaluated and compared by Intel recently [5.11], which include refrigeration, conventional liquid cooling, thermal-electric cooling, and die-level microchannel cooling. Figure 5.3, shows a summary of their study on these cooling technologies. The comparison was based on the cooling limit improvement, which was defined as the percentage reduction in thermal resistance compared to the thermal resistance of typical air cooled heat sinks. Various density factors (ratio of overall thermal resistance to unit thermal resistance) were considered. Their results indicate that refrigeration demonstrates the best performance improvement (185%) for a low localized power density (Density factor~1.5 cm^{-2}) , while microchannel cooling at *die-level* appears to offer the best performance improvement (60%) for a highly localized power density (Density factor ~7.5 cm^{-2}). Therefore, the integrated on-chip microchannel heat sink is particularly promising for "hot spot" cooling.

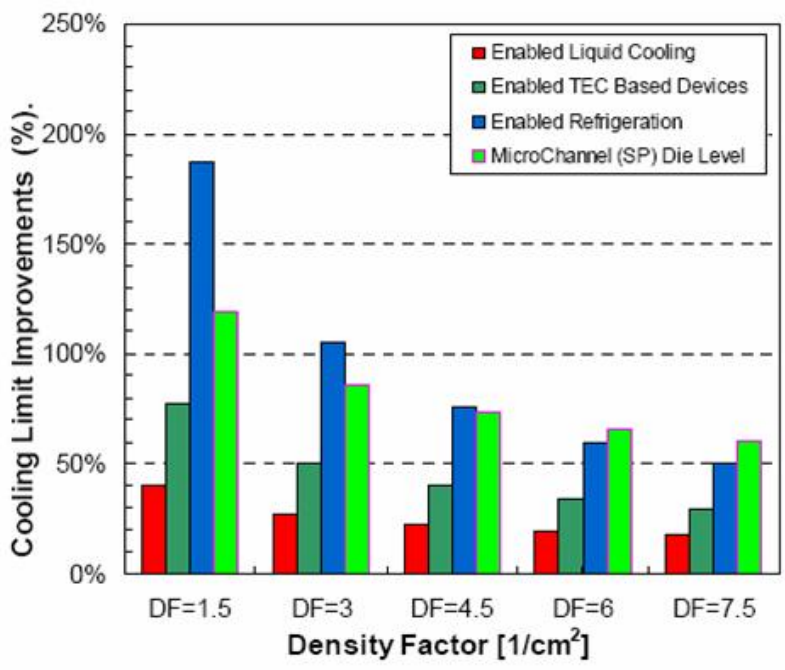


Figure 5.3: Comparison of the cooling limit improvement with various "future cooling technologies" for different density factors present in microprocessors [5.11]

5.3.2. Benefits of Low-temperature Operation for GSI Chips

Another important benefit of microchannel liquid cooling is the potential of low-temperature operation of GSI chips. Unlike conventional air cooling, liquid cooling can potentially reduce the operating temperature close to room temperature. A case study is done to evaluate the benefits of low-temperature operation based on the analysis using a system-level simulator called the Multilevel Interconnect Network Design Simulator (MINDS) [5.12, 5.13]. MINDS arranges wires in different interconnect levels based on a stochastic wiring distribution [5.14]. A detailed description of MINDS and its power estimation capabilities is given in [5.11] and [5.15]. Leakage power models [5.16] are built into MINDS to enable accurate power estimation for deep submicron technologies. It should be kept in mind that only the total signal power consumed by transistors, wires and repeaters is estimated by MINDS. I/O and clock power are not included in MINDS' power estimates.

A 70 nm ASIC chip with 55 million gates and 1 cm x 1 cm die area is considered. Two cases are taken: (1) T = 85^{o}C and (2) T = 35^{o}C. For both cases, the supply voltage is 1 V. A 70 nm Berkeley Predictive Technology Model (BPTM) [5.17] transistor and SPICE simulations were used to find the change in leakage current and threshold voltage with temperature. Mobility is taken to be proportional to $T^{-1.5}$ [5.18] and the temperature co-efficient of resistivity of copper is taken as 3.9×10^{-3} /^{o}C. A 20 W/cm^2 signal power density is fixed for the ASIC die. When the die is operated at 85 ^{o}C, the highest frequency that can be attained with this power density limit is found to be 1.5 GHz. If the chip temperature is reduced to 35^{o}C for Case 2 using the on-chip liquid cooling solution, it is found that the maximum frequency that can be attained is 1.95 GHz for the same 20 W signal power. Thus, a substantial 30% improvement in frequency can be attained using low-temperature liquid cooling. In addition, out of the 20 W signal power

dissipation of the chip, 38% (~7.5 W) is leakage power for the operation at 85 ^{o}C, while only about 15% of the total signal power is leakage power if the operating temperature is reduced to 35 ^{o}C. The principles behind these improvements at a low operating temperature are the resulting increase of carrier mobility, reduction of wire resistance and leakage current. The case study indicates that mobility is improved by 25%, wire resistivity is improved by 19%, and the leakage current is reduced by 3.13X when the operating temperature is reduced from 85 ^{o}C to 35 ^{o}C. Meanwhile, the low-temperature operation has other benefits in terms of reliability. For example, the electromigration life time can be largely increased with reduced operating temperatures according to the Black's equation [5.20]:

$$MTTF = AJ^{-n}e^{\frac{E_a}{kT}} \tag{5.10}$$

where *MTTF* is the mean-time-to-failure, *J* is the current density (A/cm^2), E_a is the activation energy (J), *k* is the Boltzmann's constant (J/°C), and *T* is the temperature (°C). *A* and *n* are material constants.

Furthermore, the lower operating temperatures also means smaller thermal excursion ranges during the operation in the field, which can lead to a longer fatigue life for the chip-to-board I/O interconnects (C4 solder joints, eg.) simply because the induced thermal-mechanical strain is reduced accordingly.

5.4. Hydraulic Analysis and Challenges for the Integrated Microchannel Heat Sink

As discussed above, a large flow rate is the key to a low thermal resistance for the on-chip microchannel heat sink, which could require a high pressure to drive the liquid flow. Assuming DI water is used as the working fluid and a fully developed laminar flow is present in the microchannels, the required pressure drop can be estimated as a function of the chip power

(heat flux) to be removed based on hydrodynamic equations in literature [5.1, 5.4, 5.5]. As illustrated in Figure 5.4, the fluidic paths between an inlet and an outlet for a straight channel pattern include the through-vias, the micro-pipes, and the microchannels. Since the micro-pipes and the vias are circular channels, the pressure drop can be calculated using [5.5]:

$$\Delta P = 2f\,\mathrm{Re}\frac{L_c}{D_h^2}\nu\mu \tag{5.11}$$

where the product of the friction and the Reynold number is a constant:

$$f\,\mathrm{Re} = 64 \tag{5.12}$$

Since the hydraulic diameter of a via equals its diameter, the velocity can be calculated as:

$$\nu = \frac{flow\quad rate}{overall\quad cross-\mathrm{sec}tional\quad area} = \frac{V}{n_{via}\pi(\frac{D_{via}^2}{4})} \tag{5.13}$$

Therefore, the pressure drop on the vias and micro-pipes can be expressed as:

$$\Delta P_{via+micropipe} = 512\cdot\frac{\mu\cdot\dot{V}\cdot(H_{via}+H_{pipe})}{n_{via}\cdot\pi\cdot D_{via}^4} \tag{5.14}$$

The pressure drop, ΔP_{ch}, on the microchannels can be estimated using the equation derived in Chapter 4:

$$\Delta P_{ch} = \frac{1}{2}f\cdot\mathrm{Re}\cdot L_c\cdot\frac{\mu\cdot\dot{V}(1+W_c/H_c)^2}{n\cdot H_c\cdot W_c^3} \tag{5.15}$$

The overall pressure drop between an inlet and outlet can then be calculated as:

$$\Delta P_{inlet/outle} = \frac{1}{2}f\cdot\mathrm{Re}\cdot L_c\cdot\frac{\mu\cdot\dot{V}(1+W_c/H_c)^2}{n\cdot H_c\cdot W_c^3} + 512\cdot\frac{\mu\cdot\dot{V}\cdot(H_{via}+H_{pipe})}{n_{via}\cdot\pi\cdot D_{via}^4}$$

$$= \left\{\frac{1}{2}f\cdot\mathrm{Re}\cdot L_c\cdot\frac{(1+W_c/H_c)^2}{n\cdot H_c\cdot W_c^3}512\cdot\frac{(H_{via}+H_{pipe})}{n_{via}\cdot\pi\cdot D_{via}^4}\right\}\cdot\mu\cdot\frac{Q}{\Delta T_{inlet/outlet}\cdot\rho\cdot C_p} \tag{5.16}$$

Based on the above equations, the minimum hydraulic pressure drop can be calculated for given dimensions. Figure 5.4 plots the calculated pressure drop as a function of the power dissipation and temperature between inlets/outlets (caloric heating of the coolant). Using the dimensions of the microchannels (n_{ch} = 50; W_{ch} = 100 μm; H_{ch} = 200 μm) and the thermal-fluidic I/O interconnects in the present design, the model suggests that it is possible to cool the ITRS projected power dissipation with a pressure drop of less than 1 atm. It must be pointed out that the pressure drop in the above analysis is the minimum required pressure because other effects such as flow splitting, combining, or turning have not been included. These effects may contribute to the overall pressure drop considerably and need to be further investigated in the future.

In practice, the additional pressure drop along the fluidic paths at the board level may also need to be considered depending on their dimensions, total length, and the nature of flow (turbulent or laminar). In this work, pressure loss on the board level fluidic paths is negligible because of their short length and large hydraulic diameters.

As indicated in Equation 5.13, the pressure loss on fluidic I/Os (vias and micro-pipes) may play an important role in the overall pressure drop if their number is small. However, increasing the number of the fluidic I/Os requires more chip area for the vias and the micro-pipes. Therefore, chip area penalty should be also considered for the through-vias and micro-pipes. Figure 5.5 shows the calculated pressure drop on the thermal-fluidic I/Os in reference to the occupied chip area by them. Obviously, the theoretical pressure drop on the fluidic I/Os can be largely reduced if the number of fluidic I/Os increases, while the occupied chip area by the fluidic I/Os increases linearly.

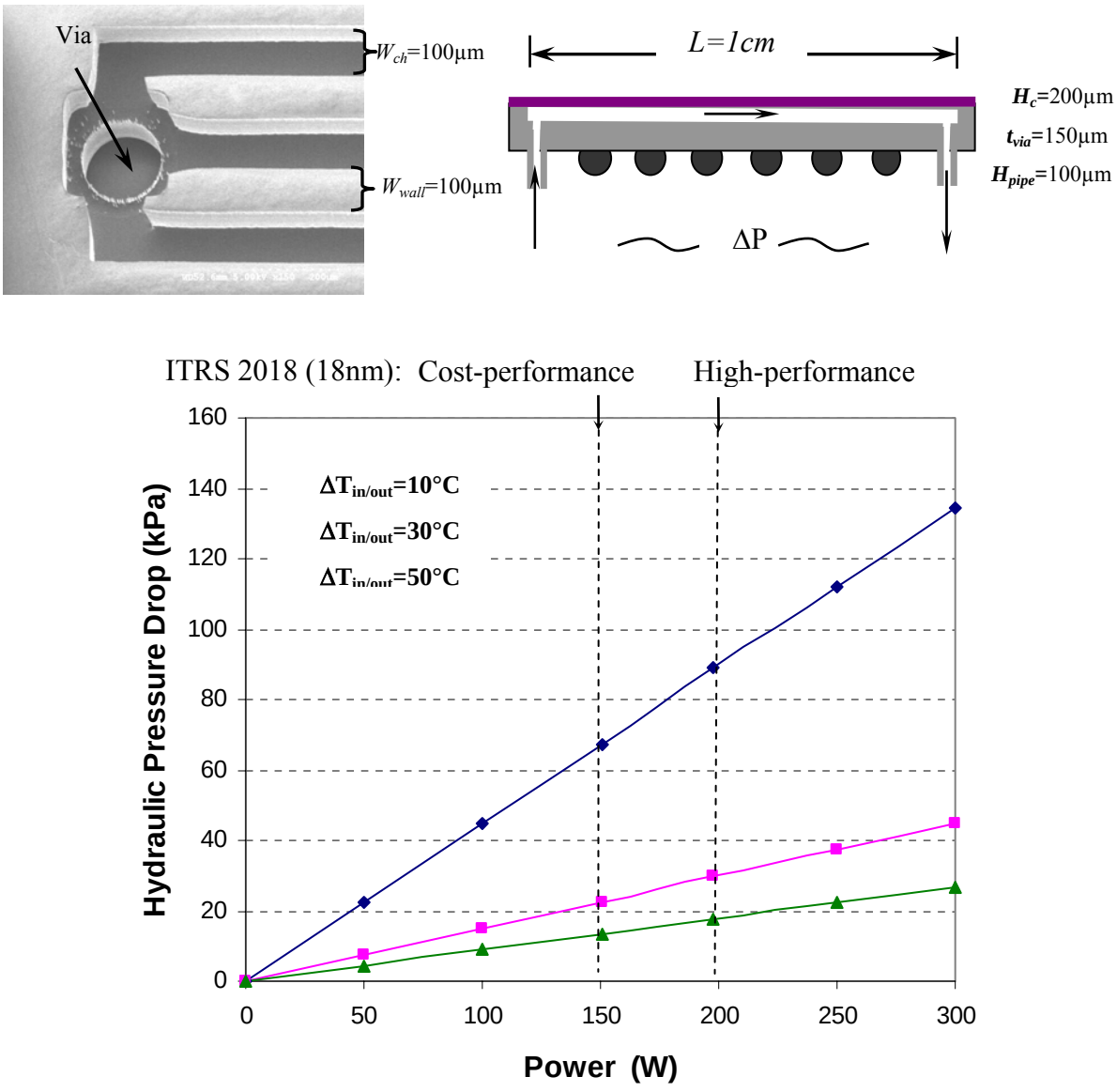


Figure 5.4: Illustration of the on-chip thermal-fluidic path and the calculated pressure drop as a function of power for various temperature rises between the inlets and the outlets with DI water as the coolant assuming fully developed flow (W_c=100µm, H_c= 200µm, $n_{channels}$=51, #_of_micropipes=34, D_{via}=100µm).

Under current design, 17 pairs of through-chip vias (D_{via} = 100 µm) occupy an area of 0.00267 cm^2, while the 17 pairs of micro-pipes (D_{pipe} = 250 µm) occupy an area of 0.0167 cm^2. For a chip that is 1.4 cm^2 (cost-performance applications projected by ITRS), these thermal-fluidic I/Os occupy less than 1.19% chip area. Therefore, the incurred chip area penalty is a

small fraction of the total chip area. The corresponding pressure loss on the fluidic I/Os is around 3.2 KPa. For a chip that is 3.1 cm^2 (high-performance applications projected by ITRS), more fluidic I/Os can be easily accommodated with even smaller pressure loss on them. Of course, the number of thermal-fluidic I/Os and the size of the vias and micro-pipes can be further optimized to provide a sound trade-off between the pressure drop and the chip area penalty in practice.

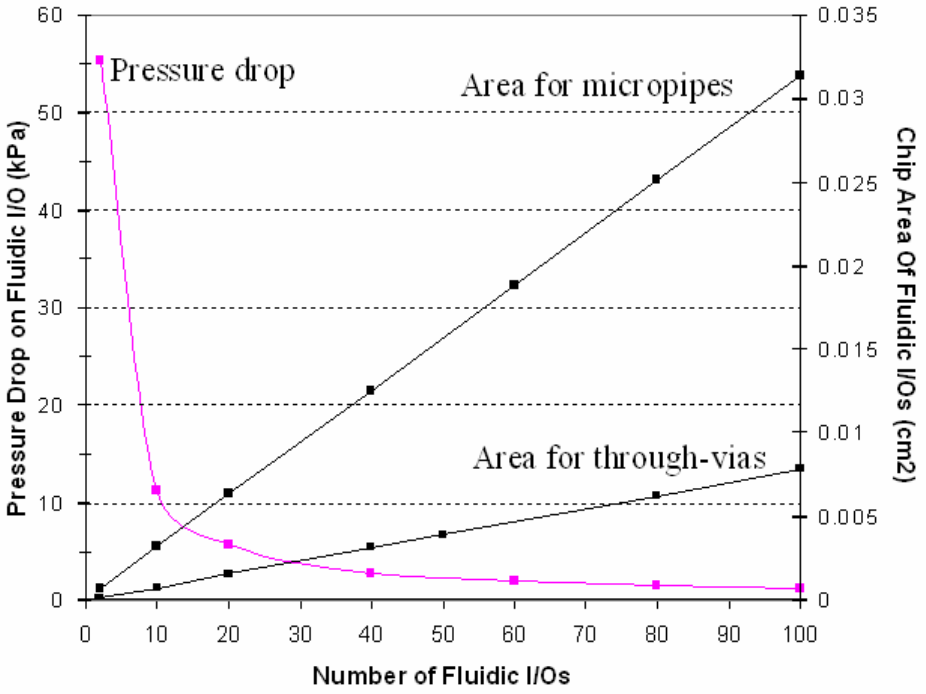


Figure 5.5: Illustration of the trade-off between the chip area penalty and pressure drop on the thermal-fluidic I/Os as a function of the number of thermal-fluidic I/Os. A power of 100W is assumed with a fluid temperature rise of 30 °C. The dimensions are same as those in Figure 5.4.

To supply the required pressure and the flow rate for a microchannel heat sink, sufficient pumping power is necessary. The theoretical pumping power can be simply calculated as the product of the flow rate (m^3/s) and the pressure drop (N/m^2) [5.26]:

$$Pumping \quad Power = \Delta P \times \dot{V} \tag{5.17}$$

In Figure 5.6, the calculated theoretical pumping power is plotted as a function of the heat flux for various temperature rises on the cooling liquid between inlets and outlets. It is

shown that the theoretical pumping power consumed on the chip-level microchannel heat sink is negligible compared with the amount of dissipated power. This is not surprising because a pumping power of ~ 2 W was used to remove 790 W/cm^2 in the Tuckerman's work [5.1]. In practice, much higher pumping power will be needed for actual fluidic systems. For instance, the pumping efficiency of available compact pumps is usually less than 70%. In addition, much longer fluidic paths should be expected in board-level fluidic systems. Nevertheless, the hydraulic requirement on any fluidic paths can be reduced if their hydraulic diameters (channel dimensions etc.,) are large. Fortunately, the board-level channels are only used for fluidic delivery and do not need to be very small for a high heat transfer efficiency. It is actually much easier to design and fabricate large channels at the board-level using various simple techniques [5.21 - 5.24].

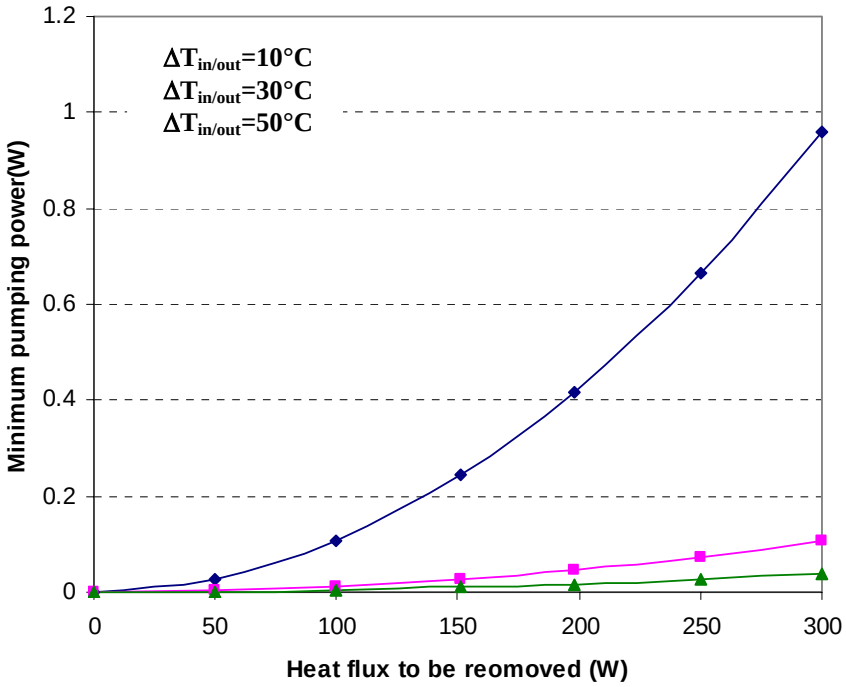


Figure 5.6: The theoretical minimum pumping power consumed for a microchannel heat sink as function of the heat flux to be removed. (The dimensions of the microchannels are same as those in Figure 5.4)

5.5. Thermal-Fluidic Demonstration and Measurement

To demonstrate liquid cooling operation with the prototype on-chip microchannel heat sink, on-chip heaters/thermometers must be integrated and test samples must be assembled and connected with a close loop thermal-fluidic system. This section will describe the details of the test chips, measurement methodologies, and demonstration of the cooling operation.

5.5.1. Integration and Characterization of the Thin-film Heaters/Thermometers

Multi-function thin-film heaters/thermometers were designed and fabricated on the test chips. The heaters are made of thin-film Ti/Pt (~300 Å/1500 Å) using a lift-off process described as follows: a 10 μm thick negative photoresist (NR9-8000P, 2000rpm/500r/s/40s) was first spun and patterned at the front of the wafer. After the development and a short RIE descum, Ti/Pt film was deposited using DC sputter. The photoresist was then removed by soaking and agitation in Acetone and the heaters were left as shown in Figure 5.7. The reason that Pt was selected for the thin-film heater/thermometer is because it is a thermally stable noble metal and its resistance changes as a linear function of temperature. According to literature [5.25], the temperature coefficient of the Ti/Pt film is 0.0033 ~ 0.0039 K^{-1} and can be used at temperatures up to 800 °C upon characterization. Therefore, the heaters can also serve as thermometers for the purpose of temperature sensing. After the heaters/thermometers were deposited, the chip surface was passivated with a SiO_2 layer (0.2 μm) and coated with a final polymer layer (~10μm thick Avatrel 2195P). Vias were opened through the passivation and solder bumps and polymer micro-pipes were then fabricated for electrical and fluidic paths.

Figure 5.8 shows the SEM photographs of the completed test chip with the integrated thin-film Ti/Pt resistors, solder bumps and polymer micro-pipes. The heights of the solder bumps and the micro-pipes are 75 μm and 90 μm respectively.

As shown in Figure 5.9, corresponding on-board wires and pads were designed for access to individual segments of the heater arrays and 25 heating zones across the whole chip area (1 cm×1 cm) may be heated and tested individually.

Figure 5.10 shows the optical micrograph of a bonded test chip. To characterize the temperature dependence of Ti/Pt resistors, the sample was heated up to various temperatures in a small oven and the DC resistance of the individual heaters was then measured. Figure 5.11 shows the measurement results that verify the excellent linear relation between the heater resistance and the temperature. The slope of the R-T curves is approximate 1.8 ~ 2 Ω/°C, which gives a sufficient sensitivity for resistance measurement using a multimeter. Good consistence was also observed between various heaters.

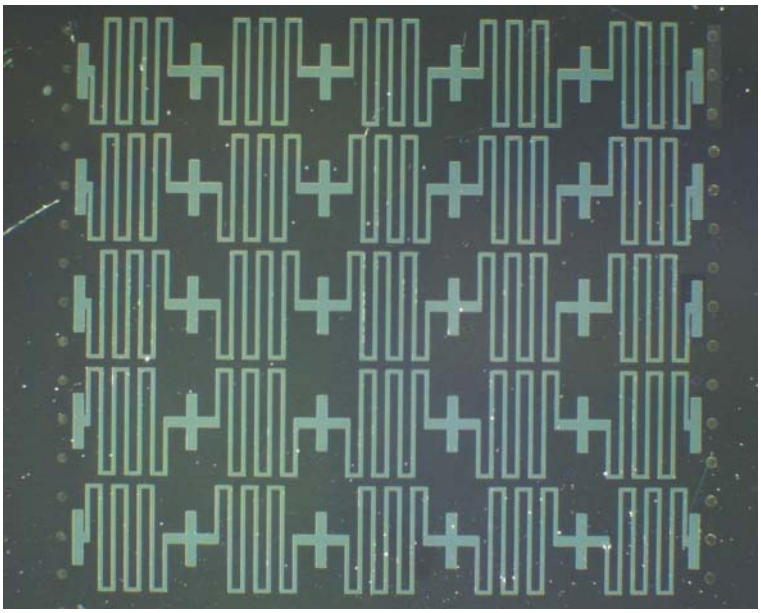
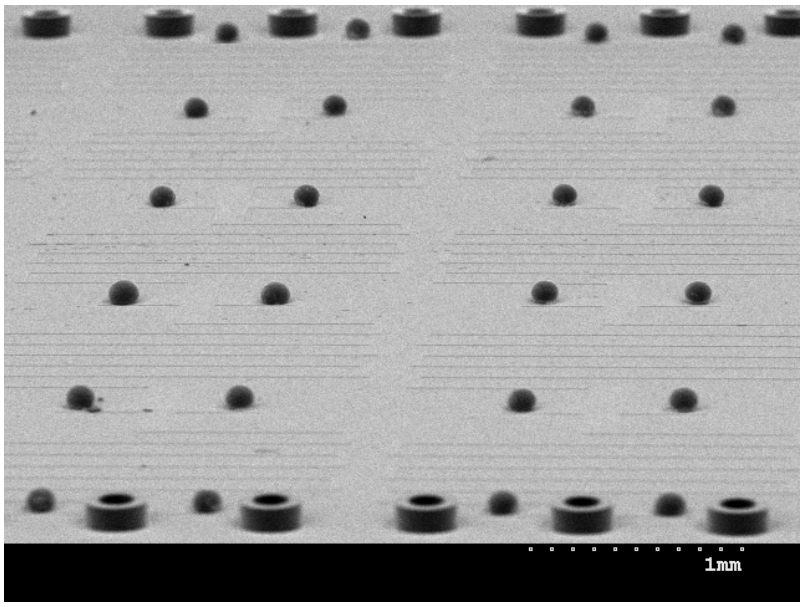


Figure 5.7: Optical micrograph of the Thin-film Ti/Pt heater/thermometers at the chip front side. The total test area is 1cm^2 and each heater occupies 4 mm^2.



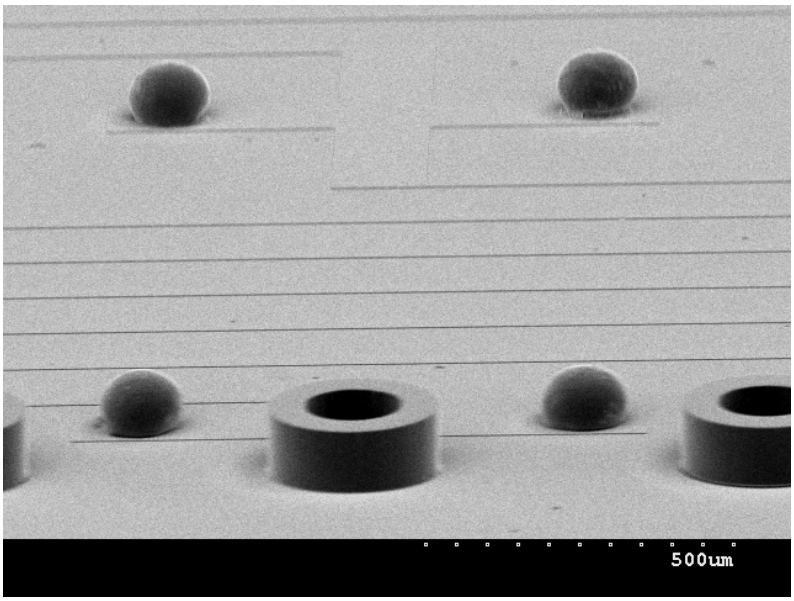


Figure 5.8: Thin-film Ti/Pt heater/thermometers integrated with micro-pipes and solder bumps at the chip front side. (t_{heater} ~ 0.18 μm; h_{bump} ~ 75 μm; h_{pipe} ~ 90 μm)

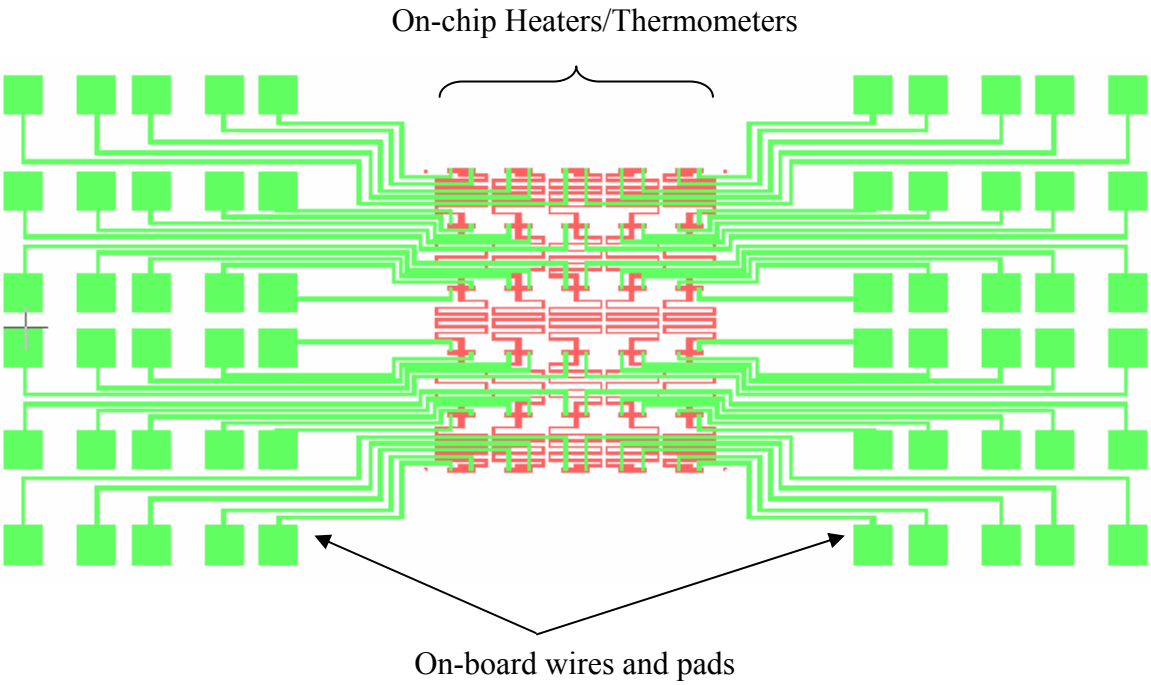


Figure 5.9: Layout of the on-chip test heaters and on-board Cu lines.

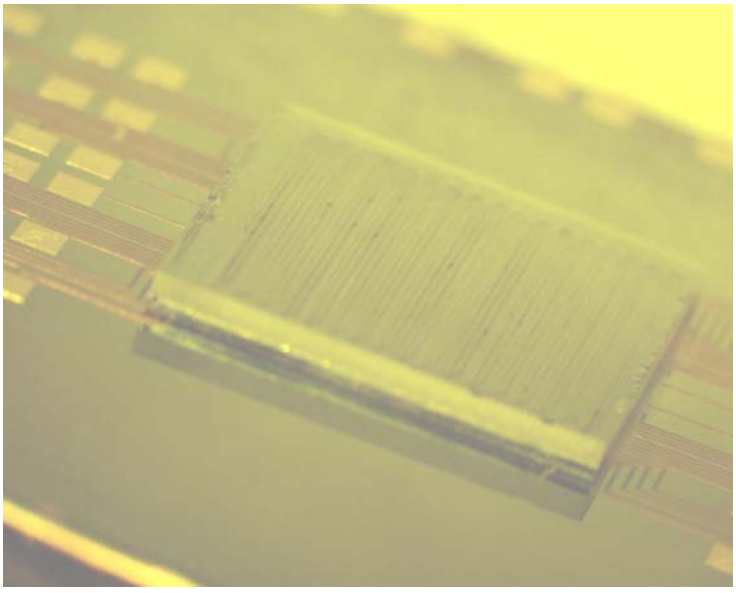


Figure 5.10: Photograph of a bonded test chip for temperature characterization of the heaters.

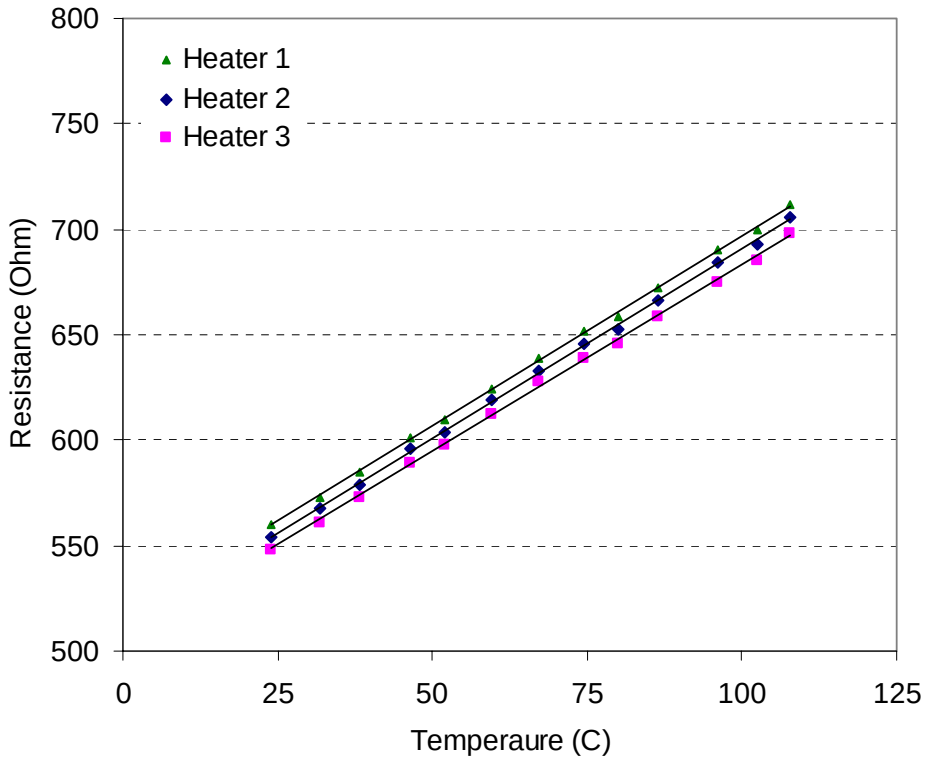


Figure 5.11: Change of DC resistance of the heaters as a linear function of temperature.

5.5.2. Thermal-Fluidic Measurements

Figure 5.12 shows the schematic of the thermal-fluidic test set-up. The key components include a mini pump, a DI water reservoir, a digital flow rate meter, a pressure sensor, and a heat exchanging metal block with cold water supplied by a separate chiller. A DC power supply was used to provide the necessary voltage and current for the heater. The pressure drop and flow rate can be automatic collected by a computer, while the corresponding heating power and the actual DC resistance can be simply calculated based on the voltage and current measured manually. As described above, the on-chip temperature rise is then obtained based on the DC resistance change of the thin film heaters. During the testing, the voltage and current values at each data point were collected after stabilization for at least 30 seconds to ensure an accurate read-out.

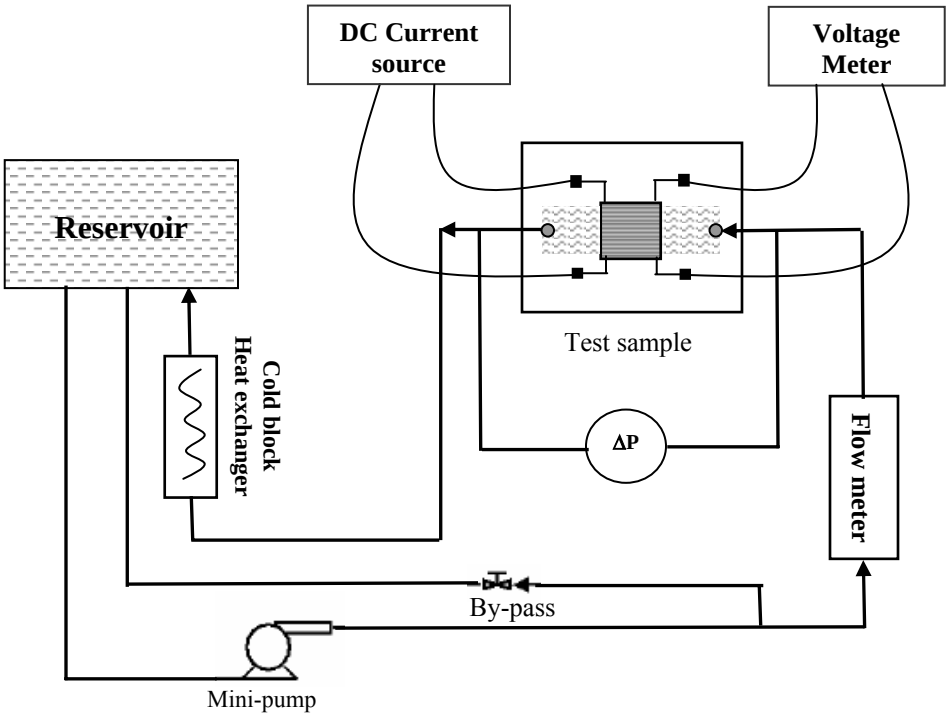


Figure 5.12: Schematic illustration of thermal-fluidic measurement set-up.

Figure 5.13 shows a test chip bonded onto a substrate equipped with through-vias using the assembly process described in Chapter 4. There are a total of 51 parallel microchannels evenly distributed across an area of ~ 1cm^2. Plastic fluidic tubes were mounted at the back side of the testing substrate to connect with fluidic through-vias. The underfill is clearly visible at the edge of the chip, which was applied to seal the micro-pipe connections with the orificies on the substrate. After the underfilling process, fluidic continuity and electrical continuity were both tested. The test pads on the substrate were then soldered with Cu wires. Since the individual heaters can be accessed, various combinations of heat distribution may be tested by routing the test pads. A "bread-board" was used for tracking the terminals. The test chip has microchannels enclosed with transparent Pyrex wafer for the purpose of inspection. As shown in Figure 5.14, the height of the microchannels is approximately 200 μm and their width is around 100 μm.

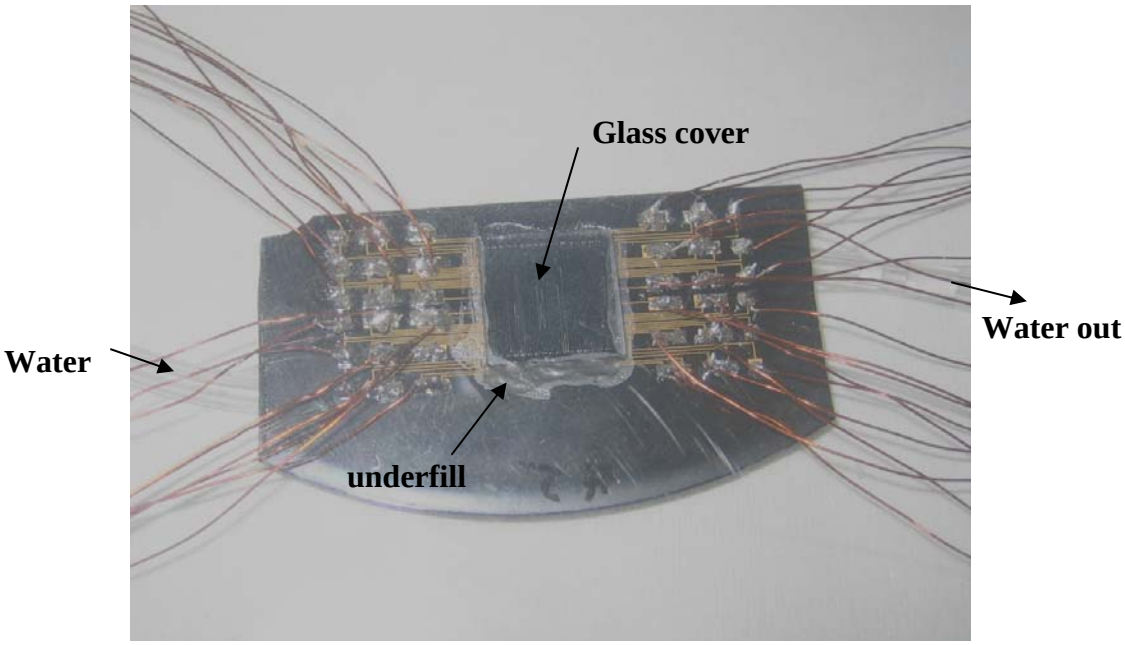


Figure 5.13: A test chip bonded on a substrate with through-vias connecting with fluidic tubes. (51 microchannels distributed across a chip area of 1 cm^2)

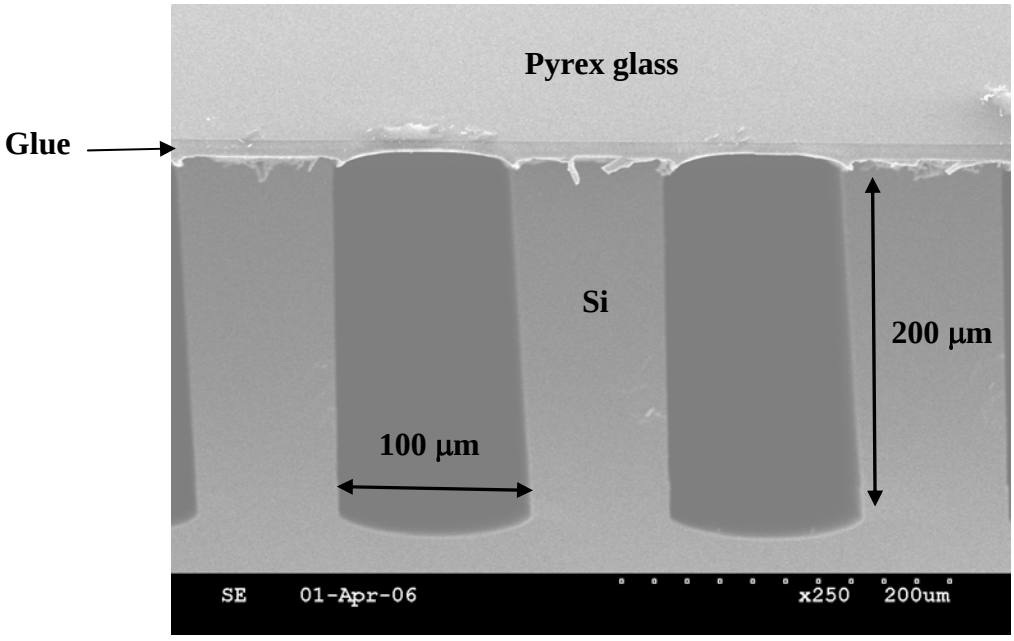


Figure 5.14: Cross-sectional view of the microchannels enclosed by glue bonding. (channel width is approximately 100 μm and the channel height is around 200 μm)

5.5.2.1. Hydraulic Measurement

Using the fluidic testing set-up described in Chapter 4, the hydraulic pressure drop across the fluidic path was measured and plotted as a function of the flow rate in Figure 5.15. The predict pressure drop was calculated using Equation 5.14 for the purpose of reference. At flow rates below 65 ml/min, the measured values closely agree with the prediction, but a deviation becomes more obvious as the flow rate increases. The deviation at large flow rates might be from the following reasons: First, as mentioned previously, Equation 5.14 assumes an ideal fully-developed flow path and does not include many effects such as flow splitting, combining, or turning. Second, the channel geometries along overall fluidic paths are not perfectly uniform due to fabrication limitation. Finally, the calculation is based on an assumption that the stream is evenly distributed across all the parallel microchannels, which may not be accurate for the simple tubing connection in the present demonstration. Accurate predication of the hydraulic behavior is always a difficult task for the microchannels in complex systems [5.3]. Particularly, the fluidic distribution manifold needs to be optimized in future designs.

Figure 5.16 shows the actual pumping power as a function of the flow rate for the fluidic paths in the test samples. The pumping power increases rapidly with increasing flow rate. The theoretical minimum pumping power was also calculated and plotted as a reference. Evidently, the actual pumping power is also much higher than the predicted, which is expected due to the similar reasons mentioned above. In addition, the pump efficiency is usually smaller than 70%. Nevertheless, as observed in various studies [5.1, 5.5, 5.26], the pumping power of the microchannel cooling is usually much smaller compared to the power dissipation. Similar results were obtained in this work. For instance, the actual measured pumping power is only 1.254 W for a large flow rate of 133ml/min, which is sufficient to dissipate a power of ~ 46 W.

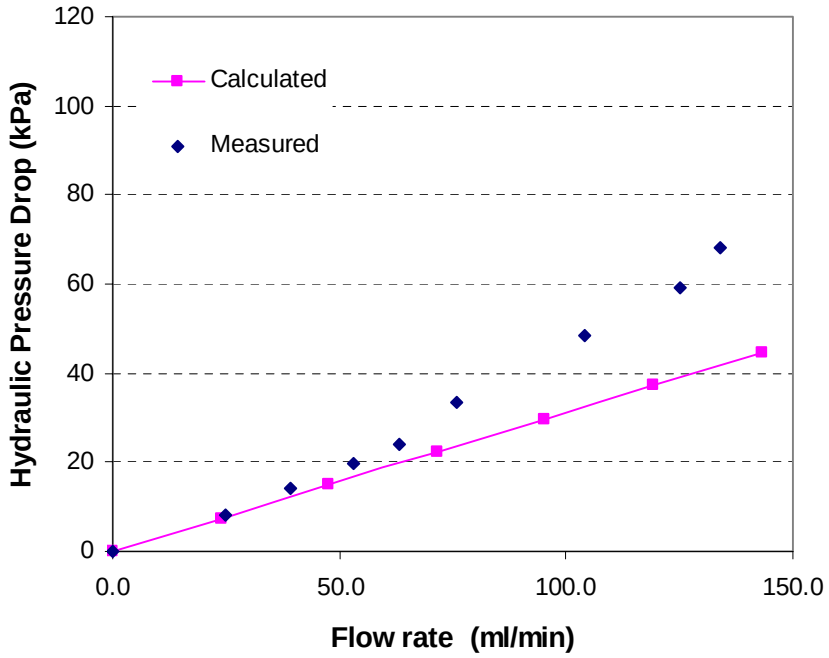


Figure 5.15: Hydraulic pressure drop as a function of DI water flow rate through the fluidic paths in the test sample with 51 parallel microchannels (h ~ 200 μm). The predicated results are based on Equation 5.14.

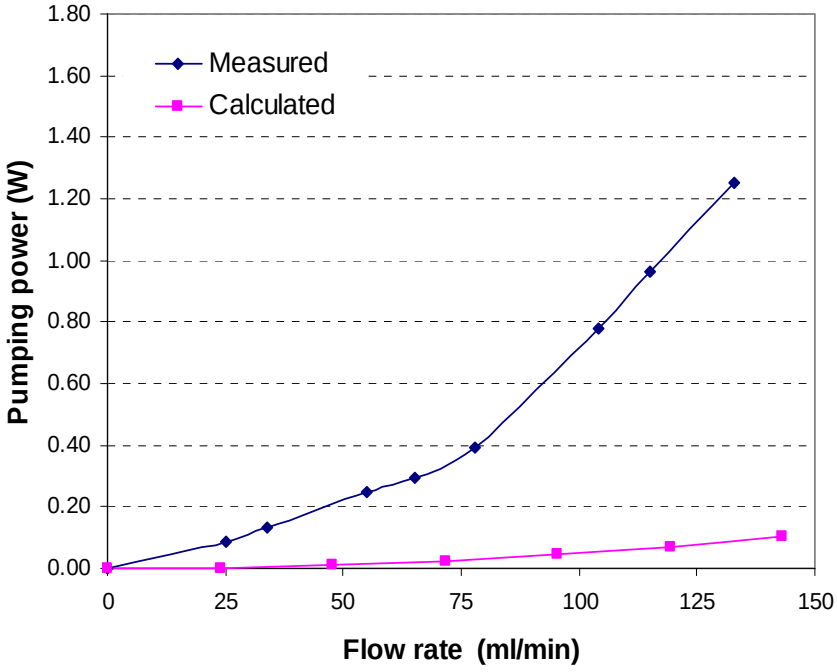


Figure 5.16: Measured pumping power as a function of the DI water flow rate through the fluidic paths in the test sample.

5.5.2.2. Thermal Resistance Measurement

Figure 5.17 illustrates the resistor network that works as heaters and thermormeters. The flow direction of DI water in the microchannels is in parallel with the current flow. Since the resistance of the heaters on the present test chip is relatively large (R_o~ 563 Ω), the required supply voltage to heat up the whole 1 cm^2 chip area is too high for a regular DC power source. Thus, only a 60% chip area was tested for global heating and the corresponding resistance of the parallel heaters is around 338 Ω. The average temperature in the heating area can then be monitored through the change in its DC resistance.

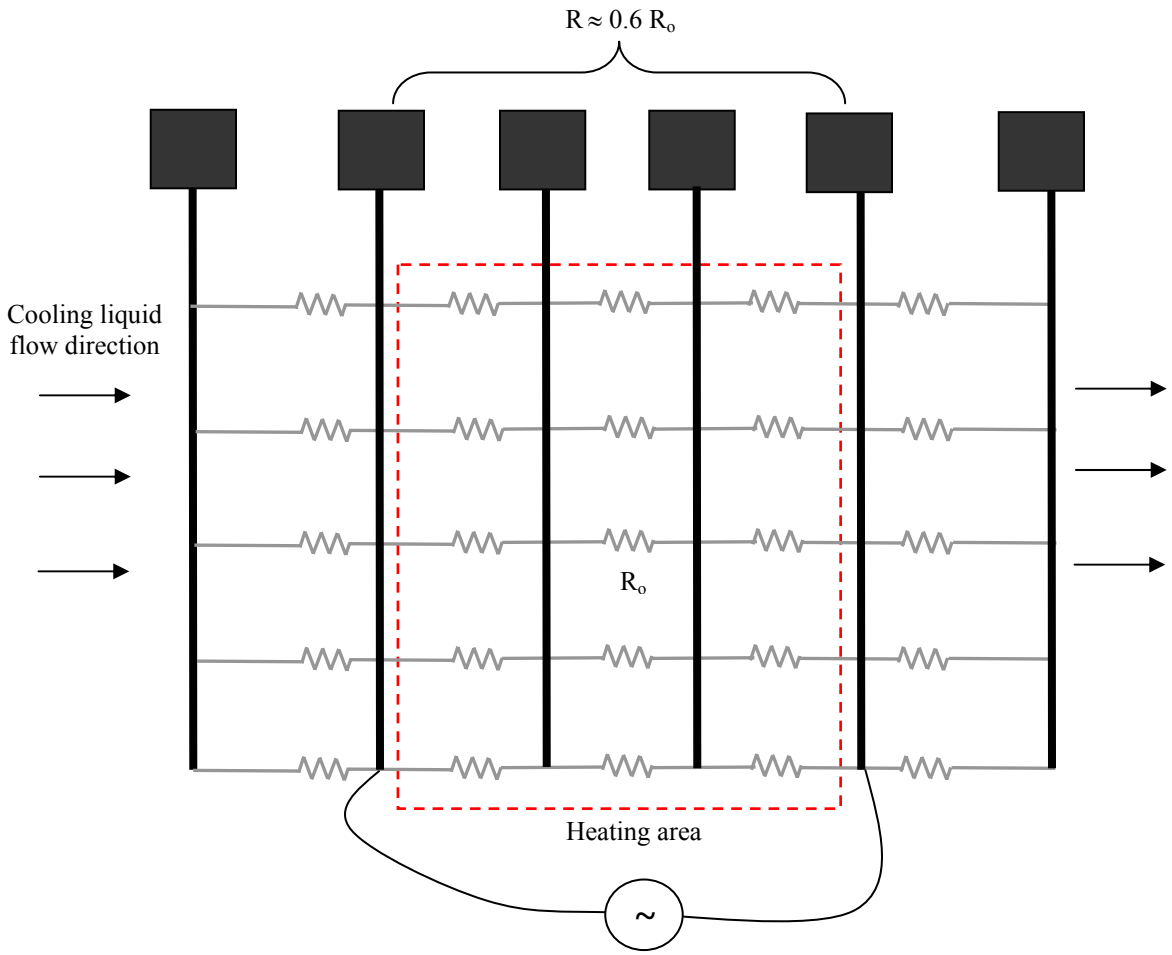


Figure 5.17: Illustration of temperature measurement through resistance change on the individual segments of the heater array.

Figure 5.18 and Figure 5.19 plot the results of temperature measurements at the inlet, outlet, and the average chip temperature, when the resistors were heated with a power of 45 W under flow rate of 65 ml and 104 ml. The inlet and outlet temperatures were measured by thermal-couples directly and recorded in the computer software (Data Logger), while the chip temperature was measured manually based on the change in the resistance of the heaters. Before each measurement, the circulating chiller was first turned on to maintain a low temperature at the metal block heat exchanger (20 ~ 22 °C) and the DI water flow was then turned on for the microchannels. After the DI water flow rate was stabilized, the DC supply power was turned on to heat the chip and the temperatures were measured. As shown in Figure 5.18 and Figure 5.19, during the testing, the supply power was intentionally turned on and off for multiple times to verify the consistency of the measurement results.

It can be seen that the on-chip temperature as well as the outlet temperature increase rapidly once the heating power is turned on, while the inlet temperature does not change because the metal block heat exchanger dissipated the power with the aid of the circulating chiller. Under a flow rate of ~65 ml/min, the average chip temperature rise is 18.1 °C and the corresponding thermal resistance for the chip is 0.4 °C/W, which translates to a unit thermal resistance of as 0.24 °C-cm^2/W considering that the heating area is 0.6 cm^2. Under a larger flow rate (~104 ml/min), the average temperature rise is 12.7 °C and the corresponding thermal resistance for the chip is 0.28 °C/W, which translates to a unit thermal resistance as small as 0.17 °C-cm^2/W.

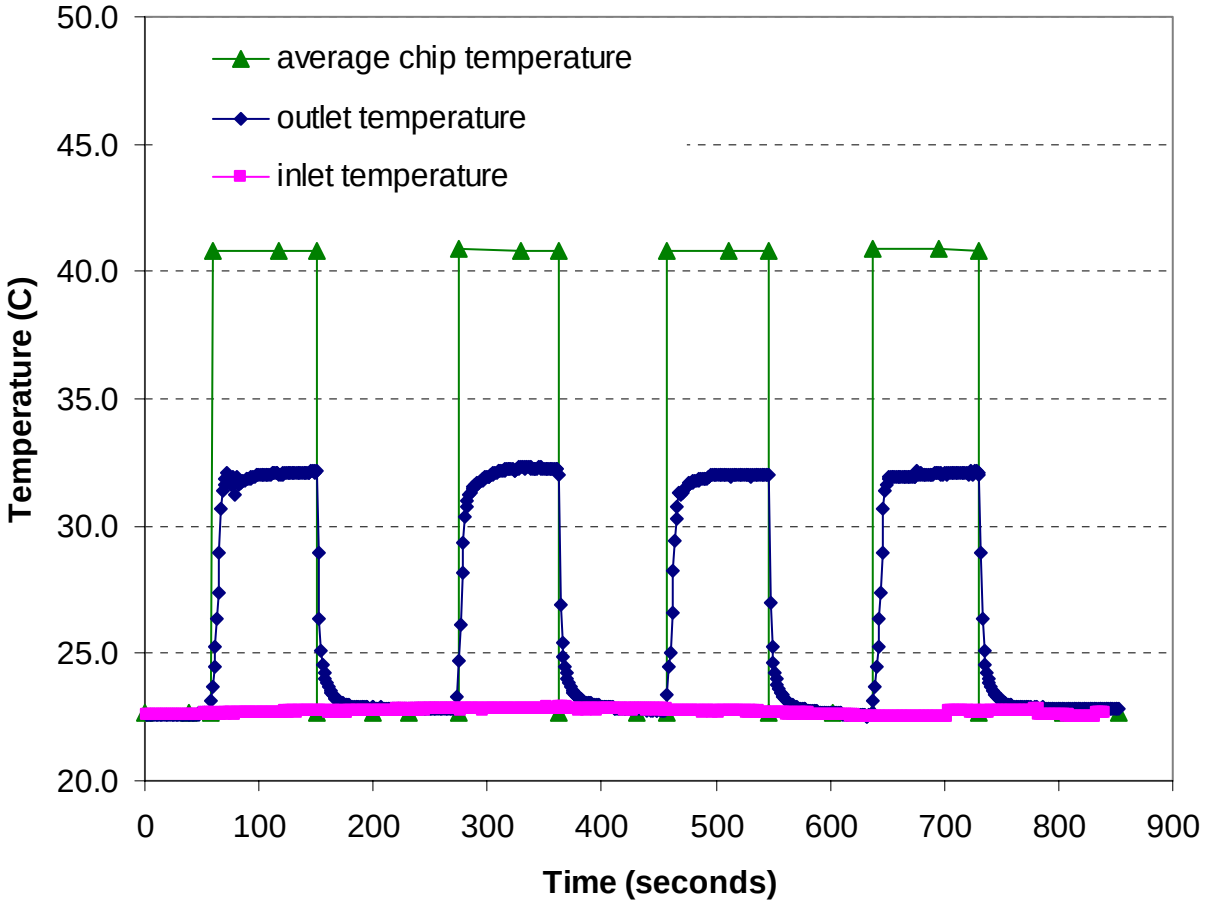


Figure 5.18: Measured temperature at the inlet and outlet in comparison of the average chip temperature at a flow rate of 65 ml/min. The calculated unit thermal resistance is around 0.24 °C-cm^2/W. (Overall power is ~45 W; heating area is ~0.6 cm^2; on-chip temperature rise is 18.1 °C)

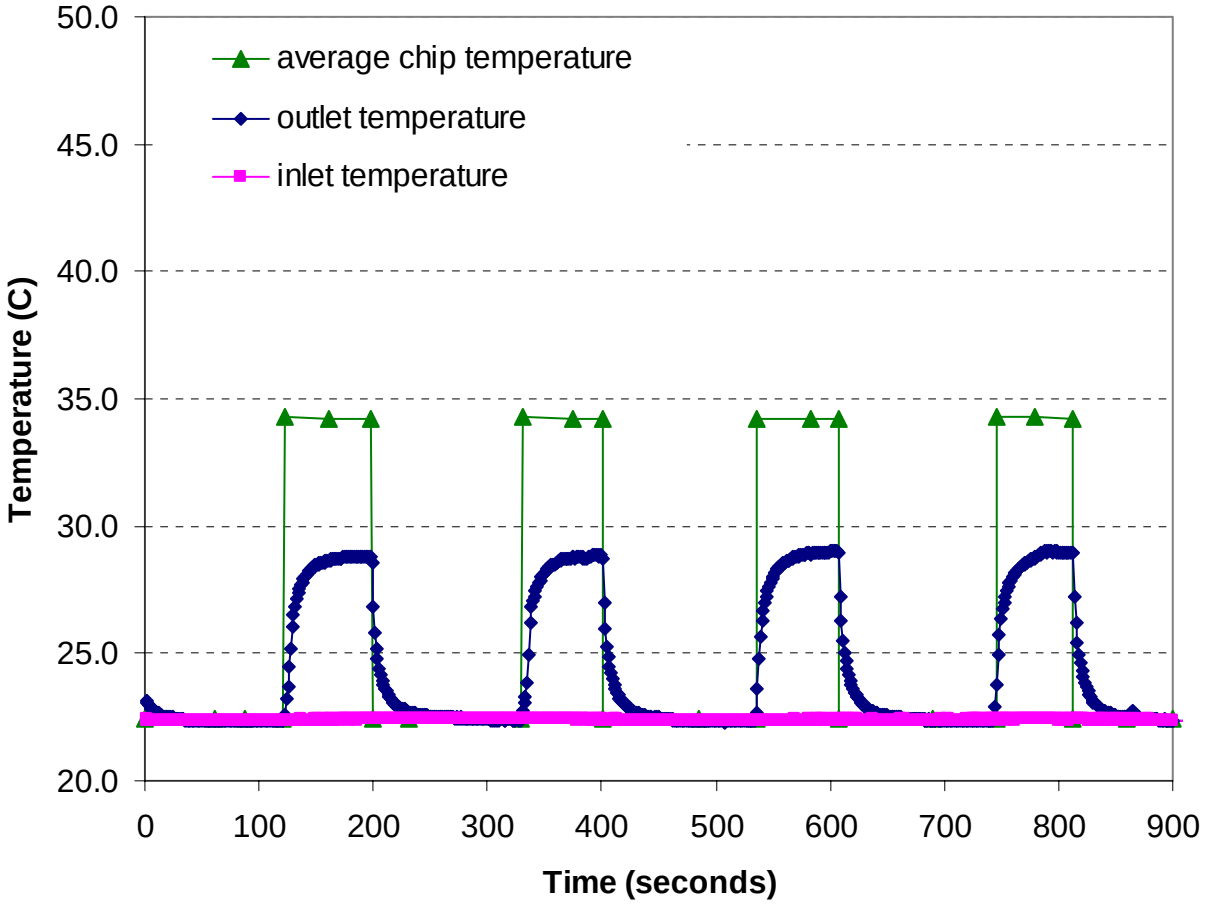


Figure 5.19: Measured temperature at the inlet and outlet in comparison of the average chip temperature at a flow rate of 104 ml/min. The calculated unit thermal resistance is around 0.17 °C-cm^2/W. (Overall power is ~45 W; heating area is ~0.6 cm^2; on-chip temperature rise is 12.7 °C)

5.5.2.3. Cooling of Localized Heating Power

As discussed previously, an important benefit of using an on-chip microchannel heat sink is to enable the cooling of highly localized power density (or hot spots). The heater design in this work also allows testing of individual heat zones. Thus, experiments were performed by supplying a large localized power in a small area (~0.08 cm^2). Figure 5.20 shows the measured temperature rise at the heating area as a function of localized heating power. As expected, the

measured temperature rise on the heaters increases with increasing localized power density; the temperature rise is reduced as the DI water flow rate increases. It is also observed, under a small flow rate, the temperature of the heaters tends to fluctuate to a small extent and rapidly increase as the heating power density increases. Under a larger flow rate, the $\Delta T - P$ curve becomes nearly linear and a localized power density larger than 325 W/cm^2 was tested with a temperature rise of 46 °C at a flow rate of 125 ml/min.

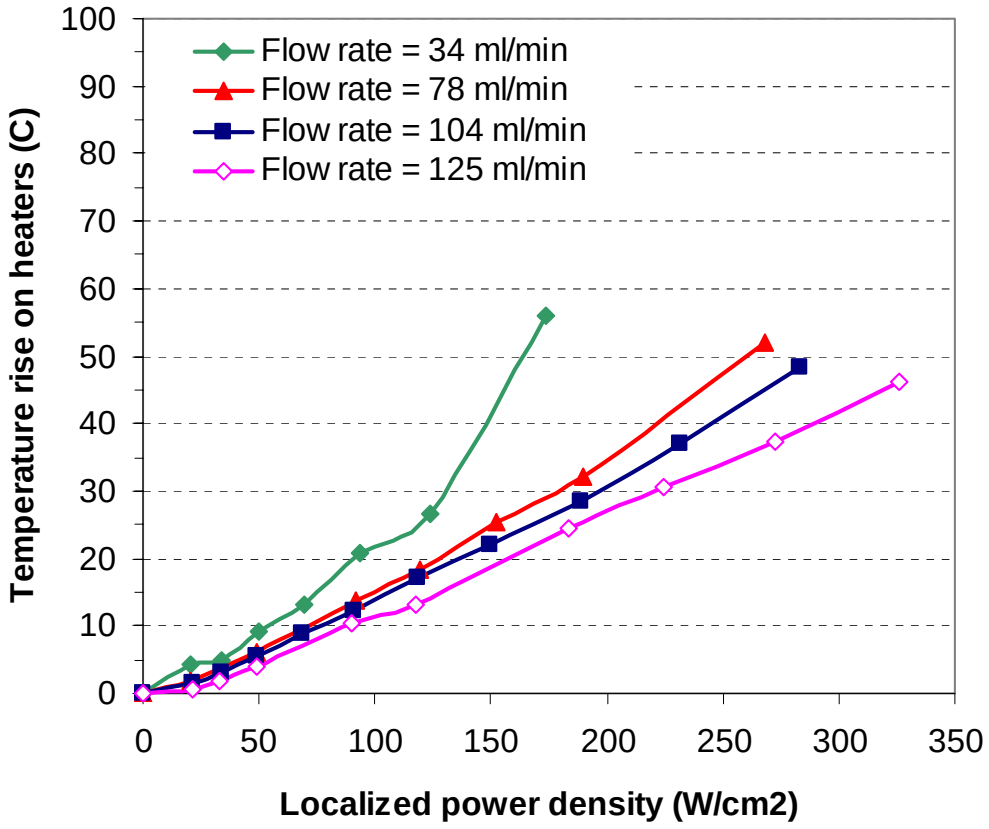


Figure 5.20: On-chip temperature rise as a function of localized heating power under various DI water flow rates (with localized heating area of ~ 0.08 cm^2).

Figure 5.21 shows the measured temperature change at the inlet and outlet as a function of the localized heating power density. It is observed that the outlet temperature increases rapidly

with an increasing heating power density at a small flow rate. However, as the flow rate is increased beyond 100 ml/min, the outlet temperature does not change much. This is understandable because the thermal resistance contributed by caloric heating becomes very small with a large flow rate. Although the power density is high in the small heating area, the actual power is less than 25 Watts, which can be easily dissipated through the DI water under the large flow rate.

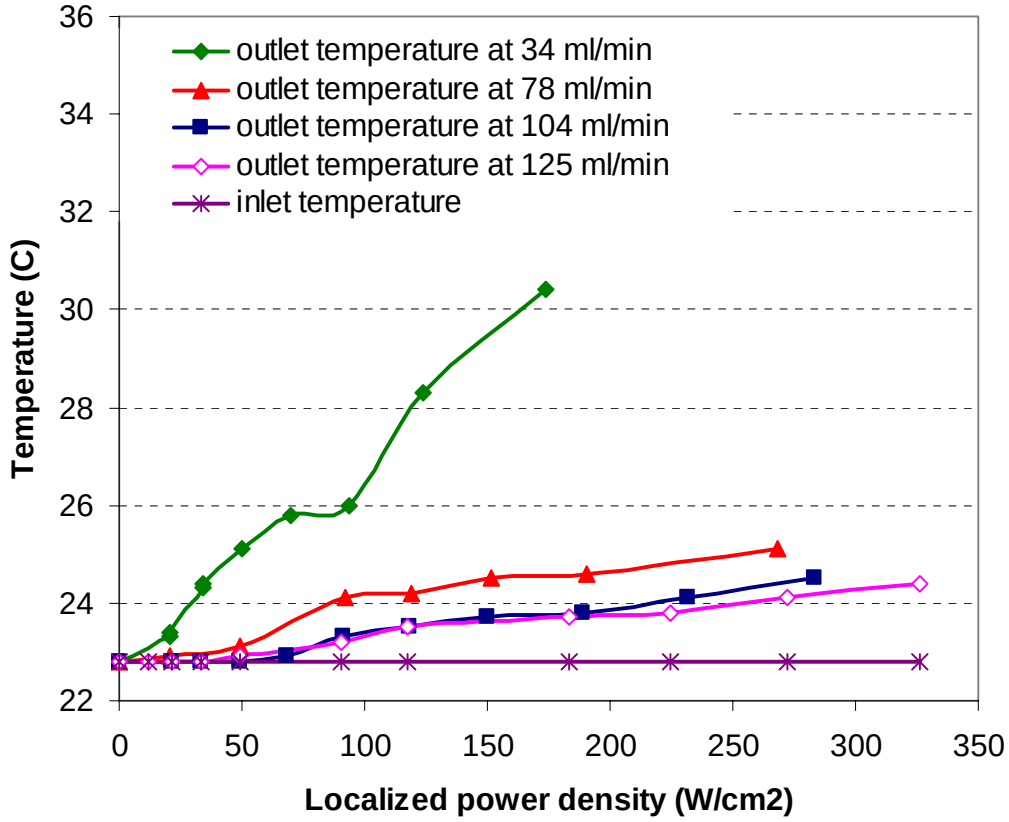


Figure 5.21: Measured inlet temperature and outlet temperature as a function of the localized heating power density for various DI water flow rates (with localized heating area of ~ 0.08 cm^2).

5.6. Summary

This chapter first discussed the benefits of an integrated microchannel heat sink through basic thermal resistance analysis. With a thermal resistance significantly lower than that of conventional air-cooled heat sinks, liquid cooling has the potential to address the "hot spot" cooling and to enable chip operation at relatively low temperatures. The low-temperature operation, in turn, leads to more benefits in terms of performance improvement and reliability improvement.

For the first time to the author's knowledge, operation of a prototype integrated thermal-fluidic package based on the mirco-pipe I/O technology, on-chip microchannels, and board assisted fluidic delivery was demonstrated through fabrication, assembly and testing. A dual-function thin-film heater/thermometer has been designed and integrated for cooling demonstration and measurement. With 51 microchannels (W_{ch} ~ 100μm, h_{ch} ~ 200μm) across chip area of 1 cm^2, unit thermal resistance below 0.2 °C-cm^2/W was demonstrated under a heating power of ~45 W at a DI water flow rate of 104 ml/min. Furthermore, cooling of a localized power density of more than 325 W/cm^2 was also demonstrated with local temperature rise less than 50°C at a flow rate of 125 ml/min. The measured pumping power is only a small fraction (~2.78%) of the power to be dissipated.

Chapter 6. Compatible Electrical, Optical, and Thermal-fluidic I/O Interconnects Based on Polymer Pillars

6.1. Introduction

Although MEMS-type compliant I/O interconnects were studied in Chapters 2 and 3 to address the CTE mismatch between a chip and its mounting substrate and to eliminate the need for underfill, another potential solution is to maintain a large stand-off height to reduce the thermal mechanical strain, as suggested by:

$$Strain = \frac{Displacement}{Height} \tag{6.1}$$

This motivates investigation of high aspect-ratio pillar-based structures to replace the collapsed solder bump structure (C4) for chip I/O interconnects. In fact, it has been recently revealed that Intel has used Cu pillar bumps in their latest high-end microprocessor products [6.1], as illustrated in Figure 6.1.

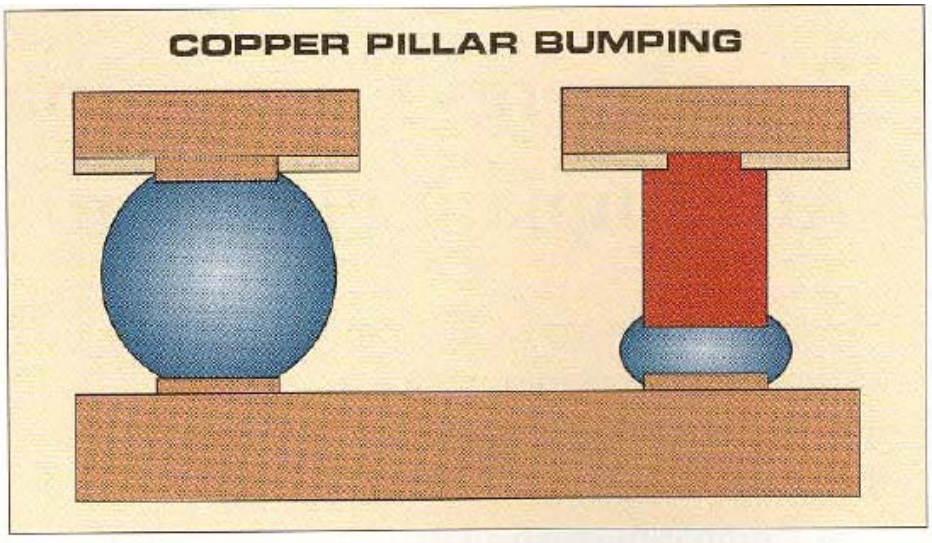


Figure 6.1: Schematic illustration of Cu pillar bumping in comparison with conventional C4 solder bumping [6.1].

The large stand-off height also means that today's underfilling process can continue to be used without additional cost, while the I/O density increases. Another advantage of using the Cu pillar based bumps is their better electromigration performance.

Nevertheless, any I/O interconnection technologies should eventually meet the ITRS projected requirements for chip I/O bandwidth, DC current drain and heat dissipation. According to the ITRS, these requirements will continue to increase [6.2]. As summarized in Table 6.1, the key challenges at the end of the roadmap (18 nm technology node in 2018) include: an I/O frequency of 56.8 GHz, an overall DC current up to 300A, as well as a power density up to 108 W/cm^2 with a junction temperature below 85 °C. In addition, a large number of I/Os (up to 8,450) must be available with "low to zero applied stress" at the chip-board interface to accommodate the mechanically fragile low-k interlevel dielectrics (ILD). Fortunately, "sea of polymer pillars" technology has the potential to enable the fabrication of compatible electrical, optical and thermal-fluidic I/O interconnects at a high integration level [6.3]. The compliant nature of the polymer structures can also simultaneously meet the ITRS requirements of low-stress chip interfacing.

Table 6.1: ITRS projections for 18nm technology node in 2018 [6.2].

	Supply voltage	**DC current drain**	**Chip-to-board I/O frequency**	**Power density**	**Junction temperature**	**# of I/Os**
Low cost	0.6 V	~5 A	150 MHz	3 W/cm^2	125 °C	1576
Cost performance	0.6 V	~250 A	800 MHz	108 W/cm^2	85 °C	5642
High performance	0.6 V	~300 A	56843 MHz	64 W/cm^2	85 °C	8450

In this chapter, fabrication of dual-mode polymer pillar-based I/O interconnects will be first presented. Demonstration of electrical/optical interconnection will then be performed through assembly of transparent test chips on various test substrates. Slab waveguides with waveguide volume grating couplers (WVGC) as well as the multiple waveguides terminated at slanted Si mirrors will be used for the demonstration. Simultaneous fabrication of the air-gaps for both fluidic channels and optical waveguide will also be presented to enable a package substrate with multifunctional interconnection capabilities.

6.2. Fabrication of Dual-mode Polymer Pillar-based I/O Interconnects

As suggested in [6.4, 6.5], dual-mode polymer pillars can provide highly integrated electrical and optical paths to enable a GSI chip with high-bandwidth photonic I/O communication. This motivates a demonstration of the assembly of the dual-mode polymer chip I/O interconnects.

Optically transparent glass (1mm thick) was used to fabricate the chips with dual-mode electrical and optical pillars for the purpose of optical inspection and measurement. As shown in Figure 6.2, fabrication of polymer pillars is a simple batch operation. A thick film of photo-polymer (Avatrel 2195P) is first applied by spin coating. After soft baking, UV exposure through a mask, hard baking and spray developing, the transparent polymer pillars are formed (Figure 6.2a). The polymer pillars are is then cured in a nitrogen-purged oven. To achieve simultaneous electrical and optical interconnection, the next step is metallization since the polymer pillars are not conductive. A stack of thin-film Ti/Cu/Ti (30nm/200nm/30nm) is sputtered to cover the entire surface of the sample as a seed layer for electrical continuity during electroplating (Figure 6.2b). Due to the nature of the DC-sputter, both sidewall and tip of the pillars are coated with a thin film of the metal.

To open the tip of the pillars for optical transmission, a layer of positive photoresist (Shipley 1827) is spun to cover the polymer pillars (Figure 6.2c) and the tip is exposed after patterning with the same mask for the pillars. After a short RIE descum, the metal film on the tip of the pillars is etched (Figure 6.2d). After the photoresist is stripped (Figure 6.2e), on-chip pads are patterned by another photolithographic step (Figure 6.2f). Metal coating is then electroplated in the area patterned for the pads (Figure 6.2g). Since the pad area is larger than the pillar area, the polymer pillars are coated while the metal pads are formed around the polymer pillars. Finally, after the photoresist is stripped and the seed layer is etched, the transparent wafer with metal pads and dual-mode polymer pillars is completed and ready for dicing (Figure 6.2h).

The main challenge in the fabrication processes is the conformal coating of the photoresist on the wafer surface with the high-aspect ratio polymer pillars. Experiments indicate that a spreading step should be performed at low spin speed for a short time before the desired spin step begins. After dicing, transparent chips were obtained and ready for assembly and testing. SEM photographs of the completed dual-mode polymer pillars with various aspect ratios at an area-array pitch of 325 μm are shown in Figure 6.3-Figure 6.5.

Various combinations of metal coating can be applied. In some cases, a nickel or Cu film is first coated to serve as a wetting base and an Au film is then deposited to prevent oxidation. In other cases, a thin layer of Ni is finished with a thick solder film, which can improve wetting during the assembly.

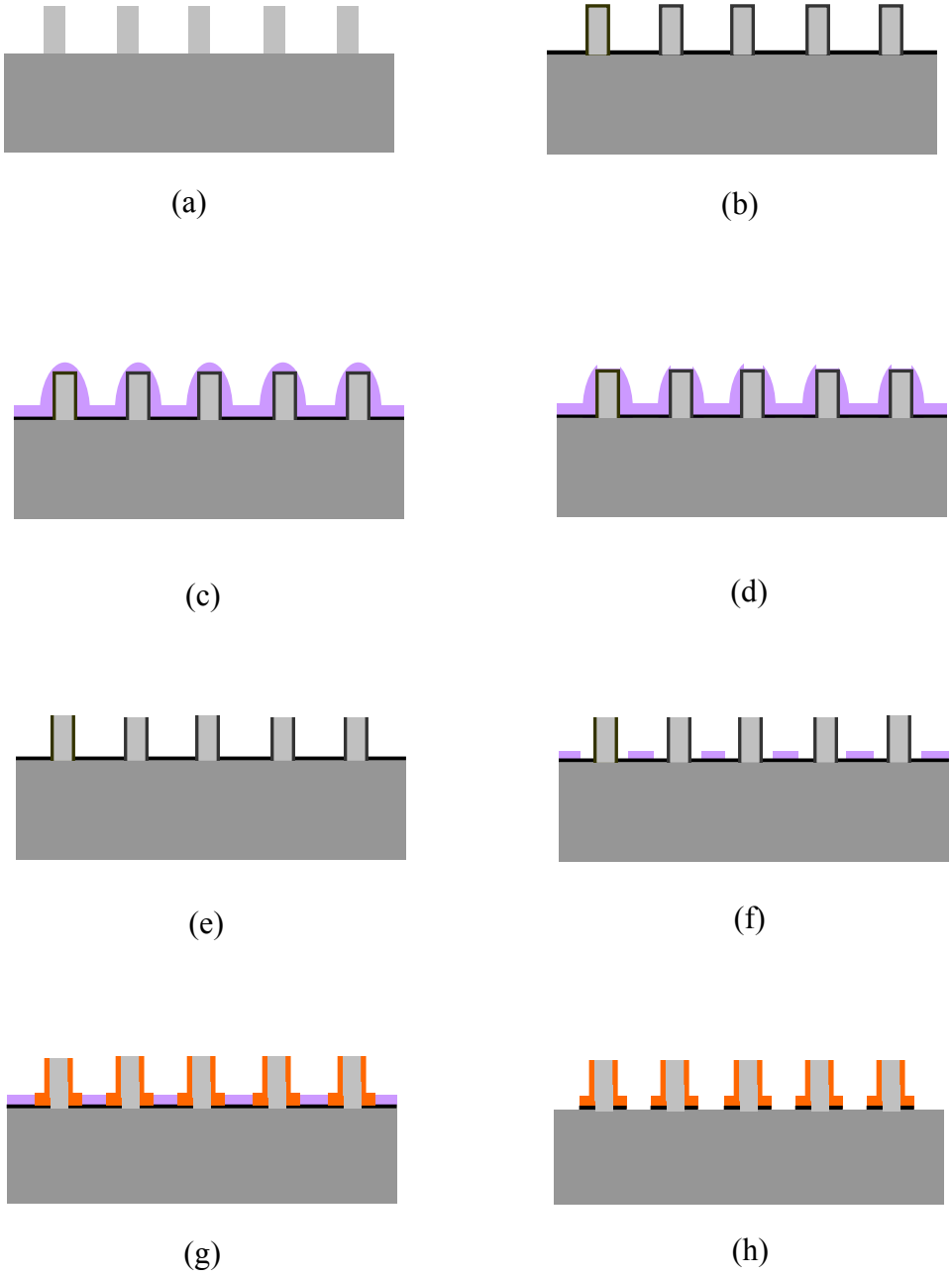
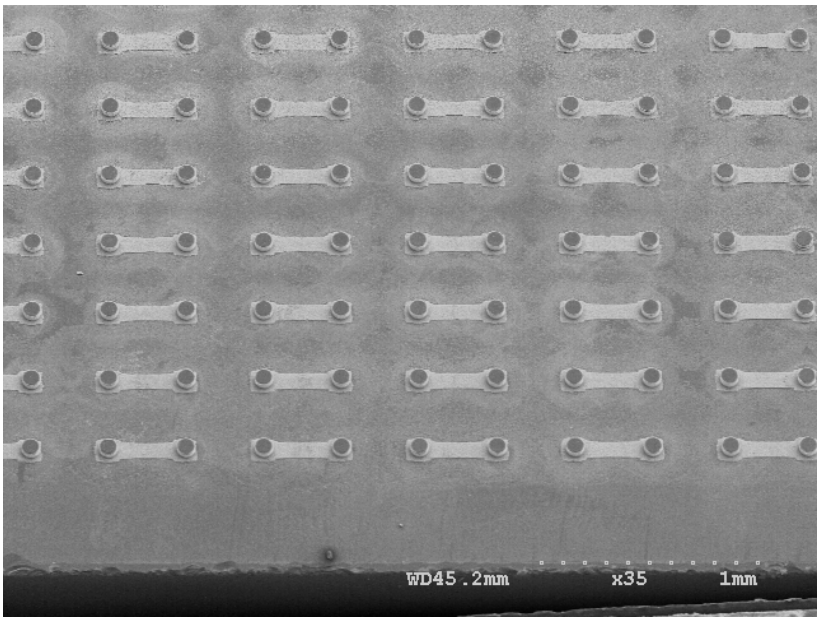
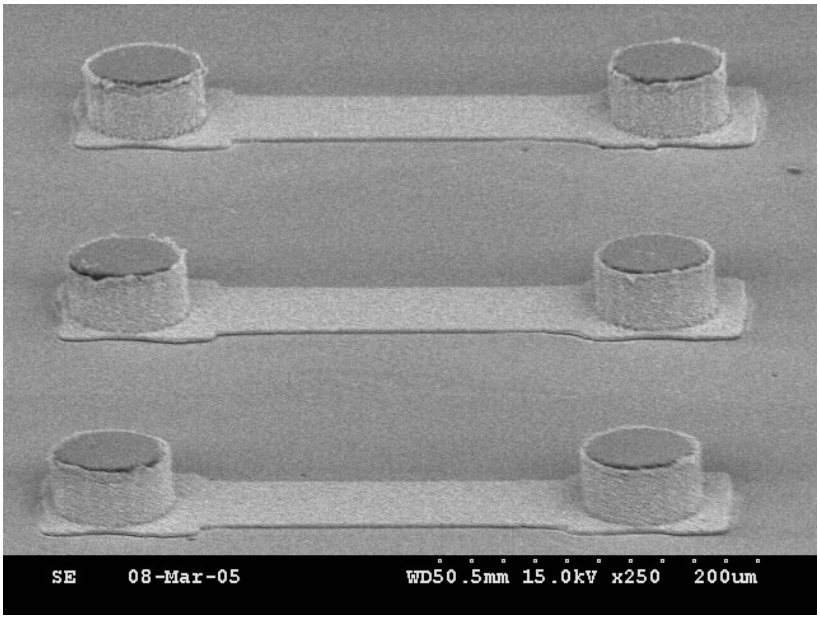


Figure 6.2: Schematic of the fabrication process of the dual-mode polymer pillars on the on-chip metal pads. (A total of three masking steps are required)

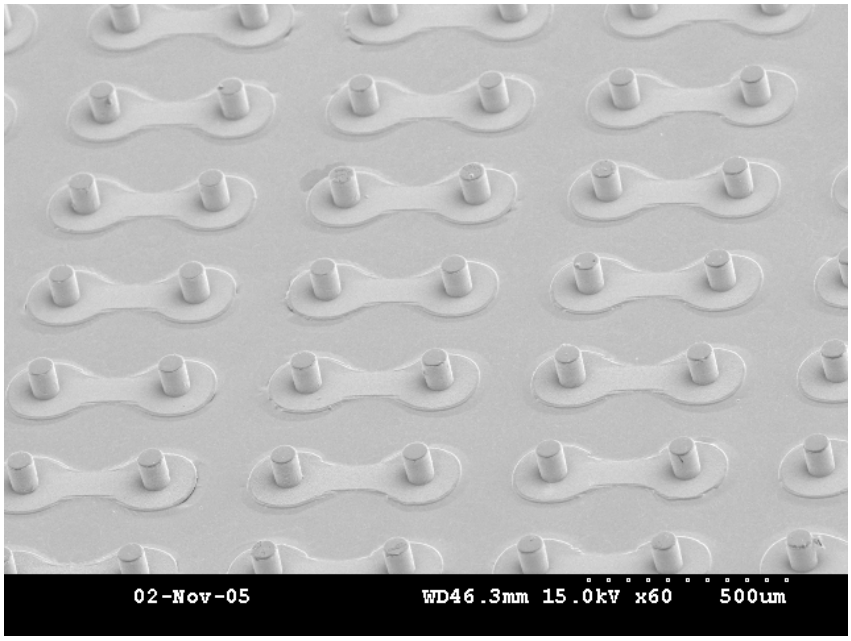


(a) overview

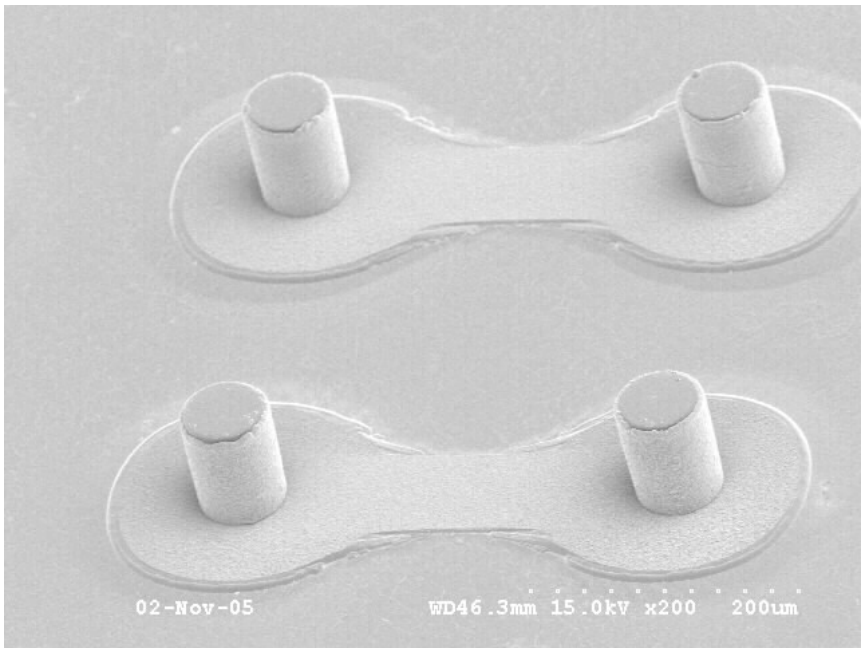


(b) perspective side-viewing

Figure 6.3: SEM micrographs of dual-mode polymer pillars with Ni/Au coating with low aspect ratio: Diameter = 55µm; Height = 65µm.

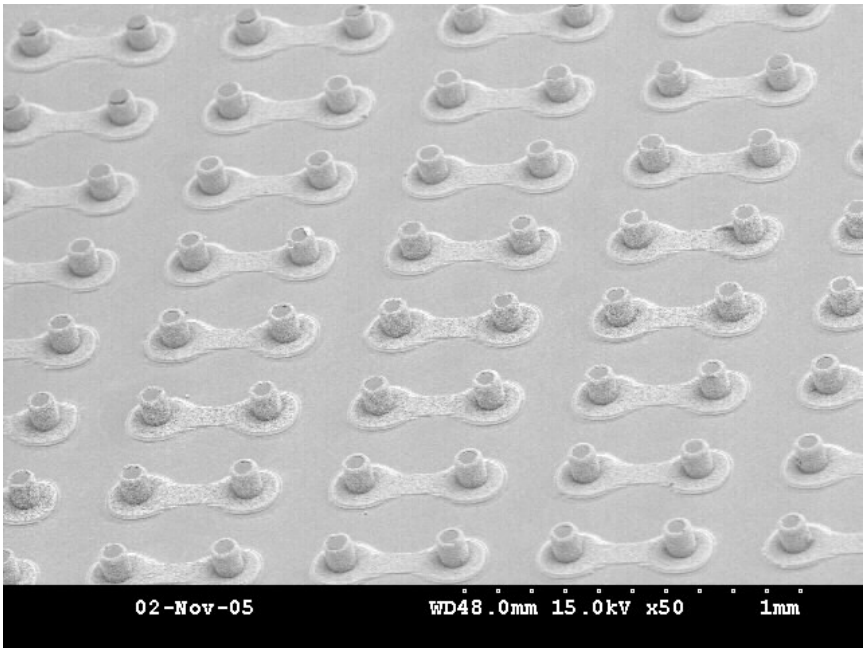


(a) overview

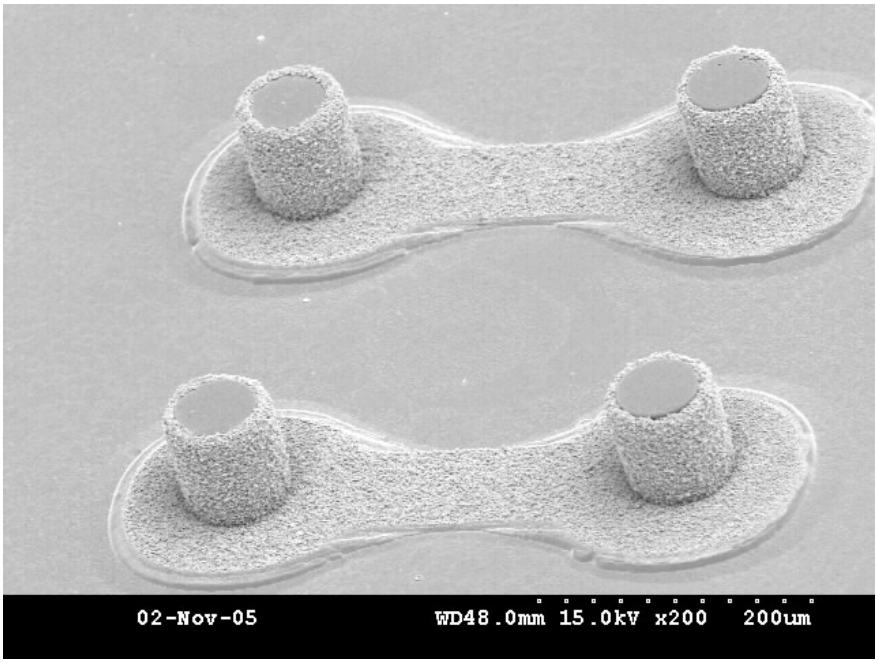


(b) perspective side-viewing

Figure 6.4: SEM micrographs of dual-mode polymer pillars with Ni/Au coating at high aspect ratio: Diameter = 55μm; Height = 110μm.



(a) overview



(b) perspective side-viewing

Figure 6.5: SEM micrographs of the dual-mode polymer pillars with Ni/Solder coating at high aspect ratio: Diameter = 55μm; Height = 110μm.

6.3. Electrical Resistance and Current Carrying Capability of Dual-mode Polymer Pillar I/Os

As illustrated in Figure 6.6, the DC electrical resistance and the current carrying capability of an I/O interconnect depends on its conducting cross-sectional area. For a solid metal pillar, the cross-sectional area is mainly determined by its diameter. Its DC resistance can be calculated simply using:

$$R_{dc} = \rho \frac{L}{A_{cross}} = 4\rho \frac{H}{\pi D^2} \qquad 6.1$$

where ρ (Ω-m) is the resistivity, H (m) and D (m) are the height and diameter of a pillar. In contrast, the conducting cross-sectional area of a dual-mode polymer pillar also depends on its cladding thickness, t (m). Its DC resistance can be estimated using:

$$R_{dc} = \rho \frac{L}{A_{cross}} = \rho \frac{H}{\pi(Dt + t^2)} \qquad 6.2$$

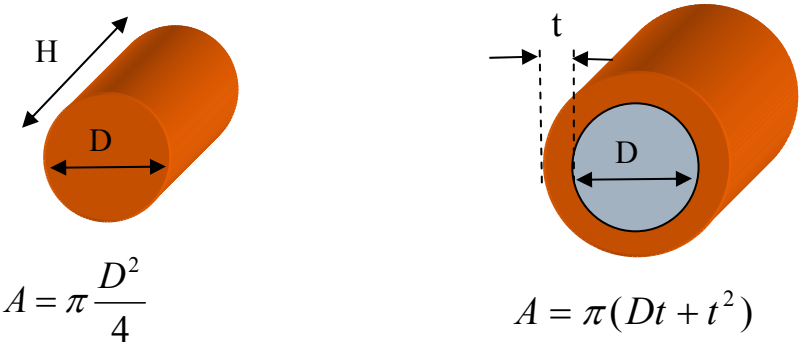


Figure 6.6: Illustration of the difference in the conducting area between a solid metallic pillar (or bump) and a dual-mode polymer pillar.

According to the ITRS projections for 2018, the area array I/O pitch will be reduced to 70 μm. Assuming Cu as the metal for an I/O interconnect with a diameter of 35 μm approximately, the calculated DC resistance of a dual-mode polymer pillar is plotted as a function of the metal

cladding thickness in Figure 6.7. For comparison, the DC resistance of a solid metal pillar with a diameter of 35 μm is also calculated and plotted.

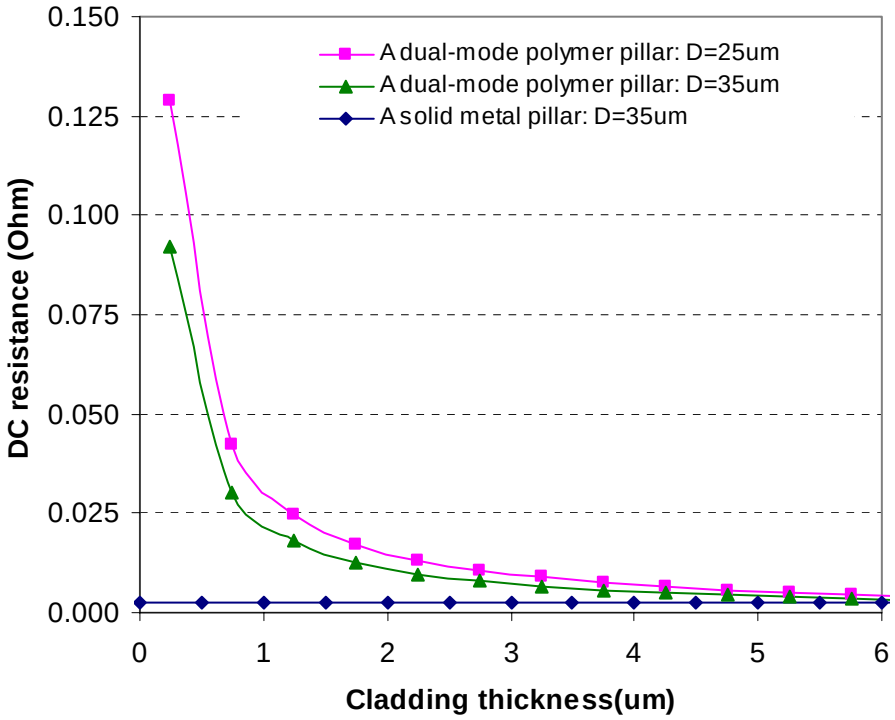


Figure 6.7: Calculated DC resistance as a function of the thickness of the Cu cladding for a dual-mode polymer pillar in comparison with a solid Cu pillar for an I/O pitch of 70 μm in 2018. The height of the pillars is assumed to be 100 μm.

As expected, the calculated DC resistance of a dual-mode polymer pillar is usually larger than that of a solid metal pillar with a comparable diameter. However, the resistance of a dual-mode polymer pillar rapidly decreases as its cladding thickness increases. When its cladding thickness is increased from 0.5 μm to 5 μm, the resistance of a dual-mode polymer pillar is reduced from 63.7 mΩ to 5.41 mΩ (a reduction of 91%) and reaches a low level comparable to that of a solid metal pillar. This is critical because a thin metal cladding thickness means a larger mechanical compliance.

In addition, the total DC supply current of a high-performance chip is projected to be more than 300 A in 2018, which is distributed across approximately 3000 power/ground I/Os [6.2]. Thus, the current through each I/O may be as much as 200 mA and electromigration becomes another concern due to the large current density. The current density of an I/O interconnect can be calculated based on its conducting cross-sectional area. Figure 6.8 shows the calculated current density for three cases, which include the 35 μm polymer pillars with 5 μm metal cladding, the 35 μm solid metal pillars, and the 25 μm polymer pillars with 10 μm metal cladding.

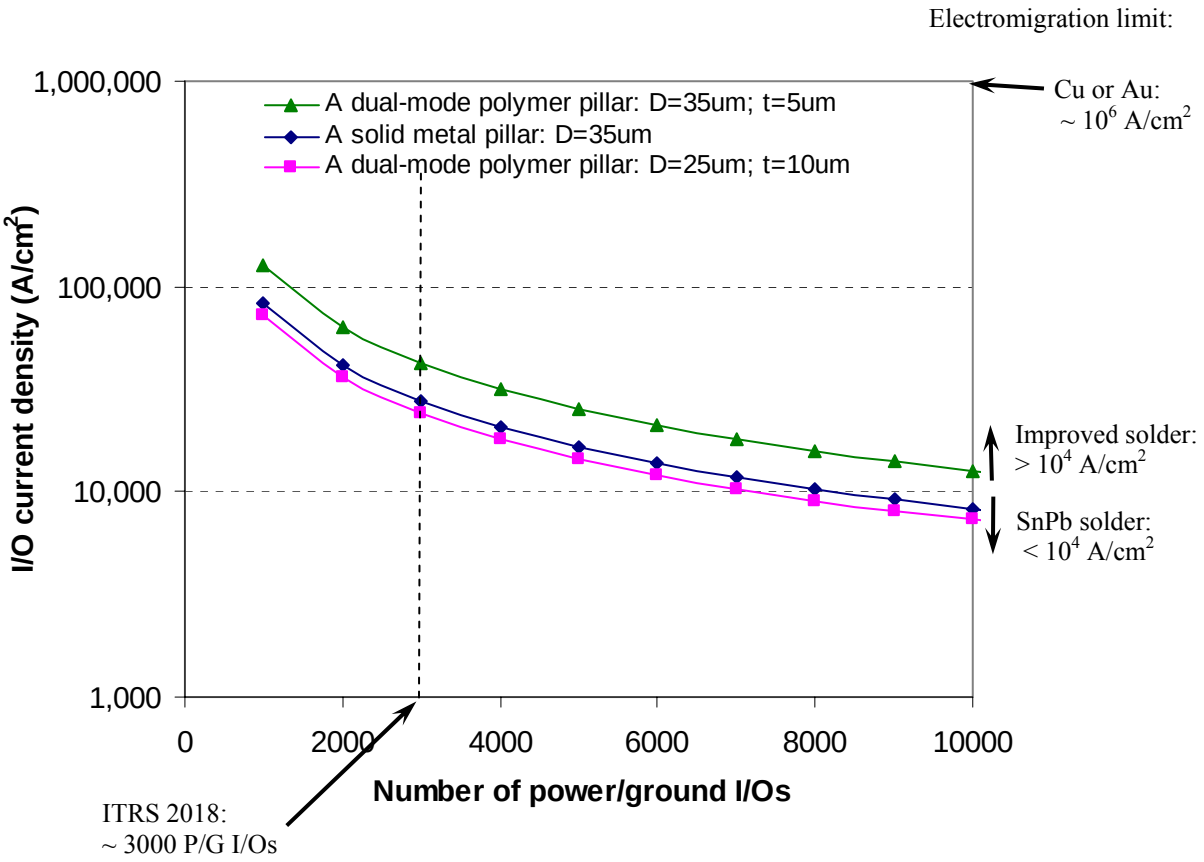
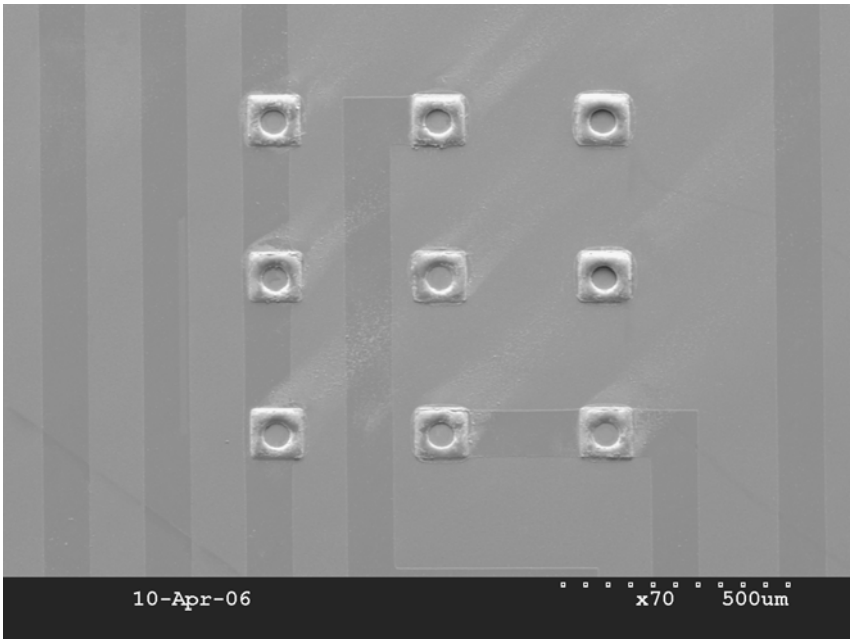


Figure 6.8: Calculated I/O current density a function of the power/ground I/O number for various cases: (a) 35 μm polymer pillar with 5 μm metal cladding (b) 35 μm metal pillar/bump (c) 25 μm polymer pillar with 10 μm metal cladding.

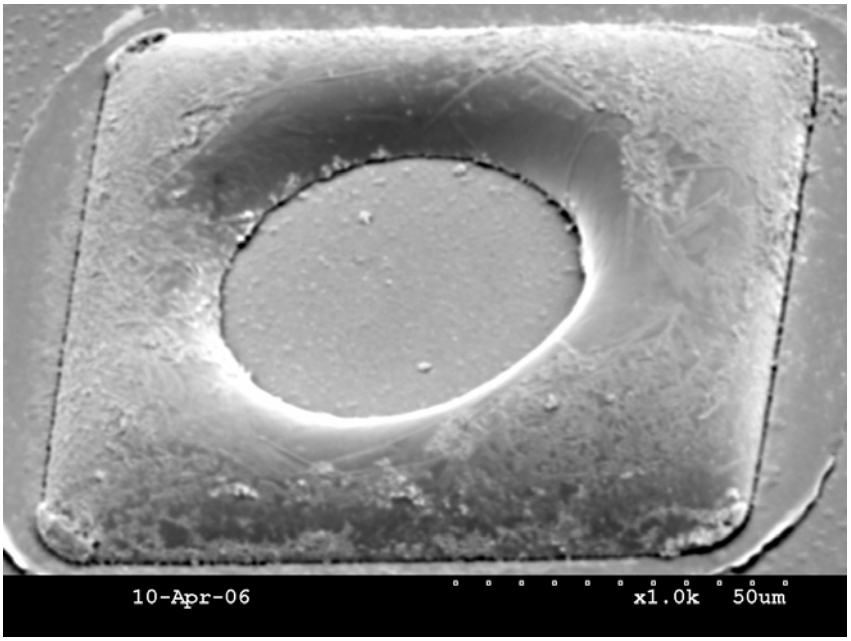
It is shown that even for solid metal pillars, I/O current density still exceeds the physical limit for conventional SnPb solder based on the ITRS projected number of power/ground I/Os. This has been identified as one of the major challenges for future high performance IC packages in the road map [6.2]. While the current density may be reduced by adding more power/ground I/Os, this issue can also be resolved by using different materials. For example, the generally accepted electromigration limit for Cu or Au is 10^6 A/cm^2 [6.6], compared with 10^4 A/cm^2 for conventional eutectic SnPb solder [6.7], which suggests that the I/O current density for all three cases is well below the physical limit for Cu or Au. Thus, a potential solution is to use Cu based I/O interconnects such as solid Cu pillars or polymer pillars with Cu cladding. In fact, as mentioned previously, the Cu based I/O interconnects are already being considered by the major semiconductor manufacturers such as Intel [6.1]. In addition, Pb-free solders have shown better electromigration performance than conventional eutectic SnPb due to the higher melting temperures [6.8, 6.9].

6.4. Assembly of Dual-mode Electrical/Optical Polymer Pillars

To accommodate the metal cladded electrical/optical polymer pillars, solder based pads (or sockets) have been designed and fabricated, as shown in Figure 6.9. The solder pads were fabricated at the desired areas by electroplating through photolithography. After reflow with the aid of a liquid flux, the solder pad rounds up because of the surface tension of the molten solder and a via is formed at the center of each pad. The unique shape of the solder pads resembles a funnel opening and can accommodate misalignment to a certain extent.



(a) overview



(b) perspective view

Figure 6.9: SEM micrographs of "funnel" like solder pads (or sockets) to accommodate the metal cladded polymer pillars.

Figure 6.10 illustrates the assembly of the dual-mode polymer pillars. A precision flip-chip bonder with an alignment accuracy of 1.5 μm was used for bonding. The temperature and force were controlled during the bonding as follows: the chip and board were brought into contact before elevating the temperature to the solder melting temperature (180˚C). Under compression, the chip and board were heated to the reflow temperature (220˚C). After 30 seconds at the peak temperature, the samples were cooled down. Figure 6.11 is an optical micrograph of an assembled glass die with dual-mode pillars on a transparent glass substrate.

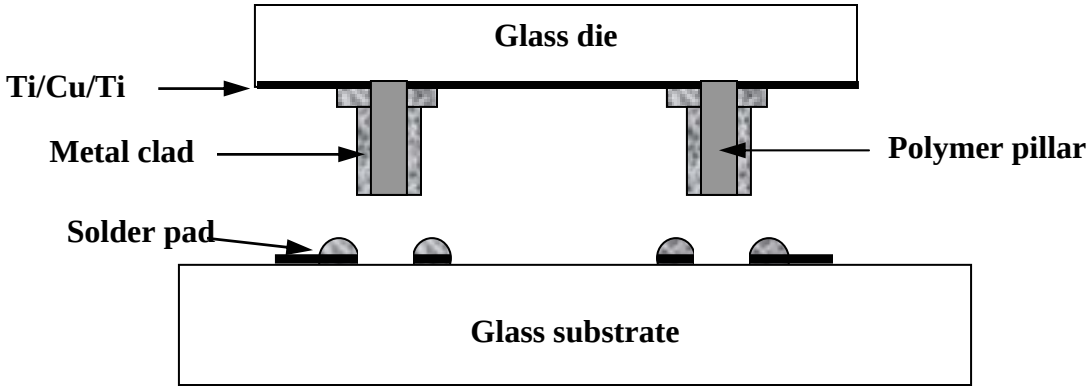


Figure 6.10: Schematic illustration of the assembly of metal cladded dual-mode polymer pillars

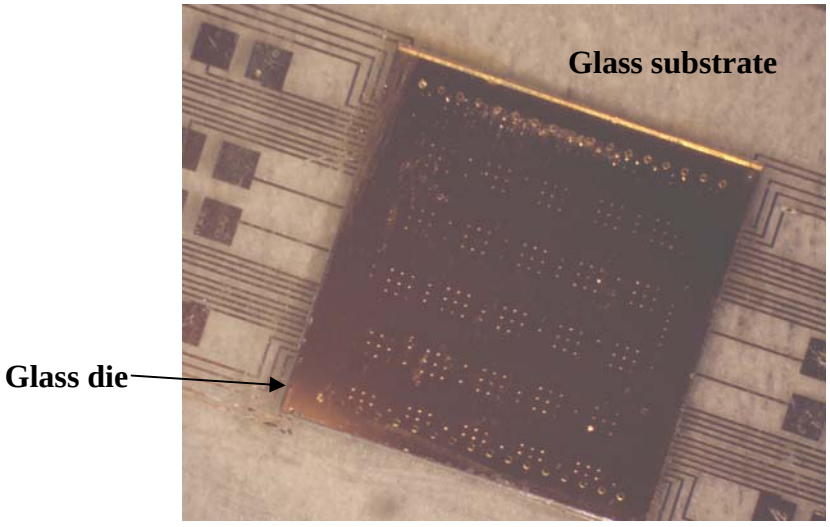


Figure 6.11: Optical micrograph of a glass die with dual-mode polymer pillars bonded onto a transparent glass substrate.

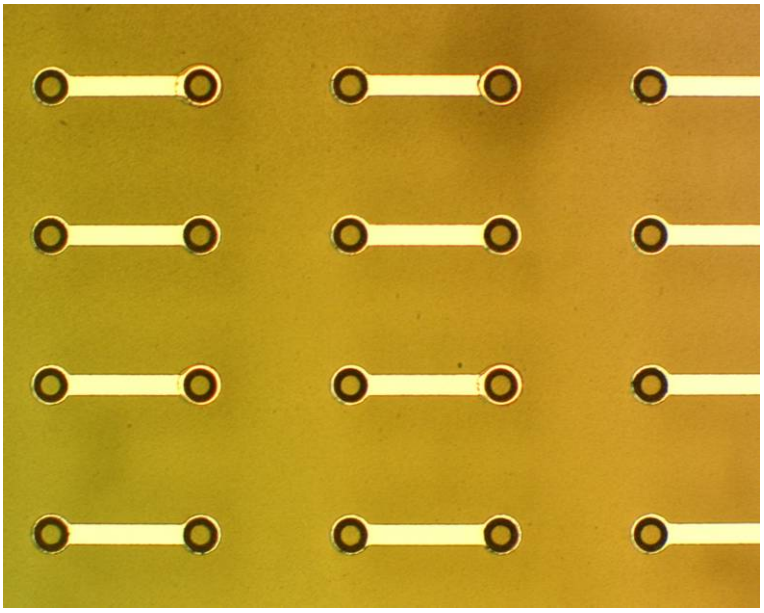
The seed layer (Ti/Cu/Ti) was intentionally left on the glass die so that light can only be transmitted and detected through the dual-mode polymer pillars. This can be used as a simple inspection method for the alignment between a pillar and a solder pad, by which the success of optical transmission through the transparent glass substrate, vias in the solder pads, polymer pillar, and the transparent glass die, was confirmed. Meanwhile, using the Cu lines and pads on the glass substrate (same test layout as described in Chapter 5), electrical continuity was also successfully tested for multiple pairs of pillars that are shorted with the seed layer on the die. Average measured resistance across a pair of dual-mode polymer pillars was less than 0.1 Ω, translating into a low resistance less than 0.05 Ω per pillar.

6.5. Demonstration of Electrical/Optical Interconnection using Waveguide Volume Grating Coupler

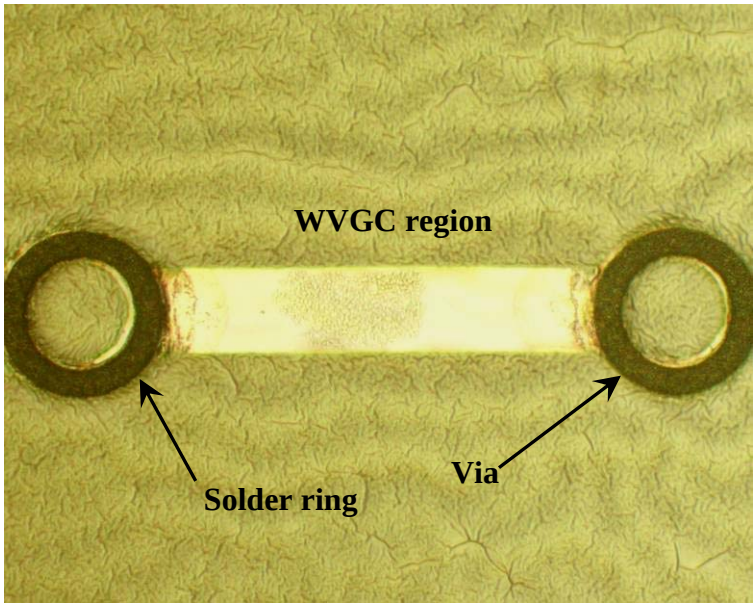
To demonstrate the simultaneous electrical/optical interconnections, a transparent glass die with dual-mode polymer pillars needs to be assembled onto a substrate that can deliver an optical signal. A waveguide volume grating coupler (WVGC) embedded in a slab polymer waveguide was fabricated on a Si substrate using the process described in [6.10, 6.11]. As shown in Figure 6.12, Cu pads (1 μm thick) were then fabricated by electroplating above the waveguide volume grating couplers. At the center of each Cu pad, a via was opened for optical transmission, which is equal in diameter to that of the polymer pillars. A 10~15 μm thick layer of solder (60/40 SnPb) was electroplated on the perimeter of the optical vias in the Cu pads. The resulting solder resembled a ring-pattern. A 0.2 μm thick layer of silicon dioxide was used around the solder as a non-wetting material.

Using the assembly process described in the previous section, a transparent glass chip has been assembled onto the Si test substrate with WVGC. Figure 6.13a illustrates the schematic of

the side view of the test structure, and Figure 6.13b shows an optical micrograph of an assembled glass die on the test substrate.

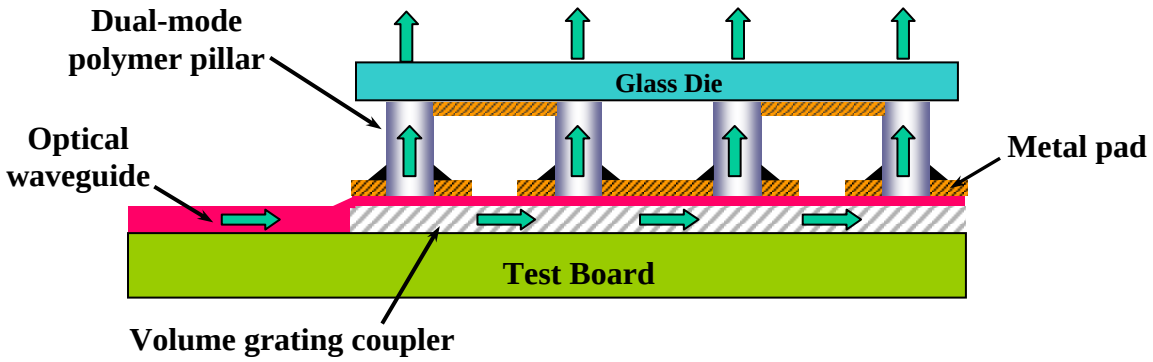


(a) overview

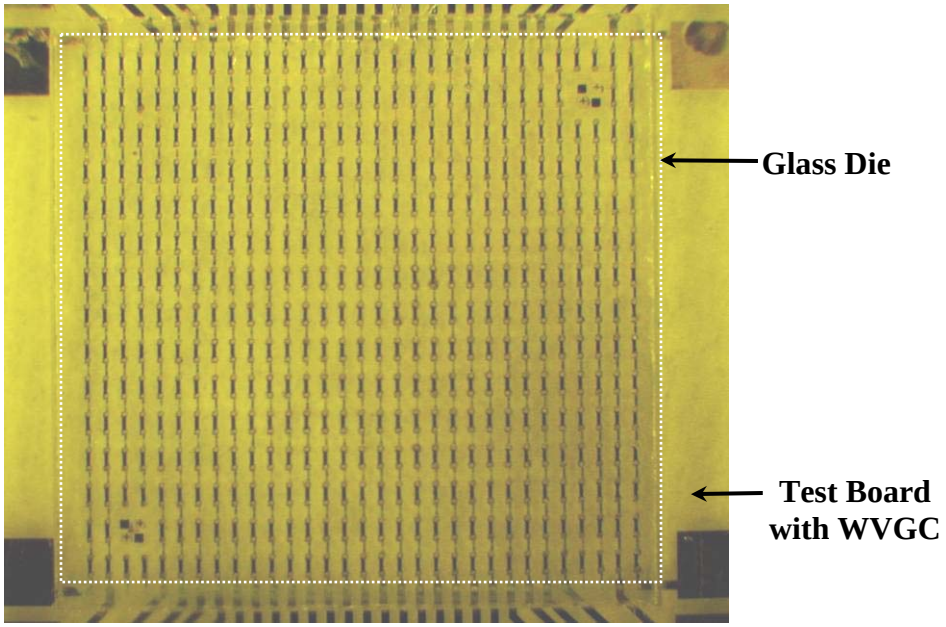


(b) perspective view

Figure 6.12: Optical micrographs of the metal interconnects over waveguide volume grating coupler (WVGC) region on the test board, which are terminated with open vias and solder ring.



(a)



(b)

Figure 6.13: Illustration of the assembly of a transparent chip with dual-mode polymer pillars on a test board with a waveguide volume grating coupler. (a) Schematic of flip-chip assembly (b) Optical micrograph of a test chip bonded onto a Si test board

Good alignment between the chip and the board was visible after the assembly. The optical transmission was then measured by coupling light (λ = 635 nm) from a single mode fiber into the board-level planar waveguide. After the planar waveguide was excited, power from the resulting waveguide mode was then diffracted by the WVGC into the pillars. The output optical signal can then be observed from the back side of the transparent die. To illustrate the transmission of out-coupled light through the pillars, unsaturated images of the surface of the board were taken. The average bit levels along two 24 μm-wide regions of the WVGC before, at, and after a polymer pillar were extracted. Before and after the polymer pillar, the expected exponential decay curves were observed. The intensity profile and exponential fits are shown in Figure 6.14. Transmission through the polymer pillars changes the output profile of the beam. The coupling efficiency (CE) through the pillars was qualitatively estimated as follows: an exponential fit to the decay profile in the region before the polymer pillar was made, and the area under the measured output profile at the pillar region (which is proportional to the output power) was compared with the area under the curve predicted using the exponential fit. With the exponential decay factor α = 2.56 mm^{-1} and the calculated preferential order coupling factor η=0.976, the expected CE for the grating without the pillar is 25.8% according to the following equation [6.10, 6.12]:

$$CE = \eta(1-e^{-2\alpha L}) \qquad 6.3$$

where L is the diameter of the pillar (60μm). The intensity profile at the area under the pillars was around 8% higher than that of the area without pillars. Therefore, the estimated CE through the polymer pillar is approximately 27.9%, which is somewhat low mainly because the WGVC in the present sample has not been optimized for individual polymer pillars.

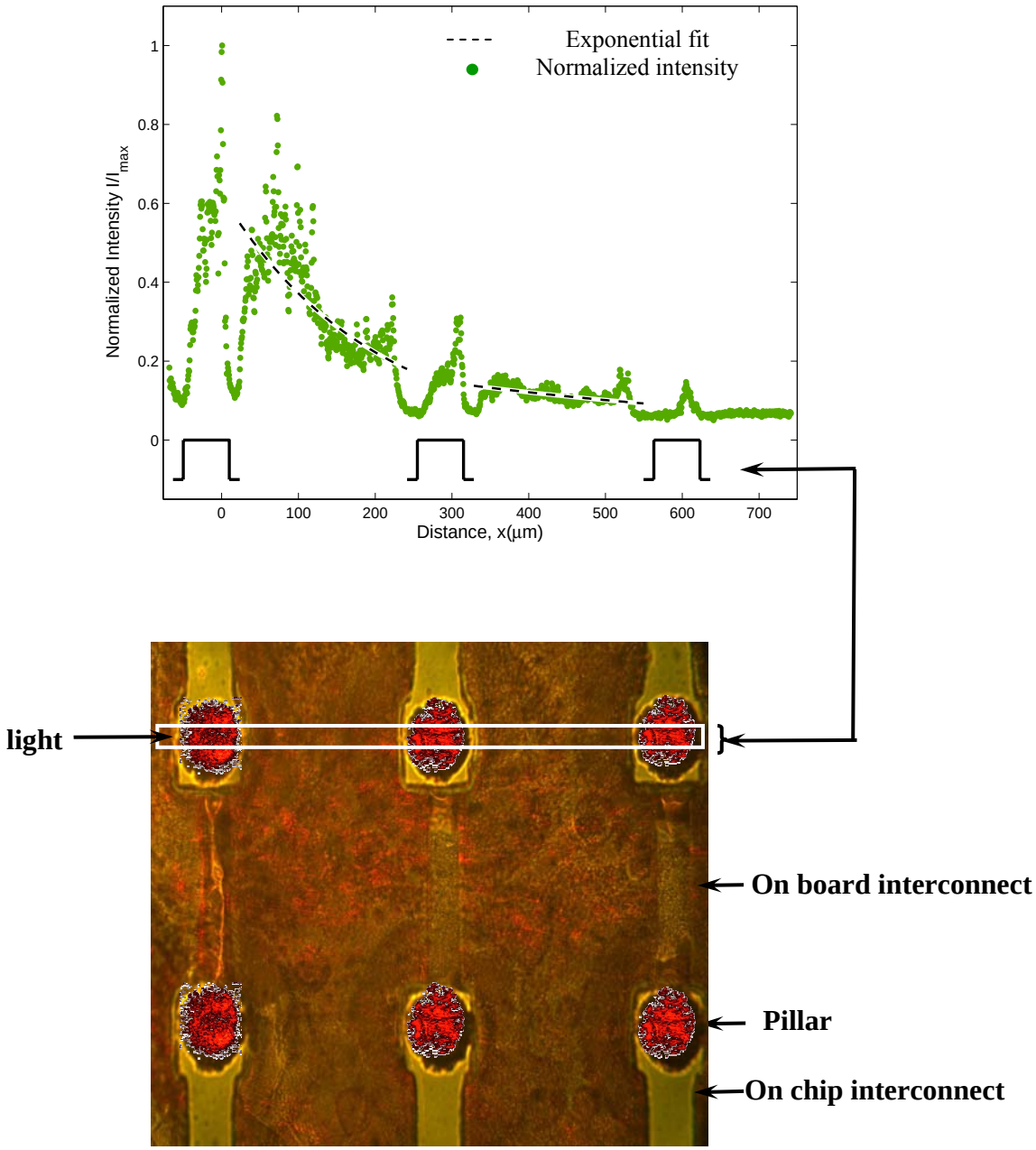


Figure 6.14: The intensity profile measured for the WVGC superimposed with the exponential fit of the theoretical decay curve across the region before and after the polymer pillars.

Electrical continuity through the daisy chain was achieved and the measured overall resistance of a chain of 31 cascaded dual-mode pillars is around ~ 10 Ω, which translates into the resistance of ~0.32 Ω for each pillar. This is relatively high compared to the result obtained using different test layout in the previous experiment. A reason for this might be the design of the solder ring in this experiment. As shown in Figure 6.15, the wetting area is relatively small and the electrical/mechanical joining between a pillar with an on-board pad may be poor.

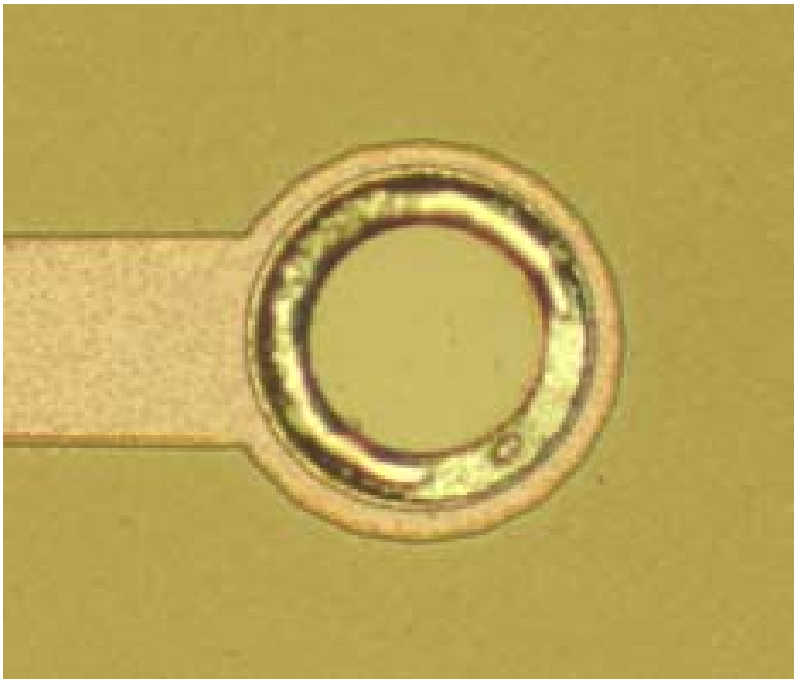


Figure 6.15: Micrograph of a reflowed solder ring that has relatively small wetting area.

To improve the soldering, a new electrical/optical pad was designed and fabricated, as shown in Figure 6.16. Under the new design, a much large amount of solder is available for each dual-mode pillar during the assembly and better electrical joining can be expected. Meanwhile, the "funnel" shape opening is still formed after the solder pads are reflowed.

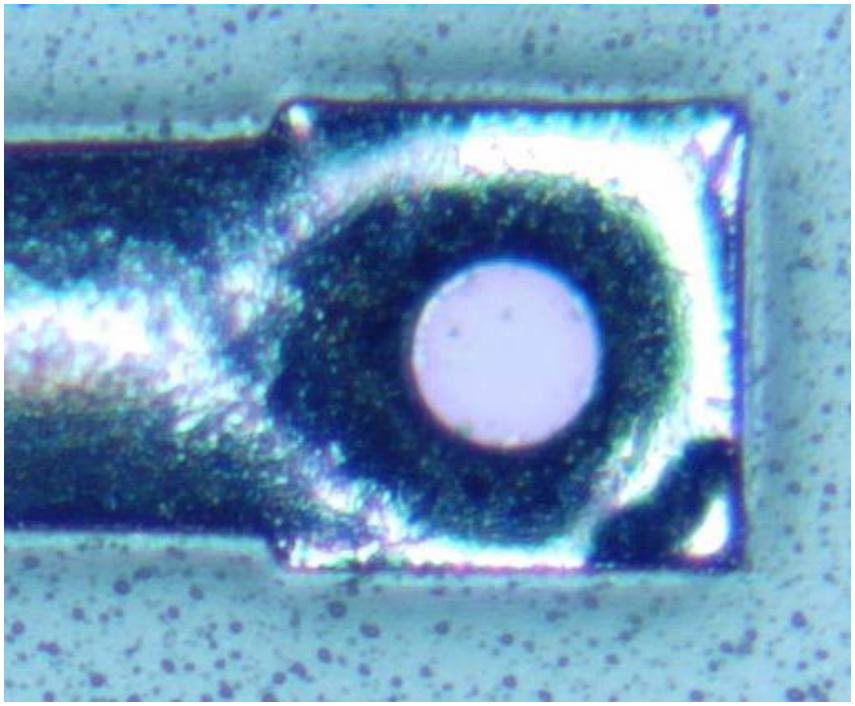


Figure 6.16: Micrograph of a reflowed solder pad with an optical via using the improved design. A "funnel" shape via is formed due to the surface tension of molten solder during the reflow.

6.6. Demonstration of Optical Interconnection through Slanted Si Mirror

In addition to WGVC, other types of couplers such as slanted mirror [6.13, 6.14] may be used on the board substrate. In this work, another demonstration of optical interconnection was performed using slanted Si mirrors. As illustrated in Figure 6.17, electrical/optical solder pads have been fabricated above the waveguides terminated with slanted mirrors to accommodate the dual-mode polymer pillars. For the purpose of simplicity, slanted mirrors of 54.7° were fabricated on a Si substrate by anisotropic wet etching [6.13]. Compared to the above demonstration using slab waveguide with WVGC, where the grating was everywhere, the slanted

mirror can be easily implemented for multiple individual polymer waveguides. In this work, a low-loss optical polymer, SU-8 was used to fabricate the optical waveguides (n ~ 1.5998) and Avatrel 2195P was used as the cladding material (n ~ 1.52). The width and thickness of the waveguides were 40 μm and ~ 20 μm, respectively. The thickness of the Avatrel cladding was ~ 45 μm.

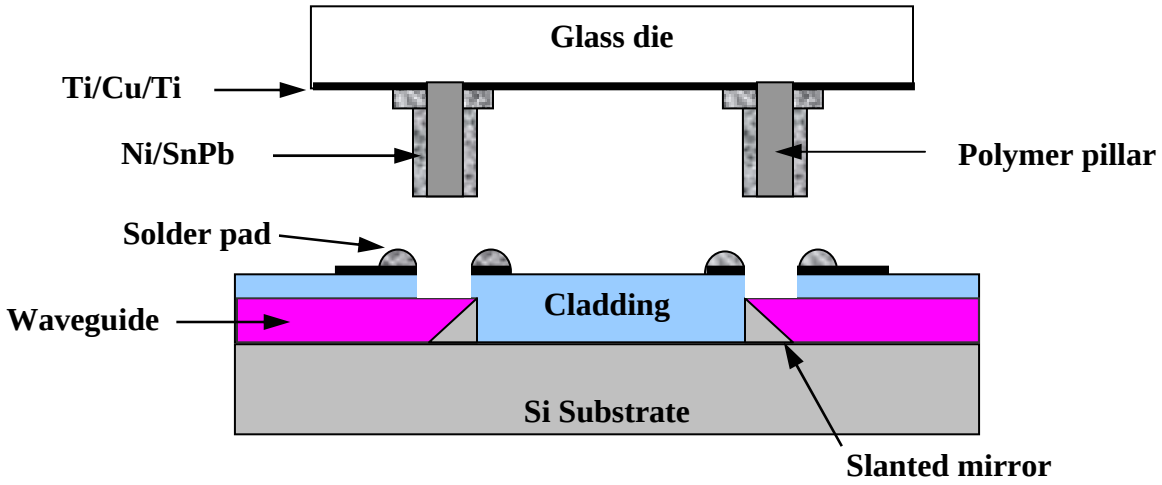


Figure 6.17: Schematic of simultaneous electrical/optical interconnection with waveguides terminated with solder pads and slanted mirrors.

Figure 6.18 shows the top view of encapsulated waveguides terminated at slanted Si mirrors. A layer of Au (~ 2000 Å) was selectively deposited only in the mirror region through DC sputtering to improve its reflectivity before the fabrication of the SU-8 waveguides. Optical vias were opened through the Avatrel cladding simply by UV exposure. Optical micrographs with magnified views have been taken for the top of the via opening and the mirrors inside the via. The sample was then cured at 160 °C in a nitrogen-purged oven.

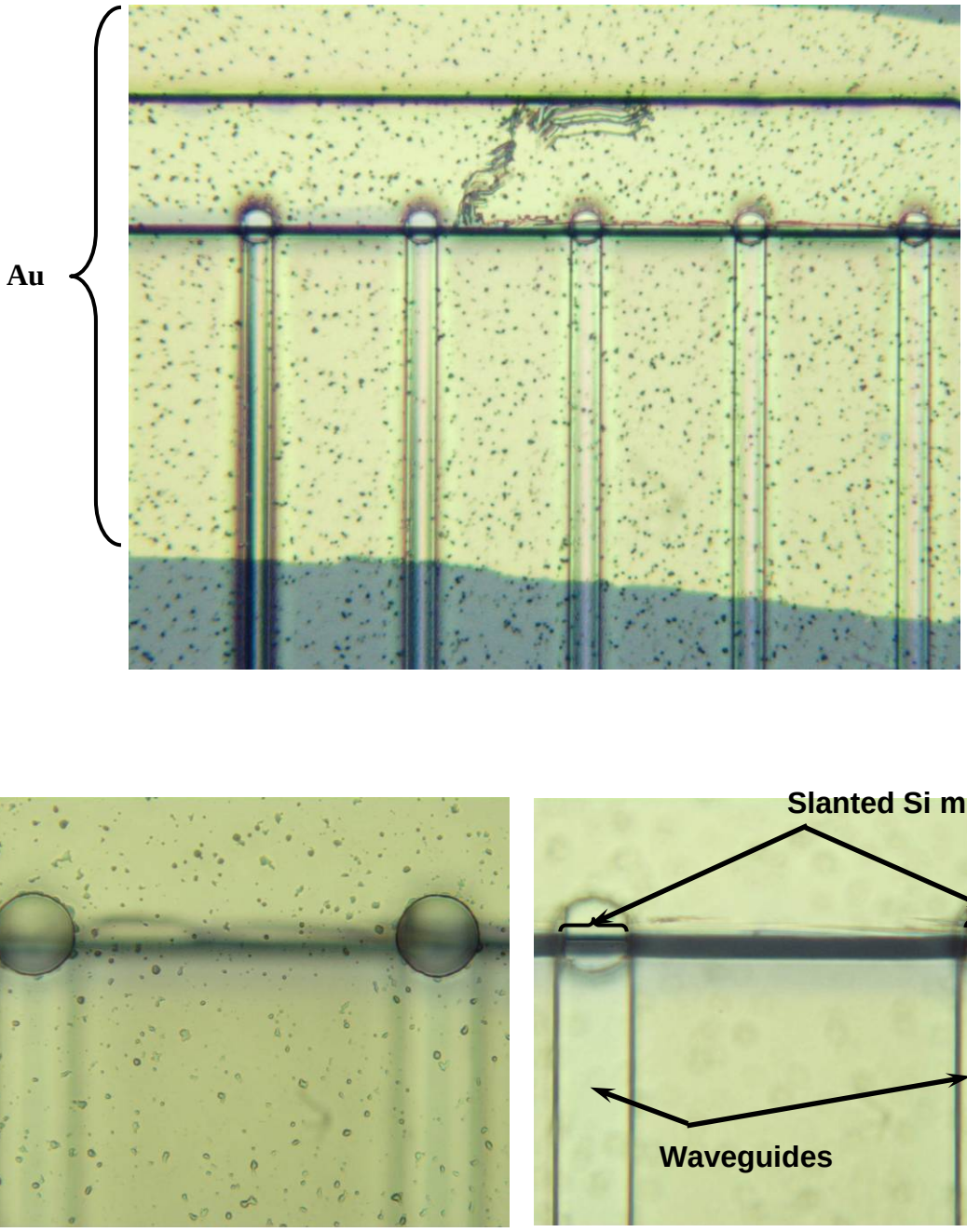


Figure 6.18: Optical micrographs of the encapsulated waveguide terminated at the slanted mirrors that are aligned with optical vias, which are used to accommodate the polymer pillars.

Metal lines and solder pads were then fabricated above the polymer cladding through electroplating, same as describe in the previous section. Figure 6.19 shows the micrograph of a solder pad aligned with an optical via. A perspective view has been shown for the top of a solder pad and the Si mirror inside a via.

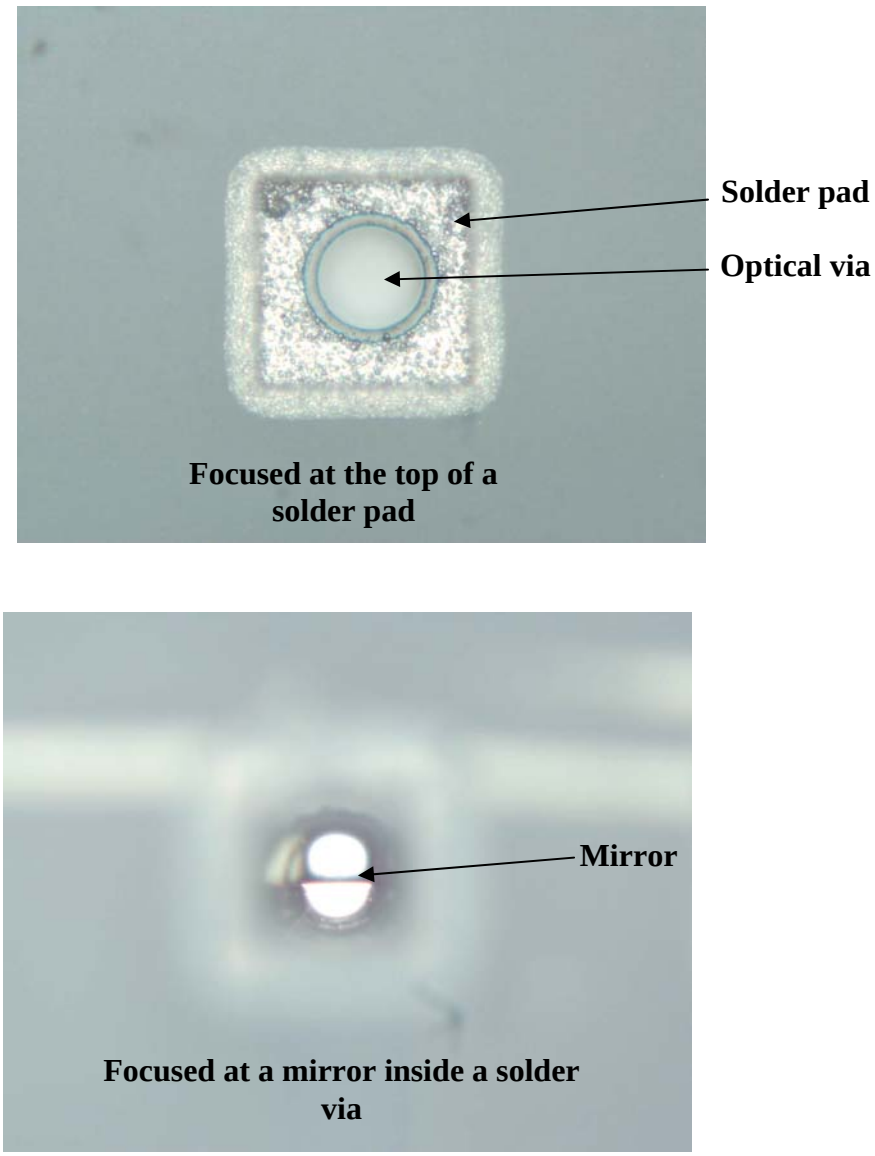


Figure 6.19: Optical micrographs of the fabricated solder pads at the top of an optical via and aligned with SU-8 optical waveguide terminated at a slanted Si mirror.

To check the optical transmission of the waveguide and the coupling of the slanted mirror, a single mode optical fiber was used to couple the light into a waveguide and the reflected light was successfully detected through the via opening at the top of the mirror (The light was of free space wavelength, $\lambda = 635$ nm).

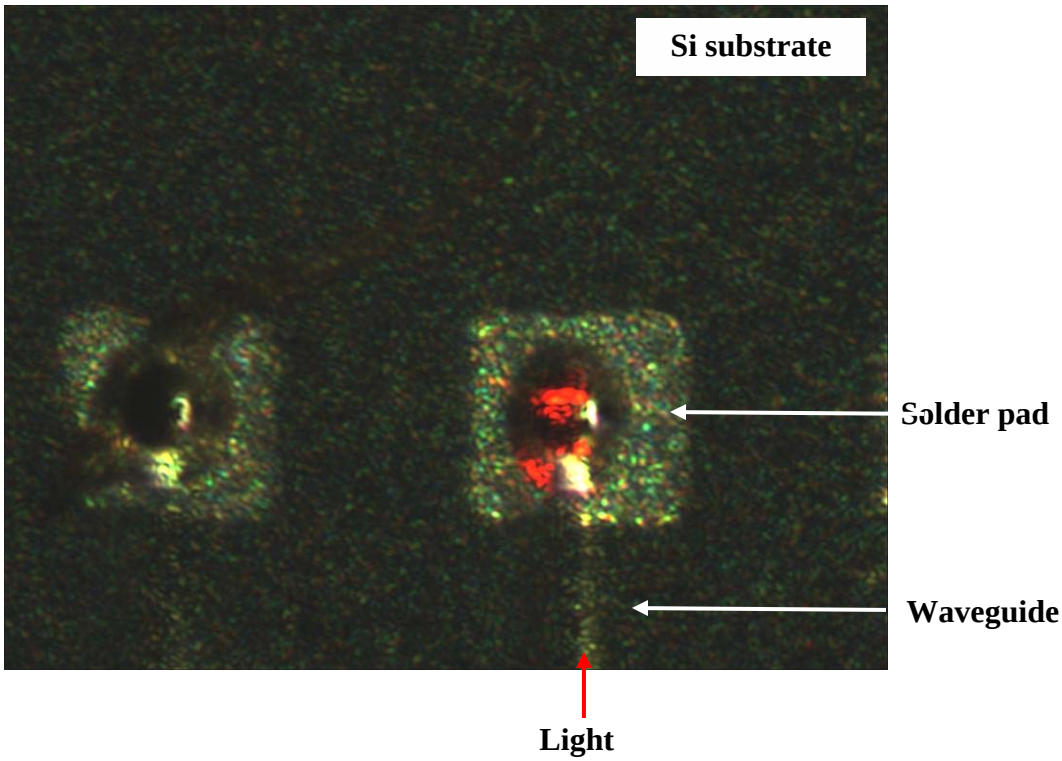


Figure 6.20: Optical micrographs of the optical vias after a waveguide was excited using a laser. Light was directed by the slanted Si mirror.

Using the similar bonding process as described in Section 6.5, transparent glass chips with dual-mode polymer pillars have been assembled onto the test substrates. To qualitatively check the optical coupling from the waveguides to the polymer pillars, multiple waveguides have been tested and the output light was successfully detected from the back side of the chip, as illustrated in Figure 6.21a - Figure 6.21d.

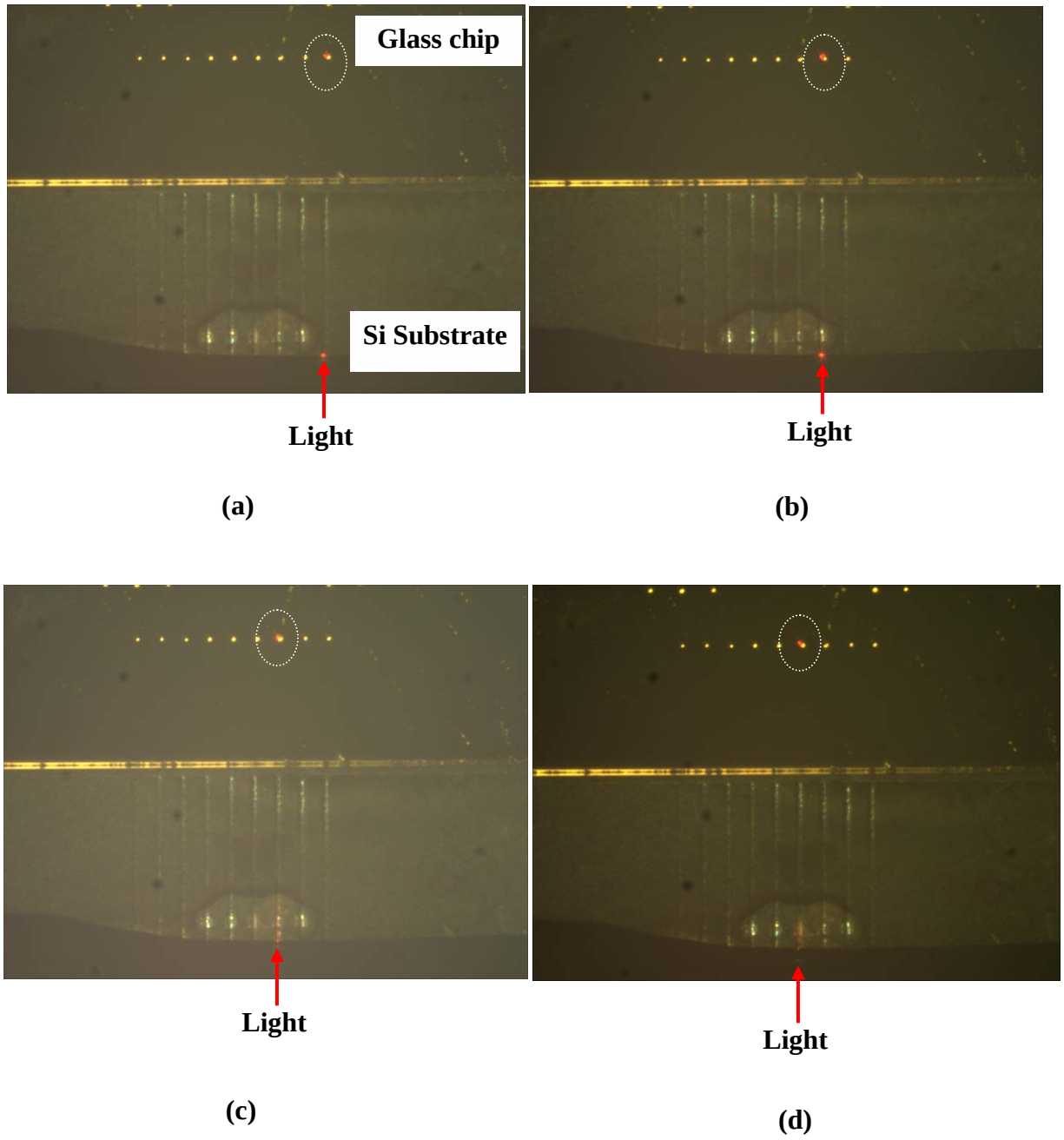
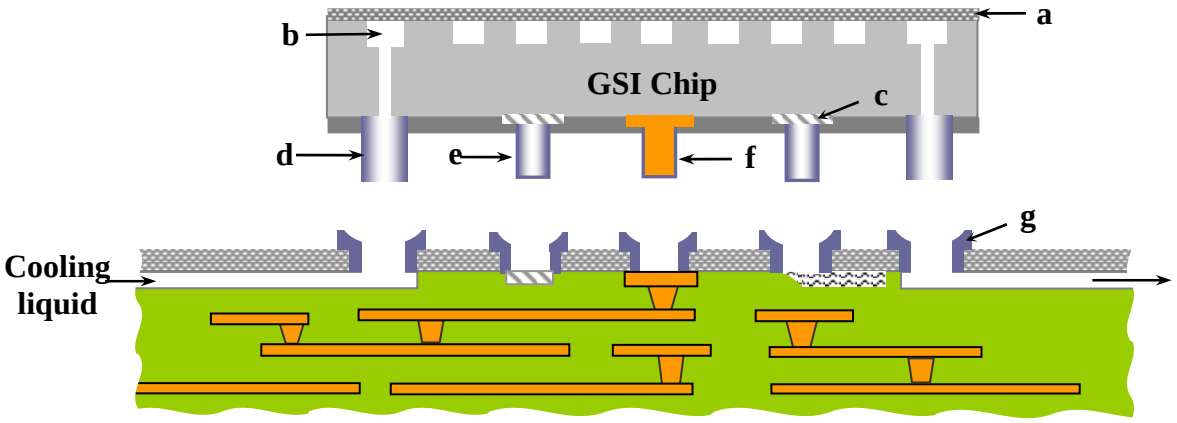


Figure 6.21: Optical micrographs of the bonded glass die on the waveguide substrate after a waveguide was excited using a laser. Light was directed by the slanted Si mirror into the polymer pillars and detected at the back side of the die. From (a) to (d), multiple waveguides have been tested.

6.7. Compatible Electrical, Optical and Thermal-fluidic I/O Interconnects

As mentioned previously, effective heat dissipation is another key challenge to future generation GSI chips and chip-scale liquid cooling is a promising solution. To simultaneously meet the projected requirements for power delivery, bandwidth, and heat dissipation, "hyper integration" of electrical, optical and thermal-fluidic I/O interconnects may be necessary. Figure 6.22 illustrates the conceived integrated chip-scale package with compatible electrical, optical and thermal-fluidic interconnection. Through the via/socket connection, the on-chip integrated circuits and microchannel heat sink can be linked with the package substrate that is equipped with fluidic networks and electrical/optical routing circuits. In this section, compatible and highly integrated electrical, optical and thermal-fluidic I/O interconnects will be explored based on the previously developed "sea of polymer pillars" technology [6.3].



a: cover-plate or overcoat b: microchannel c: optical device
d: thermal-fluidic pipe e: optical or dual-mode pillar f: electrical pillar
g: solder coating or conductive adhesive

Figure 6.22: Illustration of integrated electrical, optical and thermal-fluidic I/O interconnects for "hyper-integration".

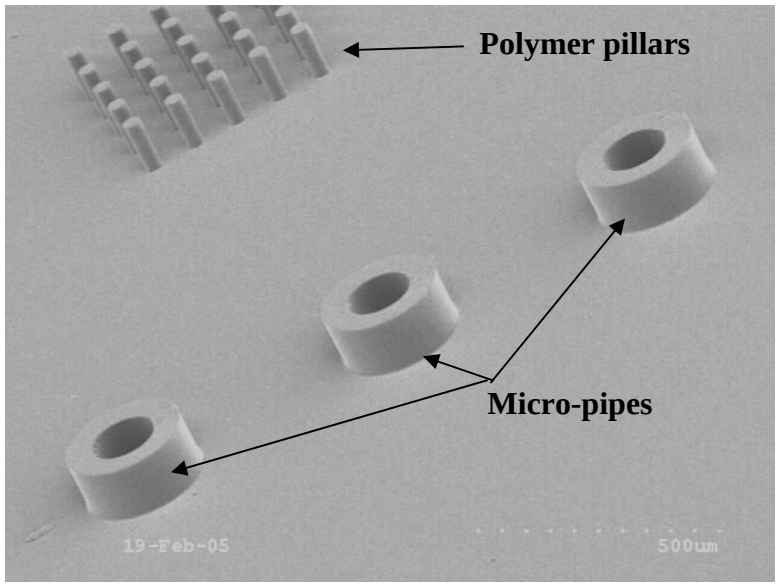
6.7.1. Polymer Pillars as the Building Block

To achieve such a compact system in a simple manner, a common building block with uniform height is necessary. Fortunately, the polymer pillar technology offers such a capability. Using photoimageable dielectric polymer materials, high aspect-ratio polymer pillars and polymer pipes can be fabricated simultaneously with one masking step. Figure 6.23 shows SEM micrographs of polymer pillars and polymer pipes fabricated using two types of polymers, Avatrel 2195 and SU-8. The processing conditions are listed in Table 6.2 for the two materials.

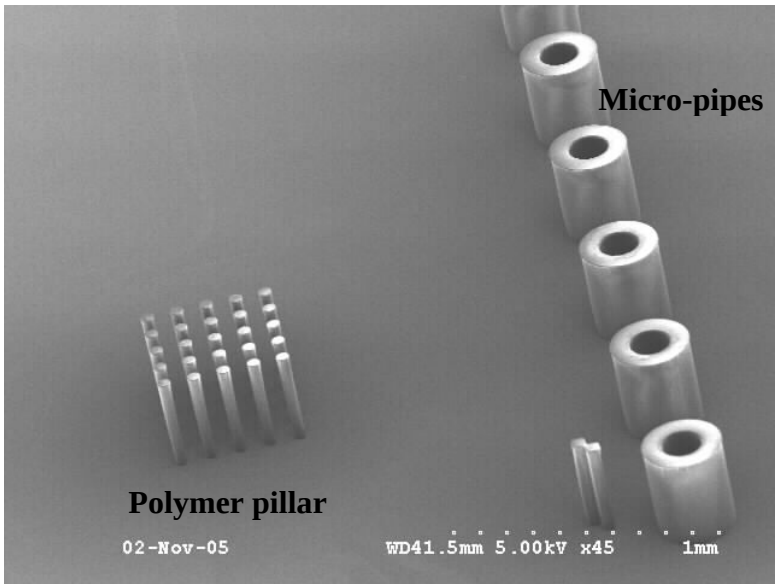
Experiments showed that an aspect ratio of more than 1:3 can be achieved using Avatrel 2195P and an aspect ratio up to 1:7 can be achieved using SU-8 for the polymer pillars. With two additional masking steps, these polymer structures can be metallized selectively to serve for different functions if necessary. For instance, the dual-mode polymer pillars can be used as simultaneous electrical/optical interconnects for optoelectronic devices such as photodetectors and VCSELs [6.15]. The polymer pillars can also be fully metallized and used only as electrical interconnects for power delivery, signal delivery, or clock distribution etc. Meanwhile, the polymer micro-pipes can be used for coolant delivery to enable on-chip microchannel heat sink, as described in Chapter 4 and Chapter 5.

Table 6.2: Processing conditions for the high aspect-ratio polymer structures using Avatrel 2195 and SU-8.

Polymer	**Spin Coating**	**Softbake**	**Exposure**	**Hardbake**
Avatrel 2195	1000rpm/500r/s/40s repeat once	35mins at 100 °C	200 mJ	15 min at 100 °C
SU8-2005	1000rpm/500r/s/40s	Ramp to 90 °C at 3°C/min; hold 1 hr	400 mJ	Ramp to 25°C at 3°C/min; hold 3hr



(a)



(b)

Figure 6.23: SEM micrographs of polymer pillars and polymer micro-pipes (h ~ 300 μm) fabricated simultaneously with various aspect ratios. (a) aspect ratio of ~ 1:3 achieved using Avtral 2195P (b) aspect ratio of ~ 1:7 achieved using SU-8.

Figure 6.24 shows SEM micrograph of a polymer pipe that is coated with a Ni/Au layer. The metallic coating can largely enhance the strength of the polymer pipe for high pressure liquid flow and might enable hermetic sealing of fluidic connection based on soldering processes.

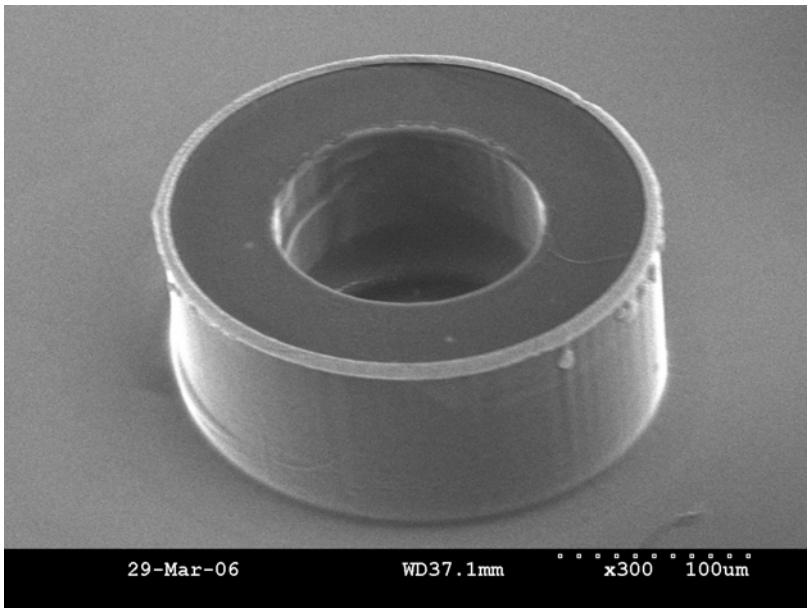


Figure 6.24: SEM micrograph of polymer pipe with electroplated Ni/Au shell.

6.7.2. Fabrication of Integrated Packaging Substrate with Electrical, Optical, and Thermal-fluidic Interconnects

Another key element for the integrated electrical, optical and thermal-fluidic interconnects is a package substrate that can provide necessary multi-functional paths. While the board-level optical waveguides have been widely studied, integrated optical and fluidic systems are not often reported, particularly for IC packaging. Fortunately, the previously reported air-gap technology for optical waveguides [6.16, 6.17] offers an opportunity for simultaneous fabrication of fluidic paths and optical paths. In this work, the sacrificial polymer, Unity 200P, has been

patterned to create air-gaps on a substrate for polymer waveguides as well as for fluidic channels, as shown in Figure 6.25. After over-coating with a structural polymer (Avatrel 2195) and thermal decomposition at around 200 °C, the air-gaps can be formed. Figure 6.26 shows the cross-sectional SEM micrographs of the air-gaps for the fluidic paths and the optical waveguides.

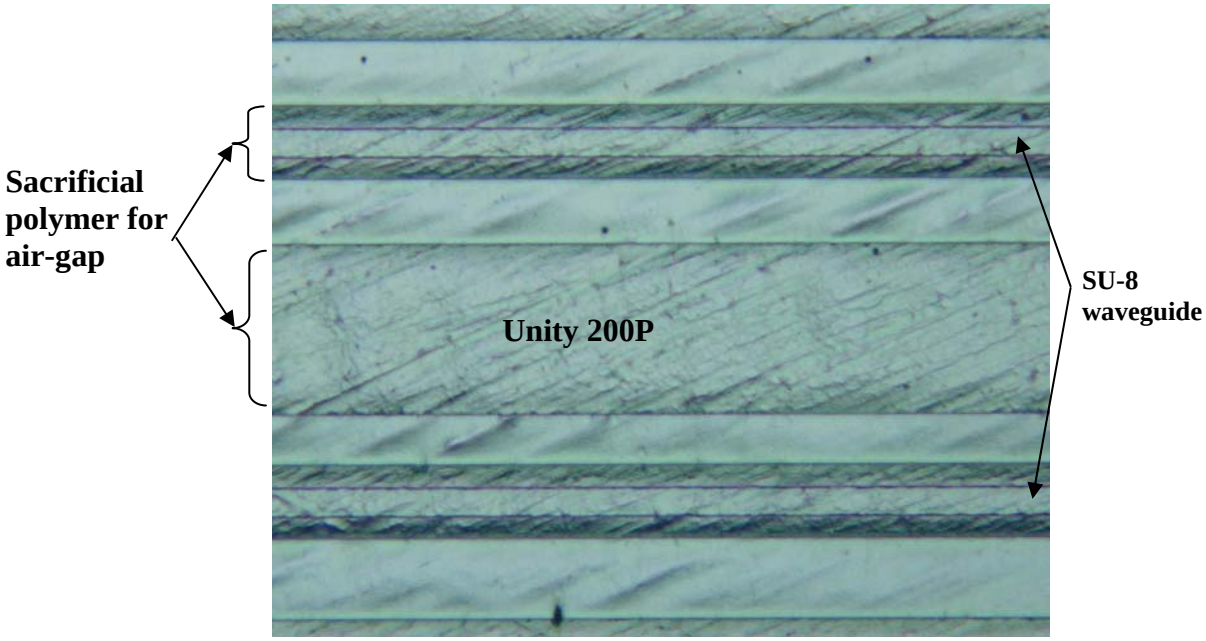


Figure 6.25: Optical micrographs of patterned sacrificial polymer for the air-gaps above optical waveguides and for fluidic channels.

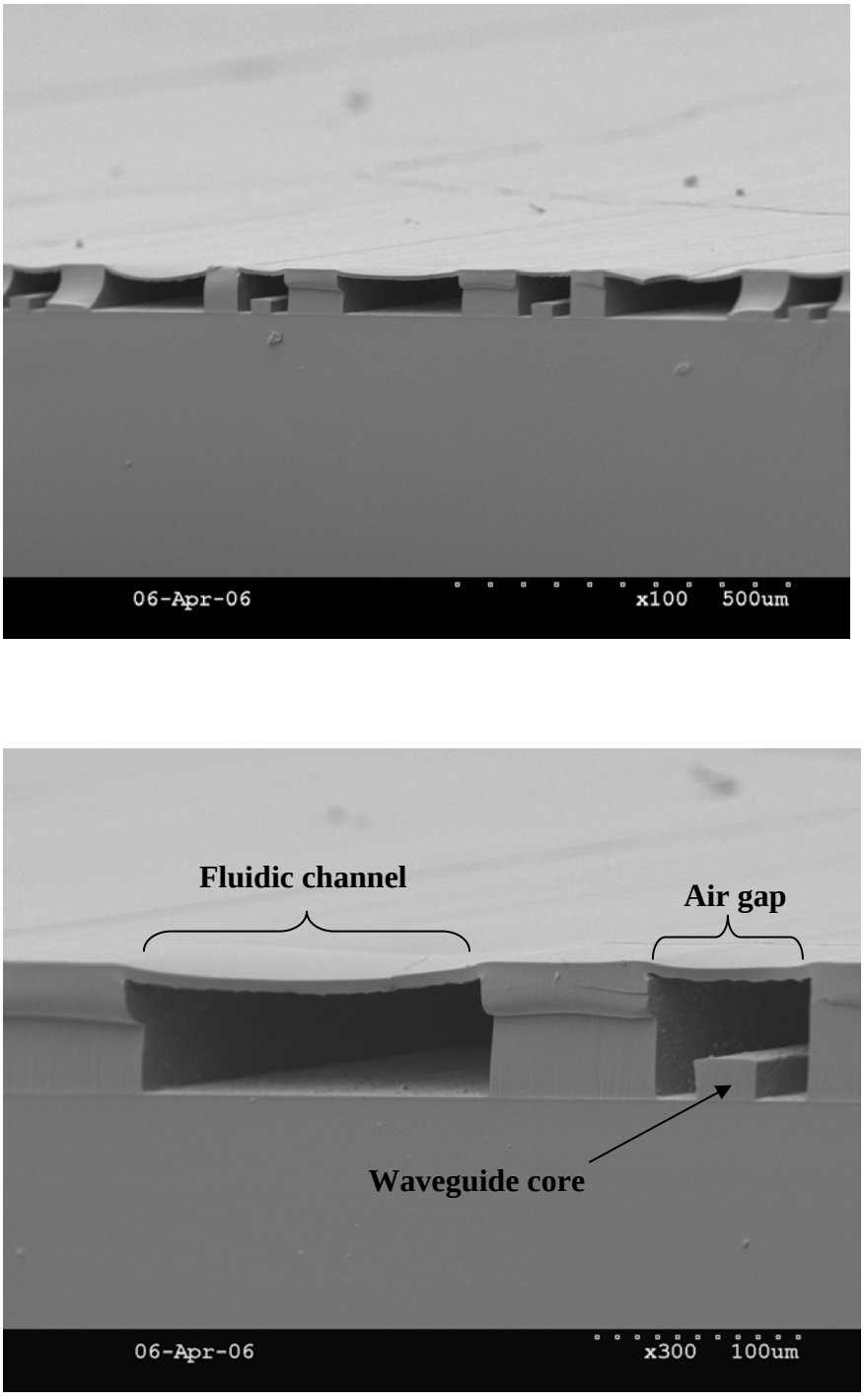


Figure 6.26: Cross-sectional SEM micrographs of the air-gaps that are fabricated simultaneously for polymer optical waveguides and mirofluidic channels.

6.8. Summary

This chapter first described the fabrication of metal-clad polymer pillars as dual-mode I/O interconnects. The polymer-based I/Os provide simultaneous electrical/optical paths between a chip and its mounting substrate. The current carrying capability was numerically analyzed to meet the ITRS projected requirement. The results indicate that the electrical resistance and current carrying capability of the polymer pillars can be comparable to that of the solid metal pillars, when they are coated with a reasonably thin metal (~5 μm).

An electrical/optical solder pad was introduced to achieve electrical/mechanical joining of the metal clad polymer pillars and to assist alignment for the optical paths during assembly. Assembly of the dual-mode polymer pillars was demonstrated and qualitatively tested with the use of a transparent glass substrate, a Si substrate with slab waveguide volume grating couplers, and a Si substrate with individual waveguides terminated by slanted Si mirrors.

An integrated I/O configuration with compatible electrical, optical, thermal-fluidic interconnects has been introduced. Polymer pillars were identified as a useful building block for the fabrication of three distinct types of I/O interconnects in a simple manner. Finally, simultaneous fabrication of air-gaps for optical waveguides as well fluidic networks was demonstrated for a packaging substrate to support the integrated electrical, optical and fluidic I/O paths.

Chapter 7. Conclusion and Future Work

This chapter presents the conclusion and summary of the key results and contributions in the dissertation. Furthermore, possible extensions of this dissertation will be outlined and discussed for future research endeavors.

7.1. Conclusion

7.1.1. MEMS-based SoL Compliant I/O Interconnects for GSI

There were three primary tasks for the demonstration of this technology: lead releasing and bumping processes; assembly and testing upon successful fabrication; characterization through simulation and numerical analysis. The key results are listed here:

- A "lift-off" process based on a thin film sacrificial layer (≤ 2μm) was first introduced for releasing of the electroplated leads, which can be better controlled since the problem of over-etching is eliminated.
- Bumping methods with masked evaporation or electroplating through photolithography have been investigated. Using the electroplating approach, bumping of the highly compliant leads can be completed through three masking steps in addition to conventional C4 processes.
- The overall process was reconciled for compatibility with the BEOL.
- Using a flip-chip bonder, the test chips with the MEMS leads were assembled on various package substrates including glass and the low-cost FR-4 PWB without use of any underfill.
- Daisy chain test structures were designed and implemented to evaluate the assembly yield and thermal-mechanical reliability.

- In the reliability test, SoL MEMS interconnects survived more than 500 thermal cycles without use of underfill, which represents a promising improvement over a regular C4 solder interconnection. Full reliability potential of the MEMS type SoL can only be better understood upon application of optimized board metallurgies, a proper design of solder mask opening, and optimized lead geometries and orientation.
- Failure analysis was performed and revealed that the main failure mechanism of the tested samples is at the solder joints instead of the compliant leads. Reliability of the SoL MEMS interconnects can be further improved by the optimization of the chip-package co-design.
- Structural effects of the MEMS leads were studied for mechanical compliance and electrical parasitics. Their mechanical compliance significantly depends on the displacement direction, cross-sectional area and aspect ratio (t/w). Trade-offs have been identified between out-of-plane compliance and the in-plane compliance, as well as between in-plane compliance and self-inductance for the MEMS leads.
- The influence from the heat sink weight was analyzed based on the vertical deformation of the MEMS leads. With presence of a large metal heat sink (~41g), spacers should be incorporated between the SoL chip and the package substrate to maintain a large enough gap so that the in-plane compliance of the SoL interconnects is not influenced by friction.

7.1.2. Integrated Thermal-fluidic I/O Interconnection and Packaging

The primary tasks for demonstration of this technology include: fabrication methods of on-chip microchannels at low temperature and compatible with CMOS wafers; simultaneous electrical/fluidic interconnection methods that are compatible with flip-chip assembly processes;

liquid-tight sealing methods for chip-scale packages; and thermal-fluidic measurement. The key results are listed here:

- Low-temperature glue bonding (≤ 200 °C) has been demonstrated using Avatrel 2195P.
- Novel monolithic microchannels with thin overcoats were fabricated using a thermally decomposable polymer (Unity 200) at low temperature, which can potentially enable highly integrated microfluidic systems. Continuous high-pressure fluidic testing (≥ 2.5 atm) was performed without cracking and leakage. Thermal-cycling tests also indicated excellent structural integrity at the interface between the layered overcoats and the Si substrate.
- Through-Si vias and polymer micro-pipes were introduced as the thermal-fluidic I/O interconnects to deliver coolants to the on-chip microchannels.
- For the approach with the sacrificial polymer, trench filling is the major challenge for the deep channels. Experimental results indicate a high-viscosity formulation sacrificial polymer is more effective to fill the deep trenches. Trenches with through-vias (375 μm in total) were successfully filled to enable the wafer-level integration.
- Fabrication of the fluidic channels using various package substrates, including Si, glass, and FR-4 laminates, was demonstrated to enable board-assisted coolant delivery.
- Assembly experiments verified the feasibility of the chip-to-board fluidic I/O interconnections and the underfilling process was performed to enhance the hermetic sealing of the polymer micro-pipes, which is compatible with conventional flip-chip assembly methods.
- For the first time to the author's knowledge, thermal-fluidic interconnection was successfully demonstrated between the board-level fluidic channels and on-chip

microchannels along with simultaneous area-array electrical interconnection using C4 solder bumps.

- Operation of the prototype integrated on-chip microfluidic heat sink based on the mirco-pipe I/O technology, on-chip microchannels, and board assisted fluidic delivery was demonstrated through testing.
- A dual-function thin-film heater/thermometer has been designed and integrated for cooling demonstration and measurement. A unit thermal resistance as small as 0.17 °C-cm^2/W was obtained at a flow rate of 104 ml/min. The measured pumping power (<1.25 W) is small compared with the power dissipated (~ 45 W). Cooling of a localized power density of more than 325 W/cm^2 was also demonstrated with local temperature rise of less than 50°C at a flow rate of 125 ml/min.

7.1.3. Compatible Electrical, Optical, and Thermal-fluidic I/O Interconnects

The primary tasks for demonstration of this technology include: a fabrication method for dual-mode electrical/optical polymer pillars at the wafer level; assembly and testing of simultaneous electrical/optical interconnects; and compatible fabrication of air-gaps for both microfluidic paths and optical waveguides. The key results are listed here:

- The fabrication of metal-clad polymer pillars as dual-mode I/O interconnects was demonstrated through three masking steps.
- The current carrying capability was numerically analyzed to meet the ITRS projected requirement. The results indicate that the electrical resistance and current carrying capability of the polymer pillars can be comparable to that of the solid metal pillars, when they are coated with a reasonably thin metal (~5 μm).

- An electrical/optical solder pad was then introduced to assist alignment and joining of the metal-clad polymer pillars. Assembly of the dual-mode polymer pillars was first demonstrated using a transparent glass die and a transparent glass substrate.
- Assembly of the dual-mode polymer pillars was demonstrated and qualitatively tested with use of waveguide volume grating couplers and slanted mirrors on Si substrates. Optical transmission through waveguides into polymer pillars was qualitatively verified.
- An integrated electrical, optical, thermal-fluidic I/O configuration was introduced for future generation GSI chips that demand high current drain, high bandwidth and high heat dissipation.
- Simultaneous fabrication of air-gaps for optical waveguides as well as fluidic networks was demonstrated for a packaging substrate with capability of integrated electrical, optical and fluidic paths.

7.2. Future Work

7.2.1. Bumping of SoL Interconnects with Lead-free Solder Alloys

In a response to the global transition to lead-free manufacturing in the semiconductor industry, lead-free solder bumping processes should be developed for SoL interconnects. Various lead-free alloys can be electroplated in methods similar to those for SnPb solders. Thus lead-free bumping of SoL interconnects can be easily demonstrated as an extension of this work.

7.2.2. Design Optimization of SoL Interconnects

Thus far, only “S-shape” or quasi-“S-shape” leads have been considered. Based on the FEM analysis approach described in the dissertation, leads with various geometries should be further studied. Dimensions and orientation can then be optimized to provide reasonably high

mechanical compliance for in-plane and out-of-plane directions for given I/O pitch, chip size or maximum distance to neutral point (DNP).

7.2.3. Metal -capped Monolithic Microchannels

A drawback of the polymer overcoat is its poor thermal conductivity. Thus, the fabrication process should be modified for metal-capped microchannels. A simple process for this is illustrated in Figure 7.1.

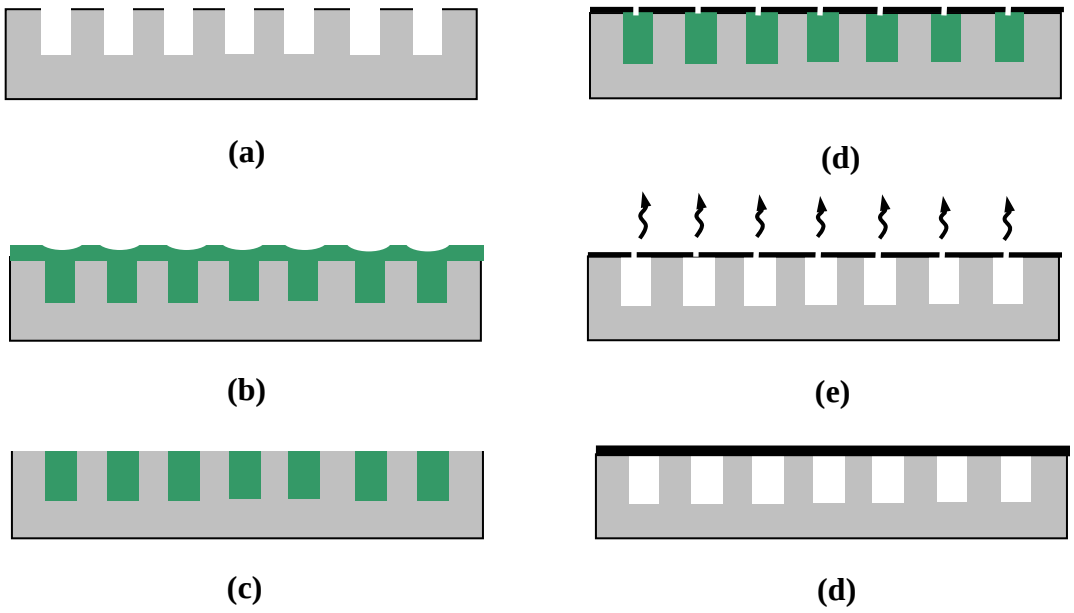


Figure 7.1: Schematic illustration of the fabrication of metal-capped microchannels.

Such a process is similar to that of the polymer based microchannels described in Chapter 4. After trench filling and polishing, by patterning and etching small openings through a metal seed layer, the sacrificial polymer inside the deep Si trenches can be removed during decomposition. The opening can then be easily enclosed by electroplating. The metal cap will provide better thermal conductivity and mechanical strength compared with the polymer cap.

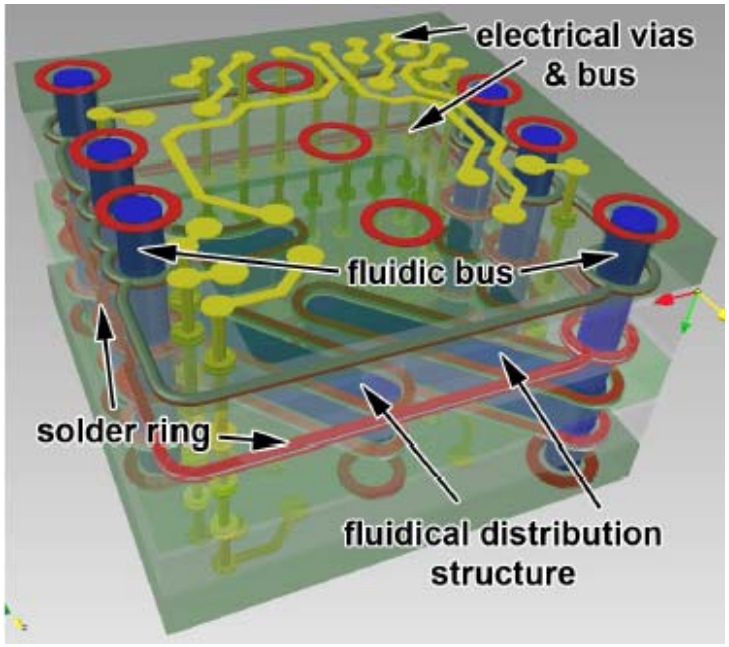
7.2.4. Optimization of Geometries and Dimensions for the On-chip Microchannel Heat Sinks

The thermal resistance analysis shown in Chapter 5 indicates that a smaller hydraulic diameter provides a large heat transfer coefficient for the convective heat transfer. In addition, with a smaller channel width, a larger number of channels can be fabricated for a give chip size. The overall surface area of the microchannels can then be largely improved and the thermal resistance for convective heat transfer can then be reduced. However, a smaller hydraulic diameter also means larger pressure drop for a given flow rate. Therefore, the dimensions of the microchannels should be optimized based on the trade-offs between the thermal resistance and required pressure drop for a give heat flux and pumping power.

7.2.5. Solder-based Hermetic Sealing for Thermal-fluidic I/Os

In this work, conventional underfilling process was used for sealing of micro-pipes. In the future work, solder-ring based hermetic sealing may be developed, as suggested in [7.1]. As shown in Figure 7.3, solder-ring based fluidic sealing has been studied to form compact 3-D packages by stacking multi-layer FR-4 substrates.

The same concept can be extended to micro-scale with wafer-level batch fabrication. As shown in Figure 7.3, solder cap has been fabricated at the top of polymer micro-pipes through electroplating. Figure 7.4 shows optical and SEM micrographs of a reflowed solder ring, which can be used to accommodate the solder/metal capped polymer micro-pipes. It can be seen that the surface tension of the molten solder assists formation of a smooth and round solder ring. An important feature of this concept is its compatibility with existing C4 solder bumping technologies.



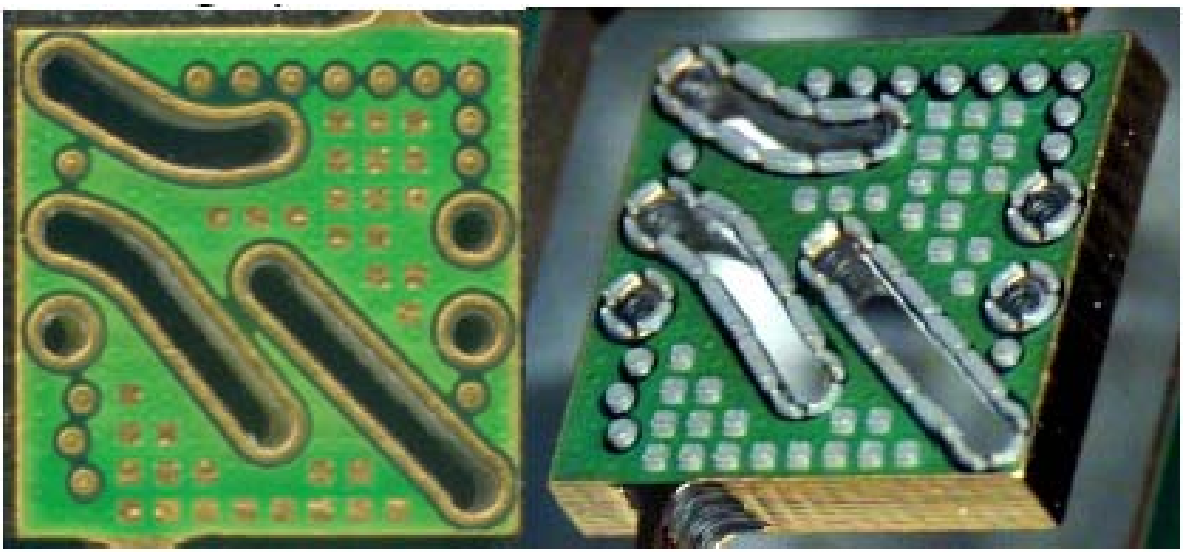


Figure 7.2: Optical micrographs of 3-D organic packages with solder based electrical interconnection and thermal-fluidic sealing [7.1].

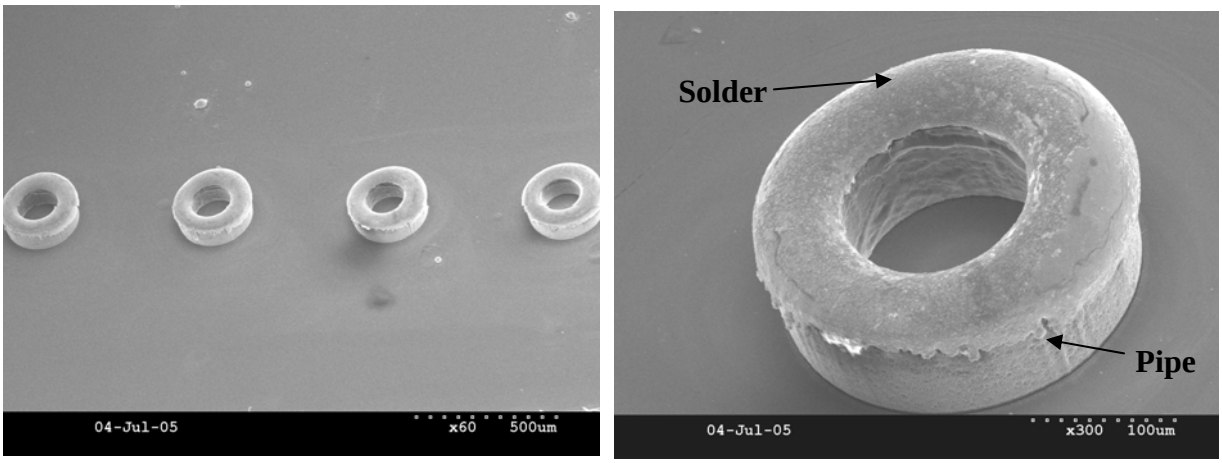


Figure 7.3: SEM micrographs of solder-caped polymer micro-pipes.

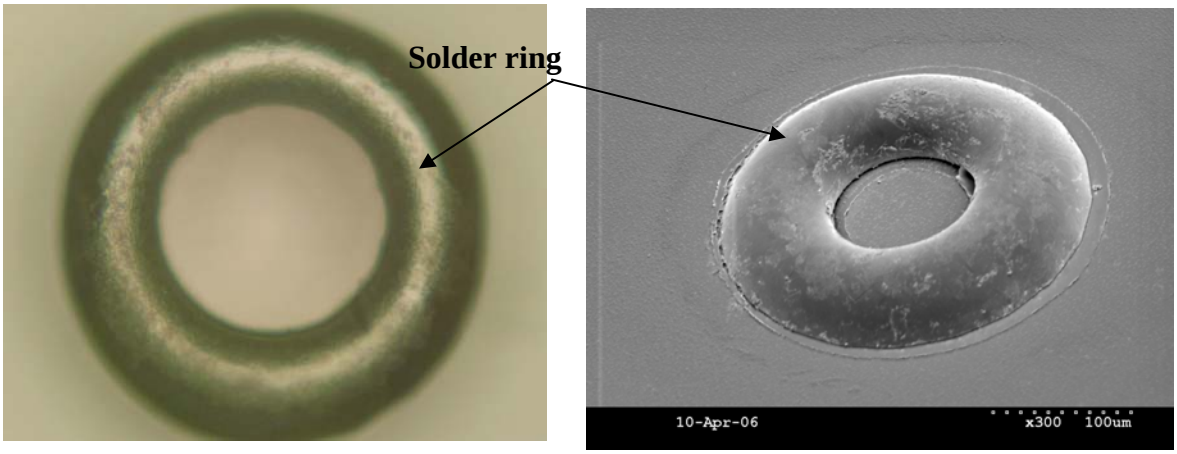


Figure 7.4: Optical and SEM micrograph of a reflowed solder ring to accommodate the solder/metal capped polymer micro-pipes.

7.2.6. Design of Integrated Thermal-fluidic Systems

In this work, the chip-package thermal-fluidic interconnection has been studied, but the overall thermal-fluidic systems need to be designed. The design of integrated thermal-fluidic systems may be based on a schematic shown in Figure 7.5. The thermal path includes three main segments: on-chip heat generation and the interface to the liquid system; the liquid system; and

the heat spreader or sub-ambient system. The fluidic path mainly includes two portions: the on-chip microfluidic channels and I/Os; and the delivering channels or pipes at the package substrate level. During the design, many issues need to be considered, such as the pump type, coolant type, the operating temperature, and so on.

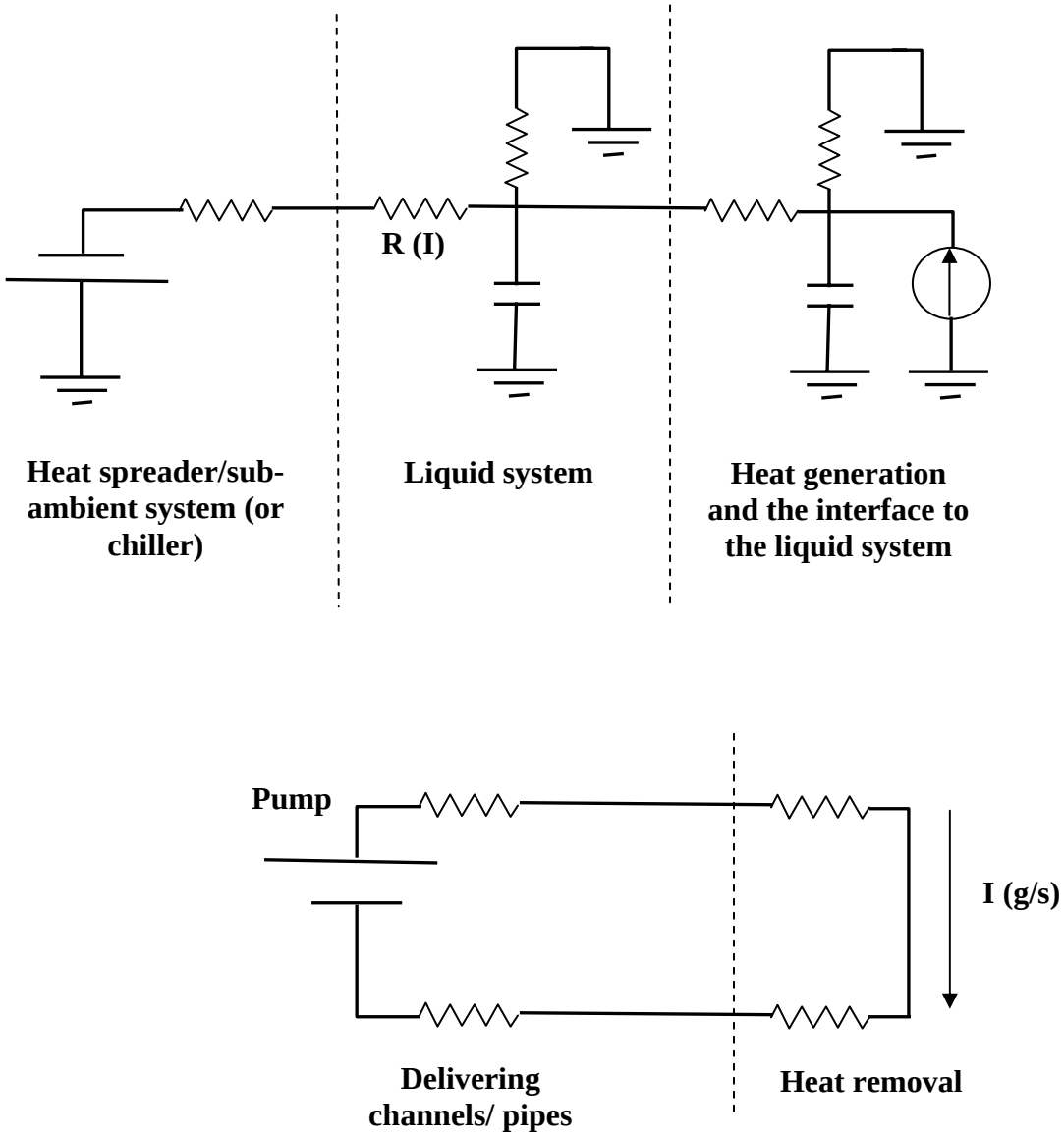


Figure 7.5: Schematic of thermal paths and fluidic paths for a closed-loop cooling system.

7.2.7. Integrated Thermal-fluidic Networks for 3-D Cooling

Effective cooling has been known as one of the major challenges for 3-D Microsystems [7.2, 7.3]. The on-chip microchannels, the thermal-fluidic I/O interconnects, and the board-assisted fluidic delivery developed in this work can potentially enable an integrated liquid cooling platform for 3-D chips. As illustrated in Figure 7.6, the glue bonded microchannels or the monolithic microchannels may be incorporated between stacked chips. The through-vias can be used to link the microchannels on different levels to form integrated thermal-fluidic networks. Parallel micro-pipes can then be used to connect on-chip fluidic systems with board-level channels for fluidic distribution.

Glue bonding seems to be a good option for wafer stacking. In fact, polymer based glue bonding (BCB) has been well studied for implementation of 3D chips in recent years [7.4]. For chip stacking, microchannels need to be monolithically fabricated for individual chips and they can then be assembled onto each other with flip-chip bonding processes.

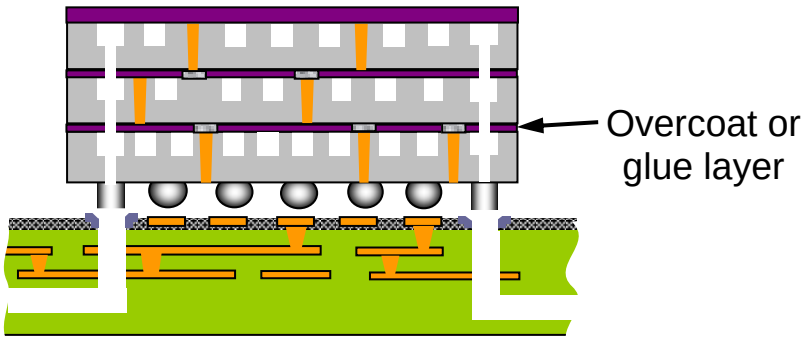


Figure 7.6: Conceived schematic for stacked chips with integrated microchannels and thermal-fluidic I/O interconnects.

7.2.8. Enhanced Microfluidic cooling of "hot-spots"

As mentioned in Chapter 5, cooling of "hot-spots" is a well-known challenge. While on-chip liquid cooling is a promising solution, it is desirable to improve the heat transfer in the regions with "hot spots". With advanced micromachining or nanotechnologies, ultra-fine fins or carbon nanotubes can be fabricated inside the microchannels selectively in desired areas. In this manner, overall hydraulic pressure drop will not be significantly affected, while the local heat transfer is improved.

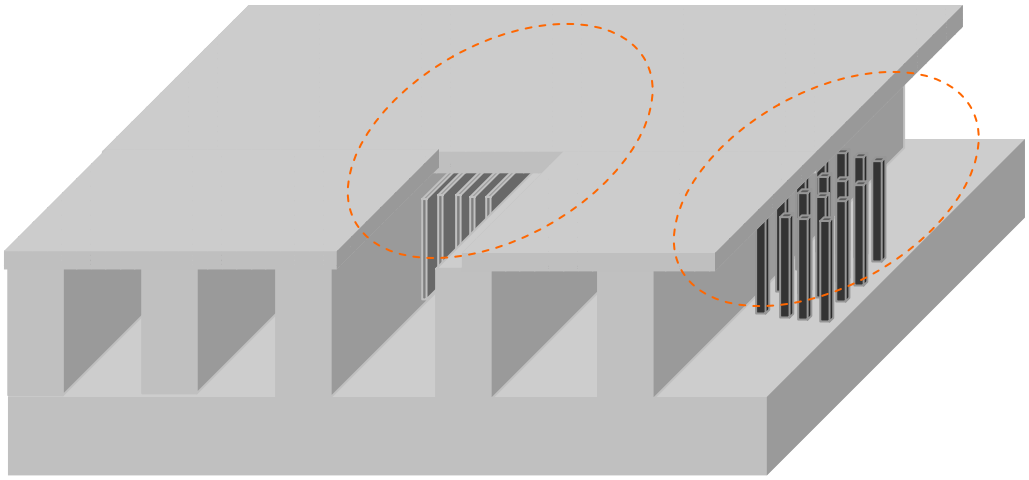


Figure 7.7: Conceived schematic of microchannels with ultra-fine fins or carbon nanotubes (CNTs) built only in the regions with "hop-spots".

7.2.9. Reliability Study for Thermal-fluidic Interconnection

A key challenge with the microfluidic cooling is its long-term reliability. While hermetic thermal-fluidic interconnection has been demonstrated based on an underfill, the long-term reliability is a complex function of the material properties and operating condition and needs to be investigated in the future.

7.2.10. Simultaneous Assembly of Electrical/Optical/Thermal-fluidic I/O Interconnects

In this dissertation, assembly of electrical and thermal-fluidic I/Os as well as assembly with electrical and optical I/Os were demonstrated, respectively. While the integrated electrical, optical, and thermal-fluidic I/O configuration was introduced, a full demonstration is still needed. A challenge is lack of chips that allow testing of the three distinct types of interconnection. For instance, a transparent glass chip is useful for electrical/optical testing, but it can not be used for thermal-measurement because it is difficult to fabricate the microchannels into glass substrates. In addition, glass substrates have poor thermal conductivity. Si chips can be used for electrical/thermal-fluidic measurement, but it is difficult for demonstration of optical measurements. There are two potential ways to address this issue. One is to incorporate optical vias in Si chips so that light can be detected at the backside of the test chips. Another is to incorporate optoelectronic devices such as MSM photodetectors onto the Si chips so that optical signals can be detected and converted into electrical signals, which requires collaboration with optoelectronics research groups.

7.3. Conclusion of the Dissertation

Using wafer-level batch processing, novel integrated I/O interconnects have been designed, fabricated, and demonstrated to enable compact GSI packaging with high I/O density, high reliability, and high performance at low cost.

MEMS-based sea-of-leads (SoL) compliant interconnects are promising for eliminating the need for underfill between a Si chip and an organic packaging substrate. Wafer-level packaging with the compliant interconnects can also largely reduce the impact on the fragile low-

k interlevel dielectric (ILD) films. The feasibility of the SoL MEMS I/O interconnects is demonstrated by process integration, assembly, and reliability assessment.

To achieve the high power dissipation with compact form factor, integrated thermal-fluidic I/O interconnects and low-temperature CMOS compatible microchannels are introduced and demonstrated. A prototype on-chip microfluidic heat sink was then demonstrated through assembly and thermal testing. The ITRS projected heat dissipation can potentially be achieved with low hydraulic pressure.

To meet the demand for high I/O bandwidth, highly integrated electrical and optical interconnects based on dual-mode polymer pillars are fabricated, assembled and tested. Coupling between waveguides and dual-mode polymer pillars was demonstrated using a test substrate with waveguide volume grating couplers (WVGC) and a test substrate with multiple individual polymer waveguides terminated by slanted mirrors.

The resulting integrated I/O interconnection and packaging technologies are compatible with back-end-of-the-line (BEOL) wafer processing and conventional flip-chip assembly. Finally, wafer-level packaging with integrated electrical, thermal-fluidic, and optical I/O interconnections is identified as the potential solution for compact packaging of future generation GSI chips.

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Vita

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