INVESTIGATION OF LIGHT INDUCED DEGRADATION IN PROMISING PHOTOVOLTAIC GRADE SILICON AND DEVELOPMENT OF POROUS SILICON ANTI-REFLECTION COATINGS FOR SILICON SOLAR CELLS

A Thesis
Presented to
the Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in Electrical Engineering

Georgia Institute of Technology
April 2004

INVESTIGATION OF LIGHT INDUCED DEGRADATION IN PROMISING PHOTOVOLTAIC GRADE SILICON AND DEVELOPMENT OF POROUS SILICON ANTI-REFLECTION COATINGS FOR SILICON SOLAR CELLS

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DEDICATION

This work is dedicated to

my mom Judith Damiani for supporting freedom of expression

my brothers and sisters for inspiring me to learn, explore, and do good

(Danny, Gabe, Donna, Tim, Debbie, Chrissie, Marie, and Tom)

my wife, Jennie Damiani for her faith, encouragement, and love

and my kids for the happiness they give me

(Lucas, Ethan, and Bailey)

ACKNOWLEDGEMENTS

I would like to express my gratitude to all the past and present members of the university center of excellence in photovoltaic research and education, UCEP, at Georgia Institute of Technology. I would like to express my sincere thanks to my advisor Dr. Ajeet Rohatgi for the incredible time commitment given to develop this thesis and for providing a truly exceptional research environment to learn in. I would like to thank Wayne Devezin, Dean C. Sutter, Ajay Upadhyaya, and Brian Rounsaville for their assistance in developing and maintaining the equipment used to fabricate and analyze the work in this thesis. I also want to extend my sincere appreciation to Denise Taylor for all her efforts to keep my research, travel, and other administrative tasks running smoothly. I would like thank to Dr. Thomas Krygowski and Dr. Abasifreke Ebong for guidance and advice. I would also like to thank Dr. Ralf Lüdemann for friendship and wisdom concerning this research. I would like to extend my sincere gratitude to all my fellow students for their friendship and dedication to photovoltaics, especially Ji-Weon Jeong, Alan Ristow, Vijay Yelunder, Mohamed Hilali, Jed Brody, Aleksander Pregelj, Kenta Nakayashiki, and Vichai Meemongkolkiat who assisted me in various aspects of this research. Finally I would like to thank my wife for her patience, inspiration, confidence, and support of this research through many challenges and accomplishments.

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SUMMARY

The current cost of photovoltaics is two to four times the cost of conventional energy sources in the United States. Crystalline Si accounts for more than 90% of the photovoltaic modules produced today. Nearly 55% of the cost of a Si photovoltaic module is associated with the crystallization and wafering of the silicon substrate. In an effort to reduce production costs, a great deal of research has been devoted to the development of low-cost photovoltaic grade silicon substrates. These low-cost silicon crystals often suffer from lower bulk lifetimes as a result of less stringent growth constraints that lead to higher incorporation of impurities, dislocations, and other defects. Cast multi-crystalline silicon substrates are used in more than 50% of the photovoltaic modules produced today. The random grain orientations of multi-crystalline silicon wafers inhibit the formation of uniform and effective surface texturing using conventional alkaline etching techniques. An effective surface texture can result in a 6 to 8% relative improvement in the conversion efficiency for multi-crystalline silicon solar cells. In addition, a textured surface acts to reduce the dependence on the bulk lifetime by obliquely coupling the light into the silicon substrate, keeping the photo-generated electron-hole pairs closer to the collecting junction. This provided the motivation for investigating porous silicon texturing in the second part of this thesis (Chapters 7 and 8).

The other main substrate used by industrial manufacturers of silicon solar cells is single crystalline Czochralski wafers (~30% of the market share). Czochralski silicon material

is known to suffer from the formation of a metastable defect under carrier injection, which acts to reduce the bulk lifetime and cause industrial screen-printed solar cells to lose 1 to 1.5% in absolute efficiency (or 7 to 10% relative efficiency) and is sometimes referred to as light induced degradation (LID). The electrical and structural properties of this defect are still not precisely known, thus providing the motivation for the first part of this thesis (Chapters 5 and 6), where the investigation of light induced degradation in low-cost photovoltaic grade silicon is studied. A typical Czochralski Si solar cell with an initial efficiency of ~16.5% could suffer a reduction in efficiency to ~15% after the formation of the metastable defect responsible for LID. It is known that the degradation in Czochralski Si occurs under illumination at room temperature and is annealed at temperatures greater than $200^{o}C$ in the dark. In Chapter 5 it is shown that trap formation can occur at temperatures above $200^{o}C$, provided sufficient carrier injection via illumination is present. Methods to eliminate or mitigate the effects of light induced degradation on finished solar cells are also discussed in Chapter 5. It is shown that by removing boron or oxygen from the silicon crystal, degradation is eliminated. Using a combination of device modeling and cell fabrication, it is also shown that by thinning the wafer substrate, the effect of light induced degradation on solar cell efficiency can be reduced. Appropriate cell design accounting for the back surface recombination velocity as well as the stable bulk lifetime in Czochralski Si solar cells can be used to optimize the efficiency performance. For the Cz material used in this study, which degraded from a 75 μs bulk lifetime to a 20μs bulk lifetime after degradation, the optimum cell thickness for planar devices was found to be in the range of 150 to 250 μm. Efficiency degradation reduced from 0.75% to 0.24% when the cell thickness was reduced from 378 to 157μm.

This represents a reduction in cell thickness by more than a factor of two. Combined with a higher stabilized cell efficiency, a reduction in cost (in $/W) of Cz solar cells can be realized. In addition, the careful analysis of defect formation conditions provides a better understanding of the trap responsible for light induced degradation.

The presence of light induced degradation in ribbon silicon solar cells is documented and analyzed for the first time in this thesis (Chapter 6). In addition, the role of light induced degradation in cast multi-crystalline silicon substrates is investigated. It is found that LID is often much smaller in cast multi-crystalline silicon compared to Cz silicon samples. In addition, the LID in multi-crystalline silicon is shown to be spatially non-uniform.

Using a photoluminescence mapping technique, the spatial dependence of light induced degradation in ribbon and cast multi-crystalline silicon (mc-Si) samples is analyzed. Trap generation and annihilation are observed in high lifetime regions of multi-crystalline silicon samples, while low lifetime regions tend to obscure light induced degradation. The impact of ambient conditions on the degradation of ribbon silicon samples was shown to be an important factor for the observation of LID. No degradation was observed over a 24-hour period at 25°C, but at an elevated temperature of $\sim 75^{o}$C, appreciable efficiency degradation was observed in high efficiency ribbon solar cells (>16%). Czochralski silicon solar cells showed full degradation within 24 hours at 25°C. Thus, a more thorough description of LID in mc-Si materials needs to include some

temperature profiling to decrease the observation time required to quantify the efficiency degradation.

Part two of this thesis involves the development of a rapid surface texturing technique suitable for all crystalline silicon substrates. It is demonstrated in Chapter 7 that chemically formed porous silicon is a simple and rapid technique for texturing single as well as multi-crystalline silicon. Only 6 to 10 seconds in a 200:1 HF to HNO_3 solution at room temperature allows for the formation of an effective porous silicon anti-reflection coating. Low reflectance and good surface passivation were achieved by using the DOSS solar cell process. The DOSS diffusion from a limited source wafer was tailored to obtain the desired sheet resistivity underneath the porous silicon layer. This resulted in a porous silicon anti-reflection coated solar cell efficiency of 15.3% on a float zone Si sample with an excellent fill factor (78.7%). This represents the highest efficiency porous silicon etched solar cell reported to date. The typical process used in the literature involves porous silicon etching as the final step in the solar cell fabrication sequence. The major problem associated with this process sequence is fill factor degradation resulting from exposure of the metal contacts to the porous silicon etching solution. This problem was overcome in this research by porous silicon etching prior to cell processing, which resulted in a 0.807 and 0.787 fill factor for photolithography cells and screen-printed solar cells, respectively.

In Chapter 8, it is shown that incorporating an acid texture prior to porous silicon etching can improve the surface reflectance for cast multi-crystalline and Czochralski (Cz) silicon

samples that have significant surface damage when they arrive from manufacturers. The addition of an acidic texture to Cz and cast mc-Si solar cells gave the highest efficiency screen-printed porous silicon solar cells fabricated to date. Solar cell efficiencies of 14.8% for Cz Si and 13.6% for cast mc-Si (without the conventional SiN anti-reflection coating) were achieved using Process D developed in this work. Although these efficiencies are lower than what can be achieved with traditional SiN coated solar cells, they provide the opportunity to use an alternative, less expensive anti-reflection coating that is rapidly formed and still achieves enhanced performance. The weighted reflectance of Cz silicon solar cells fabricated with Process D obtained a lower weighted reflectance (8.3%) than the traditional SiN single layer anti-reflection coating (12.4%). Thus, the development of a rapid, inexpensive texture and anti-reflection coating was achieved through the use of porous silicon etching and the DOSS diffusion technique.

CHAPTER 1

1   INTRODUCTION AND RESEARCH OBJECTIVES

1.1   Statement of Problem

Worldwide demand for electrical energy is growing rapidly in conjunction with the depletion of traditional energy sources and increasing world population. In addition, the burning of fossil fuels is resulting in significant increases in CO_2 and other greenhouse gases in our environment, leading to increased pollution and potential global warming. There is a real need to develop alternate energy sources that can solve energy and environmental problems simultaneously. Viable energy sources for the future must be available on demand and should be renewable and environmentally friendly. In addition, the cost of energy production and delivery must be comparable to current energy sources. This is particularly important for countries like the United States where cost competitiveness is more critical because other forms of energy are readily available through the electrical grid. Photovoltaics, or solar electricity, is a promising renewable energy technology that is rapidly approaching mainstream feasibility. Solar energy is free, unlimited, and not localized in any part of the world. The sun is expected to continue shining for the next five billion years, providing an abundant source of energy. Solar cells are simple semiconductor devices that convert sunlight directly into electricity without any undesirable impact on the environment. More than 95% of solar cells are currently produced from silicon semiconductors in the form of single crystal, multi-crystalline, or amorphous Si, with greater than 90% from crystalline silicon alone [1].

Silicon is the second most abundant element (27.7%) in the earth's crust [2]. Thus, the raw material used for energy production is also seemingly inexhaustible. Once a silicon solar module is finished, no harmful gases are emitted. Solar power generation is clean, quiet, and environmentally friendly. However, the cost of generating electricity from solar cells is currently two to four times greater than that of fossil fuels [1].

A typical cost breakdown of crystalline silicon solar modules is depicted in Figure 1 for screen-printed cast multi-crystalline silicon cells [1]. Only ~17% of the total module cost is associated with solar cell processing. Approximately 30% of the cost is associated with the module assembly. The bulk of the cost is associated with the silicon substrate,
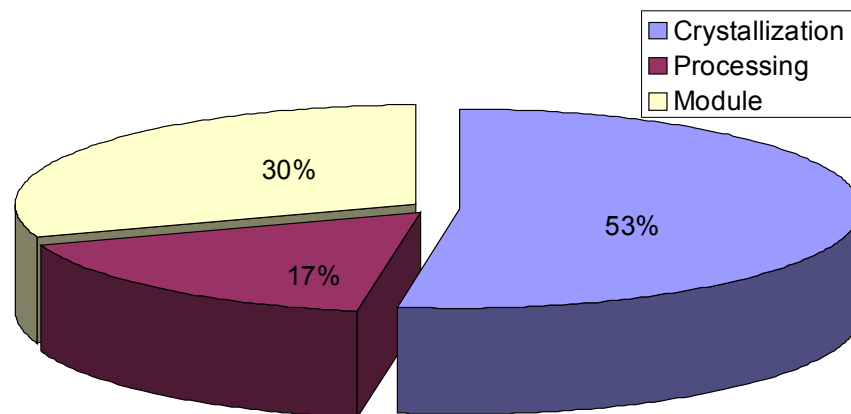
Figure 1. Cost associated with solar cell fabrication for screen-printed technologies for single and multi-crystalline silicon.

which includes feedstock production, crystallization, and wafer slicing, accounting for ~53% of the total cost. Therefore, different strategies and technologies aimed at reducing

the cost of wafer production are currently being developed and investigated. High module cost today can be partially offset by using building integrated photovoltaics (BIPV) [3]. Solar modules can be used to substitute for roofs, walls, or windows of a building, thereby reducing the marginal or effective cost of photovoltaics (PV). In addition, the power can be produced at the point of use, avoiding power transmission and distribution losses. Silicon ribbon growth techniques, such as string ribbon (SR) and edge-defined film-fed growth (EFG) can reduce the cost of Si substrates by eliminating kerf losses attributed to the loss of Si material resulting from wafer sawing and ingot shaving for the useable core section [2].

The theoretical efficiency limit of a single junction, one-sun crystalline Si solar cell is ~29% [4]. Solar cell efficiencies in laboratories have reached 24.7% for one-sun illumination [4] using high-quality float zone (FZ) silicon substrates and several advanced design features such as selective emitter, inverted pyramid texturing, and front and back surface oxide passivation incorporated into the Passivated Emitter and Rear Locally diffused back surface field cell (PERL cell). Unfortunately, the process sequence used to fabricate these cells involves many high-temperature and photo-mask steps along with low through-put technologies such as vacuum deposition and photolithography. On the other hand, current industrial cell efficiencies are only in the range of 10 to 15% because of the use of low-cost silicon and simplified processing, and the absence of high efficiency features [1]. However, industrial cells can be produced in a few hours as opposed to 1 to 2 weeks. As a result, laboratory cells are too expensive and industrial cells are not efficient enough to meet the cost and efficiency targets ($/watt)

simultaneously. There is a need for a low-cost solution that incorporates high efficiency design features in commercial cells that currently suffer from low minority carrier bulk lifetimes caused by impurities, traps, or defects. Crucible-grown Czochralski (Cz) silicon has been a dominant source material for photovoltaic (PV) substrates, accounting for ~30% of the PV modules produced today. Recently, however, light induced degradation (LID) in boron doped Cz Si solar cells has been recognized as a significant cause of minority carrier lifetime degradation during cell operation because of a metastable defect formation under carrier injection. The drop in minority carrier lifetime results in a significant decrease in Cz silicon solar cell efficiency (approximately 8 to 10%, relatively). In addition, there are recent reports on LID in multi-crystalline silicon (mc-Si).

Multi-crystalline Si, including cast and ribbon materials, accounts for ~55% of PV modules today. Model calculations have shown that light trapping via surface texturing can enhance the efficiency of Si cells by 1.2% absolute. However, because of the random grain orientation, conventional isotropic texturing methods do not effectively texture the surface of multi-crystalline materials. This introduces another efficiency-limiting mechanism for industrial solar cells fabricated on cast or ribbon multi-crystalline Si. The lack of texturing for multi-crystalline Si is estimated to account for a 6 to 8% loss in efficiency for industrial type solar cells. This thesis attempts to address both of these important issues: investigating light induced degradation in low-cost PV grade materials and improving the anti-reflection coating in mc-Si via porous silicon etching and acidic isotropic texturing using low-cost technologies.

1.2   Specific Research Objectives

The objective in this thesis is to improve the performance and stability of promising solar grade silicon materials, in particular, Czochralski and cast multi-crystalline silicon. This is accomplished by addressing major efficiency-limiting mechanisms in each substrate. The specific goals addressed in this thesis are to develop low-cost rapid technologies aimed at preserving or improving bulk lifetime in solar grade silicon wafers; in particular, understanding, quantifying, and mitigating light induced degradation in promising boron doped p-type Si substrates, including single crystal Si, cast mc-Si, and Si ribbons. Part two involves the development of a cost-effective porous silicon anti-reflection coating (ARC) suitable for single and mc-Si cells.

1.2.1   Task 1. Investigation of trap formation conditions for the metastable defect that causes light induced degradation in Czochralski silicon.

LID is known to reduce the minority carrier lifetime in single crystal Cz silicon substrates. Electrical and structural characteristics of the LID trap are not currently fully understood. Therefore, trap formation and annihilation mechanisms need to be further investigated. In this task, effective lifetime measurements are performed on as-grown and processed Si materials. First, lifetime degradation is demonstrated in traditional B doped Cz silicon with high O_i concentration before and after laboratory and industrial cell

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processing. Next, key parameters affecting the magnitude of LID are investigated, including B and Ga doping, O_i concentration, annealing temperature, and illumination time.

1.2.2 Task 2. Determination of the impact of the metastable defect on the efficiency screen-printed industrial solar cells.

Task 2 quantifies the extent of bulk lifetime and efficiency degradation in industrial-type screen-printed silicon solar cells. Industrial solar cells focus on achieving an appropriate $/Wp and therefore are typically lower in efficiency (12 to 15%) than laboratory solar cells (20%). Laboratory cells are typically fabricated on Si with high lifetimes and thus suffer more from lifetime degradation. Industrial solar cells do not typically achieve such high lifetime values and therefore would seemingly suffer less. In this task complete solar cells are fabricated using screen-printing followed by light soaking to study LID. Quantum efficiency and light and dark I-V analysis are performed on various single crystal silicon samples before and after LID to assess the impact of LID on industrial-type screen-printed solar cells. Since LID can be avoided if either B or O is eliminated from the silicon crystal, high efficiency screen-printed devices are fabricated and characterized on single crystal materials such as B doped Cz with high O_i, Ga doped Cz with high O_i, B doped FZ with undetectable O_i, and B doped MCz with low O_i content.

1.2.3 Task 3. Investigate light induced degradation trap formation conditions in low-cost multi-crystalline silicon solar cells.

In addition to Cz Si, cast mc-Si and Si ribbons are also being extensively used for silicon PV. Currently, all Si materials used for industrial photovoltaic production contain boron and some level of oxygen. However, the extent of LID in these materials is largely unknown. Limited information exists on cast multi-crystalline silicon LID [5], while there are no reports on cell efficiency degradation as a result of LID in ribbon multi-crystalline silicon cells. As-grown material lifetime is generally too low in mc-Si materials to detect any LID. Therefore, appropriate preprocessing is performed to enhance lifetime to detect the metastable defect formation. Lifetime versus injection level measurements and analysis are performed on several promising multi-crystalline silicon materials after various processing steps used to improve bulk lifetime during cell fabrication. In addition, photoluminescence lifetime mapping is used to determine spatial variation in the LID trap concentration. Special attention is given to detecting LID in very high efficiency mc-Si cells.

1.2.4 Task 4. Develop solar cell designs that reduce or eliminate the effects of light induced degradation in crystalline silicon solar cells.

In this task, special attention is given to B doped Cz Si because it is the material of choice for most PV manufacturers using single crystal wafers and it suffers the most from LID.

Appropriate cell design can limit or eliminate the affects of LID on solar cell efficiency for both single and multi-crystalline Si. For example, reducing cell thickness increases the minority carrier diffusion length to cell width ratio (L/W) and may make cell efficiency less sensitive to lifetime degradation provided other device parameters are properly selected or designed. In this task, a combination of device modeling, cell fabrication, and characterization are used to minimize LID through careful cell design.

1.2.5 Task 5. Investigate low-cost texturing methods for multi-crystalline silicon solar cells.

In addition to LID in mc-Si solar cells acting to reduce the final cell efficiency, the random grain orientation on the surface of mc-Si solar cells restricts effective light trapping. This is because of difficulties achieving uniform texturing, resulting in the loss of photo-current.   Conventional isotropic texturing methods are not effective for enhanced light trapping. This results in the loss of 8 to 10% in relative cell efficiency. Mechanical texturing, Reactive Ion Etching, isotropic acidic texturing, and porous silicon etching are four methods currently being investigated as possible solutions to this problem.   Therefore, in Task 5, a rapidly formed uniform porous silicon coating is developed that is suitable for solar cell fabrication and does not depend on surface morphology or grain orientation.

1.2.6 Task 6. Develop process sequence and fabricate high efficiency porous silicon etched solar cells.

The Dopant Oxide Solid Source (DOSS) process, developed at Georgia Tech, is particularly suitable for porous silicon etched emitters because it can produce uniform diffusions on textured surfaces. This allows the formation of porous silicon prior to the emitter diffusion. Most investigators do the porous silicon etching as the final step in the solar cell process sequence. It is sometimes undesirable to do porous silicon etching at the end of cell fabrication because it could attack the metal contacts. DOSS processing can produce emitter, BSF, and oxide passivation in a single high-temperature step and does not require any glass etching after diffusion. Task 6 focuses on fabricating DOSS solar cells with a porous silicon anti-reflection coating (ARC) applied at the end of the standard wafer cleaning, *before* the start of solar cell processing. Various porous silicon solutions are examined to minimize reflectance in conjunction with good uniformity and reproducibility. Changes in porous silicon properties during subsequent cell processing are examined, along with establishing constraints or limitations pertaining to porous silicon ARC implementation at the start of cell processing. Finally, high-efficiency solar cells are fabricated with high fill factors using porous silicon anti-reflection coatings, without the need for deposition of a conventional SiN anti-reflection coating.

CHAPTER 2

2   SOLAR CELL FUNDAMENTALS AND EFFICIENCY LIMITING MECHANISMS

2.1   Current and Voltage

The presence of a p-n junction in a semiconductor makes solar power possible. The space charge region is formed as a result of the diffusion of majority carriers across the metallurgical junction, and its width is fixed when the diffusion is counter balanced by the drift of carriers in the opposite direction (Figure 2), thus setting up a compact but strong electric field as the "collecting junction" in the depletion region.   In thermal equilibrium, drift and diffusion currents through the depletion region oppose each other, resulting in zero net current flow.   Figure 2 shows a schematic junction formation along with the space charge region and electric field that has a maximum at the metallurgical junction.   Using light as an external stimulus allows the p-n junction to behave as follows. Part of the solar spectrum is absorbed in a semiconductor through the transfer of optical energy to electrons that are excited into the conduction band, E_c,
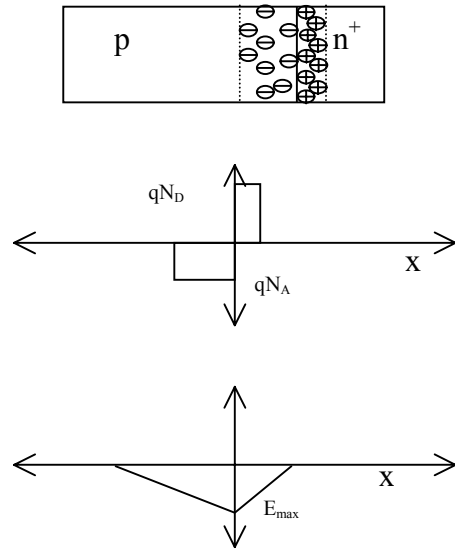
Figure 2. Model of depletion region, space charge density, and electric field.

creating holes in the valence band, E_v. The electric field in the depletion region helps in separating these electron-hole pairs, resulting in a voltage or the photovoltaic effect.

In discussing a solar cell, it is constructive to start with the simple diode equations used to describe the operation of a p-n junction. The dark saturation current, I_{o1}, is the "leakage" current that flows out a diode in the dark under reverse bias and is represented analytically by the following equation:

$$I_{o1} = qn_i^2 A(\frac{D_n}{L_n N_A} + \frac{D_p}{L_p N_D}) \tag{1}$$

where n_i is the intrinsic carrier concentration, N_A and N_D are the ionized concentration of acceptors and donors, L_n and L_p are the diffusion lengths of electrons and holes, q is the electron charge, and D_n and D_p are the diffusivity constants for the minority carriers. I_{o1} is primarily a drift current because reverse bias increases the barrier for diffusion current. On the other hand, forward bias lowers the barrier for diffusion and the current is largely dominated by diffusion, where

$$I \cong I_{o1} e^{qV/kT} \tag{2}$$

The total current of an ideal diode can be written as

$$I = I_{o1}(e^{qV/kT} - 1) \tag{3}$$

Figure 3 shows the light and dark current-voltage curves for a solar cell, along with the equivalent circuit used to analyze a solar cell. Non-ideal diode behavior in solar cells is typically a result of recombination in the depletion region, series resistance (R_s), and shunts resistance (R_{sh}) and can be described using the following equation:

$$I = I_{o1}(e^{q(V-IR_s)/kT} - 1) + I_{o2}(e^{q(V-IR_s)/nkT} - 1) + \frac{V - IR_s}{R_{sh}} \tag{4}$$

where I_{o2} and n are used to describe the recombination in the depletion region. When a light bias is applied to a solar cell, according to superposition, light and dark currents oppose each other, and the terminal current is given by

$$I = I_{dark} - I_{light} \tag{5}$$

a.)

b.)
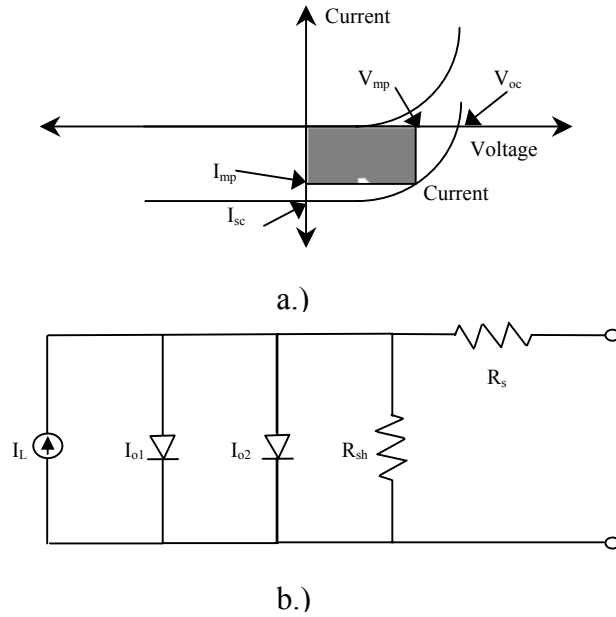
Figure 3. a) Current-voltage curve under light bias, FF is shaded region, b) Equivalent circuit.

$$I = -I_{light} + \left[I_{o1}(e^{q(V-IR_s)/kT} - 1) + I_{o2}(e^{q(V-IR_s)/nkT} - 1) + \frac{V - IR_s}{R_{sh}} \right] \qquad (6)$$

where V is the terminal voltage, k is Boltzmann's constant, n is the non-ideality factor, R_s is the series resistance, and R_{sh} is the shunt resistance. If short circuit conditions are applied, the current out of the solar cell, I, is equal to the short circuit current, I_{sc}. The above equation is sometimes approximated by a single exponential

$$I = -I_{sc} + I_o(e^{qV/nkT} - 1) \qquad (7)$$

which, under V_{oc} or open circuit conditions, I=0 and V=V_{oc}, (7) results in

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{I_{sc}}{I_o} + 1 \right) \qquad (8)$$

where I_{light} is assumed equal to I_{sc}. To maximize V_{oc}, the dark current I_o must be minimized. To maximize J_{sc}, recombination in the cell must be minimized and light trapping must be maximized. The reverse saturation current, I_{o1}, is composed of an emitter saturation current, I_{oe}, and a base saturation current, I_{ob}, or correspondingly, the emitter and base saturation current densities J_{oe} and J_{ob} make up the reverse saturation current density J_{o1}. These parameters are discussed more in Appendix A and are used throughout this thesis to help analyze and quantify surface passivation.

2.2 Fill Factor and Cell Efficiency

Terrestrial solar cell efficiency is reported at the standard AM1.5 global conditions. The measuring temperature is 298 K, and light intensity is 100 mW/cm^2 given by the zenith cycle of 48°. Cell efficiency is given mathematically by

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$$\eta = \frac{V_{oc}J_{sc}FF}{P_{in}} \qquad (9)$$

P_{in} is the incident light intensity, and the fill factor, FF, is the measure of the squareness of the illuminated curve in Figure 3, given by

$$FF = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}} \qquad (10)$$

The max power point of the solar cell is defined as (V_{mp}, I_{mp}); for maximum power output, the load curve should pass through the max power point or the voltage across the load should be the V_{mp} for optimum performance. The solar cell equivalent circuit in Figure 3 demonstrates how a high diode saturation current, a high series resistance in the circuit, and a low shunt resistance can adversely affect the output power or cell efficiency. High series resistance causes power loss because of I^2R effects. A low shunt resistance and/or high I_{o2} results in FF and voltage loss as a result of a shunt path through the collecting junction. A low surface recombination velocity and high bulk lifetime can greatly improve I_{o1} and solar cell performance, as is discussed throughout this thesis. Bulk lifetime and surface recombination are important for solar cells made from solar grade silicon substrates that suffer from LID and random grain orientation.

2.3   Carrier Lifetime and Recombination in Silicon

A typical silicon solar cell wafer is 300 μm thick. A large number of the excited carriers can be affected by bulk and surface recombination [6]. When an external stimulus is applied to a semiconductor such as light, heat, or voltage, carriers are injected in excess of equilibrium values. If the external stimulus is removed, the injected carriers will decay

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back down to equilibrium values via a mechanism referred to as recombination. Recombination can occur either at the surface of the semiconductor or within the bulk of the device.

2.3.1 Bulk

Bulk recombination is characterized by three recombination mechanisms that vary in importance, depending upon i) the level of external stimulus applied, ii) the semiconductor band gap type (direct or indirect), and iii) the amount and type of impurities present. These mechanisms are Shockley-Read-Hall recombination, Auger recombination, and radiative band-to-band recombination. These mechanisms are well documented in the literature. Figure 4 shows a schematic diagram of an electron being recombined by each mechanism. Recombination of excess carriers occurs after a given
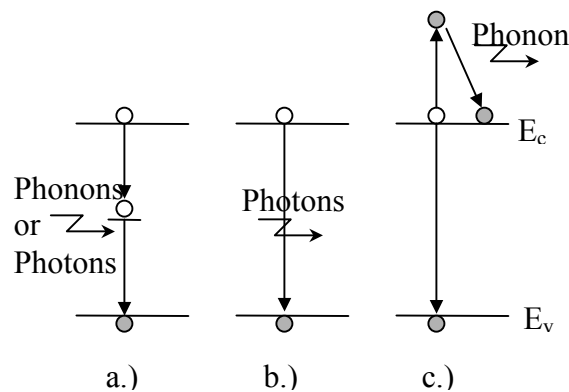
Figure 4. a) Shockley-Read-Hall recombination, b) Radiative recombination, and c) Auger recombination.

external stimulus (voltage or light) is applied. Under steady-state conditions, the recombination rate is equal and opposite to the generation rate [7]. When the stimulus is removed the injected carriers, Δn, recombine and the sample reverts to the equilibrium state. Bulk lifetime is defined as

$$\tau = \frac{\Delta n}{U} \tag{11}$$

where U is the net recombination rate, τ is the carrier lifetime, and Δn is the injected carrier concentration.

2.3.1.1 Shockley-Read-Hall Recombination

The most common type of recombination in the bulk or base of the solar cell takes place via energy levels within the forbidden energy gap of the semiconductor. These levels, or traps, are generated by impurities and/or defects. The equation used to describe the Shockley-Read-Hall (SRH) recombination lifetime is as follows

$$\tau_{SRH} = \frac{\tau_{po}(n_o + n_1 + \Delta n) + \tau_{no}(p_o + p_1 + \Delta p)}{(n_o + p_o + \Delta n)} \tag{12}$$

where

$$n_1 = n_i e^{(E_T - E_i)/kT}; p_1 = n_i e^{-(E_T - E_i)/kT} \tag{13}$$

$$\tau_{no} = \frac{1}{\sigma_p v_{th} N_T}; \tau_{po} = \frac{1}{\sigma_n v_{th} N_T} \tag{14}$$

and n_o and p_o are the equilibrium electron and hole concentrations, n_i is the intrinsic carrier concentration, Δn and Δp are the injected carrier concentrations, τ_{no} and τ_{po} are the

carrier lifetimes if the trap resides at midgap, v_{th} is the thermal velocity, σ_p and σ_n are the capture cross section for holes and electrons, N_T is the trap concentration, and n_1 and p_1 are the number of electrons or holes in the conduction or valence band when the fermi level coincides with the trap energy level, E_t [8-9]. In addition to Deep Level Transient Spectroscopy (DLTS), Injection-Level Dependent Lifetime Spectroscopy (IDLS) and Temperature Dependent Level Spectroscopy (TDLS) are two new techniques that have been used recently to determine trap characteristics in solar cells by using photo-conductance decay (pcd) measurements. Because solar grade silicon is often highly defective and contains various levels of impurities, depending on the growth techniques used, many trap levels within the forbidden energy gap are introduced. Some of the traps are radiative and thus give rise to sub-bandgap light emissions in silicon (Si bandgap = 1.09 eV), thus allowing for photoluminescence techniques to be used in special occasions to detect traps. A photoluminescence mapping technique is used in Chapter 6 to study the LID effect in single and multi-crystalline silicon.

2.3.1.2 Radiative Band-to-Band Recombination

Radiative recombination in silicon solar cells is often neglected because of its indirect bandgap structure. A phonon-assisted recombination event is often required for electrons in the conduction band, E_c, to recombine with the holes in the valence band. Since it takes three quantum particles to consummate the recombination event, it is a slow process for indirect bandgap materials, like silicon. The radiative lifetime, τ_R, is given by

$$\tau_R = \frac{1}{B(n_o + p_o + \Delta n)} \tag{15}$$

where the band-to-band recombination coefficient B is 1×10^{-14} cm^3/s for crystalline silicon at 300 K [6]. The radiative lifetime in silicon is essentially constant below 10^{18} cm^{-3} injection level. This is an important fact used by the photoluminescence mapping technique discussed in Chapter 6.

2.3.1.3 Auger Recombination

Auger recombination occurs when an electron in the conduction band recombines with a hole in the valence band and transfers its energy to another electron in the conduction band in heavily doped n-Si (or a hole in the valence band for heavily doped p-Si) that subsequently settles to the band edge by releasing phonons. Auger recombination is dominant at high injection levels ($>10^{17}$cm^{-3}) or in heavily doped regions. Auger lifetime is described by

$$\tau_{Aug} = \frac{1}{c_n n^2 + c_p n \Delta n}; or = \frac{1}{c_p p^2 + c_n p \Delta n} \tag{16}$$

for n-type or p-type respectively [6,8-9]. For terrestrially operated one-sun solar cells, Auger lifetime is not important in the bulk or base of the device; however, it is dominant in the emitter and back surface field (BSF) regions.

2.4   Surface Recombination

In addition to the bulk recombination via the three mechanisms mentioned above, carriers also recombine at the surface. At the surface of a semiconductor crystal, the bond structure is altered and the largest disturbance in the symmetry of the lattice is often observed. A large number of dangling bonds exist and give rise to surface states that act as traps in the forbidden gap, as in SRH bulk defects discussed earlier. Surface states are treated in the same manner as SRH traps but are present only on a two-dimensional plane. Instead of a recombination lifetime for minority and majority carriers, a recombination velocity results from the fact that the surface states exist in two dimensions. The equation governing surface recombination velocity for a single trap (designated by n_1 or p_1) is given by

$$S \cdot \Delta n_s \equiv U_s = \frac{S_{no}S_{po}(n_s p_s - n_i^2)}{S_{no}(n_s + n_1) + S_{po}(p_s + p_1)} \tag{17}$$

S is the surface recombination velocity, Δn_s is the excess minority concentration at the surface, S_{no} and S_{po} are surface recombination parameters for electrons and holes, and n_s and p_s are the electron and hole concentrations at the surface [6]. The effective lifetime given by the parallel contribution of four mechanisms for a given cell width (W) is described by

$$\frac{1}{\tau} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_B} + \frac{1}{\tau_{Aug}} + \frac{2S}{W} \tag{18}$$

To properly characterize and analyze surface parameters, the background information must be known because S is affected by the doping concentration, surface orientation (100) or (111), dopant type, diffusion, texturing, and chemical or dielectric passivation. Surface passivation is accomplished in two ways: i) by reducing the number of surface states through deposition or growth of a passivating film (or submersion in a polar liquid)

or ii) by using field effect passivation that drastically reduces the number of electrons or holes at the surface, thereby limiting recombination because both carriers need to be present. Two of the most successful passivating films for crystalline silicon are a deposited SiN_x film and a thermally grown SiO_2 layer. The metastable defect responsible for light induced degradation has not been detected by direct electrical measurement using DLTS. Therefore, lifetime spectroscopy has become a very powerful tool in characterizing the trap. Using Shockley-Read-Hall theory and measured effective lifetime data, a much better understanding of the trap has been achieved.

CHAPTER 3

3 A REVIEW OF TEXTURING MULTI-CRYSTALLINE SILICON SOLAR CELLS

The current density and efficiency of industrial solar cells fabricated on mc-Si substrates can be improved further by an effective texture that provides additional light trapping and reduces the reflectance. The random crystalline grain orientation on the surface of mc-Si samples does not allow for conventional alkaline (NaOH or KOH) etches to successfully texture the entire wafer surface. In addition, an effective surface texture on low-cost PV grade silicon can allow lower bulk lifetimes in mc-Si cells without sacrificing efficiency. An additional consideration for the texturing method used for the mc-Si samples is the impact on module cost and production through-put. In this chapter, some of the promising texture methods are briefly reviewed, including the low-cost porous silicon etching technique used in this thesis.

3.1 Challenges in Texturing Multi-Crystalline Silicon

Some general prerequisites for texturing mc-Si samples for industrial adaptation require that the method be effective on all crystalline grain orientations, be able to withstand subsequent processing, allow for screen-printed metallization, and justify any increased cost with efficiency improvement. Three of the more promising techniques currently being researched are acidic etching (including porous silicon), mechanical grooving by wafer sawing, and reactive ion etching (RIE) involving dry processing in a plasma machine. Each technology offers unique aspects toward efficiency improvement.

Texturing in general offers the potential for increased light absorption by changing the angle of incidence of incoming light. If the light is not absorbed at the initial surface, it is reflected toward another part of the substrate so it gets a second chance at being absorbed, the so-called "double bounce" effect. In addition, total internal reflection under encapsulation is increased by a very slight texture. Using Snell's law with Figure 5,

$$n_1 \sin \theta_1 = n_2 \sin \theta_2 \tag{19}$$

where n_1 is the refractive index of medium 1 (the encapsulation layer $n_1=1.5$), n_2 is the refractive index of medium 2 (air with $n_2=1$), θ_1 is the incident angle, and θ_2 is the transmission angle. Recognizing θ_1 as twice the texture angle (i.e., the texture angle = $\theta_1/2$) and setting θ_2 equal to 90°, total internal reflection conditions are met for a encapsulated solar cell at texture angles greater than 21° from horizontal, see Figure 5. A very slight texture will cause total internal reflection.
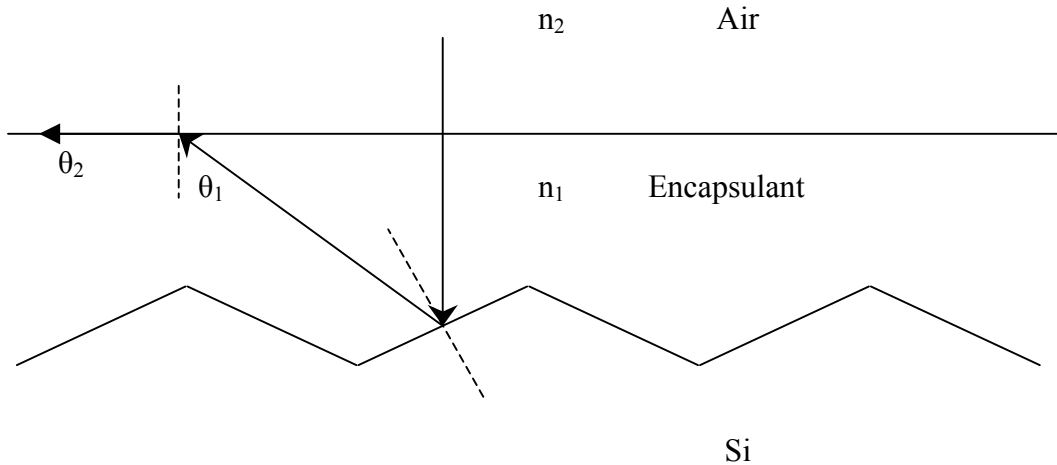
Figure 5. Total internal reflection schematic for a textured solar cell.

Each texturing method described below offers control over particular surface structure features but **the true challenge for incorporation of surface texturing is the development of an industrially viable process sequence that includes textured mc-Si**.

3.2   Reactive Ion Etching

Reactive Ion Etching of Si typically involves either chlorine- or fluorine-based plasma etching. By controlling the kind of gas, the gas ratios, the RF power, the reactor pressure, and so on, a single or mc-Si surface can be etched with homogeneous pyramid- like structures [10]. Very low surface reflectance can be achieved by tailoring the aspect ratio of the feature sizes etched into the silicon surface, resulting in so-called "Black Silicon." Figure 6 shows scanning electron microscopy (SEM) images of various RIE textured surfaces with different Cl_2 flow ratios. The silicon wafers are immersed directly into the chlorine plasma. Inomata et al found that as the surface structure size increased so did the solar cell dark saturation current [10]. The increased dark saturation current results in a lower open circuit voltage, as described by eq. (8). However, the surface reflectance decreased, providing the potential for higher current collection. Therefore, a proper balance between reduced reflection and decreased V_{oc} required process optimization.
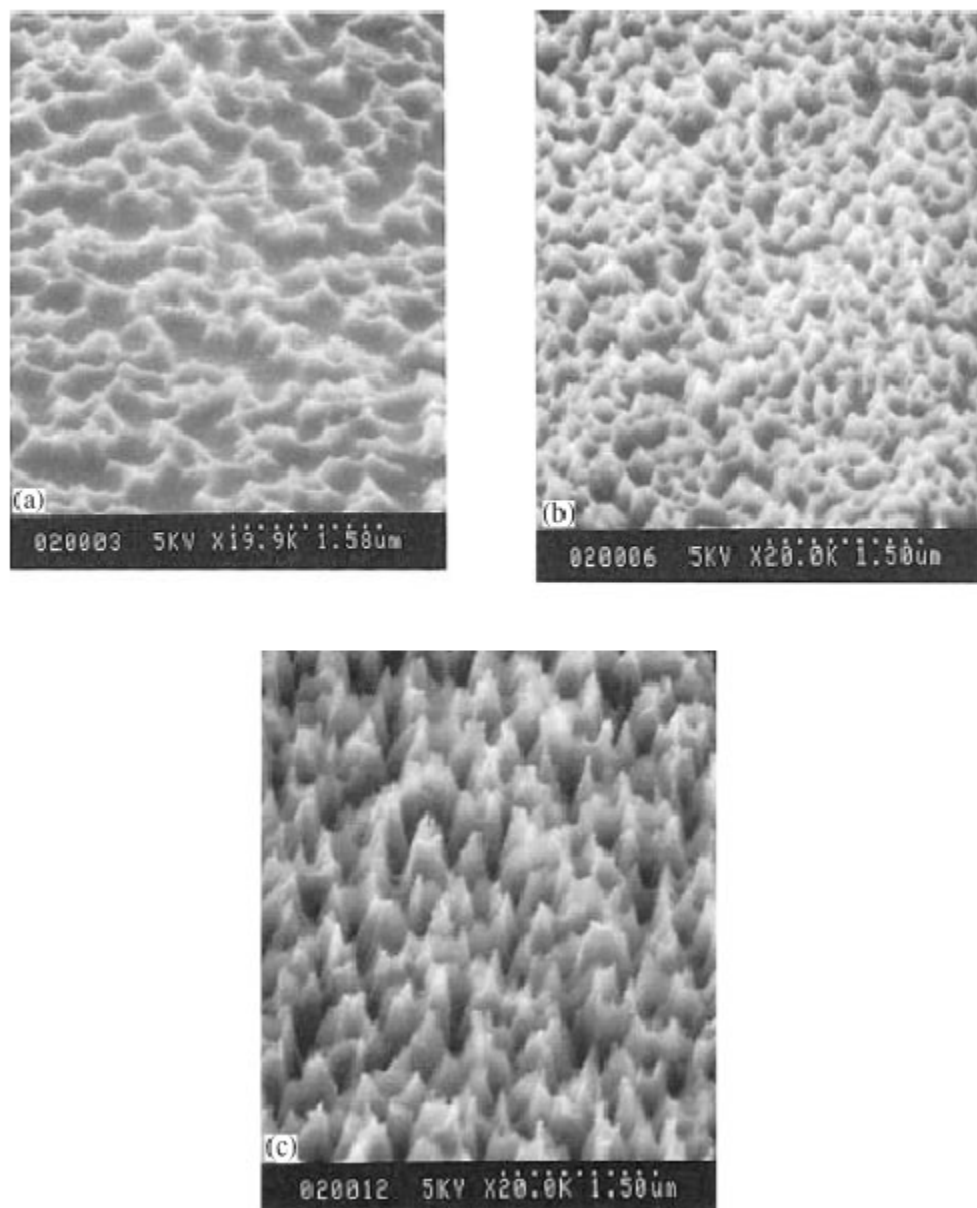
Figure 6. SEM pictures of RIE-textured material with different Cl_2 flow ratios.

RIE etched surfaces commonly suffer from increased surface damage and often require special processing techniques that do not destroy or remove the texturing while simultaneously providing for solar cell fabrication. Inomata et al achieved a 17.1% efficient large area (225 cm^2) mc-Si solar cell using photolithography techniques and laboratory processing.

Damiani et al used industrial screen-printed contacts on RIE-textured wafers treated with different damage removal etches. A maskless SF_6/O_2 plasma process using reactive ion etching was developed at Sandia National Laboratories. Table 1 shows efficiency data prior to any anti-reflection coating application. RIE-textured solar cells showed up to a 33% increase in efficiency over planar devices. Table 2 shows that after SiN deposition, an additional 1% absolute efficiency was gained (or 8% relative efficiency improvement) with a maximum efficiency of 13.7%, thus effectively demonstrating the potential for increased efficiency by incorporating RIE texturing. Figure 7 shows the resulting reflectance for various RIE-textured samples. Very low reflectances across the entire wavelength range (300-1200 nm) were demonstrated. Figure 8 shows the external quantum efficiency for the same RIE-textured cells. The external quantum efficiency measures the percentage of incident photons successfully collected by the solar cell.

Table 1. I-V data for RIE multi-crystalline solar cells.

Wafer Treatment	Voc (mV)	Jsc (mA/cm^2)	FF	η	Increase
planar controls	574	22.20	0.759	9.7	**0%**
conditioned texture 20 sec nitric	566	23.43	0.733	9.7	**0%**
Al-assisted 20 sec nitric	560	27.02	0.695	10.5	**9%**
Cr-assisted 8-min KOH	576	24.77	0.756	10.8	**11%**
conditioned texture ~ 20-25 sec nitric	577	25.12	0.748	10.8	**12%**
Al-assisted 15-sec nitric,	573	25.83	0.739	10.9	**13%**
conditioned texture 15 sec nitric	582	26.96	0.748	11.7	**21%**
conditioned texture 10 sec nitric	578	27.14	0.748	11.7	**21%**
Cr-assisted no DRE	583	29.18	0.756	12.9	**33%**

Table 2. I-V data for SiN coated solar cells.

Wafer Treatment	Voc (mV)	Jsc (mA/cm^2)	FF	η	Increase
planar controls	584	28.25	0.772	12.7	**0%**
conditioned texture 20 sec nitric	575	28.93	0.757	12.6	**-1%**
conditioned texture 10 sec nitric	587	30.84	0.751	13.6	**7%**
Cr-assisted, No DRE	591	30.63	0.759	13.7	**8%**
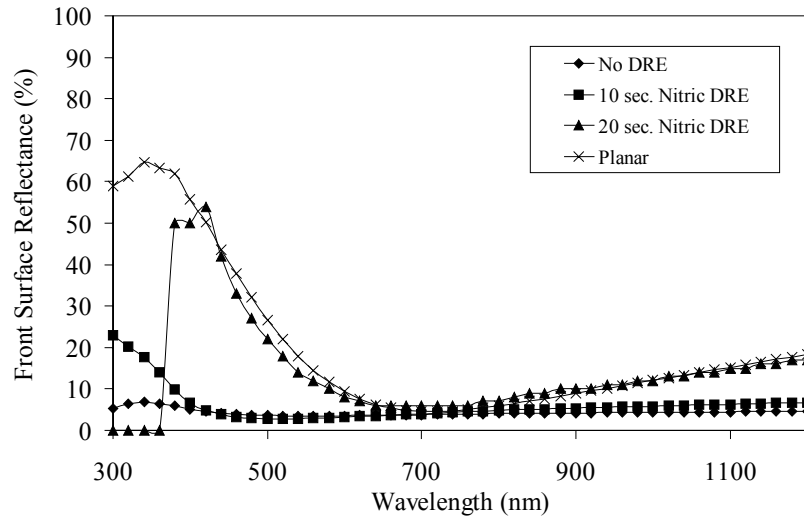
Figure 7. Front surface reflectance curves for RIE textured + SiN ARC on multi-crystalline solar cells with varying damage removal etching schemes applied.
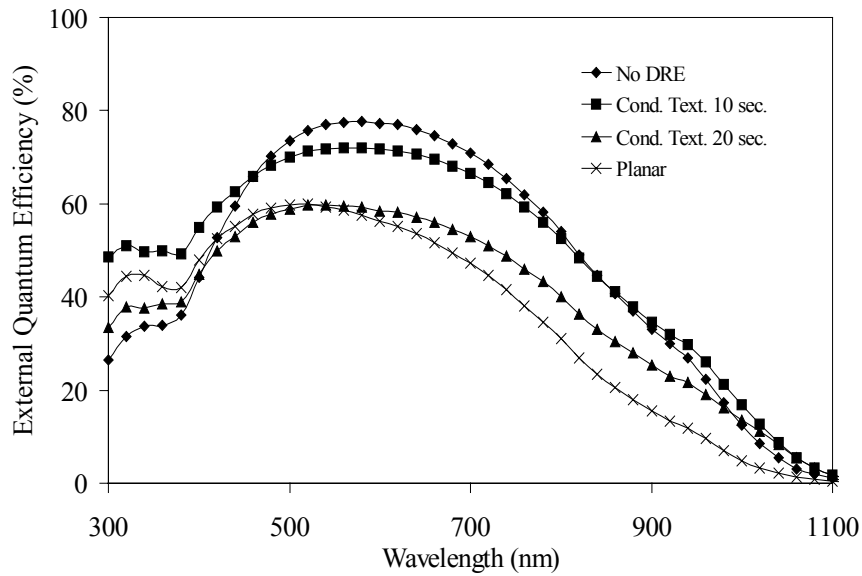
Figure 8. External quantum efficiency of RIE textured samples with different damage removal etches applied.

RIE offers the potential for an effective surface texture for mc-Si solar cells but requires some processing constraints in addition to the use of plasma machines. The capital investment required to purchase, maintain, and operate a RIE plasma machine has restricted widespread implementation. In addition, vacuum processes tend to be time intensive and could potentially reduce throughput. Only one company, Kyocera, uses RIE to make mc-Si cells in production. A more simplified approach, described next, involves mechanical grooving to form surface texturing on mc-Si wafers.

3.3 Mechanical Grooving for Surface Texturing of mc-Si Solar Cells

The mechanical grooving technique uses stacked saw blades to groove V-shaped trenches on the mc-Si surface with 3 to 4 μm tall feature sizes. Figure 9 shows a schematic drawing of the mechanical grooving technique, along with a resulting surface structure [11]. A process sequence based on screen-printed contacts fired through SiN resulted in 16.6% efficiency on a 100 cm^2 mechanically grooved mc-Si substrate [12], again demonstrating the high efficiency potential for textured mc-Si solar cells. However, mechanically grooved wafers are highly stressed and therefore are not suitable for all types of mc-Si wafers, especially thin substrates. In addition, mass production of screen-printed contacts directly on a mechanically textured surface presents additional challenges in achieving good fill factors and a low contact resistance.
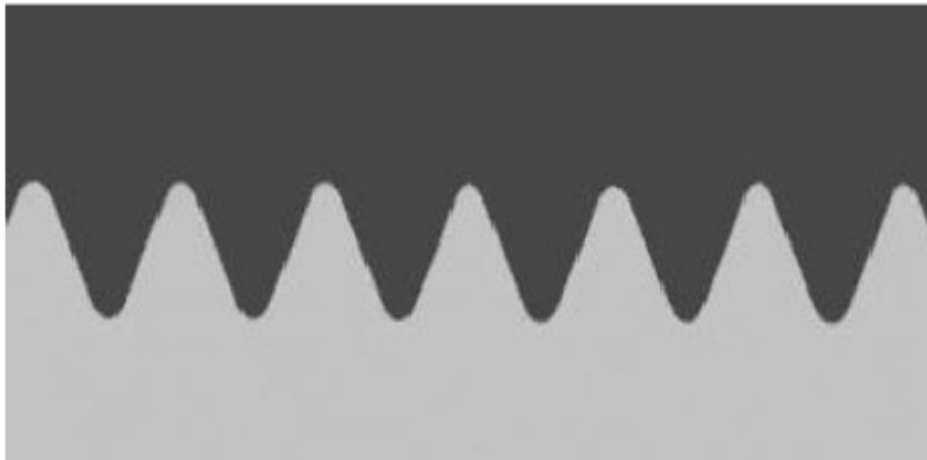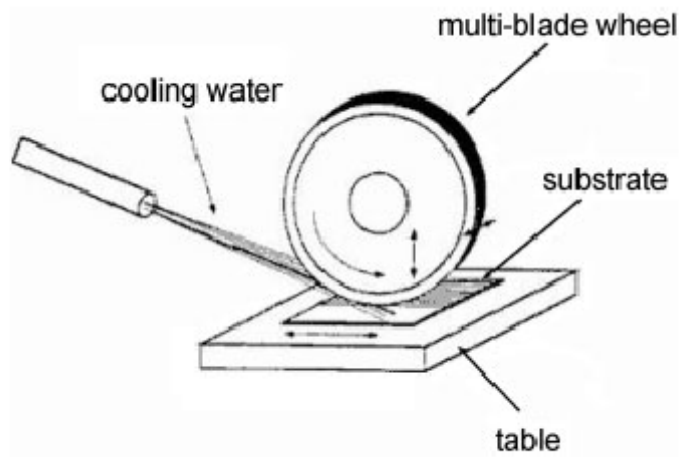
Figure 9. Multi-blade V-grooving technique and resulting surface structure with feature size from trench to peak of 3 to 4 μm.

3.4 Chemical Etching for Surface Texturing of Multi-Crystalline Wafers

Chemically etched samples generally fall into two categories: acidic and alkaline. Alkaline etches are typically used for single crystal materials and preferentially etch in the (111) direction, resulting in pyramid formation for (100) oriented surfaces. Acidic etches are typically not sensitive to surface morphology and can be used on mc-Si surfaces. In some methods, photolithography techniques are used to assist in surface texturing. However, photolithography approaches are not feasible for mass production and therefore are not discussed in this thesis.

3.4.1 Conventional Methods

Acidic isotropic etching techniques have become increasingly popular and have been shown to contribute only 0.02-0.03 \$/Wp to total cell fabrication costs [13]. However, only wire saw cut wafers can be successfully etched with the technique based on an aqueous solution of nitric acid, hydrofluoric acid, and some "additives" for wetting purposes. Currently, more than 80% of the crystalline silicon wafers are produced by wire sawing methods. Therefore, this constraint does not seem so detrimental. Figure 10 shows an SEM view of an isotropically acid etched mc-Si surface. The feature size of the texturing results in pits of 1 to 10 μm in diameter, which are uniformly distributed over the silicon surface regardless of grain orientation.
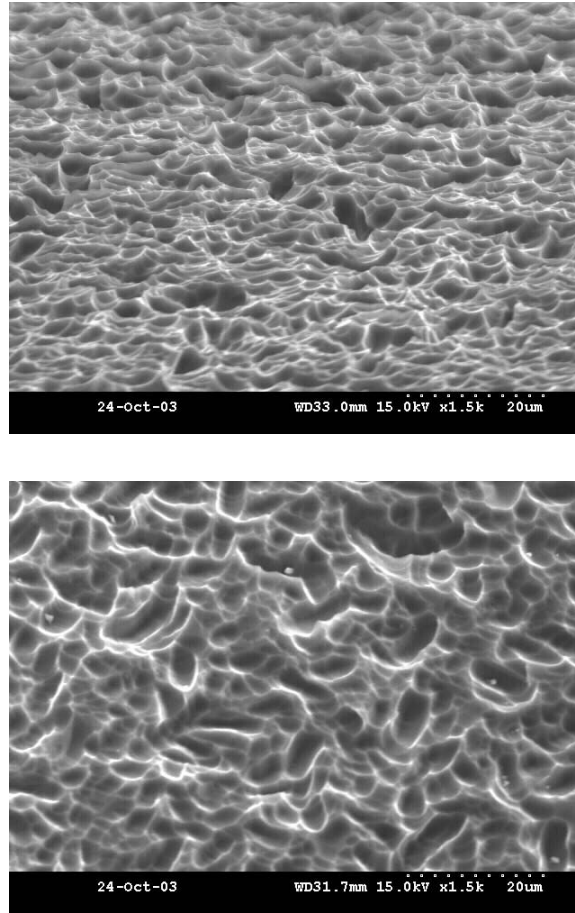
Figure 10. SEM image of isotropic acid texture on a mc-Si surface. Bottom picture is normal to the surface. The top picture is a view of the surface at a slight angle.

The acids used in the isotropic etching are similar to the acids used in the "stain etched" porous silicon technique [14]. Porous silicon etching is applicable to all crystal types but results in poor surface passivation and has a high absorption coefficient for short wavelength photons [15]. These issues are directly addressed in Chapters 7 and 8.

3.4.2 Discovery of Porous Si Formation

Porous silicon was discovered in 1955 by Uhlir while trying to use an electrolytic solution to polish silicon and germanium semiconductor wafers [16]. In the absence of an external stimulus via either illumination or electrical bias, silicon wafers practically do not dissolve in hydrofluoric acid. However, once a current flows through the silicon/electrolyte interface or when light of sufficient energy/wavelength is incident on the silicon/electrolyte interface, etching occurs. The dissolution takes place in the presence of holes (h^+) on the wafer surface that are then attacked by negatively charged fluorine ions [17]. In the case of current flow through the silicon wafer, the reaction is accomplished by making the silicon wafer the **anode,** and thus positive charge can be delivered to the wafer surface by increasing the current flow. This is often referred to as **anodization**. Depending on the current density, either electro-polishing or porous etching is achieved. Low current density acts to limit the hole injection at the surface of the Si anode and therefore only localized pits are formed, resulting in a "porous" silicon surface. If a high enough current density is used, the surface is saturated with holes and polishing occurs.

3.4.3 *Porous Silicon Anti-Reflection Coatings*

Porous silicon etching allows refractive index modulation and surface texturing simultaneously. Thus, the application of both surface texturing and anti-reflection coating during the same processing step is possible. This means that the application of a SiN coating can be omitted as a processing step. This would simplify the process sequence and reduce the capital expenditure required to purchase a SiN plasma machine.

The chemical solution used to form the porous silicon layer is comprised of various ratios of aqueous 70wt% HNO_3 in H_2O and 50wt% HF in H_2O. The same mechanism of Si dissolution occurs during chemical formation of porous silicon as in the electrochemical method. Similar to anodic etching (electrochemical), the key component of porous silicon formation in the chemical (or stain etched) method is the generation of holes (h^+) at the wafer surface. This is accomplished chemically by eq. (20), where the NO is produced and serves as the h^+ injector to initiate the following reaction:

Cathode: $\quad HNO_3 + 3\,H^+ \rightarrow NO + 2\,H_2O + 3\,h^+$ $\hfill (20)$

Anode: $\quad n\,h^+ + Si + 2\,H_2O \rightarrow SiO_2 + 4\,H^+ + (4\text{-}n)\,e^-$ $\hfill (21)$

$\quad\quad\quad\quad SiO_2 + 6\,HF \rightarrow H_2SiF_6 + 2\,H_2O$ $\hfill (22)$

Overall: $\quad 3\,Si + 4\,HNO_3 + 18\,HF \rightarrow 3\,H_2SiF_6 + 4\,NO + 8\,H_2O$

$\quad\quad\quad\quad\quad\quad\quad\quad + 3\,(4\text{-}n)\,h^+ + 3\,(4\text{-}n)\,e^-$ $\hfill (23)$
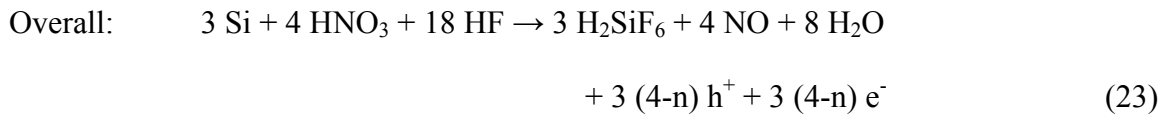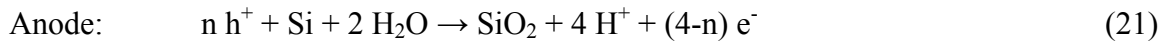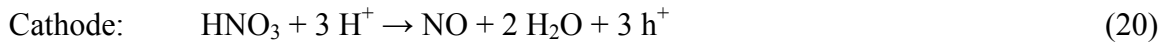
where e^- is an electron and n is less than 4. The structural characteristics of porous silicon, and especially stain etched porous silicon, are difficult to obtain. Electron microscope methods are too destructive and therefore require other morphology determining tools such as atomic force microscopy (AFM). Through transmission electron microscopy (TEM) some of the feature sizes associated with stain etched films have been determined: 40 nm pore sizes with micro-crystals of 1.5-10 nm [15]. Porosity and layer thickness are affected by the solution concentration. Investigations of the optical properties of porous silicon involve various effective medium approximations. However, in this thesis, optical characteristics were defined by reflectance measurements from an integrating sphere and in some special cases a 632.8 nm laser ellipsometer was used. In addition, naked eye observations were also a strong optical characterization tool.

Porous silicon is known to change colors according to surface thickness and porosity and therefore provided an additional optical characterization tool. Figure 11 shows a mc-Si solar cell with a porous silicon anti-reflection coating and photolithography contacts. A very uniform color distribution was observed with blue-violet coloring.

Incorporating porous silicon anti-reflection coatings into crystalline silicon solar cell processing methods offers the promise of simultaneously texturing mc-Si surfaces while changing the refractive index to also serve as an anti-reflection coating. Many exciting device structures are possible, including porous silicon hetero-junction solar cells, as well as the potential for using light filtering through the use of the photoluminescence properties of porous silicon [18]. Ultra-violet light is absorbed in the porous silicon layer and is re-emitted as visible light, which is more readily converted into useful energy by
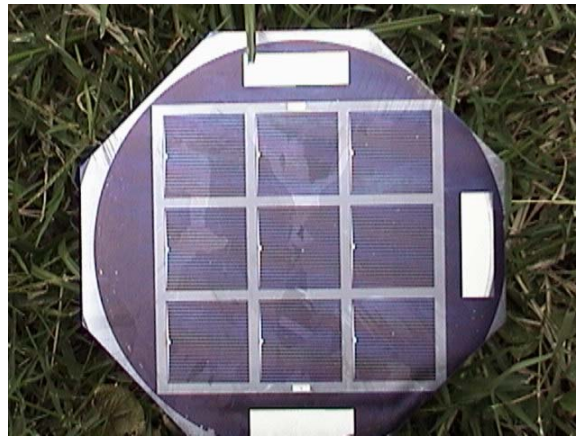
Figure 11. A porous silicon etched mc-Si solar cell fabricated using photolithography contacts. No dependence on grain orientation and the color uniformity was good to the naked eye.

silicon solar cells. However, the focus of this thesis is to develop a simple technique

using a rapidly formed porous silicon layer to serve as an anti-reflection coating for a typical crystalline silicon industrial solar cell structure. Typical emitter profiles, industrial screen-printing, and conventional furnaces were used. Before process development started, a current understanding and knowledge of porous silicon etched solar cells provided a basis for both positive and negative effects of porous silicon etching. The typical process sequence for porous silicon etched solar cells, prior to this thesis, involved implementing porous silicon as a final step in the process sequence. This thesis addresses the challenge of fabricating high efficiency porous silicon etched solar cells without the need for a SiN anti-reflection coating (ARC) using a novel diffusion technique developed at Georgia Tech and the formation of porous silicon prior to the diffusion process.

3.4.4 Porous Silicon Texturing and Anti-Reflection Coating for Multi-Crystalline Silicon Solar Cells

Si material accounts for more than 50% of the module cost. Therefore, reducing wafer thickness can have a significant impact on the cost of Si PV. In addition, a combination of surface texturing and good back surface recombination velocity can produce higher efficiency on thin materials and give a much tighter efficiency distribution with respect to variation in material quality or bulk lifetime.

Reducing the cost and improving the efficiency of solar cells is the focus of this research. By moving to thinner wafers with relaxed restrictions on purity and grain orientations,

significant cost reductions are possible. Porous silicon formation is rapid and essentially free of capital investment cost. If porous silicon induced ARC and texturing can enhance light trapping for thin silicon cells, it could help increase the throughput and performance while reducing the cost of solar cells. By using thinner wafers (~100 to 200 μm) with good back surface fields, additional increases in efficiency can be achieved because of the greater effective diffusion length to device thickness ratio. Random grain orientation in multi-crystalline Si does not allow for conventional isotropic alkaline texturing involving NaOH etching to be effective. However, porous silicon etching can overcome this problem. There are two ways to form porous silicon: electrochemically or by straight chemical etching (frequently referred to as "stain etched" porous silicon). Electrochemical porous silicon etching is somewhat more controllable but slightly more complex. Stain etching for porous silicon formation is more manufacturable and requires less manual preparation. This provided the motivation for developing and investigating stain etched PS layers for Si solar cells.

Szlufcik et al. assessed the impact of manufacturing cost for various module efficiencies to determine the cost per watt value ($/Wp), frequently used by industry to compare the cost of conventional energy sources with solar power (Table 3) [13]. Solar cell module cost must reach $1/Wp to directly compete with current energy sources in the United States. For example, if a manufacturing cost per m^2 of a solar module were $200, a solar module efficiency of 18% would be needed to reach $1.11/Wp. By implementing porous silicon ARC to offset the cost of other ARC technologies, a cost reduction can be realized. It is estimated that a porous silicon ARC would add 0.02 to 0.03 $/Wp but

Table 3. Impact of efficiency and direct manufacturing cost
for crystalline silicon technology cost [$/Wp].

Cost Eff.	350 $/m^2	300 $/m^2	250 $/m^2	200 $/m^2	150 $/m^2
10%	$3.50	$3.00	$2.50	$2.00	$1.50
12%	$3.00	$2.50	$2.08	$1.67	$1.25
15%	$2.33	$2.00	$1.67	$1.33	$1.00
18%	$2.05	$1.67	$1.39	$1.11	$0.83

could give ~40% increase in efficiency without the need for a SiN_x or TiO_2 anti-reflection coating [13].

The need for thinner solar grade materials poses additional challenges on high efficiency processing. Most single crystal Si wafers are grown with (100) orientation to allow isotropic texturing of the surface to improve light trapping and reduce the front surface reflectance. However, many promising low-cost silicon technologies produce multi-crystalline (mc-Si) structures with crystal grains that vary in size and crystal orientation. Alkaline isotropic texturing does not properly etch the mc-Si surface because of random grain orientation. A great deal of research has focused on the implementation of a surface texture for mc-Si that is industrially viable. Taking into consideration wafer yield of thin mc-Si, the mechanical grooving technique does not seem suitable for all mc-Si wafers because of various surface morphologies and rigidity. RIE involves a vacuum process that tends to slow throughput. Porous silicon formation is simple and is accomplished by either electrochemical or chemical etching but is still not completely

understood or developed for PV. Porous silicon offers a low-cost and high through-put route to surface texturing and can also serve as an anti-reflection coating. This provided the motivation to understand and develop low-cost manufacturable porous silicon etching for crystalline Si cells.

3.4.5 Applications and Limitations of Porous Silicon for Solar Cells

The use of porous silicon for solar cells offers great potential along with some challenges. The most widely applied features of porous silicon for solar cell applications include anti-reflection coating (ARC), surface texturing, and surface passivation via hydrogen termination and/or bandgap discontinuity [19]. The potential applications range from complete porous silicon solar cell structures to enhanced light absorption via energy filtering ultra-violet light to visible light [20]. Another potential application of porous silicon in photovoltaics is a device design based on a heterostructure bandgap.

Porous silicon also offers potential for cost reduction through low-cost ARC applications as well as increased through-put. So far, the use of porous silicon for ARC has been the most widely investigated. The typical process sequence for an industrial type solar cell using porous silicon is shown in Figure 12. Traditionally, the porous silicon etch has been implemented after junction formation and metallization. This approach can lead to

Wafer Clean	
Emitter Diffusion	
Phosphorus Glass Removal	
Screen Printed Aluminum BSF Formation	
Screen Printed Front Contact	
Porous Silicon Etching	
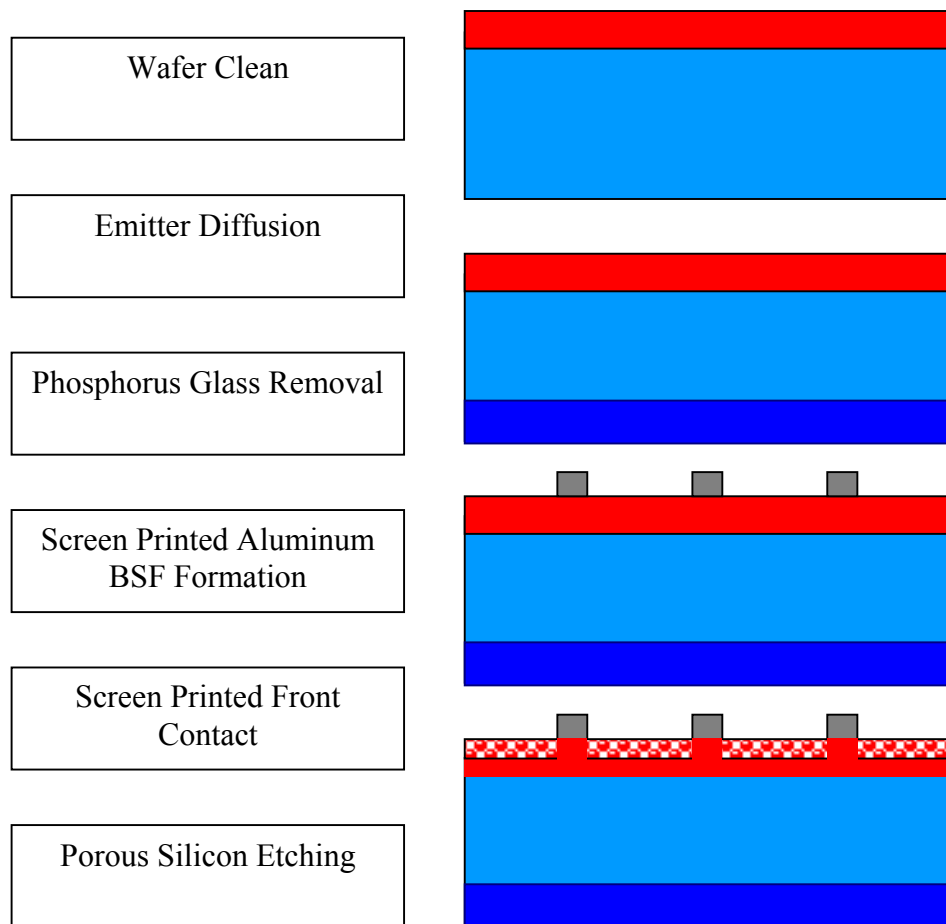
Figure 12. Typical process steps for a porous silicon ARC solar cell.

selective emitter formation, proper surface reflectance, hydrogen surface passivation, and good electrical contact [21].

However, there are some major drawbacks of the porous silicon etch at the end of the solar cell process. The PS etch attacks the screen-printed metal contacts and results in FF degradation and a high surface recombination velocity [20]. In addition, a heavily diffused emitter with a junction depth of ~1.0 μm is necessary to avoid destruction of the emitter during porous silicon etching. The highly reactive surface causes concern over the longevity of the solar cell in the field. This provided the motivation to *develop a novel process that involves porous silicon formation at the start rather than at the end of solar cell processing*.

Initial investigations of porous silicon ARCs and surface passivation were made in the mid 1990s. Although early work cited the effectiveness of a very thin porous layer (< 0.1 μm) to reduce the reflectance from 37% on bare Si to 8% [22]. It was shown that etching time, porosity, current or HNO_3 concentration, and layer thickness control the reflectance of porous silicon. Many investigations claimed various R_w values for chemical and electrochemical etching methods [20,21]. Some groups obtained better reflectance values using the electrochemical process than with the chemical or stain etch process. However, this trend is not replicated in all studies. Figure 13 shows some reflectance curves in the wavelength range of interest. The R_w of a bare silicon sample can be reduced from ~37% down to ~5 to 6% [21]. It can be comparable to the R_w achieved by a double layer ARC of ZnS + MgF_2, which is the premium coating in solar cell processing. Although the
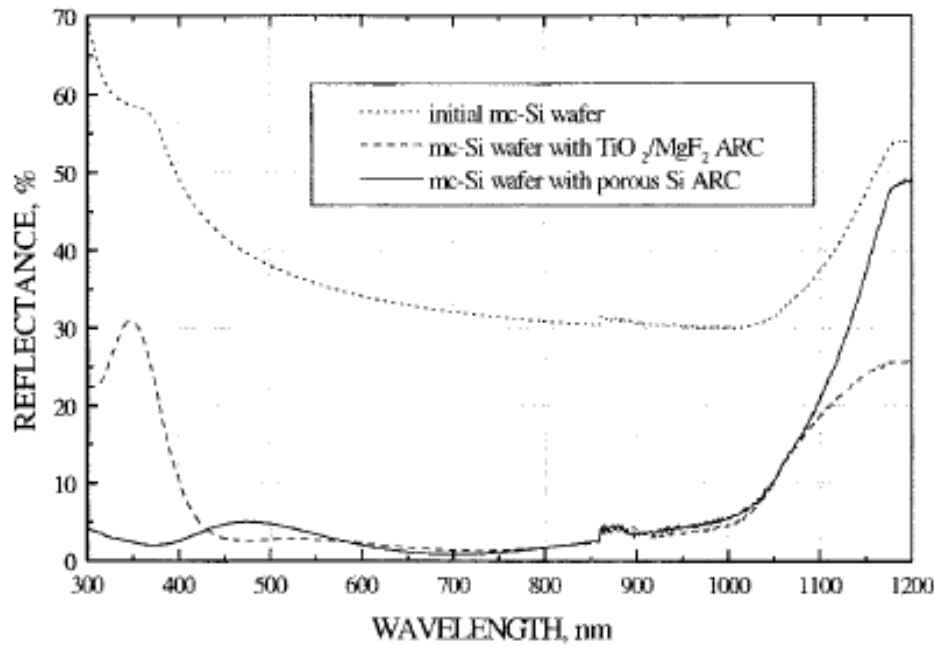
Figure 13. Reflectance characteristics of non-textured mc-Si wafer after
PS formation by stain etching and pre-textured mc-Si wafer with DLARC.

reflectance values that can be achieved are among the very best possible, there are some

additional considerations that arise with the use of porous silicon. If porous silicon is

formed early in a solar cell process, the high temperature endurance needs to be

considered, as well as the junction formation technique used for a uniform diffusion.

Figure 14 shows the progress in efficiency of Si cells using porous Si texturing. A

conversion efficiency of 14.1% (25 cm^2) on a large area mc-Si sample was achieved with

evaporated contacts [21]. It was shown that the photocurrent (J_{sc}) increased ~40% and

the open circuit voltage improved by 4 to 6 mV over a bare silicon surface. No FF

degradation was observed because evaporated contacts were used in conjunction with the

relatively short etch time (< 4s). The improved J_{sc} was attributed to ARC and removal of

heavy doping effects that cause photo-generated carriers to recombine in the emitter because of Auger mechanisms before being collected.
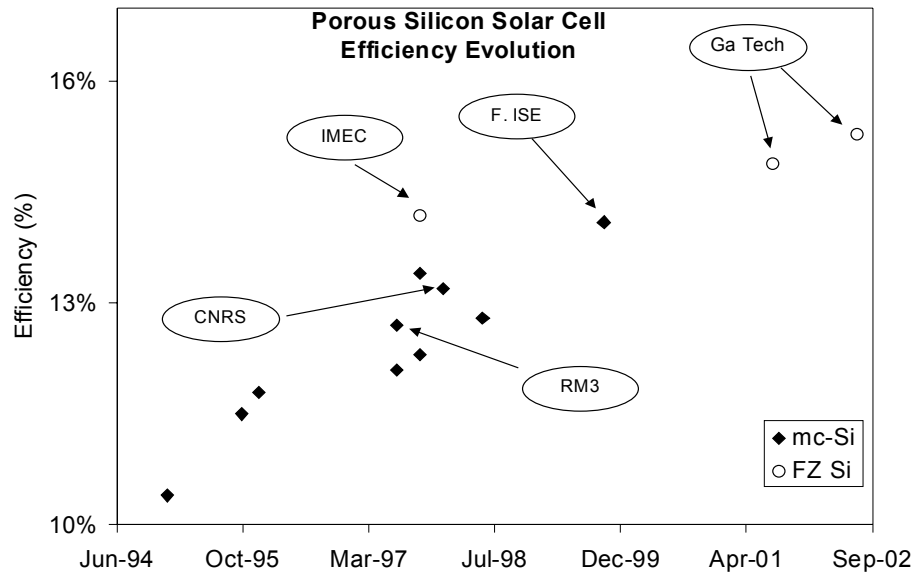
Figure 14. Efficiency evolution for all solar cells using porous silicon as part of the solar cell design [33,39].

Most investigations implement porous silicon as a final step in the process sequence. This is to take advantage of the selective emitter formation in addition to surface texture and ARC (See Fig. 12). Unfortunately, the porous silicon etch attacks screen-printed metal contacts, resulting in lower device performance along with a highly reactive surface. Matic et al. [23] tried porous silicon etching prior to screen-printed metallization in an effort to achieve a more stable surface, with no contact degradation. They showed that porous silicon ARC quality was not greatly altered during the screen-printed metal firing step at 800-900°C [23], thus demonstrating a new possibility for ARC and contact

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preservation. A major drawback for such a process sequence may arise because of the possibility of the extremely high series resistance of the porous silicon layer underneath the contacts, which translates into low FF (high series resistance) and reduced cell efficiency.

Based on the literature search, the advantages and disadvantages of industrially viable silicon solar cells with porous silicon ARC are summarized below.

Potential Advantages:

1. Porous silicon texturing does not depend on crystallographic orientation. Therefore mc-Si of all kinds can be textured.

2. The ARC can be optimized by tailoring the porosity (or refractive index) of the porous silicon layer for a given cell structure.

3. Porous silicon etching allows for selective emitter formation to improve the short wavelength (300 to 500 nm) response.

4. Partial shaving of the heavily diffused emitter region reduces heavy doping effects during porous silicon etching.

5. Porous silicon serves as an effective light diffuser with an effective light entrance angle of 60° [17] that could improve collection efficiency of photo-generated carriers.

6. Good surface passivation may be achieved by hydrogen terminated surface states (Si-H stretching mode) [17] or through band-edge discontinuity resulting from higher bandgap of porous silicon.

7. Porous silicon formation is simple and industrially scalable.

8. Using a porous silicon anti-reflection coating instead of the traditional SiN layer saves a significant amount of time and avoids the cost associated with a plasma deposition machine.

9. The formation of the porous silicon layer allows for higher through-put (<10 seconds).

Potential Disadvantages:

1. The porous silicon etch attacks screen-printed contacts, resulting in a lower FF and decreased efficiency.

2. A deeper emitter diffusion is required to avoid shunting and junction removal during etching. To achieve > 0.65 μm phosphorus diffusion, more time at a high temperature is needed, potentially reducing through-put.

3. Porous silicon etching as the final processing step does not allow for surface passivation.

4. If porous silicon is formed after emitter diffusion and before metallization, a high series resistance is realized because of the porous silicon layer.

5. Porous silicon etched surfaces do not withstand conventional phosphorus diffusion and glass removal. Therefore, the use of porous silicon anti-reflection coatings must be formed after the phosphorus emitter diffusion.

6. The implementation of porous silicon ARC as the final processing step could result in the loss of device performance and reproducibility.

7. There are appreciable absorption losses in porous silicon layers as a result of direct bandgap behavior that decreases the short wavelength response (300 to 500 nm) [24].

The work in this thesis described in Chapters 7 and 8 focuses on eliminating the potential disadvantages associated with porous silicon etching while accentuating the potential capabilities of enhanced light trapping. Thus, an alternative ARC to the conventional plasma deposited SiN layer typically used in industry is developed.

CHAPTER 4

4   REVIEW OF LIGHT INDUCED DEGRADATION IN CZOCHRLASKI SILICON SOLAR CELLS

4.1   Industrial Solar Cells

The goal of PV cell manufacturers is to reduce the cost and increase the efficiency of solar cells. Typically, this is accomplished by using low-cost photovoltaic grade silicon, including single crystalline Czochralski and various types of multi-crystalline silicon. In addition, the cell design commonly incorporates a p^+ back surface field (BSF), a heavily diffused emitter (45 Ω/sq. with 0.3-0.5 μm deep junction), a single layer SiN anti-reflection coating, and screen-printed contacts (Figure 15). PV grade silicon substrates typically suffer from low initial bulk lifetimes (1 to 5 μs) that can be improved (20 to 100 μs) during solar cell processing. This involves effective gettering and defect passivation techniques. However, light induced degradation can lower the bulk minority carrier lifetime to eliminate the positive effects of cell processing. Another efficiency limiting mechanism for low-cost multi-crystalline industrial solar cells is the absence of light trapping because conventional alkaline isotropic texturing is not effective. The focus of this thesis is to a) offer cost effective solutions to achieve and maintain higher efficiencies on low-cost silicon materials by incorporating a texturing method that is not limited to single crystal silicon and b) investigate methods to reduce or eliminate LID to improve the stabilized efficiency of devices.

Screen –Printed Solar Cell

Screen –Printed Solar Cell
Band Structure
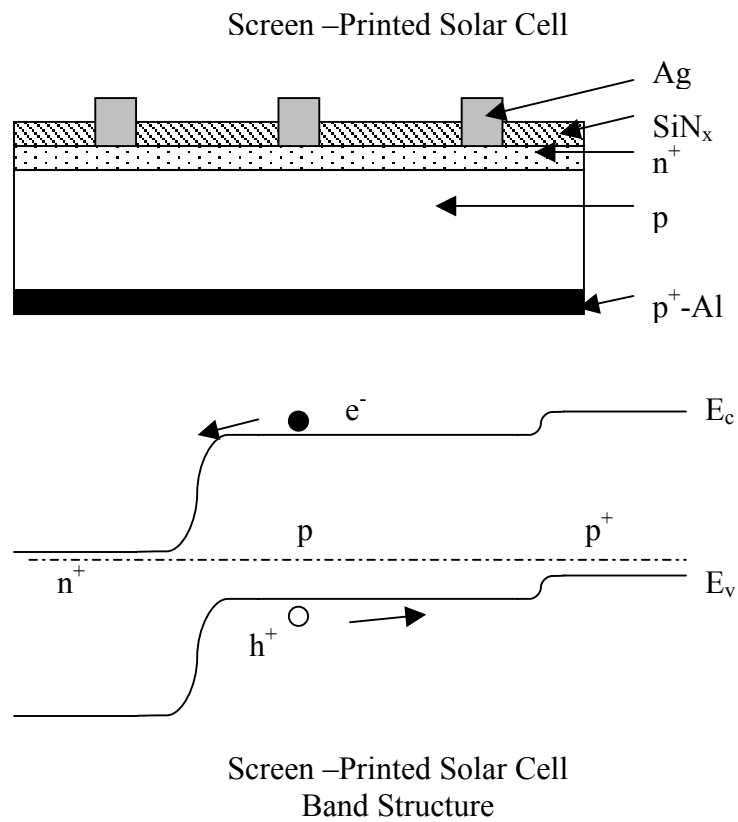
Figure 15. Schematic of industrial solar cell structure and associated
energy band diagram.

4.2 Light Induced Degradation in Czochralski Silicon Solar Cells

4.2.1 Understanding of Light Induced Degradation and its Behavior

R.L. Crabb first observed Light Induced Degradation (LID) in 1972 while investigating UV degradation of the coverslip for space solar cells [25]. Single crystal silicon cells were exposed to electron irradiation and subsequently to photon irradiation. Current and voltage (I-V) characteristics were found to degrade after photon irradiation of ~10 suns in a vacuum. The long wavelength (>800 nm) internal quantum efficiency (IQE) decreased for samples that suffered the photon degradation, indicating a reduction of the minority carrier bulk lifetime. Fischer and Pschunder then performed a more detailed study the following year. Many key observations were made to help characterize what is referred to as LID [7]. Float Zone and Czochralski (Cz) grown silicon crystals were used in the investigation. Similar to Crabb, Fischer and Pschunder also observed degradation in output power after illumination, as depicted in Figure 16. The open circuit voltage (V_{oc}), short circuit current (I_{sc}), and max power point of the 1 Ωcm Cz cell were found to degrade after photon illumination in the wavelength range of 0.2 to 1.0 μm. In addition, they found the effect was reversible by thermal treatment above 200°C for 5 hours. Thus, the degradation/recovery cycle that is unique to LID was identified for the first time. Thermal treatments were also investigated to determine if trap formation resulted from higher temperatures. Again, degradation was observed below 200°C and could be recovered by a thermal anneal (> 200°C). It was proposed that Cz silicon had a minority
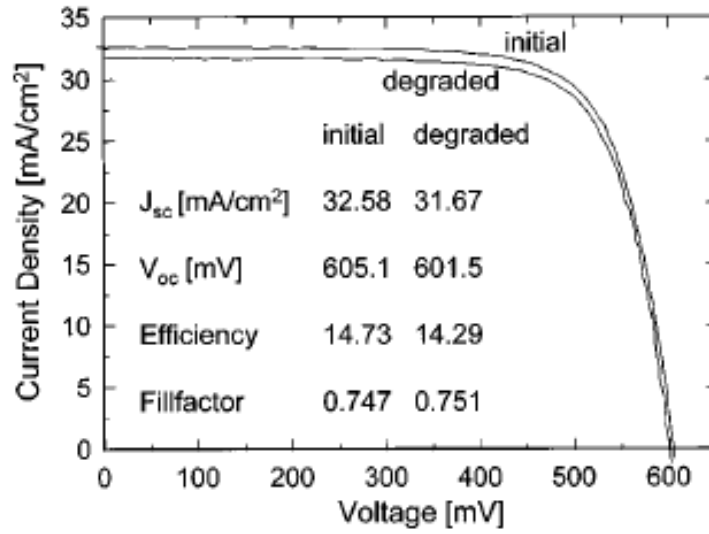
Figure 16. Change in I-V characteristics after 30 minutes
illumination at 0.1 mW/cm^2 and 25°C.

carrier lifetime that was not constant but rather oscillated between a high state, τ_A, and a
low state, τ_B. Higher temperature processing, causing oxygen precipitation, was found to
reduce LID, thus linking oxygen to trap formation. If the oxygen were precipitated, it
would no longer be available in the interstitial form for trap formation. Thus, a higher
minority carrier lifetime could be observed. Initially, metallic defects were proposed to
explain the structural identity of the trap responsible for the lifetime degradation. Graff
and Pieper proposed a vacancy-Au complex [6]. Weizer et al. suggested a lattice defect
and a Ag cluster [8]. In 1980, Corbett et al. reported that the defect formation occurred
under forward bias in the dark, suggesting the dissociation of donor acceptor pairs.
Therefore, carrier injection and not photon irradiation was proposed as the cause of trap
formation [9]. The dissociation of donor-acceptor pairs by the recombination enhanced
defect reaction (REDR) mechanism was suggested as the cause of formation of the
metastable defect. Reiss et al. investigated the Fe-B pair (a well-studied donor-acceptor

complex) as the metastable defect responsible for LID. However, the observed

degradation/recovery cycle differed from the one observed by Fisher and Pschunder [26].

Fe-B pairs fully recover bulk lifetime at room temperature (25°C) in the dark overnight

(~12 hours) and degrade at temperatures above 200°C. The metastable defect responsible

for LID **does not** recover at room temperature (25°C) and is **annealed** at temperatures

above 200°C.

Renewed interest in LID occurred during the 1990s because of a renaissance of Cz silicon

for solar cells, which accounted for ~50% of the PV modules produced at the time [2].

High efficiency solar cells fabricated using Cz silicon were found to degrade after

prolonged exposure to AM1.5 global conditions [27]. During the initial light exposure,

degradation occurred rapidly and then saturated over time. Further efforts were made to

identify the trap responsible for LID.

4.2.2 Structural Configuration of the Metastable Defect Responsible for
LID

Schmidt et al. investigated solar grade Cz Si samples doped with boron, gallium, and

phosphorus. In addition, electronic grade Si crystals free of metallic impurities were also

used as control wafers to investigate lifetime instabilities [28].   The phosphorus-doped

samples (n-type) showed no LID regardless of dopant concentration. Gallium-doped

samples (p-type) showed no degradation; instead, a slight increase in effective lifetime

was observed with illumination (See Fig. 17). In addition, the boron doped FZ samples

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with undetectable O_i showed no lifetime degradation. However, B doped Cz Si samples with high interstitial oxygen (O_i) concentration did suffer LID. Thus, only the samples that contained both boron and oxygen suffered LID. The B doped Cz samples showed the same lifetime recovery previously documented [7]. The samples could be continuously cycled between a high bulk lifetime value (after >200°C annealing) and a low bulk lifetime value (after illumination with white light). Based on these results, a model was suggested that involved one interstitial boron (B_i) and one interstitial oxygen
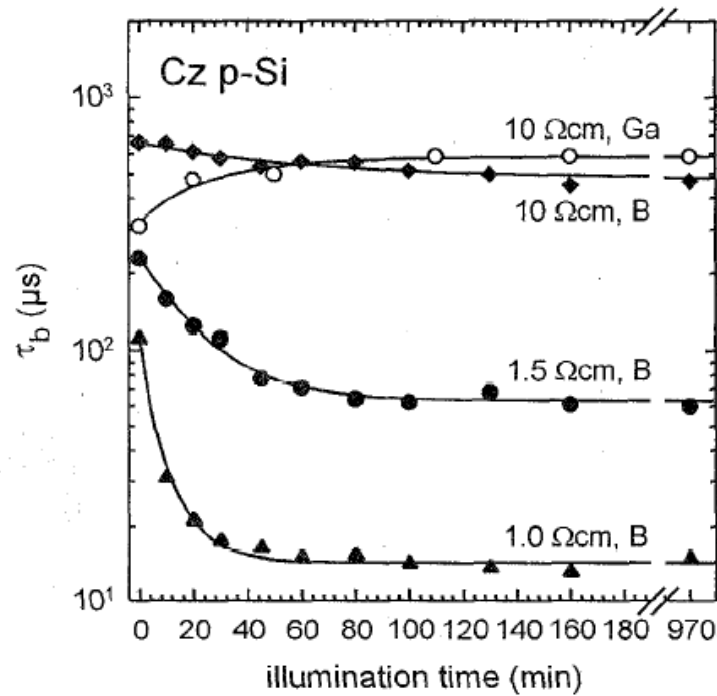
Figure 17. Bulk lifetime degradation in B doped Cz Si increasing with time but not in Ga doped Cz Si.

(O_i) atom to form B_iO_i during illumination as the metastable defect. Glunz et al. further proved the link with O_i and LID in B doped Si by oxygen contamination of a B doped FZ

sample that subsequently showed degradation (See Fig. 18) [29].   After many years of

investigation, the components necessary for trap formation were discovered/confirmed.
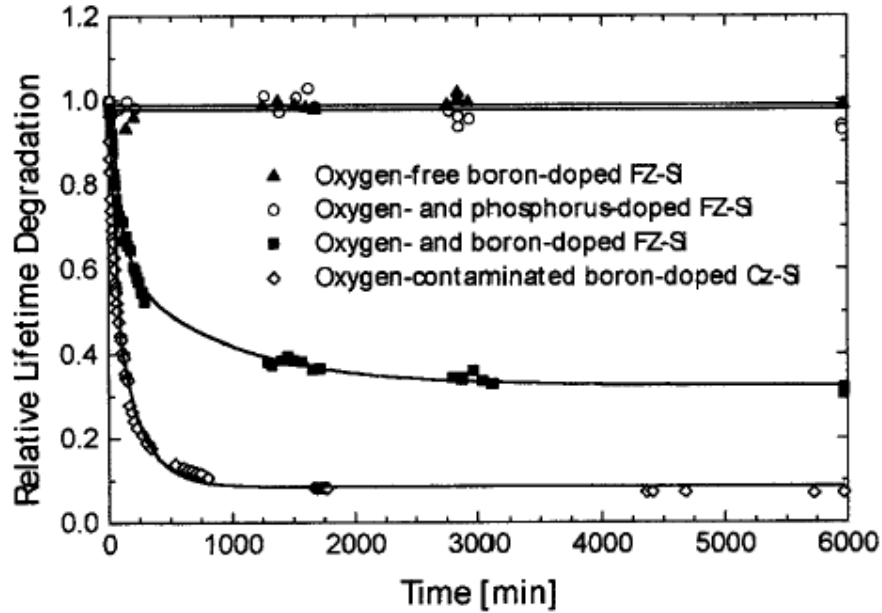
Figure 18. Lifetime degradation by 0.5 mΩ/cm^2 white light verse time.
Boron, phosphorus, and oxygen doped FZ as well as B doped Cz Si
samples exposed to carrier injection.

Exact configurations of the complex responsible for LID and its electrical properties are

still not fully understood.   However, many experiments, including an international joint

research project organized by Saitoh and Abe to understand the defect responsible for

LID, have resulted in a wealth of knowledge over the past 5years [30-42].   Various Si

samples such as Ga doped Cz with high oxygen content and magnetic Cz (MCz) grown

silicon with low oxygen content were sent to leading research institutes around the world

with the hope of further increasing the understanding of LID.   Georgia Tech was part of

this project and the results from that experiment are reported in this thesis.

Deep Level Transient Spectroscopy (DLTS) is a powerful technique to study trap characteristics. However, trap location and concentration could not be detected by DLTS yet. Other ingenious methods such as injection level and temperature dependence of the lifetime are being applied to more fully characterize the LID trap characteristics. In addition, methods to reduce or eliminate the harmful effects of LID on solar cell efficiency are also being investigated. The trap responsible for LID is not effectively gettered by phosphorus diffusion and there is no known method for passivation. Figure 17 shows the effective bulk lifetime of various FZ and Cz silicon samples exposed to illumination for long periods of time. The only samples to suffer LID contain both boron and oxygen [30-34]. Replacing B with Ga doping (See Fig. 17) in Cz Si eliminates LID despite high oxygen concentration. B-doped MCz with low oxygen content also reduces LID compared to a traditional B-doped Cz sample with high oxygen and equal resistivity. The international joint research confirmed that the trap responsible for LID requires the presence of boron and oxygen. The particulars of the structural composition and electrical properties are still unknown.

Multiple studies have been conducted to investigate the relationship between boron and oxygen concentration and LID trap (N_t) concentration [29-35]. A linear relationship is found between the B concentration and N_t as depicted in Figure 19. A super linear relationship was suggested between the oxygen concentration and N_t [29]. A best fit to the experimental data of Glunz suggested a fifth-order relationship between O_i and N_t. However, surface passivation of the Cz cells investigated by Glunz et al. was subjected to
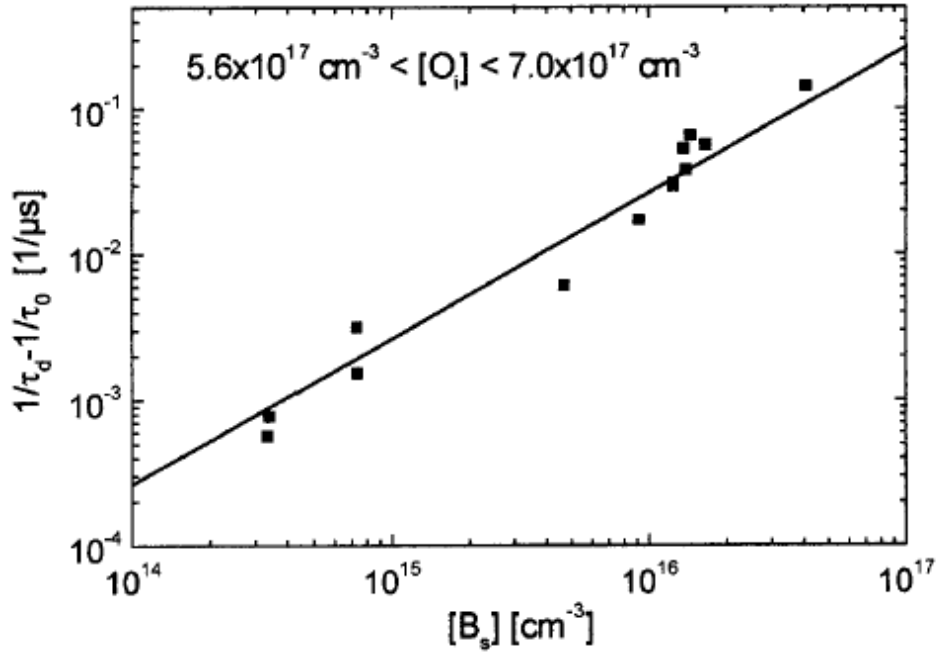
Figure 19. $1/\tau_d$-$1/\tau_o$ (proportional defect concentration) vs. boron concentration for Cz Si wafers with O_i between 5.6×10^{17} and 7.0×10^{17}.

thermal oxidation (1050^oC), which may have altered the original O_i concentration as a result of some oxygen precipitation. As a result, Schmidt et al. employed a low-temperature SiN_x, deposited at 375^oC, for surface passivation and performed detailed lifetime analysis to enhance the fundamental understanding of LID.

Using the annealed and degraded lifetime states that exist for samples that suffer LID, along with the assumption that the trap responsible for LID is independent of other traps and acts in parallel with the original bulk lifetime, the following analysis can be used to obtain an effective trap concentration to better quantify trap behavior. First, the effective lifetime of a sample was measured directly after annealing (above 200^oC) and recorded as τ_a. Next, the same sample can be measured at any arbitrary time after LID occurs and the

corresponding effective lifetime is recorded (τ_{eff}). Using the assumption that the defect formation responsible for LID is the only participant in effective lifetime reduction, the following equations were used for the analysis to determine **normalized defect concentration**, N_t^* [39]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_a} + \frac{1}{\tau_d} \tag{25}$$

where τ_d is the SRH lifetime for the metastable defect responsible for LID. Next, recognizing that the degraded lifetime is inversely proportional to N_t under low-level injection where bulk lifetime is the SRH lifetime and solving eq. (25) for $1/\tau_d$, the normalized defect concentration in eq. (29) was obtained as follows:

$$\frac{1}{\tau_b} = \frac{1}{\tau_{SRH}} \Rightarrow \tau_{SRH}(ll) \cong \tau_{no} \tag{26}$$

$$\frac{1}{\tau_{no}} = \sigma_n \upsilon_{th} N_t \tag{27}$$

$$\frac{1}{\tau_d(ll)} = \frac{1}{\tau_{no}} \tag{28}$$

$$\frac{1}{\tau_d} = \frac{1}{\tau_{eff}} - \frac{1}{\tau_a} = \sigma_n \upsilon_{th} N_t \Rightarrow N_t^* \tag{29}$$

where τ_{eff} is measured at a time after LID, σ_n is the capture cross section, υ_{th} is the thermal velocity, and $\tau_d(ll)$ is the defect lifetime at low-level injection. Section 4.3 further analyzes the SRH lifetime behavior associated with the metastable defect in order

to justify the assumptions used to obtain the normalized defect concentration. Figure 20 shows a plot of the defect lifetimes associated with different resistivity samples that suffer LID. Using SRH lifetime theory to fit the trap energy level to all the τ_d curves, Schmidt concluded that the trap energy level is restricted to mid-gap ($E_v+0.35eV$ and $E_c-0.45eV$) and the τ_{no}/τ_{po} ratio is in the range of 0.1 to 0.2 for all samples except the 31 Ωcm sample. To better quantify the normalized defect concentration, N_t^* it is recorded at an injection level equal to $0.1N_B$, where N_B is the base doping level. Combining all of the above information led to the proposal of a new structure involving substitutional boron (B_s) and "n" O_i atoms. Using the fact that interstitial boron is typically only found in electron irradiated samples and that the metastable defect in the active state was shown
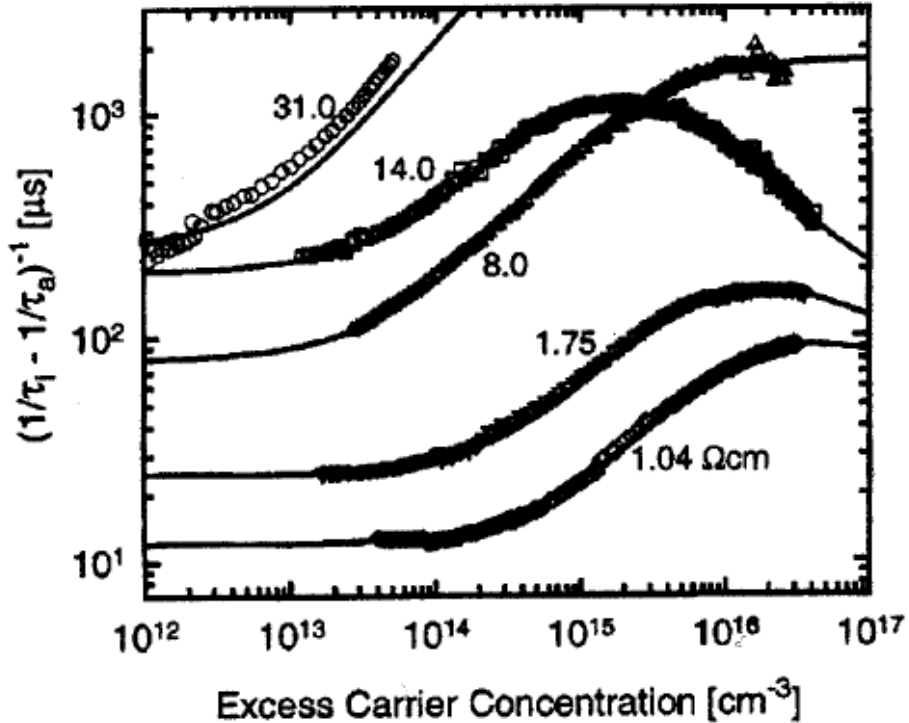
Figure 20. Measured injection level dependence of τ_d on excess carrier concentration for various resistivity Cz Si samples (using SRH theory).

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to be confined to a mid-gap trap, the structural configuration of B_iO_i was eliminated as the defect configuration because the energy level associated with B_iO_i is 0.27 eV below the conduction band and not a mid-gap trap.

Temperature dependence of trap generation and annihilation, along with illumination wavelength and intensity, have also been frequently used to analyze trap behavior. Annealing has been shown to occur at temperatures >100°C. However, only partial recovery is realized below 200°C [36-37]. In addition, the irradiation wavelength from ultra-violet (UV) to infra-red (IR) was found to effectively degrade samples, i.e., degradation was essentially independent of photon energy. Irradiation intensity was not found to be proportional to the degradation rate [36]. Schmidt et al. examined the trap generation rate as a function of temperature and used an Arrhenius plot (defect generation rate versus inverse temperature) to determine the activation energy for trap generation (E_g) of 0.4 eV [38], using the following equations to determine the generation time constant τ_{gen} as a function of temperature:

$$N_t^*(t,T) = N_t^*(t \rightarrow \infty)\left(1 - e^{-t/\tau_{gen}}\right) \tag{30}$$

$$R_{gen}(T) = 1/\tau_{gen}(T) \tag{31}$$

$$\frac{1}{\tau_{gen}} = R_{gen}(T) = R_{gen}(T \rightarrow \infty)\exp(-\frac{E_g}{kT}) \tag{32}$$

where T is temperature, $N_t^*(t,T)$ is the normalized defect concentration as a function of time and temperature, R_{gen} is the generation rate of defects, and τ_{gen} is the generation time constant. Similarly, the annihilation energy (E_{ann}) was determined by Schmidt and Rein

to be 1.8 eV and 1.3 eV, respectively [38,39]. This approach is described in more detail in the next section. In addition, Schmidt et al. suggest a new defect formation process based on a substitutional B_s and an interstitial oxygen dimer (O_{2i}), which is known to be a fast diffuser in Si. Figure 21 shows that a quadratic dependence of O_i with the normalized defect concentration N_t^* supports this model. The migration energy is equal to the generation energy ($E_{mig}=E_{gen}=0.4$ eV) and the dissociation energy (E_{diss}) of the B_sO_{2i} complex is equivalent to the $E_{ann}=1.8$ eV [39]. However, the binding energy of the defect in the passive state cannot be determined because the activation energy does not retain information concerning the original defect state.

The end goal of LID research in this thesis is to discover ways to avoid or minimize the harmful effects of the lifetime degradation on the efficiency of solar cells. This provided the motivation to investigate two tangible approaches to minimize or eliminate the
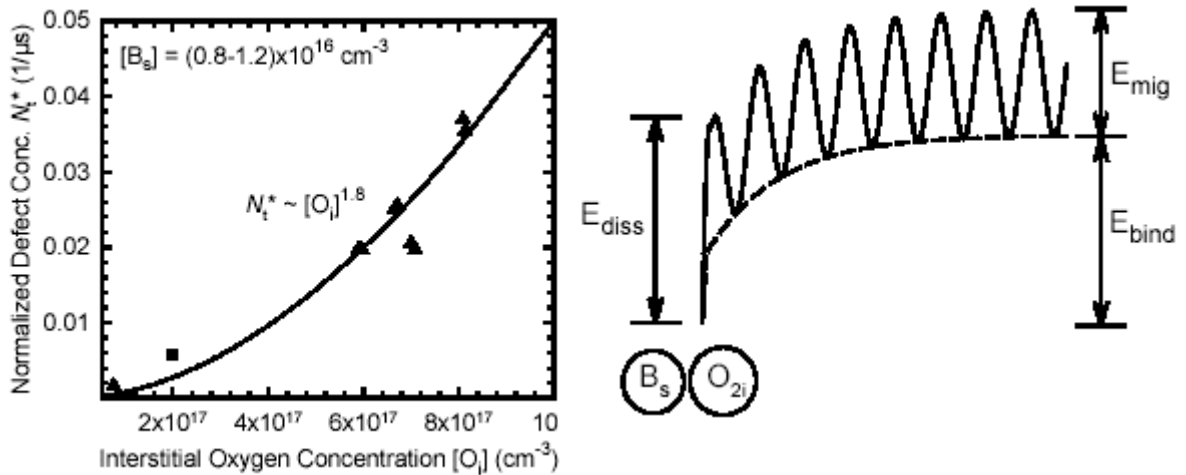
Figure 21. Normalized defect concentration N_t^* as a function of O_i concentration which supports the defect model proposed for the B_sO_{2i} interaction.

detrimental effects of LID on solar cells: 1) Eliminate or reduce the formation of traps responsible for LID or 2) Design and fabricate solar cells to minimize the efficiency dependence on lifetime (τ). It is important to recognize that using Ga or P as a base dopant avoids LID but would require a major shift in conventional technology. The much lower segregation coefficient of Ga (<<1) poses a challenge for growing Ga doped Cz ingots with uniform doping concentrations from seed to tank. The use of MCz drastically reduces the LID and subsequently increases the efficiency but also adds the complexity of a magnetic field application during ingot growth. Phosphorus doped Si would require a major shift in processing techniques typically used for p-type Si. Specific thermal treatments have also been shown to increase final bulk lifetime coupled with a decrease in interstitial oxygen concentration [38-44]. This is accomplished via oxygen precipitation either during solar cell processing or by a pretreatment before solar cell fabrication. Oxygen precipitation during conventional furnace processing and RTP processing has been shown to increase the final stabilized lifetime for B doped Cz Si with high O_i content [40,43]. Samples with a total degraded lifetime of 10 µs were shown to have a stable degradation lifetime of 25 µs after RTP heating. Similar results were observed for samples after optimized conventional furnace heating as well [40].

The second method to reduce the impact of LID on solar cell efficiency is to use a cell design where efficiency is less sensitive to bulk lifetime. It was found that decreasing the wafer thickness down to 100 to 150µm decreased the LID effect on solar cell efficiency [35,45]. This approach offers the additional benefit of cost reduction resulting from decreased wafer thickness. This provided the motivation to explore optimum cell design

by reducing cell thickness that gives the highest stabilized cell efficiency after LID. The impact of cell parameters like surface recombination velocity and bulk lifetime on the optimum cell design was also investigated for both manufacturable screen-printed and high efficiency photolithography cells.

Solar cell fabrication is currently done predominantly on p-type Si crystals that are boron doped. Besides Cz Si, many of the low-cost cast mc-Si wafers and ribbon technologies also have O_i content in the bulk. In 2002, the use of low-cost multi-crystalline material accounted for ~58% of the total PV market compared to ~30% for mono-crystalline Si [1]. Cast and ribbon mc-Si materials contain defects, such as transition metals, dislocations, and grain boundaries, in addition to boron and oxygen. Very little is known about the LID in mc-Si materials. Since these materials are becoming increasingly important as a result of improved efficiencies, this provided the motivation to study LID in promising low-cost mc-Si PV materials. Quantitative determination of which silicon crystals are affected by LID and to what extent is very important for realizing the goal of cost-effective PV with crystalline silicon.

4.3 Lifetime Analysis of the Metastable Defect

The metastable defect responsible for light induced degradation has not yet been detected by direct electrical measurement using DLTS. Therefore, lifetime spectroscopy has been used for characterizing the trap. Using Shockley-Read-Hall theory and measured effective lifetime data, a better understanding of the trap has been achieved.

To better understand the metastable defect responsible for LID, it is helpful to first understand the injection level dependence of lifetime for different traps. Under low-level (ll) injection, eq. (12) reduces to

$$\tau_{SRH}(ll) = \tau_{po}\left(\frac{n_1}{p_o}\right) + \tau_{no}\left(1 + \frac{p_1}{p_o}\right) \qquad (33)$$

where $n_o \ll \Delta n \ll p_o$, and is sometimes further approximated by $\tau_{SRH}(ll) \approx \tau_{no}$ for mid-gap traps, and $\tau_{SRH}(ll) \approx \tau_{no}(1+p_1/p_o)$ for a shallow trap. However, for high-level injection (hl), $\tau_{SRH}(hl) \approx \tau_{no} + \tau_{po}$. Therefore, if τ_{SRH} is dominated by only one trap, curve fitting coupled with measured lifetime data can be used to determine some of the trap characteristics. For example, if the $\tau_{no}/\tau_{po}=0.1$ and the base resistivity (30 Ωcm p-type) are held constant, the energy level for the trap can be varied to fit the measured data. The use of a higher resistivity (i.e., lower doping concentration) material makes τ_{SRH} more sensitive to n_1 and p_1 (or trap energy level, E_T). Figure 22 shows how lifetime varies from low to high injection level as a function of trap location, using a fixed base resistivity (30 Ωcm) and $\tau_{no}/\tau_{po}=0.1$ for five different trap energies. Notice that only trap energies near the mid-gap show a similar injection level dependence where the SRH lifetime increases with injection level up to 10^{16}cm^{-3}. Therefore, if the SRH lifetime versus injection level is known and only one trap controls the lifetime, the above curve fitting technique can be used. The curve fitting technique can be used to determine τ_{no}/τ_{po} ratio, provided the trap is assumed fixed to a mid-gap energy level and the measured data is matched by varying the τ_{no} to τ_{po} ratio. In addition, if all the parameters for τ_{SRH} are held constant except for the trap concentration, N_t, then the ratio of τ_{no}/τ_{po} remains constant (τ_{no}/τ_{po} is not a function of N_t), but the individual values change. Figure 23 shows the τ_{SRH} verses injection level for an increasing N_t. The constant $\tau_{no}/\tau_{po}=0.1$ ratio
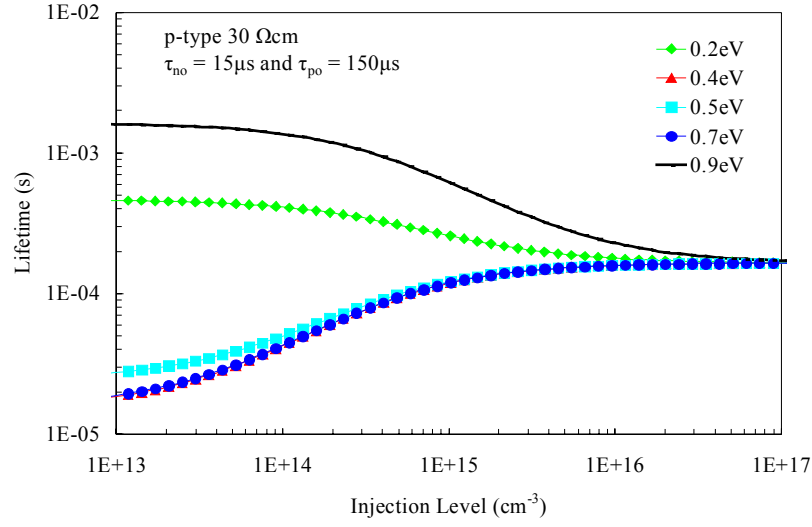
Figure 22. Shockley-Read-Hall lifetime vs. injection level for various trap energy levels.
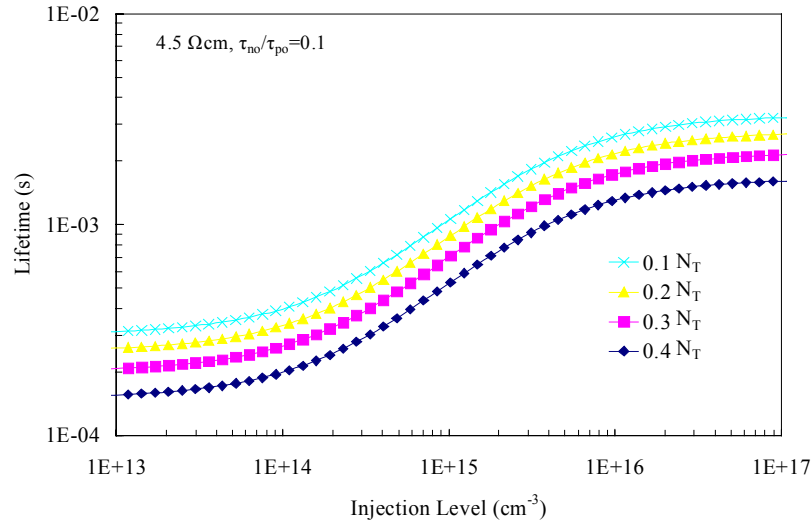
Figure 23. Shockley-Read-Hall lifetime vs. injection level for various trap concentration N_T values.

indicates that a single trap participates to cause the reduced τ_{SRH} lifetime. Multiple trap participation would cause a change in the τ_{no}/τ_{po} ratio. Thus, if one trap or impurity is known to be the sole factor changing the τ_{SRH} (for silicon wafers τ_{SRH} dominates the bulk lifetime τ_b at low injection levels), a significant number of trap characteristics can be derived from IDLS. This also indicates that if measured data demonstrates a similar constant τ_{no}/τ_{po} ratio, then a single trap can be used to model experimental data.

Temperature dependent lifetime spectroscopy (TDLS) can also be used to determine the activation energy for trap formation or annihilation. To properly study the defect generation or annihilation energy, the mechanisms must be isolated during the analysis. Although the metastable defect is completely annealed at 200°C in the dark, some defect annihilation does occur at temperatures as low as 100°C. Therefore, the temperature dependent defect generation should be analyzed at temperatures below 100°C. Figure 24 shows the isothermal measurement [46] of the normalized trap concentration $N_t^*(t)$ as a function of time at a fixed injection level ($\Delta n=1 \times 10^{15} cm^{-3}$). As the temperature increases so does the trap generation rate, thus demonstrating that the trap is thermally activated. The temperature dependent defect generation rate is expressed by

$$R_{gen} = \frac{1}{\tau_{gen}} \qquad (34)$$

where, τ_{gen} is the rise time of the $N_t^*(t)$ and depends strongly on temperature and is exponential in nature. Next, $R_{gen}(T)$ can be determined by fitting the $N_T^*(t,T)$ as a function of both time and temperature:

$$N_T^*(t,T) = N_T^*(t \rightarrow \infty)\left[1 - e^{-(R_{gen}(T)t)}\right] \qquad (15)$$

Once $R_{gen}(T)$ values are extracted, an Arrhenius plot (See Fig. 24) of the defect generation rate can be made and the generation energy E_{gen} can be determined from

$$R_{gen}(T) = R_{gen}(T \to \infty)e^{-E_{gen}/kT} \qquad (16)$$

where the E_{gen} was found to be 0.4eV [38]. Thus, the energy required to generate traps (i.e., activate traps) was more precisely determined using this method by Schmidt and Rein independently while staying in agreement with the IDLS claim that the trap energy level is a mid-gap trap with an energy greater than E_v+0.35 and less than E_c-0.45eV. More specific, the energy level of the trap responsible for LID is currently thought to be at 0.4 eV above the valence band. A similar analysis can be made to determine the annihilation energy (E_{ann}=1.8eV), which is proportional to the deactivation or dissociation energy. The metastable defect is generated by injected carriers with E_{gen}=0.4 eV from the initial annealed state (or stationary binding energy of the defect) and then is deactivated by 1.8 eV, according to the model described by Schmidt [46].
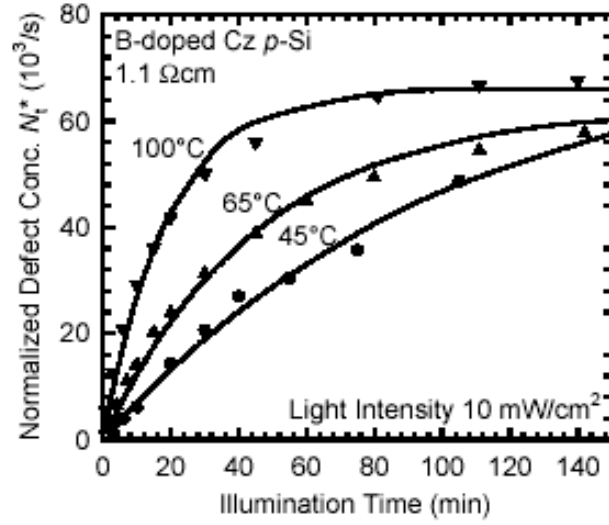
a.)
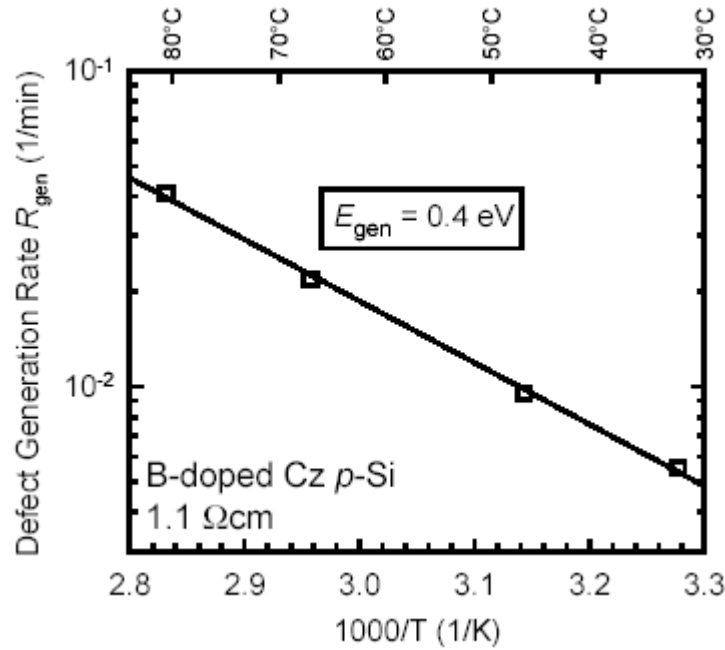
b.)

Figure 24. a) Isothermal measurements of the time-dependent normalized defect concentration $N_t^*(t)$. Between each measurement, the sample was illuminated with a halogen lamp at 0.1 suns at temperatures ranging from 45 to 100°C [64]. b) Isothermal measurements of the time-dependent normalized defect concentration $N_t^*(t)$. Between each measurement, the sample was illuminated with a halogen lamp at 0.1 suns at temperatures ranging from 45 to 100°C [64].

4.3.1 Illumination Intensity and Temperature Dependence of Efficiency Degradation

Light intensity (power) directly affects the injected carrier concentration into solar cells. The number of injected carriers is directly proportional to illumination intensity. Thus, the more light that is absorbed on the surface of a solar cell, the more carriers are generated. The formation of the metastable defect is an injected carrier phenomena, so a reasonable assumption would involve a higher generation rate for a higher intensity illumination. However, this is not necessarily the situation. Hashigami et al. showed how the formation of LID traps was relatively independent of illumination intensity [36]. Figure 25 shows the degradation rate of the open circuit voltage as a function of light intensity and exposure time. At intensities higher than or equal to 1% ($\geq$ 1 mW/cm^2) of the standard solar cell test illumination conditions (100 mW/cm^2), the rate of decay was essentially saturated and independent of intensity. The low intensity light required for the saturation suggests a low defect concentration. The photon flux for 1 mW/cm^2 is 10^{15}cm^{-2}s^{-1}. To extract the activation energy from the decay time of the temperature dependent $V_{oc,}$ the following equations can be used, similar to the lifetime analysis previously described:

$$V_{oc}(t) = V_{oc}(t \rightarrow \infty) + V_{oc}(0) * e^{-t/\tau_{dec}} \tag{35}$$

$$1/\tau_{dec}(T) = 1/\tau_{dec}(T \rightarrow \infty)e^{-E_{act}/\tau_{dec}kT} \tag{36}$$

where t is time, T is temperature, τ_{dec} is the decay time constant, E_{act} is the activation

energy, and k is Boltzmann's constant. Similar to the lifetime approach, an Arrhenius

plot of the temperature versus τ_{dec}^{-1} allows for the determination of the activation energy,

which was found to be 0.4eV, in excellent agreement with the lifetime analysis.
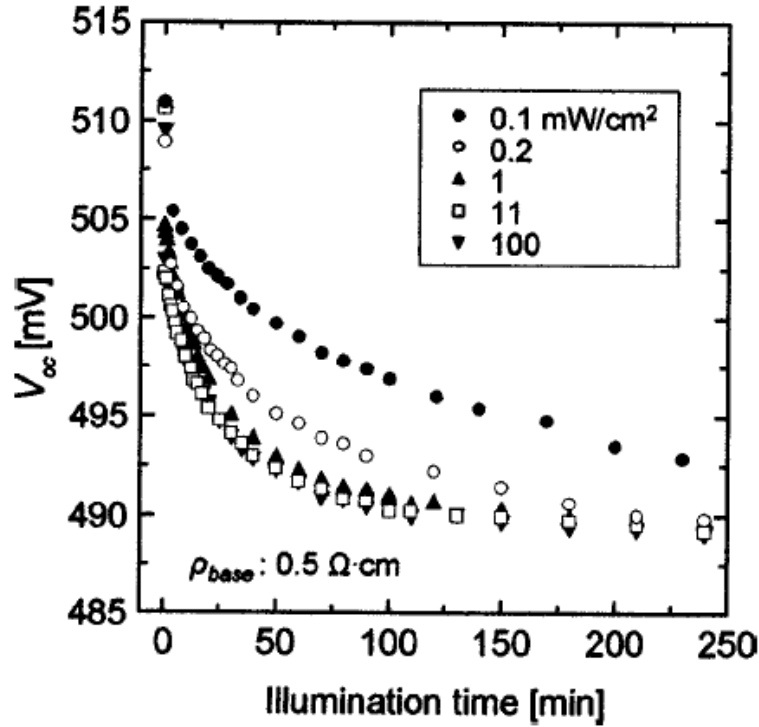
Figure 25. V_{oc} decay curves of solar cell with base resistivity of 0.5
Ωcm under illumination of various intensities [20].

Another important illumination characteristic recognized by Hashigami was the

dependence on infrared light compared to ultra-violet light (blue light). Degradation

occurred regardless of the illumination spectra. The underlying significance of this

observation suggests charged carrier-dependent trap generation. Blue light is absorbed

near the silicon surface. However, the bulk lifetime still suffered degradation, Suggesting

that charged carriers (electron-hole pairs) created at the surface of the silicon device were transported through the base material and generated traps deep into the bulk. This is supported by Figure 26, where the spectral response before and after illumination with blue light shows a decreased response only in the long wavelength range, similar to normal LID phenomena. A typical solar cell has a thickness on the order of 300 μm. The charged carriers created within the first micrometer had to travel well into the bulk of the device (~100 to 300 μm). This can be easily explained using diffusion length arguments because even a 10 μs bulk lifetime corresponds to a diffusion length of ~ 150 μm.
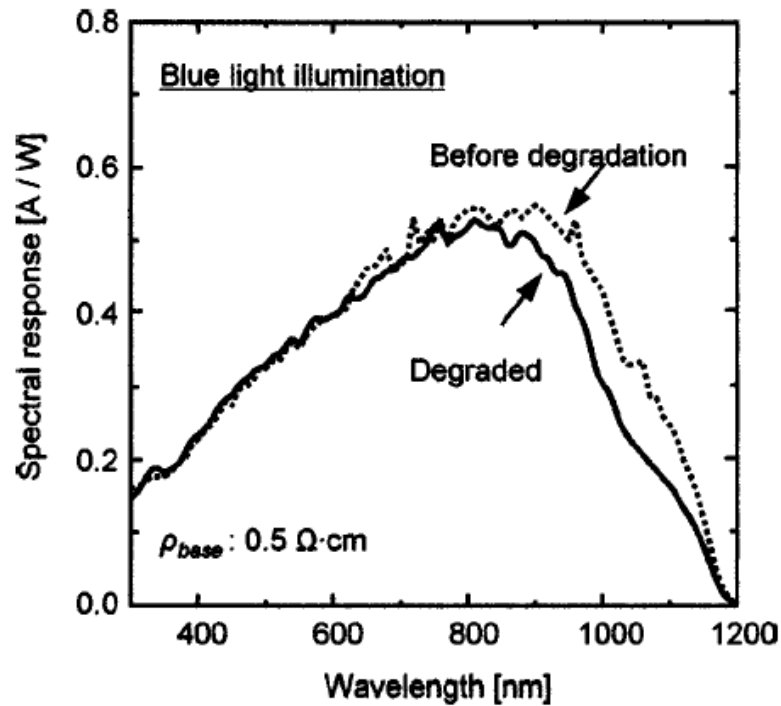
Figure 26. Spectral response degradation of a solar cell with a base resistivity 0.5 Ωcm under a blue light illumination for 6 hours [20].

The understanding of light induced degradation is continually evolving but is still only partly understood. Excellent research has been conducted to determine ways to quantify the trap, leading to clarifications on the temperature, time, electrical, and optical characteristics associated with the metastable defect known to cause light induced degradation. This provided the motivation to further investigate the metastable defect in both Czochralski and mc-Si samples to better understand the basic characteristics so that the effects of LID in finished solar cells can be minimized.

CHAPTER 5

5   IMPROVED UNDERSTANDING OF THE METASTABLE DEFECT IN CZOCHRALSKI SILICON

5.1   Study of LID Under Simultaneous Generation and Annihilation

Trap formation is known to occur under carrier injection, and trap annihilation is achieved by annealing above 200°C [6,7,9]. To improve the understanding of the trap formation mechanism and gain insight into the defect configuration, trap annihilation and creation are investigated more thoroughly. Trap dissociation at elevated temperatures has been suggested as a possible explanation for recovery. Previous investigations have studied LID trap annihilation and formation individually but not in combination [25-45]. It is known from the literature that trap creation is an injected carrier phenomenon and not a photon phenomenon. That is why trap formation also occurs under forward bias in the dark [26]. However, if a sample is subjected to both heat and illumination, then creation and annihilation of the metastable defect may also occur simultaneously and a different LID behavior may be observed, thereby providing additional information on the LID trap formation mechanism.

Therefore, illuminated heating is investigated in this research in an industrial belt furnace (BF) as well as in a rapid thermal processing (RTP) system. Both use high intensity light to heat wafers. Samples received a light phosphorus diffusion followed by a SiO_2/SiN_x stack passivation prior to lifetime analysis. A ~10 nm SiO_2 layer was grown in a furnace

at 925°C followed by a 65 nm SiN_x layer deposited using a Plasma Therm PECVD. The stack passivation is known to provide a stable surface recombination velocity (SRV) below 500°C [47]. Therefore, it is well suited for studying bulk lifetime degradation using the photoconductance (PCD) technique. Float zone (FZ) samples were used as controls to monitor bulk lifetime and SRV changes caused by high temperature processing. Bayer Cz wafers with a 1.0-1.5 Ωcm resistivity were used in all the experiments, along with 1.3 Ωcm FZ samples as control wafers.

Figures 27 and 28 show the τ_{eff} of Cz and FZ Si wafers after various illumination and heating processes. Both were passivated with a SiO_2/SiN_x stack and were subjected to 15 minutes of heat treatment in a belt furnace at three different temperatures (400°C, 600°C, 800°C). A 400°C conventional furnace tube anneal (in the dark) was used to remove any LID prior to belt furnace treatment. Initial τ_{eff} values were in the range of 200 to 250 μs for the Cz Si and 1100 to 1200 μs for the FZ samples (Figs. 27 and 28). After belt furnace (BF) heating, the samples were annealed again in the conventional furnace (CF) tube to recover the lifetime by annealing the LID traps. The FZ samples reveal that 600°C and 800°C belt processing lowers the effective lifetime because of surface passivation degradation. Using iodine-methanol surface passivation, a bulk lifetime (τ_b) of 1580 μs (at 10^{15} cm^{-3} injection level) was found for the FZ Si used in this investigation. The τ_{eff} was measured to be 1100 to 1200 μs for the FZ samples with the $SiO_2/SiNx$ stack passivation, corresponding to a SRV value of 3 cm/s using the following equation:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S}{W} \qquad (37)$$

where W is the wafer thickness. This is consistent with values reported in the literature for high quality SiO_2 / SiN_x stack passivation [48]. Using the initial measured τ_{eff} value of ~1150 μs for the FZ Si, the data in Figure 27 shows that the SRV remained unaffected at 400^oC. However, after 600^oC belt processing, the SRV increased to ~15 cm/s (τ_{eff} = 600 μs) and at 800^oC the SRV reached ~35 cm/s (τ_{eff} = 360 μs). Thus, special attention must be given to the effective lifetime values to properly separate surface lifetime degradation from bulk lifetime degradation.

Figure 27 shows that after the first 400^oC anneal in the belt furnace (BF), Cz Si showed a lifetime degradation to 30 μs, followed by a full recovery to ~250 μs in the conventional tube furnace (CF) at 400^oC. In the case of the FZ sample, the effective lifetime remained unaltered (~1.2 ms) by the 400^oC anneal in the BF and CF, indicating all changes to the τ_{eff} were caused by bulk LID effects. After the 600^oC BF process, the Cz Si effective lifetime degraded to 40 μs and then only partially recovered to 130 μs after a 15-minute nitrogen anneal at 400^oC in the CF (Fig. 27). The apparent partial recovery to 130 μs, instead of 200 μs, is attributed to the degradation in surface passivation by the 600^oC BF anneal, as is evident from the FZ control sample demonstrating an increased SRV from 3 cm/s to 15 cm/s, corresponding to an effective lifetime of 150 μs for the Cz material used in this study.   Thus, full effective lifetime recovery is obscured by the increased SRV.
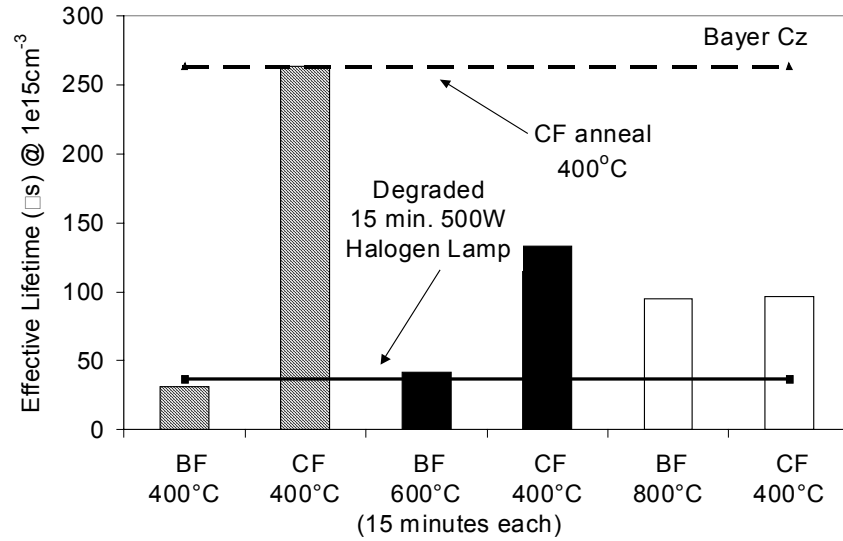
Figure 27. Belt furnace processing (BF) induced LID at 400, 600, and 800°C in Cz sample followed by conventional furnace (CF) recovery at 400°C.
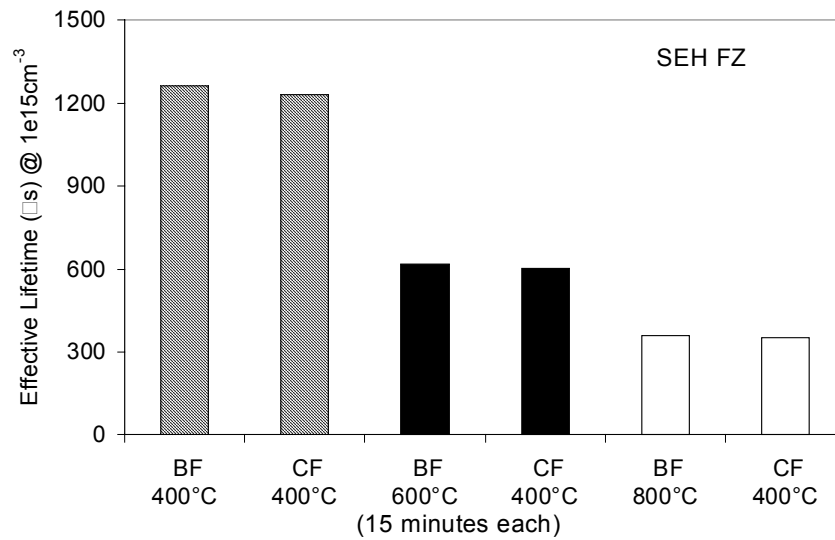
Figure 28. Surface passivation performance on FZ samples at 400, 600, and 800°C in a belt furnace (BF) followed by a conventional furnace (CF) anneal or recovery at 400°C.

After 800°C belt processing, the SRV is further increased to 35 cm/s (decreasing the measured effective lifetime), but no change in the measured effective lifetime is observed for either Cz or FZ samples after a subsequent anneal at 400°C in the CF. Any lifetime degradation recovered by the subsequent CF anneal (400°C) in Figure 27 is attributed to LID in Cz Si samples. The fact that Figure 27 shows no lifetime recovery after 800°C BF processing suggests that the trap annihilation rate at 800°C in the BF is greater than the trap creation rate. However, substantial degradation was observed after 400°C and 600°C BF processing (See Fig. 27), indicating that trap annihilation rate at these temperatures is lower than the trap formation rate. Thus, LID can occur during belt processing up to a temperature of 600°C, demonstrating that the metastable defect responsible for LID does not dissociate completely above 200°C, but rather is still an active trap.

Similar to belt processing, RTP heating of the Cz samples can also result in LID at elevated temperatures, as shown in Figure 29. However, 200°C was the highest degradation temperature in the RTP (See black bars in Fig. 30) as opposed to 600°C in the BF (See black bars in Fig. 27) at which net LID was observed. FZ samples subjected to 200°C heat cycling in the RTP maintained stable surface passivation.

Figure 29 shows that if the degraded Cz Si sample is subjected to an RTP cycle (200°C / 10 min.), the 25 µs effective lifetime recovers partially to 45 µs. If the same sample is then annealed in a CF at 400°C, the initial lifetime of 180 µs is restored. By subjecting the same sample to another RTP cycle (200°C/10 min.), the effective lifetime was then

partially degraded back to 45 μs. This demonstrates that during the illuminated heating in

RTP, both LID and recovery occur simultaneously and reach an equilibrium point (45 μs
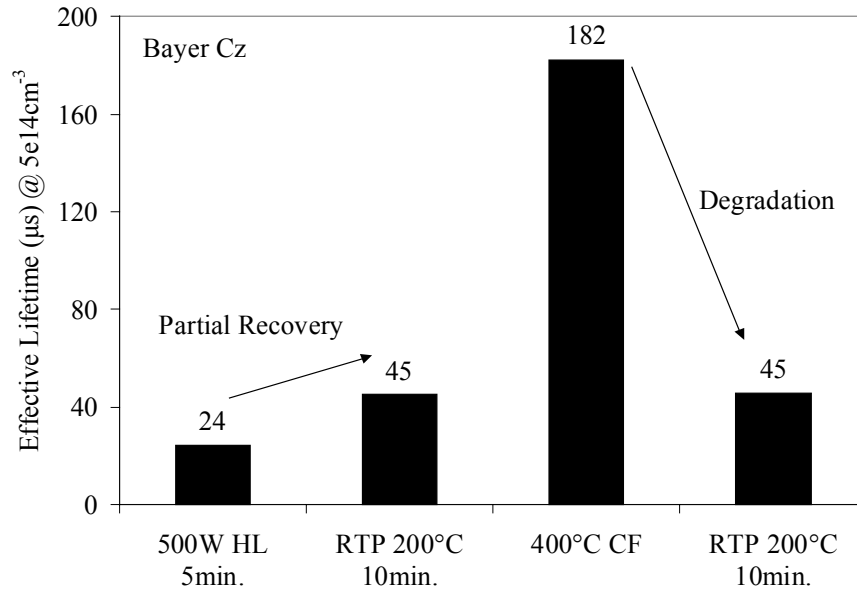
at 200°C).

Figure 29. RTP LID cycling revealing partial recovery after halogen lamp
(HL) heating at 200°C as well as partial degradation following a CF anneal.

Figure 30 shows the recovery of the effective lifetime of samples subjected to heat

treatments in the belt at 400°C and in the RTP at 200°C and 300°C. No recovery of the

degraded sample was observed up to the 400°C belt process. This is because both

generation and annihilation of traps take place at 400°C in the BF. If the 400°C anneal is

done in the dark, full recovery is observed because only annihilation occurs in the

absence of light. Only a partial recovery was observed at 200°C in the RTP (24 μs to 40

μs), indicating that the trap annihilation rate at 200°C in RTP is slightly higher than the
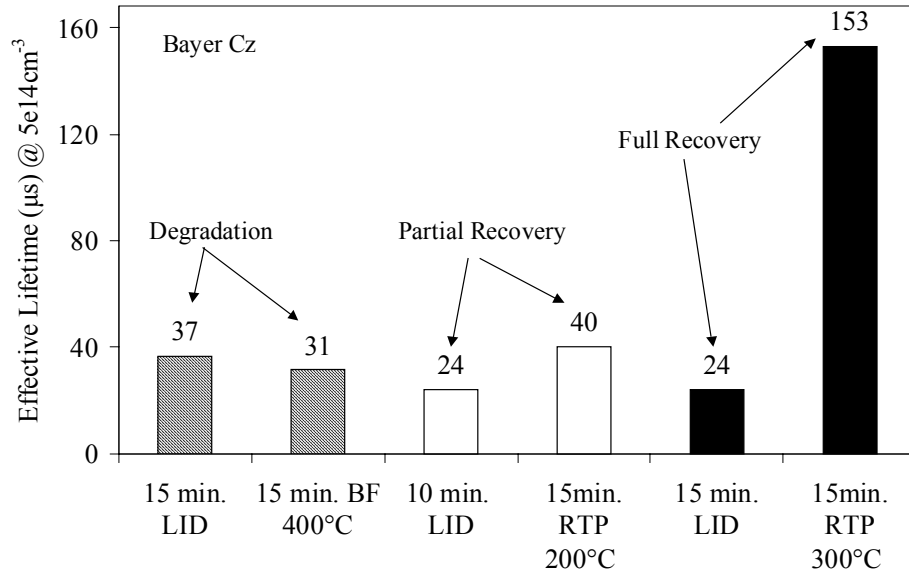
Figure 30. RTP LID partial recovery at 200°C and 300°C preceded by LID
and BF partial degradation at 400°C.

trap generation rate. However, RTP annealing at or above 300°C showed a full recovery

(25μs to 153 μs), indicating that the trap annihilation rate exceeds the generation rate at ≥

300°C in RTP to fully recover the bulk lifetime. Again, recall that this temperature was

above 600°C in the case of BF processing. Thus, depending on the external stimulus

applied (including both heat and illumination), either the annihilation or creation rate of

traps can dominate at a given temperature. For the RTP system used in this study, the

recovery rate exceeded the degradation rate at a much lower temperature than the lamp

heated BF. This is partly due to the difference in the photon flux and spectrum in the two

lamp heated systems, as well as to the amount of time needed for cooling.

Thus, lifetime degradation under illumination at elevated temperatures is documented for

the first time in this study. Both degradation and recovery were demonstrated during the

same thermal cycle, supporting the creation and annihilation of trap centers under the same external stimulus conditions. Photon flux helps in creating LID traps, while the heat flux anneals the defect.

5.2   Light Induced Degradation Via Charged Carrier Transport

Hashigami et al. showed that blue light absorbed near the surface in silicon caused LID deep in the bulk. This indicates that LID is not only caused by carrier injection but also the transport of injected carriers deep into the bulk. This led to the design of an experiment in this thesis to explore and understand this phenomenon further. A B doped Cz wafer with a 0.7 Ωcm based resistivity and > 13 ppma O_i was passivated by SiN_x and annealed above 200^oC in the dark to fully recover the bulk lifetime. The sample was then illuminated on only half of the wafer surface, while the other half was shielded by a 1-inch thick aluminum block. The sample was carefully prepared with no metal contacts so that no potential difference could be transported from the illuminated side to the dark side via the metal contacts. This equally distributed the electrical charge created on the illuminated side (avoiding carrier injection resulting from a forward bias created by illumination). A low intensity white light was used to degrade the sample for 90 minutes. A spatially resolved photoluminescence effective lifetime mapping technique, discussed in more detail in Chapter 6, was used to obtain a surface map of the lifetime of the Cz sample. In Figure 31, the lifetime is proportional to the gray bar, where a high number correlates to a high lifetime. The x and y axes are the length and width of the Cz sample in Figure 31. This figure shows that the sample degradation primarily occurred on the illuminated side of the Cz wafer.
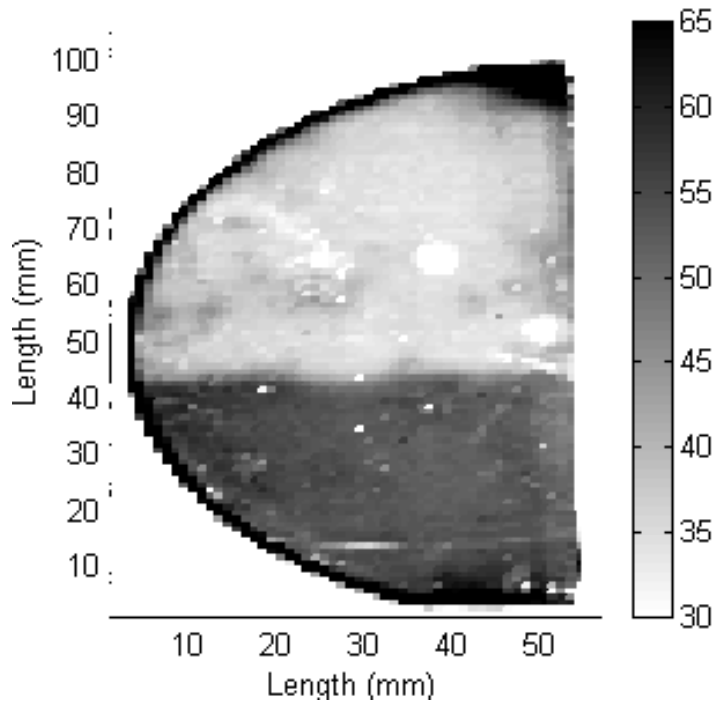
Figure 31. Photoluminescent map of a half wafer of B doped Cz Si subjected to shading by an aluminum block on the bottom ~42 to 43 mm of the wafer. LID confined predominantly to the illuminated region.

However, a closer inspection of the boundary between the illuminated and the dark side in Figure 32 gives a better grasp of the extent of carrier transport. The figure shows the transition from the high lifetime shaded region at ~42 mm (on the y axis) to the lower lifetime illuminated part of the Cz wafer, supporting the creation of LID traps by carrier transport. The transition region has a footprint on the order of ~3 mm, indicating that charged carriers diffused from the illuminated region to the dark region and were responsible for trap generation. Some carriers can diffuse three times the diffusion length (2000 μm) or 2 mm for the 200 μs lifetime Cz material, a much larger distance than

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expected by the injected carriers. This could be due partly to imperfect boundary

conditions between the illuminated and non-illuminated sides.

Fig. 25 y-axis (distance mm)
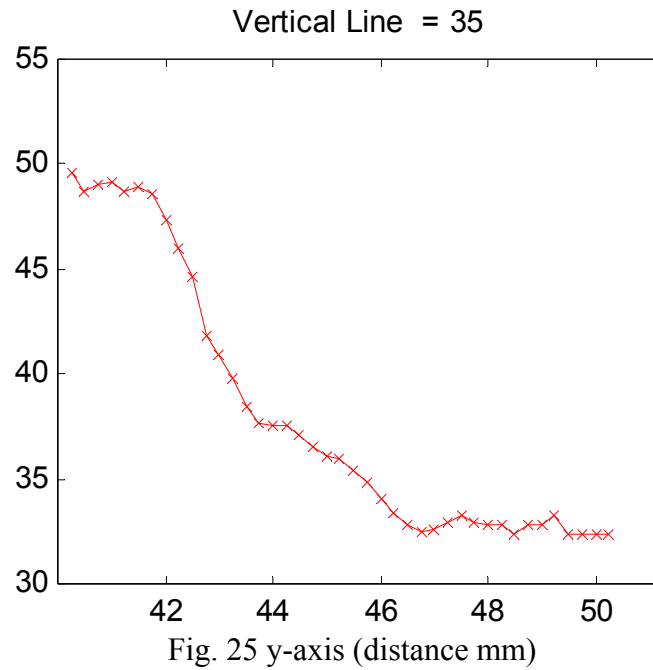
Figure 32. Change in effective lifetime (arbitrary units) along the
vertical line at 35 mm showing the transition from the illuminated side
of a B doped Cz wafer that suffered localized degradation to the shaded
region. The transition region was from ~42 mm to ~46 mm on the y
axis in Figure 31.

5.3 Effects of Light Induced Degradation on Low-Cost Crystalline Silicon Solar Cell Performance

5.3.1 Electrical and Material Characteristics of Light Induced Degradation

The real challenge in solar cell research is to improve efficiency while decreasing the overall cost of production. High efficiency cells on crucible-grown single crystal Cz silicon have the potential for reducing the cost of PV. However, Cz Si cells tend to suffer some efficiency loss caused by LID of the bulk lifetime. A fundamental understanding of LID is necessary to reduce or eliminate LID to maximize the energy production from Cz Si modules. To accomplish this goal, LID was studied by effective lifetime measurements on 11 different Si samples (Table 4) with various resistivities (1-33 Ωcm) and different silicon ingot growth conditions and techniques. Boron doped Cz refers to conventional crucible-grown Si with high O_i (10-20 ppma). Cz-grown Si, using Gallium as the dopant, is referred to as Ga doped Cz. When a magnetic field is used during the growth of boron doped Cz, the O_i content can be controlled and reduced. This method is referred to as magnetic Czochralski (MCz) growth. In Table 4 B doped Float Zone Si with very low oxygen ($<5x10^{15}cm^{-3}$) is referred to as FZ.

First, the effective lifetime (τ_{eff}) was measured by photoconductance modulation using the quasi-steady-state (QSS) method on all the samples prior to cell fabrication. The stability of the effective lifetime before and after carrier injection via illumination was

Table 4. LID characteristics of various single crystal Si materials.

Measured at GT					
Material	Width (mils)	N_A (cm^{-3})	O_i (ppma)	No LID τ_{rec} (μs)[*]	LID τ_{deg} (μs)[*]
1 Cz Boron	15.5	2.20E+16	9.654	50	16
2 Cz Boron	15.5	2.23E+16	13.629	60	9
3 MCz Boron	15.5	2.65E+15	9.618	400	264
4 MCz Boron	15.5	1.24E+16	1.258	185	185
5 MCz Boron	15.5	2.90E+15	1.829	572	570
6 Fz Boron	15.5	2.47E+16	0	100	124
7 Fz Boron	15.5	3.41E+15	0	114	238
8 Cz Galium	10	5.71E+15	12.01	260	285
9 Cz Galium	10	3.37E+15	14.772	377	444
10 Cz Galium	10	4.04E+14	14.306	950	950
11 Cz Boron	15	3.10E+15	21.37	100	66

[*] *Effective lifetimes were measured at 1×10^{15} cm^{-3} injection level*

examined. Figure 33 shows the effective lifetime versus injection level of a B doped FZ sample, a B doped Cz sample, a B doped MCz sample with low O_i, and a Ga doped Cz sample, all with 4 to 5 Ωcm resistivity. The bottom two curves in Figure 33 represent the change in lifetime before and after trap generation. The curve of open squares was measured after a thermal anneal prior to trap formation. The curve of solid squares shows the resulting effective lifetime versus injection level curve after trap generation for 24 hours. Note that the largest difference in effective lifetime is at lower injection levels. Using the analysis outlined in Chapter 4, a plot of the SRH defect lifetime can be extracted according to eq. (29), proportional to N_t^*. In addition, Table 4 shows τ_{eff} values at a 1×10^{15} cm^{-3} injection level before and after 24 hour- LID under 1 sun illumination. It is clear from Table 4 that only samples containing both B and O_i suffered LID, demonstrating that both B and O in sufficient concentrations need to be present in a

sample for trap formation. The FZ sample with negligible O_i and the Ga doped Cz with negligible boron did not show any appreciable LID. In addition, MCz with only 1.25 ppma O_i also did not show significant LID. However, B doped Cz with >10 ppma O_i and $\geq 10^{16}$ cm^{-3} boron concentrations showed significant LID. These results have been confirmed and replicated in excellent research labs around the world.
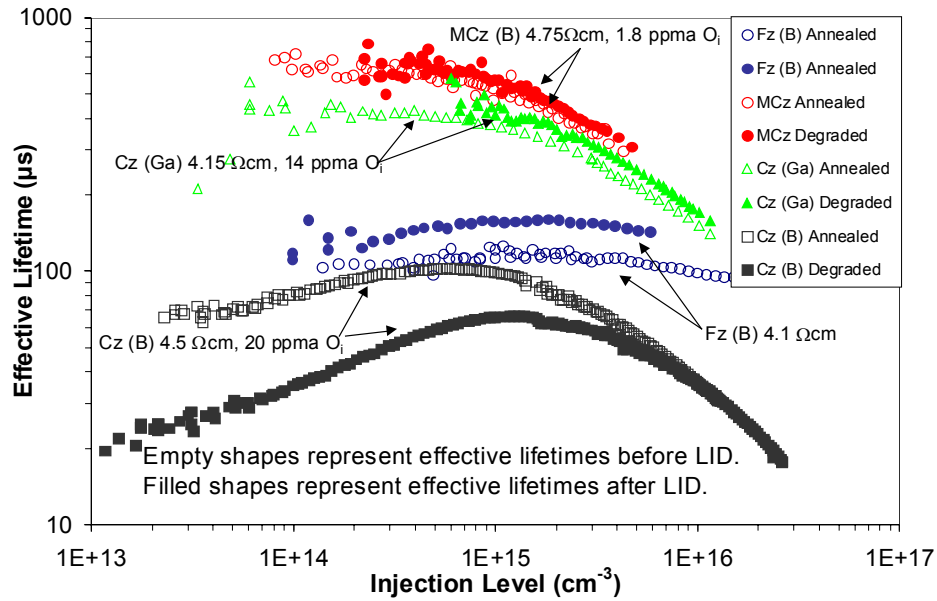
Figure 33. Effective lifetime measurements before and after illumination on similar resistivity Si crystal types. Investigation of LID effects in B doped FZ, Ga doped Cz, B doped MCz, and B doped Cz.

Figure 34 shows the measured Shockley-Read-Hall (SRH) lifetime resulting from the trap responsible for LID as a function of exposure time for two different resistivity (0.6 and 4.5 Ωcm) samples. This was accomplished by assuming that the degraded lifetime was only affected by LID traps and the original inherent traps remained constant and unchanged. Using eq. (2), $1/\tau_d = 1/\tau_a - 1/\tau_{eff2}$, τ_d was determined by measuring an

effective lifetime versus injection level before LID (τ_a) and after LID (τ_{eff2}). Illumination time was varied from a few minutes to a few days. Any decrease in the measured effective lifetime from the original annealed lifetime was attributed to the generation of the SRH traps responsible for LID. The slope of τ_d versus injection level is characterized by the ratio of τ_{no}/τ_{po}. Figure 34 reveals that the slope of the extracted SRH lifetime (τ_d vs Δn) remains independent of boron doping and illumination time. Both resistivities exhibit a constant τ_{no} to τ_{po} ratio, indicating a single trap with an increasing trap formation for longer exposure time causing a decrease in the extracted τ_d value (Figure 34). Using the analysis outlined in Chapter 4 confirms that the resulting lifetime data is caused by a single mid-gap SRH trap formation (Fig. 23).
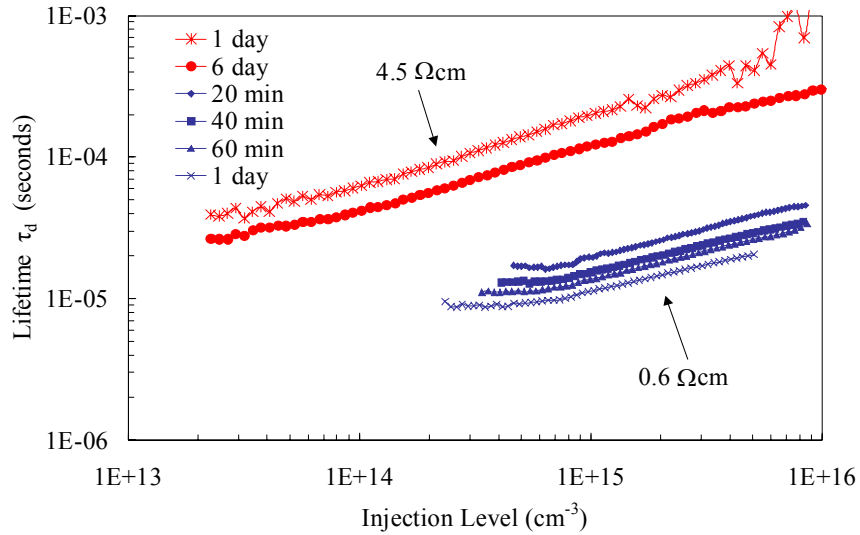
Figure 34. Injection level dependence of the trap responsible for LID. Rising slope reflects near mid-gap trap behavior.

5.3.2 Understanding and Mitigation of Light Induced Degradation in Single Crystalline Silicon Solar Cells

Industrial solar cells typically are ~300 μm thick, utilize screen-printed (SP) metal contacts, and use B doping in the base (with 10-20 ppma oxygen). Therefore, light induced degradation decreases the lifetime in Cz because of the formation of boron-oxygen complexes.   A decrease in bulk lifetime resulting from LID can have a significant impact on the final stabilized efficiency of commercial Cz silicon solar cells. To assess this impact, screen-printed solar cells were modeled using the PC1D device simulator [49]. Figure 35 shows calculated efficiency as a function of bulk lifetime for an industrial solar cell design.   Only the bulk lifetime was varied, while the FSRV (15,000 cm/s), BSRV (3000 cm/s), base resistivity (0.6 Ωcm), and all other pertinent parameters remained constant (Table 5).

Table 5. PC1D simulation settings.

Front Surface	Planar	Resistivity	0.6 Ωcm
Single layer ARC	n=2.0 t=79nm	FSRV / BSRV	15000 / 30000 cm/s
n-type diffusion	10^{20} cm^{-3} @ d=0.3μm 45 Ω/sq.	R_{sh} ,R_s,	100000 Ωcm^2, 1.0 Ωcm^2

Model calculations in Figure 35 show that for the 300 μm thick screen-printed (~16%) cells, the most drastic effects are observed only when the bulk lifetime falls below ~25

μs. For example, a 0.4% loss in absolute efficiency results when the bulk lifetime

decreases from 100 μs to 25 μs, but an additional 1.2% absolute efficiency drop occurs

when the bulk lifetime decreases from 25 μs to 5 μs.
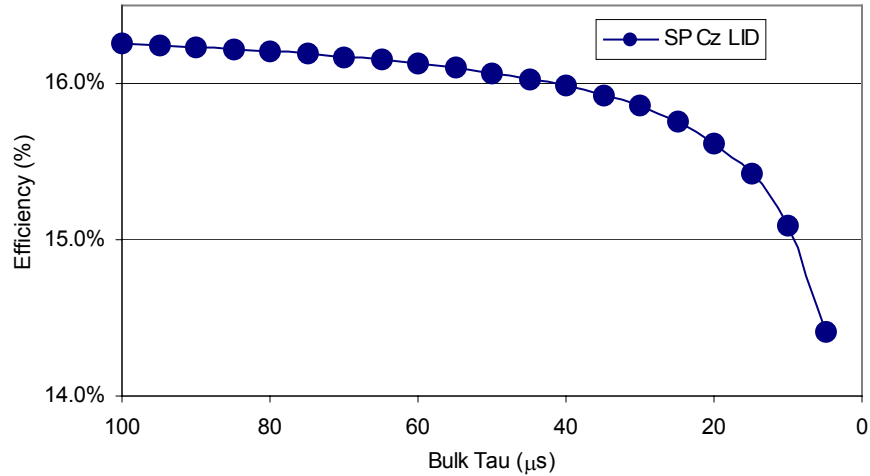
Figure 35. PC1D simulation of LID effect on solar cell efficiency.

After modeling the efficiency dependence of bulk lifetime for screen-printed cells, boron

doped Cz silicon cells were fabricated and subjected to LID. In addition to the B doped

Cz, single crystal Ga doped Cz, B doped magnetic Cz, and B doped FZ silicon are also

investigated in this chapter in order to understand and mitigate the LID effect in silicon

solar cells. Table 4 shows a detailed characterization of the 10 different crystals

investigated in this chapter. The base resistivity, interstitial oxygen, and measured bulk

lifetime before and after LID are all shown in Table 4. The oxygen concentration was

measured by Fourier Transform Infra-Red Spectroscopy using a Digilab FTS40-pro

spectrometer. Effective lifetime measurements were made using the QSS-PCD technique

shown in Figure 33 and recorded in Table 4 for a fixed injection level (1×10^{15} cm^{-3}) for all 11 samples.

In this research, industrial type planar cells were fabricated by high through-put belt line processing with screen-printed front and back contacts and a SiN$_x$ single layer ARC. Figure 36 shows a schematic diagram of the process sequence used to fabricate these industrial type solar cells on all four single crystal types (FZ, Ga Cz, B MCz, and B Cz). First, a conventional furnace diffusion was used to form the emitter using spin-on dopants. Next, SiN$_x$ was deposited for SLARC. After SiN$_x$ deposition, a screen-printed Al back surface field (BSF) was belt fired at 860°C. Finally, screen-printed Ag front contacts were fired in the belt furnace at 740°C.
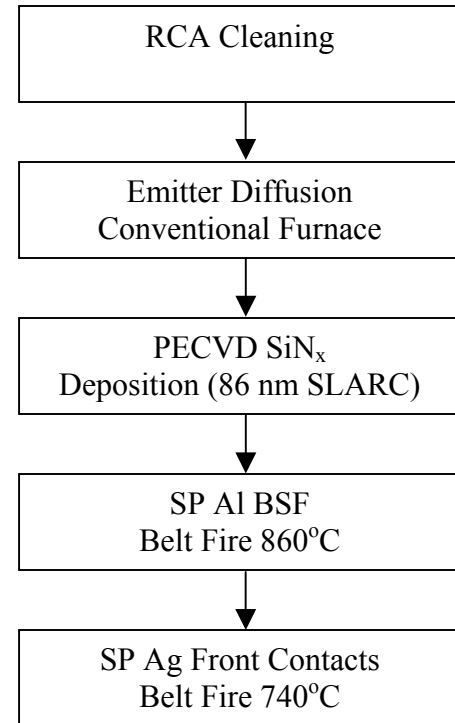
Figure 36. Process sequence diagram for single crystal SP solar cells used to analyze LID in finished devices.

All the cells were subjected to one-sun illumination at 25°C for 24 hours. Figure 37 shows that only the B doped Cz with high O$_i$ degraded from 16% to 15.2%, while the Ga doped Cz sample had an efficiency of 16.6% that did not degrade at all, consistent with the effective lifetime measurements made in Table 4 and Figure 33. Figure 37 shows the measured cell efficiency before and after 24

hours of light induced degradation for the B doped FZ (~0 ppma O_i), B doped MCz (1.2 ppma O_i), Ga doped Cz (12.0 ppma O_i), and a B doped Cz (9.6 ppma O_i). This was a promising result because there was no appreciable difference in the absolute efficiency of screen-printed Ga doped Cz and FZ cells. The B doped MCz with an efficiency in excess of 16% also showed a very small degradation because of the very low concentration of O_i (1.2 ppma). The loss in efficiency was less than 0.05%. Thus, both the Ga doped Cz and B doped MCz effectively eliminate or drastically reduce LID and produce cell performance comparable to screen-printed FZ cells (Fig. 34). This is consistent with the fact that the starting bulk lifetime in all three materials was >100μs (Table 4), and they do
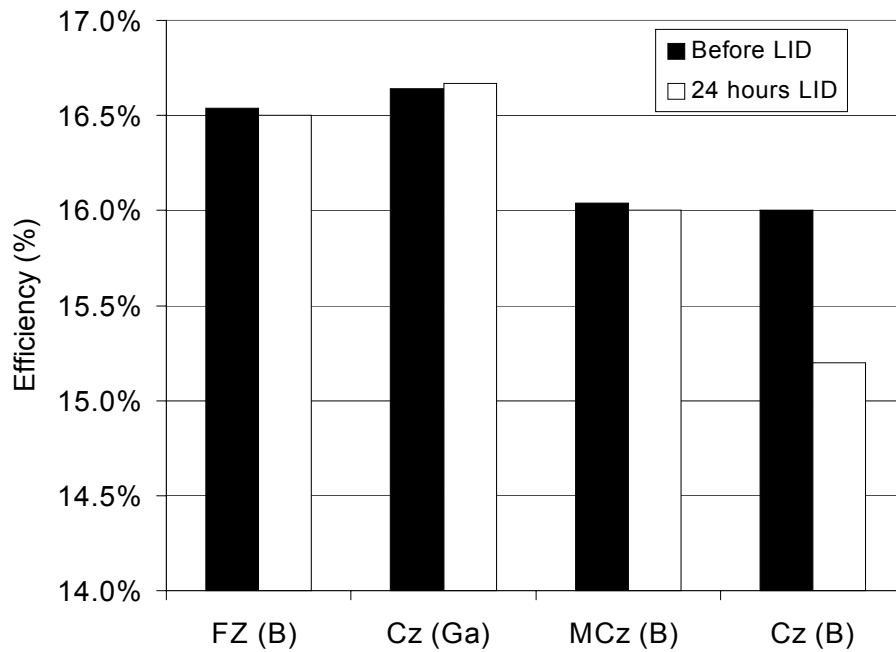
Figure 37. AM1.5 efficiencies for various single crystal silicon solar cells (400 μm) before and after 24 hours of one-sun illumination.

not suffer from any appreciable LID. Model calculations in Figure 35 show that the cell efficiency tends to saturate above 60 μs lifetime for this screen-printed cell design.

Simulated data in Figure 35 also agrees well with the LID behavior of 0.6 Ωcm Cz material, which had ~ 75 μs initial lifetime with an efficiency of 16%. After the LID, lifetime dropped to ~ 25 μs with an efficiency of 15.2%. It is important to note that these lifetimes were measured at low injection level ($< 10^{14}$ cm^{-3}) because the injection level under one-sun illumination is generally in the range of 5×10^{13} and 5×10^{14} cm^{-3}.

In Figure 37, cells were subjected to 24 hours of illumination to ensure full degradation. To investigate the rate of degradation, cell efficiency was also measured as a function of illumination time at 25°C. Figure 38 shows efficiency versus illumination time for the first 10 samples listed in Table 4. Only the B doped Cz samples suffered substantial efficiency loss as a result of LID, and it took more than two hours to reach full degradation. Starting efficiencies were somewhat lower in this experiment partly because
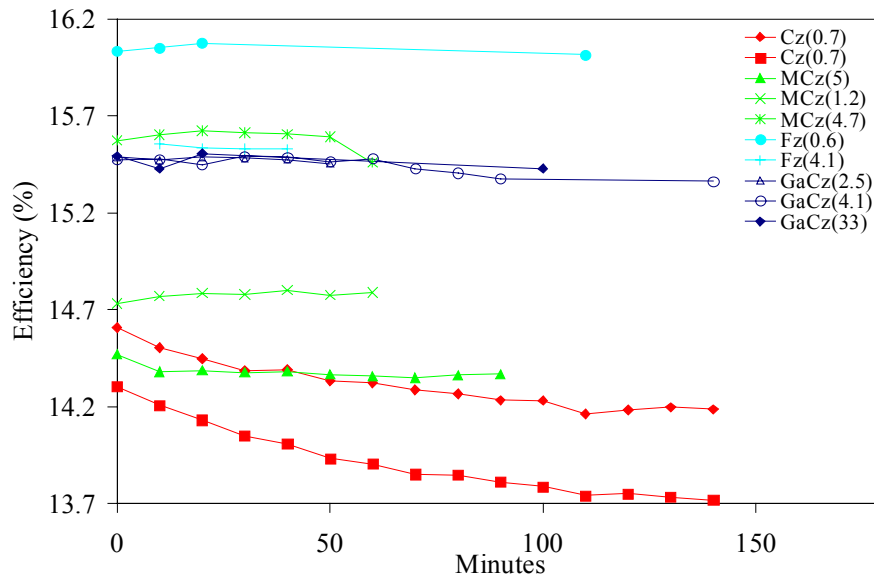
Figure 38. Efficiency degradation or stability for single crystal Si samples listed in Table 4.

belt furnace emitter diffusion (instead of a conventional tube furnace) from spin-on dopants was used for p-n junction formation. Screen-printed Cz cells in this study lost 0.7 to 1.2% absolute efficiency as a result of LID. The drop in efficiency was readily observed in the decreased long wavelength internal quantum efficiency (IQE), as shown in Figure 39. This also confirmed that LID was responsible for the efficiency degradation. It is important to note that ~1% loss in absolute efficiency for a 16% efficient cell amounts to a 6% reduction in the production capacity, or a $25 million/year loss in annual revenue (assuming a module cost of $4/W) for a 100 MW production line. Thus, this study clearly shows that efforts should be made to grow Ga doped Cz, low oxygen Cz, or MCz to eliminate LID in crucible-grown Cz. Another alternative is to modify cell designs to make the efficiency is less sensitive to bulk lifetime. One such approach is to reduce cell thickness. This is discussed in more detail in the following section.
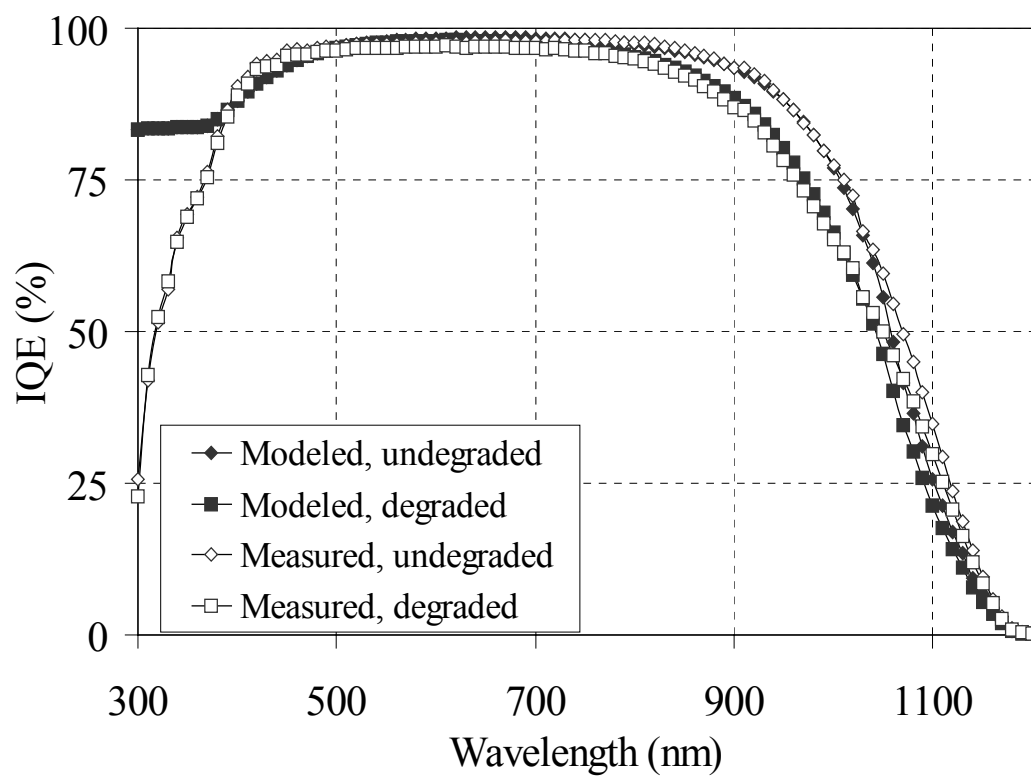
Figure 39. Measured and modeled IQE of the 254µm B doped Cz solar cell.

5.3.3 Solar Cell Design Parameters to Reduce or Eliminate Light Induced Degradation Effect on Efficiency

As shown earlier in this chapter, both the B doped MCz with limited O_i content and Ga doped Cz (instead of B doping) produced high efficiency manufacturable solar cells with stable efficiencies greater than 16%. These results provide future technology directions and offer two possible solutions to eliminating LID in PV grade silicon samples. However, industry is currently focused on traditional B doped Cz and therefore any methodology to increase stable solar cell efficiency using B doped Cz is highly desirable. One way to accomplish this is to have a cell design that correctly accounts for LID behavior of the material and is less sensitive to changes in bulk lifetime.

This section provides a comprehensive analysis of an approach involving appropriate cell design aimed at thickness optimization, which not only mitigates the impact of LID on cell efficiency, but also achieves relatively high stable efficiency without any reduction in LID trap density (N_T). Münzer et al. reported reduced efficiency degradation for thin Cz cells (100 μm) manufactured to test yield strength [45]. A combination of device modeling, cell fabrication, testing, and analysis of complete solar cells is used in this section to establish appropriate design of solar cells that are less sensitive to LID. The methodology involves reducing cell thickness and improving back surface recombination velocity (BSRV) to a point where the degraded diffusion length of the minority carrier remains more than 1.5 times the cell thickness. This will result in good electrical

confinement of the carriers without significantly sacrificing the optical confinement for a planar device. For example, the lifetime of a 100 μm thick sample needs to be only 10 μs to achieve a diffusion length that is 1.5 times the thickness ($L = (D\tau)^{1/2}$). It is important to recognize that reduced cell thickness not only decreases the efficiency degradation, but also reduces the cost. In this section, Cz silicon solar cells of varying thickness are fabricated and their performance measured before and after 24 hours of LID under one-sun illumination. An important consideration in design of thin solar cells (<200μm) is the back surface field (BSF). Aluminum is known to create warping and thus adversely affect manufacturability. Therefore, a boron BSF was implemented in this work in conjunction with thin wafers. The DOSS technique [50] was used to diffuse phosphorus and/or boron simultaneously from a limited source that allows for an in-situ oxide to be grown on both surfaces for passivation. No diffusion glass removal was necessary because the residual oxide was very thin. All solar cells fabricated in this study had a SiN_x single layer anti-reflection coating (SLARC).

Solar cells were fabricated on 0.7 Ωcm B doped Cz-Si (9.6 ppma O_i) with varying thicknesses (100 μm to 400 μm). These samples were subjected to a single step DOSS process at 925°C that resulted in a light phosphorus emitter diffusion (80-120 Ω/sq.), transparent boron BSF (110 Ω/sq.), and a 20 nm in-situ oxide for passivation. The B BSF was used to avoid warping caused by Al BSF formation on thin Si. Effective lifetime using the quasi-steady-state PCD method [51] was measured prior to metallization. Front and back contacts were applied by photolithography and metal evaporation. Evaporated point contacts were used on the transparent B BSF passivated with a 20 nm oxide. Cells

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were measured immediately following a 15-minute forming gas anneal (FGA) at 400°C in a CF and then subsequently degraded for 24 hours under one-sun illumination and remeasured. The internal quantum efficiency (IQE) was measured using an OL Series 750 Automated Spectroradiometric Measurement System from Optronic Laboratories, Inc. both before and after light-induced degradation. The difference or loss in IQE at each wavelength was plotted to assess the performance degradation over the entire solar spectrum.

Figure 40 shows the measured loss in IQE in the long wavelength range resulting from LID for the cells with varying thicknesses. This data clearly shows that LID was most evident in the long wavelength range (>800 nm). This was expected because long
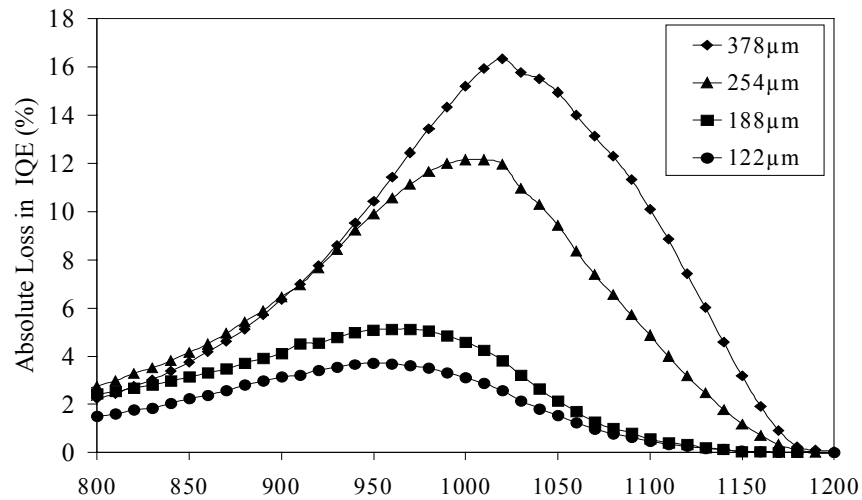
Figure 40. Measured LID in IQE in the long wavelength range for cells. with varying thickness.

wavelength response is much more sensitive to bulk lifetime. More significant is the fact that thinner devices suffer less LID. The measured IQE was modeled using PC1D [49], following extended IQE analysis of the degraded and undegraded cells. An excellent match between the measured IQE and calculated IQE (See Fig. 39) revealed that the bulk lifetime degraded from 75 to 20μs after 24 hours of LID in these B doped Cz cells.

Using these cell parameters and a PC1D quick batch file, degraded (20 μs) and un-degraded (75 μs) devices were simulated and the efficiency difference was plotted as a function of cell thickness to show that thin cells suffer much less from light-induced degradation than the thick cells (Fig. 41), regardless of BSRV. Further modeling was performed to determine the optimum thickness that would result in the highest stabilized cell efficiency and significantly reduced LID. Plots in Figure 42 show the optimum thickness determined for the stabilized lifetime (20 μs) as a function of BSRV for solar cells with 100-to-400 μm thickness. When the BSRV is extremely high, $>10^6$ cm/s, surface isolation is desirable for the highest efficiency. Therefore, increased cell thickness (~400 μm) results in the higher efficiency shown in Figure 42. However, once the BSRV drops below 5×10^4 cm/s for a 20 μs device, a peak in efficiency is observed at ~150 μm, as shown in Figure 42.
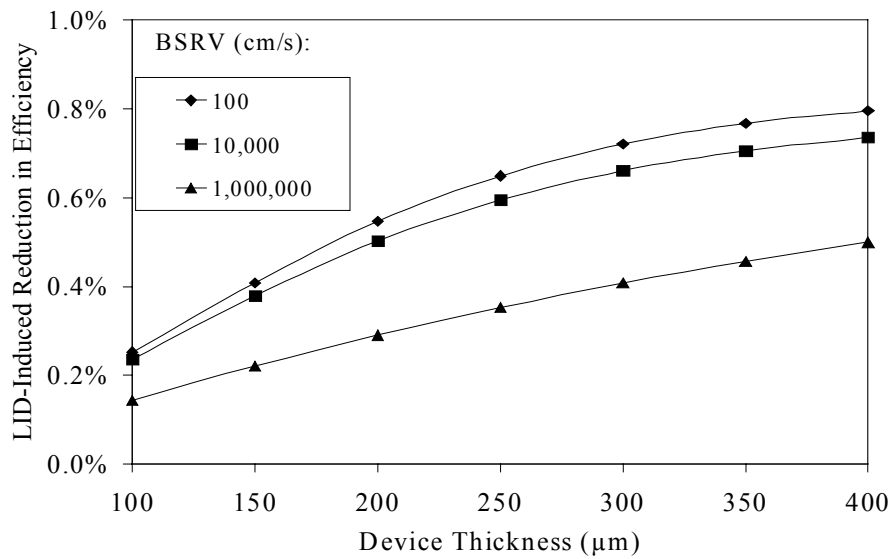
Figure 41. PC1D modeling of the effect of LID on efficiency in Cz Si solar cells that suffer bulk lifetime degradation from 75 to 20 μs.
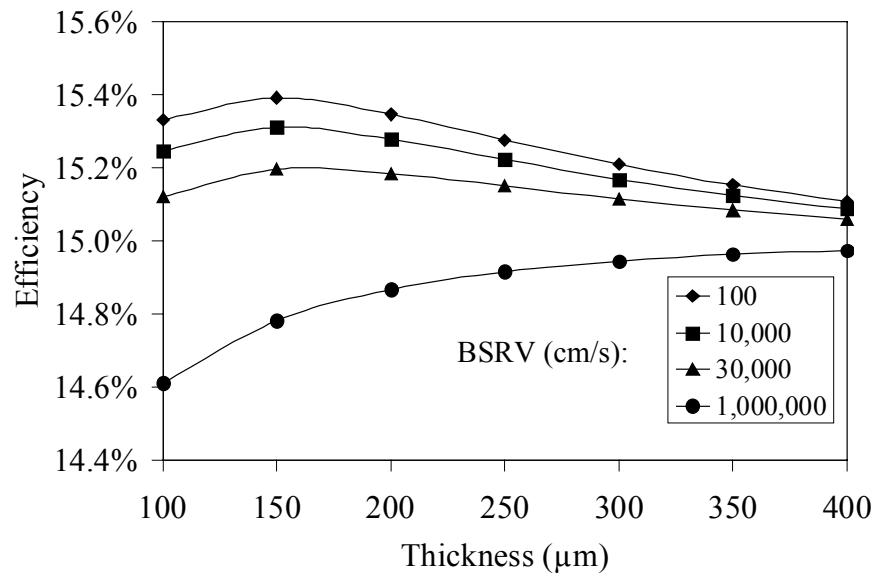
Figure 42. PC1D modeling of the effect of BSRV on the optimum thickness and efficiency of light degraded Cz Si solar cells with 20 μs bulk lifetime.

To support the above model calculations, cells of varying thicknesses were fabricated and analyzed before and after LID. Table 6 shows the decrease in V_{oc}, J_{sc} and cell efficiency of these cells before and after 24 hours of one-sun LID. As expected, the long wavelength response was lower for degraded solar cells. The magnitude of current loss in thicker solar cells is clearly greater than in thinner solar cells. As the thickness decreases so does the effect of the lifetime degradation on short circuit current density (J_{sc}) and cell efficiency. It is important to recognize that the LID of the bulk lifetime is independent of thickness. The reduction of current loss in thinner devices is not due to improved bulk lifetime but is the result of increased probability of carrier collection from the higher effective diffusion length (L_{eff}) to thickness ratio.

The reduction in current loss for the thinner device structures was supported by the decreased loss in cell efficiency (Table 6). Figure 43 shows the starting cell efficiency as well as the efficiency degradation before and after 24 hours of ~one-sun illumination for six cells with different wafer thicknesses. The degradation in absolute efficiency

Table 6. Light induced degradation in V_{oc}, J_{sc}, and
efficiency of B doped Cz cells with varying
thicknesses.

Cell ID	Thickness	ΔV_{oc}	ΔJ_{sc}	ΔE_{ff}
Cz1n-1-2	378 μm	12.18 mV	1.03 mA/cm^2	0.75 %
Cz1n-2-2	330 μm	8.92 mV	0.81 mA/cm^2	0.57 %
Cz1n-3-2	254 μm	10.55 mV	0.51 mA/cm^2	0.49 %
Cz1n-4-2	187 μm	6.61 mV	0.02 mA/cm^2	0.15 %
Cz1n-5-2	157 μm	7.88 mV	0.19 mA/cm^2	0.24 %
Cz1n-6-2	122 μm	2.73 mV	0.07 mA/cm^2	0.10 %

decreases as the wafer thickness is reduced. This is consistent with the model calculation

shown in Figure 41. In addition, the optimum cell thickness changes after LID. For

example, the optimum cell thickness prior to LID is 253 µm (Fig. 43), while the best

efficiency after the LID has a broad peak between 253 and 157 µm. The 157 µm

thickness is more desirable for this material because it reduces the cost of Si material

significantly while producing nearly the maximum stable efficiency. Stable efficiencies

after degradation ranged between 15.3% and 14.8% for all the samples, as shown in

Figure 43. Thinner cells with a reasonable BSRV are less sensitive to lifetime

degradation as long as the diffusion length is comparable to or greater than the cell
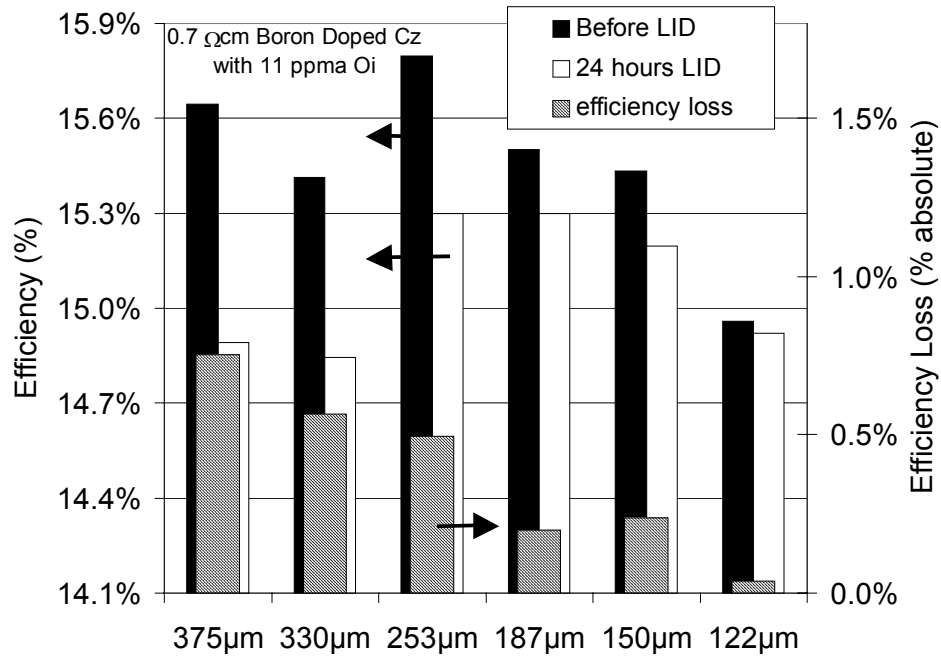
Figure 43. Degraded and undegraded efficiencies for B doped Cz Si
solar cells for varying wafer thicknesses.

thickness. This is supported by the model calculations in Figure 44, which shows that for

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the observed degradation in lifetime (from 75 μs to 20 μs), the 400 μm thick cell with a

BSRV of 30,000 cm/s, suffers ~0.8% loss in absolute efficiency, while the 150 μm

sample decreases by only ~0.3%.   These calculated values match well with the

experimental data in Table 6.
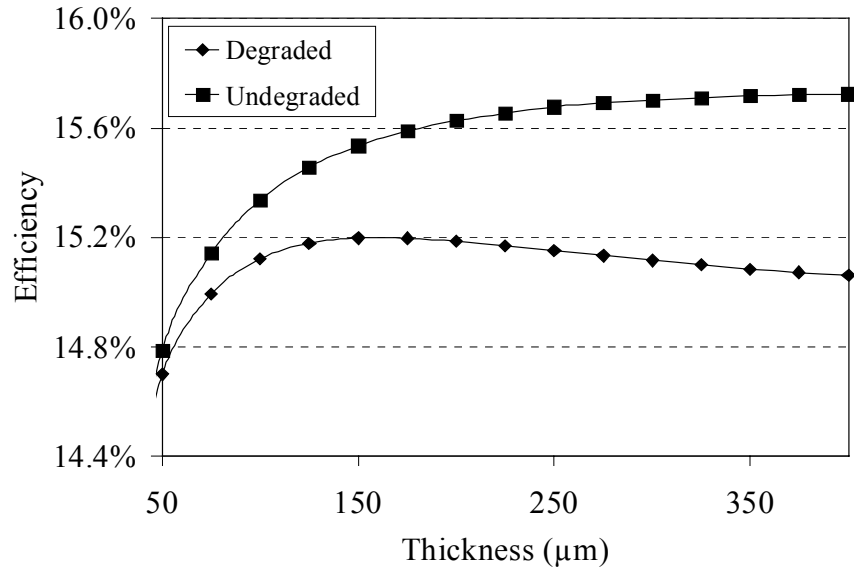
Figure 44. PC1D modeling curve showing the effect of LID as a
function of thickness (BSRV = 30,000 ^{cm}/s).

The true figure of merit should be the stabilized cell efficiency after the degradation for

Cz silicon solar cells. Model calculations in Figure 42 show that there is an optimum

thickness of ~150 μm, which maximizes the stabilized efficiency for devices with a 20 μs

lifetime after LID and a BSRV in the range of 100 to 10^5 cm/s. This was consistent with

the experimental results, which showed that for this Cz material and cell design, where

lifetime degraded from 75 μs to 20 μs with a BSRV ~ $3x10^4$ cm/s, the optimum thickness

for the highest stabilized efficiency was ~150 μm. Reducing the thickness below this

value reduces the light induced efficiency degradation (Fig. 41 and Table 6), but it also lowers the stabilized cell efficiency (Figs. 42, 44, Table 6).

5.4 Conclusions

Degradation and recovery of LID traps are affected differently by heat and illumination. This could lead to process-induced lifetime degradation in lamp-heated furnaces such as widely used belt and RTP systems. Significant lifetime degradation was observed in a lamp heated belt furnace up to 600^oC, while full recovery was observed in the RTP at temperatures $\geq 300^o$C. The creation and annihilation of traps responsible for LID occur independently of each other and at the same time at temperatures over 200^oC. During RTP heating, the trap annihilation rate exceeds the generation rate at temperatures > 300^oC, while in belt processing this occurs at temperatures above 600^oC. The observed difference in the LID behavior during RTP and BF processing at the same temperature is attributed to the difference in the optical spectrum and/or photon flux during a given heating cycle coupled with the amount of thermally activated traps. Since commercial Cz cells are frequently processed in the lamp-heated belt furnace in the temperature range of 500 to 900^oC, this investigation shows that processed devices may suffer partially from LID. In addition, it was shown that charged carrier transport by diffusion, as well as injection, results in trap formation. The trap formation rate for a given resistivity sample was shown to arise from the creation of one mid-gap trap. A constant τ_{no}/τ_{po} ratio was maintained as degradation time increased, supporting the SRH analysis that a single mid-gap trap was responsible for bulk lifetime degradation.

This chapter also showed that by controlling the cell design parameters, it is possible to reduce LID and optimize stabilized cell efficiencies for B doped Cz solar cells. A combination of device modeling and actual cell fabrication was used to demonstrate that reducing the cell thickness for B doped Cz solar cells from 378 μm to 157 μm reduces the LID effect on efficiency and produces a higher stabilized SP cell efficiency of 15.2% compared to 14.8%. Light induced efficiency degradation is also shown to be a function of BSRV. Higher BSRV results in lower LID, but it also lowers overall cell efficiency. It was also shown that the optimum thickness can be calculated from the LID of minority carrier lifetime and the BSRV of the cells. For the Cz material used in this study, which gave a 20 μs lifetime after degradation, the optimum cell thickness for planar devices was found to be in the range of 150 to 250 μm. In addition, efficiency degradation was reduced from 0.75% to 0.24% when the cell thickness was decreased from 378 to 157 μm, thereby representing a reduction in cell thickness by more than a factor of two. *This combined with higher stabilized cell efficiency, should significantly reduce the cost (in $/W) of Cz solar cells.*

CHAPTER 6

6 LIGHT INDUCED DEGRADATION IN CAST MULTI-CRYSTALLINE AND RIBBON SILICON

6.1 Efficiency Degradation in Industrially Screen-Printed Multi-Crystalline Silicon Solar Cells

In the previous chapters, the conditions for LID trap generation and annihilation were investigated: the impact of LID on single crystal Si materials, the elimination or reduction of LID by Ga doping or reduced oxygen concentration, and the mitigation of degradation on cell efficiency through cell thickness reduction were investigated. This chapter deals with the investigation of LID in low-cost PV grade Si materials, with special emphasis on multi-crystalline silicon (mc-Si). More than 55% of current PV modules in production use cast mc-Si wafers. Three of the most promising mc-Si materials are investigated for light induced degradation in this thesis. Cast mc-Si grown by the Heat Exchanger Method (HEM), String Ribbon (SR) grown by Evergreen Solar, and Edge-Defined Film-Fed Growth (EFG) by ASE (RWE Schott), are analyzed along with Cz and FZ Si. To check for the characteristic degradation/recovery cycle (discussed in Chapter 4) resulting from LID in the low-cost promising silicon materials, first, phosphorus gettering with in-situ oxidation for passivation was performed to increase the bulk lifetime to a high enough level so LID could be detected. Low lifetime materials (< 5 μs) tend to mask LID because degradation effects are only significant in Cz Si with lifetimes between 10 and 1000 μs. Subsequently, SiN_x was deposited on both sides of the wafer for enhanced surface passivation and ease of handling during measurements. Lifetime measurements

were made using the quasi-steady-state photoconductance (QSSPCD) lifetime technique to assess the impact of LID. Additional samples were prepared for lifetime measurement by etching the solar cell down to bare Si and coating it with a SiN_x layer for surface passivation on both sides. Complete screen-printed solar cells were fabricated and analyzed after various exposures to illumination and annealing to study the degradation and annealing cycle. In the case of HEM Si, thick wafers were sliced to measure the oxygen concentration as a function of ingot position. Interstitial oxygen concentration was measured by Fourier Transform Infra-Red (FTIR) spectroscopy, using a Digilab FTS40-pro spectrometer. In addition, a room-temperature scanning photoluminescence technique was used for lifetime mapping of wafers with and without LID [52]. This is important because oxygen and defect concentration could vary significantly over a given mc-Si wafer, which could result in spatial variation in LID. This lifetime mapping technique can provide information about LID effects in the vicinity of defects relative to high lifetime regions.

Initial lifetime measurements were performed on phosphorus gettered mc-Si samples. Figure 45 shows the area-averaged lifetime data obtained by QSSPCD at 5×10^{14} cm^{-3} injection level. Cast mc-Si, EFG, and web showed detectable degradation/recovery. Only the SR sample did not show LID, probably because the very low lifetime acted to obscure the LID, coupled with low oxygen concentration.

Complete manufacturable screen-printed solar cells were fabricated and analyzed before and after LID. Depending on the base material, an optimized screen-printed cell
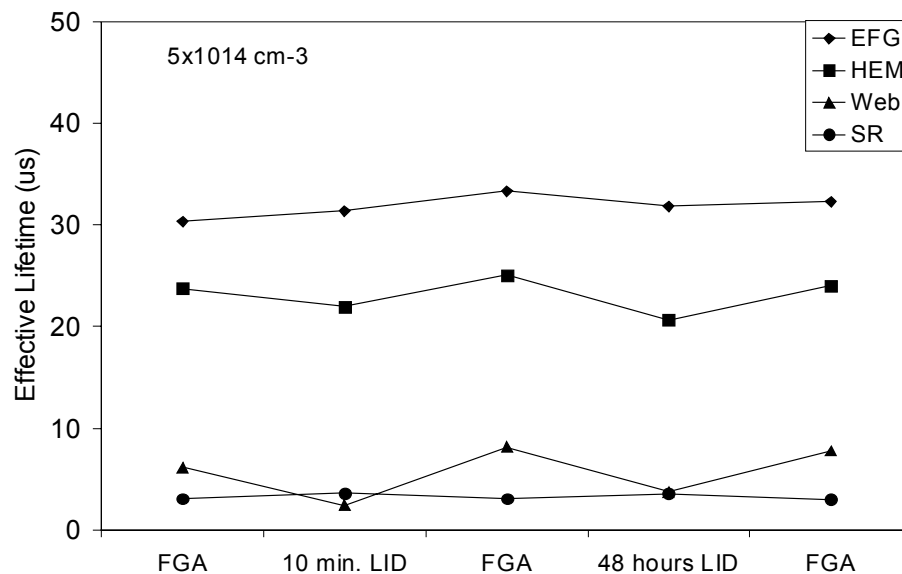
Figure 45. QSSPCD effective lifetime data for ribbon and cast mc-Si.

fabrication sequence was used. All samples had a conventional furnace diffused emitter and a screen-printed Al BSF. Deposition of a ~78 nm SiN layer for SLARC by PECVD was applied to all samples, but the screen-printed Ag front contacts were different for each crystal type. In addition, the front contact firing time and temperature were also unique to each crystal type. The firing temperature is tailored to optimize hydrogenation. Figure 46 shows the LID on screen-printed (SP) mc-Si solar cells. Cell efficiencies on all the materials (except dendritic web, where the ~100 μm thickness and somewhat lower efficiency obscured degradation) before LID were over **15%**. Cell efficiencies after 24

hours of one-sun illumination, where cell temperature was allowed to float, are also plotted in Figure 46. The cell temperature during degradation was measured to reach temperatures above 75°C during extended illumination at a one-sun intensity. Again, FZ and Ga doped Cz showed no degradation in cell performance but B doped Cz with high O_i content showed significant LID. In addition to the B doped Cz (0.8 Ωcm) solar cells, the HEM (1.5 Ωcm), EFG (~3 Ωcm), and SR (~3 Ωcm) cells also showed LID, but not as much (See Fig. 46). The B doped Cz sample showed a ~1% drop in absolute efficiency compared to only a 0.2% decrease in absolute efficiency for the other materials. Notice that the SR material, after the phosphorus gettering, did not show significant degradation
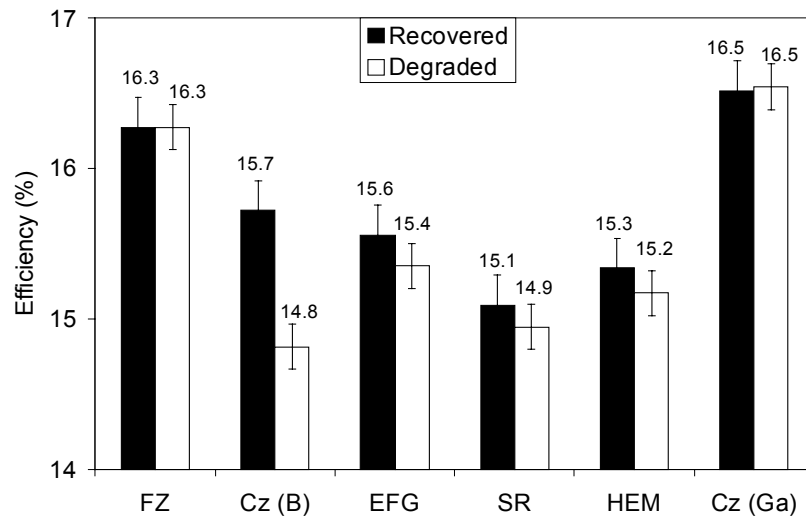
Figure 46. Average efficiency change after four degradation / recovery cycles for mc-Si solar cells.

(See Fig. 31), but a small and reproducible light induced efficiency degradation was observed in the cells during four consecutive degradation/ recovery cycles. This is because the bulk lifetime in the cells is much higher than the as-grown or even phosphorus gettered samples because of SiN induced defect hydrogenation in the finished

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devices [47]. Ribbon silicon solar cells have been shown to have an area-averaged lifetime of ~30–100 μs after cell processing optimized for hydrogenation.

Materials used in Figure 46 are known to have different oxygen concentrations. To understand the role of oxygen on LID in these materials, O_i concentration data was obtained for these materials from the literature as well as from private communications. Table 7 summarizes the most recent data available or reported, to our knowledge, on interstitial oxygen (O_i) content in these promising crystalline Si materials.

Table 7. Interstitial oxygen O_i concentration in promising crystalline Si materials [53,54].

	(O_i) cm^{-3}
Float Zone (FZ)	$<10^{15}$
String Ribbon (SR)	$4\text{-}8 \times 10^{16}$
Edge defined Film-feed Growth (EFG) sheets	$<5 \times 10^{16}$
Heat Exchanger Method (HEM)	$<4 \times 10^{-17}$
Dendritic Web	10^{18}
Boron doped Czochralski (Cz)	$\sim 10^{18}$
Boron doped Magnetic Czochralski (MCz)	$10^{16}\text{-}5 \times 10^{17}$
Gallium doped Czochralski (Ga Cz)	$\sim 10^{18}$

The oxygen concentration has varied over the years as ribbon growth techniques have evolved. Moreover, in the case of the cast mc-Si ingot, the O_i concentration is often dependent on position within the ingot. Therefore, in this study, thick mc-Si wafers were

also obtained from different locations to determine the oxygen concentration by FTIR as a function of ingot position. Figure 47 shows the room-temperature FTIR spectra as a function of ingot position for the oxygen interstitial peak in a directionally solidified HEM ingot. The oxygen concentration was found to increase from top to bottom of the ingot, with a saturation of O_i content near the bottom. Figure 46 shows that we were able to achieve very respectable SP cell efficiencies ($\geq$15%) on these low-cost mc-Si materials. Despite the varying O_i content and base doping level, the ribbon and cast mc-Si screen-printed efficient cells (~15%) showed similar light induced efficiency degradation (0.2% absolute). To understand the reason for this, a detailed investigation
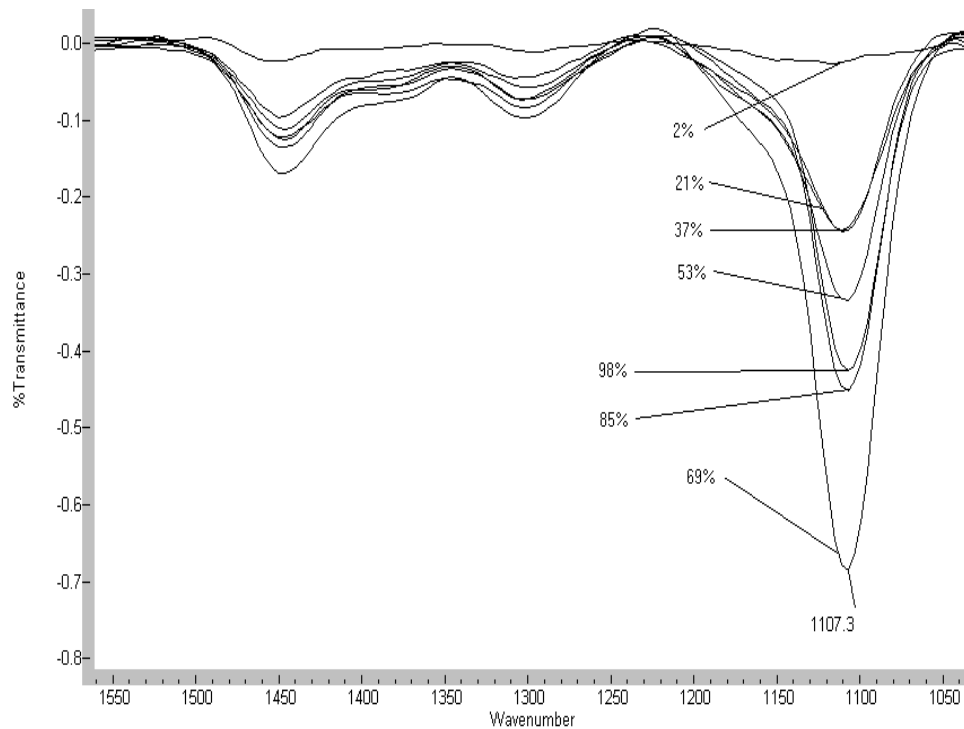
Figure 47. Room-temperature FTIR spectra that show the relative O_i concentration (wavenumber = 1107 cm^{-1}) in HEM mc-Si as a function of wafer position from the top of the ingot (2%) to the bottom of the ingot (98%). Detection limit ~ 5×10^{16} cm^{-3}.

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was performed using QSS effective lifetime in the fully processed ribbon materials, and spatially resolved photoluminescence measurements were made. Figure 48 demonstrates that the fully processed EFG Si sample with good lifetime displayed the characteristic degradation curve for the minority carrier lifetime as a function of injection level. This EFG sample showed LID in lifetime from 30 μs down to 22 μs at the $5x10^{14}$ cm^{-3} injection level. The degradation is less pronounced at the higher injection level, which is consistent with the reported characteristics of the LID trap [31].
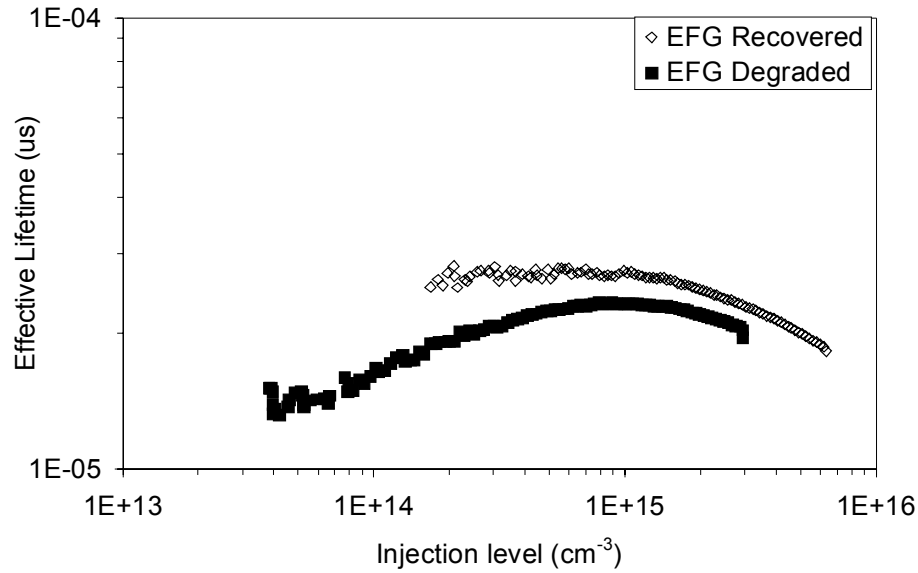
Figure 48. τ_{eff} vs. injection level for processed and hydrogenated EFG Si. "Recovered" is before LID and "Degraded" is after.

6.2 Efficiency Degradation in Laboratory Photolithography Multi-Crystalline Solar Cells

Variability in defect distribution leads to a higher spread in the efficiency of low-cost materials. The LID effect is expected to be more pronounced in higher efficiency cells. Therefore, additional samples were examined to understand and quantify the LID effect in very good mc-Si cells. Table 8 shows the change in important solar cell parameters for these materials. Preliminary investigations of LID in very high efficiency SR (>17%) and EFG (~16%) cells made with photolithography front contacts (initial V_{oc}= 619 and 612 mV respectively) showed a higher (0.5% and 0.9%) efficiency degradation compared to the >15% SP cells in Figure 46. Further investigation is required to determine if this was the result of higher than normal oxygen in these ribbon samples, or higher starting efficiency and other factors, such as high sample temperature during illumination used for degradation. Table 8 also shows that screen-printed SR and EFG cells with efficiencies in the range of ~13.5 to 15% showed negligible degradation because the lower bulk lifetime in these finished devices obscures the degradation of efficiency.

Table 8. Efficiency degradation after 3 days' illumination of ~0.5 suns for various efficiency mc-Si wafers.

mc-Si type	ΔV_{oc} (mV)	ΔJ_{sc} (mA/cm^2)	ΔEff. (%)	Comments
SR 17.1%	9.1	0.44	0.50	Photo-lithography contacts
SR 13.3%	0.0	0.0	0.00	Screen-Printed contacts
EFG 16.0%	19.0	0.93	0.90	Photo-lithography contacts
EFG 14-15%	0.0	0.01	0.03	Screen-Printed contacts
HEM 15.6%	4.0	0.47	0.28	Screen-Printed contacts
HEM 15.3%	2.0	0.13	0.04	Screen-Printed contacts

Interestingly, the two screen-printed cast mc-Si HEM samples in Table 8 with comparable efficiencies of ~15.5% showed different amounts of efficiency degradation (0.3% and 0.04%). This is possibly due to the difference in O_i content of these two wafers that may have come from different ingot positions, as shown in Figure 47 and [5]. Thus, more accurate knowledge of O_i and defects is needed to properly explain the variation in the LID behavior obscured in these materials.

6.3 Understanding and Investigation of Spatial Dependence of the Metastable Defect (Light Induced Degradation) in Cast Multi-Crystalline Silicon

To further improve the understanding of the effect of LID in the ribbon materials, a spatially resolved photoluminescence (PL) mapping technique was applied. The PL mappings and spectra were analyzed using a Spex 500M grating spectrometer coupled to a liquid nitrogen cooled Ge detector. The optical pump was an 800 nm AlGaAs laser diode with a 10 nm bandwidth operating in a pulse mode (a peak power of 140 mW). The target sample was placed on an X-Z motion stage to generate a spatially resolved lifetime map using a statistical relationship to approximate effective lifetime values for samples being measured. This technique gives a map of the band-to-band PL intensity peak at

Figure 49. Room-temperature PL spectra in the area with a high (1) and low (2) minority carrier bulk lifetime. The defect band at about 0.8 eV is observed only in low lifetime regions of EFG and cast mc-Si wafers [51].

the energy of 1.09 eV along with the intensity map of a "defect" band with PL peak at ~0.8 eV for some mc-Si samples like EFG ribbon silicon (See Fig. 49). Using the band-

to-band intensity (I_{bb}) values, it is possible to quantify the minority carrier lifetime through the following relationship [52] :

$$I_{bb} \sim \frac{\tau_{rad}^{-1}}{\left(\tau_{rad}^{-1} + \tau_{nr}^{-1}\right)} \qquad (38)$$

where I_{bb} is the intensity of the band-to-band recombination, and τ_{rad} and τ_{nr} are the radiative band-to-band lifetime and non-radiative lifetime, respectively. The non-radiative lifetime is dominant in silicon at room temperature and is proportional to the measured effective lifetime (τ_{eff}). The relationship described in eq. (38) is based on probability. The τ_{rad} is a material constant for a given doping density and is much larger than the τ_{nr} in Si. The I_{bb} is controlled by the non-radiative lifetime because if the non-radiative lifetime is long, more radiative recombination events will occur in direct proportion to the τ_{nr}, provided the carrier injection level is below ~10^{18}cm^{-3}, where Auger recombination is not a factor. Using the above information and eq. (38), the following relationship is obtained through simplification:

$$I_{bb} \sim \tau_{nr} \Big/ \tau_{rad} \sim \tau_{eff} \Big/ \tau_{rad} \sim \tau_{eff} \qquad (39)$$

This enables the analysis of the effective normalized LID trap concentration (N_{LID}^{*}), similar to what is used in the photoconductance lifetime measurements described in Chapter 4 [39]:

$$1 \Big/ \tau_{SRH} (ll) \cong 1 \Big/ \tau_{no} = \sigma_n v_{th} N_t \qquad (40)$$

$$1 \Big/ \tau_{SRH} (ll) \cong 1 \Big/ \tau_{nr} \cong 1 \Big/ \tau_{eff} \qquad (41)$$

Using the same relationship established in Chapter 4 with the Shockley-Read-Hall lifetime approximation at low-level injection, the change in effective lifetime (or the

lifetime resulting from the trap only) resulting from LID trap formation can be written in terms of the effective SRH lifetime with the LID trap (τ_{eff}) and SRH lifetime without the LID trap after the trap anneal (τ_a) as follows:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_a} + \frac{1}{\tau_d} \tag{42}$$

$$\frac{1}{\tau_d} = \frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_a} = N_t \sigma_n \upsilon_{th} \Rightarrow N_t^* \tag{43}$$

$$I_{bb} \sim \frac{\tau_{\text{eff}}}{\tau_{\text{rad}}} \sim \tau_{SRH}(ll) \sim \tau_{no} = \frac{1}{\sigma_n v_{th} N_t} \tag{44}$$

$$N_{LID}^* = I_{bb}(\deg)^{-1} - I_{bb}(rec)^{-1} \tag{45}$$

$$N_{LID}^* = \frac{\tau_{\text{rad}}}{\tau_{\text{eff}}} - \frac{\tau_{\text{rad}}}{\tau_a} = \tau_{\text{rad}} N_t^* \tag{46}$$

$$N_{LID}^* = \tau_{\text{rad}} N_t^* \tag{47}$$

where σ_n is the electron capture cross section of the trap, υ_{th} is the thermal velocity of electrons, and N_{LID}^* is a unitless number referred to as the effective normalized trap concentration determined from the measured change in band-to-band PL intensity in the recovered lifetime state $I_{bb}(rec)$ and degraded lifetime state $I_{bb}(deg)$. Figure 50 shows two spatially resolved PL maps of a B doped Cz-Si wafer before and after LID. The PL maps show a uniform distribution of the intensity ($\sim N_{LID}^*$) across the entire wafer in the degraded state, as well as the recovered state in the single crystal B doped Cz Si sample. The resulting spatially averaged N_{LID}^* was 0.019. PL maps were also obtained for all multi-crystalline Si wafers passivated with SiN_x on top and bottom surfaces. Preservation of the bulk lifetime increases the signal-to noise ratio by minimizing the surface effects. For some types of low-cost ribbon crystalline silicon, an additional set of
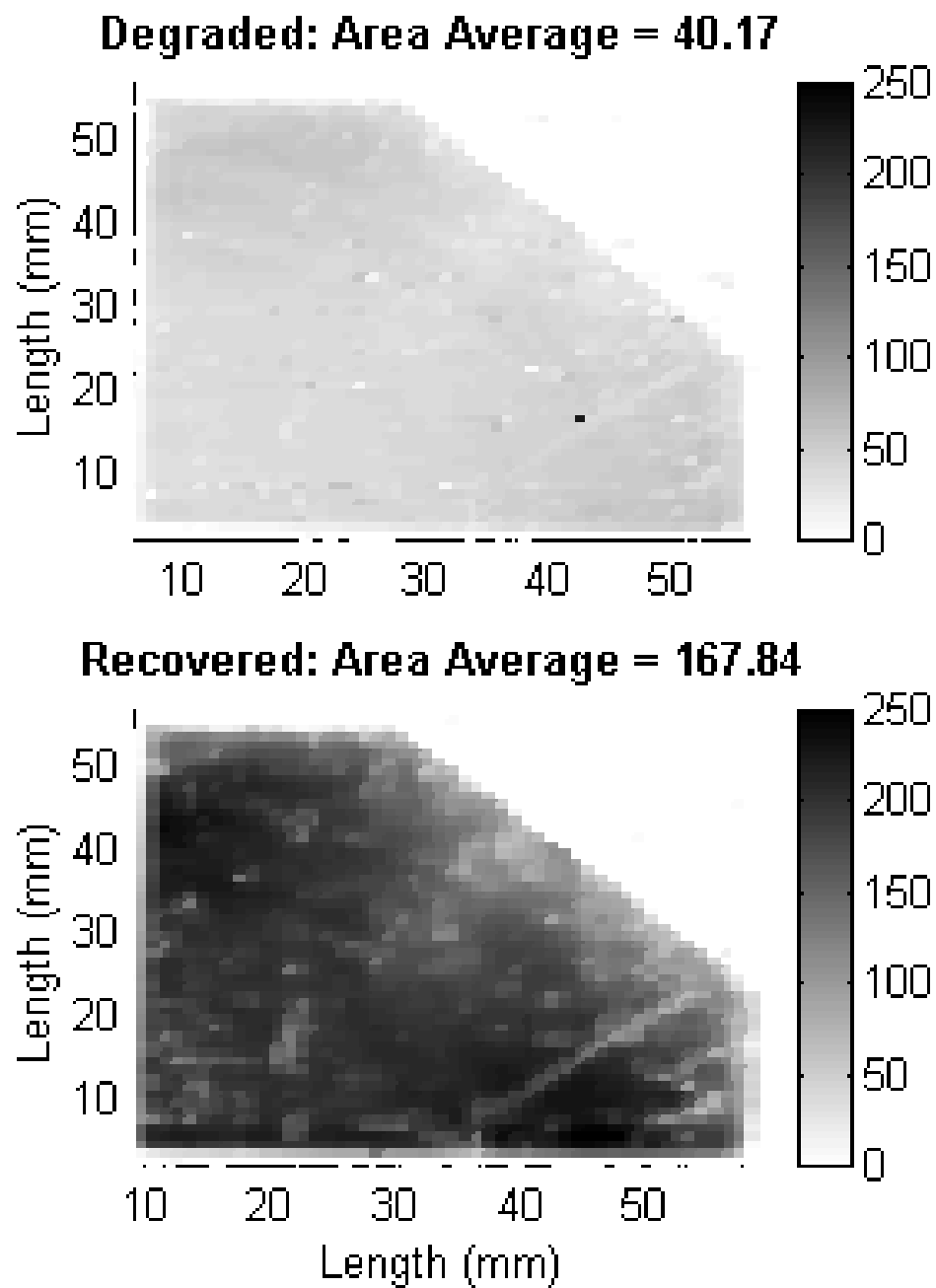
Figure 50. PL map of a quarter B doped Cz Si wafer before and after LID.

data is often possible using this technique associated with a sub-band gap radiative recombination event in highly defective regions (low lifetime regions).

Radiative recombination in defective materials gives rise to a broad peak at ~0.8 eV [52] (See Fig. 49). It is important to note that a higher intensity measurement of a band-to-band PL directly corresponds to a higher effective lifetime (more intensity results from longer effective lifetime, which increases the probability of a radiative band-to-band event), while a high intensity defect band signal signifies a low effective lifetime region.

Figure 50 demonstrated the ability of this technique to correctly identify the spatial behavior of the trap responsible for LID. In traditional B doped Cz Si, the trap is uniformly distributed in both the degraded and recovered state. This was anticipated because of the high-quality single crystalline structure of the Cz sample with a uniform distribution of O_i and B. However, cast mc-Si and ribbon silicon samples do not have a uniform crystalline structure and the ribbon silicon samples contain a much higher level of defects, dislocations, and impurities. Using the band-to-band PL wavelength spectra to map the effective lifetime of these materials in both the degraded and annealed state provided a deeper insight into the distribution and presence of the metastable defect responsible for LID. Figures 51, 52, and 53 show the PL effective lifetime map (band-to-band intensity) for three different octagon-shaped HEM cast mc-Si wafers before and after degradation. In addition, the percentage change in intensity between annealed and recoved states was also determined. Figure 51 shows a relatively homogeneous distribution of trap formation and annihilation with ~100% improvement on much of the

wafer, regardless of crystal orientation. To futher analyze the relationship to oxygen, two additional cast mc-Si wafers with known oxygen concentrations (see Fig. 47) were also measured. Figure 52 shows the LID present in a wafer from around ~37% ingot depth, where there was a small but measurable amount of O_i. Only a small fraction of the wafer in the upper left corner shows any change in I_{bb} after light exposure and consequently no LID or lifetime recovery after a >200°C anneal. This suggests that LID behavior is non-uniform over the mc-Si wafer. If boron doping is assumed to be uniform and the defect formation is directly linked to O_i concentration, then the oxygen incorporation within the cast multi-crystalline ingot also varies laterally as well as vertically. Figure 53 shows another HEM cast mc-Si wafer that demonstrates essentially no change in I_{bb} after light exposure and consequently no LID or lifetime recovery after thermal anneal, despite a higher O_i content (~69% ingot depth in Fig. 47). Therefore, cast mc-Si wafers show no light induced degradation across an entire wafer known to have the highest O_i content (Fig. 53), only partial degradation across a different wafer with a slightly lower O_i (Fig. 52), or relatively uniform degradation across a third wafer (Fig. 51), which had the highest measured bulk lifetime using the QSSPCD technique. The samples with known O_i had effective lifetimes on the order of 5 to 10 μs after phosphorus gettering. The low lifetime could have obscurred the LID in these samples. Oxygen is known to decrease the bulk lifetime in these cast mc-Si materials [5]. Thus, only some solar cells manufactured on these types of crystals should suffer efficiency degradation, depending upon the ingot position or O_i concentration and final bulk lifetime.

Degraded

Annealed

% Difference
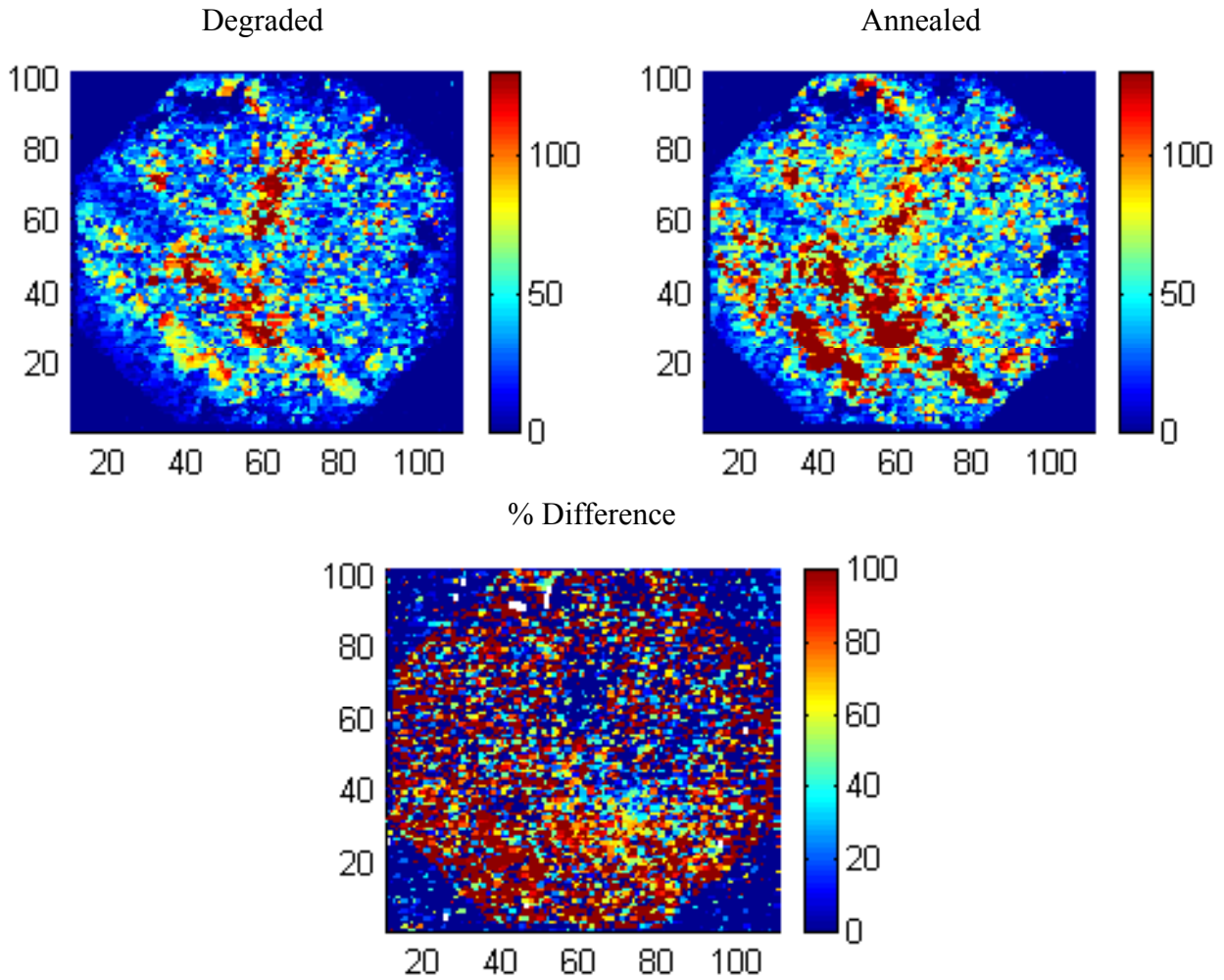
Figure 51. HEM cast mc-Si wafer passivated with SiN and measured using a photoluminescence mapping technique analogous to effective lifetime mapping. The change in the annealed and degraded state is mapped in the bottom figure labeled %Difference. This cast mc-Si has the highest measured effective lifetime before and after LID (18-25 μs) using the QSSPCD technique. A relatively uniform trap recovery is observed with up to a 100% improvement in effective lifetime. The colorbar has arbitrary units of intensity for I_{bb}.
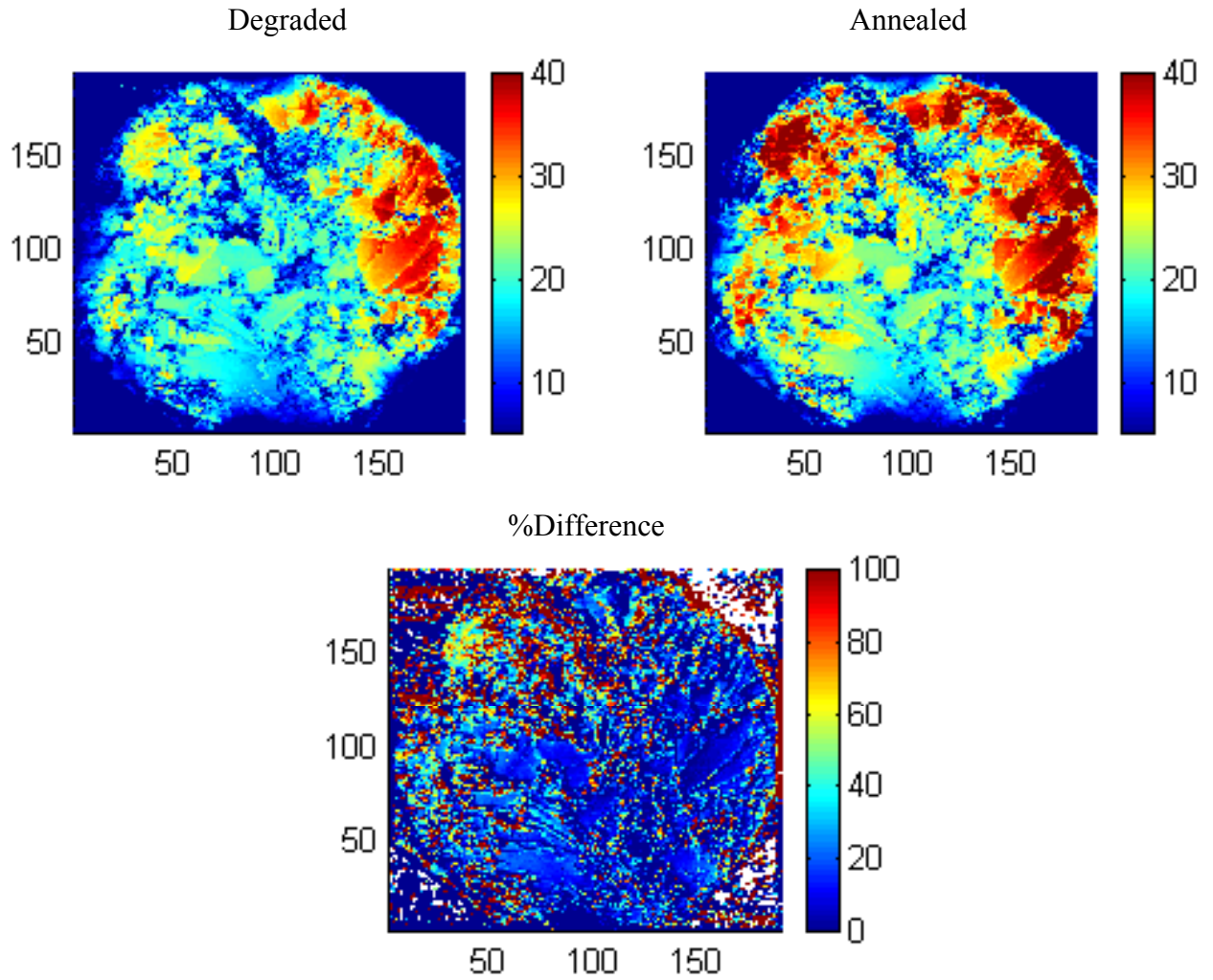
Figure 52. HEM cast mc-Si passivated with SiN and measured using a photoluminescence mapping technique analogous to effective lifetime mapping. The change in the annealed and degraded state is mapped in the bottom figure labeled %Difference. This sample has a relatively low oxygen concentration because it was taken from an ingot depth of ~37% from the top. Only the upper left corner shows LID. QSSPCD effective lifetime measurements revealed a low initial (or as-grown) bulk lifetime (< 8μs). The low lifetime could obscure LID. The colorbar has arbitrary units of intensity for I_{bb}.
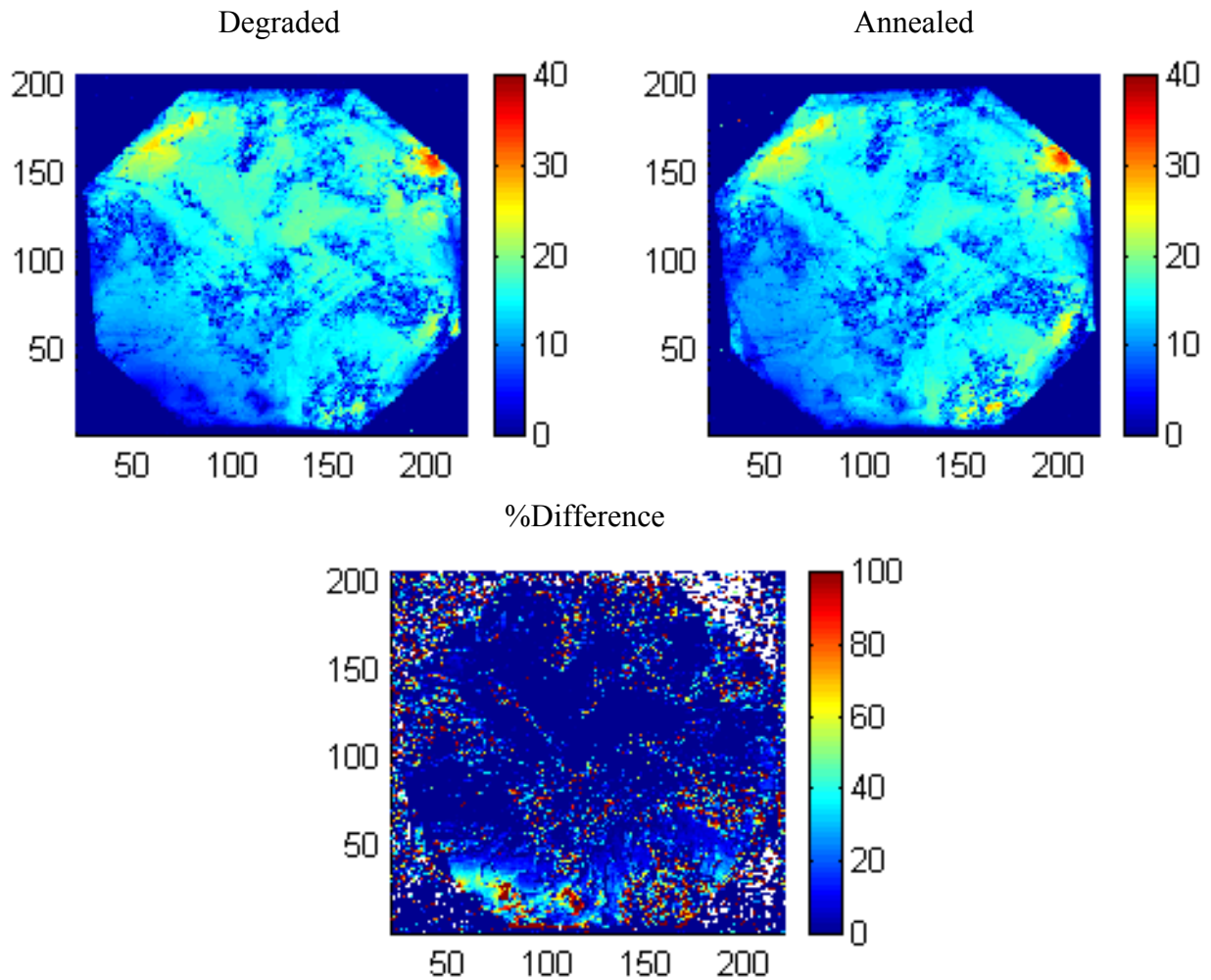
Figure 53. PL (effective lifetime) mapping of HEM cast mc-Si with relatively high O_i content (taken from ~69% ingot depth from the top). The change in the annealed and degraded state is mapped in the bottom figure labeled %Difference. Essentially no lifetime is recovered or degraded, suggesting no LID. However, QSSPCD effective lifetime measurements reveal low initial (or as-grown) bulk lifetime values that could obscure the LID cycle.

6.4 Spatial Distribution of Light Induced Degradation in String Ribbon and Edge-Defined Film-Fed Growth Ribbon Silicon

Figure 54 shows the SR sample response to the degradation/recovery cycle using the PL mapping technique. Recovery was observed after annealing the light-soaked samples. The very high lifetime region on the left side of the wafer seemed to improve in the band-to-band PL intensity. The averaged measured effective lifetime by QSSPCD technique for this material was ~30 μs before degradation and ~22 μs after degradation. Only a select few of these SR samples demonstrated LID at the time of this thesis. An additional difficulty in measuring the lifetime degradation in SR silicon via PL mapping, was that the bulk lifetime for these materials benefit greatly from hydrogenation during cell processing. To remeasure, the destruction of the solar cell is required. All metal and diffusions need to be etched away to expose the bare silicon surface, which then required SiN passivation before lifetime measurements were made. Retaining the excellent hydrogenation seemed more challenging on the SR samples than on the EFG ribbon silicon samples. Figure 55 shows the PL mapping for an EFG ribbon sample that had all metal and diffusions etched away after solar cell processing. After SiN passivation, PL mapping was used to characterize the degradation recovery cycle. As seen in Figure 55, the recovery after annealing the light-soaked EFG sample was observed in the band-to-band PL map. Areas of high PL intensity seemed to recover the most dramatically. To quantify this behavior, a line scan through the lifetime area map of the EFG wafer before and after degradation of the I_{bb}, as well as the corresponding defect band I_{db} location, was used in Figure 56. The difference in I_{bb} between the degraded line scan and the annealed line scan in the top figure directly corresponds to the extent of LID. Note that the LID

degradation/recovery cycle is observed only in the band-to-band PL spectra and shows significant spatial non-uniformity. LID is not pronounced in the low intensity (low lifetime) or defective regions, while strong LID is observed in the high lifetime or high PL intensity regions. The sharp drop in the PL intensity at defect locations causes the LID data to be obscured. The defect-band intensity peaks where the band-to-band intensity dips, suggesting that defective regions display a radiative characteristic via ~0.8 eV energy level. The I_{db} line scan shows no change in intensity before and after LID, suggesting that the LID trap is not a radiative trap with energy ~0.8 eV from band edges, further supporting a near mid-gap trap location for LID. The mean values of the N_{LID}^{*}, determined by equation (47), across the whole Cz-Si and EFG wafers were 0.019 and 0.0061, respectively, indicating the LID effect was about three times greater in Cz than in EFG. In addition, I_{bb} did not change appreciably in the defective regions, which helps to explain the lack of efficiency degradation observed in lower efficiency (or low lifetime) ribbon solar cells that are dominated by defective regions.
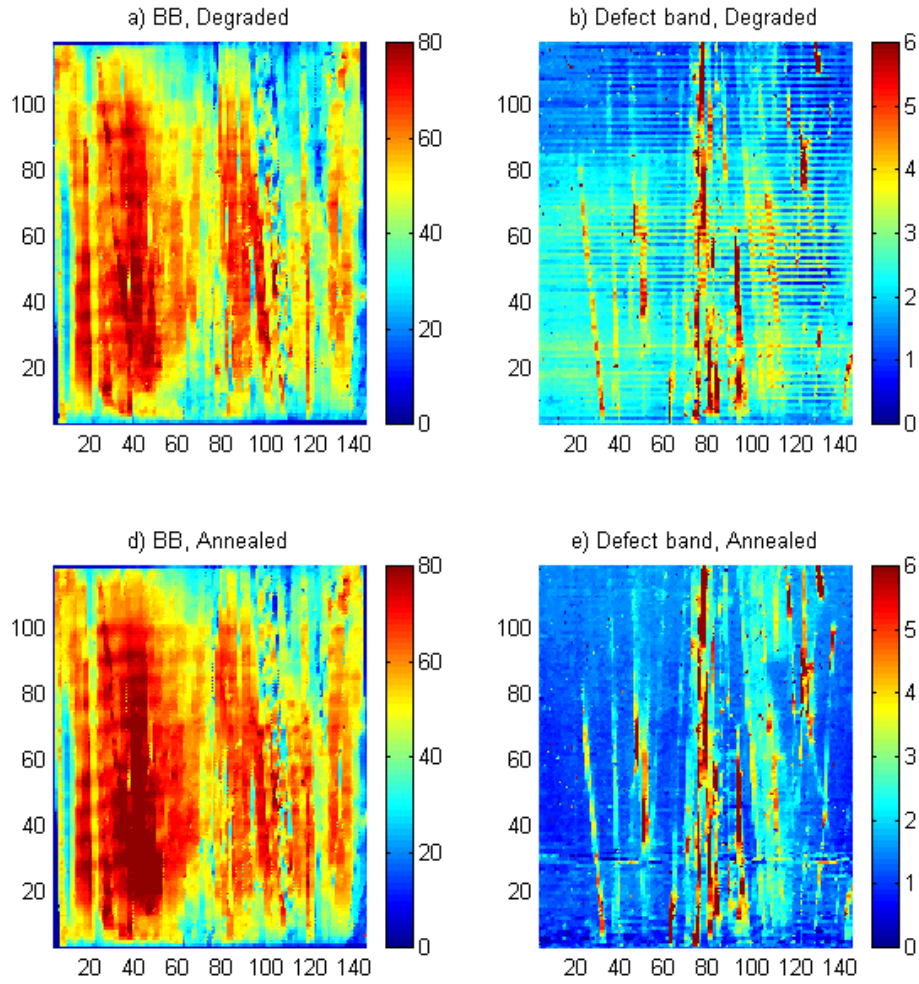
Figure 54. String Ribbon (SR) photoluminescence map using the band-to-band radiative recombination intensity before and after treatment for light induced degradation (LID) for the two pictures on the right. The two pictures on the left are the defect band intensity before and after LID. The colorbar has arbitrary units of photoluminescent intensity for either the defect band or the band-to-band recombination.
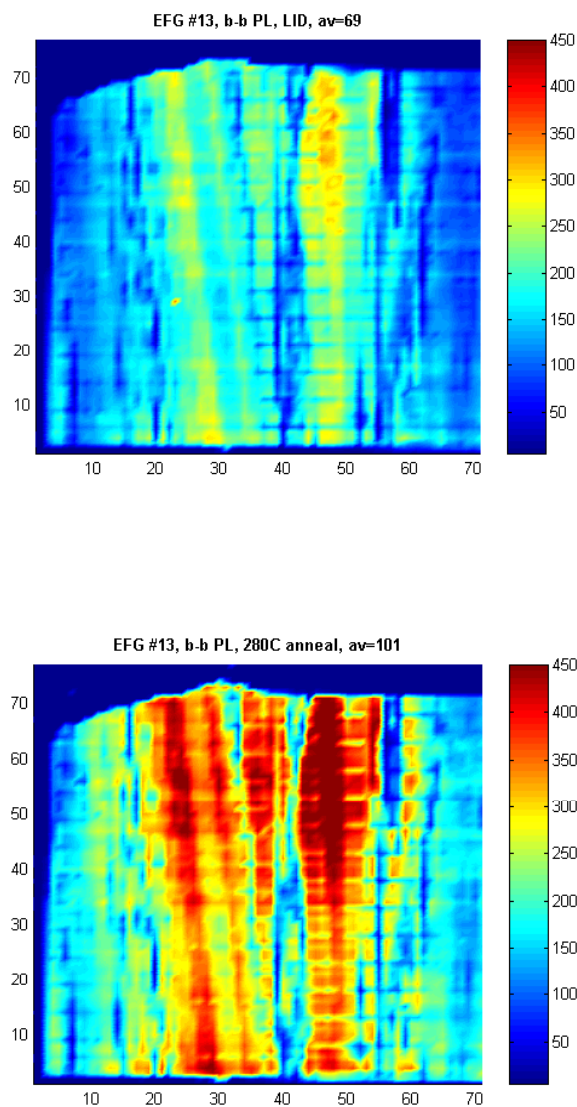
Figure 55. Edge Defined Film-fed Growth (EFG) ribbon photoluminescence map using the band-to-band radiative recombination intensity before and after treatment for light induced degradation.
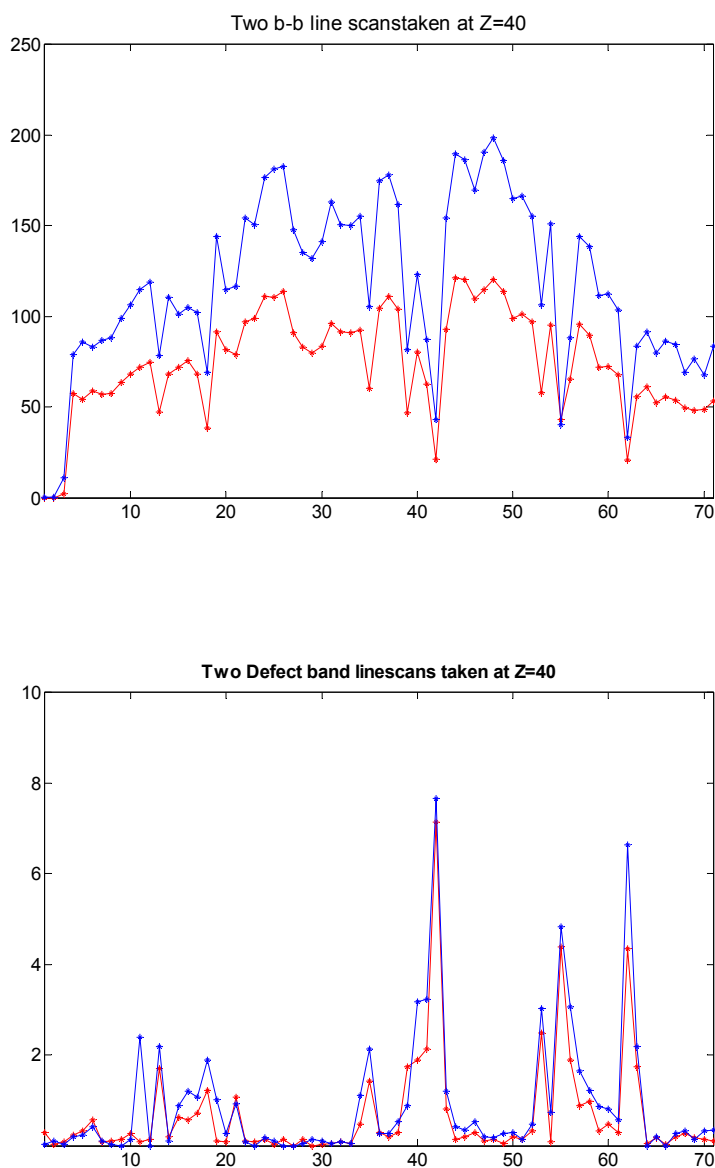
Figure 56. Line scans through the photoluminescence map for the EFG sample at the 40 mm height. Top graph is the band-to-band intensity comparison for the degraded and annealed state. Bottom graph is the defect band intensity (sub bandgap recombination event) for the annealed and degraded state. Blue is annealed and red is degraded. Y-axis is arbitrary units. X-axis is the width in mm.

6.5 Impact of Ambient Conditions on LID in Ribbon Silicon Solar Cells

Observation and interpretation of LID in ribbon silicon materials is not a straightforward or consistent phenomenon. Conflicting results have been published between the years 2002 and 2004, some of which are addressed in this section. Much of this confusion could result from the ambient conditions during degradation, especially the temperature. The initial claim of LID in ribbon silicon was published from this work in May 2003. A small 0.2% absolute drop in efficiency for screen-printed devices (~15-15.5%) on ribbon and cast mc-Si was shown. In addition, a much stronger degradation in higher efficiency devices (~16-17%) was shown to be up to ~1% absolute efficiency decrease. In August 2003, Hahn et al. reported no efficiency degradation in a 17.8% efficient SR sample and suggested process induced instabilities as the cause for the May 2003 reports on LID in ribbon materials. This type of confusion is typical of the metastable defect that causes LID. Over the past decade many different trap characteristics have been reported. The atomic structure of the defect is still not completely understood. Many different defect structures (Fe-B, B_iO_i, B_sO_{2i}, etc...) have been proposed over the years. The energy level of the trap has evolved from a shallow donor-level trap (at E_c-0.27 eV) to a mid-gap trap located at 0.35 eV above the E_v and 0.45 eV below the E_c with recent census of ~0.4 eV above the E_v established by the IDLS and TDLS analysis. The involved constituents are known to be boron and oxygen, but Fe-B pairs, among many others, were also suggested to show a similar behavior or response. Therefore, it is not surprising that initial

observations of LID in ribbon materials were conflicting at times. Further investigations were performed in this research to clarify some of the conflicting results.

In this study degradation conditions were found to be the source of conflicting information. Samples tested under AM1.5 global conditions at 25^oC were found to demonstrate a stable efficiency profile regardless of where the solar cell was fabricated. Figure 57 shows the V_{oc} temperature dependence of a traditional B doped Cz sample versus time. The rate of degradation increases with temperature, but the starting and ending points remain constant. The decay curves appear to be multi-exponential, consistent with results in the literature. Therefore, the analysis used by Hashigami (described in Chapter 4) was used for further characterization. Hashigami found a multi-exponential behavior for the degradation curve, requiring three distinct fit regions. The data in Figure 57 also shows similar behavior, where one exponential was not sufficient to properly match the open circuit voltage decay curve. Hashigami used V_{oc} measurements only to record the degradation with a special setup for monitoring LID. The measurements made in this thesis used a complete solar cell test setup that measured efficiency including V_{oc} and J_{sc}. Overall characteristics were similar in that the initial V_{oc} degradation was very fast, followed by the slower middle region and finally the slowest end region where saturation occurred. Similar analysis was used for a high efficiency SR silicon solar cell (~17%). Temperatures were varied from 25^oC to 125^oC and solar cell parameters were measured as a function of time. Figure 58 shows the V_{oc} decay behavior. For the 25^oC temperature, there was essentially no observable degradation for more than 24 hours. Cz samples, on the other hand, showed significant degradation in a
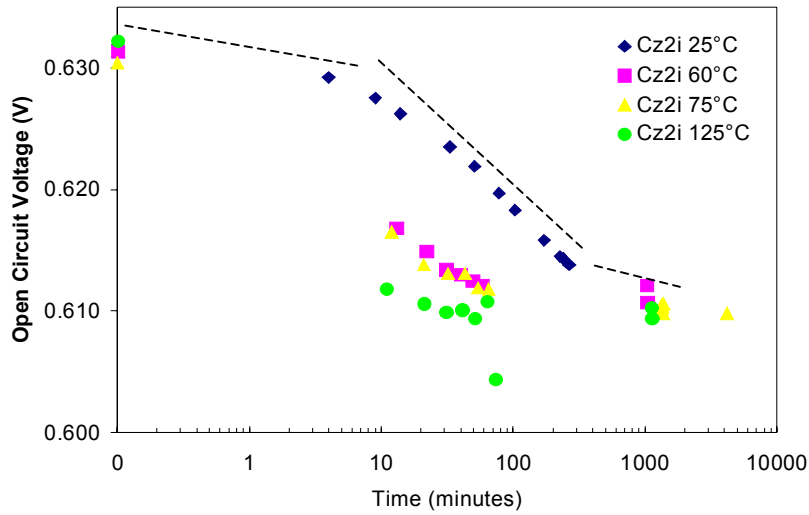
Figure 57. Open circuit voltage degradation for increasing temperatures from 25°C to 125°C. The degradation rate increases with temperature. The initial fast degradation, the slower middle region, and slowest end regions are denoted by the dashed lines for the 25°C curve.

relatively short period of time at 25°C. Thus, the observation made by Hahn et al. was completely accurate but also incomplete, because the operating conditions for solar cell modules in the field can reach temperatures in excess of 80°C, as measured from the 340 kW PV system on top of the Aquatic Center at the Georgia Institute of Technology. The SR solar cell in Figure 58 also demonstrates a multi-exponential behavior but does not achieve acceptable fits using just three exponential curves. However, the general behavior of the degradation was similar and exponential in nature. Special care during these measurements was taken to ensure that the degradation being characterized was directly attributed to the metastable defect known to cause LID. Fe-B pairs also exhibit a cyclical behavior between a high lifetime and low lifetime state. However, the stimulus required for recovery and degradation differ in very distinctive ways. Fe-B pairs recover

at room temperature (~25°C) overnight in the dark (~12 hours), but LID does not. Once

the samples in Figures 57 and 58 were degraded, they were left overnight in the dark to

ensure that no efficiency recovery occurred.
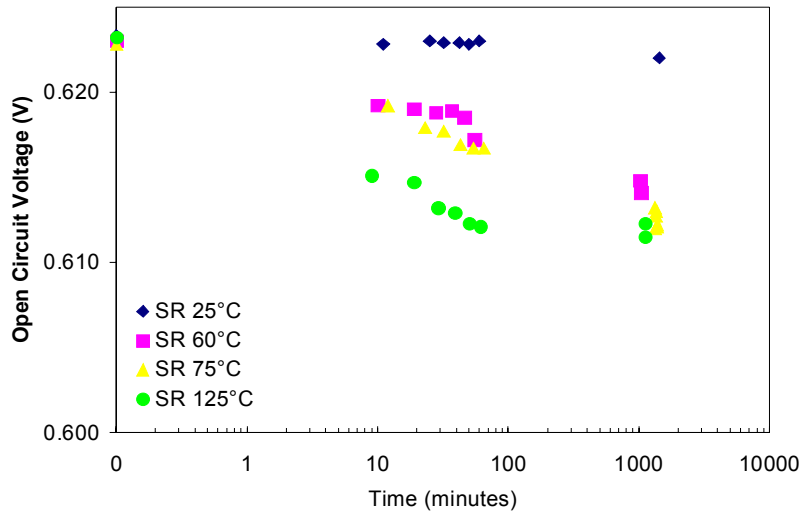
Figure 58. Open circuit voltage degradation for increasing temperatures
from 25°C to 125°C. The degradation rate increases with temperature.

It is important to note that there were only a select few ribbon samples with efficiencies

over 16% at the time of this thesis. Therefore, it is not appropriate to attribute the initial

observations made in this work to all ribbon Si solar cells. Ribbon Si materials are

unique to one another and have the potential to exhibit very different characteristics from

wafer to wafer, not to mention the temperature dependence of the LID in these materials.

For the samples in this work, 25°C showed stable operation. However, the 25°C

temperature is not the normal stable operating temperature for solar cells in the field.

Further proof of this can be seen in Figure 59, which shows a scatter plot of the magnitude of degradation observed for 50 different EFG ribbon samples measured at various times under various degradation conditions. As cell efficiency increases, the degradation becomes more prominent, but it is not uniform by any means. Samples with greater than 16% initial efficiency show as much as ~1% absolute efficiency degradation and as little as 0.1% degradation, depending on temperature or test conditions. Therefore, much more statistical work needs to be performed before proper characteristics can be determined. This work simply serves as an outline for observation conditions and initial data points. As the efficiency of these materials increases, more attention to the presence of LID may be critical to appropriate solar cell design to mitigate or eliminate the effects of LID in finished solar modules, including the effective use of texturing to allow for solar cells to be less sensitive to bulk lifetime constraints.

Boron doped MCz samples were also checked for LID at elevated temperatures. No substantial increase in degradation was observed for MCz samples with low O_i concentration.
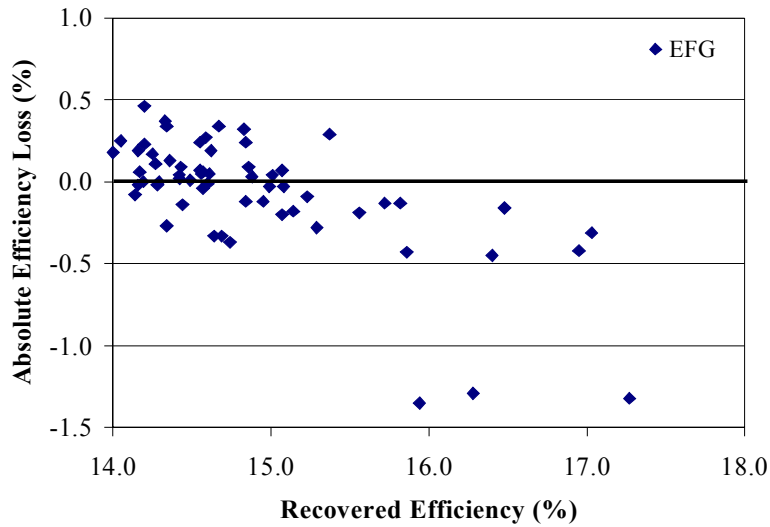
Figure 59. Scatter plot of the absolute efficiency degradation for samples with initial efficiencies recorded on the x-axis.

6.6 Conclusions

Significant LID was detected in B doped Cz Si (~300 μm), resulting in a 1 to 1.5% degradation in absolute efficiency. Ribbon Si materials were also found to exhibit LID but to a much lesser extent. The LID effect was smaller in SP mc-Si materials because of slightly higher resistivities for ribbon crystals, lower oxygen concentrations, and higher concentrations of defective regions. Cast mc-Si was shown to degrade 0.2-0.3% in some cases but not in the others (0.04%), depending on the position of the wafer in the ingot. This is partly due to the variation in oxygen content in the ingot. The top of the cast ingot showed undetectable interstitial oxygen, but the bottom section had $\sim 4 \times 10^{17}$ cm^{-3} O$_i$. Photoluminescence maps were taken to provide a spatially resolved picture of the LID

behavior in promising low-cost materials. Appreciable LID was observed away from defective regions in EFG Si. Some degree of LID in the most promising solar grade silicon materials was detected in this research. Thus, an increased importance on solar cell design is mandated to avoid or reduce the harmful effects of LID on solar cell efficiency.

The clarification of degradation in ribbon silicon samples was also discussed. The impact of ambient conditions on the degradation of ribbon silicon samples was shown to be a dominant factor for the observation of LID. Stable efficiency performance was observed over a 24-hour period at $25^{o}C$, but at an elevated temperature of $\sim75^{o}C$ significant efficiency degradation was observed. Thus, a more comprehensive description of LID in mc-Si materials needs to include some temperature profiling to decrease the observation time required to quantify efficiency degradation.

CHAPTER 7

7 UNDERSTANDING AND DEVELOPMENT OF POROUS SILICON ANTI-REFLECTION COATINGS BY STAIN ETCHING

7.1 Development of Low-Cost Porous Silicon ARC by Stain Etching

The second part of this research deals with the development of rapid low-cost anti-reflection coating (ARC) and texturing of Si by formation of a porous Si layer. The use of thin silicon (100 to 150 μm as opposed to 300 μm) can significantly reduce the LID and cost of Si PV modules. However, thin silicon cells require light trapping to absorb more photons for high performance. It is difficult to texture mc-Si uniformly by conventional etching techniques because of random grain orientation. As described in Chapter 3, several methods are being investigated to texture mc-Si. Porous silicon offers a potential for a low-cost, rapid, and uniform texturing technique that can also serve as a very good ARC. Therefore, in the second half of this thesis, the formation and implementation of porous silicon ARC is investigated for solar cell applications.

A chemically etched porous silicon layer on top of various PV grade silicon substrates was investigated in this work because of its promise for low-cost industrially scalable process. Chemically etched porous silicon uses equipment that is readily available in all semiconductor-processing labs. A major concern in the use of stain-etched porous silicon is the reproducibility of the layer. To obtain a reproducible porous silicon layer by HF/HNO_3 etching, the role of each component of the solution must be understood.

Therefore, first a study was conducted in this research to assess the surface reflectance as a function of HF and HNO_3 concentration. Figure 60 shows the surface reflectance of several porous silicon layers for etching solutions with varying nitric acid concentrations. Reflectance was measured in the range of 300 to 1200 nm using an "integrating sphere." Figure 61 shows the reflectance data as a function of HF concentration in the HF/HNO_3 mixture. Some important observations can be made from Figures 60 and 61. Elevated nitric acid concentrations increase (See Fig. 60) the reflectance of the porous silicon layer formed by a solution that has 5 parts water and 1 part HF. Additionally, the reaction becomes more violent and the porosity increases, eventually resulting in a polishing-type etch. The reflectance minimum tends to shift toward shorter wavelengths with the increasing nitric acid concentration. For the 5:3:1 mixture of $H_2O/HNO_3/HF$, the reflectance value was minimum at 550 nm and its value was ~10%. Figure 61 shows that the integrated reflectance decreases with the increase in HF concentration. In addition, the reaction is observed to occur faster and more uniformly with increasing HF concentration. The reflectance minimum is blue shifted with increasing HF concentration because of the change in porosity, but its value still remains high (~10%). Figures 60 and 61 also show that these reflectances were inferior to the reflectance of the widely used SiN_x single layer ARC in industry. For comparison we also deposited SiN_x ARC in a Plasma Therm PECVD with a ~2.0 refractive index and a thickness of 780 nm. Extrapolating the trends demonstrated in Figures 60 and 61, a new solution concentration was implemented. The HF acid was observed to cause a more uniform porous silicon layer in a much faster time period. Nitric acid seemed to affect the porosity of the porous silicon film. Thus, a hydrofluoric acid-based solution was used to achieve a rapid and

uniformly coated porous silicon coating. Only 0.5% of the porous silicon solution (1 part

nitric 200 parts hydrofluoric) was HNO_3 in order to better control porosity while still

achieving a uniform and rapidly etched layer. This resulted in a solution that produced a

reflectance curve very similar to the single layer SiN_x ARC, as seen in Figure 61 by the

curve labeled "2 dips ~1% HNO_3". To keep the porous silicon etched surface a uniform

color, the time of etching was limited to ~3 seconds per submersion (or "dip") into the

etching solution. Throughout this chapter and the next chapter, the etching time for a

given sample is referred to as either "number" *dips* or "number"*X*. A label of *2 dips* and

2X time in porous silicon are interchangeable. Therefore, in the following sections the

porous silicon formation solution was modified and a combination of etching and cell

processing was developed to achieve good anti-reflection coatings for solar cell

applications.

Using the information in the literature and the experience gained from the above

experiments, the new solution was developed to lower the Si surface reflectance. Starting

with pure HF from the bottle (1600 ml of 49% HF) and adding 6 to 8 ml of HNO_3 gave a

very reproducible, uniform, and rapidly formed (<5 sec.) porous layer with a low

reflectance minimum approaching 0%. Figure 62 shows that the reflectance minimum at

~450 nm (for 1 dip) can be shifted between 450 to 850 nm simply by altering the etching
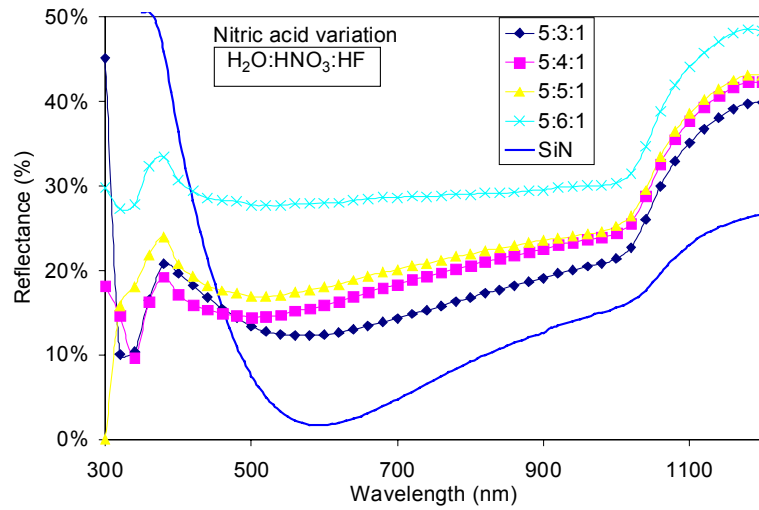
Figure 60. Total reflectance for porous silicon layers etched in a solution with varying concentrations of nitric acid.
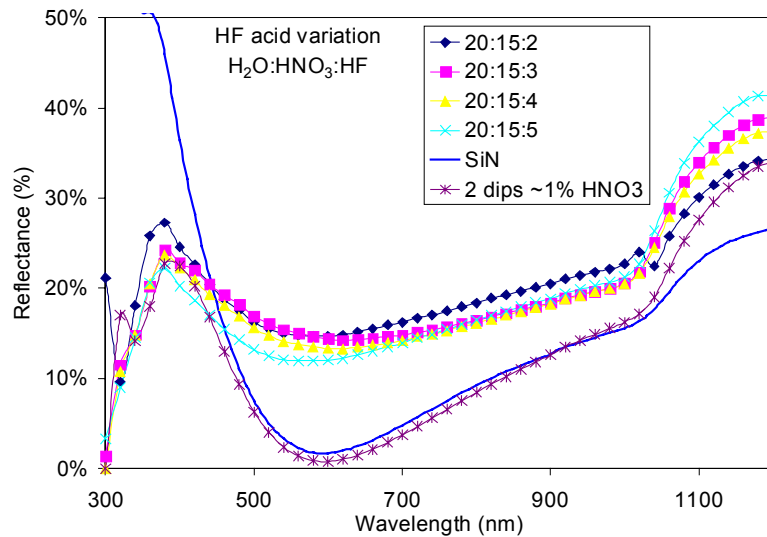
Figure 61. Total reflectance for porous silicon layers etched in a solution with varying concentrations of hydroflouric acid.
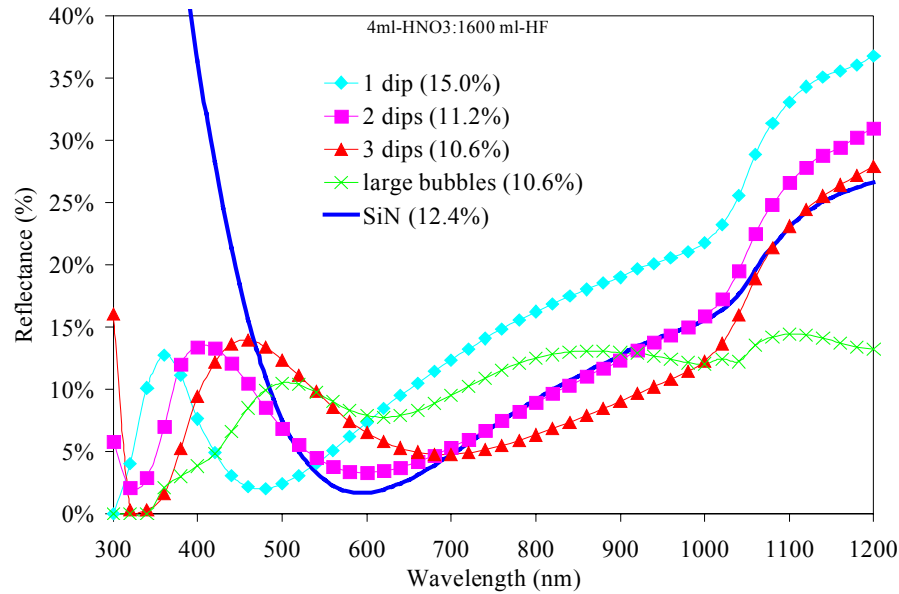
Figure 62. Evolution of porous silicon layer reflectance for increased soak time in etching solution.

time. The reflectance minima shifted toward longer wavelengths with increasing time. This was consistent with the literature, where porous silicon was known to behave similar to a SiO_2 layer with increasing thickness.   Thus, the quarter wave-reflecting layer becomes thicker, resulting in a corresponding increase of the wavelength for destructive interference ($2nd = \lambda/4$).   Figure 62 also shows that the reflectance of the porous silicon ARC can be tailored to closely match the reflectance of the widely used SiN_x single layer anti-reflection coating. Results in Figures 60, 61, and 62 demonstrate a promising level of control for tailoring the reflectance of the initial porous silicon layers before any heat treatment is encountered during solar cell processing, which may alter the characteristics of the ARC. Since the objective of this work is to optimize porous silicon ARC for finished solar cells, the impact of cell processing on AR coating quality was investigated using a cell process involving the Dopant Oxide Solid Source (DOSS) diffusion process

developed at Georgia Tech by T. Krygowski [50]. The DOSS process is illustrated in Figure 63. Spin-on dopants (either P or B) are spun onto dummy wafers that are subsequently stacked next to a solar cell wafer during a single high temperature diffusion step. The spin-on glass delivers a fixed amount of dopant to the solar cell surface that is diffused during the one high temperature step. The uniqueness of the process is that it can give uniform diffusion over the porous silicon layer when it is formed prior to cell processing. The benefits and detriments of forming the porous silicon layer prior to cell processing rather than at the end, as well as its development in conjunction with the DOSS process, are described in the following sections.

P   C   B   C   P   C   B
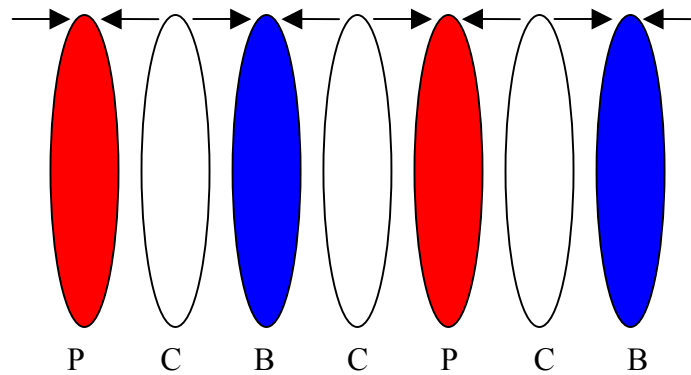
Figure 63. DOSS diffusion source diagram. Boron sources (B), phosphorus sources (P), and solar cells. (C)

7.2 Novel Processing of Silicon Solar Cells with Porous Silicon Etching and DOSS Diffusion

Several groups are working on the application of porous silicon layers to silicon solar cells, as outlined in Chapter 3 of this Thesis (See Fig. 14). The objective of most previous studies was to form an ARC and selective emitter simultaneously by forming PS on finished cells (See Fig. 12). Since the metallization grid on the front acts as an etch mask, a selective emitter is formed because PS etching thins the emitter region between the grid lines. However, this method has several drawbacks. The screen-printed metallization is attacked by the porous silicon etching, leading to inhomogeneities and, more important, a degradation in fill factor (FF). In addition, the etch solution is contaminated with metal, which limits its usability and re-usability and demands expensive waste management. Moreover, another wet-chemical step does not fit well into an industrial fabrication sequence and holds the risk of increased handling of chemicals. Therefore, our efforts in this research focus on the formation of PS as part of the normal wafer cleaning sequence used at the beginning of the solar cell run. This approach does not degrade contact metallization and FF but has to contend with potential change in porosity or ARC properties during the high temperature processing of cells. Also, the contact resistance to porous silicon layers is known to be high and the ability to form an appropriate pn junction through the etched silicon layer poses potential difficulties and challenges.

7.2.1 Formation of Porous Silicon and the Change of the Optical Properties Before and After Cell Processing

Figure 64 shows the measured reflectance of various crystalline silicon wafer types etched in the same 70wt% HNO_3 and 50wt% HF solution for <5 seconds and subsequently processed into solar cells. The stability of the porous silicon texture against subsequent processing, including high temperature and other chemical etching steps, was one of the more challenging technological problems of this approach. The PS layer was formed in our cell process sequence during the final step of the initial cleaning process.
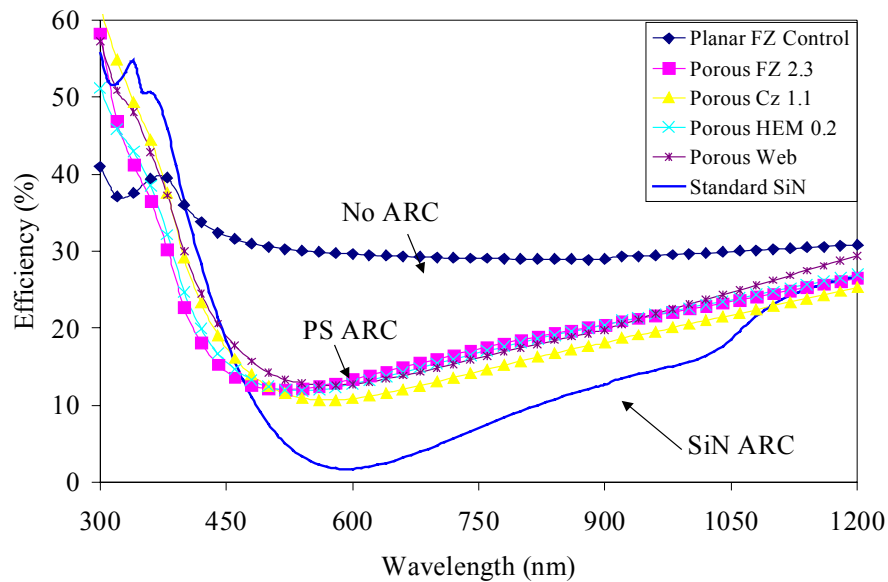
Figure 64. Porous silicon solar cell reflectance for FZ, Cz, and mc-Si (web and HEM) samples after cell processing.

The wafers were subsequently dried and loaded into the furnace for DOSS diffusion.

Figure 64 shows that the PS ARC was superior to bare Si but inferior to SiN ARC after the complete cell process. However, Figure 65 shows that prior to any heat treatments, reflectance was quite good (<10% for the front integrated surface reflectance) for both single and mc-Si. The diffuse reflectance (Fig. 65) of porous silicon etched wafers (HNO_3:HF solution) prior to cell processing showed a minimum at about 600 nm with an average weighted front surface reflectance of ~9% compared to ~35% for the uncoated sample. This was quite comparable to the widely used SiN ARC. The weighted
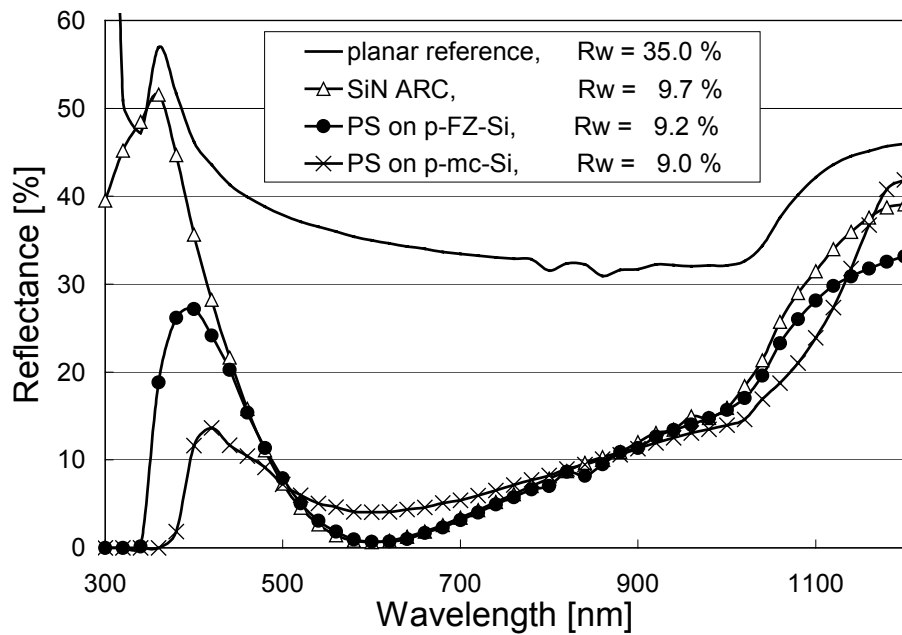
Figure 65. Reflectance of planar silicon, silicon with SiN ARC, and with porous silicon texturing, respectively.

reflectance (R_w) is the integral reflectance between 400 and 1100 nm weighted with the AM 1.5 global spectrum.

$$R_W = \frac{\int R_\lambda N_\lambda d\lambda}{\int N_\lambda d\lambda} \qquad (48)$$

where R_λ is the reflection at a particular wavelength of light, N_λ is the number of photons at the particular wavelength, and λ is the wavelength of light.

It is interesting to note that above 500 nm, the reflectance characteristic of PS etching is similar to that of a SiN_x ARC. The extremely small feature size of the porous silicon, coupled with the small layer thickness compared to the useable light spectrum, supports the use of an effective medium approximation, often used to characterize the optical properties of porous silicon layers. This behavior supported the use of an effective medium refractive index for the porous silicon layer above 500 nm, where it acts like a virtual dielectric layer resembling SiN_x with n=2 and a 780 nm thick layer. An ellipsometer measurement with a 632.8 nm laser gave a thickness of ~110 nm and n = 1.69 for a processed PS layer. A freshly etched porous silicon layer cannot be measured by conventional ellipsometry because of the dispersion of light from the texturing. A spectroscopic ellipsometer is needed. Therefore, an integrating sphere was used to characterize the optical performance of the porous silicon layer. Experimental data in Figure 65 reveals that the weighted reflectance of this porous Si layer (9.2%) was initially ~0.5 % lower than that of a SiN_x ARC but suffered degradation during cell processing, resulting in an R_w value of ~17%.

7.2.2 Surface Recombination Properties of Porous Silicon Emitter

The good reflectance of stain-etched PS results from a rough surface that unfortunately could lead to high surface recombination velocities (SRV) if not properly passivated. However, the DOSS diffusion process developed at Georgia Tech and used in this research simultaneously forms a phosphorus emitter with an in-situ surface oxide for excellent surface passivation. In addition, the diffusion glass layer is so thin that it does not require chemical etching or removal. In addition, it delivers a fixed dose of dopant from a limited solid source, over the entire surface, which produces a uniform doping on a non-uniform or rough surface. This made the DOSS process a very attractive candidate for porous silicon etched cells fabricated in this thesis.

To determine the front surface recombination velocity (SRV) of the porous silicon etched solar cells formed by the DOSS diffusion process, the same P diffusion was performed on both sides of a high resistivity, high lifetime FZ wafer with and without porous silicon etching.   Emitter saturation current density (J_{oe}) was determined using PCD lifetime measurements, where effective lifetime is first measured as a function of injection level and then the J_{oe} value is extracted using the following equation:

$$\left(\frac{1}{\tau_{eff}} - cn_{av}^2\right) = \frac{1}{\tau_{bulk}} + \frac{2J_{oe}n_{av}}{qn_i^2W} \tag{49}$$

where τ_{eff} is the measured effective lifetime, c is the Auger recombination coefficient, τ_{bulk} is the bulk lifetime, n_{av} is the average carrier density obtained by conductance measurement, q is the electron charge, n_i is the intrinsic carrier concentration, and W is the wafer thickness.   Higher SRV or J_{oe} can lower cell performance. For the same diffusion, the planar sample with no PS etching gave an emitter saturation current density of 428 fA/cm^2 for a 32 Ω/sq. emitter.   The corresponding PS sample gave a J_{oe} of 169

fA/cm^2 with a ~100 Ω/sq. emitter. Thus, PS formation raised the sheet resistance value from 32 Ω/sq. to ~100 Ω/sq. and gave a lower J_{oe} value. The sheet resistances were measured using a four-point probe method. To extract the SRV from the measured J_{oe} values, measured doping profiles with and without a PS layer were imported into the PC1D solar cell modeling program to establish a relationship between J_{oe} and SRV. This was done by biasing the device in PC1D at a fixed voltage (~0.4 volts) in the dark and determining the current density on the p-type side, J_p, at the emitter junction edge for various SRV values. Then, the J_{oe} was obtained as a function of SRV by

$$J_p = J_{oe} e^{qV/kT} \qquad (50)$$

Calculated J_{oe} as a function of the SRV was plotted for both planar and porous silicon etched emitters (Fig. 66). Next, the measured J_{oe} value is used to obtain the actual SRV value for respective emitters (Fig. 66). Using this methodology gave a SRV of 17,000 cm/s for a ~100 Ω/sq. PS etched emitter with a J_{oe} of 169 fA/cm^2, and a SRV of 500,000 cm/s for a 32 Ω/sq. planar emitter with J_{oe} = 428 fA/cm^2 without PS etching. The measured J_{oe} on the porous silicon etched samples was consistently lower than the J_{oe} of the corresponding planar samples that received the same diffusion. This was partly due to the increased emitter sheet resistivity for the porous silicon etched samples for the same initial diffusion. Figure 66 also shows that a 32-35Ω/sq. emitter formed on a porous silicon etched surface gave a FSRV of ~100,000 cm/s as opposed to a FSRV of ~6,000,000 cm/s for the planar device with similar sheet resistivity (~32 Ω/sq.). Thus, the potential for obtaining a low SRV coupled with a low reflectance presents an opportunity to improve the efficiency of low-cost solar cells without using a traditional
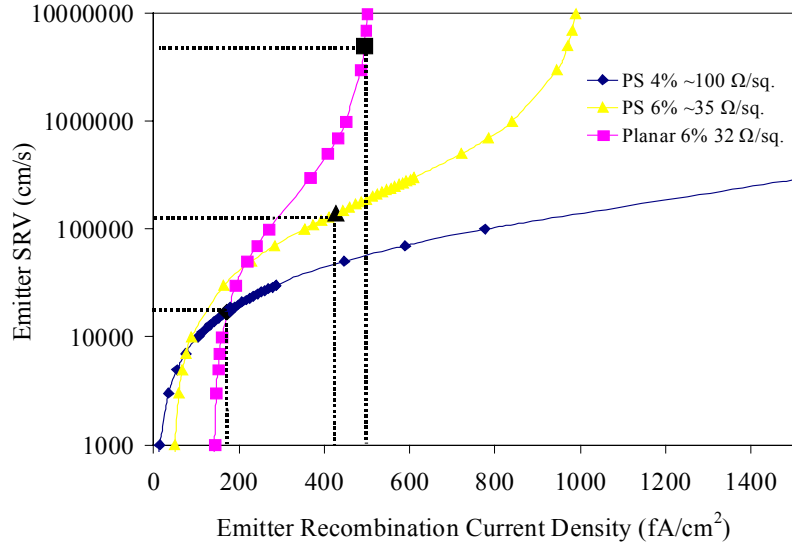
Figure 66. Calculated front surface recombination velocity (FSRV) versus J_{oe} for porous silicon and planar control wafers of various sheets.resistivity

ARC after solar cell processing. This is further investigated in the next section by the fabrication and analysis of complete solar cells.

Phosphorus sources used for DOSS diffusion can yield a sheet resistivity in the range of 6-600 Ω/sq. at 925°C [55] by selecting the proper concentration of P_2O_5 in the spin-on dopant for a fixed time frame (20-60 minutes). For a diffusion cycle that gave a ~40 Ω/sq. emitter on a planar surface, an emitter saturation current (J_{oe}) of 500 fA/cm^2 was obtained. A porous silicon textured sample diffused during the same furnace process gave a sheet resistance of ~100 Ω/sq. and a J_{oe} of 128 fA/cm^2, which could support open-circuit voltage (V_{oc}) values in excess of 670 mV using the following equation and assuming a nominal J_{sc} value of 35 mA/cm^2 for a screen-printed device.

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{J_{sc}}{J_{oe} + J_{ob}} + 1 \right) \qquad (51)$$

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These results demonstrate that the porous silicon layer acts somewhat like a diffusion barrier and *limits* the introduction of phosphorus dopant into the bulk silicon region because of a fixed dopant dose and high surface area (more detail is provided in a subsequent section). Thus, a much heavier concentration of P_2O_5 is required to obtain the desired sheet resistivity than would be necessary for a planar sample. The overall thickness of the PS layer dictates how heavily the sample should be diffused for a desired dopant concentration.

Thus, the above results indicate that a combination of PS ARC formed by stain etching and the DOSS diffusion process can give reasonable J_{oe}, SRV, and sheet resistance, leading to a high V_{oc} and cell efficiency.

7.2.3 Porous Silicon Etched DOSS Solar Cells

After establishing the appropriate conditions for porous silicon etched DOSS solar cells, the next step was to fabricate actual cells to demonstrate that high efficiencies can be achieved with this technology. In this section, porous silicon etched DOSS solar cells with a screen printed Al BSF were fabricated on 0.6 Ωcm FZ-Si (Shin Etsu), 0.7-1.3 Ωcm Cz-silicon from Bayer and 0.2 Ωcm mc-Si from Eurosolare. The actual DOSS diffusion time was 1 hour, followed by an in-situ oxidation step of 15 minutes. Thus, a single furnace step led to diffused, textured, in-situ oxide passivated, and AR-coated solar cells with a stain-etched PS layer. In addition, no phosphorus glass removal was necessary in this process because the glass thickness was less than 10 nm [50,55]. Thus, the DOSS

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diffusion method was found to be an excellent match for porous silicon etched solar cells and can offer a low-cost and rapid manufacturable process for high efficiency cells. Complete porous silicon etched cells are fabricated and analyzed in the following section.

The PS layer was formed prior to emitter diffusion and metal contact formation. The solar cells were fabricated using a DOSS diffusion process that gave 20 Ω/sq. emitter on a planar surface. This ensured a sufficiently heavy diffusion on the porous silicon etched samples. Table 9 shows cell results obtained for both photolithography and screen-printed front contacts for the conventional furnace tube DOSS diffused porous silicon etched samples. For the photolithography process, metal contact was made by removing the in-

Table 9. Best porous silicon solar cell results for photolithography (PL) and screen-printed porous silicon solar cells. *Confirmed at Sandia National Labs.

Material	Voc(mV)	Jsc(mA/cm^2)	FF	Eff(%)
*0.6 Ωcm FZ	629	29.32	0.807	14.9 (PL)
1.0 Ωcm Cz	618	27.61	0.785	13.4 (PL)
0.2 Ωcm mc	615	27.07	0.762	12.7 (PL)
0.6 Ωcm FZ	627	28.91	0.759	13.8 (SP)
1.0 Ωcm Cz	613	27.05	0.768	12.7 (SP)
0.2 Ωcm mc	602	26.70	0.741	11.9 (SP)

situ oxide and PS layer below the area to be covered by a metal grid. Screen-printed front contacts were simply printed directly onto the PS surface and fired, with the hope of punching through the porous silicon layer. This is similar to what is done for conventional SiN$_x$ coated samples. The initial results in Table 9 show the highest confirmed efficiency of 14.9 % for the porous silicon etched cell with the photolithography contacts. Good open circuit voltages (~620 mV) and fill factors in excess of 80 % were achieved for the photolithography cells. However, a somewhat

lower short circuit current (J_{sc} = 29.3 mA/cm^2) was obtained along with a higher weighted reflectance of 17 %, contributing to the appreciable loss of photocurrent. The post-processed reflectance was much higher than the 9% front surface weighted reflectance of the PS layer prior to fabrication.   Thus, high temperature processing degraded the reflectance of the porous silicon layer. On a positive note, further optimization of the starting sheet resistance and reflectance can result in much higher cell efficiency.   Light beam-induced current (LBIC) analysis of a porous silicon etched FZ cell in Figure 67 revealed that even though the reflectance is somewhat higher in these cells, the PS ARC
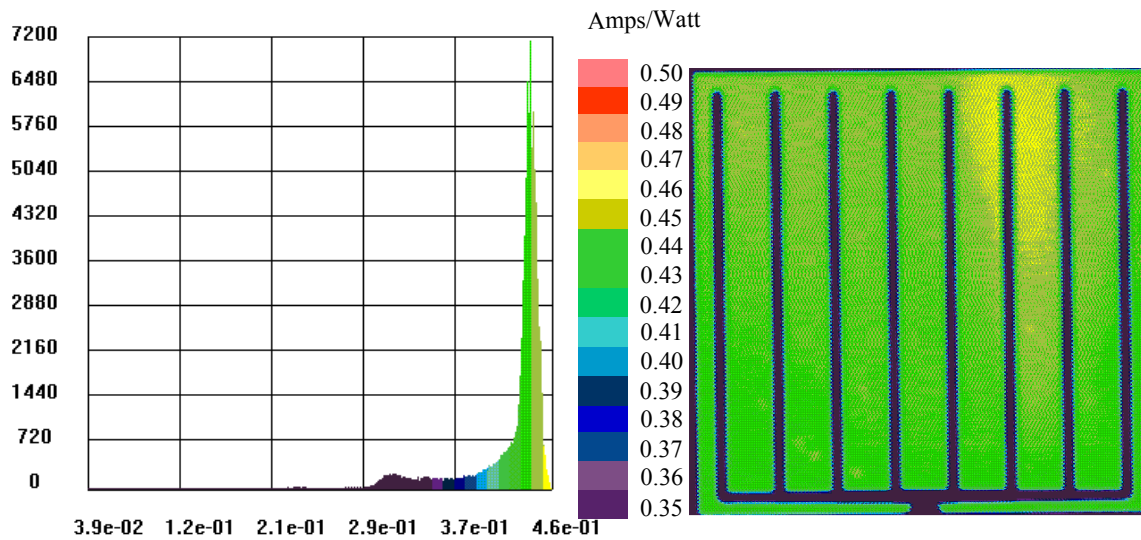
Figure 67. LBIC map of 0.6 Ωcm (4 cm^2 FZ) sample with a porous silicon ARC along with the histogram of data points.

is quite uniform.

The porous silicon ARC did not limit the V_{oc} because the measured J_{oe} of 300 mA/cm^2 for a 40 Ω/sq. indicates that a V_{oc} of 650 mV is possible. Thus, the V_{oc} of 630 mV in

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these cells is limited by the base or J_{ob}. The current densities in Table 9 were much lower than the conventional cells. The observed lower efficiency (below 15%, Table 9) was the result of the non-optimal PS ARC resulting from the cell processing induced increase in reflectance. Therefore, the next section addresses the issue of high temperature induced change in porous silicon anti-reflection coating properties.

7.3 Investigation and Optimization of Post-Processed Reflectance of Porous Silicon Etched Solar Cells

To establish that porous silicon etching can be implemented and optimized as the first processing step, reflectance characteristics were tailored so that post-processing reflectance stays low. In addition, the phosphorus diffusion temperature was selected so that it could diffuse through the porous layer to create an effective n^+-p collecting junction. First, generation porous silicon ARC samples followed process sequence "A", which is outlined in Figure 68. Reflectance was measured before and after solar cell processing. A typical change in the reflectance curve of the porous silicon layer after Process A is shown in Figure 69. In both samples shown in Figure 69, the integrated reflectance of porous silicon increased from ~12.5% to more than ~17%. Total integrated reflectance is the sum of the front surface

| **Process A** |
| Clean   15 minutes |

| Porous Silicon Etch
6 seconds |

| CF DOSS Emitter
150 minutes |

| SP Al BSF + Bake + Fire
8 minutes (Belt Furn.) |

| SP Ag + Bake + Fire
8 minutes (Belt Furn.) |

| Total Time
~3 hours |

	V_{oc}	J_{sc}	FF	Eff.
FZ	624	29.9	74.9	**14.0**
Cz	614	29.2	74.6	**13.4**
Mc	619	26.9	75.5	**12.5**
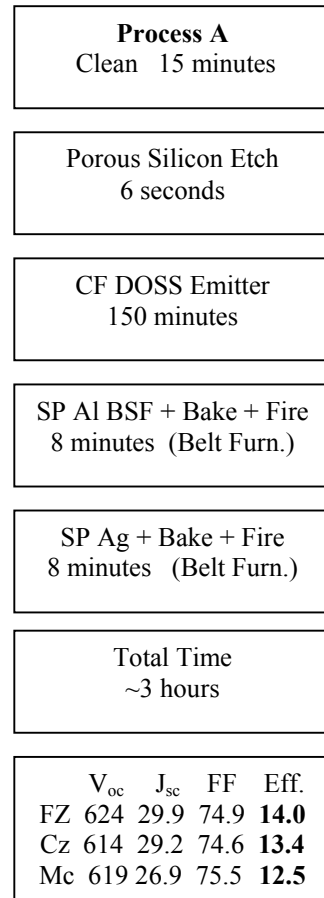
Figure 68. Process sequence diagram for porous silicon ARC solar cells using DOSS processing.

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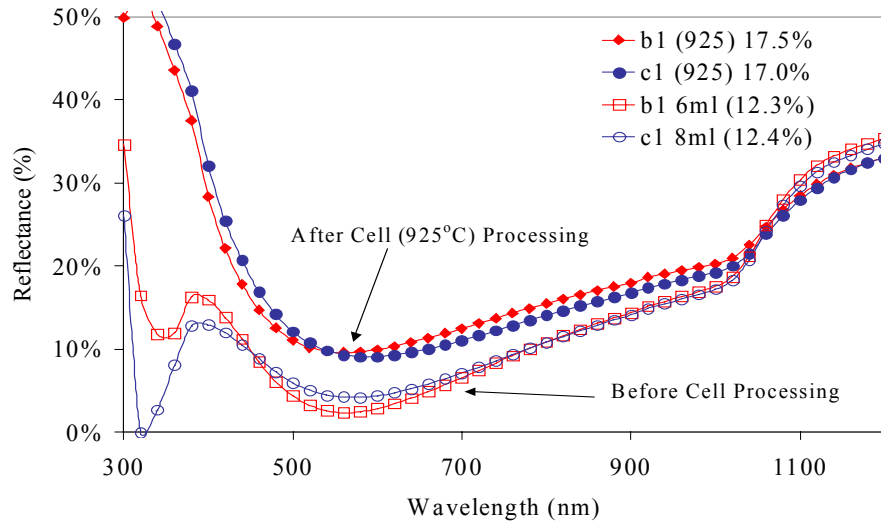
Figure 69. Change in porous silicon reflectance subjected to high temperature processing in a conventional tube furnace.

reflectance and the escape reflectance, which includes the light reflected from the rear surface. Recall that the standard SiN_x layer had a total weighted reflectance $R_w = 12.4\%$ (*front surface reflectance alone was 9.7%*). Even though this was still higher than the target value of ~10%, it was clearly a big improvement over a bare silicon surface with an integrated reflectance of ~35%, supporting the notion that porous silicon can withstand high temperature processing in a conventional furnace for ~1 hour at 925°C. Since complete and functional screen-printed cells were obtained with efficiency in the range of 12.5-14% with Process A, it demonstrates that the n^+p junction can be formed by diffusion through the porous silicon layer and contacts can be SP through the porous silicon layer. Optimizing junction formation, oxide passivation, and contact formation can further improve the performance of porous silicon DOSS solar cells. To accomplish this, further process development was undertaken in this section, followed by detailed characterization and analysis of porous silicon etched cells. The use of Rapid Thermal

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Processing (RTP) was investigated to minimize the change in process-induced reflectance of the porous silicon layer.

In this section, solar cells were fabricated using the DOSS technique to form an n^+ emitter in both a conventional furnace (CF) and in an RTP system. Porous silicon layers were formed on Si substrates prior to phosphorus emitter diffusion by chemical etching (stain etching) solutions comprised of HF acid, HNO_3 acid, and water (1:3:5). Porous silicon etching time was limited to <10 seconds. Screen-printed Al BSF was formed on the rear for surface passivation. A silver (Ag) grid was SP on top of the porous silicon and fired through it in a belt furnace (BF) or RTP to form the front contacts. Spreading resistance analysis (SRA) was performed to obtain diffusion profiles. Figure 70 shows a dopant profile for a planar sample and a sample with a porous silicon layer subjected to the same CF diffusion cycle. A spin-on coated wafer with a 6% P_2O_5 concentration was used as a DOSS diffusion source at ~925°C for ~1 hour. The porous silicon etched sample showed lower surface concentration and a shallower diffusion depth compared to the planar control (~0.5 μm and 0.95 μm, respectively). Thus, porous silicon again acted as a diffusion *limiter,* not a barrier. Diffusion profiles can be tailored by changing the temperature, spin-on dopant concentration, or time of diffusion.
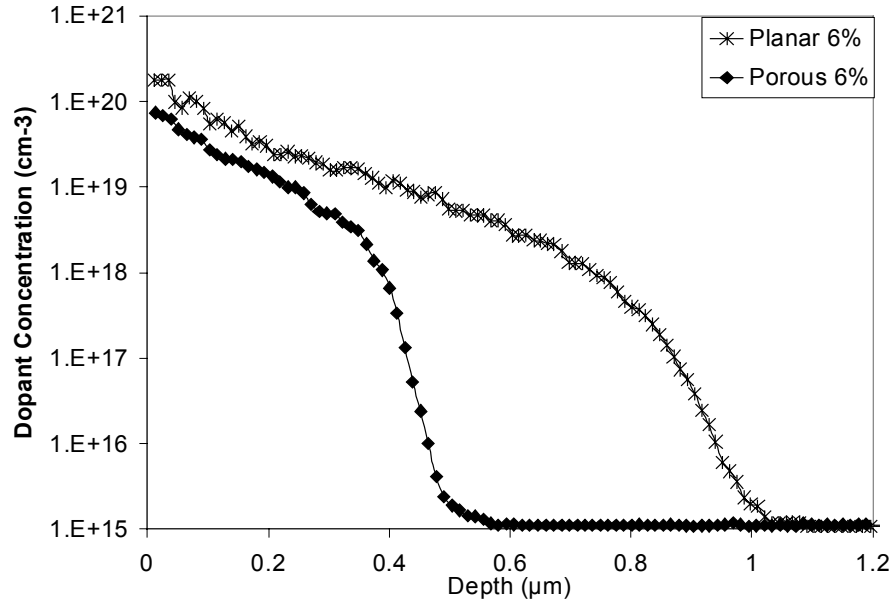
Figure 70. Phosphorus dopant concentration diffused at 925°C using 6% P_2O_5.

Figure 68 compares the internal quantum efficiency (IQE) and reflectance curves of a SP porous silicon solar cell subjected to a CF diffusion cycle with a standard screen-printed cell made in our lab. The standard 16.7% efficient cell consists of a ~40 Ω/sq. $POCl_3$ emitter with a full RTP fired Al BSF on a 1.3 Ωcm FZ wafer with a SiN_x single layer ARC. Figure 68 shows that the porous silicon cell, fabricated by Process A in Figure 65, has an inferior reflectance with a minima of ~10% at ~600 nm. The total weighted reflectance was 17.4% compared to 12.4% for the SiN_x coated standard cell. However, the blue response is better for the porous silicon sample. This is partly due to the higher sheet resistance and in-situ oxide passivation of the DOSS emitter. An important feature of the excellent blue response suggests that the absorption coefficient of the porous silicon layer after cell processing is not as significant a detriment as the freshly etched

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porous silicon layers used by groups implementing the porous silicon etch as the final process step. To realize the full benefit of the improved blue response, the front surface reflectance needs to be optimized. It is clear from Figure 71 that during high temperature processing, the porous silicon layer reflectance curve undergoes changes. The initial total weighted reflectance values were ~11.5% but increased to 17.4% after CF processing. Therefore, initial reflectance needs to be tailored to minimize the *final reflectance* profile. In addition, the long wavelength response of the porous silicon etched solar cell was inferior to the standard screen-printed cell. This was attributed to the inferior BSF formation step used for the porous silicon etched solar cell. A belt furnace firing process was used for the porous silicon etched sample instead of an RTP fired BSF used for the standard screen-printed solar cell. Thus, the decreased long wavelength response of the porous silicon etched sample resulted in the loss of photocurrent.

Process	V_{oc}	J_{sc}	FF	Eff.
Std. SP	626	33.9	0.786	16.7
Process A	624	29.9	0.749	14.0

Figure 71. IQE and reflectance curves for the standard screen-printed solar cell and a porous silicon ARC solar cell (Process A).

7.3.1 Implementation of Rapid Thermal Processing for Higher Efficiency

   Porous Silicon Textured Solar Cells

To reduce cell fabrication time (~1 hour diffusion cycle in a CF) and improve the porous silicon layer reflectance, the use of RTP was explored. RTP offers better control of the diffusion ambient and shorter cycle times that can potentially help minimize reflectance changes in the porous silicon layer. DOSS diffusion was performed in an RTP system at 880-900°C in only 3 minutes. Figure 72 shows the resulting reflectance curves for samples subjected to various RTP processes. Porous silicon layers prior to any processing had an average weighted reflectance of ~11%. However, the sample that
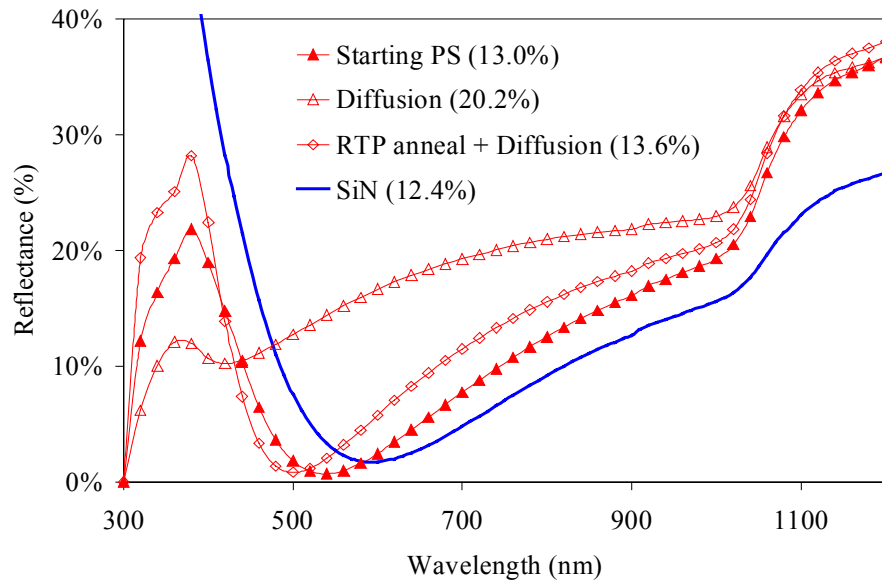
Figure 72. Reflectance curves for SiN$_x$ and porous silicon AR coatings subjected to different RTP processing.

received no RTP heat treatment prior to emitter diffusion showed a substantial jump in minimum reflectance value from ~0% to ~10%, similar to the aforementioned CF process. The total weighted reflectance after RTP increased to ~20%, with a minimum at 420 nm, which was higher than ~17% for the furnace diffused samples with a minimum at 580 nm. This suggests that it is not the diffusion time but rather the gas ambient at the elevated temperatures that controls the post processed reflectance. To support this finding, a separate sample was used to test the effect of the RTP heating cycle only on the porous silicon layer in a nitrogen ambient. The heating cycle alone did not significantly change the optical properties of the anti-reflection coating so the sample was subsequently DOSS diffused at $880^{o}C$ for 3 minutes to form the n^{+}-p collecting junction. Again, the surface reflectance was measured (empty diamond line in Fig. 72) and shows that the RTP anneal + RTP DOSS diffusion maintained a much lower weighted reflectance (13.6% compared to 20.2%). Thus, by implementing an RTP anneal prior to emitter formation, a much-improved anti-reflection coating performance can be maintained. In addition, the sheet resistivity measured using a four-point probe was much lower for RTP annealed samples. Planar samples and porous silicon etched samples had approximately the same sheet resistivity for an identical process sequence once the porous silicon etch sample received the RTP anneal prior to diffusion. Using these findings led to the development of a new solar cell process sequence (Process B in Fig. 73) for porous silicon etched solar cells fabricated by the DOSS diffusion process. The CF and RTP solar cell fabrication sequences developed and used in this study are shown in Figure 73. CF Process A gave a SP cell efficiency of 14% on FZ Si (Fig. 68) with the corresponding IQE shown in Figure 71. This process took ~3 hours. Process B

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Process A	Process B	Process C
Process A Clean 15 minutes	**Process B** Clean 15 minutes	**Process C** Clean 15 minutes
Porous Silicon Etch 6 seconds	Porous Silicon Etch 6 seconds	Porous Silicon Etch 6 seconds
CF DOSS Emitter 925°C 150 minutes	RTP 725°C 6 minutes	RTP 725°C 6 minutes
SP Al BSF + Bake 200°C + Fire 850°C 8 minutes (Belt Furn.)	900°C RTP DOSS Diff. 6 minutes	SP Al BSF + Bake 200°C 2 minutes
SP Ag + Bake 200°C + Fire 730°C 8 minutes (Belt Furn.)	SP Al BSF + Bake 2 minutes	880°C RTP DOSS Diff. 6 minutes
	SP Ag+Bake+Fire 700°C 3 minutes (RTP)	SP Ag+Bake+Fire 700°C 3 minutes (RTP)
Total Time ~3 hours	Total Time ~32 minutes	Total Time ~32 minutes

V_{oc} J_{sc} FF Eff. FZ 624 29.9 74.9 **14.0** Cz 614 29.2 74.6 **13.4** Mc 619 26.9 75.5 **12.5**	V_{oc} J_{sc} FF Eff. FZ 603 28.6 76.2 **13.2** FZ 592 30.1 77.0 **13.7**	V_{oc} J_{sc} FF Eff. FZ 618 31.5 78.7 **15.3**

Figure 73. Process sequence diagram for porous silicon ARC solar cells using DOSS processing with and without RTP.

was developed to fabricate solar cells in the RTP in approximately 17 minutes after the initial cleaning. This process resulted in a much-improved front surface reflectance compared to Process A, as shown in Figure 72 (RTP anneal + RTP DOSS). However, to maintain the low reflectance of porous silicon, no BSF step was implemented in Process B because prolonged exposure to the oxygen ambient (~2 minutes) for screen-printed Al BSF formation was found to degrade the front surface reflectance. This resulted in a somewhat inferior red response (See Fig. 74) and lower cell efficiency of 13.7%.

Finally, a novel process sequence (Process C in Fig. 73) was developed that provides a proper BSF formation simultaneously with the emitter formation while limiting the oxygen exposure to the porous silicon etched surface. Here, Al is SP on the back prior to DOSS diffusion. Process C allows for BSF formation to match the standard process because the RTP DOSS diffusion temperature is 880°C, which simultaneously forms a good Al BSF on the rear. In Process B, the Al firing temperature was 700°C for only 1 second, which does not form a good BSF. A 15.3% efficiency was obtained using process C, an improvement of greater than 1% absolute efficiency over Process A and Process B. To our knowledge, this is the **highest reported efficiency for a porous silicon solar cell of any kind.** Figure 74 shows that the V_{oc} was 618 mV, J_{sc} was 31.5 mA/cm^2, and FF was very good (FF=0.787). Notice that the FF degradation is avoided by not exposing the SP metal contacts to porous silicon etching. Figure 74 shows the IQE and reflectance of RTP DOSS cells formed with RTP, along with the SiN coated standard cell. The solar cells processed by PS and RTP in <35 minutes achieved FFs in excess of 78% and efficiency of 15.3%. Thus, the high series resistance of the porous
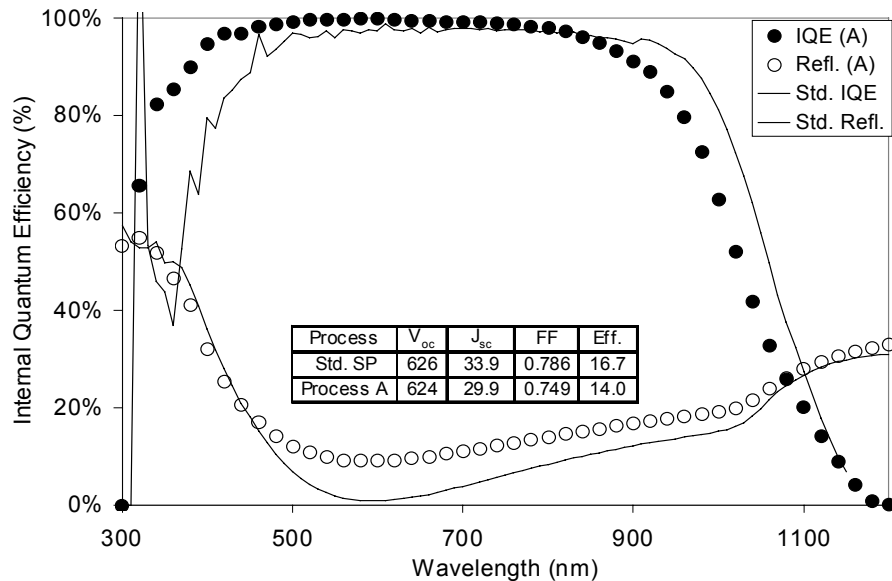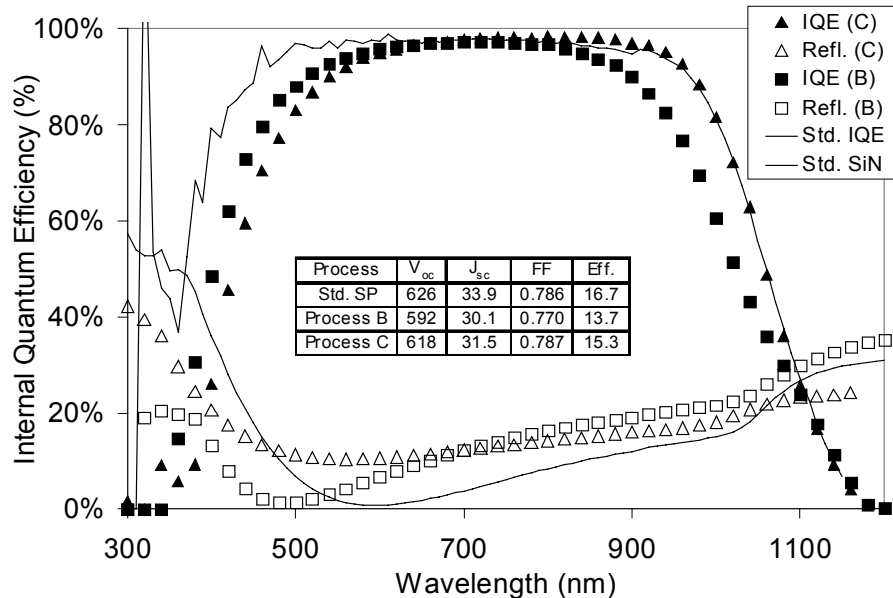
Figure 74. IQE and reflectance curves for the standard screen-printed solar cell and porous silicon ARC solar cells (Process B and Process C).

silicon layer did not limit the fill factor. Note that the efficiency was only ~1.5% lower than the standard cells with PECVD SiN$_x$ coating. Further optimization can reduce the gap between the two, especially because the reflectance was still not as good as a SiN ARC, but the potential for improved surface reflectance was demonstrated in Process B. Improved front surface passivation of the porous silicon etched cells may also help the efficiency.

The porous silicon layer provides a uniform coating that has a violet appearance on the entire wafer surface for samples that were dipped one to three times in the etching solution. The etching solution used in Process B, Process C, and Process D consisted of 1 part 70wt% HNO$_3$ and 200 parts 50wt% HF at room temperature, with no external heating or cooling. A sacrificial silicon wafer was used to initiate the homogeneous

etching on subsequently etched wafers. The sacrificial silicon wafer needed to have surface defects to catalyze the reaction. Figure 75 shows a picture of processed FZ Si, Cz Si, EFG ribbon silicon, and cast mc-Si wafers etched for <10 seconds to form a porous silicon layer as an ARC. RTP pretreatment in N_2 was found to stabilize the porous silicon layer. In addition, a short simultaneous RTP heat treatment was developed to form the n^+ emitter and p^+ BSF simultaneously without appreciably degrading the porous silicon reflectance. This process sequence also allowed for a much heavier diffusion for identically processed wafers if the RTP anneal process step was included in the fabrication sequence of the porous silicon etched samples.

Figure 75. Porous silicon etched wafers after DOSS diffusion. Top left – FZ, Top Right – cast mc-Si, bottom left – EFG ribbon, bottom right – Cz.

7.4 Conclusions

It was demonstrated that chemical porous silicon etching is a very simple and rapid technique for texturing single as well as multi-crystalline silicon. Low reflectance and good surface passivation were achieved using the DOSS solar cell process. The DOSS diffusion from a limited source wafer was tailored to obtain the desired sheet resistivity underneath the PS layer that gave high screen-printed solar cell performance (15.3%) with excellent fill factors (78.7%). This represents the highest efficiency porous silicon etched cell to date. Poor fill factors have been a problem in past investigations in the literature when etching was done after metallization. This problem was overcome in this research by PS etching prior to cell processing, which resulted in a 0.807 fill factor for photolithography cells. The in-situ oxidation in the DOSS process appears to completely oxidize the PS layer to provide excellent surface passivation. The DOSS process does not require the removal of the phosphor silicate glass after diffusion, which could keep the porous silicon layer intact, and prevents degradation of the reflection. Cell fabrication still needs to be optimized to realize the full potential of PS etching and understand its effects on all pertinent solar cell parameters.

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CHAPTER 8

8 IMPROVED REFLECTANCE BY A COMBINATION OF ACID TEXTURING AND POROUS SILICON ANTI-REFLECTION COATING FOR LOW-COST CRYSTALLINE SILICON SOLAR CELLS

The porous silicon etched solar cells fabricated in the previous section achieved a 15.3% conversion efficiency on FZ Si using a novel process sequence developed in this work. The total time used in the fabrication sequence was calculated to be ~32 minutes (not counting setup and cleanup or travel time between labs), making it attractive for industry. The long wavelength IQE in Figure 74 shows that the quality of the back surface field formation on a porous silicon etched surface is equivalent to the BSF formed on the flat back standard screen-printed solar cells. In addition, excellent fill factors with values up to 78.7% were achieved on screen-printed porous silicon etched solar cells using Process C (Fig. 73). Unfortunately, Figure 74 shows that the front surface reflectance was only slightly improved in Process C over the original Process A. Nevertheless, several technological advantages were achieved in Process C that resulted in more controlled processing capabilities and a 1.3% absolute efficiency improvement over Process A. One of the major findings involved "RTP anneal" after porous silicon formation to allow a heavier, more uniform phosphorus diffusion. The "RTP anneal" was also shown to do a better job of maintaining the reflectance of the porous silicon coated solar cells. To properly form the Al BSF, oxygen in the furnace ambient is required. Unfortunately, the presence of oxygen has a detrimental effect on the porous silicon anti-reflection coating. To further improve the conversion efficiency of porous silicon coated solar cells in the

previous section, reflectance should be improved further. In the following section an acidic texture prior to porous silicon formation is developed.

8.1   Characterization of Acidic Texture for Silicon Wafers Formed by Wire Saw

Acidic texture was discussed in Chapter 3 as being a promising technique for isotropic texturing of mc-Si wafers that are cut by a wire saw. Both Cz and cast mc-Si samples for PV are typically cut from an ingot by a wire saw, leaving significant surface damage. Various solutions have been used to achieve acidic texturing on mc-Si surfaces. Some of the more developed solutions are commercially available for purchase [56]. During the optimization of porous silicon etching in this research, a solution consisting of hydrofluoric, nitric, and acetic acids (in a ratio of 2:5:15 and subsequently referred to as the "2:5:15" etch) was found to produce isotropic acidic texturing on wafers cut from an ingot that had not been chem.-mechanically polished. In order to allow for texture formation, as received samples were submerged into the 2:5:15 etch prior to any chemical treatments. Initial investigations using this solution focused on establishing the effects of the acidic etch on the quality of surface texture. Figure 76 shows how the surface reflectance changed with increased etching time. Both Cz and cast mc-Si wafers showed the same trend, with an increase in total weighted reflectance for longer etching times as measured by a spectrophotometer (limited wavelength range 400 to 700 nm). The total weighted reflectance for both Cz and mc-Si in the wavelength range (400 to 700 nm) was 20-29% compared to ~ 35% for the bare silicon.
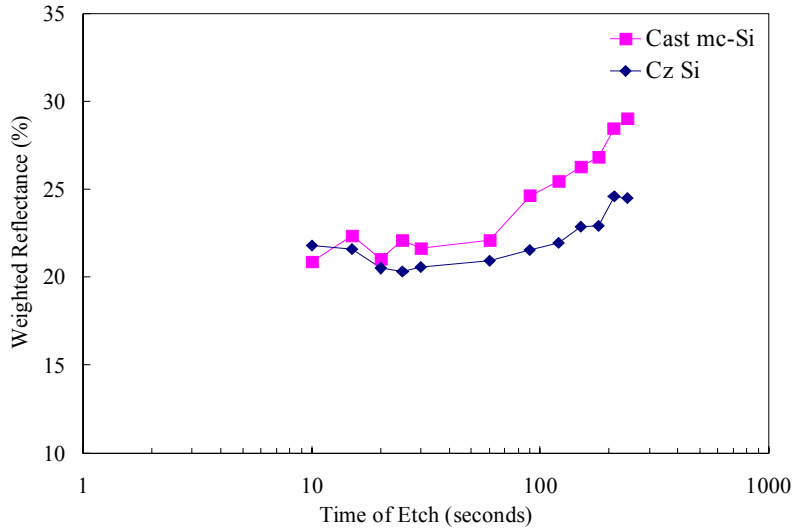
Figure 76. Weighted reflectance (400 to 700 nm) of acidic texture developed at Georgia Tech on cast mc-Si and Cz Si samples as a function of increasing etch time.

To better understand the effects of etching time on surface morphology, scanning electron microscopy was used to view the silicon surface. Figure 77 shows the surface morphology of the Cz and cast mc-Si wafers on a 5 μm scale (Fig. a, b, and c) and a 50 μm scale (Fig. 77d). Figure 77a shows the surface of a Cz wafer etched for only 10 seconds in the hydrofluoric, nitric, and acetic acid solution (2:5:15), while Figure 77b shows the surface of a Cz wafer etched for 60 seconds in the same solution. Figure 77a shows much more surface roughness with smaller feature sizes. Figure 77b shows much smoother features with crests and valleys on the order of 2 to 4 μm. Figure 77a appears to have much more significant surface damage that reveals a rough surface with a slightly lower weighted reflectance. However, it was pointed out in Chapter 3 that only a very slight surface texture (> ~21°) is needed to allow for increased light trapping via total

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internal reflection. Therefore, when considering the possibility of surface passivation and contact formation for screen-printed solar cells, an extremely rough surface may not be desirable. Figure 77c shows the SEM for a 60-second etch time on a cast mc-Si sample. Again, smooth surface features with etch pits and sharp peaks were observed, with feature sizes on the order of 2 to 4 μm. Finally, Figure 77d shows the SEM of a planar view of a cast mc-Si across a grain boundary. The grain boundary produces the slight discoloration of the SEM between the right and left sides. However, the acid texture was uniformly distributed, even on the micrometer scale for both crystal orientations. To further reduce the front surface reflectance, a Single Layer Anti-Reflection Coating (SLARC) can be deposited on top of the acidic texture.
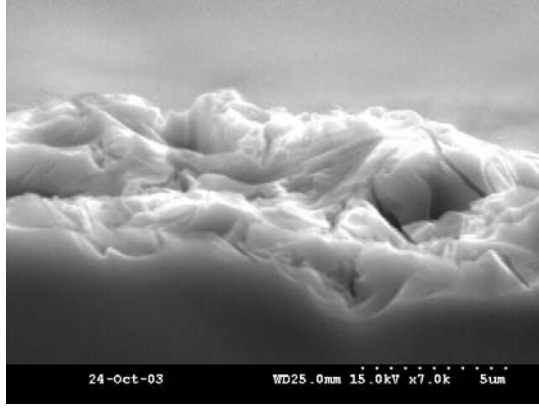
a.
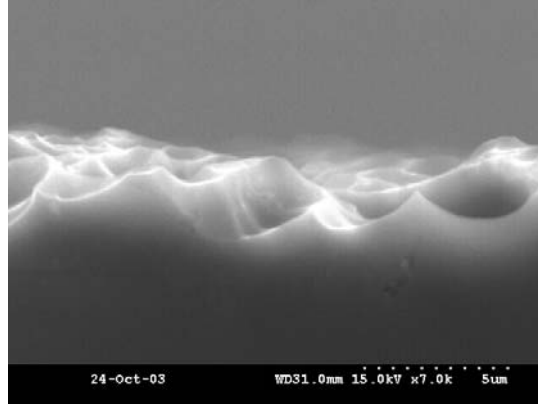
c.
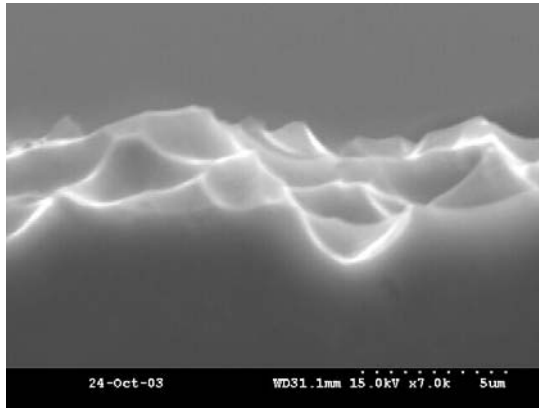
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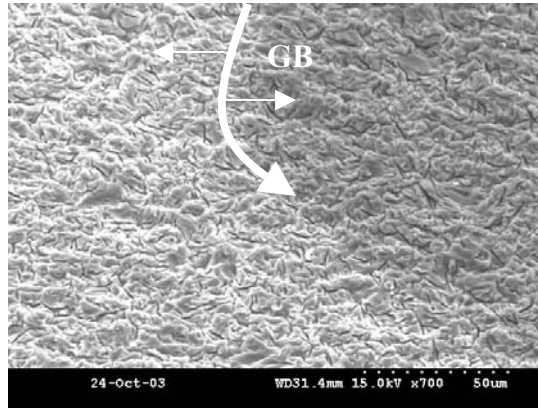
d.

Figure 77 (a, b, c, d). SEM pictures of crystalline silicon wafer surfaces after acidic texturing developed at Georgia Tech. Picture "a" shows the surface morphology of a Cz sample etched for 10 seconds. Picture "b" shows the surface morphology of a Cz sample etched for 60 seconds. Picture "c" shows the surface morphology of a cast mc-Si sample etched for 60 seconds. Picture "d" shows the surface morphology of a planar view for a cast mc-Si wafer across a grain boundary labeled GB.

8.1.1 Formation of Porous Silicon Layer on Top of Acidic Texture

The addition of either a SiN layer or a porous silicon layer can further reduce reflectance of an isotropically textured surface. Figure 78 shows the new weighted reflectance trend over the 400 to 700 nm range measured by a spectrophotometer. With the application of the SiN_x, the best weighted reflectance in the 400 to 700 nm range (Cz = 2.9% for 240 seconds, and cast mc-Si = 5.5% for 240 seconds) occurred for longer etching times for a fixed SiN deposition time (thickness = 78 nm on a planar surface). By tailoring the SiN layer thickness for the samples etched for 60 seconds a **weighted reflectance of 2.9%**
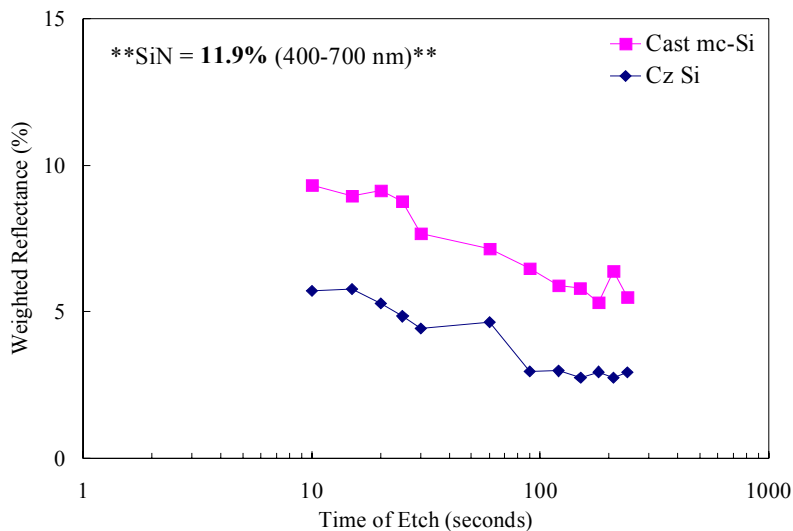
Figure 78. Weighted reflectance behavior of Cz Si samples that were submerged in an acidic texture for various amounts of time and then subsequently coated with a SiN layer that would deposit 78 nm on a planar surface.

was achieved in the 400 to 700 nm range for both **Cz and cast mc-Si** (*not shown in Fig. 78*).

The impact of porous silicon etching on top of an acidic textured surface was explored to further improve the reflectance of porous silicon coated DOSS diffused RTP solar cells. First, Cz and mc-Si samples were acid textured using a 60-second etch time. Next, samples were submerged in the optimized porous silicon solution for various lengths of time after the standard RCA cleaning process. Figure 79 shows the reflectance curves generated by spectrophotometer measurements in the 400 to 700 nm wavelength range. Notice the very low reflectance values on the y-axis. All reflectance values are under
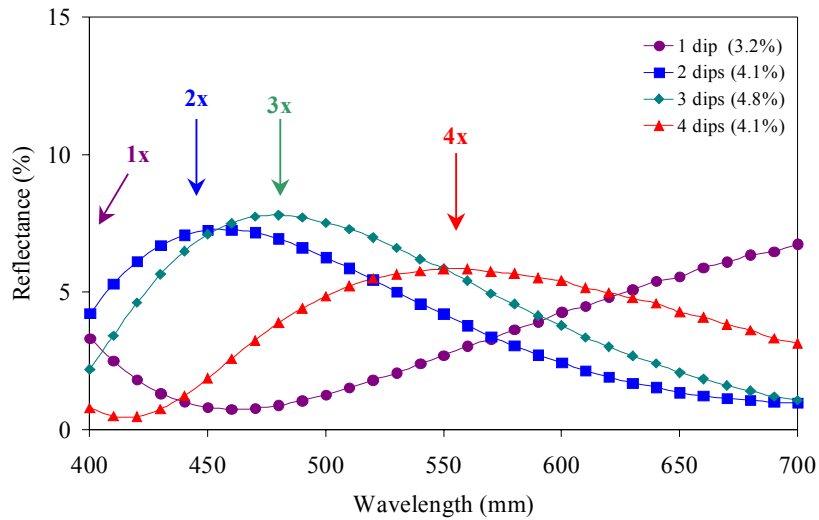
Figure 79. Porous Si etched acid textured Cz wafers for multiple dips into the optimized porous silicon etching solution. Notice the shift of the initial peak to longer wavelengths with increasing time. The weighted reflectance for the 400 to 700 nm wavelength range is denoted in parenthesis.

10% for the entire 400 to 700 nm wavelength range. In addition, the effect of the porous silicon etching was similar to the effect of porous silicon etching of planar surfaces for various lengths of time shown in Figure 62 in Chapter 7. The porous silicon etching was not detected by SEM imaging, but the optical microscope in Figure 80 shows the blue-violet color of porous silicon on top of the acidic texture of a Cz Si wafer. The next challenge was to incorporate the new acid texture into a modified fabrication sequence similar to that of Process C to optimize porous silicon etched solar cell performance.

Some important observations made during acidic texture development are important to consider when designing a formation sequence. First, the acidic texture does not texture surfaces that have been chemically polished. A defective surface was needed to initiate texturing. In addition, the porous silicon etch did not react on an acidic textured surface upon direct submersion into the solution. For porous silicon etching to occur, a sacrificial silicon wafer with a defective surface needed to be submerged to catalyze the etching for a few minutes. Once the etching started, all surface morphologies explored in this work could be successfully etched, including acidic textured surfaces and polished surfaces, as well as conventional alkaline textured surfaces.
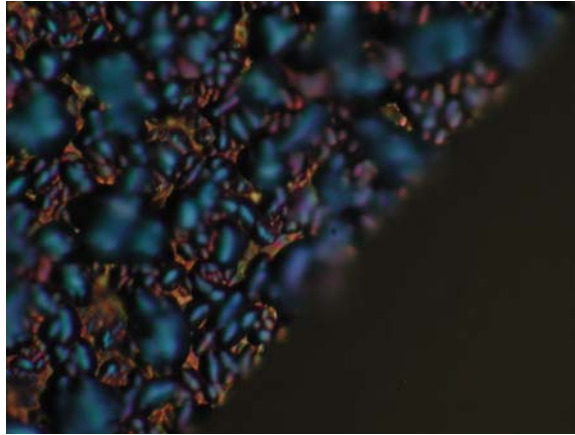
Figure 80. Optical microscope view of the edge of an acid textured Cz Si sample etched in a porous silicon solution at 50X magnification.

8.2 Rapid Thermal Processing of Low-Cost Czochralski and Cast Multi-Crystalline Silicon Solar Cells Using a Porous Silicon Anti-Reflection Coating

In this section Process C was modified to include acid texturing as the first chemical etch.

This led to Process D, shown in Figure 81. This process is similar Process C, with the exception of the acidic texture being used as the initial step (for all wafers cut from an ingot) and a reduced RTP anneal time to 2 minutes in step 3 instead of 6 minutes. Recall that the addition of RTP anneal in Process B and Process C allowed the porous silicon etched samples to retain reflectance properties and behave similarly to the planar control samples during the DOSS diffusion process. The addition of the acidic texture step required a slight re-optimization of the diffusion process. Figure 79 shows that minimum reflectance can be controlled by the etching time and is shifted to longer wavelengths for increased dwell time (6 to 12 seconds) in the solution. This is depicted in Figure 79 by the arrows pointing to a local maximum labeled with 1X, 2X, 3X, or 4X, where

| Process D |
| Acid Texture + Clean
15 minutes |
| Porous Silicon Etch
6-12 seconds |
| RTP anneal 725°C
2 minutes |
| SP Al BSF + Bake 200°C
2 minutes |
| 880°C RTP DOSS Diff.
6 minutes |
| SP Ag+Bake+Fire 700°C
3 minutes (RTP)

Total time = ~28 min. |

Figure 81. Process D sequence diagram for porous silicon ARC solar cells using DOSS processing

"X" represents one unit of time, which in this research is ~3 seconds. Therefore, 3X would represent a dwell time of ~9 seconds in the porous silicon etch solution.

Figure 82 shows the IQE and total reflectance of two Cz cells fabricated using Process D with two different dwell times (6 and 9 seconds) in the porous silicon etch. Again, there was a red shift in the reflectance local minima for the 3X (9 seconds) dwell time compared to the 2X (6 seconds) dwell time in the finished solar cells. The total weighted reflectance values are also shown in the figure. A lower total weighted reflectance of 8.3% was achieved for the cell etched for 3X compared to the cell etched for 2X, which resulted in 9.9%. This 1.6% decrease in weighted reflectance amounts to ~0.5 mA/cm^2 increase in J_{sc} for screen-printed devices. This increased the solar cell efficiency in the 3X devices by more than 0.5% (from 14.1% to 14.8%) absolute.
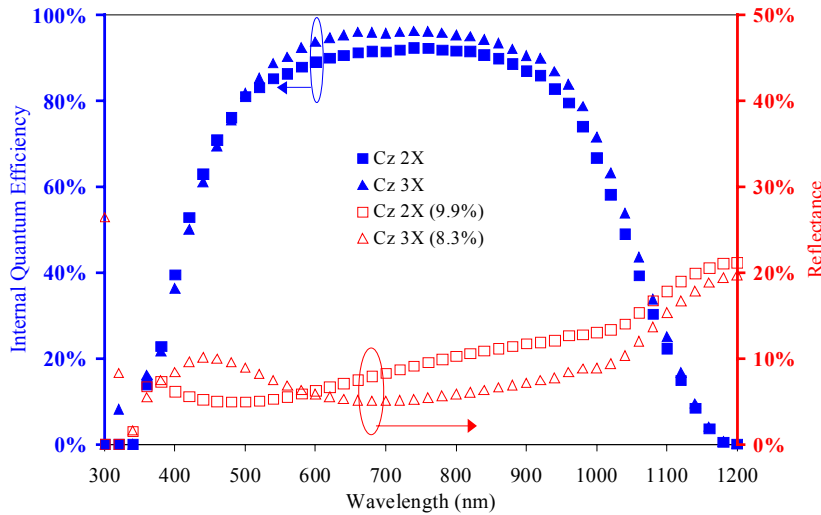
Figure 82. Internal Quantum Efficiency (primary y-axis) and total reflectance (secondary y-axis) for acid textured porous silicon etched RTP processed Cz silicon solar cells using Process D.

The IQE performance in Figure 82 shows a slight improvement for the 3X sample over the 2X sample in the mid-range wavelengths (500 to 900 nm). This part of the IQE curve holds information about the bulk lifetime and some surface effects. The slightly improved IQE in the mid-range wavelengths could also suggest improved light trapping for the 3X sample. However, this was not verified by additional experimentation. Next, the improved reflectance for the Cz silicon solar cell using Process D was compared to the standard SiN coated FZ solar cell. Figure 83 shows the measured IQE and total reflectance of the standard SiN FZ cell, the "Process C" FZ cell, and the "Process D" Cz cell. The total weighted reflectance for each cell measured by an integrating sphere is also shown in Figure 83. The Cz silicon solar cell fabricated with Process D showed a significantly better total weighted reflectance of 8.3% compared to both the standard SiN coated FZ cell (12.4%) and the "Process C" FZ cell (13.2%). Some improvement was observed over the standard cell in the short wavelength region (<450 nm). However, the lower reflectance in the long wavelength regime was outstanding, accounting for part of the 4% improvement in weighted reflectance. This represents an opportunity to enhance the efficiency of lower lifetime materials by trapping a larger portion of the useable light for energy conversion into the solar cell. Also note that the "Process D" Cz solar cell has a lower reflectance than the SLARC SiN coating for all wavelengths above ~700 nm. As expected, the IQE data in the mid- to long wavelength range indicates that the bulk lifetime of the FZ samples is superior to that of the Cz solar cell. However, the IQE data in the short wavelength range reveals that the front surface passivation for the Process D and Process C devices is essentially the same. Thus, the front surface acid texture

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incorporated in Process D does not adversely affect the front surface passivation compared to the chemically polished porous silicon etched FZ surface in Process C.
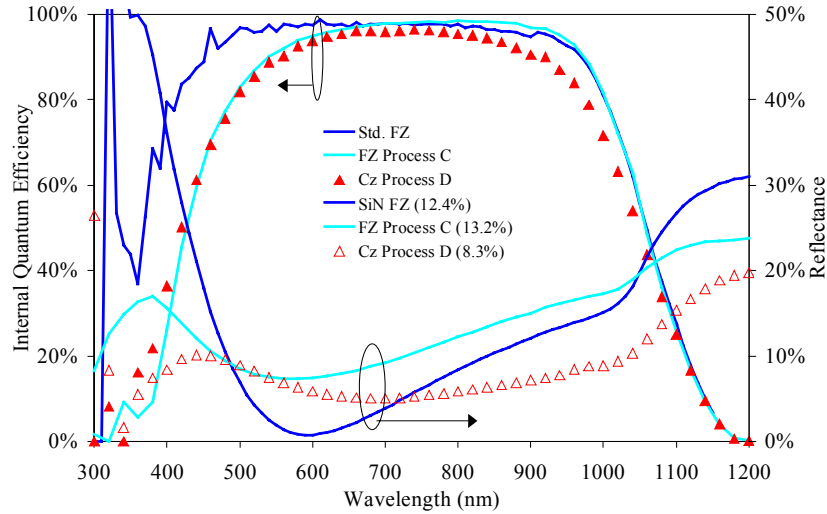
Figure 83. Internal Quantum Efficiency (primary y-axis) and total reflectance (secondary y-axis) for the standard FZ screen-printed solar cell process compared to a porous silicon etched FZ (Process C) and Cz silicon solar cell (Process D).

Next, the impact of Process D on the performance of cast mc-Si devices was compared and analyzed using lighted current-voltage (I-V) characteristics of four different solar cells. Table 10 shows the highest cell efficiencies obtained for various device structures fabricated using slight modifications to Process D on Bayer cast mc-Si samples. The I-V parameters are listed for comparison. In addition, a net gain or loss of J_{sc} is listed in the final column.

Table 10. Cell efficiency performance for various surface treatments on cast mc-Si wafers

Surface Morphology	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	J_{sc} Gain (mA/cm^2)
aTx+SiN	591.3	32.9	76.2	14.8	**0.0**
SiN	598.9	32.2	77.6	15.0	**-0.7**
aTx+PS (D)	594.2	30.9	73.9	13.6	**-2.0**
PS (C)	591.5	30.6	74.1	13.4	**-2.3**

The last column of data represents the current density gained by incorporating the given surface morphology compared with an acidic textured SiN coated cell on the Bayer cast mc-Si substrate, which gave the highest J_{sc}. Open circuit voltages for all devices were in the range of 590 to 600 mV. The emitter sheet resistivity was 40 to 55 Ω/sq. on all the cast mc-Si wafers, regardless of surface morphology, for the same RTP diffusion cycle. The sample labeled "aTx+SiN" was used as the reference solar cell and achieved the highest short circuit current (32.9 mA/cm^2) because the sample was acid textured and then coated by a SiN_x SLARC, resulting in the lowest front surface reflectance. If the acid texture were eliminated and replaced by a chemical polish, the resulting solar cell efficiency for a SiN_x coated solar cell would result in the loss of approximately 0.7 mA/cm^2 because of the increased front surface reflectance. Using the acid textured porous silicon (aTx+PS) etched surface the loss of photo-current was 2 mA/cm^2 compared to the "aTx+SiN" sample. Using a porous silicon etched ARC on the Bayer cast mc-Si sample gave a cell structure that resulted in the loss of 2.3 mA/cm^2. Thus, the

lower reflectance achieved by Process D (aTx+PS) resulted in a slightly improved device performance than Process C (PS) and also closed the gap in efficiency between SiN_x coated devices and porous silicon coated devices.

8.3 Efficiency Improvement of Low-Cost Czochralski and Cast Multi-Crystalline Silicon Solar Cells with Porous Silicon Anti-Reflection Coatings

The motivation to form a porous silicon anti-reflection coating prior to any high temperature processing and metallization resulted in the development of a novel process sequence capable of rapidly producing respectable solar cells without the need for widely used SiN single layer anti-reflection coatings. The first generation porous silicon etched DOSS diffused solar cells were greatly improved through process sequence optimization performed in this thesis. Table 11 shows the achievements and challenges faced during the process development of the porous silicon etched, RTP DOSS diffused solar cell process fabricated in this work.

Table 11. List of positive and negative attributes for Cz Si solar cells fabricated with each process sequence developed at Georgia Tech.

Process	J_{sc} mA/cm^2	V_{oc} mV	Achievements	Challenges
A (CF)	29.9	611	1. Porous Silicon ARC 2. pn junction formation 3. Stable FF 4. Excellent FSRV	1. Longer Process 2. High Reflectance due to O$_2$ ambient for Diffusion
B (RTP)	28.0	594	1. Fast Process 2. Porous Silicon ARC 3. pn junction formation 4. Stable FF 5. Better Maintain Refl.	1. Poor FSRV 2. No BSF (limit O$_2$) 3. R_w inferior SiN$_x$
C (RTP)	27.9	604	1. Fast Process 2. Porous Silicon ARC 3. pn junction formation 4. Stable FF 5. Excellent BSF	1. Poor FSRV 2. R_w inferior - (B) and SiN$_x$
D (RTP)	32.1	611	1. Fast Process 2. Porous Silicon ARC 3. pn junction formation 4. Stable FF 5. Excellent BSF 6. R_w lower than SiN$_x$	1. Poor FSRV

Process A demonstrated the capability of using DOSS diffused emitters to incorporate a porous silicon texturing prior to any high temperature processing, while still maintaining a reduced reflectance through the use of the porous silicon ARC. Excellent front surface recombination velocities (FSRV) were achieved, but further development of the process was not possible because the reflectance could not be optimized in the finished solar cells. Therefore, RTP diffusion was explored. Process B incorporated the RTP anneal step, allowing the initial reflectance behavior to be better maintained. However, no BSF

formation was used because the incorporation of oxygen during any high temperature processing caused increased reflectance. Therefore, Process C was developed to incorporate a BSF structure to improve solar cell efficiency without using a dedicated BSF formation step. Rather, the emitter diffusion and BSF formation were achieved simultaneously during the RTP diffusion step. Still, the weighted reflectance for Process C devices was inferior to SiN_x single layer anti-reflection coatings. **Finally, Process D allowed for BSF formation, emitter diffusion, acid texturing, and a porous silicon ARC, resulting in a weighted reflectance superior to a SiN SLARC.**

Table 12 shows the efficiency improvement on the low-cost cast mc-Si and Cz Si substrates from the first generation screen-printed solar cells fabricated using Process A to the best efficiency achieved using Process D. **Process D gave a Cz cell efficiency of 14.8% for a 4 cm^2 device**. Nine 4 cm^2 solar cells fabricated on a 100 cm^2 Cz silicon wafer gave a J_{sc} distribution that ranged from 31.0 to 32.1 mA/cm^2 across the entire wafer, demonstrating the uniformity of the porous silicon ARC.

Table 12. Lighted I-V parameters for screen-printed solar cells fabricated using Process A and Process D for cast mc-Si and Cz Si solar cells.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor (%)	Efficiency (%)
mc-Si (Process A)	619	26.9	75.5	12.5
mc-Si (Process D)	594	30.9	73.9	**13.6**
Cz (Process A)	*614*	*29.20*	*74.6*	*13.4*
Cz (Process D)	*612*	*32.12*	*75.3*	***14.8***

Approximately **3 mA/cm^2** in short circuit current density was gained by going **from Process A to Process D** in Cz Si samples for similar resistivity wafers. An increase of 4

mA/cm^2 in short circuit current density was gained in cast mc-Si solar cells from Process A to Process D. The slightly higher increase in J$_{sc}$ for the mc-Si sample was in part due to the lower resistivity sample used for Process A (0.2 Ωcm) compared to the resistivity for the mc-Si sample used for Process D (1.0 Ωcm). Lower resistivity samples tend to have higher V$_{oc}$'s but slightly lower J$_{sc}$ for screen-printed devices. The technologies that allowed for such a significant improvement in the J$_{sc}$ involve the use of the RTP anneal step to allow for improved emitter performance while maintaining a much lower surface reflectance after high temperature processing and the inclusion of the acidic texture to help further reduce the total weighted reflectance to 8.3% in finished solar cells. The total weighted reflectance was lower than that of the traditional SiN$_x$ single layer anti-reflection coating (12.4%) deposited by PECVD. Even though the overall efficiencies are 1 to 2% lower than those of traditional high performance SiN coated cells, the 15.3% FZ and 14.8% efficient Cz porous silicon textured cells represent very respectable efficiencies without the SiN ARC. These efficiencies also represent the highest efficiencies known to date for screen-printed porous silicon textured solar cells (Fig. 84).
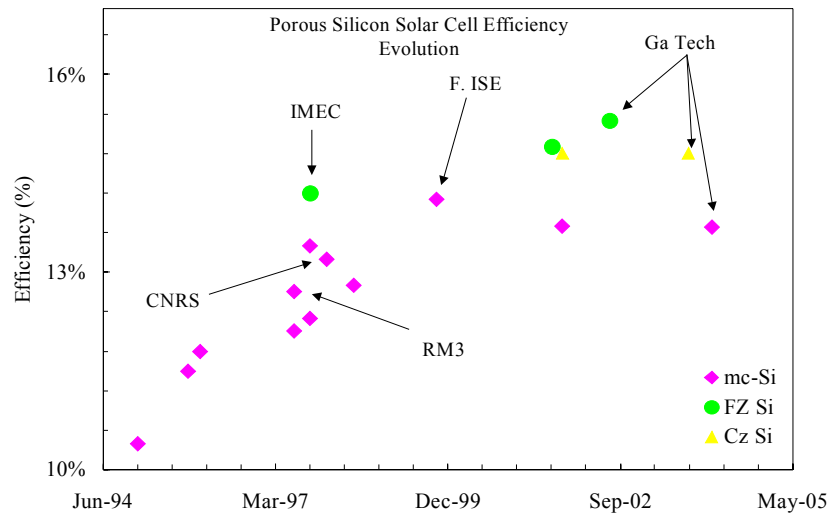
Figure 84. Efficiency evolution for all types of porous silicon etched solar cell structures, including photolithography. All reported efficiencies from Georgia Tech are manufacturable screen-printed devices [33, 36, 38, 39].

8.4 Conclusions

The addition of an acidic texture to Cz and cast mc-Si solar cells resulted in the highest efficiency screen-printed porous silicon solar cells fabricated to date. A 14.8% Cz Si and a 13.6% cast mc-Si solar cell efficiency was achieved using Process D developed in this work. These efficiencies are lower than that of traditional SiN coated solar cells but still represent the opportunity to use an alternative ARC that is less expensive and rapidly formed while still achieving a decent level of performance. The weighted reflectance of Cz silicon solar cells fabricated with Process D (8.3%) obtained a lower weighted reflectance than the traditional SiN single layer anti-reflection coating (12.4%). Thus, the development of a rapid, inexpensive texture and ARC was achieved through the use of porous silicon etching and the DOSS diffusion technique.

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CHAPTER 9

9   GUIDELINES FOR FUTURE RESEARCH

9.1   Future Research for Light Induced Degradation

Ribbon and cast multi-crystalline silicon solar cell efficiencies have dramatically improved over the last decade with the incorporation of hydrogenation to getter the bulk lifetime. Initially, the bulk lifetimes of these materials were too low to detect any light induced degradation. However, as the efficiencies for these promising materials approach values equal to Czochralski silicon devices, the presence or absence of light induced degradation needs to be properly determined. Degradation conditions need to be such that realistic operating conditions are simulated so that the degradation can be properly assessed. The extent of light induced degradation in ribbon and cast mc-Si samples needs to be statistically investigated to properly assess the impact of LID in these materials.

Another area of interest touched upon in this research is the creation of traps via charged carrier diffusion in the lateral direction of the Czochralski silicon wafer. A more precise experimental setup could provide additional information concerning trap characteristics, such as the diffusion length.

The spatial non-uniformity in cast mc-Si needs further investigation. If the trap responsible for light induced degradation is dependent on the spatial distribution of O_i

concentration in cast mc-Si, then a study to determine the spatial distribution of O_i both as a function of ingot depth and lateral concentration would be helpful. By observing the lateral distribution of the oxygen and LID trap simultaneously, a deeper understanding of the trap could be attained. Further investigations of light induced degradation may provide alternative methods to mitigate and reduce the metastable defect in finished solar cells.

The ribbon crystalline silicon materials investigated in this research showed various levels of light induced degradation that were strongly dependent on ambient conditions. A thorough investigation of the cyclical generation/annihilation process related to ribbon crystalline silicon would provide interesting results. Characterization of the activation energy and annihilation energy through the use of the equations in Chapter 4 would further clarify the characteristics associated with light induced degradation in multi-crystalline silicon substrates.

9.2   Future Research for Porous Silicon Anti-Reflection Coatings

Future research topics related to the application of porous silicon anti-coatings using the DOSS process include the following:

1. Figure 82 shows the IQE associated with two different Cz Si solar cells that were acid textured and porous silicon etched. The Cz wafer labeled "3X" shows a slightly higher IQE performance in the mid-range wavelengths (500 to 800 nm), suggesting that either the bulk lifetime was improved by the "3X" sample or the

that the light was being more effectively trapped. Investigating light trapping capabilities to further enhance efficiency performance could also reduce the dependence on bulk lifetime and provide a tighter efficiency distribution for cell manufacturers.

2. The determination of an effective surface passivation of the highly reactive surface during solar cell processing needs to be investigated. As was shown in the IQE behavior of the RTP processed solar cells in this research, the short wavelength response was less than desirable. Porous silicon hydrogenation is one such possibility to achieve better surface passivation. One of the big advantages of SiN is the incorporation of hydrogen during cell processing. Prior to plasma deposition, solar cells are pretreated with NH_3 in the plasma tube. The highly reactive surface of freshly etched porous silicon could act as a sink for the NH_3. Instead of an RTP anneal step in nitrogen, a different process step could be explored to increase front surface passivation.

3. Another possible surface passivation method could be to apply a very thin SiN layer. The purpose of the SiN layer could be for a double layer anti-reflection coating or simply surface passivation and hydrogenation.

4. Application of the porous silicon process sequence to large area screen-printed devices is another area of interest.

5. Porous silicon texturing is effective on all crystalline silicon surfaces. In addition, even textured surfaces can be porous silicon etched. Porous silicon coatings on top of a random pyramid structure, a mechanically grooved surface, or even a porous silicon etched RIE surface may produce excellent solar cell structures.

APPENDIX A

Measurement Theory

Lifetime

Surface passivation is one of the key ingredients that has allowed for improved solar cell efficiency over the past decade. There are various methods used for surface passivation. Silicon substrates frequently make use of silicon dioxide (SiO_2), which forms readily at the surface of Si at high temperatures (>850°C) and is very effective at passivating dangling bonds at the edge of a crystal structure. Surface passivation focuses on maintaining bulk properties of the silicon substrate. Minority carrier diffusion length (L_n), bulk lifetime (τ_b), Surface Recombination Velocity (SRV), dark current density J_o, and open circuit voltage V_{oc} can all be used to characterize surface passivation. Initially, the dark current density effects of surface passivation will be examined.

$$J_o = qn_i^2 (\frac{D_n F_P}{L_n N_A} + \frac{D_p F_N}{L_p N_D})$$

(52)

The dark current density of a solar cell is in principle the same J_o in a diode, where F_P and F_N account for surface effects on the p-type side and n-type side, respectively. In a solar cell, the dark current density can also be viewed as the emitter component and the base component ($J_o = J_{oe} + J_{ob}$). J_o needs to be minimized in order to maximize the efficiency of the solar cell. One of the contributing factors to an increased dark current density is a high SRV. To reduce J_o, the front and rear surfaces of the solar cell need to be

passivated. Rear surface passivation often differs from front surface passivation because different device properties are desired at each surface. The traditional rear surface passivation is the high-low junction or Back Surface Field (BSF), pp$^+$ structure. The back of the solar cell is heavily doped, usually to a sheet resistivity of ≤ 25 Ω/sq., which acts to shield minority carriers from the back surface where the metal is contacted. Metal contacted to silicon has a SRV approximately equal to 10^6 cm/sec, essentially infinite. Solar cells are a minority carrier device and the loss of carriers to recombination of any kind reduces the current and thus lowers the overall efficiency. Figure 15 shows a diagram of the band gap of a traditional BSF n$^+$pp$^+$ solar cell. High SRV causes the effective lifetime (τ_{eff}) of a solar cell to be shorter. The τ_{eff} is the amount of time a minority carrier is active after an electron-hole pair (EHP) is formed before recombination. It can be thought of analytically as

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \; ; \text{ where } \frac{1}{\tau_b} = \frac{1}{\tau_{SRH}} + B_n n + C_n n^2 \text{ (electrons)} \tag{53}$$

where τ_b is the lifetime of the bulk region and τ_s is the surface lifetime (or surface recombination rate provides a good analogy). τ_s is often described in terms of SRV, and J_{oe} or J_{ob}. Bulk lifetime τ_b, is a function of Auger ($C_n n^2$), band-to-band ($B_n n$), and Shockley-Read-Hall (τ_{SRH}) recombination. If the surface is poorly passivated, the surface recombination rate increases and τ_s decreases. A well-passivated surface will decrease the SRV and increase τ_s which makes τ_{eff} more dependent on τ_b. This is the desired result. The goal of surface passivation is to maintain bulk properties or improve them. To determine the quality of surface passivation, one needs to be able to make the appropriate measurements and quantify the results. A very popular method is to analyze

the lifetime of the material using the correct boundary conditions that can be controlled by the device structure. Lifetime is traditionally measured using a photoconductance decay (PCD) method. The principles behind lifetime measurements are derived from the change in the conductance of a semiconductor under illumination resulting from the injection of EHPs. This can be seen analytically by first examining the conductivity of a solar cell:

$$\sigma = q\mu_n n + q\mu_p p \tag{54}$$

$$n_o = n_i e^{q(E_f - E_i)/kT} \tag{55}$$

$$p_o = n_i e^{q(E_i - E_f)/kT} \tag{56}$$

where σ is the conductivity, n and p are the carrier concentrations of electrons and holes, respectively, E_f is the energy of the fermi level, E_i is the intrinsic energy level or mid-band gap, μ_n and μ_p are the electron and hole mobility, and T is the temperature. Under illumination, carriers are injected and "quasi"-fermi levels are formed for each carrier concentration. If we assume δ EHPs are injected, then

$$n = n_o + \delta \text{ ; or } n = n_i e^{q(E_{fn} - E_i)/kT} \tag{57}$$

$$p = p_o + \delta \text{ ; or } p = n_i e^{q(E_i - E_{fp})/kT} \tag{58}$$

where E_{fn} and E_{fp} are the quasi-fermi levels for electrons and holes, and there is a change in carrier concentrations, which results in a change in the conductance of the semiconductor by

$$\sigma = q\mu_n (n + \delta) + q\mu_p (p + \delta) \tag{59}$$

which increases the conductance or lowers the resistance. The PCD method traditionally uses a short light pulse and then records the exponential decay of the conductance. This change in conductance can be measured by coupling an inductor to the sample and measuring the change in voltage across the semiconductor. Figure 85 shows a diagram of the circuit used to measure the change in voltage that is then related to a change in the conductance. This change in conductance is used to monitor the number of injected carriers. The thickness of the material as well as the base conductance must be known to properly extract the number of injected carriers. Many semiconductor properties can be derived from this relationship between the change in conductance and injected carriers. First, SRV is analyzed. Non-diffused surfaces are relatively simple. Starting with the continuity equation and applying the boundary condition that the entire substrate is
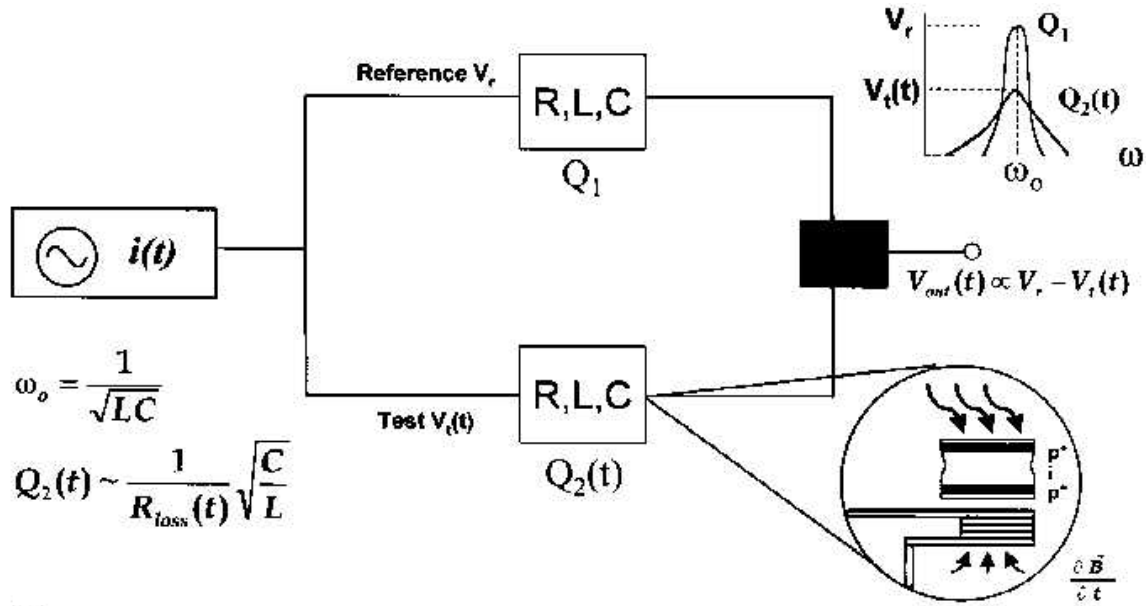
Figure 85. Using Maxwell's laws and a basic circuit structure, the Q factors are nulled initially to get maximum signal. The change in voltage response is then analyzed to yield the carrier lifetime. Many considerations need to be accounted for in the circuit design and measurement reliability range.

uniformly illuminated, so that there is no diffusive component to the recombination of the carriers, the equations reduce as follows:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} - \frac{n}{\tau} \tag{60}$$

$$J_n = q\mu_n nE + qD_n\frac{\partial n}{\partial x} \rightarrow qD_n\frac{\partial n}{\partial x}\Big|_{E=0} \tag{61}$$

$$\frac{\partial n}{\partial t} = D_n\frac{\partial^2 n}{\partial x^2} - \frac{n}{\tau} \Rightarrow \frac{\partial n}{\partial t} = -\frac{n}{\tau}\Big|_{NoDiffusion} \tag{62}$$

where E is the electric field, D_n is the electron diffusion constant, t is time, and J_n is the electron current density. Solving this differential equation, eq. (62), shows the exponential dependence of the carrier lifetimes.

$$n(t) = n(0)e^{-t/\tau} \tag{63}$$

Using eq. (62) and solving for the $1/\tau$ term, the following relationship is obtained:

$$\frac{1}{\tau} = -\frac{1}{n(t)}\frac{\partial n(t)}{\partial t} \tag{64}$$

where n(t) is the time-dependent carrier concentration. Equation (63) shows the exponential decay of injected carriers as a function of time. A pulse of light uniformly illuminates the entire wafer surface. Then, the change in conductance is measured. Using the change in conductance to monitor n(t) provides the information necessary to derive the effective lifetime (τ_{eff}). Equation (64) applied to eq. (63) shows analytically how to extract the desired information. From this effective lifetime, the following analysis can be performed to derive the SRV for a non-diffused surface. From the paper written by Luke and Cheng [65], τ_{eff} was found to behave according to the following relationships:

$$-\frac{1}{n(t)}\frac{\partial n(t)}{\partial t}=\frac{1}{\tau_{eff}}=\frac{1}{\tau_n}+D_n\beta^2 \qquad (65)$$

$$\beta \tan\frac{\beta W}{2}=\frac{S}{D_n} \qquad (66)$$

$$\beta=\sqrt{\frac{1}{D_n}(\frac{1}{\tau_{eff}}-\frac{1}{\tau_n})} \quad \text{vs.} \quad \text{n} \qquad (67)$$

where S is the surface recombination velocity (SRV), β is a transcendental term described by eq. (66) that results from solving a complex differential equation involving derivatives with respect to both space and time and therefore cannot be solved in closed form (starting from the continuity equation), and W is the width of the sample. If you assume S→∞, then eq. (65) reduces to (which is accomplished by surface roughing)

$$\frac{1}{\tau_{eff}}=\frac{1}{\tau_n}+D_n\frac{\pi^2}{W^2} \text{ ; thus, } D_n \text{ can be measured} \qquad (68)$$

and if S→0, then (which is accomplished by HF passivation)

$$\frac{1}{\tau_{eff}}=\frac{1}{\tau_n}+\frac{2S}{W} \quad \text{ ; thus, S can be measured} \qquad (69)$$

To determine the effective lifetime when S is between 0 and ∞, first measure τ_{eff} with the oxide passivation, next the bulk lifetime (in HF) and then make a plot of equation (67) and use β in eq. (66) to solve for S. A simple Si-SiO$_2$ surface is generally the best passivation, but because a low resistivity substrate is needed for good contact, higher SRV values result from the heavier base doping. For a diffused surface, both J_{oe} and $J_{ob'}$ can be derived. $J_{ob'}$ is the dark current density that results from the BSF formation. It gives a good indication of the effective surface passivation at the rear of the cell. $J_{ob'}$ is

only a fraction of J_{ob} and should not be confused. The diffusion being analyzed determines the steps necessary to extract the SRV for a diffused surface from a PCD measurement. There are three initial assumptions that are the same for either junction: the carrier concentration, $n(x)$, is assumed constant in the base; $D_n/L_n >$ "Instantaneous" SRV at the junction, which also ensures that the carrier concentration remains constant in the sample and also places an upper limit on the value of J_{oe} that can be measured at ≈ 1 pA/cm^2; and the last assumption is that the substrate is under HLI so the np product is equal to n^2 [66-67]. This is important so J_o can be properly extracted. For example, at the surface of a p-type substrate with an n-type diffusion, the recombination current is equal to the increased minority carrier dark current, which results because of the increase of carriers under light. This can be seen mathematically by realizing that because of the change in carrier concentration, the correlated dark current density (or recombination current) must also increase if under open circuit conditions (generation rate must equal the recombination rate for charge nuetrality). From eq. (57) and eq. (58), the increase in carriers is accounted for by the quasi-fermi levels that result from the light pulse. The resulting current density increases by the "applied" voltage from the light biasing. Thus,

$$J_{oe} = -q\frac{D_n}{L_n}n_p\bigg|_{light} \rightarrow J_{oe,light} = -q\frac{D_n}{L_n}n_{po}e^{E_{fn}-E_{fp}/kT} = -J_{oe}e^{E_{fn}-E_{fp}/kT} = J_E \qquad (70)$$

where J_{oe} is the saturation current of the diffused region. Now, using eqs. (57) and (58) to form the new np product, the quasi-fermi levels can be expressed as

$$np = n_{po}p_{po}e^{E_{fn}-E_i/kT}e^{E_i-E_{fp}/kT} = n_{po}p_{po}e^{E_{fn}-E_{fp}/kT} \qquad (71)$$

$$E_{fn} - E_{fp} = kT(\ln\frac{np}{n_i^2}); \quad \text{where } n_i^2 = n_{po}p_{po} \qquad (72)$$

If HLI is assumed, then np=n^2 and eq. (72) can be substituted into eq. (70) and the emitter recombination current is found equal to

$$J_E\big|_{x=0,W} = qD_n \frac{\partial n}{\partial x} = \pm J_{oe} \frac{n^2}{n_i^2} \tag{73}$$

where W is the width of the sample, J$_E$ is the total recombination current, and the middle equation comes from eq. (61). This provides a direct link between the recombination current and the number of injected carriers for a diffused surface and serves as the boundary condition. This argument can be used under the assumption made earlier that the total carrier concentration is constant spatially in the bulk.

$$\frac{1}{W} \int_{x=0}^{x=W} \left(\frac{\partial n}{\partial t} = D_n \frac{\partial^2 n}{\partial x^2} - \frac{n}{\tau_b} \right) \partial x \tag{74}$$

and performing the integration results in the following equation

$$\frac{\partial \overline{n}}{\partial t} = D_n \frac{\partial \overline{n}}{\partial x}\bigg|_{x=W} - D_n \frac{\partial \overline{n}}{\partial x}\bigg|_{x=0} - \frac{\overline{n}}{\tau_b} \tag{75}$$

where $\overline{n}$ is the average carrier density, which is assumed constant. Now, a simple substitution of the emitter saturation current density established in eq.(73) allows for

$$\frac{\partial \overline{n}}{\partial t} = -\frac{2J_{oe}\overline{n}^2}{qWn_i^2} - \frac{\overline{n}}{\tau_b} \tag{76}$$

This equation is solved differentially in closed form. However, an easier derivation can be obtained using eq. (63), which only requires eq. (76) to be multiplied by -1/$\overline{n}$ and then using eq. (53) for τ$_b$ (for silicon band-to-band recombination can be ignored), which results in

$$-\frac{1}{\overline{n}} \frac{\partial n}{\partial t} = \frac{1}{\tau_{eff}} = \frac{2J_{oe}\overline{n}}{qn_i^2 W} + \frac{1}{\tau_{SRH}} + C_n \overline{n}^2 \tag{77}$$

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which is rearranged to extract J_{oe} from the PCD measurement

$$\left(\frac{1}{\tau_{eff}} - C_n \bar{n}^2\right) = \frac{2J_{oe}\bar{n}}{qn_i^2 W} + \frac{1}{\tau_{SRH}}$$ (78)

Equation (78) allows a plot between τ_{eff} and $\bar{n}$ (if Auger recombination is included in the effective lifetime), with the intercept equal to the bulk lifetime ($\tau_{SRH} \approx \tau_b$) and the slope of the line equal $2J_{oe}/qn_i^2 W$, which are all constants with the exception of J_{oe}. Under low-level injection (LLI), the effective surface recombination velocity can be extracted directly if the bulk dopant type and diffusion dopant type are the same and, again, both surfaces are similarly diffused. In addition, the bulk material cannot be intrinsic and the appropriate dark saturation component is known from a previous measurement (i.e., J_{oe} or J_{ob}) [24]. Mathematically, this is described (assuming a p-type substrate) as

$$J_{rec} = qnS_{eff} = J_{ob'}\frac{np}{n_i^2} = J_{ob'}\frac{\delta(\delta + N_A)}{n_i^2} \rightarrow S_{eff} = \frac{J_{ob'}(\delta + N_A)}{qn_i^2}$$ (79)

where the minority carrier (n) is equal to δ. A similar analysis works for n-type material as well. Carrier lifetime is an excellent gauge of solar cell performance capabilities. How long the average EHP survives before recombining allows for a better determination of the number of carriers that will be collected and used for actual power. However, forming the EHP is just the beginning of the journey for the charged carriers. Further analysis using Internal Quantum Efficiency methods adds insight into the problem areas limiting solar cell efficiency that cannot be detected during lifetime measurements because of the device structure having metal and ruining the conductance changes.

IQE

The internal quantum efficiency, IQE, of a solar cell is defined as the number of electron-hole pairs collected under short circuit current conditions for each photon that is absorbed into the device.

$$IQE(\lambda) = \frac{J(\lambda)}{q(1-R)F_{ph}(\lambda)} \tag{80}$$

where R is the reflectance of the solar cell in question, F_{ph} is the monochromatic photon flux density incident on the cell, and $J(\lambda)$ is the current density, which is a function of the absorption coefficient (which is a function of wavelength) described by the following equation.

$$J(\alpha) = qF_{ph}(1-R)\left(\frac{\alpha L_n}{\alpha^2 L_n^2 - 1}\right) \cdot \left[\frac{\left(\frac{SL_n}{D_n} + \alpha L_n\right) - e^{-\alpha x_j}\left[\frac{SL_n}{D_n}\cosh\left(\frac{x_j}{L_n}\right) + \sinh\left(\frac{x_j}{L_n}\right)\right]}{\left[\frac{SL_n}{D_n}\sinh\left(\frac{x_j}{L_n}\right) + \cosh\left(\frac{x_j}{L_n}\right)\right]} - \alpha L_n e^{-\alpha x_j}\right] \tag{81}$$

where x_j is the junction depth and α is the absorption coefficient. Using this technique to characterize the solar cell reveals very specific information such as emitter performance, bulk diffusion length, back surface recombination velocity (BSRV), and a more accurate current collection profile. By examining trouble areas on an IQE curve, one may be able to extract information about the problem causing the reduced performance, i.e., the BSRV, front surface recombination velocity, or bulk lifetime issues. An excellent example of this is demonstrated in the analysis of the defect responsible for light induced degradation of the bulk lifetime of solar grade Cz silicon wafers.

APPENDIX B

Process D -- Run Sheet

Clean

1. **Acid Texture Etch** samples in 2:5:15 (Hydrofluoric : Nitric : Acetic) for 60 seconds
2. DI water Rinse (30 seconds)
3. 1 minute HF (1:10 of HF:H_2O)
4. DI water Rinse (30 seconds)
5. 5 minutes HCl (1:1:1 of HCl:H_2O_2:H_2O)
6. DI water Rinse (30 seconds)
7. 1 minute HF (1:10 of HF:H_2O)
8. DI water Rinse (30 seconds)
9. 5 minutes Sulfuric (1:1:1 of H_2SO_4:H_2O_2:H_2O)
10. DI water Rinse (30 seconds)
11. 1 minute HF (1:10 of HF:H_2O)
12. DI water Rinse (30 seconds)
13. **Porous Silicon Etch** (6-12 seconds) in 200:1 of HF:HNO_3
14. DI water Rinse (30 seconds)

RTP anneal

1. Load sample into Heatpulse 610 RTP
2. Process Flow
    a. 10 second purge (N_2 only!!!!)
    b. 20^oC/s ramp to 400^oC (N_2 only!!!!)
    c. 30 second steady state 400^oC (N_2 only!!!!)
    d. 100^oC/s ramp to 725^oC (N_2 only!!!!)
    e. 100^oC/s cool down to 300^oC (N_2 only!!!!)

Diffusion

1. Screen-print Al (FX-53-038)
2. Belt dry--5 minute -; bake 200^oC
3. Prepare spin-on dopant (typically P509 from filmtronics)
    a. Place approximately 1 ml of dopant on center of wafer using a clean pippet
    b. 3000 rpm, max acceleration
    c. 15 seconds
    d. 15 minute bake in 215^oC oven
4. Load porous silicon etched wafer in RTP with Al BSF side down

5. Stack three pieces of broken 300 μm wafer (spacers) on top of porous silicon etched wafer in a triangle shape at the edges (for air-gap to allow diffusion)
6. Place source wafer directly on top of spacers facing the porous silicon etched surface
7. Diffuse by RTP
   a. 10 second purge N_2
   b. 20°C/s ramp to 400°C (N_2)
   c. 30 seconds 400°C (O_2) for burn out
   d. 100°C/s ramp to 880°C (O_2) keep oxygen on till max temp achieved then turn off!!
   e. 180 seconds 880°C (N_2)
   f. 1°C/s cool down to 800°C (N_2)
   g. 20°C/s cool down to 300°C (N_2)

Front Contacts

1. Screen-print Ag3349 paste from Ferro
2. Belt dry--5 minutes; bake 200°C

RTP Fire

1. Load porous silicon etched diffused cell into RTP with the Al-BSF side down
2. RTP Fire
   a. 10 second purge (N_2)
   b. 20°C/s ramp to 350°C (N_2)
   c. 30 seconds 350°C (O_2)
   d. 100°C/s ramp to 700°C (O_2)
   e. 1 second 700°C (O_2)
   f. 100°C/s cool down to 300°C (N_2)

Measure

1. Isolate
2. 15 minutes FGA 400°C (if necessary)
3. Measure I-V

******* Video of Process C is on the UCEP server labeled
\\uceperserver2\UCEP Videos\Porous Silicon Run *******

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