Operation of SiGe BiCMOS Technology Under Extreme Environments

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SUMMARY

"Extreme environment electronics" represents an important niche market and spans the operation of electronic components in surroundings lying outside the domain of conventional commercial, or even military specifications. Such extreme environments would include, for instance, operation to very low temperatures (e.g., to 77 K or even 4.2 K), operation to very high temperatures (e.g., to 200 °C or even 300 °C), and operation in a radiation-rich environment (e.g., space).

The suitability of SiGe BiCMOS technology for extreme environment electronics applications is assessed in this work, including: the high-temperature capability of SiGe HBTs; the effects of proton radiation on vertical SiGe HBTs fabricated on CMOS compatible thin-film SOI; stability constraints in epitaxial SiGe strained layers under radiation exposure; and low-temperature operation of bulk CMOS devices found in a SiGe BiCMOS platform.

The suitability of SiGe HBTs for use in high-temperature electronics applications is first investigated. SiGe HBTs are shown to exhibit sufficient current gain, frequency response, breakdown voltage, achieve acceptable device reliability, and improved low-frequency noise, at temperatures as high as 200-300°C. A comprehensive investigation of substrate bias effects on device performance, thermal properties, and reliability of vertical SiGe HBTs fabricated on CMOS-compatible, thin-film SOI, is presented. The impact of 63 MeV protons on these vertical SiGe HBTs fabricated on a CMOS-compatible SOI is then investigated. The results show that proton irradiation creates G/R trap centers in SOI SiGe HBTs, creating positive charge at the buried oxide interface, effectively delaying the onset of the Kirk effect at high current density, which increases the frequency response of SOI SiGe HBTs following radiation. The thermodynamic stability of device-relevant epitaxial SiGe strained layers under proton irradiation is also investigated using x-ray diffraction techniques. Irradiation with 63 MeV protons is found to introduce no significant microdefects into the SiGe thin films, regardless of the starting stability condition of the SiGe film, and thus does not appear to be an issue for the use of SiGe HBT technology in emerging space systems. CMOS device reliability for emerging cryogenic space electronics applications is also assessed. CMOS device performance

improves with cooling, with higher carrier mobility, better subthreshold swing, and higher current drive at low temperatures. However, CMOS device reliability becomes worse at decreased temperatures due to aggravated hot-carrier effects. The device lifetime is found to be a strong function of gate length, suggesting that design tradeoffs are inevitable. Interface state generation is the dominant limiting reliability factor, regardless of the device geometry and operating temperature for the CMOS technology considered.

Details of this dissertation can be found in the following refereed publications:

1. High-Temperature (to 300°C) Characteristics of SiGe HBTs (Chapter II, also published in [1]).

2. Substrate Bias Effects in Vertical SiGe HBTs Fabricated on CMOS-Compatible Thin Film SOI (Chapter III, also published in [2]).

3. Proton Radiation Effects in Vertical SiGe HBTs Fabricated on CMOS-Compatible SOI (Chapter IV, also published in [3]).

4. The Effects of Radiation Exposure and Thermal Annealing on Stability Constraints in Epitaxial SiGe Strained Layers (Chapter V, also published in [4]).

5. CMOS Device Reliability for Emerging Cryogenic Space Electronics Applications (Chapter VI, also published in [5]).

CHAPTER I

INTRODUCTION

1.1 Extreme Environment Electronics

Though the market volume for a niche application such as "extreme environment electronics" is small, the end users in this market are nevertheless very important, and the value-added to the electronic components can be substantial. Extreme environment electronics can be loosely defined as operation of electronic components under adverse ambient conditions that lie outside the domain of commercial or even military specifications. Such extreme environments would include regions with temperatures either above or below the standard mil-spec -55 °C to 125 °C temperature range (0 °C to 85 °C for commercial applications), a radiation intense environment such as space, a high-vibration (shock) environment, a high- (or low-) pressure environment, and even a caustic or chemically corrosive environment (e.g., inside the human body). For the purposes of this work, we confine ourselves to the three most important extreme environment electronics scenarios: 1) operation at cryogenic temperatures (e.g., to 77 K); 2) operation at very high temperatures (e.g., to 300 °C); and 3) operation in a radiation-rich environment (e.g., space).

The fabrication of electronic devices and systems capable of operating at high temperatures represents an important niche industry and embodies applications in automobiles, heavy vehicles, power switching, engine electronics, aerospace (e.g., the "all-electric aircraft"), shipping, oil well logging, nuclear power, planetary space missions, and radar systems [6]. In consumer applications, however, typical operating temperatures range from -40°C to +85°C and the "wider" military specification is still only -55°C to +125°C. The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors (ITRS) only extends the ambient operating temperature for integrated circuits in harsh environments to -40 °C to +150 °C by the year 2010. One near-term driving force for developing high-temperature electronics is emerging applications in the area of automotive/vehicle electronics and in advanced aircraft systems. As an example, Table 1 lists the maximum ambient operating temperatures associated with the different automotive

Table 1: Automotive maximum ambient temperatures.

Under-hood	100 - 125°C	On Wheel	150 - 250°C
On-Engine	150 - 200°C	Cylinder	200 - 300°C
In-Transmission	150 - 175°C	Exhaust	Up to 850°C

environments.

At present, cryogenic electronics represents a small industry with niche applications such as high-sensitivity cooled sensors and detectors, semiconductor-superconductor hybrid systems, space electronics, and perhaps eventually cryogenic computer systems.

The electronic systems operated in space environment experience persistent exposure to large and potentially lethal fluxes of high-energy protons, neutrons, electrons, gamma rays, x-rays, and cosmic rays (high-energy heavy ions). A typical orbital satellite is expected to be exposed to fluences of the order of 10^{10}-10^{12} cm^{-2} of protons and 10-1,000 krad (Si) of gamma radiation during its flight lifetime (typically 10 years). With upward trend in operating speeds, space electronics are also becoming increasingly susceptible to single-event effects caused by cosmic rays and other high-energy particles. Until now there has not been a serious threat to terrestrial electronics from radiation exposure. But continued down-scaling of device dimensions has made the effects of terrestrial radiation non-negligible. For instance, the effects of neutron radiation has become a critical reliability issue in memory ICs for manufacturers of consumer electronics. Using electronics in both extreme temperatures (high/low) and in high radiation environments further degrades system performance and overall system reliability. On the moon, for example, in addition to the temperature varying from -230°C to +120°C, there is a high level of radiation present.

The goal of this dissertation is to help assess SiGe BiCMOS technology for potential use in such extreme environment applications.

1.2 The SiGe HBT Technology

1.2.1 The development of SiGe technology

Modern SiGe BiCMOS technology owes its biggest debt to Herbert Kroemer, who put forward the theoretical foundation for the heterojunction transistor (HBT) in 1957 [7]. Kroemer postulated

that with alloy grading, the energy bandgap could be altered such that the electrostatic force could be overcome by a "quasi-electric" field, thereby enhancing carrier transport. In a graded-base SiGe HBT, there is a Ge concentration gradient across the base, with a higher Ge content at the collector side. As such, the band structure is altered by the alloy grading of Ge and a corresponding quasi-electric field aids electron transport across the base. The primary advantages of the SiGe technology include: a) it is 100% compatible with existing Si technology; b) it provides significant speed enhancement over conventional Si bipolar transistors; c) and it allows further performance enhancement by scaling.

One of the most challenging tasks in the early development of SiGe HBTs was to fabricate a very thin, high-quality SiGe base layer while maintaining good control over the Ge fraction, boron doping, and layer thickness. By the early 1980s, ion-implanted base bipolar technology was widely used. This technology, however, has poor base thickness control because of the boron-channeling tail and transient enhanced diffusion of boron. Dopant diffusion and strained film relaxation are thermally activated processes, and thus their rate of change depends exponentially on temperature. Low-temperature epitaxy (LTE), therefore, is a tempting choice for fabricating epitaxial layers with a highly controllable dopant and alloy content. The most important event in the early development of silicon LTE was the observation of the dewetting of silicon wafers after hydrofluoric (HF) etching. This conflicted with the conventional opinion of the day that freshly etched silicon immediately formed a thin layer of native oxide when exposed to air, which wet readily. Surface science studies found that HF etching provided a passivation layer consisting of hydrogen-terminated silicon bonds across the silicon surface. This passivation layer reduced silicon's oxidation rate by more than 13 orders of magnitude. Hydrogen-passivated wafers could thus be exposed to a silicon-source gas such as silane, and there would be no silicon growth until the wafers were heated to a high enough temperature to disrobe the hydrogen passivation layer. Within a certain temperature range, silane decomposes and not only incorporates silicon into the crystal, but also replenishes the hydrogen-passivation layer at a higher rate than its desorption rate. The surface is protected from ambient oxygen contamination during the epilayer growth, and films of extraordinarily high quality can be produced. An ultrahigh vacuum/chemical vapor deposition (UHV/CVD) LTE technique was ultimately developed to provide the basis for the systematic preparation of the layers required to

implement the SiGe epitaxial base transistor technology [8]. This result helped launch the field of practical SiGe technologies.

1.2.2 SiGe HBT device physics

To fully appreciate many of the constraints faced in the operation of SiGe HBTs in extreme environments, particularly as a function of technology scaling, it is useful to have good knowledge of the physics behind the operation of these devices, and particularly how their operation differs from a similarly constructed Si BJT. The introduction of Ge into the base region of a bipolar transistor has two tangible *dc* consequences: 1) The potential barrier to injection of electrons from emitter into the base is decreased. Intuitively, this will yield exponentially more electron injection for the same applied V_{BE}, translating into higher collector current and hence higher current gain in the device, provided the base current remains unchanged. Of great practical importance of introduction of Ge is the effective decoupling of the base doping from the current gain, thereby providing device engineers with much greater design flexibility than in Si BJTs. 2) The presence of a finite Ge content in the CB junction positively influences the output conductance of the transistor, yielding higher Early voltage (V_A). Figure 1 shows a cross-section of a first-generation SiGe HBT manufactured by IBM (and used in this study). The Ge profile was grown in the base region to improve the device performance (e.g., f_T, f_{max}, noise, etc.).

If we consider a comparably constructed SiGe HBT and Si BJT with identical emitter contact technology, and further assume that the Ge profile on the EB side of the neutral base does not extend into the emitter enough to change the base current density, the theoretical expectations are that for a comparably constructed SiGe HBT and Si BJT, the J_B should be comparable between the two devices, while J_C at fixed V_{BE} should be enhanced for the SiGe HBT. This expectation is confirmed by experimental data plotted in Figure 2.

With J_B being comparable, we note that the ratio of the current gains of identically constructed SiGe HBT and a Si BJT can be written as

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \frac{J_{C,SiGe}}{J_{C,Si}} \tag{1}$$

The output conductance ratio (as reflected equivalently by the Early voltage ratio) of a SiGe HBT and a Si BJT exponentially depends on the amount of bandgap grading across the base divided by

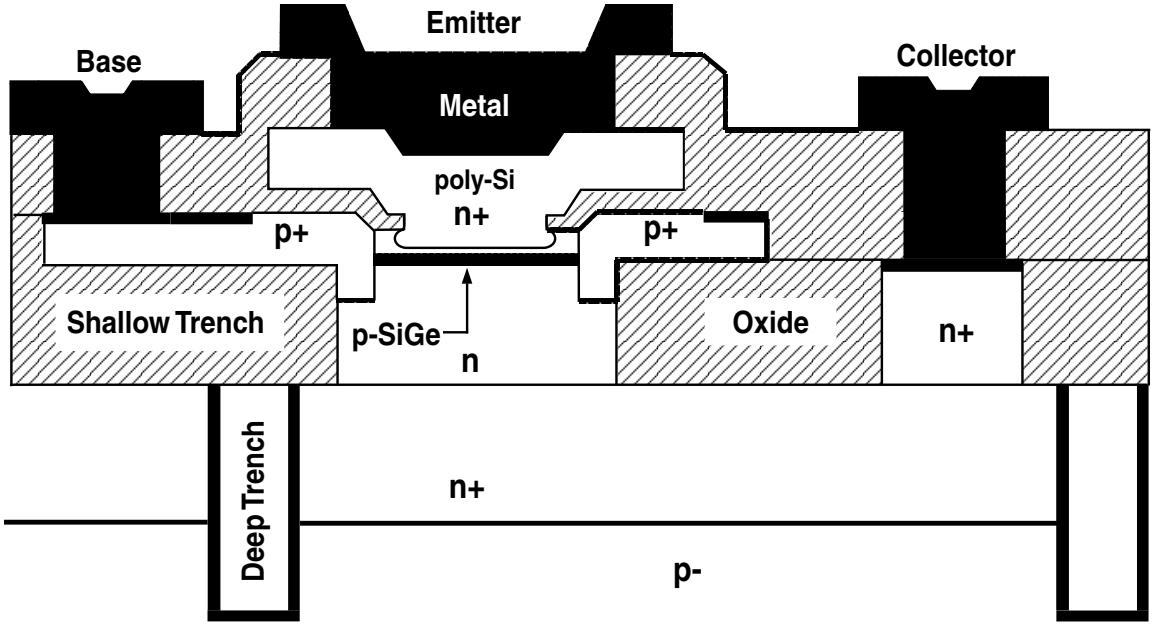

Figure 1: Cross-section of a first generation SiGe HBT [9].

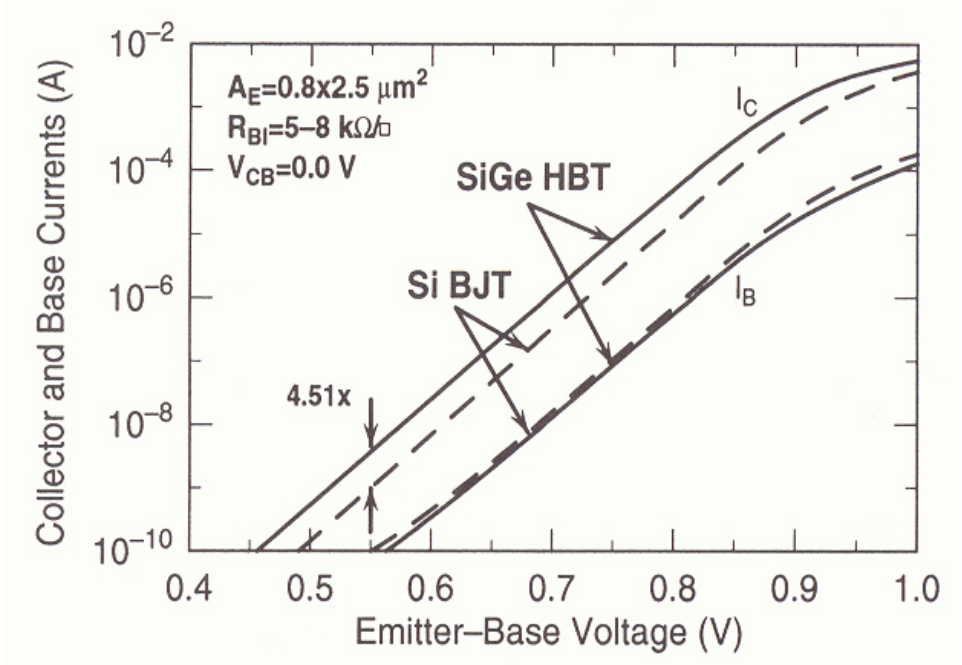

Figure 2: Comparison of the current-voltage characteristics of a comparably constructed SiGe HBT and Si BJT. [10]

kT

$$\frac{V_{A,SiGe}}{V_{A,Si}} = e^{\frac{\triangle E_{g,Ge(grade)}}{kT}} \left[\frac{1 - e^{-\triangle E_{g,Ge(grade)}/kT}}{\triangle E_{g,Ge(grade)}/kT} \right] \tag{2}$$

The dependence of SiGe HBT device performance on temperature is an important issue, especially when a SiGe HBT is operating under extremely high/low temperatures. A multitude bipolar parameters are affected by temperature variation. The current gain, for example, is a function of both the emitter efficiency and base transport factor. The emitter efficiency in turn depends on the ratio of the carrier densities, diffusion constants, and widths of the emitter and base regions. The carrier densities are linked to the doping densities. Barring incomplete ionization, which can be highly temperature dependent, the carrier densities are independent of temperature as long as the intrinsic carrier density does not exceed the doping density in either region. The widths of the base and emitter regions are only weakly temperature dependent. Carrier mobility is expected to be only moderately temperature dependent since the base and emitter doping is fairly high in modern devices. The base transport on the other hand is more likely to be temperature dependent since it is a function of the product of the diffusion constant and the carrier lifetime. The diffusion constant in turn equals the product of the thermal voltage and the minority carrier mobility in the base. The recombination lifetime depends on the thermal velocity. The result is therefore a moderate dependence on temperature. Typically the base transport reduces with temperature, primarily because the mobility and recombination lifetime are reduced with increasing temperature. The major contribution to temperature dependence in Si BJT is from factors associated with heavy doping effects [11]. The single impurity energy level formed due to the introduction of "moderate" amounts of dopant atoms, splits into an impurity band when doping levels are increased dramatically, which in turn causes heavy doping effects to take shape. In addition, an energy band "tail" is formed in the density-of-states. In practical device analysis, to account for heavy doping effects in the transport equations while maintaining their conventional form, the term "apparent bandgap narrowing", $\triangle E_g^{app}$, is introduced [12].

$$n_{i,heavy\_doping}^2 = N_C N_V e^{-\frac{E_g - \triangle E_g^{app}}{kT}} = n_{i0}^2 e^{\frac{\triangle E_g^{app}}{kT}} \tag{3}$$

where n_{i0} is the intrinsic carrier concentration. Note, however, that $\triangle E_g^{app}$ does not necessarily represent the physical change in the bandgap with heavy doping. Rather, it is a "phenomenological" parameter. Generally, for common dopants in silicon, $\triangle E_g^{app}$ can be estimated to be 0 and 100 meV for doping densities of 10^{17} and 10^{20} cm^{-3}, respectively, and can be linearly interpolated between

these points. As the emitter is heavily doped, bandgap narrowing introduced by emitter dominates

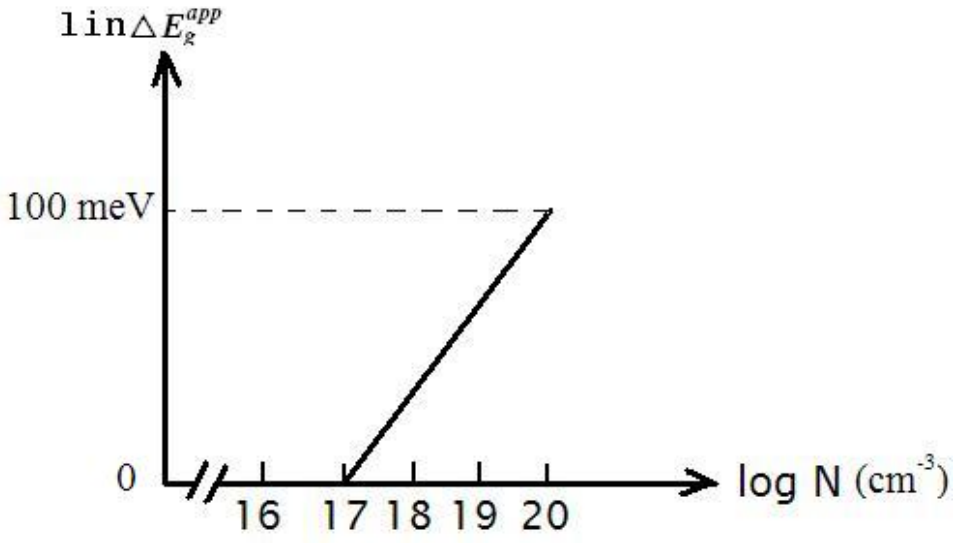

Figure 3: Apparent bandgap narrowing at various doping concentrations.

the temperature dependence of current gain in modern Si BJTs. The thermal dependence of the current gain can be written as

$$\beta_{Si}(T) \propto e^{\frac{\triangle Eg_{base}^{app} - \triangle Eg_{emitter}^{app}}{kT}} \propto e^{-\frac{E_\beta}{kT}} \tag{4}$$

Since the emitter is much more heavily doped than the base, the net bandgap narrowing couples into the β expression of Si BJT in an exponentially decreasing form 4, and hence the β of Si BJT deceases dramatically with cooling.

The heavy doping effects have a similar effect on the temperature dependence of current gain in SiGe HBTs. However, the reduction in base bandgap in a SiGe HBT lowers the potential barrier to electron injection into the base and thus exponentially increases the number of electrons injected from emitter to base for fixed bias. The result from a device terminal viewpoint is an increase in J_C for fixed V_{BE} compared to a Si BJT. Thus β increases for a SiGe HBT according to Equation **??**. The temperature dependence of β can be expressed as

$$\beta_{SiGe}(T) \propto e^{-E_\beta/kT} \times \frac{\Delta E_{g,Ge}(grade)}{kT} \times e^{\Delta E_{g,Ge}(0)/kT}, \tag{5}$$

where $\Delta E_{g,Ge}(grade)$ is the grading factor associated with the change in Ge content across the neutral base, and $\Delta E_{g,Ge}(0)$ is the Ge induced bandgap narrowing at base-emitter boundary. The

Ge induced bandgap narrowing is typically 75 meV for every 10% of Ge. For a typical linearly graded SiGe HBT, $\triangle E_{g,\,Ge}(0) - E_{\beta} > 0$. Thus, unlike Si BJT, for a SiGe HBT the β will naturally increase with cooling. From at least a theoretical standpoint, this clearly bodes well for the operation of SiGe HBTs at cryogenic temperatures, but also raises questions with respect to operation at elevated temperatures (given that β decreases as the temperatures increases).

1.2.3 SiGe HBT on SOI

From a space electronics perspective, SiGe technology offers an advantageous built-in total dose tolerance [13], but on the other hand has proven to be susceptible to single event upset [14]. Clearly, placing SiGe HBTs on SOI, particularly thin film CMOS-compatible SOI, is an attractive option in the context of SEU for space applications of SiGe circuits.

SOI technology has matured over the past 15 years to become a production-worthy process suitable for advanced CMOS manufacturing [15]. The most useful SOI properties are its ability to provide total electrical isolation and to reduce active semiconductor volume. The thin oxide-isolated Si layer allows us to shrink device geometries, incorporate high voltage operation capability, improve soft error immunity, and eliminate latch up. Today, many wireless and communication applications place stringent demands on both bipolar transistors for RF/analog functions and on CMOS transistors low power digital functions, and often want them available on the same chip. Hence, BiCMOS is the preferred technology platform for realizing these circuits. The challenge of achieving SOI BiCMOS integration arises from the fundamental differences in device architecture between SiGe HBT and CMOS transistors, in that the bipolar transistors need thick subcollectors to maintain low collector resistance, which are incompatible with thin-film SOI CMOS. Past approaches to SOI BiCMOS integration either used a thick silicon layer on a bonded SOI substrate to accommodate the vertical bipolar transistors or used lateral bipolar transistors on thin silicon film SOI, both of which can result in significant loss of performance for the HBT. Recently, a novel vertical bipolar transistor suitable for integration on CMOS-compatible SOI has been proposed, and npn transistors with a SiGe base were demonstrated on 0.12μm SOI [16]. Figure 4 shows a cross-section of a vertical SiGe HBT on SOI manufactured by IBM.

Although bulk silicon devices can be operated at high temperature with marginal success (at

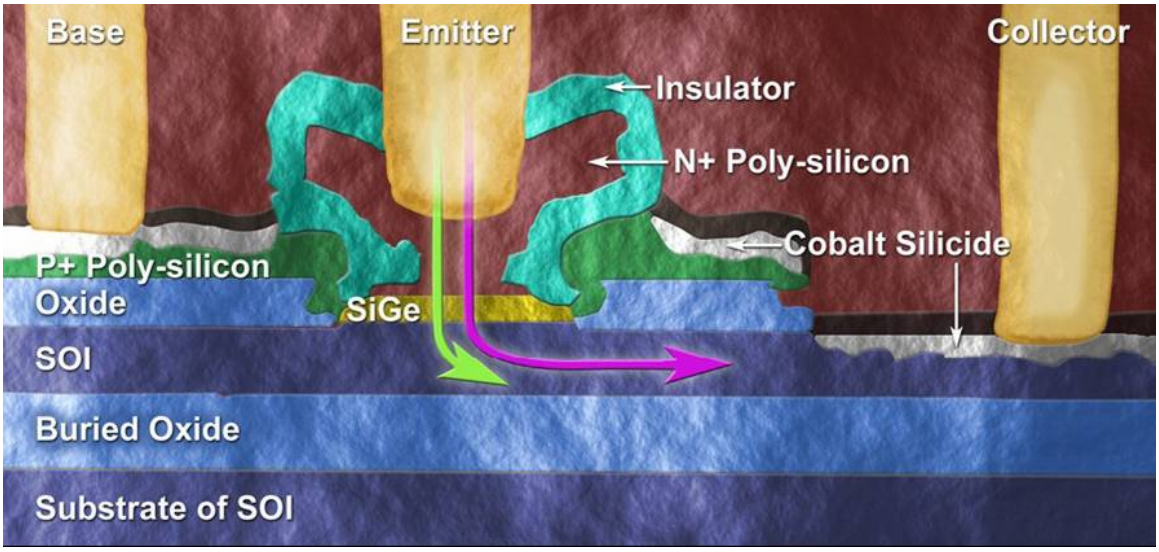

Figure 4: Cross-section of vertical a SiGe HBT on SOI [17].

least to say 150°C), parasitic leakages often dominate, requiring expensive process optimization. In SOI technology, however, the buried oxide helps reduce the substrate leakage significantly and provides RF noise isolation between digital and RF/analog components. SOI is presently the most suitable process for constructing electronic circuits capable of operating at temperatures up to and beyond 300°C.

1.3 Extreme environment electronics applications

1.3.1 Traditional solutions for extreme environment electronics

Niche applications such as extreme environments can often place much more demanding constraints on the electronic components building blocks than required to be met by commercial ICs, and hence often call for significant modifications to the standard foundry IC processes, at a very large and highly undesirable cost. For example, the surprisingly extreme temperature conditions on the lunar surface (at worst case, reaching down to -230 °C in the polar shadows and up to +120°C is the sunlight) preclude the use of conventional terrestrial electronics for sensing, actuation, and control. Unmanned lunar missions necessarily combine mobility on the surface (i.e., on a rover) with sensing functions, electronics, and motors/actuators for controllers on the rover. For instance, a typical lunar mission might include a mobile mineralogy station for mapping in-situ resources. The sensor/actuator networks on such a lunar rover would provide a distributed system to monitor

the health and performance of the rover, and to sense the environment for scientific exploration or to act on the environment, for example by using a drill to obtain a soil sample for analysis. To facilitate these operations, the rover has networks that consist of remote "intelligent" nodes. The remote electronics unit (REU) typically defines these remote intelligent nodes. These remote electronics nodes in principle need to be distributed over the entire vehicle, and hence when located within protective "warm boxes," the current methodology for housing on-board electronics, their efficiency is compromised. This need for protective electronic "warm boxes" critically limits the designer's ability to create a truly distributed, modular electronics system for lunar rovers resulting in excessive point-to-point wiring, increased system weight and complexity, lack of modularity, and an overall reduction in system reliability.

1.3.2 SiGe technology for extreme environment electronics

There are currently two recent but rapidly growing thrusts within the space electronics community: 1) the use of commercial-off-the-shelf (COTS) parts whenever possible for space-borne systems as a cost-saving measure and 2) the use of SoC integration to lower chip counts and system costs, as well as to simplify packaging and to lower total system launch weight. The "holy grail" in the realm of space electronics can thus be viewed as a conventional terrestrial IC technology with a SoC capability, which is also radiation-hard as fabricated, without requiring any additional process modifications or layout changes. As will be argued in this dissertation, SiGe HBT technology embodies great potential to simultaneously satisfy all three extreme environment applications, potentially with little or no process modification, providing compelling cost advantage.

Bandgap engineering generally has a positive influence on the low-temperature characteristics of bipolar transistors [10]. SiGe HBTs operate very well, in fact, in the cryogenic environment (e.g., liquid nitrogen temperature 77.3 K or -196 °C), an operational regime traditionally forbidden for Si BJTs.

With their low cost and high processing maturity, silicon-based technologies can generally dominate any market for which they are technically feasible. The high-temperature capability of Si, however, is often under-appreciated because of its relatively small bandgap. Early demonstrations have shown that for a particular SiGe HBT, the off-state leakage remains below 10 nA at 275°C,

with a respectable current gain of greater than 200 across the useful range of bias currents [10]. There is thus no fundamental reason why SiGe HBTs cannot satisfy this important emerging niche application of high-temperature electronics.

SiGe HBTs have demonstrated to be inherently radiation hard as fabricated. The observed current gain degradation of SiGe HBTs for gamma rays [18], neutrons [19], and protons [20] is much smaller than that found in conventional Si BJTs (even radiation-hardened versions). A comparison of the radiation tolerance of these SiGe HBTs to epi-base Si BJT's from the same fabrication run suggest that the inherent radiation hardness of this technology is due to its special device structure [10]. From a radiation immunity viewpoint, this SiGe HBT structure has several intrinsic advantages: 1) the EB spacer is very thin and composed of a oxide-nitride composite; 2) the extrinsic base doping under the EB spacer is very high, effectively confining any ionization damage to that region; 3) the active device region is very thin (< 200 nm) and, hence, the total volume exposed to particle displacement damage is minimal; and 4) the deep- and shallow-trench isolation minimizes the exposure of oxides that can contribute to junction leakage.

1.4 Stability constraints for SiGe HBTs under extreme environments

The SiGe films used in SiGe HBTs actually have a three-layer composite structure: a thin, undoped Si buffer layer; the actual boron-doped SiGe active base layer; and a thin, undoped Si cap layer. The Si buffer layer is used to start the growth process off on the right foot, and serves two purposes. First, the Si buffer layer helps to ensure that a pristine SiGe epitaxial growth interface is preserved between the original Si substrate, which was grown by a high-temperature Si epitaxy process, and the succeeding SiGe strained layer that will be grown by a more difficult low-temperature epitaxy process. Maintaining a contaminant-free growth interface with perfect crystallinity is essential for obtaining device-quality SiGe films. Second, this Si buffer layer also frequently plays a role in device design for extreme environments, since it allows the incorporation of intrinsic layers (i-layers) to be easily embedded in the collector-base junction and can be used to decrease the junction field, and aid in both breakdown voltage and parasitic junction leakage tailoring.

The active SiGe layer has a position-varying Ge composition, and an embedded boron-doping spike, typically deposited as a boron box profile for a given integrated base charge. The SiGe layer

forms the active region of the bandgap-engineered device, and the specific shape, thickness, and placement of the Ge profile with respect to the boron base profile will in large measure determine the resultant dc and ac performance of the transistor.

Finally, the Si cap layer serves four purposes. First, it provides a Si termination to the SiGe composite. This is particularly important, since most SiGe HBT fabrication approaches involve some form of oxidation step to form the emitter-base spacer used in self-alignment, and SiGe does not oxidize well. Second, the Si cap provides additional space to allow the modest out-diffusion of the boron base profile during processing, while at the same time providing room for the emitter out-diffusion. Third, as with the Si buffer layer, a Si cap layer can be used to introduce an active -layer into the emitter-base junction to lower the junction electric field and thereby reduce the parasitic EB tunneling current, which typically limits the base current ideality at low-injection and hence degrades device reliability. Finally, an unintentional but nonetheless important consequence of having this Si cap layer is that it helps improve the overall stability of the film, increasing the thickness and Ge fraction of the layer to levels higher than might otherwise be expected.

The strain "relaxation" (resulting in misfit dislocations and defects) of SiGe epitaxial layers can result in a break in crystallinity across the growth interface, which is clearly unacceptable for high-yielding IC applications. The SiGe layer thickness is a key variable in SiGe HBT device design. The critical thickness is defined as the maximum film thickness for obtaining pseudomorphic growth post-fabrication. The force balance [21] and the energy minimization [22] are the two most common approaches to determining the equilibrium-critical thickness of a coherently strained layer structure. A much-cited equilibrium model for buried SiGe strained layers has been introduced to show excellent agreement between theory and experiment for both CVD and MBE grown films, which applies the existing force-balance theory with a proper consideration for the effects of the Si cap layer [23]. The theory predicts that during strained-layer epitaxy, the formation of a network of misfit dislocation at the substrate/strained-layer interface becomes energetically favorable to further commensurate growth when the thickness exceeds a critical value. It is generally agreed, however, that SiGe films can be grown by certain low-temperature techniques to thicknesses far exceeding the theoretical critical thickness without misfit dislocations, e.g., a technique called the ultrahigh-vacuum chemical vapor deposition (UHVCVD) low-temperature epitaxy (LTE). Using

this approach, thin films can be grown to several times the theoretical critical thickness without lattice relaxation. Furthermore, the temperature dependence of the Peierls force, which is opposite to the dislocation glide, leads to the thermodynamic factor involved in determining SiGe thin-film stability. Since standard Si devices and circuit fabrication processes undergo several unavoidable high-temperature steps such as oxidation and annealing, a thin film that is metastable when as-grown may relax during the subsequent device fabrication. Two fundamental materials questions remain unanswered for the intrinsic SiGe base layer in the context of extreme environments: how and to what extent is the SiGe thin-film stability affected by proton irradiation? How does the high-temperature annealing affect the film stability?

1.5 The low-temperature operation of CMOS devices

While the large power dissipation associated with conventional bipolar digital circuit families such as emitter coupled logic (ECL) would likely preclude their widespread use in cooling-constrained cryogenic systems, the combination of cooled, low-power, scaled Si CMOS with SiGe HBTs offering excellent frequency response, low noise performance, radiation hardness, and excellent analog properties represents a unique opportunity for the use of SiGe HBT BiCMOS technology in cryogenic systems.

One new and interesting cryogenic application involves NASA's recent presidentially-mandated refocus on Lunar exploration. The development of modular, expandable, and reconfigurable human and robotics systems for lunar missions clearly requires electronic components and integrated packaged electronics modules that are capable of operating robustly without external thermal control. At present SiGe BiCMOS technology is being actively explored for future lunar electronics needs requiring no external thermal control. Clearly, any device technology for lunar missions must be proven to be both robust and "reliable." That is, under typical circuit operating conditions, the circuits and most importantly the systems constructed from those circuits must not wear out or degrade to a level at which they will fail "on the field" during the functional life of the system, irrespective of the operating temperatures. In this work we explore the reliability issues associated with the operation of CMOS devices from a SiGe BiCMOS platform, and in particular with operation down to cryogenic temperatures.

1.6 Scope of the Thesis

Given this highly encouraging picture of the maturation and deployment of SiGe ICs in a variety of commercial communications applications, and its emerging pervasiveness in the electronics industry as a whole, it is very logical to wonder if the scope for use of SiGe technology can be extended to support a variety of extreme environment electronics applications. There has been significant recent research effort devoted to investigate the cryogenic capabilities and radiation tolerance of SiGe HBT bulk technology [13]. Much remains to be done, however, if SiGe BiCMOS circuits is to be deployed in real systems to be operated in extreme environments. Three different devices types, namely, bulk SiGe HBT, SiGe HBT on SOI, and Si CMOS, are assessed for such critical extreme environment applications in this work. The corresponding device degradation mechanisms and device physics are also investigated. Furthermore, a study on the stability constraints in SiGe thin films is also presented. The topical scope of this dissertation is summarized in Table 2.

Table 2: Scope of the research work of this thesis.

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-	High T	Low T	Radiation	Device Physics	Reliability
Bulk SiGe HBT	x	-	-	x	x
SOI SiGe HBT	-	-	x	x	x
Si CMOS	-	x	-	x	x
SiGe Thin Films	x	-	x	-	x

CHAPTER II

ON THE HIGH-TEMPERATURE (TO 300°C) CHARACTERISTICS OF SIGE HBTS

2.1 Motivation for this work

The high-temperature (to 300°C) operation of electronic devices and systems represents an important niche industry, and embodies applications in automobiles, heavy vehicles, power switching, engine electronics, aerospace (e.g., the "all electric aircraft"), shipping, oil well logging, nuclear power, planetary space missions, and radar systems [6]. At present, the device technologies deployed for such applications typically include SOI CMOS, GaAs, and SiC. Conventional Si CMOS and Si BJTs are typically limited to operating temperature below 125°C due to substrate leakage and reliability concerns, unless extensive (costly) modification to the device technologies is performed.

SiGe HBT BiCMOS technology has recently emerged as an important platform for a vast array of analog, digital, RF, and microwave applications. It is well known that the bandgap engineering employed in the design of SiGe HBTs generally favors their operation at cryogenic temperatures, while, conversely, producing degradation in device performance at elevated temperatures. As such, the applicability of SiGe HBTs to emerging high-temperature electronics applications has to date not been seriously contemplated. In the present work, we present a comprehensive investigation of the high-temperature operation of SiGe HBTs, and demonstrate that, contrary to popular opinion, SiGe HBTs are potentially well-suited for many electronics applications operating at temperatures as high as 300°C [25].

2.2 Device technology and experiments

The SiGe HBTs used in this investigation are based on a commercial SiGe HBT BiCMOS technology which integrates 0.20 μm, 1.8 V BV_{CEO}, 120 GHz f_T SiGe HBTs (henceforth "high-performance"), 4.3 V BV_{CEO}, 35 GHz f_T SiGe HBTs ("high-breakdown"), together with 0.18 μm, 1.8 V Si CMOS devices [26]. This SiGe technology incorporates deep and shallow trench isolation

and copper metalization (with a thick top aluminum metal), but was not optimized in any way for high temperature operation. Both types of SiGe HBTs were measured on-wafer using an Agilent 4155C (for *dc*), an Agilent 8510C VNA (for *ac*), and custom 1/f and reliability test systems, on probe stations capable of operating from 20 to 300°C (for *dc*), and 20 to 200°C (for *ac*).

2.3 dc characteristics

The Gummel characteristics of the high-performance SiGe HBTs at 25, 150, and 300°C are shown in Figure 5.

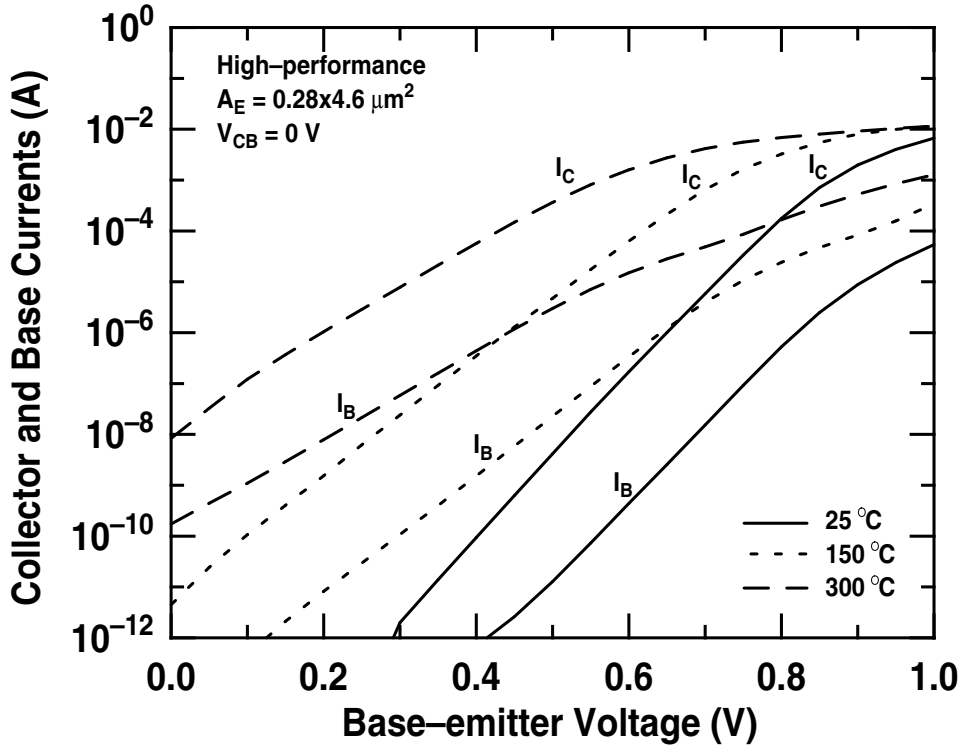

Figure 5: Forward-mode Gummel characteristics as a function of temperature.

The turn-on voltage decreases as the temperatures increases, as expected, due to the decrease in the emitter-base built-in potential, which is driven by the changes in the intrinsic carrier density. Observe, however, that the device remains ideal to 300°C, with a current gain above 100 and higher current drive capability than at room temperature, suggesting that the impact of high temperatures on the carrier mobility, and hence series resistances, is not a serious factor. Clearly,

minority carrier generation in the collector-substrate junction, and the consequent parasitic leakage, is a concern for high temperature applications. Figure 6 shows the temperature dependence of collector-substrate junction leakage. The collector-substrate junction leakage current is generally dominated by space-charge region generation-recombination (G/R) leakage ($I_{gen} \propto n_i$(T)) over the range 25 to T_{tran}°C, and by band-to-band thermal generation ($I_{diff} \propto n_i^2(T)$) above T_{tran}°C [27]. The collector-substrate leakage at 25°C is less than the smallest detectable current of the measurement system (< 1 pA) and hence negligible in practical circuit applications. It can be seen from Figure 6 that T_{tran}°C is about 135°C for this SiGe technology.

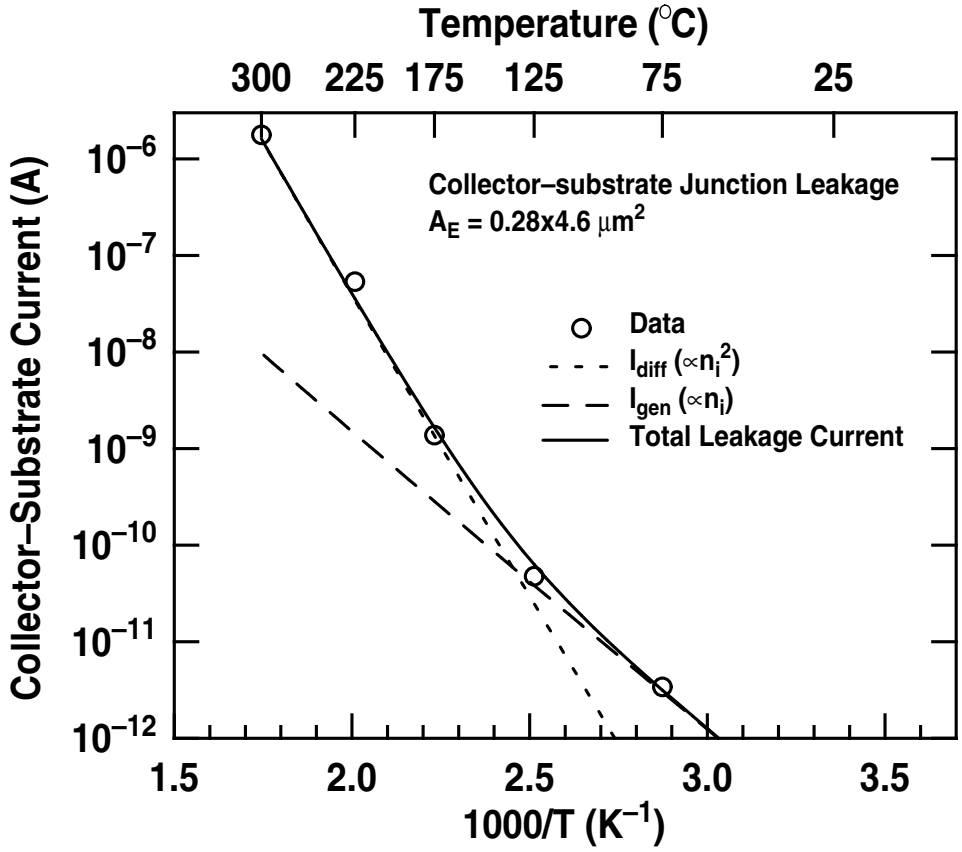

Figure 6: Collector-substrate junction leakage as a function of temperature when collector-substrate voltage is fixed at 1 V.

Figure 7 shows the explicit impact of substrate leakage on the Gummel characteristics at 300°C. Observe from Figure 7 that while the off-state leakage is 1.6 μA at 300°C at $V_{CB} = 1V$, and thus might be of potential concern for certain analog circuits biased at very low currents for high g_m, there remains over 4 orders of magnitude of useful bias range in this device at 300°C. Observe that

at high V_{BE} (> 0.7V) collector current increases and base current decreases as V_{CB} increases from 0 to 1V, due to the avalanche multiplication effect. At the same time, as the floating substrate is grounded, the collector current increases due to the collector-substrate leakage, and the base current also increases through the parasitic pnp (base-collector-substrate) transistor.

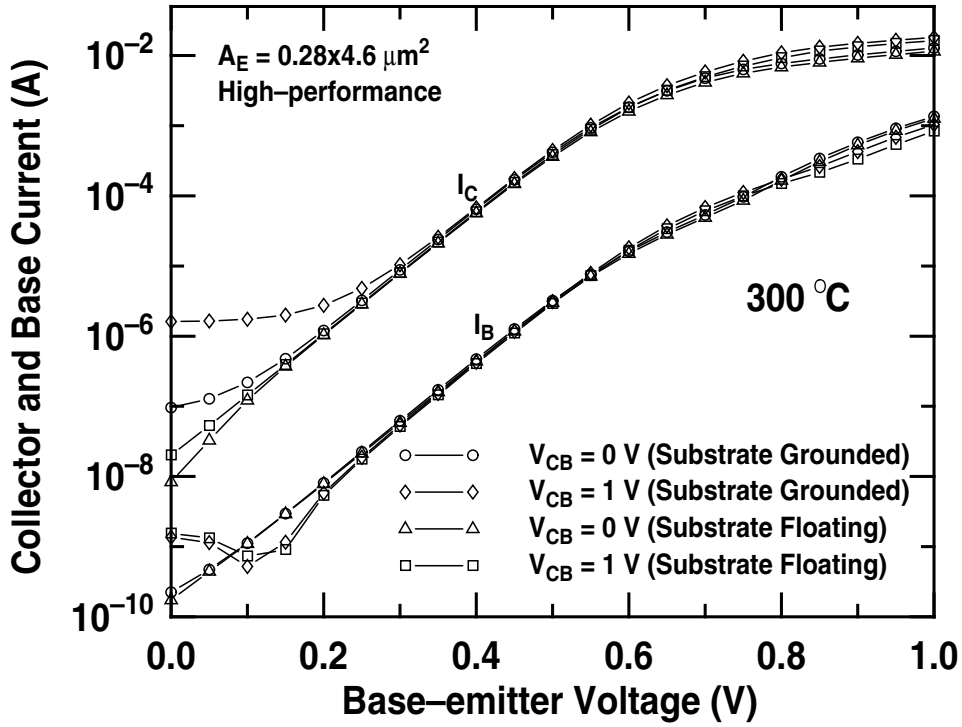

Figure 7: Gummel characteristics at 300°C with both floating and grounded substrate conditions.

The current gain as a function of collector current at 25, 150, and 300°C for both the high-performance and the high-breakdown transistors is shown in Figure 8. The shapes of the β versus I_C for high-performance and high-breakdown SiGe HBTs are profoundly different at high I_C. β for high-breakdown devices decreases rapidly at I_C close to 1 mA due to the Kirk effect and heterojunction barrier effects (HBE) [28]. The higher collector doping level in the high-performance SiGe HBTs delays the onset of the kirk effect, and hence HBE. Observe that as the temperature increases, the HBE effect in high-breakdown HBTs becomes less important due to the thermally-activated nature of HBE [29]. This provides additional design freedom regarding the Kirk effect/HBE at high temperatures compared to room temperature applications, which is clearly good news for high-temperature applications.

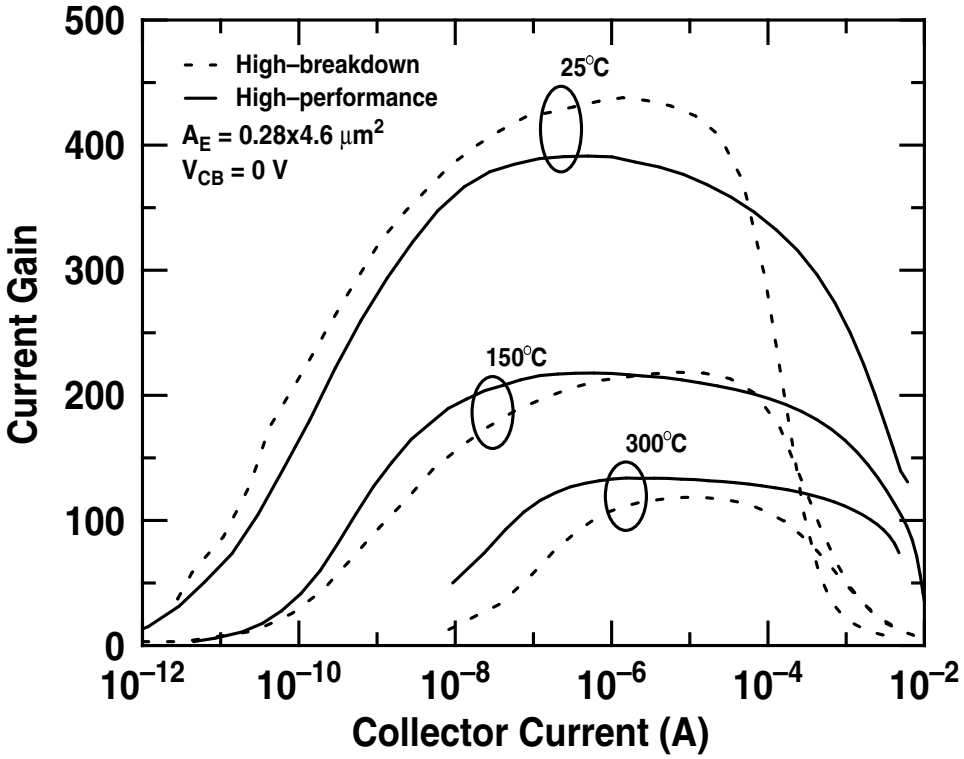

Figure 8: Current gain as a function of collector current at 25, 150 and 300°C.

Figure 9 shows that the peak β decreases as temperature increases, as expected. The β of a SiGe HBT can be described by

$$\beta \propto e^{\Delta E_{gb}^{app}/kT} \times \frac{\Delta E_{g,Ge}(grade)}{kT} \times e^{\Delta E_{g,Ge}(0)/kT}, \tag{6}$$

where ΔE_{gb}^{app} is the heavy-doping-induced apparent bandgap narrowing in the base region, and $\Delta E_{g,Ge}(grade)$ is the Ge grading factor across the base. Based on the SIMS profile data, the theoretical $\beta(T)$ dependence is also included in Figure 9, and the measured results agree well with our calculations. The negative temperature coefficient of β in SiGe HBTs (in contrast to Si BJTs) can be potentially used to mitigate thermal-runaway in high-power applications at elevated temperatures, a decided advantage over Si BJTs.

Shown in figure 10 are typical output characteristics of SiGe HBTs operating between 25 and 300°C. The output characteristics remain ideal at temperatures up to 300°C. The small negative slope in the output characteristics reflects self-heating in the device, and will be addressed in detail in Section 2.6.

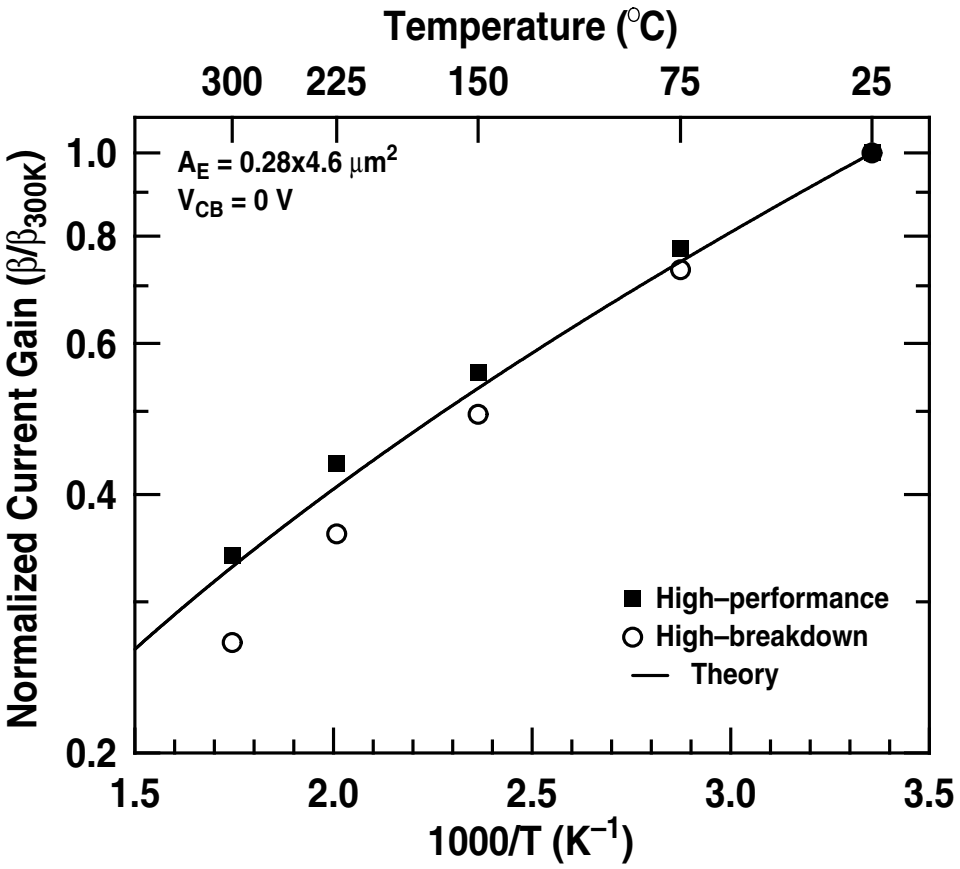

Figure 9: Peak current gain as a function of temperature.

2.4 ac Characteristics

The measured f_T and f_{max} versus bias current at 25, 100, and 200°C are shown in Figure 11 and Figure 12 for the high-performance and high-breakdown SiGe HBTs, respectively. The normalized peak f_T and f_{max} for both types of HBTs are shown in Figure 13. Similar changes in peak f_T and f_{max} were observed for the two device types. Thus, for brevity, we will limit our discussion here to the high-performance SiGe HBTs.

The peak f_T for the high-performance HBTs, as shown in Figure 13, decreases by 29% across the temperature range, from 125 GHz at 25°C to 89 GHz at 200°C, while the peak f_{max} decreases by 23%, from 122 GHz at 25 °C to 94 GHz at 200°C.

The f_T can be expressed as a series of transit times according to

$$f_T = \frac{1}{2\pi}\left\{\frac{kT}{qI_c}(C_{eb}+C_{cb})+\tau_F\right\}^{-1}, \tag{7}$$

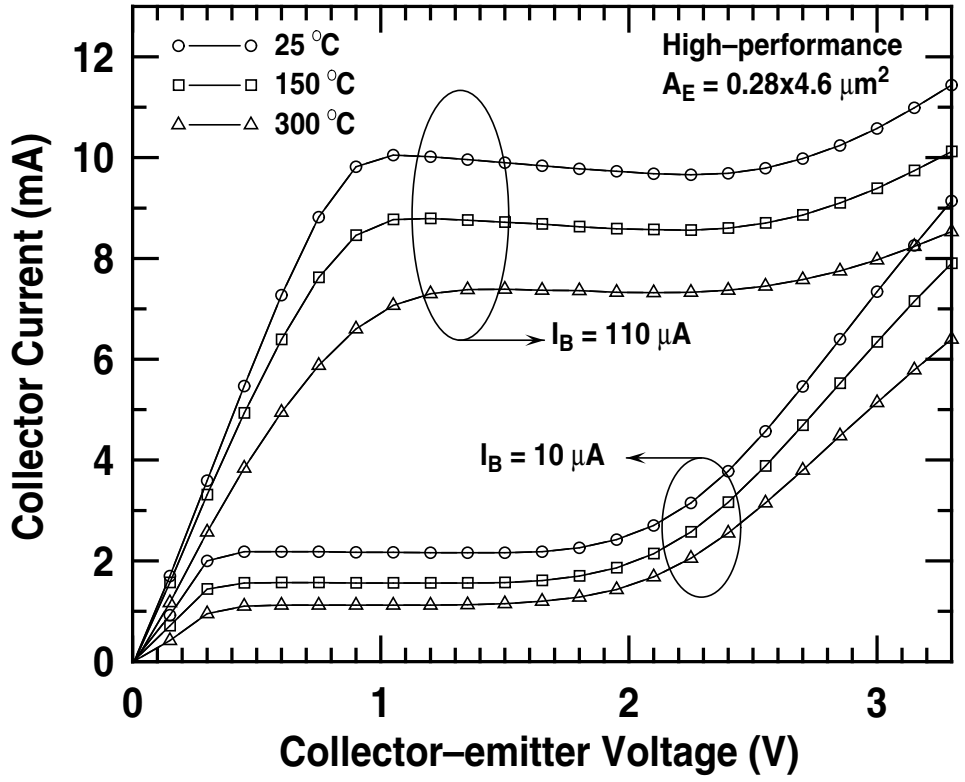

Figure 10: Common emitter output characteristics between 25 and 300°C for a high performance SiGe HBT.

$$\tau_F = \tau_b + \tau_e + \tau_c, \tag{8}$$

where C_{eb} is the emitter-base capacitance, C_{cb} is the collector-base capacitance, and τ_F is the forward transit time comprised of base, emitter, and collector transit times τ_b, τ_e, and τ_c, respectively. The value of τ_F can be easily extracted from a plot of $1/2\pi f_T$ versus $1/I_C$ [10]. The extracted forward transit time is found to increase by 39% from 1.09 pS at 25 °C to 1.51 pS at 200 °C. Assuming τ_F is dominated by τ_b at all temperatures, τ_b can be expressed as

$$\tau_b \approx \frac{W_b^2}{\widetilde{D}_{nb}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \right\}, \tag{9}$$

where W_b is the base width, $\widetilde{D}_{nb}$ is the position-averaged diffusion coefficient, k is the Boltzmann's constant, and $\Delta E_{g,Ge}(grade)$ is the Ge grading factor. $\widetilde{D}_{nb}$ can be expressed as

$$\widetilde{D}_{nb} = \frac{kT}{q}\mu \tag{10}$$

where the temperature dependence of μ is well understood as $T^{-1.5}$ [30]. By applying the appropriate Ge grading factor deduced from the SIMS data in (9), τ_f is found to theoretically increase by

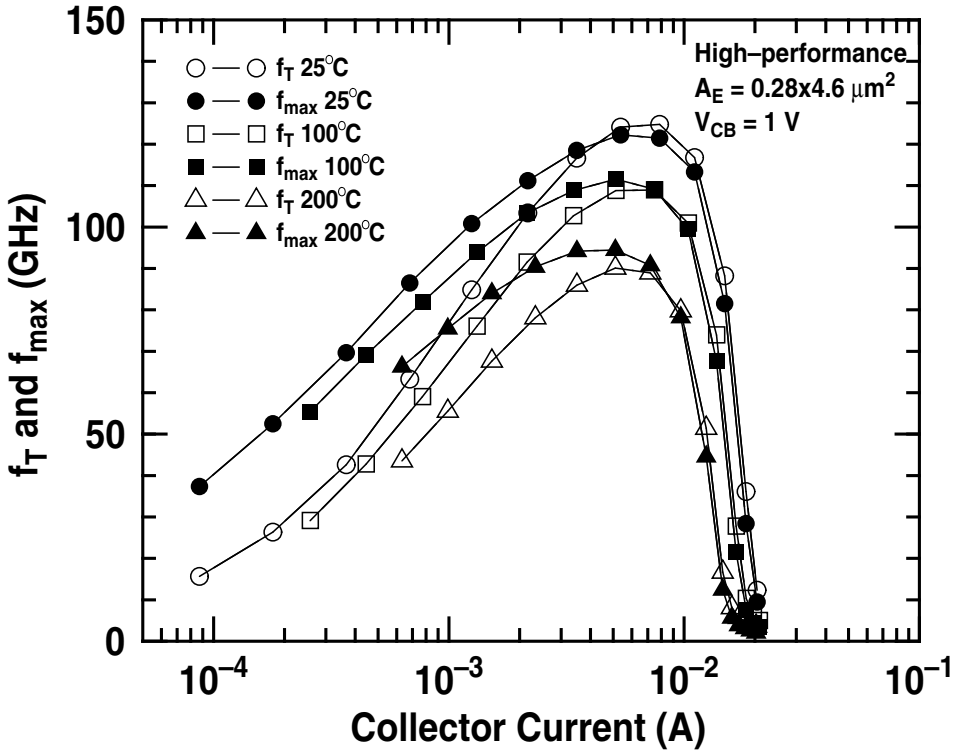

Figure 11: f_T and f_{max} versus collector current density for a high-performance SiGe HBT.

46% when the temperature is increased from 25 to 200 °C, which is in reasonable agreement with the data and suggests that high-temperature degradation in the minority mobility dominates the $f_T(T)$ dependence. The estimated peak f_T at 300°C (beyond the measurement temperature range of our present test system) is about 75 GHz, clearly adequate for a large class of circuit applications. f_{max} can be expressed as

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{cb} r_b}}, \tag{11}$$

where r_b is the base resistance. By assuming C_{cb} is a temperature independent constant, and extracting r_b from the deembedded S-parameters, f_{max} is found to theoretically decrease by 22%, which is again in reasonable agreement with the data. The estimated peak f_{max} at 300°C is roughly 65 GHz. A similar agreement between data and theory is obtained for high-breakdown HBTs. Note from Figure 12 that f_T and f_{max} for the high-breakdown devices decreases rapidly at I_C around 1 mA due to HBE, as discussed in Section 2.3.

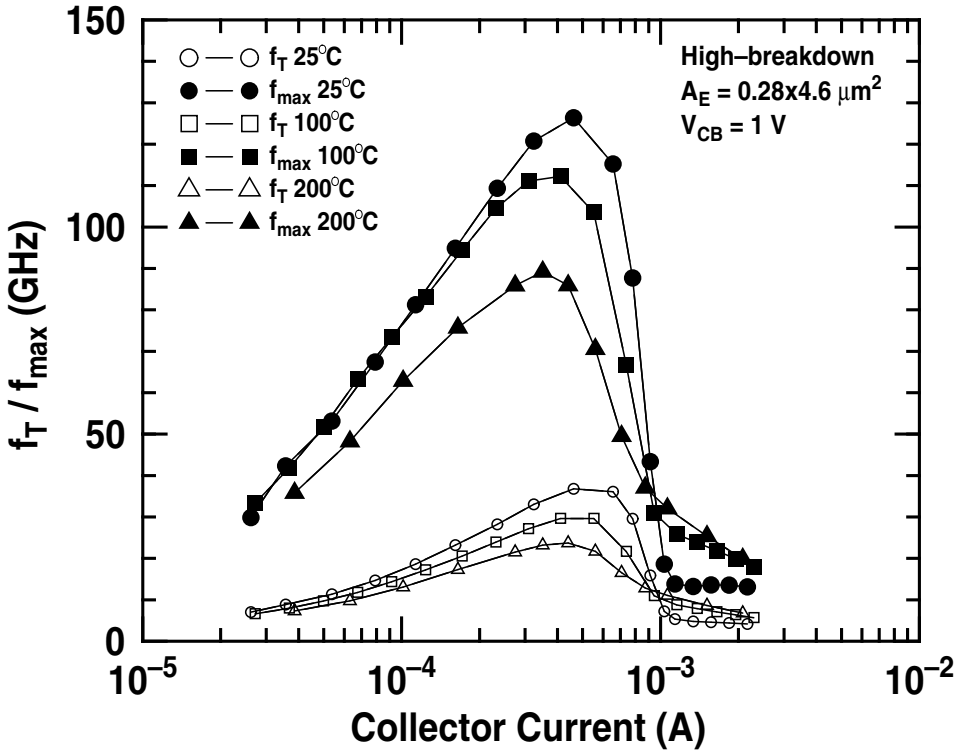

Figure 12: f_T and f_{max} versus collector current density for a high-breakdown SiGe HBT.

2.5 Breakdown Voltage

Due to the finite impedance at the base terminal in real circuits, BV_{CEO} does not represent the maximum voltage that can be sustained by the device. From a temperature perspective it does, however, provide an accurate gauge of the impact of high temperatures on the voltage limits for circuit design. Figure 14 shows the normalized BV_{CEO} of both the high-performance and the high-breakdown devices over temperature.

Since BV_{CEO} is to first-order determined by the product of M-1 and β at any given temperature, M-1 was measured using the techniques described in [31], and the results are shown in Figure 15 and Figure 16.

The combination of the temperature dependencies of β and M-1 will determine BV_{CEO} in the device at any temperature. As β decreases with increasing temperature, an increase of M-1 is necessary to offset the β decrease, in agreement with the data shown in Figure 15 and Figure 16 (the cross mark). It can be seen from Figure 15 and Figure 16 that M-1 decreases for the same V_{CB} as the temperature increases due to the increase in phonon scattering with temperature

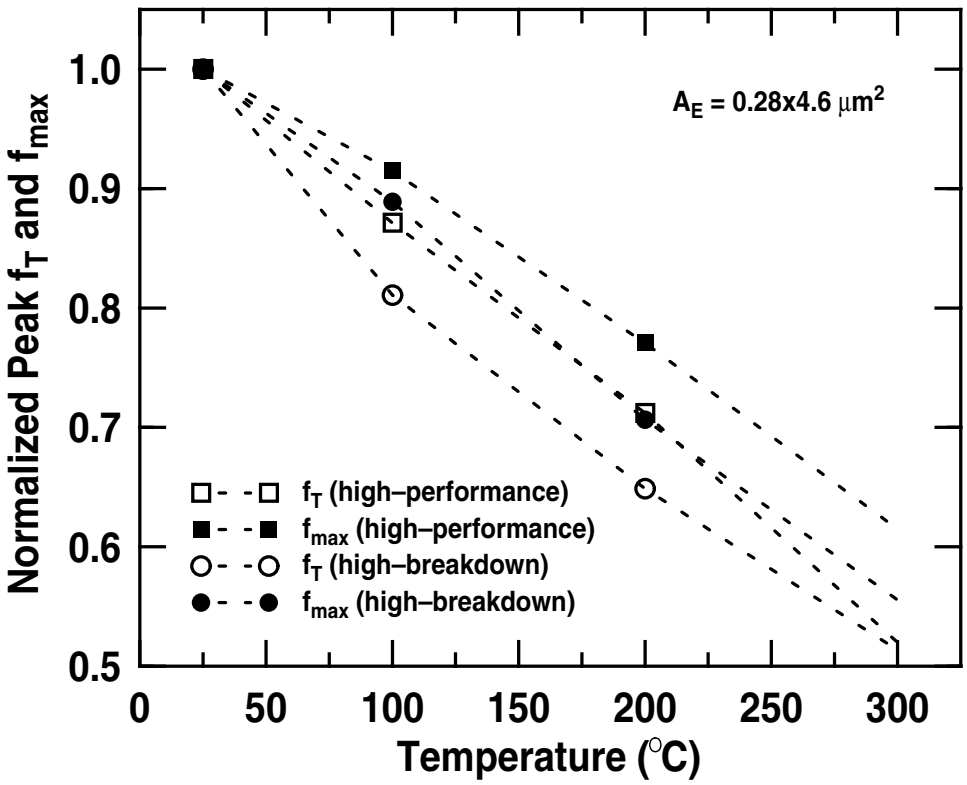

Figure 13: Peak f_T and f_{max} as a function of temperature.

[32]. Note that for the same biasing current the base-emitter turn-on voltage inherently decreases at higher temperatures due to the increase of the intrinsic carrier concentration. Hence, V_{CB} increases with temperature for the same V_{CE}. M-1 is a complicated function of temperature, as are V_{CB} and the emitter-base turn-on voltage. Observe that BV_{CEO} (the cross marks in Figure 15 and Figure 16) of the high-performance devices decreases slightly as the temperature increases, while that for the high-breakdown devices increases with temperature (obviously good news in the latter case). This difference is noteworthy for circuit applications and is the result of the differences in M-1 between the two (the temperature dependence of β is nearly the same for both – refer to Figure 9). A comparison of Figure 15 and Figure 16 suggests that M-1 of the high-breakdown device is more temperature dependent, as expected due to its lower collector doping and consistent with the results in [32]. The existing compact models may thus need to be refined to accurately capture the BV_{CEO} of these SiGe HBTs at high temperature if they do not explicitly account for the temperature dependence of M-1.

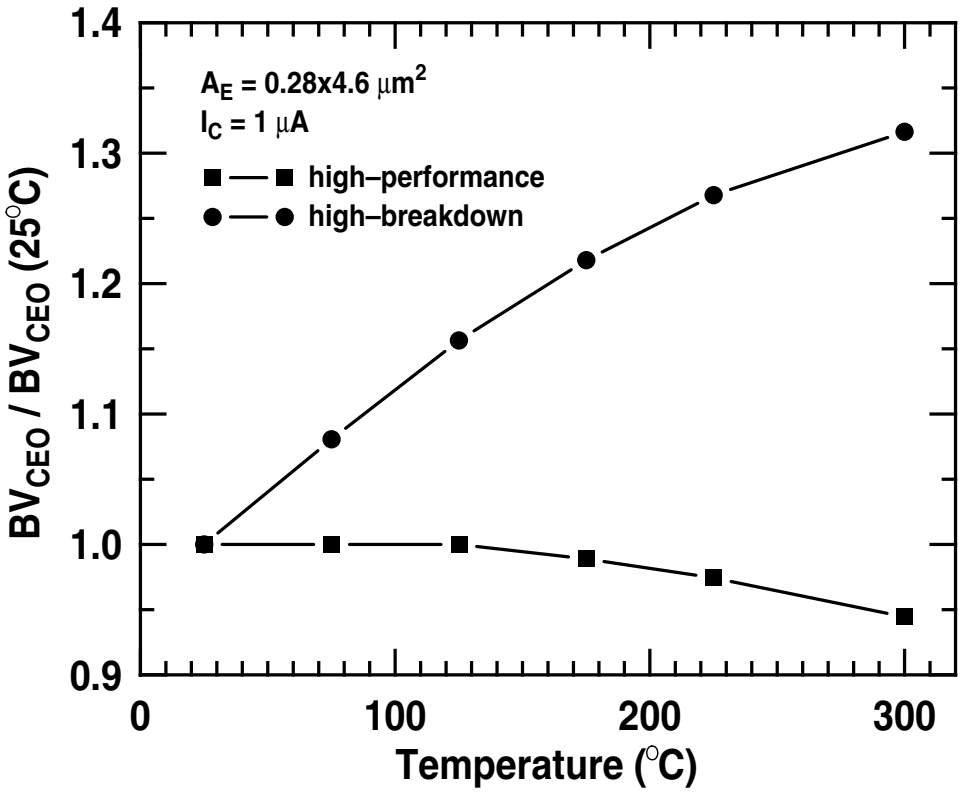

Figure 14: Normalized BV_{CEO} between 25 and 300°C.

2.6 Reliability issues

Temperature is a well-known, albeit complicated, accelerator for most device failure mechanisms, and thus is a key concern for any high-temperature applications of SiGe HBTs. In addition to simple changes in ambient temperature, transistor self-heating also increases the internal device temperature as well as the temperature gradients, potentially producing additional reliability concerns. Since the increase in phonon scattering with increased temperature will generally degrade the thermal conductivity, this issue is an important consideration for high temperature electronics. The self-heating characteristics of these SiGe HBTs as a function of ambient temperature were therefore measured using the technique described in [33], and the results are shown in Figure 17.

Figure 18 plots the thermal resistance R_{th} extracted by the relation

$$T_j = T_{amb} + R_{th} \times P_{diss}, \tag{12}$$

R_{th} maintains a constant value over the entire power range considered. It can be seen that

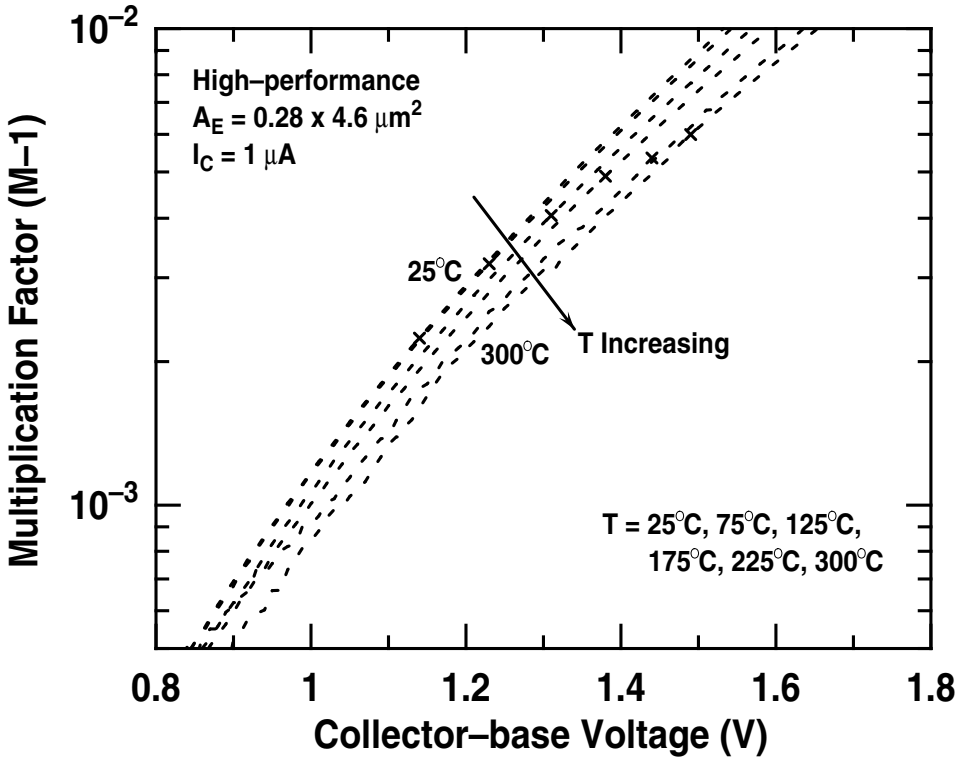

Figure 15: M-1 as a function of temperature and collector-base voltage for high-performance devices.

thermal resistance increases as ambient temperature increases, as expected. The model presented in [34] suggests that device self-heating and its thermal resistance can be significantly reduced by breaking the emitter finger into smaller segments, and thus has been confirmed by our data at higher temperatures, as shown in Figure 17 and Figure 18. It should thus be possible to use this approach to help mitigate the impact of high-temperature operation on the device self-heating characteristics.

The effect of reverse emitter-base hot carrier stress is to increase (degrade) the base current without affecting the collector current. Typical Gummel characteristics with increasing stress time are shown in Figure 19.

Shown in Fig 20 is the base current damage ratio at different stress temperatures.

As the temperature increases from 25 to 75°C, the base current damage ratio decreases, consistent with [35]. As the temperature increases further, however, observe that the base current damage ratio "saturates" for the same stress time. The net temperature dependence of the device degradation depends on the number of injected hot carriers and the energy of those carriers. Under constant

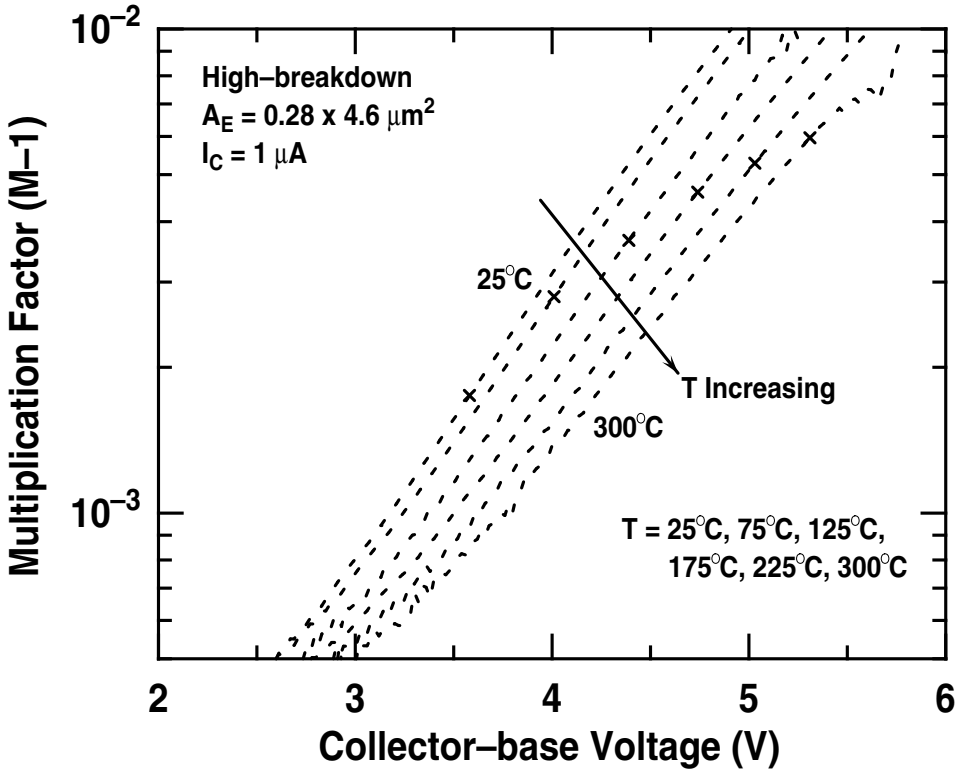

Figure 16: M-1 as a function of temperature and collector-base voltage for high-breakdown devices.

stress voltage conditions, the number of hot carriers present at the Si-SiO_2 interface is proportional to the reverse-bias stress current, which increases with the ambient temperature. The energy of the carriers, however, depends on the mean free path between the carrier scattering events, which decreases with any increase of the ambient temperature due to enhanced phonon scattering, and thus for these devices, at least between 25 and roughly 75°C, appears to dominate the damage process. Clearly, the reverse EB stress at high temperatures is improved compared to room temperature, which is good news from an application standpoint.

We have previously reported a robust, time-dependent stress methodology for investigating "mixed-mode" (simultaneously forcing of high J_E and high V_{CB}) reliability degradation in SiGe HBTs [36], and this technique has been applied in the present investigation. First, the known J_E dependence at 25°C was investigated as a reference point for the damage process, and then J_E was fixed at 30 mA/μm^2 and the ambient temperature was increased first to 100 then 200°C. The resultant base current damage ratios for the forward- and inverse-mode characteristics are shown in

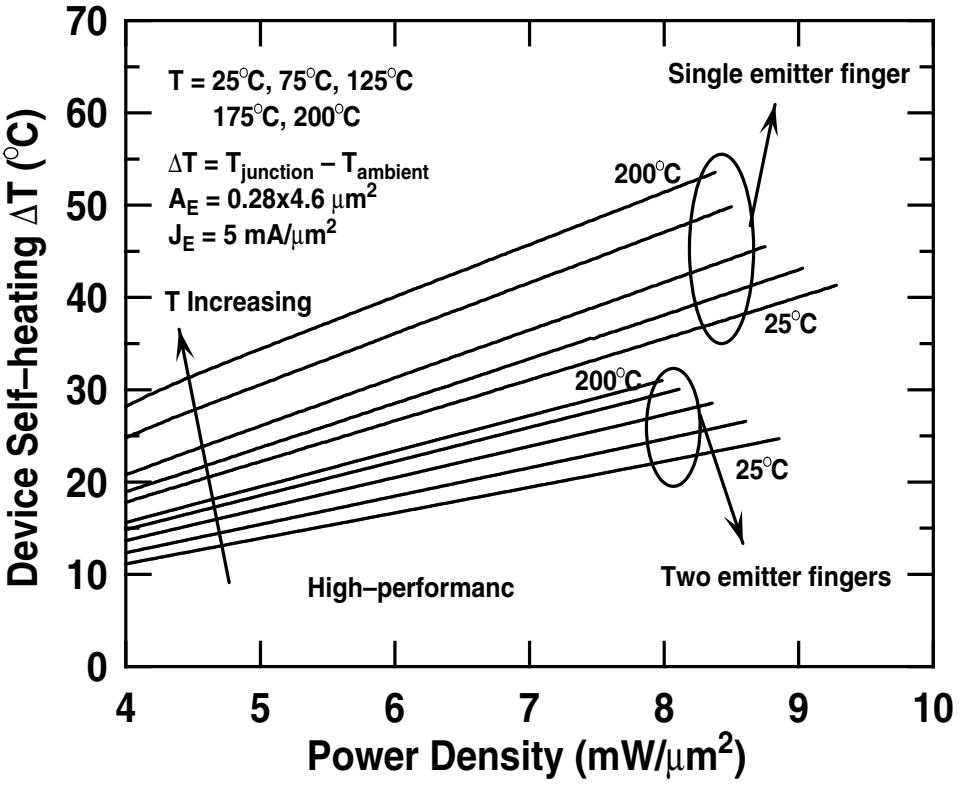

Figure 17: Device self-heating characteristics at various temperatures.

Figure 21 and Figure 22, respectively.

For the forward-mode Gummel characteristics, when J_E is fixed at 30 mA/μm^2 and the ambient temperature increases from 25 to 100°C, the base current damage ratio increases slightly. As the temperature increases further to 200°C, however, the base current damage ratio actually decreases to a level similar to the ratio for mixed-mode stress at room temperature with a J_E of 20 mA/μm^2, which is clearly excellent news. Mixed-mode stress is known to create a large inverse-mode base leakage current component, while reverse EB stress does not create any excess base leakage in the inverse-mode SiGe HBTs [37]. The mixed-mode stress induces traps not only in the EB space-charge region but also in the CB space-charge region, the latter being consistent with the observed increase in inverse-mode base current leakage, as shown in Figure 22. The base current damage ratio for the inverse-mode Gummel characteristics shows similar changes as for the forward-mode Gummel characteristics with current density and temperature, as shown in Figure 22. This competing damage enhancement and subsequent passivation with increasing stress was also reported in

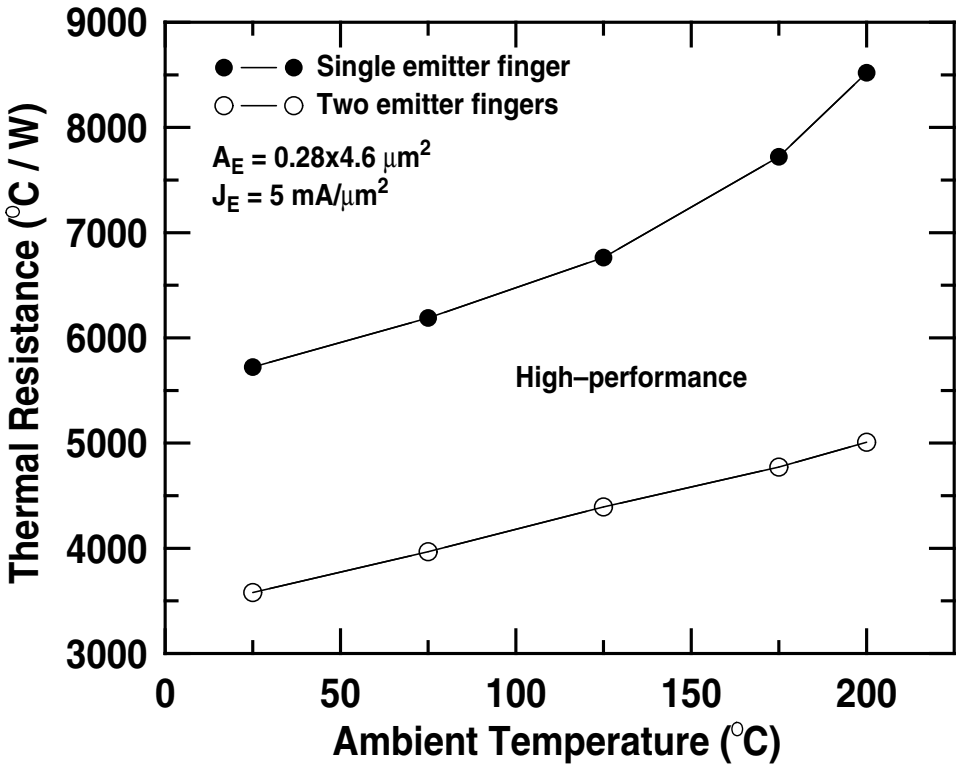

Figure 18: Device thermal resistance as a function of temperature.

[38]. These results suggest that the effects of the high current stress dominate those of the ambient temperature alone, consistent with the results given in [39]. The emitter resistance extracted from the Gummel characteristics decreases with increasing stress time. The variation of emitter resistance, however, has little temperature dependence. The decrease of the emitter resistance is also reported under very high forward current stress [39].

In general, contrary to popular wisdom, we do not see any obvious device-level reliability damage mechanisms in these SiGe HBTs that would be of direct concern for electronics operating at high temperatures. Although we have not as yet measured it experimentally, given that this SiGe technology incorporates full-copper metalization, electromigration concerns at high temperatures are not expected to be a serious constraint for this technology. Moreover, it will be important to "build in" reliability for high-temperature applications by designing and processing devices to make them resistant to failures due to known failure and degradation mechanisms. Once the failure mechanisms and their functional dependencies upon stress conditions are known, design and layout rules for circuits can be developed that maintain the stresses within tolerable limits.

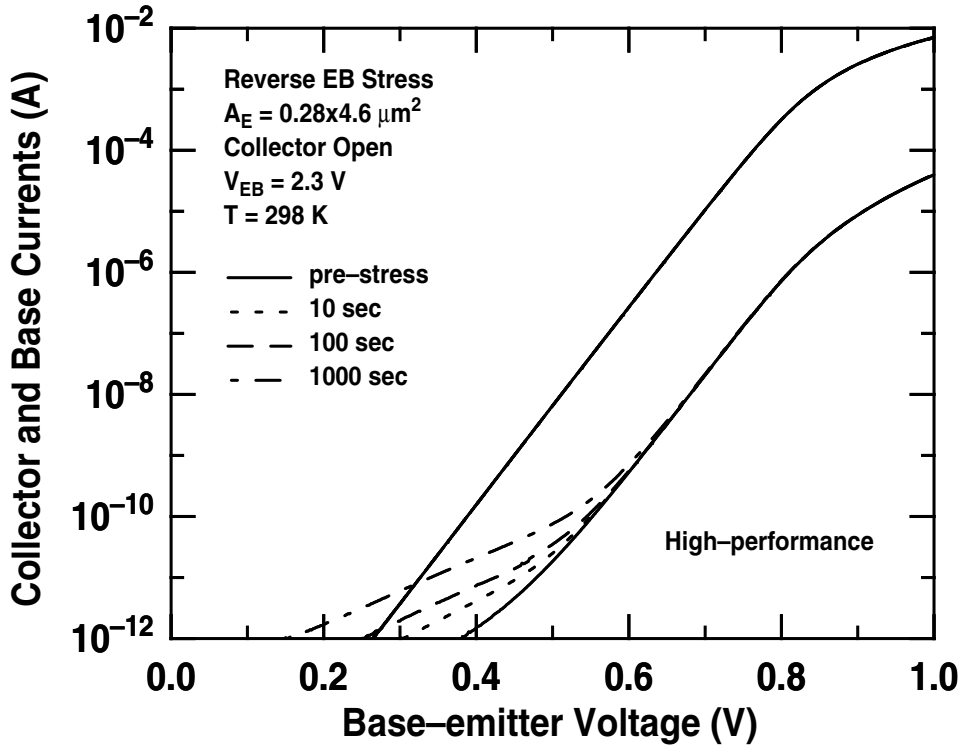

Figure 19: Typical Gummel characteristics vs. stress time for reverse emitter-base stress at room temperature.

2.7 Low-frequency noise

Low-frequency noise in transistors usually has a 1/f-like spectrum and sets the lower limit on the signal level, not only in the low frequency range, but also at high frequencies via the up-conversion to the carrier frequency through the non-linearities of the device. Low-frequency noise is thus a crucial design issue in many analog and RF circuits and in systems such as direct-conversion receivers, oscillators, and mixers. Being able to simultaneously achieve very small low-frequency noise and noise figure is one of the unique advantageous features of SiGe HBTs [29]. Figure 23 shows the input-referred base current noise spectra in SiGe HBTs operating at high temperatures with I_B of 0.4 and 4 μA, and Figure 24 shows S_{I_B} at 10 Hz as the temperature increases.

As can be seen clearly from the results, LFN actually improves with increasing temperature, which is again clearly good news. The LFN mechanism in these SiGe HBTs consists of a superposition of Lorentzian spectra due to trapping/detrapping of free carriers [40] and $S_{I_B} = KI_B^2/f^\gamma$, where γ is the frequency dependence coefficient close to unity. According to [41], as a result of the

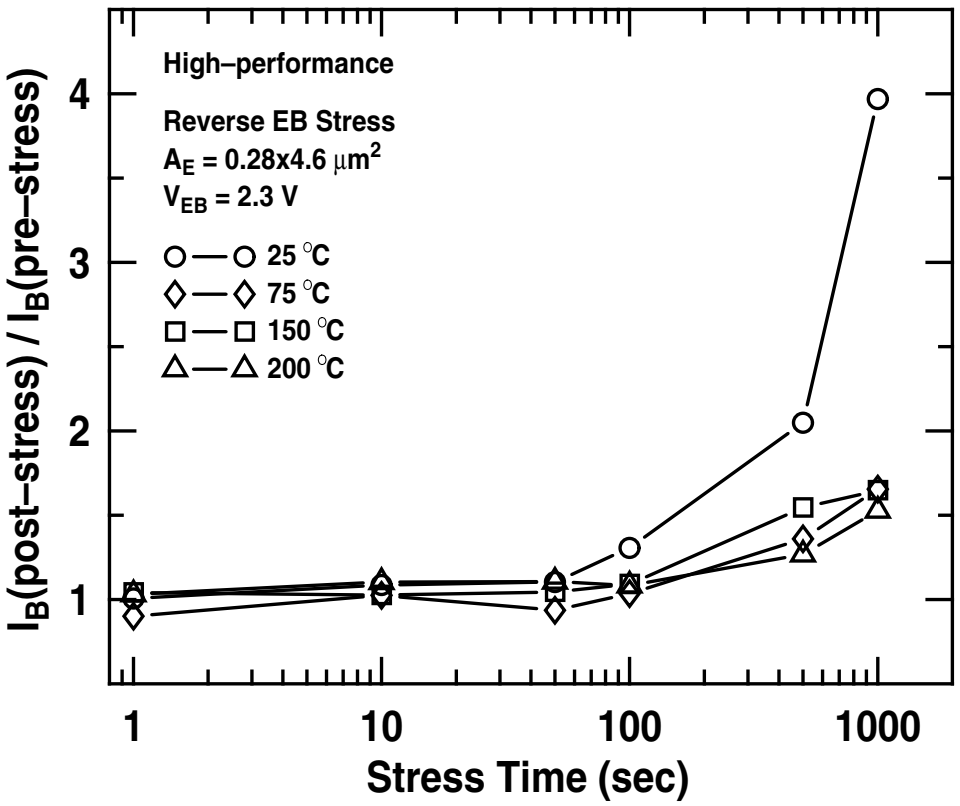

Figure 20: Base current damage ratio at $V_{BE} = 0.5$ V vs. stress time for reverse emitter-base stress at various temperatures.

superposition of Lorentzian spectra, the frequency dependence term γ of LFN can be expressed as

$$\gamma = 1 - \frac{1}{ln(\omega\tau_0)} \left\{ \frac{dlnS(\omega, T)}{dlnT} - 1 \right\}, \tag{13}$$

where τ_0 is of the order of 1e-14 sec, and $S(\omega, T)$ is the noise power spectral density at frequency ω and temperature T. Eq. 13 suggests that γ changes slightly as the derivative of $lnS(\omega, T)$ on $ln\ T$ changes. Here γ was extracted at two bias currents from the measured spectra at 10Hz. The extracted γ is consistent with the results predicted by Eq. 13, and thus confirms that the superposition of Lorentzian spectra due to trapping-detrapping of carriers is the LFN mechanism in these devices. Experimental results thus show that high temperature operation does not compromise the decided advantage of small LFN in these SiGe HBTs.

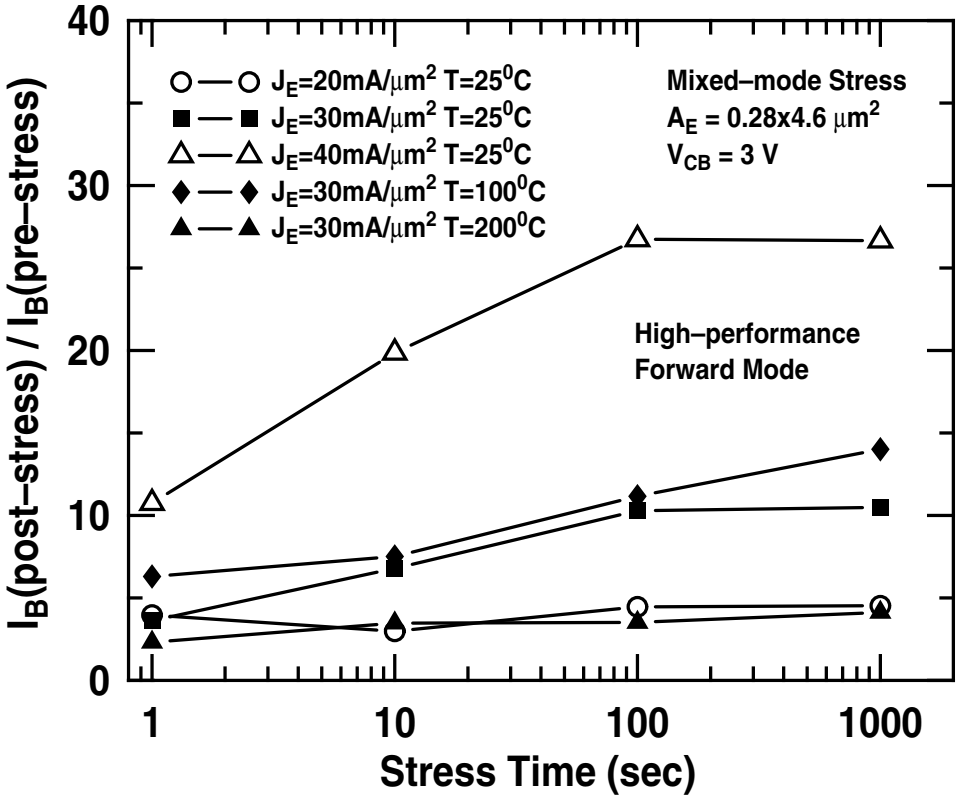

Figure 21: Base current damage ratio in forward-mode Gummel characteristics at $V_{BE} = 0.5$ V vs. "mixed-mode" stress time for different emitter current densities and different stress temperatures.

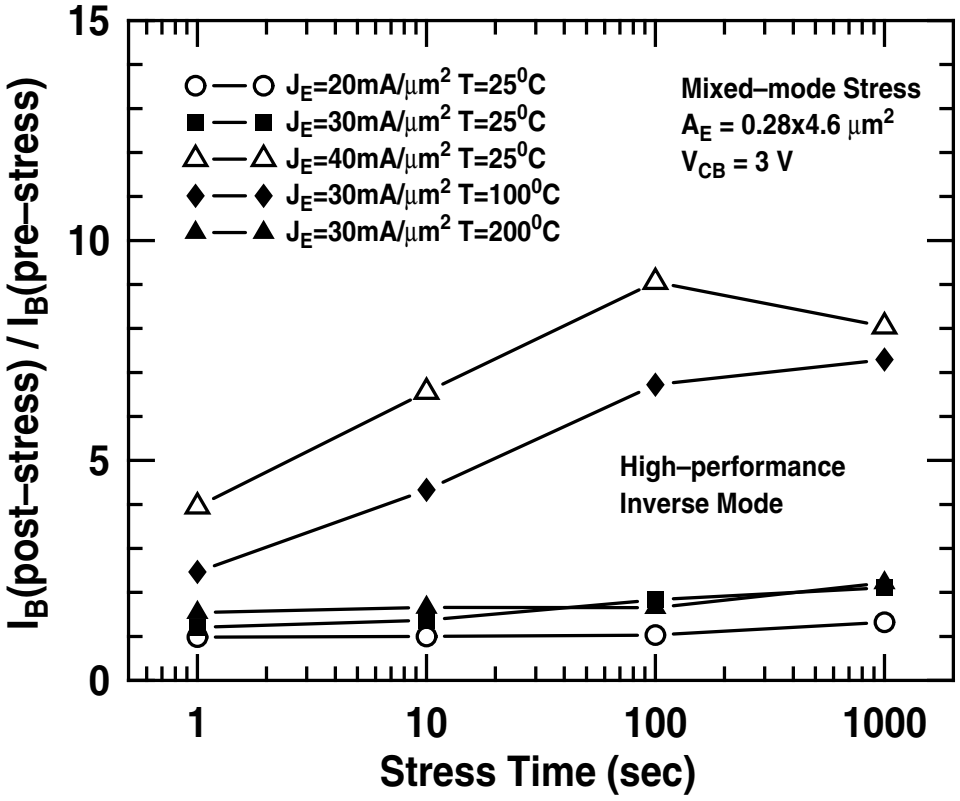

Figure 22: Base current damage ratio in reverse-mode Gummel characteristics at $V_{BE} = 0.5$ V vs. "mixed-mode" stress time for different emitter current densities and different stress temperatures.

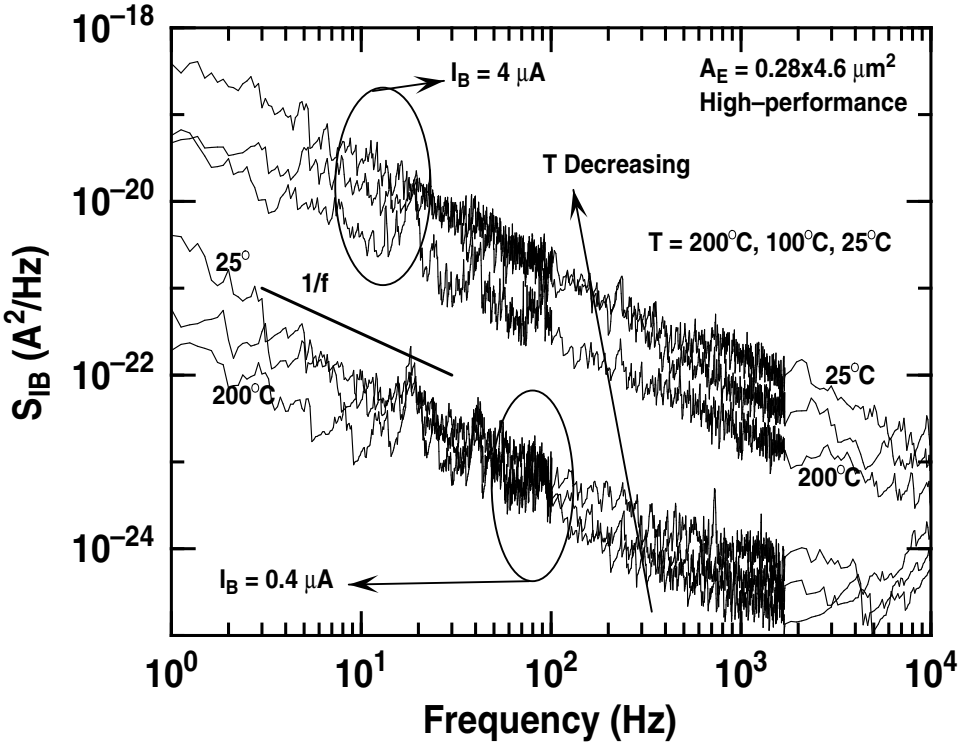

Figure 23: Low-frequency noise performance at elevated temperatures.

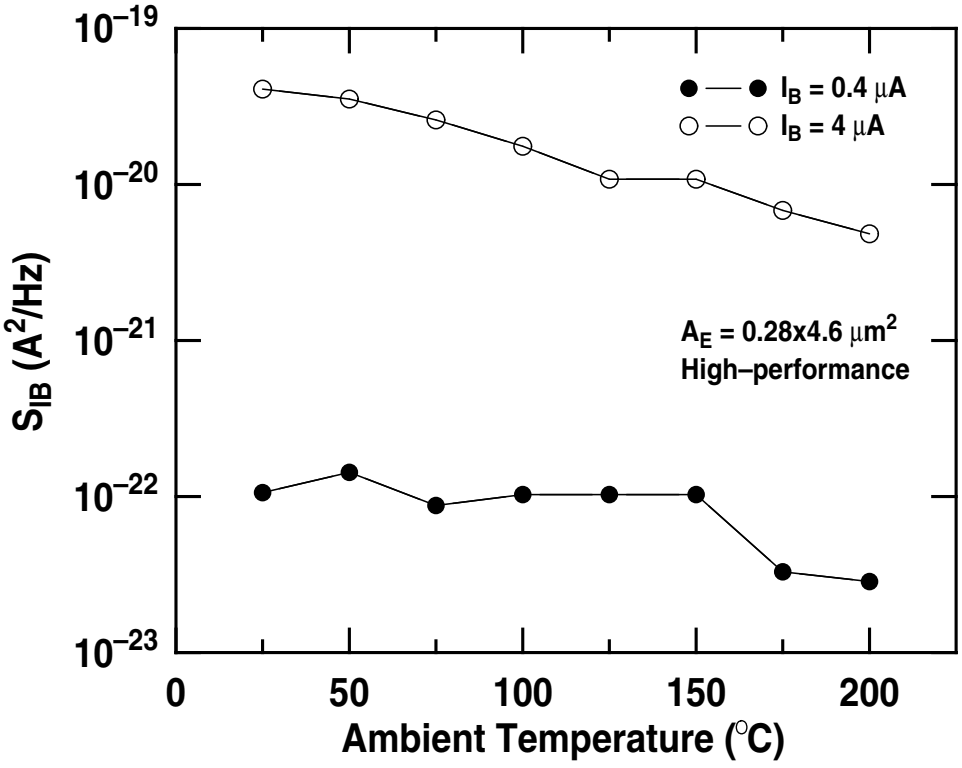

Figure 24: S_{I_B} at 10Hz versus I_B as a function of temperature.

CHAPTER III

SUBSTRATE BIAS EFFECTS IN VERTICAL SIGE HBTS FABRICATED ON CMOS-COMPATIBLE THIN FILM SOI

3.1 Introduction to HBT on SOI

Silicon-on-insulator (SOI) technology is rapidly progressing from the realm of a "niche technology" into mainstream IC production. The use of SOI allows a reduction in device parasitic, a built-in higher voltage capability, a reduction in signal cross-talk, improved soft error immunity, high temperature operation, and an elimination of latch up [42]. SiGe BiCMOS is often a preferred technology platform for wireless and communication applications because it combines the merits of both SiGe HBTs (for RF/analog functions) and CMOS transistors (for low-power digital functions) on the same die. SOI research, however, has been primarily limited to CMOS technology due to the difficulty of integrating BiCMOS on thin-film SOI. The challenge for achieving BiCMOS integration on SOI arises because bipolar transistors require thick subcollector (epi) regions to maintain low collector resistance, which is incompatible with standard thin-film SOI CMOS fabrication. Recently, however, a novel vertical SiGe HBT has been demonstrated on CMOS-compatible thin-film SOI [43]. The thick subcollector is eliminated in this approach and replaced by a "folded" collector structure, while the vertical profile (doping and Ge) is kept the same as for bulk SiGe HBT technology to preserve its high speed and low cost.

It is well-known that for double-gate MOSFETs with a thin back-gate oxide, threshold voltage fluctuations due to SOI thickness variations can be reduced by actively controlling the back gate voltage (substrate potential) [44], and research is on-going concerning these so-called "back-gate bias effects" in SOI CMOS [45] [46]. In such cases, the substrate can be viewed as a (controllable) fourth device terminal to optimize device and circuit performance. For SiGe HBTs on thin-film SOI, previous work has shown that a positive substrate bias can help alleviate transistor saturation effects due to the inherently high collector resistance, and hence improve the device frequency response

[43].

In the present work, we report the first comprehensive study of the substrate bias effects in vertical SiGe HBTs on thin-film SOI, and assess the impact on collector resistance, avalanche multiplication, thermal resistance, and device reliability. 2-D MEDICI simulations were used to help elucidate the underlying physics, and the simulation results correlate well with our measured data.

3.2 Device technology

The SiGe HBT on SOI devices used in this work feature a 120 nm silicon layer with an average collector doping concentration of 1.5 x 10^{17}/cm^3, on top of a 140 nm buried oxide layer [43]. Fig. 25 shows an SEM cross-section of a vertical SiGe HBT on CMOS-compatible, thin-film SOI.

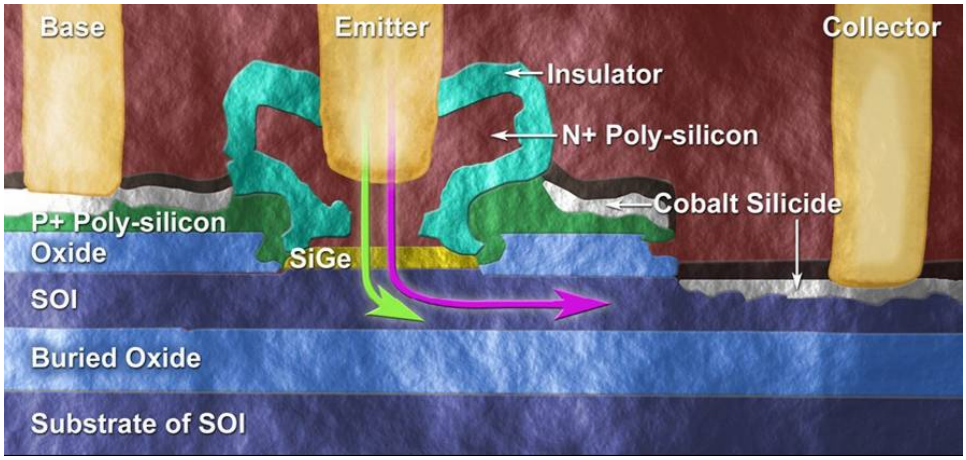

Figure 25: Cross-sectional SEM of the SiGe HBT on SOI.

3.3 dc Characteristics

The Gummel characteristics of the SiGe HBTs on SOI with an emitter area of 0.16 x 0.8 μm^2 are shown in Figure 26, with the substrate voltage increasing from 0 to 20 volts. Observe that the collector and base currents are influenced by the substrate bias at V_{BE} greater than about 0.9V. The collector current increases while the base current decreases for a fixed V_{BE} when the substrate bias voltage increases from 0 to 20 volts. Due to the absence of a true subcollector and the use instead of a "folded" collector structure, collector resistance (R_C) is clearly a key design issue in SiGe HBTs on thin-film SOI, dramatically limiting performance. This behavior indicates that quasi-saturation,

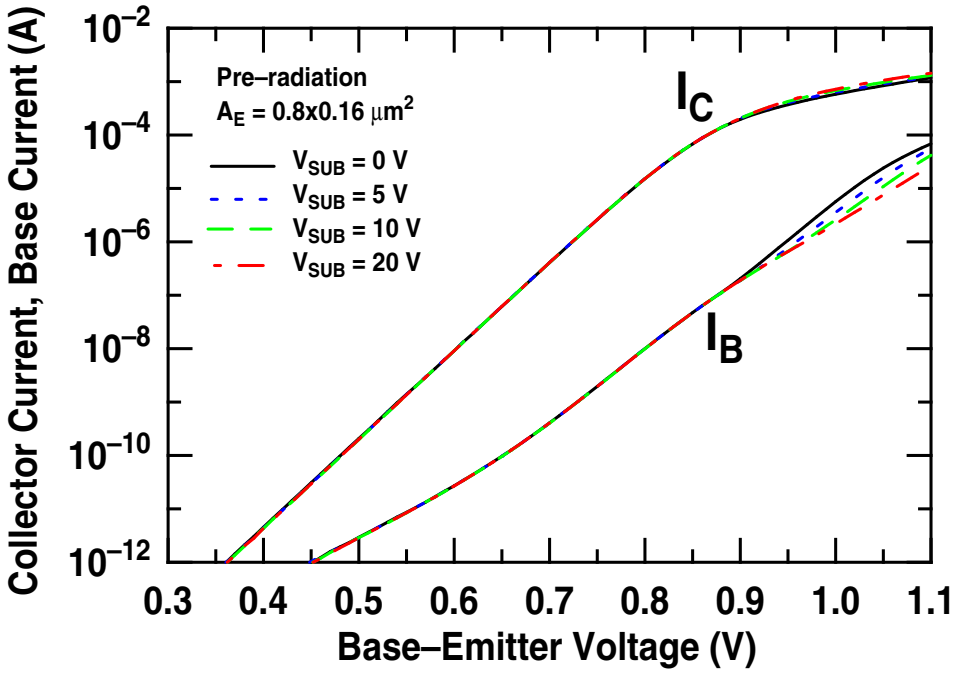

Figure 26: Forward-mode Gummel characteristics of a SOI SiGe HBT under four substrate bias conditions: 0V, 5V, 10V and 20V.

which arises due to the inherently high collector resistance (R_C) in this structure, is partially suppressed when the substrate bias increases. To obtain a deeper insight into this substrate bias-induced R_C modulation, calibrated two-dimensional MEDICI simulations were used [47]. Fig. 27 shows 2-D MEDICI simulations of the electron concentration in SiGe HBT for substrate biases of 0V and 20V, respectively. With the increase of substrate voltage, a very thin n^+ electron accumulation layer forms at the collector-buried oxide interface. This accumulation layer serves as a bias-induced "sub-collector," and provides a lower-impedance conduction path for the collector current. The simulated electron current flow under two different substrate bias voltages of 0 and 20V are shown in Figure 28. With the increase of substrate voltage, this accumulation layer serves as a bias-induced "sub-collector," and the collector current conduction path is modified from the uniform distribution across the Si collector layer to a lower-impedance very thin "sub-collector" as the substrate voltage increases from 0 to 20 V. As such, R_C-induced quasi-saturation effects decrease with increasing substrate bias voltage.

The substrate bias affects not only the quasisaturation effect through collector resistance, but also the total output collector current. Fig. 29 shows the constant base current drive output characteristics

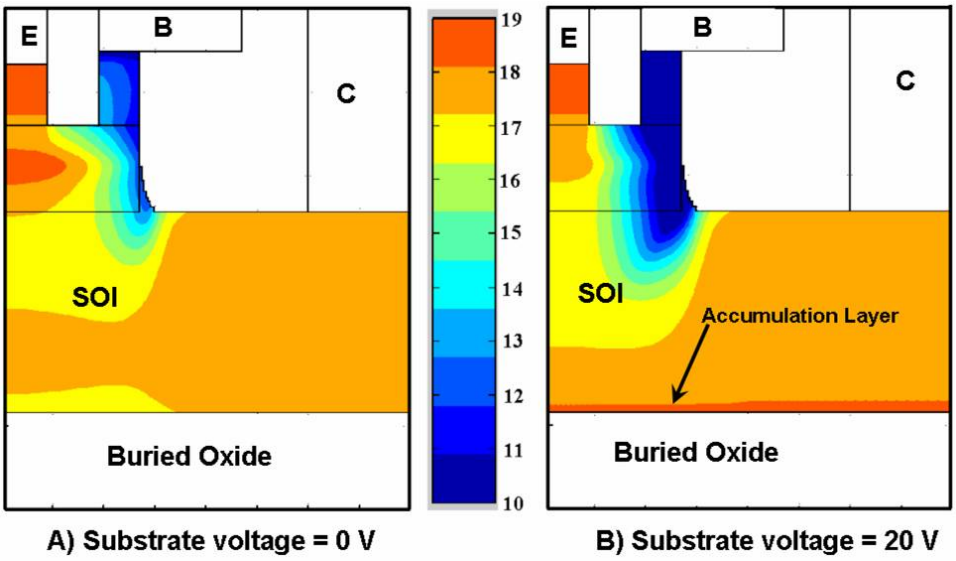

Figure 27: Simulated 2-D electron density ($I_B = 1.0\ \mu$A, $V_C = 1.5$ V).

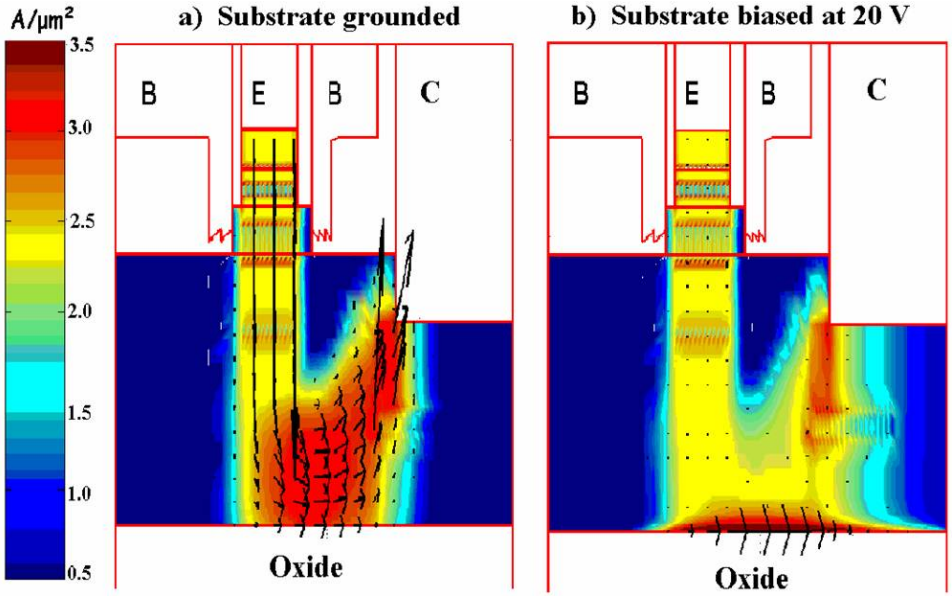

Figure 28: MEDICI simulation results showing electron flow contours at two different substrate bias conditions: a) 0V; b) 20V.

at different substrate biases for a typical vertical HBT on SOI. It can be clearly seen from Fig. 29 that the output collector current increases by about 40% for a constant base current drive as V_{Sx} increases from 0 to 20 V. It can also be inferred from the slopes in the saturation region of the output characteristics in Fig. 29 that R_C decreases significantly as V_{Sx} increases. Fig. 30 shows the

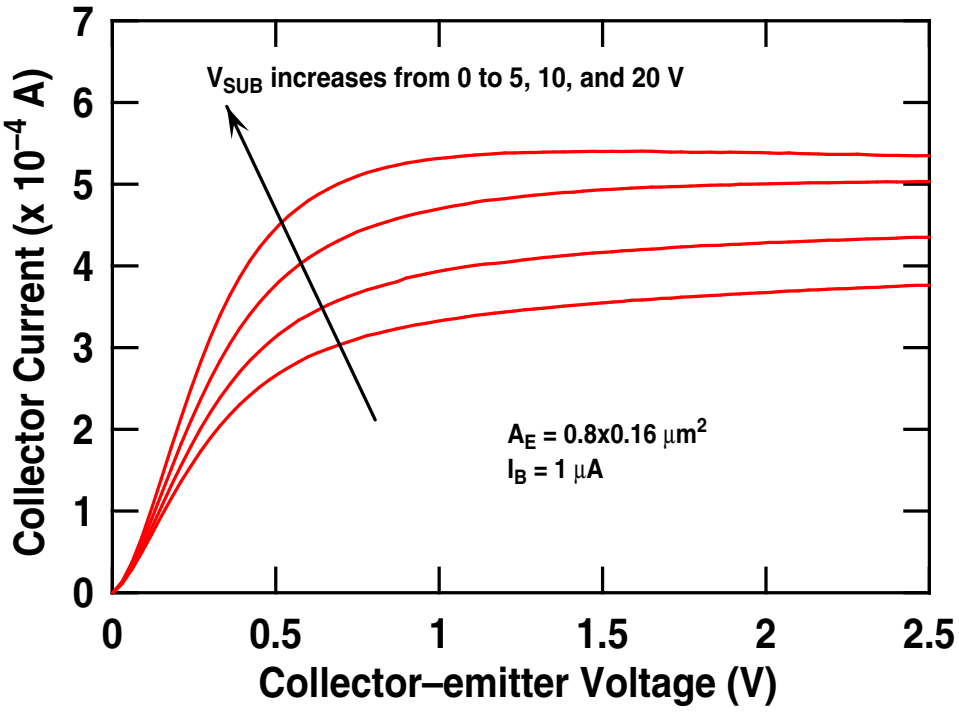

Figure 29: R_C as a function of V_{Sx} (Output characteristics at different V_{Sx}).

extracted R_C at low current for two SiGe HBTs on SOI with different emitter sizes as a function of substrate bias.

Clearly the R_C decreases strongly as substrate bias (V_{Sx}) increases, with the low-J_C collector resistance at 20V substrate bias being 580 and 790 Ω, for the two SiGe HBTs tested, which is still high but manageable, as it will decrease further at actual operating bias currents. The simulated R_C by MEDICI correlates well with the measured data. This clearly suggests that a positive substrate bias is very effective in R_C reduction and can be used as an active terminal to greatly enhance the device performance.

3.4 ac Characteristics

The measured f_T and f_{max} versus bias current at different substrate bias are shown in Figure 31 for a vertical SiGe HBT on SOI.

The peak f_T of the device improves from 37 GHz to 60 GHz when changing V_{Sx} from 0V to 20V. The corresponding f_{max} improves from 52 to 68 GHz. The collector-base capacitance increases with V_{Sx} due to the presence of an accumulation back surface. Since $f_{max} \propto \sqrt{f_T \,/\, C_{CB}}$,

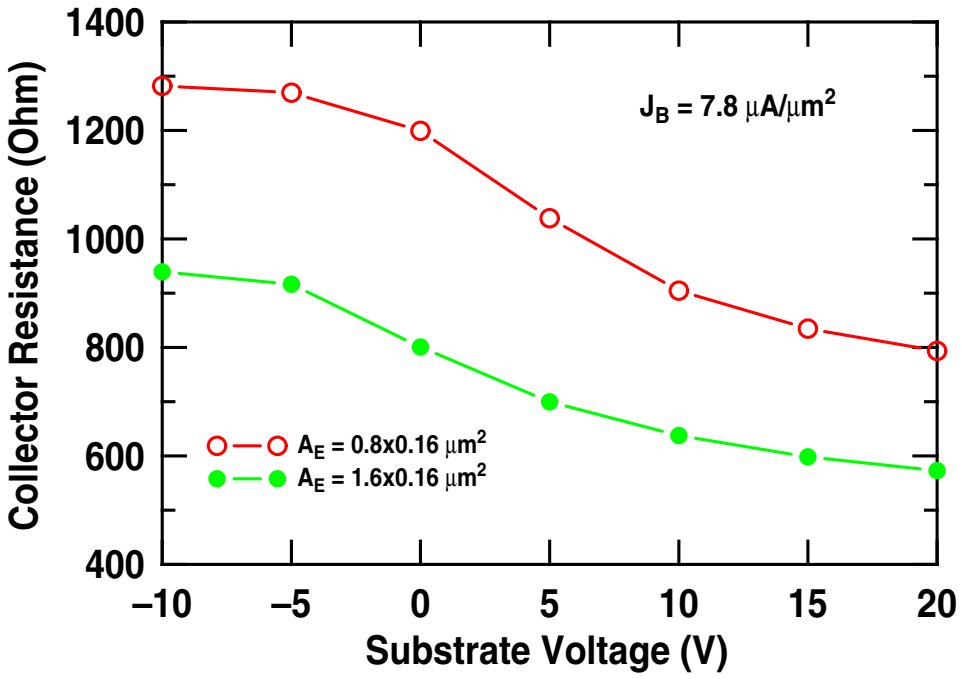

Figure 30: R_C as a function of V_{Sx} for HBTs on SOI with two different emitter length.

the peak f_{max} increases less compared to peak f_T with the increase of V_{Sx}. The substrate bias affects f_T and f_{max} by modulating the two-dimensional electric field and electron drift path. TCAD simulation was performed to better understand the strong dependence of f_T and f_{max} on V_{Sx}. Fig. 32 shows the simulated two-dimensional accumulated transit time in a vertical HBT on SOI.

It can be seen from Fig. 32 that base transit time τ_b is the dominant fraction of the overall transit time and that τ_b is reduced significantly when V_{Sx} increases from 0 to 10 V.

3.5 Avalanche multiplication

Substrate bias not only affects quasi-saturation in the device, but also the breakdown voltage (e.g., BV_{CEO}) [43]. To further understand the BV_{CEO} variation with substrate bias, M-1 was measured using the techniques described in [32], and the results are shown in Fig. 33. BV_{CEO} is to first-order determined by the product of the M-1 and β. Since β is only a weak function of substrate bias, BV_{CEO} occurs at a fixed level of M-1, which is a sensitive function of substrate bias, and thus BV_{CEO} can be manipulated (in principle, dynamically) in this device, which is unique and potentially of great benefit in circuit design (e.g., here BV_{CEO} changes from 4.7V to 2.3V with

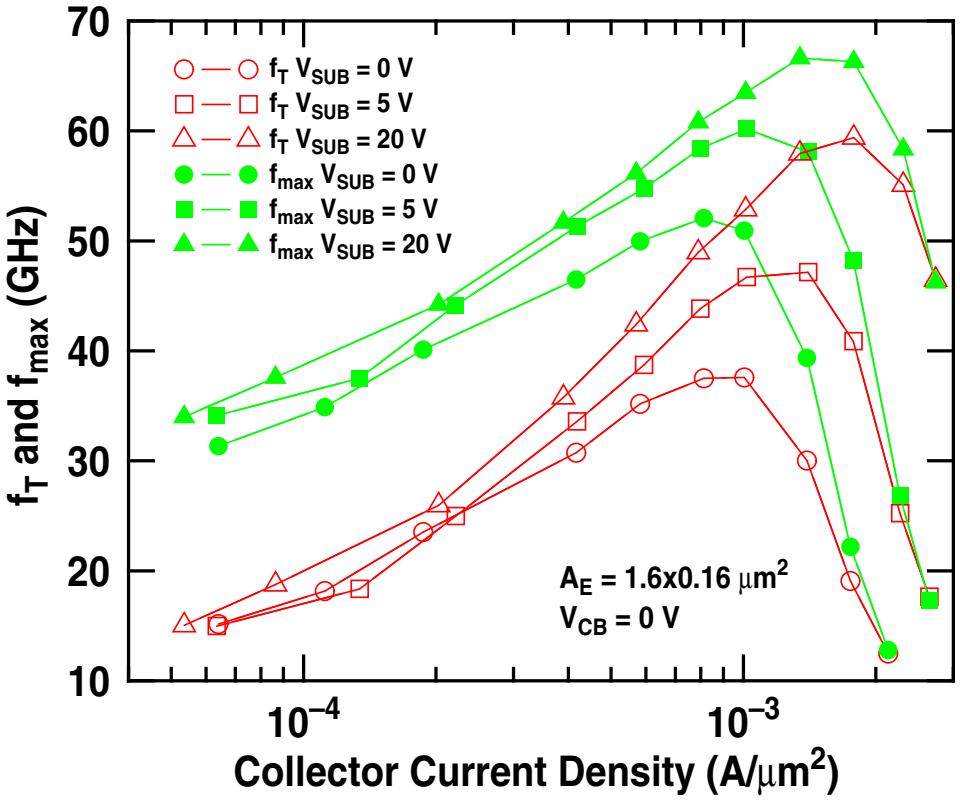

Figure 31: f_T and f_{max} as a function of J_C at various V_{Sx} for a HBT on SOI.

V_{Sx} of 0V to 20V, respectively). There are two different sources of M-1, one of which occurs at the lateral collector when $V_{CB} > 2.5$ V, and is hence is referred to as "extrinsic M-1"; the other occurs in the intrinsic vertical collector for relatively small V_{CB}, hence we call it "intrinsic M-1". Extrinsic M-1 dominates when the substrate bias is zero or negative, and intrinsic M-1 dominates for positive substrate bias. For simplicity, consider part of the SiGe HBT structure, with base, collector, n+ reachthrough and SOI substrate, as illustrated in Fig. 25. Due to the symmetry, along the central cut line, the electric field is vertical and the potential distribution can be solved exactly using the one-dimensional Poisson's equation. Based on the depletion approximation, the electric field distribution in the forward-active biased intrinsic transistor is shown qualitatively in Figure 34 for both low and high substrate biases. The problem is simply a pn diode in series with a MOS capacitor. For Figure 34a, the substrate bias is low and both the pn diode and MOS capacitor are reverse-biased (V_B<V_C, V_S<V_C). There are two distinct depletion regions, with widths y1 and y2, respectively. With a further increase of the collector voltage, the collector becomes fully depleted

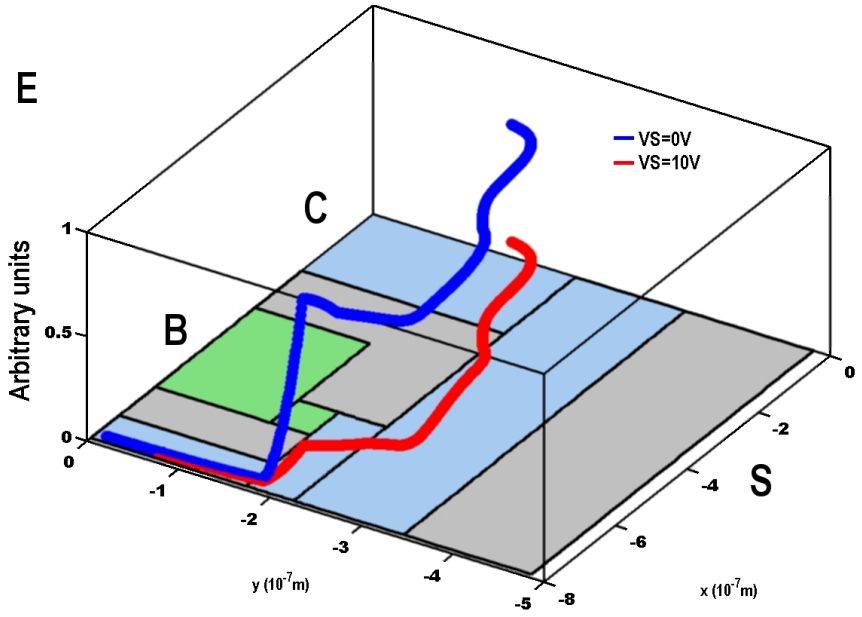

Figure 32: Accumulated transit time at different V_{Sx}.

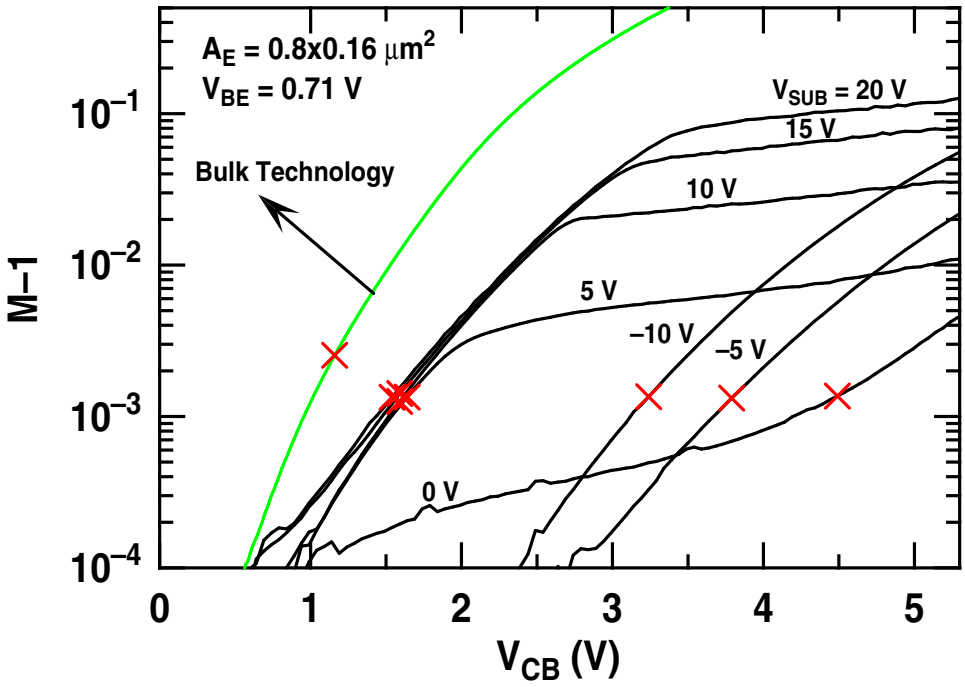

Figure 33: M-1 vs. V_{CB} and V_{Sx} (cross-marks indicate base current reversal).

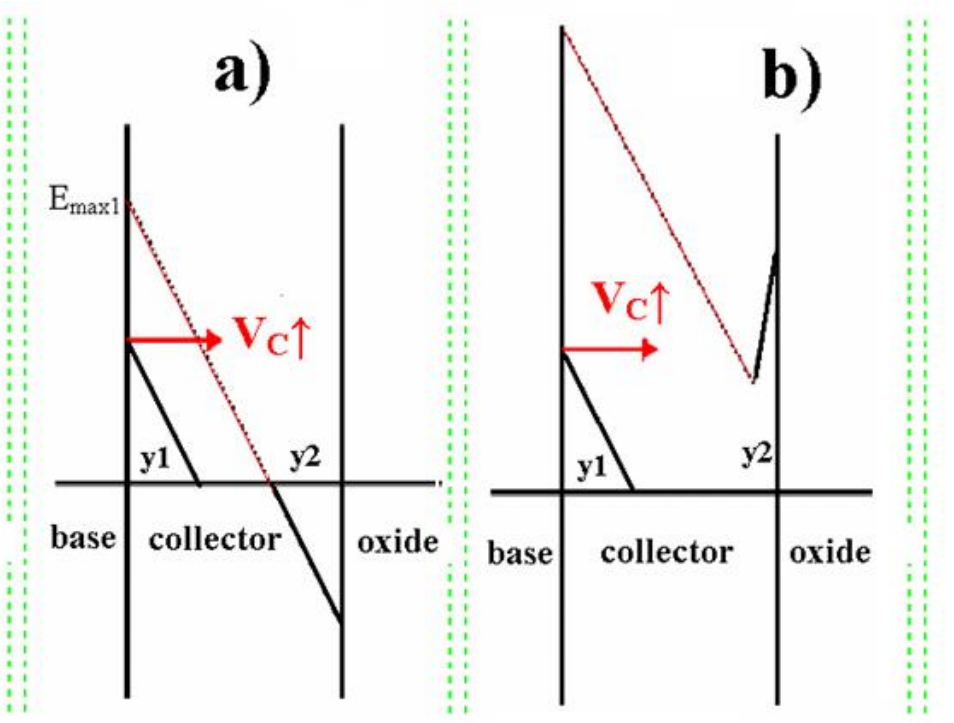

Figure 34: Electric field distribution in the intrinsic transistor: a) V_{SUB} low; b) V_{SUB} high;.

and the maximum electric field at the base-collector interface, E_{max}, decides the magnitude of the intrinsic M-1. For high positive substrate voltages, the inversion electron layer switches the electric field direction in the y2 region in Figure 34b. E_{max} hence the magnitude of intrinsic M-1 is several orders higher than in Figure 34a. When the collector becomes fully depleted, any further increases in the collector voltage will not influence the vertical electrical field hence the intrinsic M-1. Thus, we see the "flat" portion of M-1 for positive substrate bias. Note, however, that the collector voltage corresponding to the full depletion condition increases with substrate bias. Hence, with increasing substrate bias M-1 also increases in the "flat" portion of M-1 data.

The 2-D impact ionization rates at substrate biases of 0V and 20V were also examined using MEDICI simulations, as shown in Fig. 35, and indicate that avalanche multiplication is dominant at the lateral (extrinsic) collector at low substrate bias, while avalanche multiplication in the vertical (intrinsic) collector dominates at high substrate bias, effectively shifting and strongly manipulating the breakdown voltage in the device.

For comparison, the avalanche multiplication in a bulk SiGe HBT with 120-GHz f_T was also

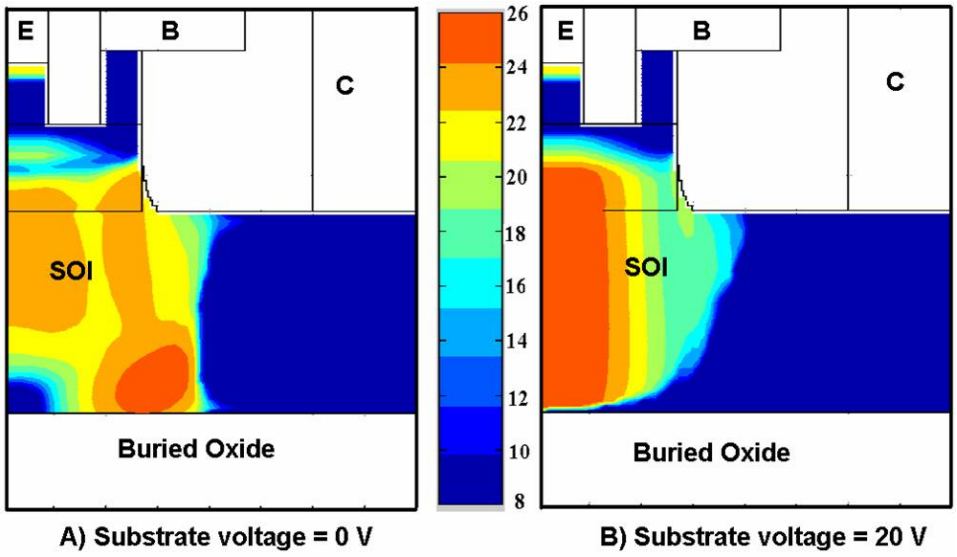

Figure 35: Simulated 2-D impact ionization rate (V_{BE} = 0.7V, V_{CB} = 5.2V).

plotted, and the avalanche multiplication has the similar exponential dependence on V_{CB}. The $M-1$ was higher than that of the HBTs on SOI due to its higher collector doping.

3.6 Self-heating

Self-heating is a known disadvantage in all SOI technologies, especially for those using very thin SOI films [48]. In a bulk SiGe HBT, heat is quickly spread through the subcollector into the silicon substrate. For a SiGe HBT on SOI, however, this heat transfer path to the Si substrate is effectively blocked by the buried oxide layer, which has a much lower thermal conductivity. Self-heating degrades not only the performance of the transistor, but also potentially jeopardizes its long-term reliability [49]. Fig. 36 shows the *dc* vs pulsed constant base-emitter voltage output characteristics, clearly demonstrating that self-heating is significant once the power dissipation density reaches 5 mW/μm^2. In circuits that require accurate matching, additional thermal simulation is often necessary to account for self-heating effects. The self-heating characteristics of these SiGe HBTs on SOI as a function of substrate bias were measured using the techniques in [33] and [50]. This thermal resistance extraction method makes two important assumptions: a) V_{BE} is a linear function of ambient temperature; b) V_{BE} varies linearly with dissipated power when the dissipated power is increased by increasing V_{CB}. More details about thermal resistance extraction are explained in Appendix B.

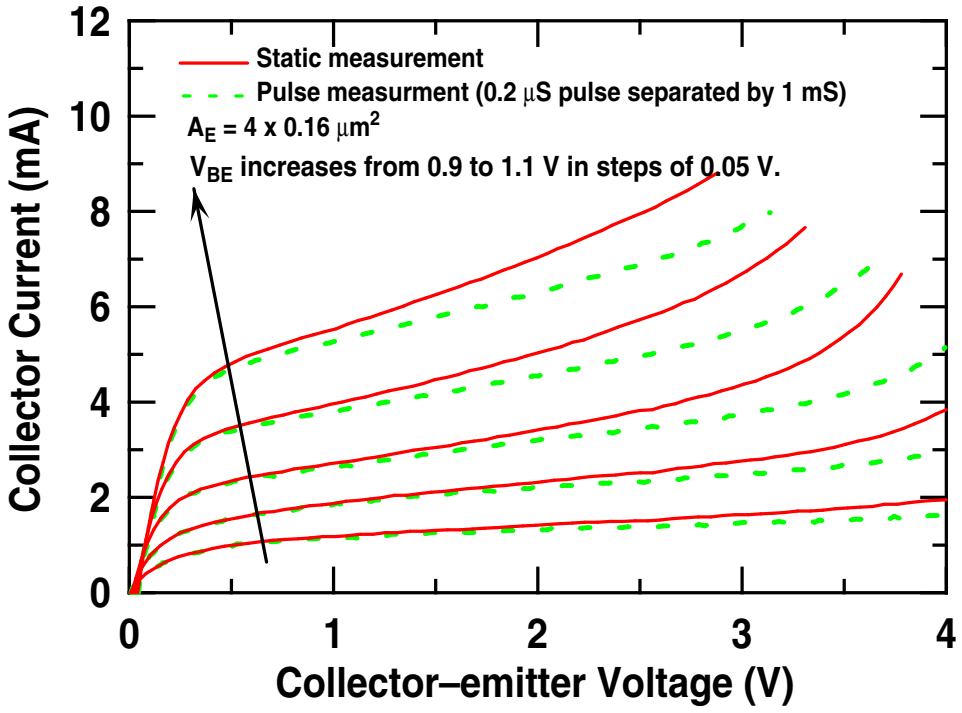

Figure 36: Self-heating effects in a SiGe HBT on SOI (dc vs. pulsed operation).

Fig. 37 shows the temperature dependence of V_{BE} and V_{BE} as a function of dissipated power. In Fig. 37, V_{BE} demonstrates that there is a fairly linear relationship for both ambient temperature and dissipated power across the substrate bias range, validating our extraction technique. The extracted thermal resistances for two different emitter sizes are plotted in Fig. 38. The thermal resistances for both transistors increase by about 20% when the substrate bias increases from -10 V to 20 V. The thermal resistances for their two bulk counterparts are 9,000 K/W and 5,500 K/W, respectively. As discussed above, the collector current flows closer to the Si-buried oxide interface with an increase of the (positive) substrate bias, and the buried oxide serves as an effective trap for this (local) generated heat, thus increasing the thermal resistance.

3.7 Device reliability

"Mixed-mode" stress (simultaneously forcing high J_E and high V_{CB}) is a time-dependent stress methodology for investigating reliability degradation in SiGe HBTs under more realistic operating conditions than conventional reverse EB stress techniques [36]. During the stress, J_E was fixed at 31.25 mA/μm^2 (current overstress) and the substrate was biased at 0V, 5V, and 20V. Typical

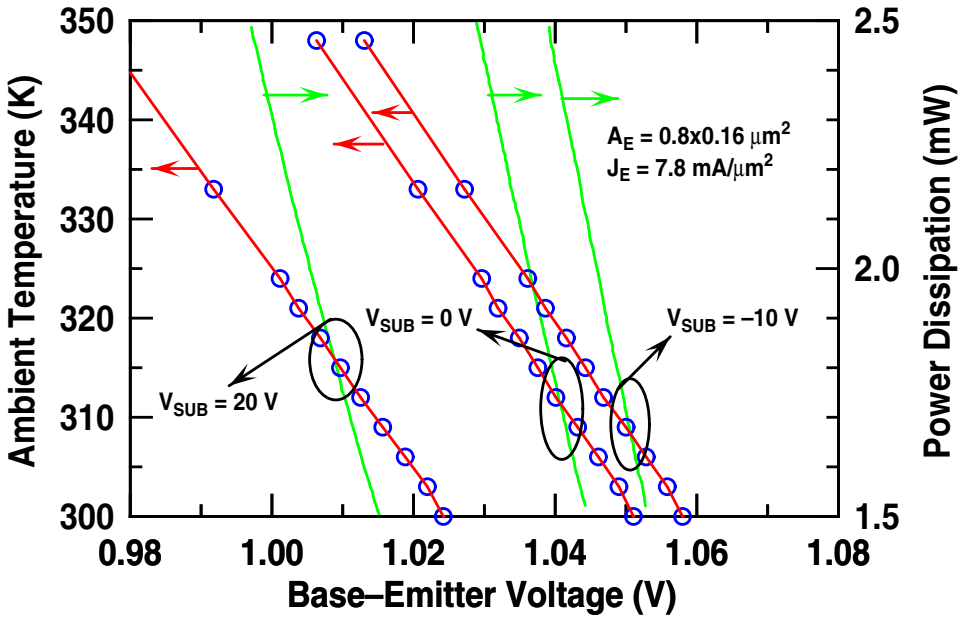

Figure 37: Temperature dependence of V_{BE} and V_{BE} vs. power at different V_{Sx}.

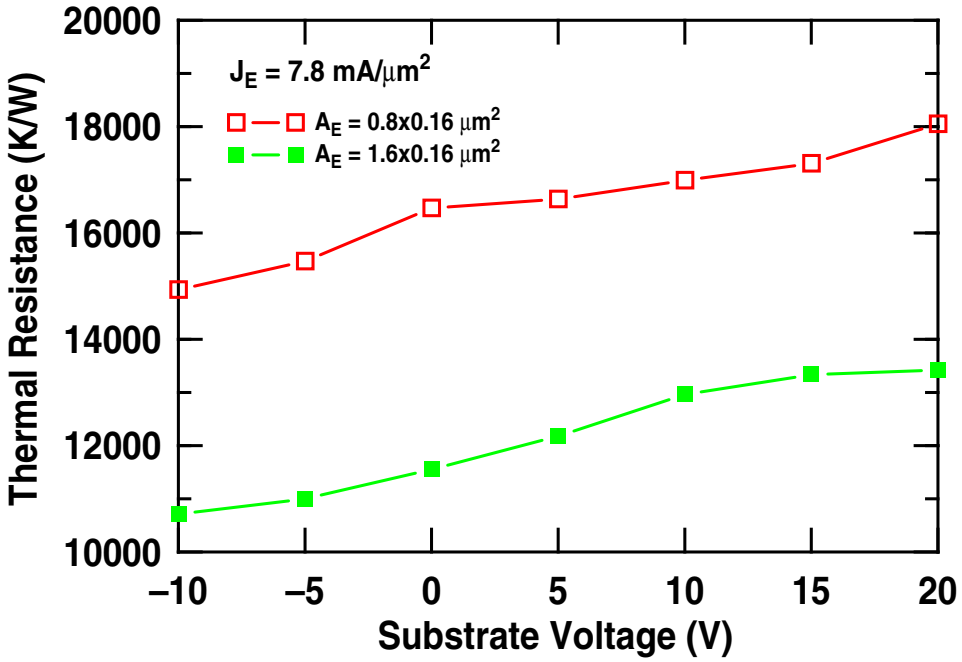

Figure 38: Thermal resistance as a function of V_{Sx}.

Gummel characteristics with increasing stress time at zero substrate bias are shown in Fig. 39. It can be seen from Fig. 39 that the collector current is not affected by the mixed-mode stress, while the base current increases significantly at both low V_{BE} ($V_{BE} < 0.8$ V) and high V_{BE} ($V_{BE} > 0.9$ V).

The excess base current leakage at low V_{BE} is associated with hot carrier damage at the $Si - SiO_2$ interface of the EB spacer. The increase of base current at high V_{BE} is consistent with an increase in quasi-saturation due to a post-stress collector resistance increase. Fig. 40 shows the stress-induced

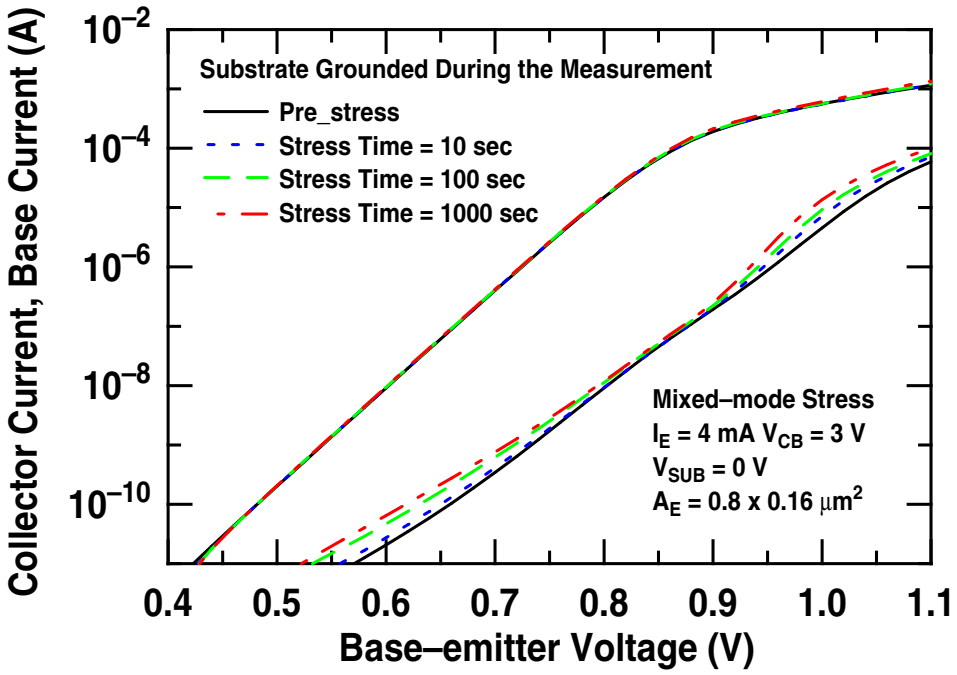

Figure 39: Gummel characteristics for mixed-mode stress with $V_{Sx} = 0$V.

excess base current at fixed V_{BE} versus stress time for mixed-mode stress at substrate biases of 0V, 5V, and 20V. The base current leakage increases with stress time, and is lower for the same stress time for a higher substrate bias. This is clearly good news for positive substrate bias operation of these SiGe HBTs on SOI. The device degradation depends on the number of injected hot carriers and the energy of the hot carriers present at the $Si-SiO_2$ interface. As discussed above, the electric field (and hence the carrier energy) at the EB junction is higher for a larger substrate bias. We believe that for a positive substrate bias, the change of current flow towards the electron accumulation region at the SOI interface effectively produces a lower density of hot carriers at the $Si - SiO_2$ interface, and is supported by simulation. With increasing substrate bias, the decrease of the number of hot carriers dominates the increase in average carrier energy. As such, the excess base current leakage at low V_{BE} is smaller for mixed-mode stress with a higher substrate bias. During mixed-mode stress, the hot carriers damage the SOI interface, resulting in a post-stress collector resistance increase.

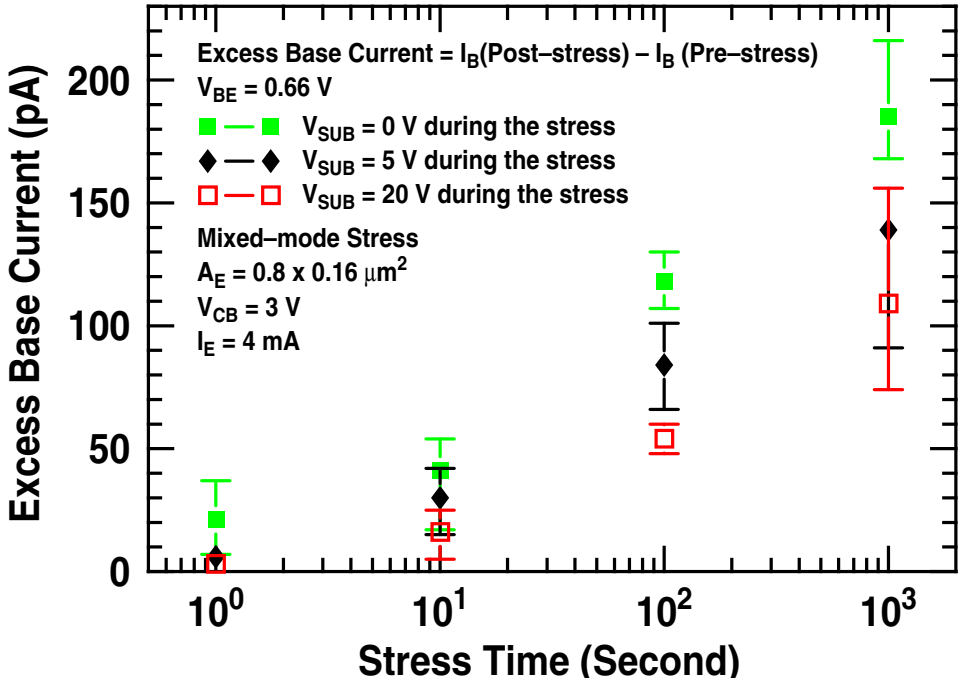

Figure 40: Excess base current at V_{BE} = 0.66V vs. stress time for mixed-mode stress at various V_{Sx}.

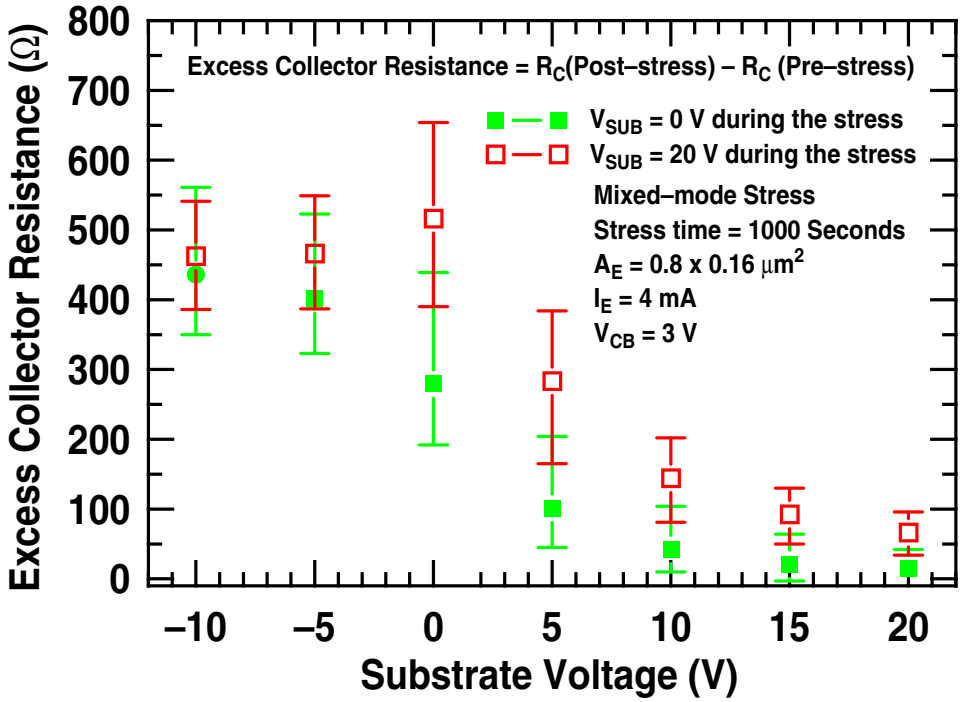

Figure 41: Excess R_C vs. V_{Sx} with V_{Sx} biased at 0V and 20V during the stress (1,000 second stress).

Fig. 41 shows the excess R_C vs. V_{Sx} for 1000-second mixed-mode stress with substrate biased at 0 and 20 V. It can be seen from Fig. 41 that for transistors stressed with a 0V substrate bias, the excess R_C measured post stress is significant for zero and negative substrate bias. However, the corresponding excess R_C measured post stress for a high positive substrate bias is negligibly small. Assuming that R_C is dominated by the intrinsic collector resistance at high positive substrate bias, the hot-carrier-introduced damage is mainly in the extrinsic collector for transistors stressed with 0V substrate bias. The excess R_C measured post stress across the substrate bias range for transistors stressed with 20V substrate bias is slightly higher than those stressed with 0V substrate bias. During 20V stress, the carrier energy is higher than for 0V stress case in the intrinsic collector, and the hot carriers thus cause damage in both intrinsic and extrinsic collector.

3.8 ECL ring oscillator

The circuit performance can also benefit from the improved device speed with increasing V_{Sx}. Fig. 42 shows the output waveform of an ECL ring oscillator made by vertical HBT on SOI. The collector switching current is fixed at 0.74 mA with V_{Sx} of Vcc (the power supply voltage, 1.5 V), 5 V, and 15 V. With the increase of V_{Sx}, there is only a minimal change of the logic swing, while the period decreases, suggesting a significant reduction in the gate delay time. The calculated ECL delay time per stage at various V_{Sx} are shown in Fig. 43. The *dc* bias was varied to modulate the collector switching current from 1.7 mA for a logic swing of 560 mV to 0.7 mA for a logic swing of 260 mV. As V_{Sx} increases from Vcc to 20V, the delay time per stage decreases from 150 psec to 60 psec for an Ic of 1.7 mA, and from 55 psec to 20 psec for an Ic of 0.7 mA.

3.9 Design implications

Interestingly, the speed-breakdown tradeoff in bipolar devices can be fundamentally altered for SiGe HBT on SOI devices when the substrate is treated as an active bias terminal for device/circuit operation. The speed (f_T) can be significantly increased by a positive substrate bias, which induces an accumulation subcollector (peak f_T increases from 37 GHz to 60 GHz for V_{Sx} of 0V to 20V, respectively), but the BV_{CEO} simultaneously decreases due to the increase of $M-1$ (BV_{CEO}

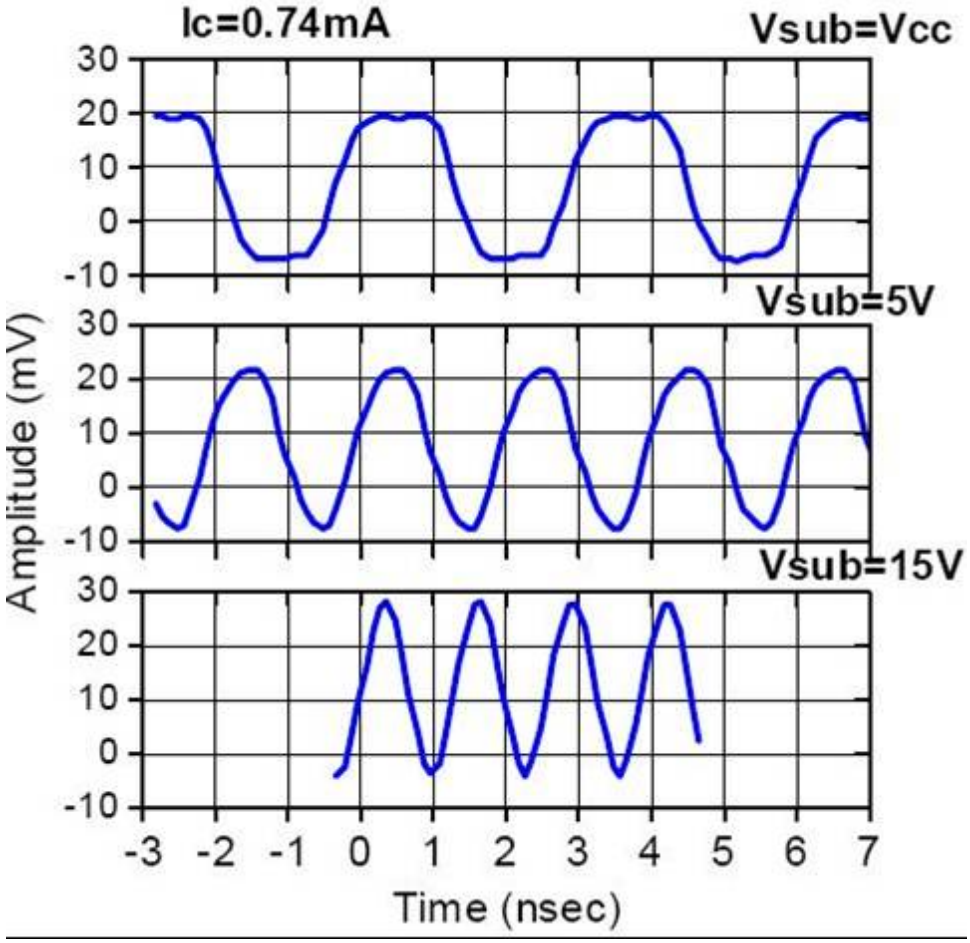

Figure 42: Output waveform of a ECL ring oscillator incorporating vertical HBTs on SOI at various V_{Sx}.

decreases from 4.7V to 2.3V for V_{Sx} of 0V to 20V, respectively). Clearly a design tradeoff is suggested. BV_{CEO} depends largely on $M-1$ for a fixed β, and it is thus possible to increase BV_{CEO} significantly by reducing β (by EB and/or Ge profile engineering) to a value such that the $M-1$ needed for breakdown is equal or above the "flat" portion shown in Fig. 33 at a given substrate bias. Increasing the substrate bias to improve f_T, however, can aggravate the (already serious) self-heating characteristics. Optimized thermal design using robust layout techniques must therefore be carefully considered. Clearly, needing 20V of substrate bias is problematic for circuit/system design. However, with the continued technology scaling of SOI CMOS, the buried oxide thickness for future SOI generations will decrease (to perhaps as low as 20 nm). For a SiGe on SOI device with

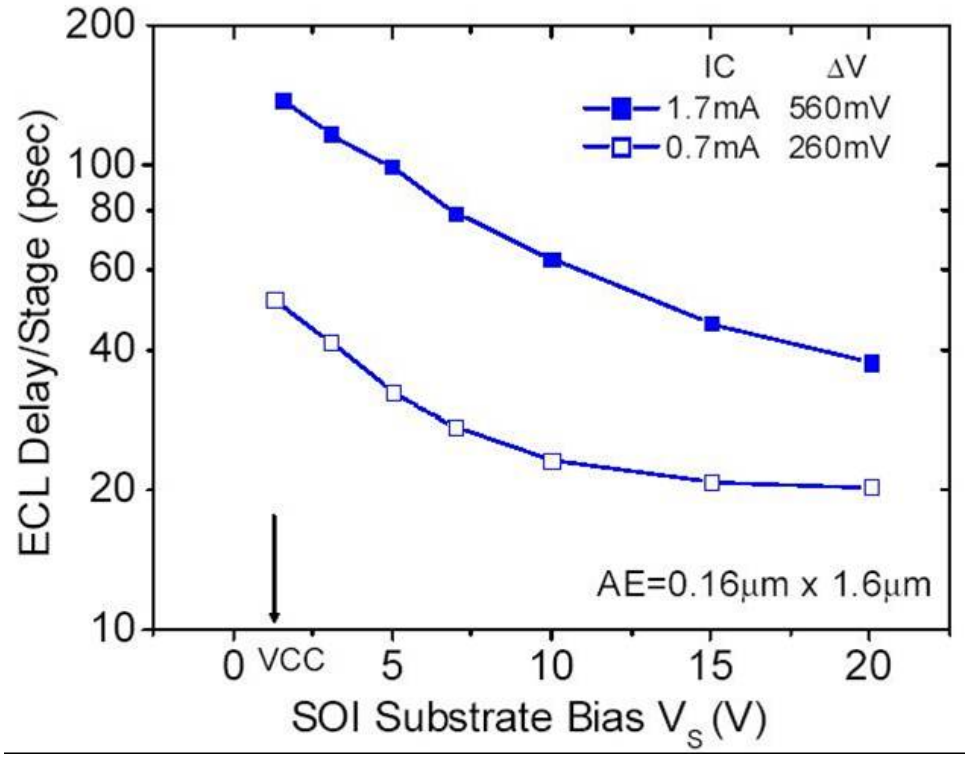

Figure 43: ECL ring oscillator delay at various V_{Sx}.

such a very thin buried oxide, simulations suggest that a supply voltage of 3V would be sufficient to bias the substrate and form the accumulation subcollector needed to minimize R_C. In addition, the use of an n^+ substrate instead of p^+ would further decrease the required substrate bias by about 1V.

CHAPTER IV

PROTON RADIATION EFFECTS IN VERTICAL SIGE HBTS FABRICATED ON CMOS-COMPATIBLE SOI

4.1 Introduction

Silicon-on-insulator (SOI) CMOS technology has matured over the past 15 years to join the mainstream of electronic devices [15]. The most useful SOI properties are a direct result of the ability of SOI to both provide total electrical isolation and at the same time to reduce active semiconductor volume. The thin oxide-isolated silicon layer allows a reduction in device parasitic, a built-in higher operating voltage capability, a reduction in signal cross-talk, improved soft error immunity, and an elimination of latchup [42]. Many wireless and communications applications are best served by having both RF/analog functions using that use bipolar transistors as well as low power digital functions from CMOS transistors on the same package (or die). BiCMOS is often the preferred technology platform and SiGe HBT BiCMOS, in particular, has proven to be an extremely attractive option. From a space electronics perspective, SiGe technology offers an advantageous built-in total dose tolerance [51], although has proven susceptible to single event upset [14]. Clearly, placing SiGe HBTs on SOI, particularly thin film CMOS-compatible SOI, is an attractive option in the context of SEU and SiGe. Achieving the best of SiGe and SOI has proven exceptionally difficult in practice, however. The challenge for achieving SOI BiCMOS integration arises from the fundamental device architectural differences between SiGe HBT and CMOS transistors, since bipolar transistors need thick sub-collectors to maintain low parasitic collector resistance, and this is incompatible with thin-film SOI CMOS technologies. Past approaches to SOI BiCMOS integration used either a thick silicon layer on a bonded SOI substrate to accommodate the vertical bipolar transistors, or lateral bipolar transistors on thin film SOI, both of which can result in a significant performance loss of the HBT. Recently, however, novel vertical SiGe HBTs suitable for integration on CMOS-compatible SOI were demonstrated on 120nm SOI [43]. We present here,

for the first time, an investigation of the impact of 63 MeV protons on SiGe HBTs fabricated on CMOS-compatible SOI.

4.2 Vertical HBT on SOI

The SiGe HBTs used in this work feature a 120 nm silicon layer with an average collector doping concentration of 1.5 x 10^{17}/cm^3 on top of a 140 nm buried oxide layer [43]. Fig. 25 shows the SEM cross-section of a vertical SiGe HBT on CMOS-compatible, thin-film SOI. The substrate is used as an active terminal in this device. The collector region of the SiGe HBT on the SOI is effectively bent by 90 degrees such that the carrier transport in the collector is horizontal for part of its current flow path. Under forward active bias, the carriers flow horizontally from the depleted collector region to the collector reachthrough.

4.3 Radiation Experiment

63.3MeV proton irradiation of the SiGe HBTs was performed at the Crocker Nuclear Laboratory at the University of California at Davis, to fluences as high as $5x10^{13}$ p/cm^2 (equivalent to 6.8 Mrad(Si)). The dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. The radiation source (Ta scattering foils) located several meters upstream of the target establish a beam spatial uniformity of about 15% over a 2.0 cm radius circular area. Beam currents from about 20 nA to 100 nA allow testing with proton fluxes ranging from 1.0×10^9 to 1.0×10^{12} proton/cm^{2}sec. The dosimetry system has been previously described [52] [53], and is accurate to about 10%.

The SiGe HBT *dc* and *ac* test structures were irradiated with the emitter, base, and collector terminals grounded at four different proton fluences of 1.0×10^{12}, 7.0×10^{12}, 2.0×10^{13}, and 5.0×10^{13} p/cm^2, respectively. The HBTs used in this work have the same emitter width (0.16 μm) but two different emitter lengths (0.8 and 1.6 μm). In-situ *dc* measurements were immediately performed on an Agilent 4155C Semiconductor Parameter Analyzer after each proton fluence. Wirebonding of *ac* test structures is not compatible with robust broadband measurements, and hence on-wafer probing of S-parameters was used to characterize the high-frequency performance. The transistor S-parameters were measured using an Agilent 8510C Vector Network Analyzer (VNA) both pre-

and post-proton irradiation, and the corresponding f_T and f_{max} values were extracted. The substrate was biased at 0, 5, and 20 volts during proton exposure.

4.4 Radiation Effects

Figure 44 shows the forward-mode Gummel characteristics of the SOI SiGe HBT at different proton fluences. The base current at low V_{BE} increases monotonically with proton fluence, a classical signature of radiation-induced damage in the emitter-base spacer region. Proton irradiation is known to create generation-recombination (G/R) trap centers near the emitter-base spacer oxide and shallow-trench isolation edges [54], and this leads to the observed increase of base current leakage in these SiGe HBTs. It is interesting to note that at high V_{BE} (>0.9 V) the base current decreases as the proton fluence increases, while the collector current increases with proton fluence. There are two possible mechanisms that may be responsible for this: a) a decrease in the quasi-saturation effects through the decrease of the collector resistance, or b) a delay in the onset of the Kirk effect (base push-out) [55]. The common-emitter output characteristics for the SOI SiGe HBT are shown in Figure 45, both before and after proton irradiation. The collector resistance can be estimated from the inverse of the slope at low collector-emitter voltages (in the saturation region). It can be seen from Figure 45 that the collector resistance decreases as the substrate bias increases, consistent with the substrate effects described in Section 3.3. The post-radiation collector resistance, however, increases for the same substrate voltage compared with the pre-radiation data. This rules out mechanism a) for the observed base and collector current variation at high V_{BE} in the Gummel characteristics. As discussed below, we believe that proton irradiation introduces positive charges in the buried oxide and at the collector-buried oxide interface, which act to retard (reduce) Kirk effect by altering the local electron density and the electric field in the collector-base junction. This was confirmed by examining the simulated electron density distribution under high-injection conditions, as shown in Figure 47. Figure 47 shows that the electron density on the the collector side of collector-base junction depletion region decreases significantly when the interface charge increases from 0 to 1.0×10^{12} C/cm^2. This decrease in the electron density would effectively serve to postpone the onset of base pushout (the Kirk effect).

The measured f_T and f_{max} versus bias current are shown in Figure 46 for a SOI SiGe HBT both

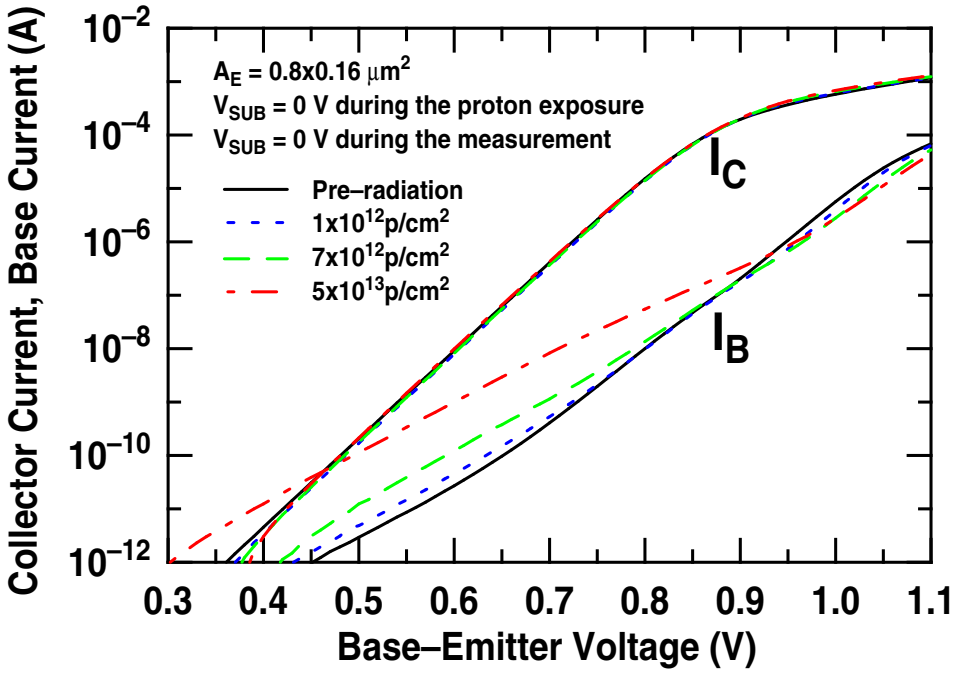

Figure 44: Forward-mode Gummel characteristics of an SOI SiGe HBT at different proton fluences.

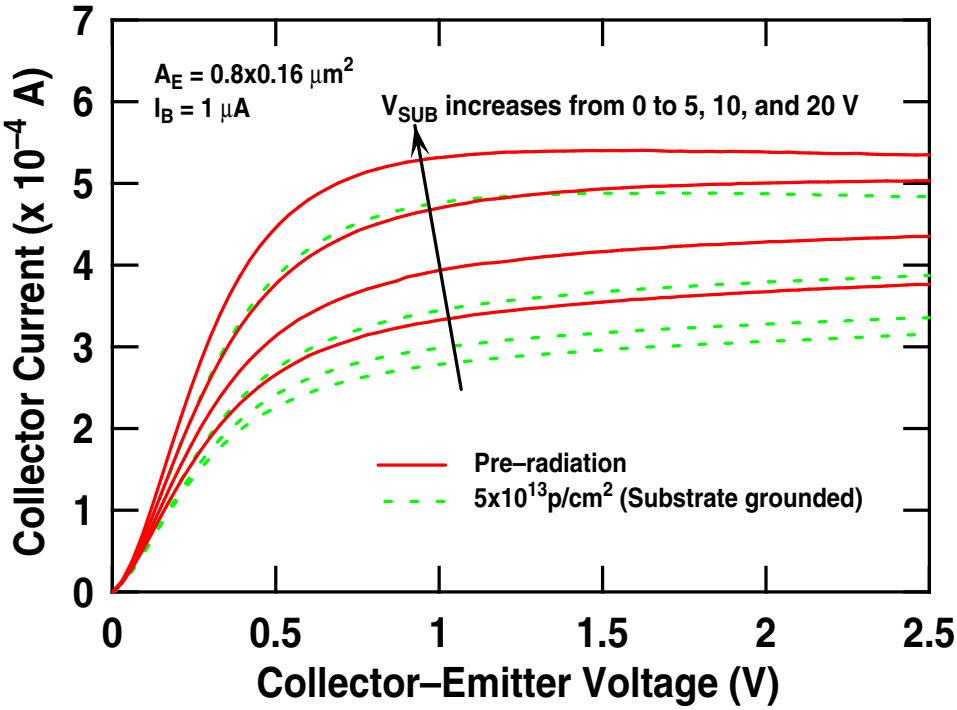

Figure 45: Pre- and post-proton irradiation common-emitter output characteristics of an SOI SiGe HBT.

pre- and post-proton irradiation. Interestingly, the post-radiation peak f_T and f_{max} values increase significantly compared to their pre-radiation values. The scattering-parameters (S-parameters) for the open and short de-embedding structure are essentially identical for pre- and post-radiation samples, and the raw data (without de-embedding) show similar f_T and f_{max} percentage increases, as shown in Figure 46. This indicates that the increase of f_T and f_{max} is not due to any measurement related artifact. From Figure 47, we know that after proton irradiation the onset of the Kirk effect is delayed, increasing f_T at high collector current densities. Figure 48 shows the simulated peak f_T increase at various interface charge densities, indicating that a positive interface charge density of about 1.5×10^{12} C/cm^2 correlates to the observed post-radiation experimental f_T increase. Previous radiation work on SOI CMOS [56] suggests that at a proton fluence of $5x10^{13}$ p/cm^2, the net interface charge introduced by 63 MeV proton irradiation is about 1.7×10^{12} C/cm^2, which is in good agreement with the value inferred in the present work. The value of the forward transit time τ_F, which is comprised of the base, emitter, and collector transit times, was extracted from a plot of $1/2\pi f_T$ versus $1/I_C$ [10]. The extracted forward transit time was found to decrease from 4.64 *psec* for pre-radiation to 2.61 *psec* after proton irradiation, presumably due to the combination of a radiation charge-induced altered current flow path and the retarded Kirk effect.

The measured variation of BV_{CEO} with substrate voltage and proton fluence is plotted in Figure 49. BV_{CEO} is determined by both β and M-1: β decreases with increasing proton fluence due to the radiation-induced base current leakage, while M-1 is a very complicated function of both proton fluence and substrate voltage, as discussed above. At low substrate voltages, the increase of M-1 dominates and BV_{CEO} decreases compared with the pre-radiation value, while at higher substrate biases the increase of M-1 has a smaller effect and the decrease of β begins to dominate, and BV_{CEO} increases. Note that BV_{CEO} for samples with a proton fluence of 5.0×10^{13} p/cm^2 is very large, regardless of substrate bias, due to significant β degradation (i.e., a relatively large base current leakage at $V_{BE} = 0.7$ V). Figure 50 shows the saturated M-1 as a function of substrate voltage for an SOI SiGe HBT for different proton fluences. It is interesting to note that at low substrate voltages, M-1 increases with proton fluence, but it decreases with proton fluence at higher substrate voltages. Based on the depletion approximation, the electric field distribution in the intrinsic transistor is shown qualitatively in Figure 51 for both pre- and post-radiation SOI SiGe

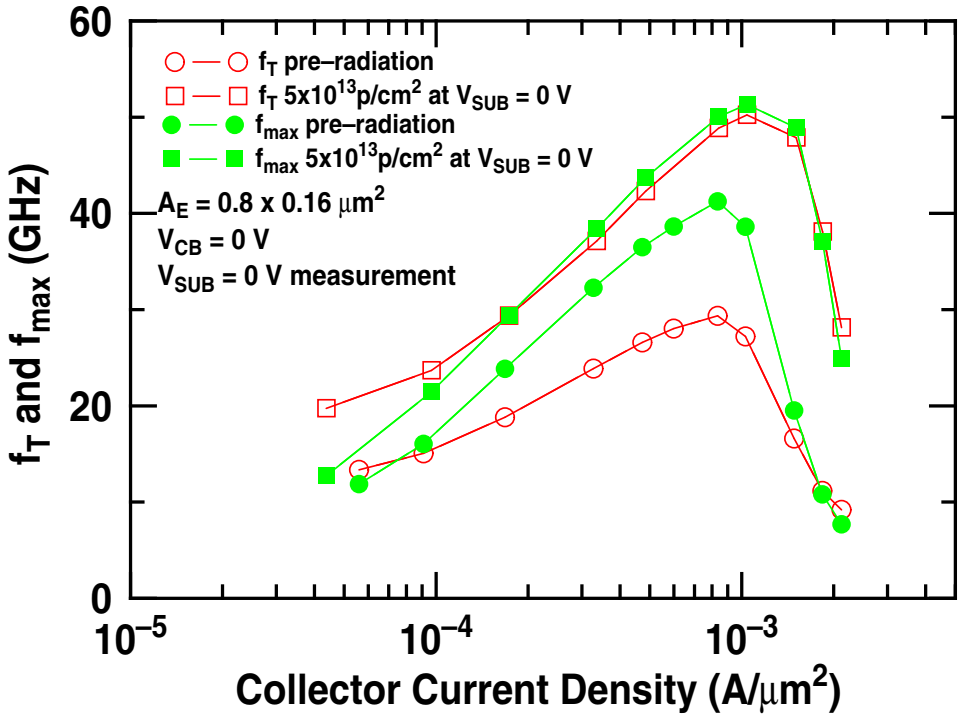

Figure 46: Pre- and post-proton irradiation f_T and f_{max} versus collector current density for an SOI SiGe HBT.

HBTs at different substrate biases. This problem is analogous to a pn diode in series with a MOS capacitor. For Figure 51a, the substrate bias is low and both the pn diode and MOS capacitor are reverse-biased (V_B<V_C, V_S<V_C) and there are two distinct depletion regions, with widths y1 and y2, respectively. With further increases of the collector voltage, the collector becomes fully depleted and the maximum electric field at the base-collector interface, E_{max}, determines the magnitude of M-1. Further increases of the collector voltage will not influence the vertical field or hence, M-1. Proton irradiation introduces positive interface charges at the collector-buried oxide interface, which modulate the electric field in the collector close to the interface, as shown in Figure 51b. E_{max} increases for the post-radiation SiGe HBT compared with its pre-radiation condition, which is consistent with the M-1 data in Figure 50 at low substrate bias. For high positive substrate voltage, the accumulated electron layer switches the electric field in the y2 region to the opposite direction in Figure 51c, as compared with Figure 51a for the low substrate bias. For the case of a post-radiation transistor under high substrate bias, the radiation-induced positive interface charges decrease the electric field in the y2 region and E_{max} is decreased, hence lowering M-1, as shown in Figure 51d

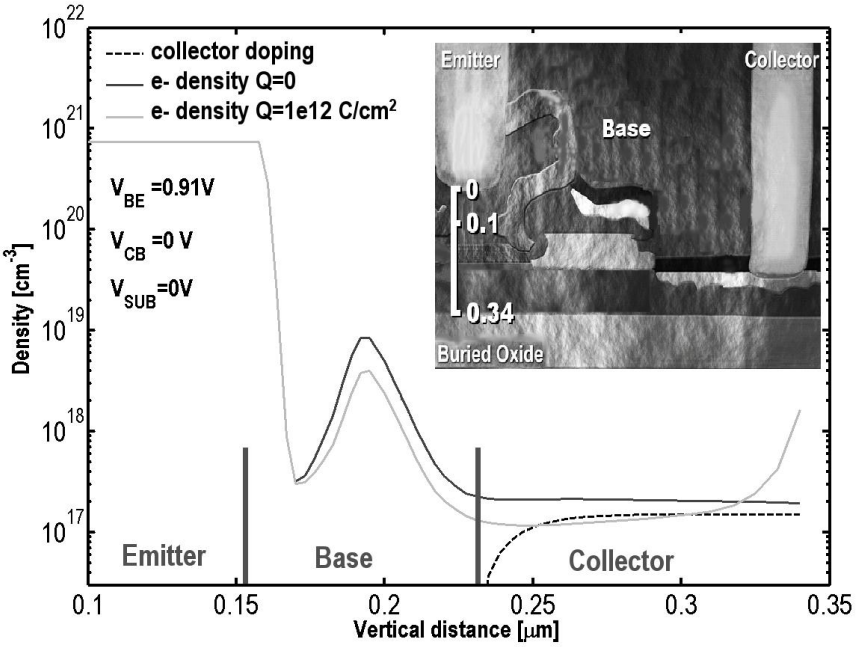

Figure 47: Electron density distribution with and without a positive collector-buried oxide interface charge under high injection conditions.

and Figure 50. 2-D MEDICI simulations support this interpretation.

To understand the effects of transistor geometry and the substrate bias condition during proton irradiation on the radiation response, the excess base currents at different proton fluences, for SOI SiGe HBTs with different geometries and different irradiation substrate bias conditions are compared in Figure 52. The proton-induced base current leakage is similar for the two different transistor geometries and three different substrate bias conditions used during proton irradiation. The radiation response of both BV_{CEO} and M-1 are also very similar across different transistor geometries and substrate bias conditions. Note, however, that this observed lack of geometry dependence is based only on results from HBTs with a grounded emitter, base, and collector during proton exposure, and could in principle be different for devices biased under forward-active conditions (with active substrate bias). The coupling of device bias effects (for all four terminals, namely the emitter, base, collector, and substrate) to the device geometry is currently a subject of further investigation.

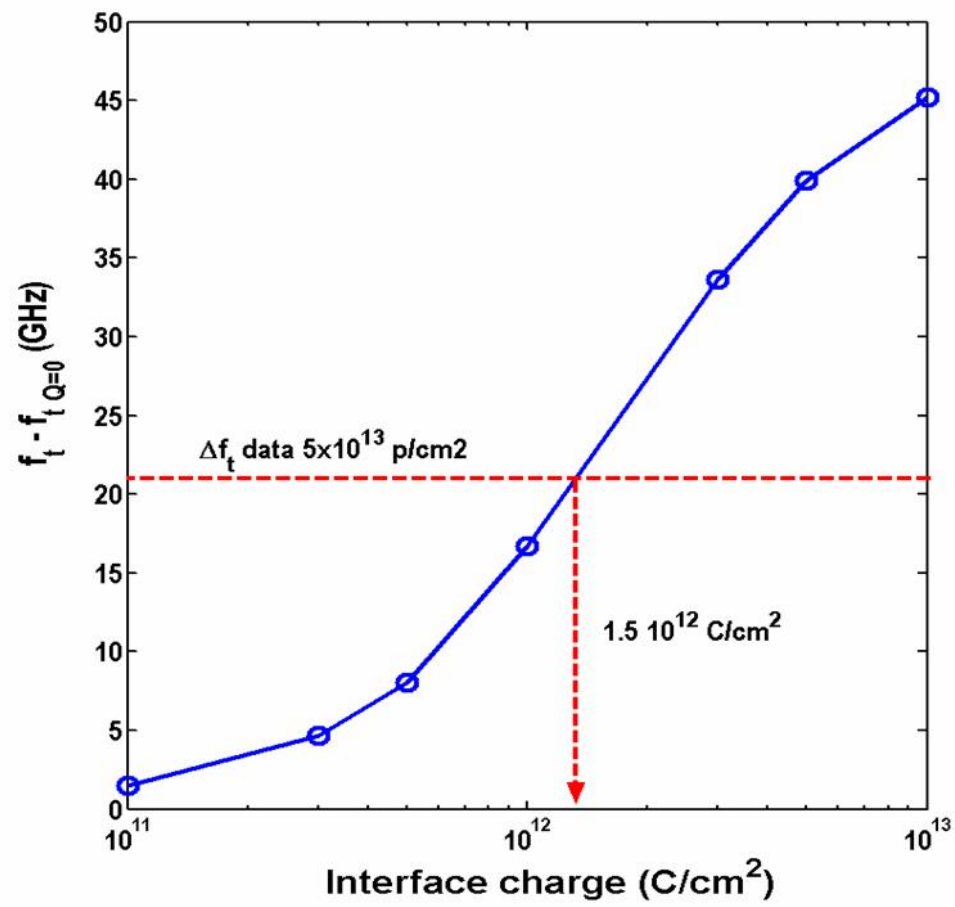

Figure 48: The increase of peak f_T at various interface charge densities simulated by MEDICI.

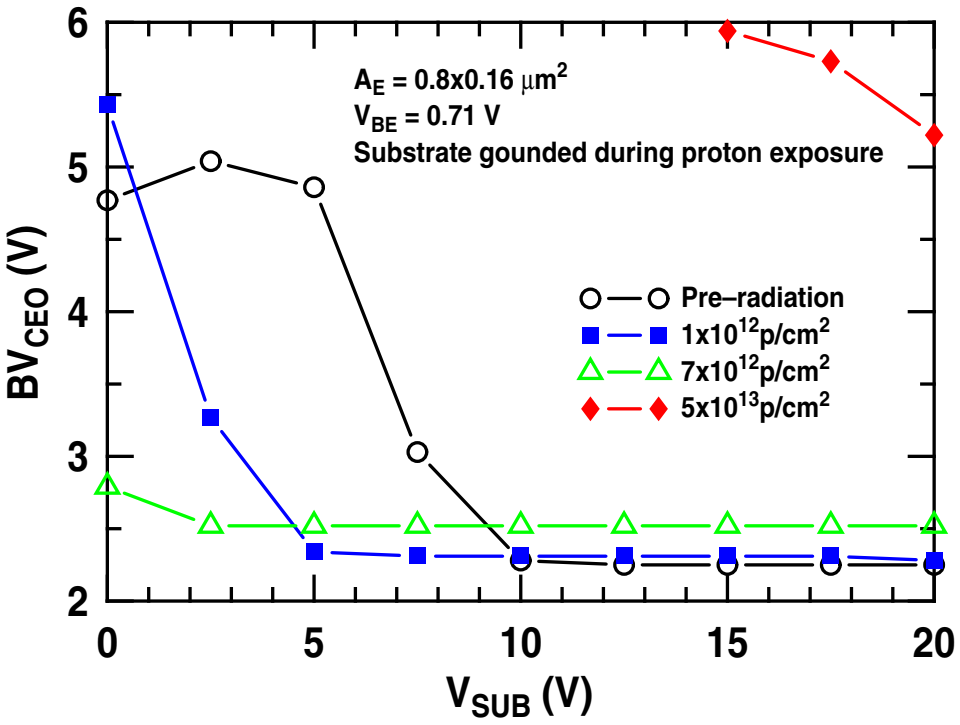

Figure 49: The variation of BV_{CEO} with substrate voltage and proton fluence for an SOI SiGe HBT.

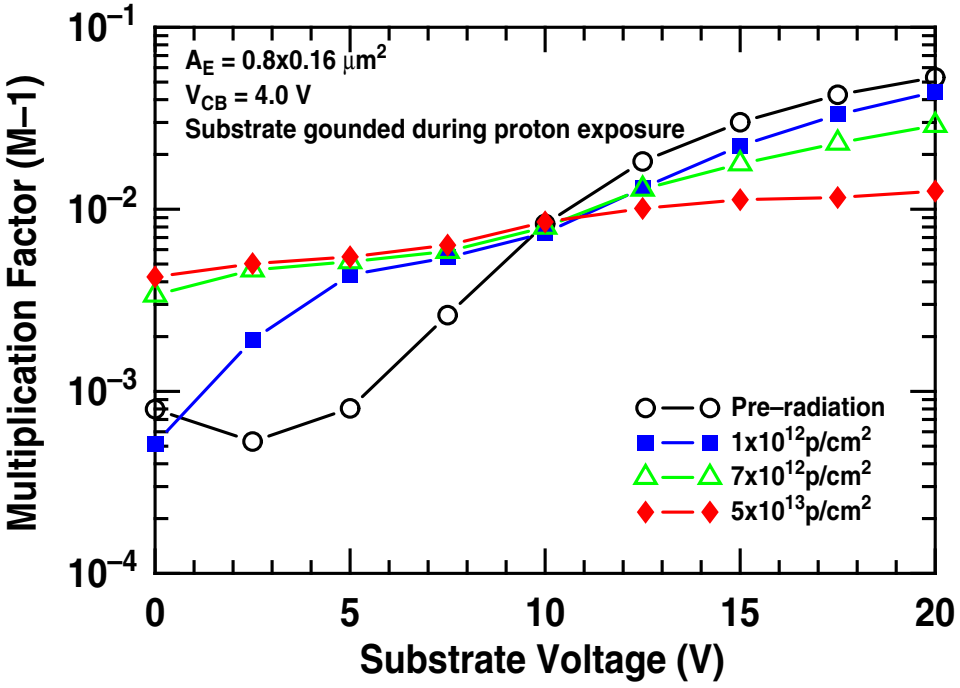

Figure 50: M-1 as a function of substrate voltage for an SOI SiGe HBT for different proton fluences.

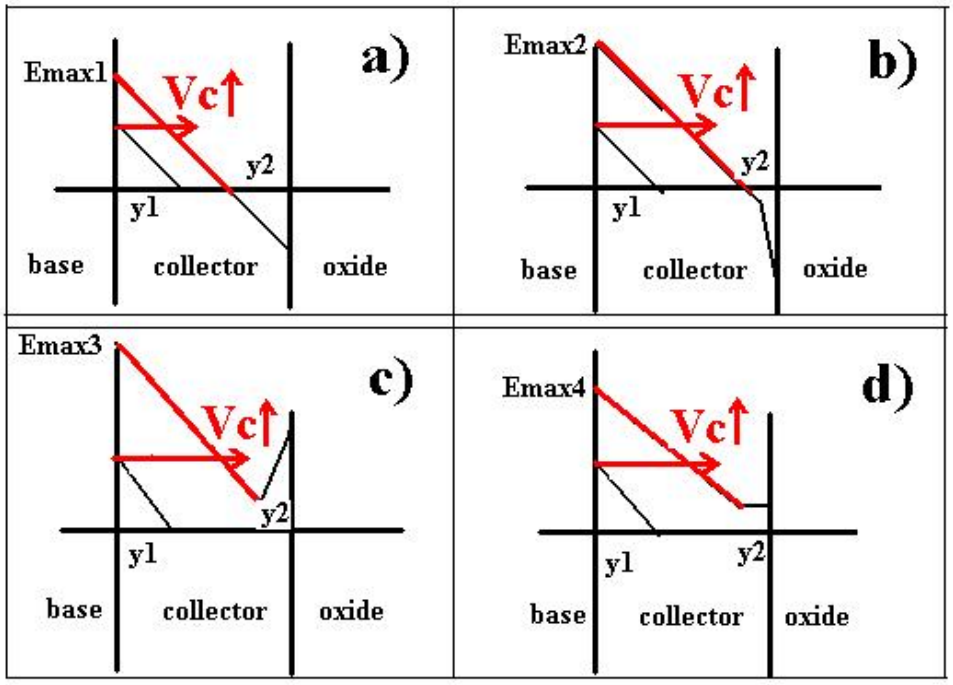

Figure 51: Electric field distributions in the intrinsic transistor: a) pre-radiation, V_{SUB} low; b) post-radiation, V_{SUB} low; c) pre-radiation, V_{SUB} high; d) post-radiation, V_{SUB} high.

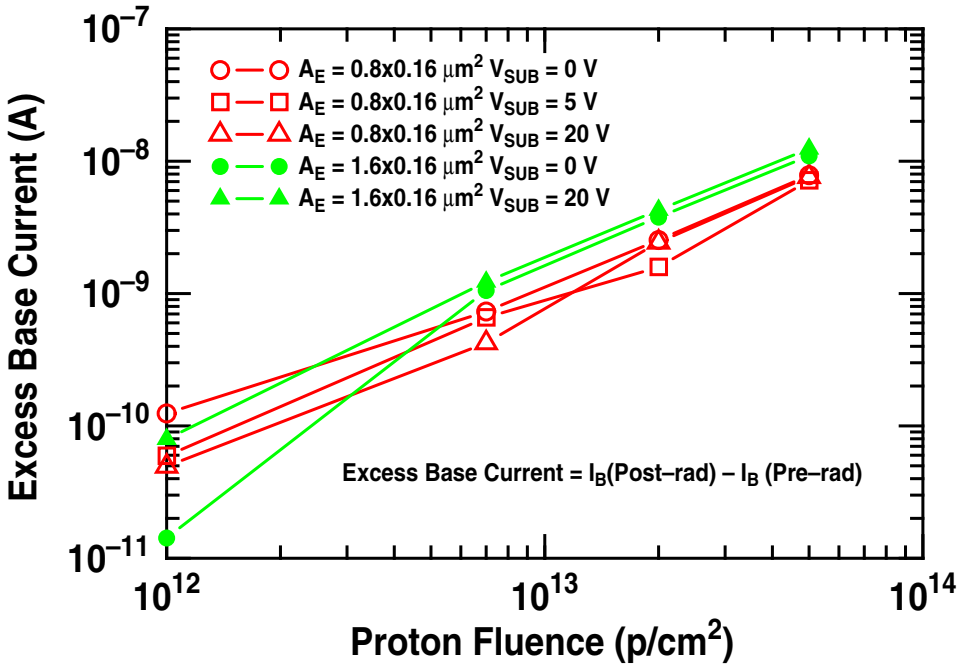

Figure 52: The variation of excess base current with proton fluence for SOI SiGe HBTs with different geometries and different substrate biases during proton irradiation.

CHAPTER V

THE EFFECTS OF RADIATION EXPOSURE AND THERMAL ANNEALING ON STABILITY CONSTRAINTS IN EPITAXIAL SIGE STRAINED LAYERS

5.1 Introduction

Epitaxially-grown SiGe strained layers have found wide application in Si-based bandgap engineering, and have been successfully applied to both HBTs [57], CMOS [58], and optoelectronic devices. Because Si and Ge are not lattice-matched (there is a 4% difference in lattice constant), SiGe alloys of perfect crystallinity are necessarily under compressive strain when grown on a Si substrate. In SiGe HBT fabrication, the SiGe base layer is routinely used to increase β, decrease R_B, increase V_A, reduce noise, and increase f_T, leading to remarkable performance levels for fully-Si-processing-compatible technology ($f_T > 300$ GHz). SiGe films used in SiGe HBTs actually have a three-layer composite structure: a thin, undoped Si buffer starting layer; the actual boron-doped SiGe active base layer; and a thin, undoped Si cap ending layer. Strain "relaxation" (resulting in misfit dislocations and defects) in the SiGe epitaxial layers can result in a break in the crystallinity across the growth interface, which is clearly unacceptable for high-yielding IC applications. SiGe HBTs have been demonstrated to be inherently tolerant to ionizing radiation, thus potentially opening the door for a host of space-borne applications of SiGe devices [59]. A fundamental materials issue in SiGe technology remains unanswered, however, for the intrinsic SiGe base layer: How and to what extent is the SiGe thin film stability affected by radiation? X-ray scattering methods have been developed to determine not only the composition and thickness of thin semiconductor layers, but also to reveal detailed structural information concerning material quality, interface structure, relaxation, defects, surface damage, etc [60]. The present work uses x-ray diffraction techniques to investigate the impact of space-relevant proton-irradiation on the material quality of epitaxial SiGe thin films suitable for use in SiGe HBT design, and examines three different Ge profiles spanning a

range of thermodynamic stability from thermodynamically stable through metastable to overstable. We also present the first comparison of the effects of proton irradiation and thermal annealing on stability in such SiGe thin films.

5.2 Thin film stability

The SiGe base layer thickness is a key variable in SiGe HBT device design. The "critical thickness" is defined as the maximum film thickness that results in pseudomorphic (defect free) growth post-fabrication. Force balance [21] and energy minimization [22] are the two most common approaches to theoretically determining the equilibrium critical thickness of a coherently strained layer. A recent equilibrium model for buried SiGe strained layers has been proposed and shows excellent agreement between theory and experiment for both CVD and MBE grown device-relevant SiGe films. This formalism employs force-balance theory and takes into account of the top Si cap layer on the total strain in the composite structure [23]. Theory predicts that during strained-layer epitaxial growth the formation and glide (movement) of a network of misfit dislocations at the substrate/strained-layer interface become energetically favorable once the thickness exceeds the film critical thickness. It is, however, generally agreed that SiGe films can be grown using certain low-temperature techniques to thicknesses exceeding this theoretical critical thickness forming metastable films without creating misfit dislocations, provided processing conditions post-growth do not exceed the film growth temperature (about 550°C for ultrahigh-vacuum / chemical vapor deposition (UHV/CVD))[61]. As such, SiGe thin films can in principle be grown to several times the theoretical critical thickness forming overstable films without lattice relaxation. Since routine SiGe device and circuit fabrication goes through several unavoidable high-temperature steps (e.g., oxidation and annealing in the range of 900°C), SiGe strained layers which are metastable or overstable as-grown may, however, "relax" (forming defects) during the subsequent device fabrication steps [62]. Stable, metastable, and overstable SiGe thin films were fabricated by UHV/CVD, as shown in Figure 53, and analyzed by x-ray diffraction both before and after exposure to 63 MeV protons. The impact of radiation on these SiGe thin films was then compared with the effect of thermal annealing.

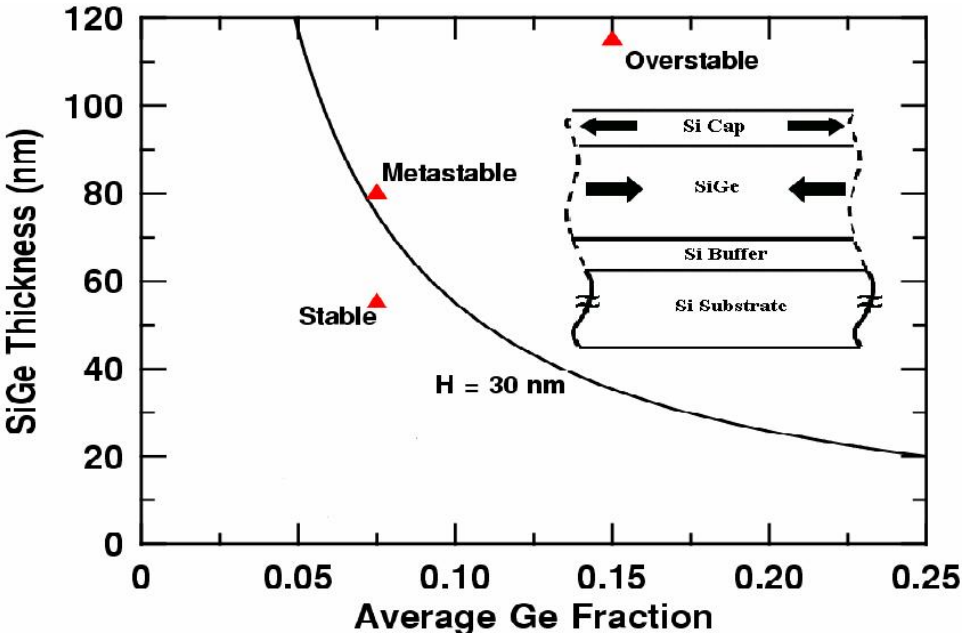

Figure 53: SiGe thermodynamic stability diagram showing the stability points of the SiGe profiles used in this work. The solid line is a theoretical stability constraint curve.

5.3 Experiment

The SiGe thin films were grown on Si (100) using the UHV/CVD technique with exactly the same growth condition as that used in practical SiGe HBT fabrication[63]. Three experimental points in stability space were grown, which for clarity we will term "stable," "metastable," and "overstable", as shown in Figure 53. The Si bottom buffer layer and cap layer thickness were fixed at 30 nm for all films. Ge "box" (constant Ge) profiles were used for ease of comparison. TEM cross-sections were made using standard mechanical "pre-thinning" (10-12 μm thickness) and subsequent formation of an approximately 15 μm wide by approximately 150 nm thick TEM membrane using a focused-ion beam-based (FIB) tool. X-ray diffraction (XRD) can be used to examine in great detail the underlying crystallinity of the films, and to infer the inherent strain present in them. XRD measurements were carried out with a Philips Materials Research Diffractor meter equipped with a rotating Cu anode x-ray source and an asymmetrically cut four-crystal Ge (220) monochromator. The 004 reflections were measured in the triple-axis (TA) mode (i.e., with an analyzer crystal in front of the detector) using $\omega/2\theta$ scans, where ω is the angle between the incident beam and the wafer surface and 2θ is the angle between the incident beam and the detector. The reciprocal lattice

map was obtained by undertaking a series of scans by driving the $2\omega'$ $(= 2\theta)$ and ω axes in a 2:1 ratio and then offsetting ω by a small amount before the following scan. This gives a radial sector of reciprocal space that can then be converted using software to form a reciprocal space image or "map." The 63.3MeV proton irradiation was performed at the Crocker Nuclear Laboratory at the University of California at Davis, with fluences as high as $5x10^{13}$ p/cm^2 (equivalent to 6.8 Mrad(Si) of total ionizing dose).

5.4 Results

5.4.1 As-grown samples

Cross-sectional transmission electron microscopy (TEM) was used to measure the thickness of each layer of the stable, metastable, and overstable as-grown samples. Figure 54 shows the TEM images of the stable, metastable, and overstable samples, indicating no obvious dislocations at the Si/SiGe interfaces. Carefully calibrated Secondary Ion Mass Spectrometry (SIMS) was also used to characterize the layer thicknesses and Ge fraction in the SiGe layers, as shown in Figure 55. Table 3 gives a summary of the measured thickness and Ge fraction of all three types of samples obtained from both TEM and SIMS, which correlate well with their designed nominal values.

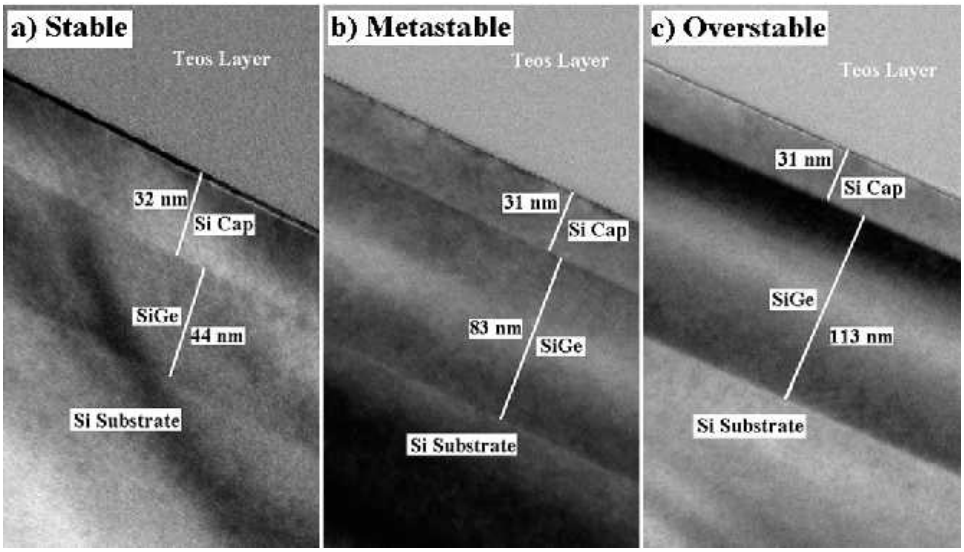

Figure 54: TEM micrographs of the as-grown stable, metastable, and overstable SiGe samples.

Figure 56 shows the 004 x-ray rocking curves for the as-grown stable, metastable, and overstable

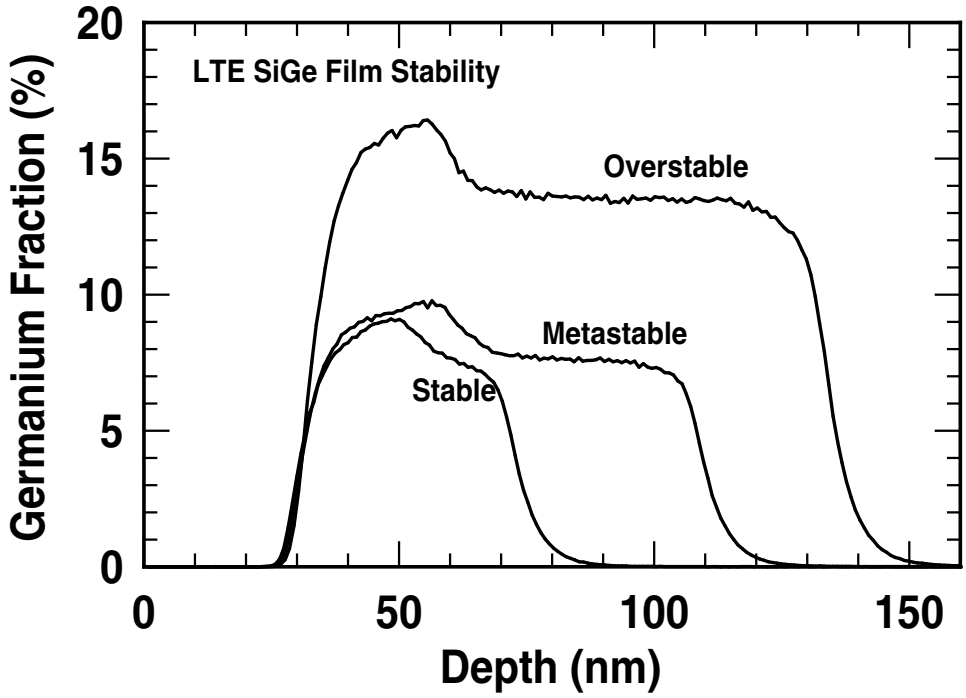

Figure 55: The Ge depth profile measured by SIMS.

samples. The rotation angle is related through Bragg's law to the interatomic spacing:

$$d = \frac{n\lambda}{2sin\theta}, \tag{14}$$

where n is any integer number, λ is the x-ray wave-length. The separation of the SiGe layer peak and the Si substrate peak is related to the difference in the lattice parameters of Si and SiGe. Assuming that the lattice parameter of SiGe alloy follows a known relationship with its composition, the Ge fraction of each sample can be calculated. This direct analysis of x-ray data, however, can lead to significant error because the peak position of the SiGe layer does not necessarily correspond to the peak position expected from Bragg's equation due to the extremely thin nature of the layer [60]. The build-up of the wave-field in the crystal requires a reasonable sustained periodicity to lock into, and for the very thin film samples used in this work this has not been established. Interference fringes observed in the scattering pattern, which arise due to the different optical paths of the X-rays, are related to the thickness of the layers through Equation 15:

$$L = \frac{\lambda}{2(sin\omega_1 - sin\omega_2)} \approx \frac{\lambda}{2\Delta\omega cos\omega}, \tag{15}$$

where ω_1 and ω_2 correspond to the angular positions of the fringe peaks, $\Delta\omega = \omega_1 - \omega_2$, and ω is the

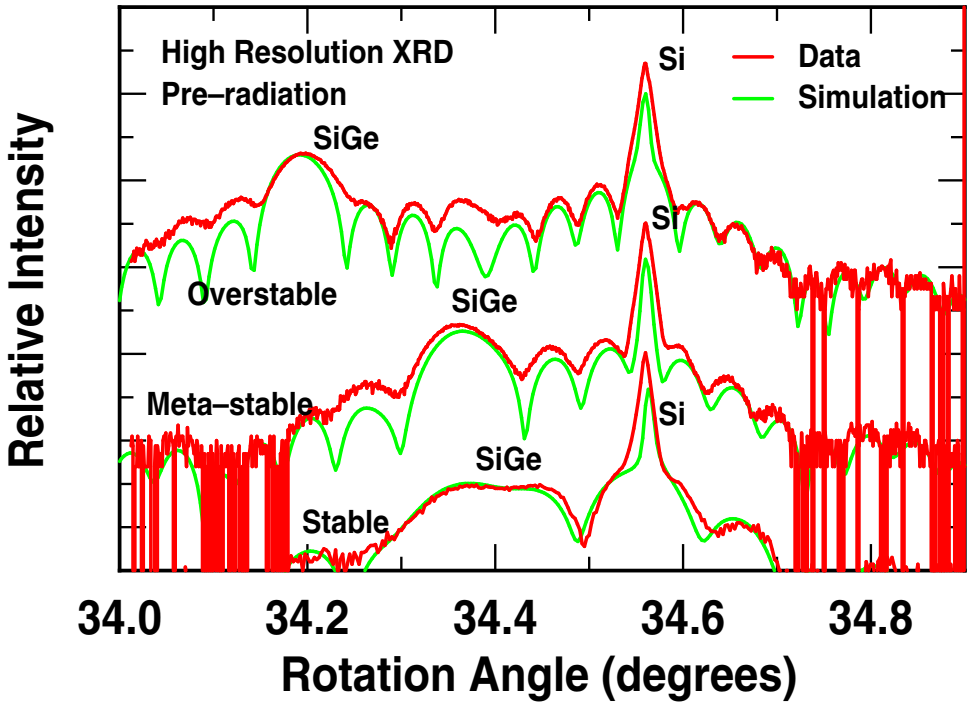

Figure 56: 004 XRD rocking curves of the as-grown SiGe samples, with the upper curve offset for clarity.

average of the two values. The smooth and strong fringe peaks in Figure 56 suggest an extremely high layer interface quality, consistent with the TEM results. Due to the linear relationship between the layer thickness and the fringe frequency, the calculation of the SiGe layer thickness based on the fringe peak separation becomes difficult when the Si cap layer has a comparable thickness to the SiGe layer, since it is impossible to decouple the fringe peaks due to the SiGe and Si cap layers. Dynamical theory considers the whole process of scattering as wave-fields that include all the interactions, and therefore simulation using this theory becomes the most precise way to interpret the data. The experimental rocking curves were fitted through an iterative process with the aid of the "automatic fitting" function of the x-ray software. The simulated curves fit the experimental data very well, as shown in Figure 56. The extracted SiGe thickness and Ge fraction are within 1% of the data from Table 3, demonstrating that x-ray diffraction can be used as a fast, non-destructive materials characterization tool.

Furthermore, more information (e.g., on the strain) can be extracted during the x-ray data-fitting step. The as-grown stable and metastable samples are found to be fully-strained, while the overstable

Table 3: SiGe Film Parameters.

Sample	Stable		Metastable		Overstable	
Analysis	TEM	SIMS	TEM	SIMS	TEM	SIMS
t_{sige}(nm)	44	45	83	80	112	110
Ge(%)	-	7.5	-	7.5	-	14.5

sample is relaxed by about 3%. The degree of relaxation (usually expressed as a percentage, R) is given by

$$\frac{R}{100} = \frac{a_x - a_{Si}}{a_{rel} - a_{Si}}, \tag{16}$$

where a_{Si} is the lattice parameter of the Si substrate, a_x is the in-plane SiGe lattice parameter, and a_{rel} is the lattice parameter of the fully relaxed SiGe layer.

Figure 57 shows the reciprocal space map of as-grown metastable and overstable samples.

The layer and the substrate peaks lie on the same $\omega/2\theta$ scan for both as-grown samples, suggesting that the SiGe layer is not tilted with respect to the substrate. The fringe peaks along the $\omega/2\theta$ scan again indicate the good interface quality of the as-grown samples. The intensity distribution of the SiGe and Si peaks along the ω direction is a joint contribution of the dynamical diffraction streak and the diffuse scattering. The width of the dynamical diffraction streak is inversely proportional to the smaller value of either the coherence width of the x-ray wavefront or the finite lateral dimension of the perfect crystal, while the diffuse scattering arises from the strain fields around the dislocation. The narrow SiGe peak distribution along the ω direction suggests that there is a very low dislocation density for both as-grown samples. The weak dynamic streak in the Si peak along the ω direction is most likely related to the beam properties (wavelength spread) of the hybrid, and may be the tail of the Cu Alpha 2 component.

5.4.2 Radiation Effects

Figure 58 shows the 004 XRD rocking curves of the stable, metastable, and overstable samples following exposure to 63 MeV protons at fluences of up to 5×10^{13} p/cm^2, chosen because this is a worst case radiation level for most orbital space applications.

The post-radiation rocking curves for all three types of samples indicate insignificant shifts in the Ge peaks relative to the Si substrate peaks compared with those of the as-grown samples. This

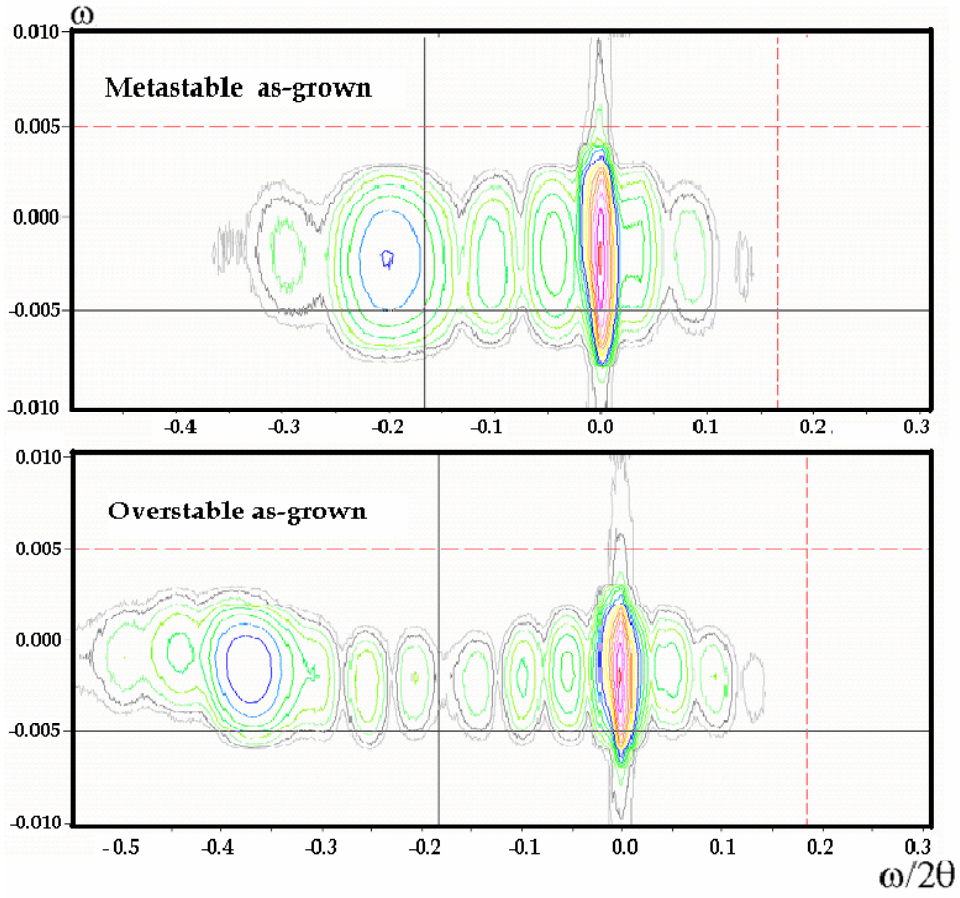

Figure 57: Reciprocal lattice map of post-radiation metastable and overstable samples. The intensity scale is logarithmic with 2x/contour and the most intense contours are at 1.20×10^6 and 1.65×10^6 count/s for the metastable and overstable samples, respectively.

is clearly excellent news, suggesting that this is only a minimal lattice structure change due to the proton irradiation. Figure 59 shows the reciprocal lattice map of post-radiation metastable and overstable samples.

The layer and the substrate peaks center on the same $\omega/2\theta$ scan, suggesting that there is a negligible tilt of the SiGe layer introduced by proton irradiation. The SiGe peaks become broader along the ω direction compared with the as-grown reciprocal lattice map. The full width of half-maximum (FWHM) of the SiGe peak increases from 0.005° to 0.012° for the metastable sample, while that for the overstable sample increases from 0.005° to 0.007°. This result suggests increased diffuse scattering, possibly due to an increased number of dislocations introduced by proton irradiation. The fringe peaks are distorted slightly but there is no significant intensity degradation relative to the

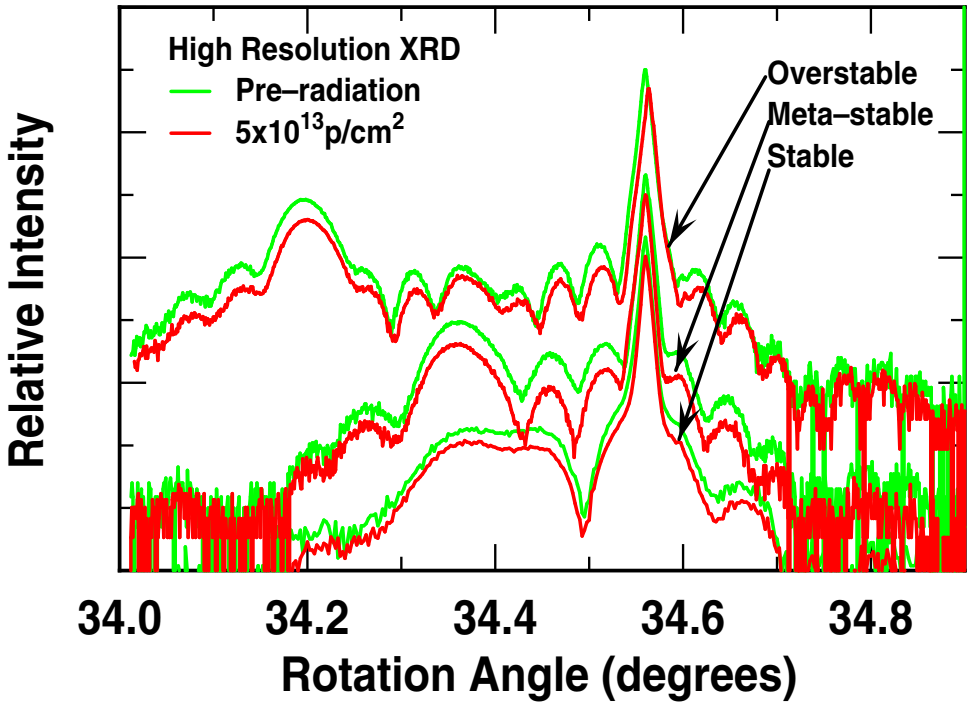

Figure 58: 004 XRD rocking curves of post-radiation samples, with the upper curve offset for clarity.

as-grown samples, suggesting limited damage at the layer interface due to proton exposure.

5.4.3 Thermal Effects

For comparison, we also investigated the impact of thermal annealing on the same SiGe films. Figure 60 and Figure 61 are the 004 XRD rocking curves at different annealing times at 900°C, for the metastable and overstable samples, respectively.

It can be seen from Figure 60 that there is an almost undetectable change in the rocking curves for the metastable samples annealed at 900 °C for up to 75 seconds. The SiGe peak height relative to the substrate peak decreases slightly and shifts to the right by 0.035° when the annealing time increases to 375 seconds, indicating that a substantial amount of relaxation is induced, as expected, since the film is not thermodynamically stable as grown. The fringe peaks do not change significantly even for annealing times up to 375 seconds, and this suggests that the interface remains of high quality during the annealing. Figure 61 shows that for the overstable sample, both the SiGe peak and the fringe peaks' intensities relative to the substrate peak decrease monotonically with

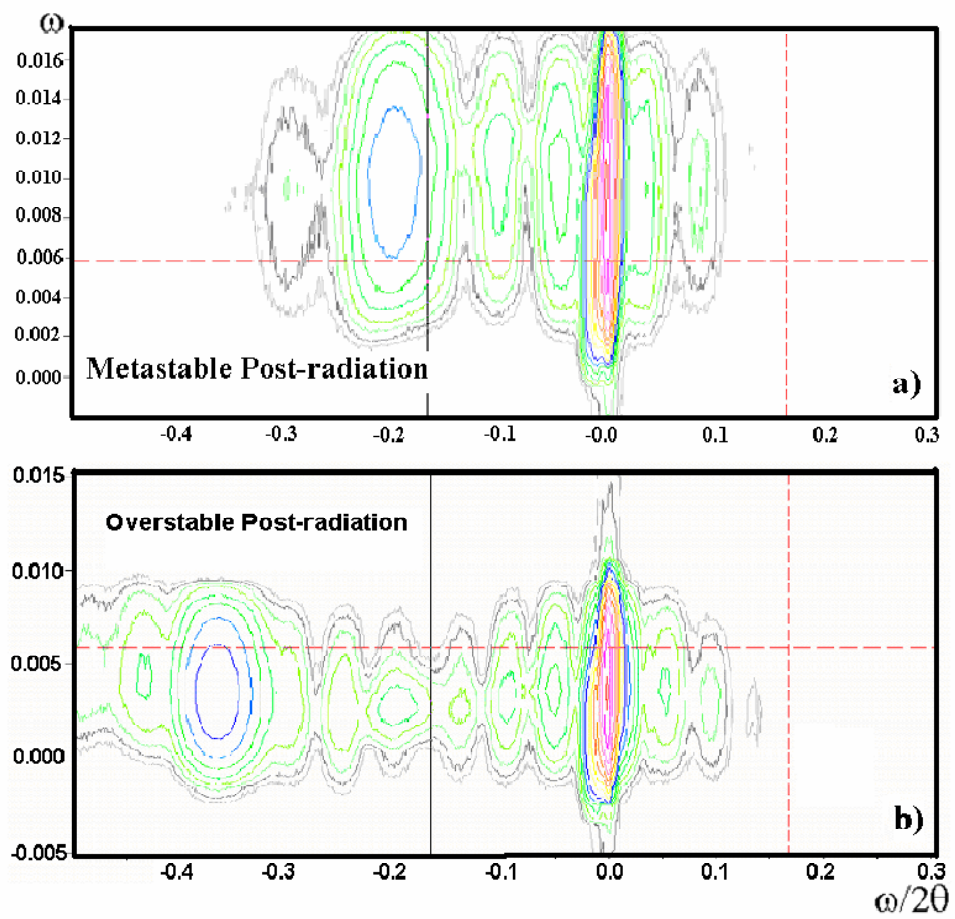

Figure 59: Reciprocal lattice map of post-radiation metastable and overstable samples. The intensity scale is logarithmic with 2x/contour and the most intense contours are at 0.7×10^6 and 1.11×10^6 count/s for the metastable and overstable samples, respectively.

annealing time. When the degree of relaxation is well above the few percent level, the x-ray wavefields are uncoupled at the interface and this will cause a decrease in the height of the SiGe peak. These results suggest that the overstable sample relaxed consistently and faster than the metastable sample during the annealing. The calibrated x-ray simulation models for as-grown metastable and overstable samples were used to simulate the relaxation of both samples during the annealing and the simulation results are summarized in Table 4.

Figure 62 shows the reciprocal lattice maps of the metastable and overstable samples after annealing.

The SiGe layer of the metastable sample is tilted by about 0.001° relative to the bottom Si substrate. The fringe peaks remain clean and strong for the metastable sample and suggest only

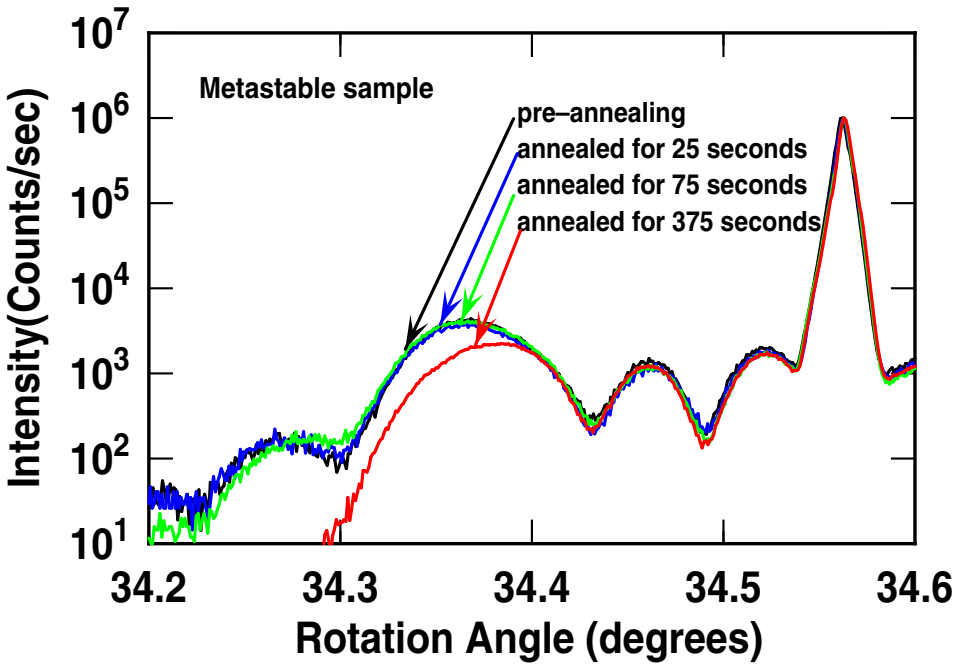

Figure 60: 004 XRD rocking curves of the metastable samples at different annealing times at 900°C.

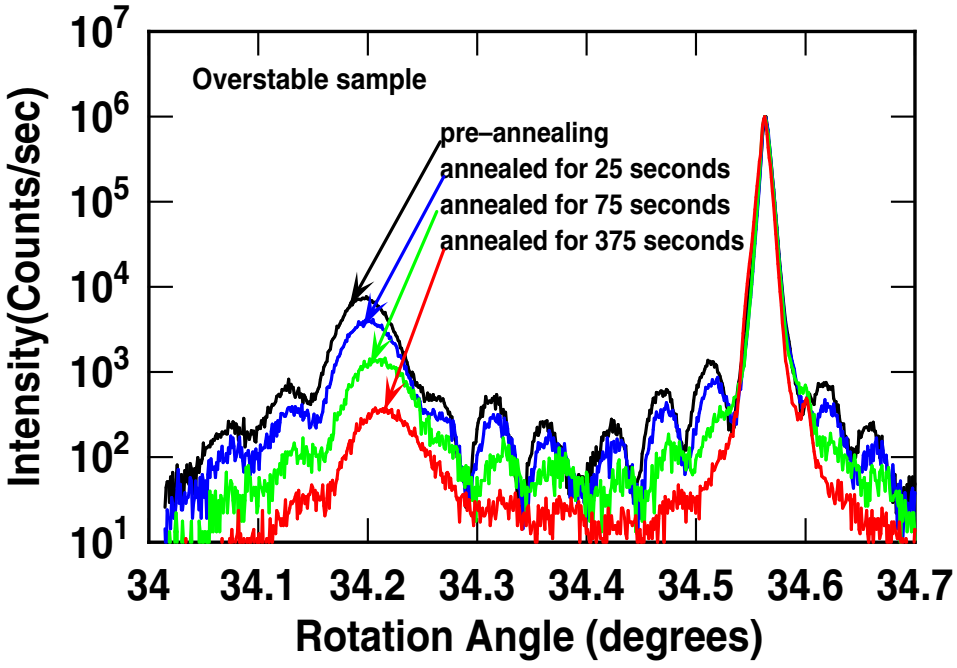

Figure 61: 004 XRD rocking curves of the overstable samples at different annealing times at 900°C.

minor interface degradation occurs due to annealing, consistent with Figure 60. Both the SiGe peak and Si substrate peak broaden considerably along the ω direction, suggesting a huge increase in

Table 4: SiGe relaxation when annealed at 900°C (±1%)

.

Annealing time (seconds)	0	5	25	75	375
Metastable sample	<1%	<1%	<1%	<1%	9%
Overstable sample	3%	6%	8%	13%	17%

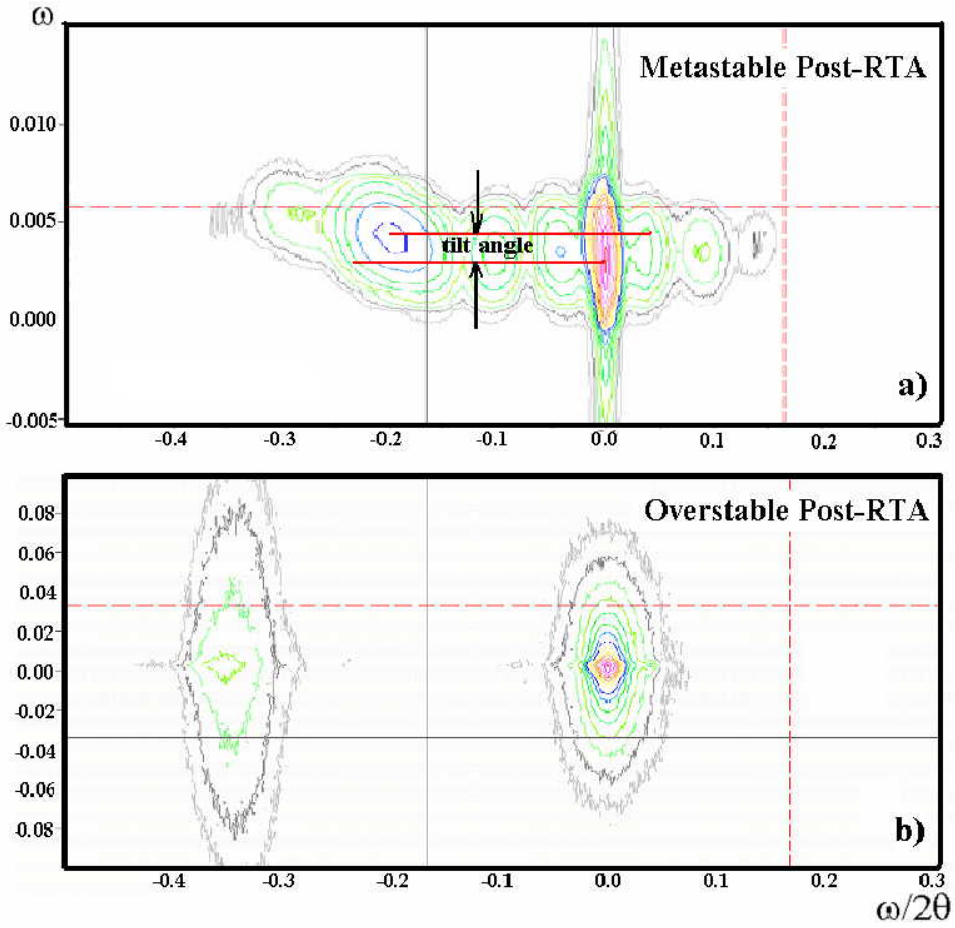

Figure 62: Reciprocal lattice map of post-annealing metastable and overstable samples. The intensity scale is logarithmic with 2x/contour and the most intense contours are at 2.30×10^6 and 1.02×10^6 count/s for the metastable and overstable samples, respectively.

the diffuse scattering. The fringe peaks for overstable samples disappear after annealing at 900°C, indicating significant interface degradation. The tilt between the SiGe layer and the Si substrate cannot be determined due to the very broad SiGe layer peak. TEM micrographs of the metastable and the overstable samples annealed at 900 °C for 375 seconds are shown in Figure 63.

Figure 63a indicates that the metastable sample suffers only minor interface degradation after

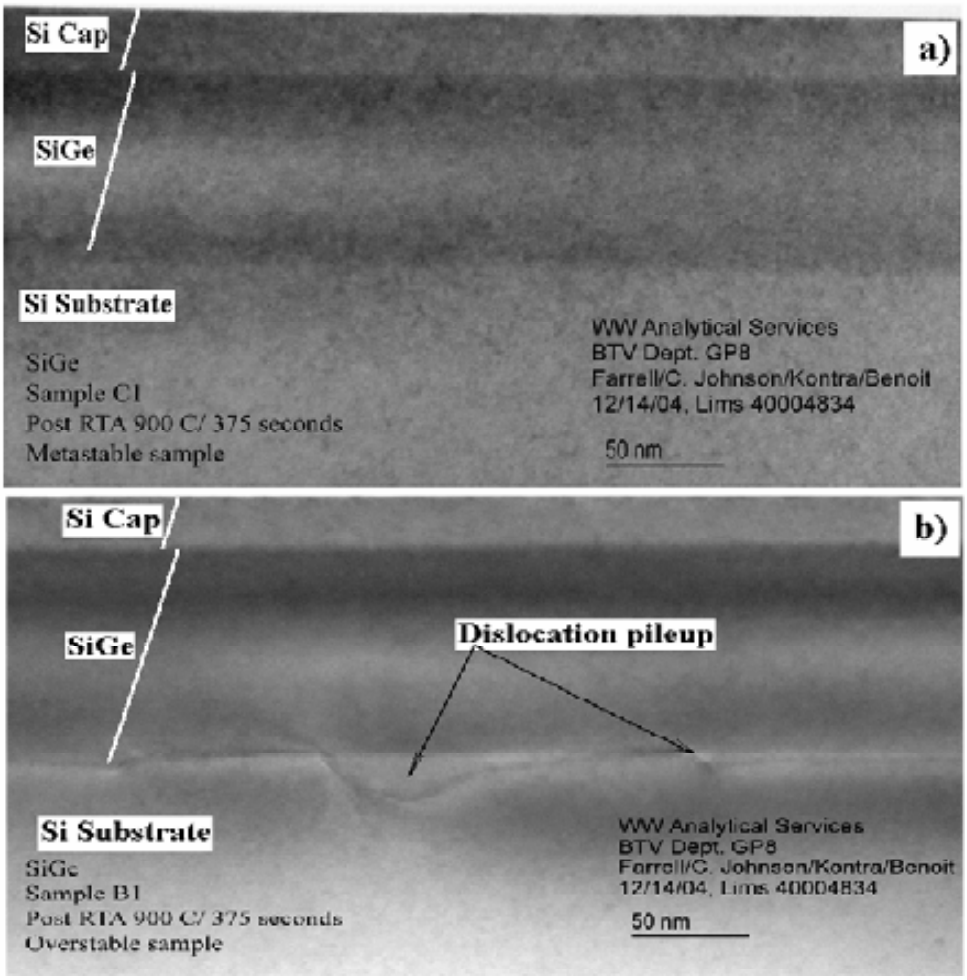

Figure 63: TEM micrographs of the metastable and overstable samples annealed at 900 °C for 375 seconds.

being annealed at 900 °C for 375 seconds, while Figure 63b shows a typical dislocation pileup at the interface below the SiGe layer, with dislocation loops pushed down into the silicon buffer layer. This is characteristic of the modified Frank-Reed mechanism, in which dislocations are formed by the reproduction of "corner dislocations" [64].

5.5 Discussion

The epitaxial SiGe strained layer relaxation process necessarily involves the formation and propagation of defects. Proton irradiation is known to create ionization and displacement damage in silicon that leads to defects in the material. The temperature used during the irradiation in this work, however, is not high enough to thermally activate the modified Frank-Read sources that relax the thin

film and for dislocations to glide (move). Thus, proton irradiation has little effect on the SiGe thin film macro-stability, and the materials' damage due to proton irradiation is similar and minimal for both stable, metastable, and overstable samples. This suggests that device designers contemplating a wide range of Ge profiles need not be constrained when considering space electronics applications of their technology. In contrast, during 900 °C annealing the balance between the internal stress and the Peierls force is broken. The macroscopic glide velocity of the dislocations is thermally enhanced, and the strain relaxation rates are thus highly sensitive to the initial stress (i.e., composition and thickness) of the as-grown thin film samples. The lattice relaxation of the overstable sample hence occurs at a much higher rate than in a metastable sample. Radiation is thus judged to not provide any impediment to the fundamental strain and defect density of SiGe layers used in practical SiGe technologies.

CHAPTER VI

CMOS DEVICE RELIABILITY FOR EMERGING CRYOGENIC SPACE ELECTRONICS APPLICATIONS

6.1 Introduction

While it is well-established that cryogenic (i.e., -196 °C or 77K) operation of Si CMOS technology can provide significant device performance improvements beyond geometrical scaling [65], cooled CMOS has to date made no significant in-roads into conventional electronics applications, primarily because of the cost and complexity associated with the requisite cooling systems. One newly emerging (and interesting) cryogenic electronics application, however, involves NASA's recent mandated refocus on Lunar and Martian robotics and human exploration. The surprisingly extreme temperature conditions on the Lunar surface, for instance (ranging from +120 °C in the sunshine to -230 °C (43K) in the polar shadows), makes the operation of electronics sub-systems on the surface of the Moon exceptionally difficult, although nonetheless essential for the envisioned complex suite of electronics systems that will be needed for the sensing, actuation, and control of robotic systems. Such applications are typically fairly low frequency in nature (e.g., < 100 MHz) and hence do not require the most aggressively scaled CMOS technology, but rather a full suite of mixed-signal circuit building blocks. Thus reliable operation of those circuits across extremely large variations in temperature is needed. Adequate device reliability must clearly be achieved to accomplish this task. CMOS device degradation resulting from the hot carrier effect (HCE) is known to be considerably worse at low temperatures [66]. Device lifetime data at cryogenic temperatures, along with a solid understanding of the corresponding degradation mechanisms, will be critical in this context of space electronics and are therefore addressed in this work.

6.2 Device Technology

The Si CMOS devices investigated here utilize an advanced 0.5 μm SiGe BiCMOS technology, with a fixed channel width of 10.0 μm and effective gate lengths ranging from 0.35 μm (minimum

geometry), to 5.0 *mu*m. The devices were characterized using a custom cryogenic probe system that could be varied from 300K down to 43 K (-230 °C). For brevity, we will focus on the nFET data, since this represents the worst case for this technology.

6.3 Bench Test Results

The *dc* and *ac* performance of CMOS devices changes dramatically at lower temperatures. A temperature-sensitive transistor model is thus crucial to enable circuit designers to predict accurate circuit performance at a given ambient temperature for particular *dc* or *ac* bias conditions. Four different measurement were taken at different temperature points from 300K down to 43K to help extract a BSIM3 model with proper temperature consideration:

1) Ids vs. Vgs @ Vds = 0.05V with different Vbs;

2) Ids vs. Vds@ Vbs = 0V with different Vgs;

3) Ids vs. Vgs@ Vds = Vdd with different Vbs;

4) Ids vs. Vds@ Vbs = Vbb with different Vgs.

The model development is outside the scope of this thesis, but important device parameters such as threshold voltage, carrier mobility, transconductance, and output current are examined in this chapter for physical analysis. Figure 64 and Figure 65 show typical I-V characteristics for CMOS devices at different temperatures. Their current drive capability increases for the same bias condition as the temperature decreases, indicating a significant performance improvement for low-temperature operation. It can also be seen from the slope in the subthreshold region of Figure 64 that the CMOS can be switched on and off in a relatively small gate bias range, a decided design advantage for low-temperature operation that is to be used to reduce power supply voltages.

Figure 66 gives the normalized linear transconductance and normalized low-field mobility at different temperatures. The low-field mobility is extracted by the method described in [67]. The transconductance increases by a factor of 3 as the temperature decreases from 300K to 43K. The low field mobility increases with decreasing temperature from 300K to 43K by a factor of 2 and 5.5 for holes and electrons, respectively, because of the reduced carrier scattering at low temperatures.

Figure 67 shows the temperature dependence of the threshold voltage and subthreshold swing The threshold voltage increases from 0.6 to 0.8 V with cooling. The subthreshold voltage can

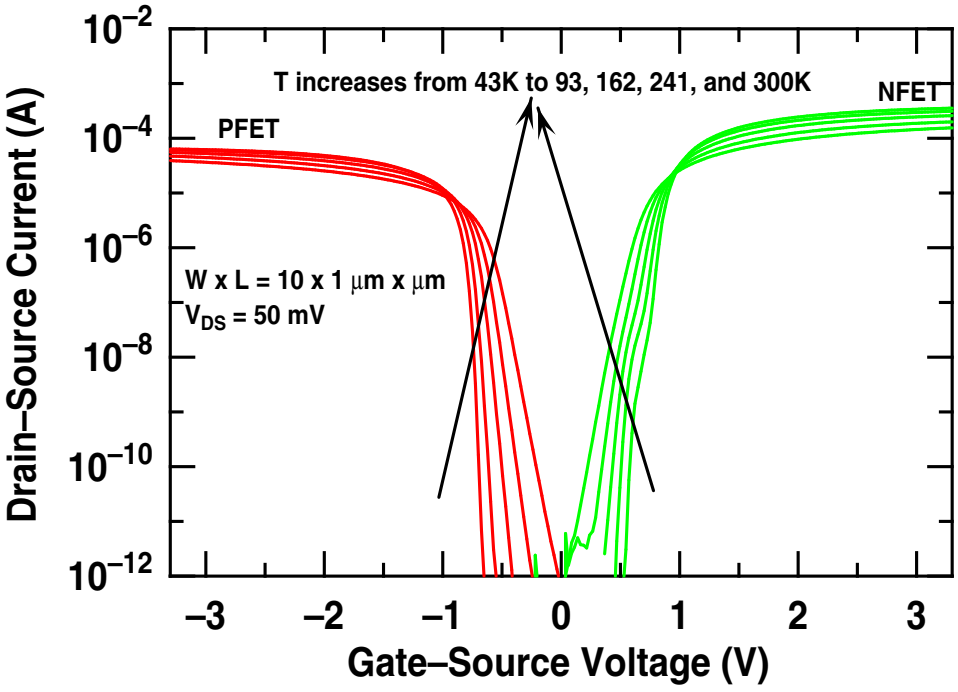

Figure 64: I_D versus V_G for CMOS at different temperatures.

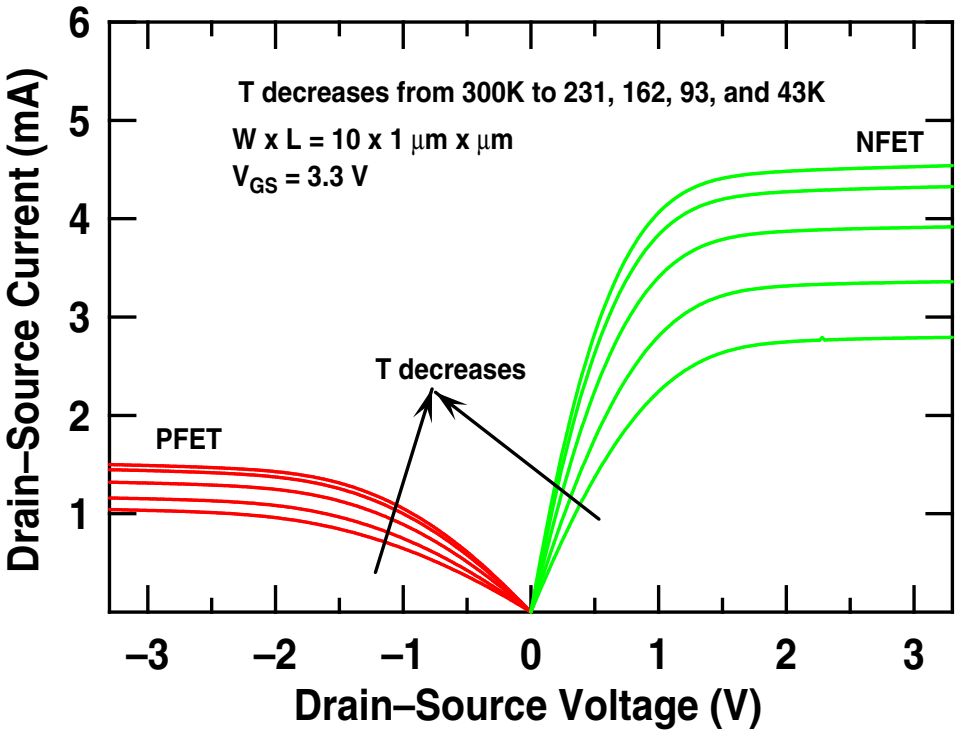

Figure 65: I_D versus V_D for CMOS at different temperatures.

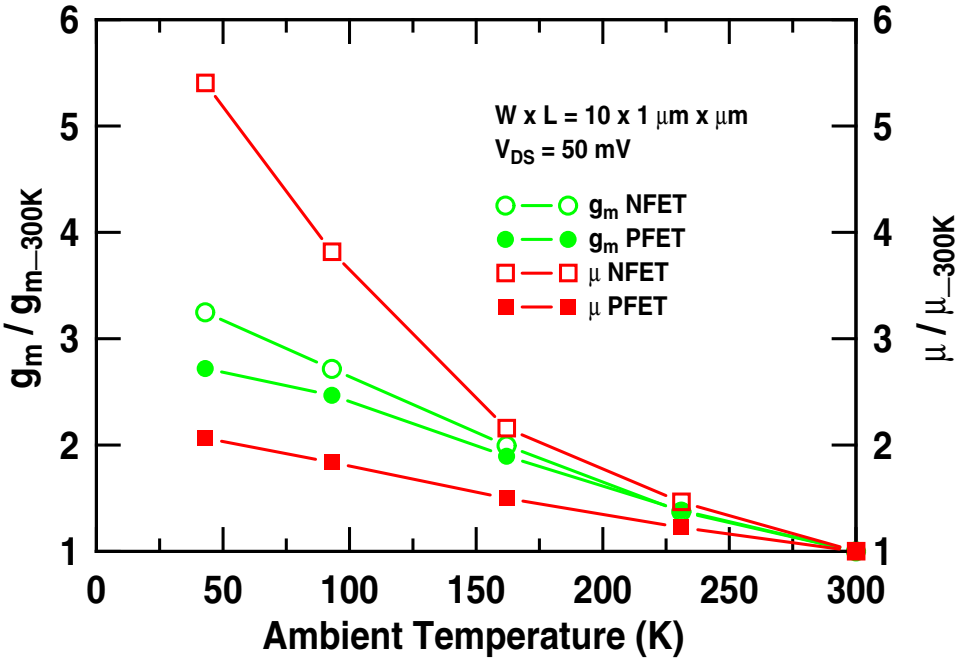

Figure 66: Extracted transconductance and mobility at various temperatures.

be approximated as the sum of the flatband voltage and the gate bias to create a channel surface potential of $2\phi_b$, which is the Fermi potential of the bulk silicon with respect to the intrinsic Fermi level. The increased ϕ_b at lower temperatures leads to an increase in the threshold voltage. The subthreshold swing decreases from 90 mV/decade to about 20 mV/decade with cooling, which is also suggested by Figure 64.

6.4 Device Reliability

The nFET lifetime was inferred using stress-induced changes to the I_D-V_G characteristics. The lifetime τ is defined here as the inferred stress time for which a certain parameter of the I_D-V_G characteristics has shifted by a predefined amount (i.e., a 10% degradation of gm). A typical lifetime assessment analysis using the I_D-V_G characteristics for a 1.0 *mu*m nFET is shown in Figure 68 and Figure 69.

It can be seen from Figure 68 that transistor parameters such as drain current, transconductance, threshold voltage, and subthreshold swing degrade with increasing stress time. The slope of 0.6 for the linear fitting in Figure 69 suggests that interface state generation is responsible for the observed device degradation at the maximum substrate current (VG 1/2 VD), while that of 0.3 for the

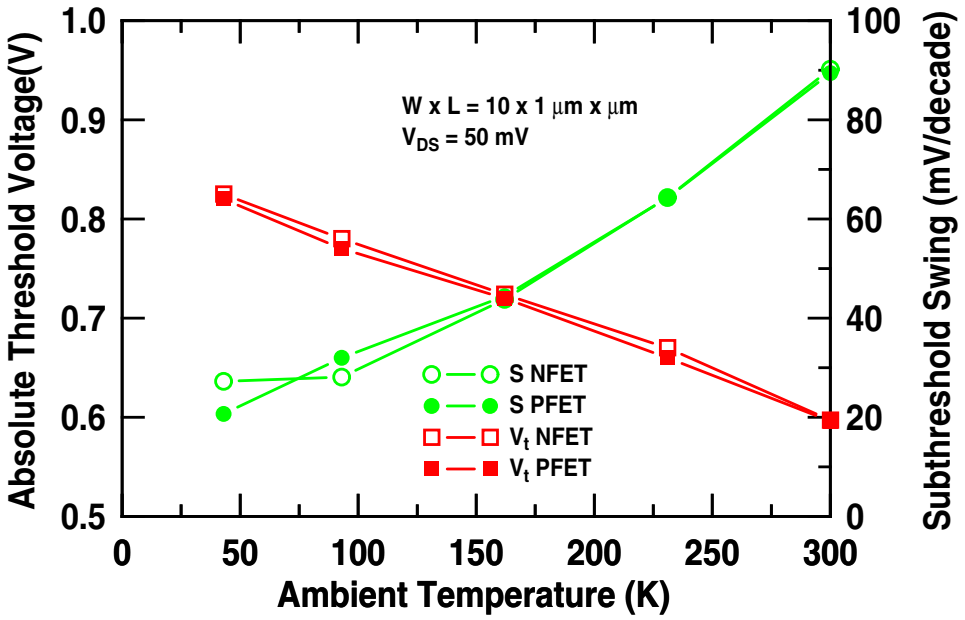

Figure 67: Subthreshold swing and threshold voltage at various temperatures.

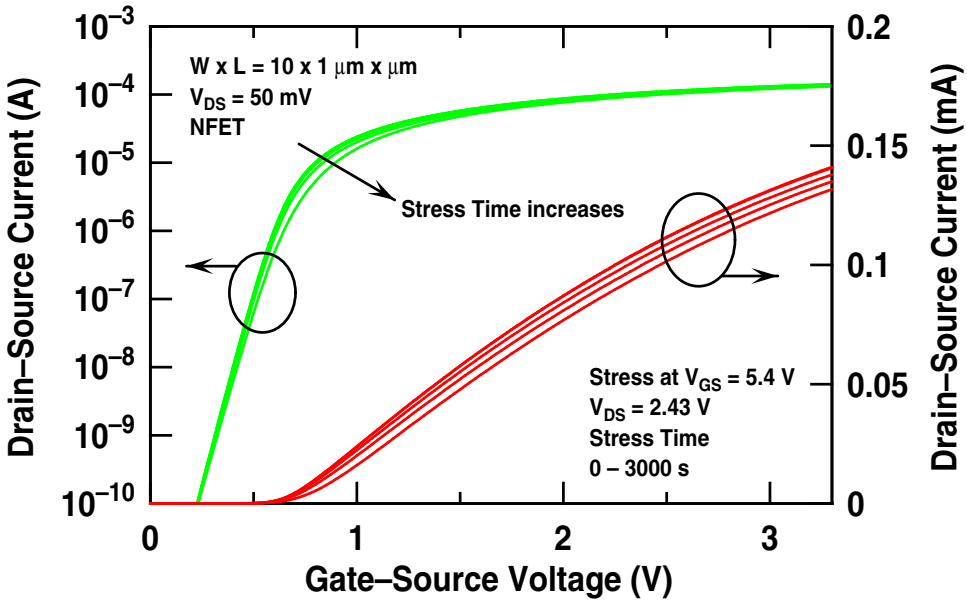

Figure 68: I_D V_G characteristics for different stress times.

maximum gate current bias condition (VG = VD) suggests that oxide trapped charge dominates [66]. For the nFETs operating at 300K, the worst case bias condition for hot carrier degradation is known to be under maximum substrate current bias. There has been speculation that the worst case bias conditions for hot carrier degradation can, however, be a function of temperature [68]. It

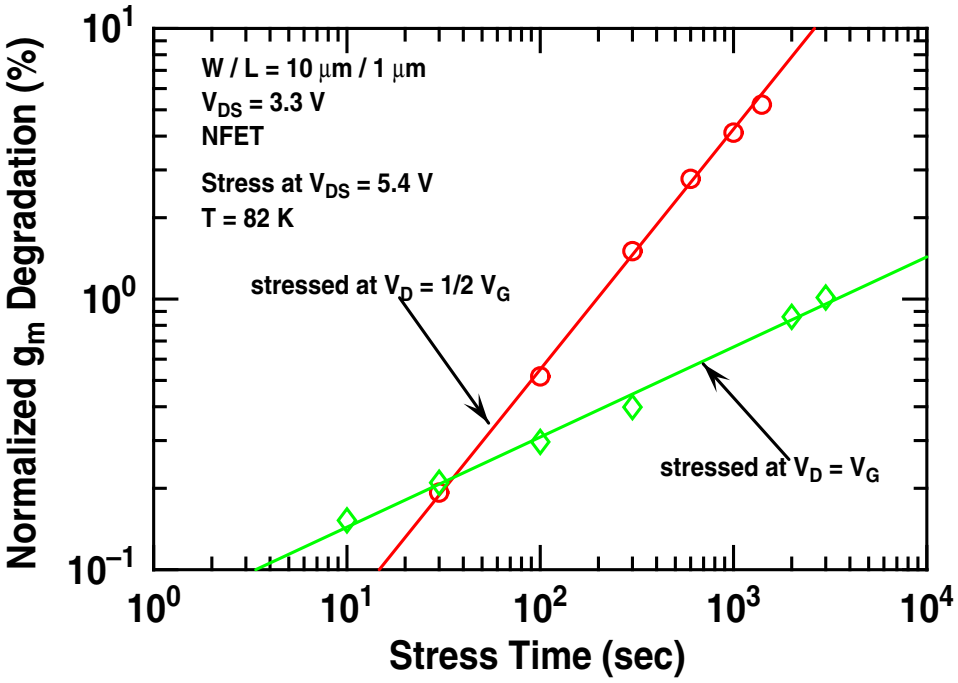

Figure 69: Time-dependent transconductance degradation used to extract device lifetime.

can be verified from Figure 69 that for this technology, the maximum substrate current is indeed the worst bias condition, at least down to 82K, and hence was the condition used here for device lifetime evaluation. The substrate current comprises the generated hot carriers and is thus a good monitoring parameter for HCE in practical measurements. Figure 70 and Figure 71 show the effects of temperature and gate length on substrate current, respectively.

It can be seen from Figure 70 that the maximum substrate current under the same bias condition increases by 3x as the temperature decreases from 300K to 43K, while Figure 71 suggests that the maximum substrate current increases by more than 10x as L shrinks from 1.0 μm to 0.35 μm, and becomes negligible as L increases to 5.0 μm. This suggests that HCE is impacted more by device geometry than by the temperature. Figure 72 and Figure 73 show the inferred lifetime versus drain bias condition for nFETs at different temperatures and gate lengths, respectively.

Figure 72 shows that τ decreases by 10x as the temperature is reduced from 300K to 82K. Furthermore, τ differs by more than 100x between the 1.0 μ m and 0.35/5 μm transistors, and hence the longer-channel devices are preferred for cryogenic applications of this technology. Assuming that fast interface trap generation dominates the HCE degradation, plotting τI_D versus $I_S U B / I_D$ on

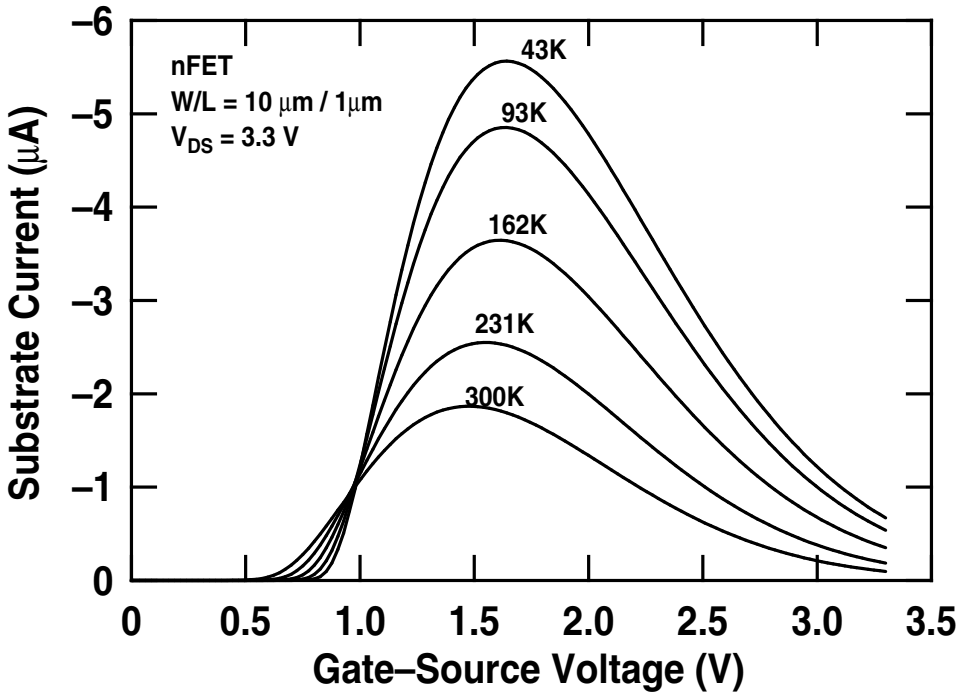

Figure 70: Substrate current as a function of gate bias at different temperatures.

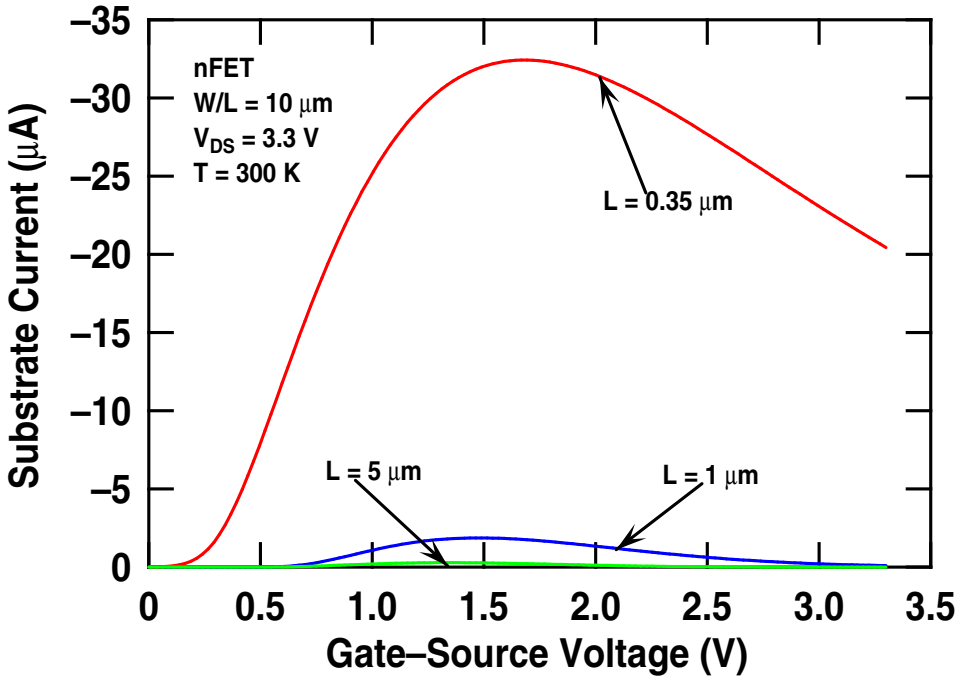

Figure 71: Substrate current as a function of gate bias for nFET with different gate lengths.

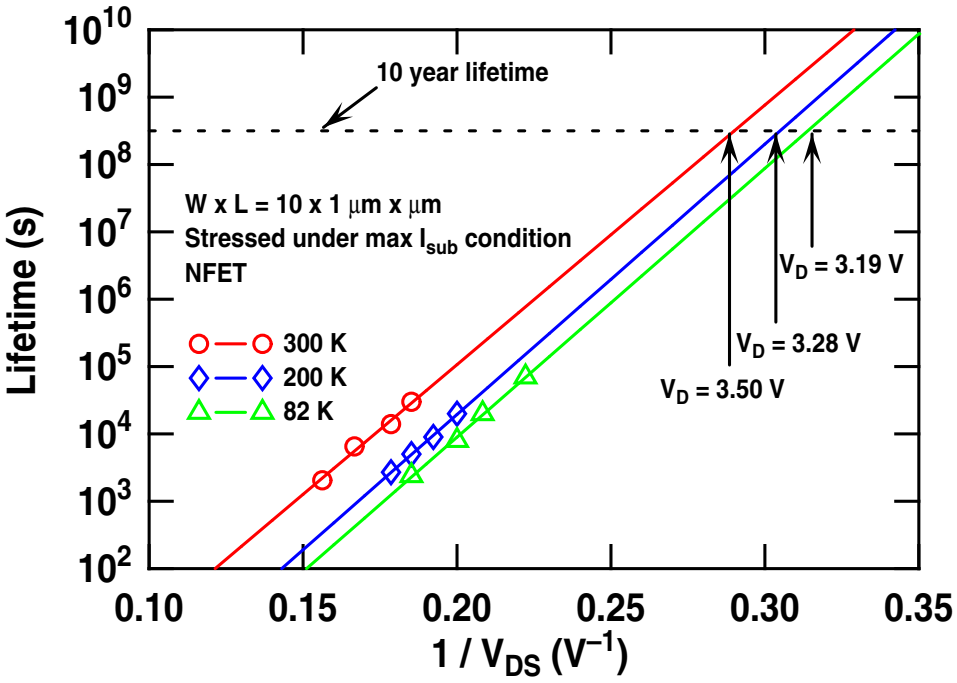

Figure 72: The inferred lifetime as a function of bias condition for a nFET at 82, 200, and 300K.

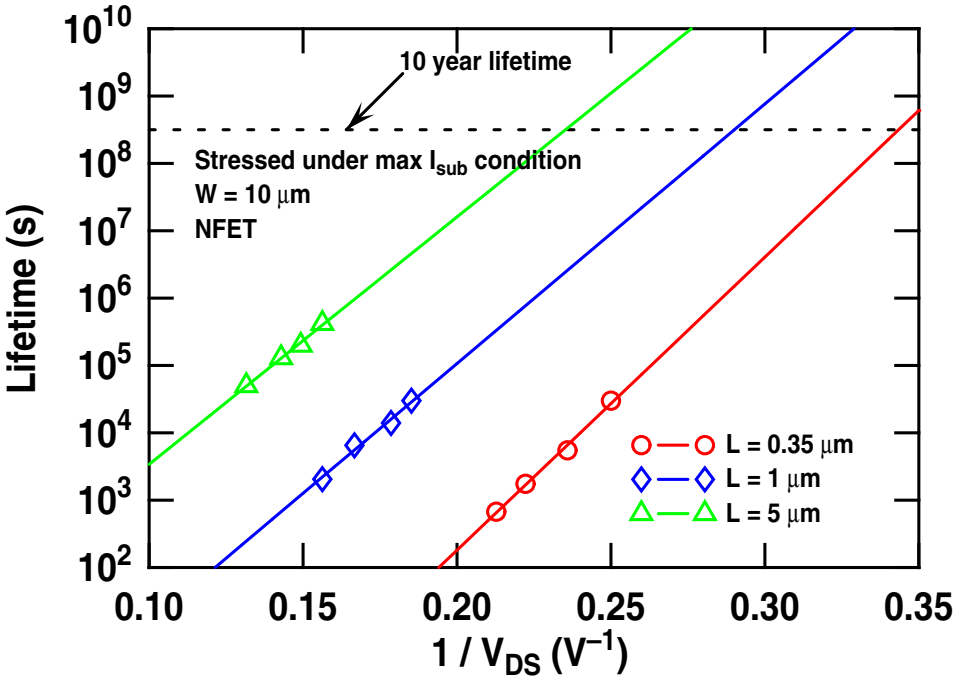

Figure 73: The inferred lifetime as a function of bias condition for nFETs with various gate lengths.

a log-log scale should yield straight line behavior [69], and the critical electron energy for generating an interface trap is calculated to be 3.9 eV from the slops of the line. Both the slope and the critical

energy from Figure 74 correlate well with literature data (2.9 and 3.7 eV, respectively, in [69]), suggesting that interface state generation is the dominant limiting reliability factor regardless of operation temperatures and transistor gate length.

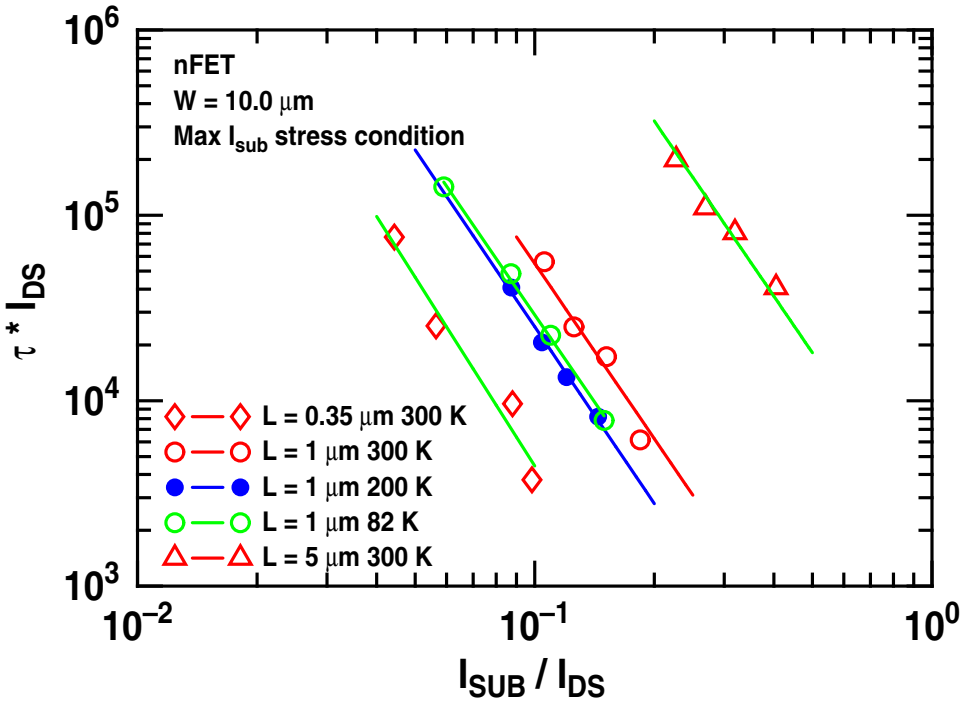

Figure 74: nFET extrapolated lifetime plots used to evaluate activation energy.

6.5 Discussion

Low-temperature operation provides CMOS device performance improvement at the expense of shorter device lifetime. Part of this reliability degradation can be offset by using CMOS with longer channel transistors, since the hot carrier induced device degradation is more strongly dependent on channel length than on operation temperature. The use of longer channel devices will lead to smaller output current drive capability because of the smaller W/L ratio. Trade-offs must be negotiated between output current and device reliability. The choice of the right device geometry will often depend on the practical application of the transistors in the circuit. For example, the output current-driving capability will be critical for a source follower transistor in a buffered FET logic circuit, so a short-channel CMOS will be preferred, while long-channel device will be preferred for CMOS in an inverter that requires a large logic swing.

One of the advantage of low-temperature operation is the reduced power consumption resulting from the scale of the power supply voltage with temperature. The threshold voltage of the CMOS will increase, however, as the temperature goes down. One typical solution to this problem is to reduce the threshold voltage through careful channel profile design. For example, V_t can be reduced by decreasing the channel doping. Another solution is to modulate the threshold voltage by forward biasing the source-body junction. An interesting V_t engineering scheme at room temperature has been reported based on the active well CMOS strategy [70]. By forward-biasing the body at about 0.6 V, CMOS gain significant performance enhancements such as faster device speed and lower power consumption. This technique requires, however, the use of a dual trench isolation process to limit the junction leakage and prevent latch up. When the temperature is reduced, both the body-source junction leakage and latch up can be tolerated with ever higher forward substrate bias. With the elimination of an additional isolation process, CMOS can be used "as is" for better performance, thus dramatically reducing their design costs.

CHAPTER VII

CONCLUSIONS AND FUTURE WORK

The contributions made by this work can be summarized as follows:

1. A comprehensive assessment of the high-temperature capability of SiGe HBT. The current gain decreases at increased temperatures, and this can be used to help mitigate thermal run away. The frequency response decreases with the increase of temperature, but remains sufficiently high for most circuit applications at temperatures as high as 200-300°C. The device breakdown voltage is a complicated function of current gain and avalanche factor. Its temperature dependence is affected by the collector doping. The device reliability actually improves under reverse EB stress, and the reliability under mixed-mode stress is also acceptable. The device thermal reistance increases at increases temperature, and can be optimized by device geometry design.

2. A comprehensive study of the substrate bias effects in vertical SiGe HBTs fabricated on CMOS compatible SOI. A high positive substrate bias is found to suppress the undesirable quasisaturation effect and improve device *ac* response. But this positive substrate bias increases the impact ionization in the intrinsic collector-base junction. Furthermore, the device thermal resistance increases with the substrate bias, and device reliability could be another important design issue for positive substrate bias. The speed improvement is also demonstrated in an ECL circuit. At last, important design trade-offs are discussed. including quasisaturation effects, dynamic response, breakdown voltage, self-heating, device reliability, and ECL circuits.

3. A first assessment of the proton irradiation effects on vertical SiGe HBTs fabricated on CMOS compatible SOI. The porton irradiation is found to creat generation-recombination trap center in SOI SiGe HBTs and creat positive charge at the buried oxide interface that effectively delay the onset of the Kirk effect. The delay of Kirk leads to increased f_T and f_{max}. TCAD

simulation is incorporated to help understant the physical mechanism.

4. A comparison of the SiGe thin film stability under proton irradiation and high-temperature annealing. Irradiation with 63 MeV protons is found to introduce no significant microdefects into the SiGe thin films, regardless of the starting stability condition of the SiGe film, and thus does not appear to be an issue for the use of SiGe HBT technology in emerging space systems. The strain relaxation of SiGe thin film under thermal annealing, however, is found to be sensitive to the composition and thickness of the as-grown samples, as expected, with the subsequent lattice relaxation of the overstable samples occuring at a much higher rate than that of metastable samples.

5. Bench tests of CMOS devices for low-temperature operation, and stress tests of nFETs with multiple gate lengths at low temperatures. CMOS device performance improves with cooling, with higher carrier mobility, better subthreshold swing, and higher current drive at low temperatures. However, CMOS device reliability becomes worse at decreased temperatures due to aggravated hot-carrier effects. The device lifetime is found to be a strong function of gate length, suggesting that design tradeoffs are inevitable. Interface state generation is the dominant limiting reliability factor, regardless of the device geometry and operating temperature for the CMOS technology considered.

In the future, this work should be extended to three aspects:

1. Characterize the electromigration of SiGe technology for high-temperature operations, especially the high-temperature capability of passive components, and demonstrate its high-temperature capability at the circuit level.

2. Characterize the radiation tolerance of vertical SiGe HBTs fabricated on CMOS compatible SOI when they are actively biased under proton irradiation.

3. Build a suitable BSIM3 model for low-temperature operation, characterize CMOS *ac* performance under low-temperature conditions, and demonstrate low-temperature operations of CMOS circuits.

APPENDIX A

THERMAL RESISTANCE MEASUREMENT OF SIGE HBTS

A.1 Measurement consideration

Thermal resistance is a mathematical concept analogous to the electrical resistance in basic physics. It is a measure of junction temperature rise relative to the ambient temperature due to certain power dissipation inside a transistor

$$\triangle T \;=\; T_{junction} - T_{ambient} \;=\; R_{th} \times P_{diss} \tag{17}$$

where R_{th} is the thermal resistance and P_{diss} is the power dissipation inside a transistor. Thermal resistance can be extracted from the relation between the power dissipation and the junction temperature, for which a temperature-sensitive electrical parameter (TSEP) is utilized in order to link the two parameters experimentally. One of the most applied TSEP in bipolar transistor is the base-emitter voltage. By sweeping the bias condition across a BJT hence a certain range of power dissipation, the base-emitter voltage is monitored to infer the junction temperature. For most modern bipolar devices, the base-emitter voltage varies linearly with temperature for the same bias condition. If V_{BE} changes linearly with the power dissipation level,

$$V_{BE} \;=\; A \;+\; B \;\times\; T_{amb} \tag{18}$$

R_{th} is a constant independent of power dissipation.

A.2 Constant self-heating method

A method utilizing V_{BE} for the R_{th} extraction is first demonstrated in [33]. The temperature dependence of V_{BE} is first calibrated. The transistor is biased with fixed emitter current I_E and zero collector-base voltage V_{CB}, and V_{BE} is measured for different substrate temperatures T_S (e.g. 283K to 353K). Then I_E and T_S are fixed, and V_{BE} is measured for different dissipated power ($P_{diss} = I_C V_{CE} + I_B V_{BE}$) by sweeping V_{CB} from 0 to a moderate voltage without significant impact

ionization (e.g. 1.0V). By correlating V_{BE} with the two measurements, the junction temperature rise as a function of power dissipation is obtained, which could be very linear for the measured devices. As a final step, a compensation is made in order to account for the self-heating effect in the first measurement, since it related V_{BE} to the substrate temperature T_S, not to the junction temperature T_j. This can be done by taking y-axis intercept point of the obtained temperature-power relation, denoted by To in Figure 75, and shifting the entire curve upward by the amount of the difference between the ambient temperature T_{amb} and To. This completes the extraction procedure.

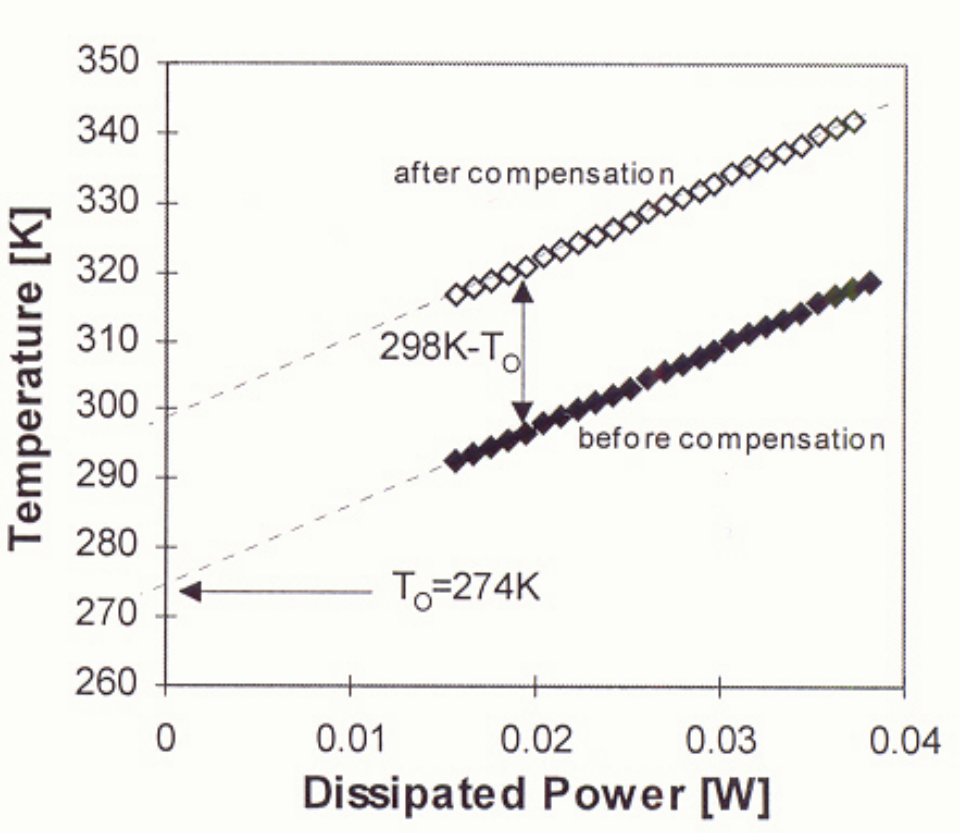

Figure 75: The calculated junction temperature before and after compensation [33].

A.3 Variable self-heating extraction method

In the constant self-heating method, the junction temperature differs from the ambient temperature due to the self-heating of the device during the first measurement , i.e. $T_j > T_{amb}$. Therefore,

in the last step, a compensation is made using $T_{amb} = T_j - \triangle T$ which transforms Equation 18 into

$$V_{BE} = A + B \times (T_j - \triangle T) \tag{19}$$

This shifts the temperature curve [lowest line in the inset of Figure 75] toward higher values so that the (extrapolated) junction temperature at zero power dissipation, T_0, equals room temperature. This shift, without changing the slope, is only valid if the self-heating during the temperature sweep measurement is constant. During the calibration of the temperature dependence of V_{BE} on T_{amb}, the dissipated power $P_T = I_E \times V_{BE}$. Thus P_T is not a constant during the temperature sweep due to the change of V_{BE}. A revised thermal resistance extraction method has been proposed with proper consideration of the change of P_T during the first measurement [50]. Now the junction temperature can be written as

$$T_j = T_{amb} + R_{th} \times P_T = T_{amb} + R_{th} I_E V_{BE} \tag{20}$$

By adding parameters α and β to fit the relation between V_{BE} and P_T

$$V_{BE} = \alpha + \beta \times P_T \tag{21}$$

Equation 17- Equation 21 can be used to obtain junction temperature as

$$T_j = \frac{\beta \times (1 + B R_{th} I_E) \times P + \alpha \times (1 + B R_{th} I_E) - A}{B} \tag{22}$$

The thermal resistance can be obtained from the first derivative of T_j over P

$$R_{th} = \frac{dT_j}{dP} = \frac{\beta}{B \times (1 - \beta I_E)} \tag{23}$$

In the constant self-heating method, $R_{th} = \frac{\beta}{B}$. Thus a correction factor $1 - \beta I_E$ is ignored in the constant slef-heating method. Since $\beta < 0$ for the experimental data, constant self-heating method leads to overestimation of junction temperature and thermal resistance.

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