

CMOS INTEGRATED LC Q -ENHANCED RF FILTERS FOR WIRELESS RECEIVERS

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CMOS INTEGRATED LC Q -ENHANCED RF FILTERS FOR WIRELESS RECEIVERS

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To My Parents, Royce and Fran Gee

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SUMMARY

The research presented in this thesis examines the feasibility of employing RF bandpass filters designed using the passive and active components available in a standard digital CMOS process. The intent of this prospective filter integration is to create a front-end circuit for an integrated wireless receiver and alleviate or minimize the requirement for off-chip passive filter components, with the anticipated outcome of reducing the overall component count and size of next generation wireless devices and systems.

The circuit investigated in this work introduces a loss-compensated second-order RF bandpass filter implemented in a 0.18 μm digital process provided by National Semiconductor. This filter utilizes an integrated resonant tank comprised of an on-chip transformer along with parasitic and designed capacitors. The design incorporates a novel method of controlled positive feedback via the integrated transformer and a single transistor, providing an adjustable quality factor, Q , for the inherently lossy on-chip resonator. The filter has a measured center frequency of 2.12 GHz, a maximum gain of 4 dB, and a tunable Q of 2 to 30. With the filter adjusted for the maximum Q , the input $P_{1\text{dB}}$ is measured at -3.5 dBm with a power dissipation of 143.1 mW. The measured input referred noise power at a spot bandwidth of 1 Hz is -144.3 dBm, which facilitates a prospective input sensitivity of -84.3 dBm and dynamic range of 80.8 dB with the designed filter incorporated into a receiver utilizing a 1 MHz channel bandwidth.

CHAPTER 1

INTRODUCTION

The realization of complete system-on-chip (SoC) solutions for complex circuits and systems has been the focus of great deal of research and industrial pursuit for over two decades [1]. Although debate continues on the practicality of SoC methods for future designs [2], Electronic Trends Publications (ETP) projects the SoC market to show a compound annual growth rate of 20% until the year 2007 [3]. In the field of communications circuit design, the realization of the complete integration of radio frequency (RF) transceivers and digital signal processing blocks onto a single integrated circuit (IC) is a logical area in which to develop SoC solutions. Presently, with the growing demand for multi-functional wireless consumer devices, the need for full integration of the RF and logic circuits in wireless communications systems is becoming increasingly evident.

At this time, some of the most prevalent off-chip components required in wireless transceiver circuits are discrete filters, mostly surface acoustic wave (SAW) or ceramic. These devices are used in the receiver for the filtering of downconverted intermediate frequencies (IF) as well as at the front end of the system for RF signals that are received at the device input antenna, processing signals in a spectrum ranging from tens of megahertz to gigahertz. If on-chip high frequency filters with acceptable electrical

characteristics can be realized, the need for these currently required off-chip filters would be eliminated. This implementation of integrated filters could lead to complete SoC communications system design solutions that would decrease the complexity, reduce the size, and lower the cost of future wireless transceiver circuits and systems.

The objective of this work is to investigate the feasibility of employing on-chip continuous-time (CT) filters and examine the electrical characteristics of these circuits up to frequencies in the gigahertz range. Specifically, the implementation of filters in standard complementary metal-oxide semiconductor (CMOS) processes is examined. CMOS is the standard design medium for digital circuitry and with the increased transit frequency (f_T) values that accompany steadily shrinking device sizes, the implementation of gigahertz frequency circuits in this medium is increasingly feasible. This high frequency design practicality, along with the dense levels of integration achievable in standard digital CMOS, make this IC process an attractive platform for the development of RF circuits that would further the progress towards full integration of complex mixed-signal transceiver designs.

First, an overview of some commonly implemented wireless receiver topologies is presented along with a qualitative analysis of the filtering requirements for each type of system. Some inherent advantages and disadvantages for each type are also briefly covered. Specifications that define the operational characteristics of wireless receivers are also examined and the requirements of some current wireless standards are analyzed to highlight performance parameters required for integrated filters.

Second, circuit topologies that are conducive to the implementation of on-chip continuous-time filters are examined in detail. The building blocks that make up these

filters are presented along with the overall circuit architectures. The areas of application for the different topologies in relation to specific areas in receiver system design are also discussed. Also, a comparison of the different types of filter circuits is undertaken to highlight the advantages and disadvantages of each.

Finally, the RF bandpass filter circuit that is the focus of this research effort is introduced. This circuit is a Q -enhanced gigahertz range bandpass filter incorporating a novel design technique that provides improvements in filter linearity through a unique bias level shifting method while also facilitating prospective single-to-differential signal conversion. This design differs from previous RF integrated filter work with the introduction of a unique transformer feedback method to facilitate magnetically coupled loss-restoration and subsequent filter Q -enhancement. With the prospect of implementing this circuit as a building block in an integrated RF receiver front-end, and in order to identify and designate specific commercial operational criteria, the design targets the specifications for Bluetooth receiver applications. A theoretical evaluation of this new RF filter circuit topology is presented along with detailed results of computer-aided simulations and experimental test results.

CHAPTER 2

WIRELESS RECEIVERS

The function of a wireless receiver is to detect a low-level modulated RF signal in the presence of noise and unwanted signals and to accurately amplify and process this signal to extract the modulating digital or analog information that is present in the received RF energy. The following sections provide a qualitative overview of receiver architectures, specifications, and several current commercial frequency allocations with the intent of establishing a foundation from which to base subsequent discussion regarding the RF filter design work that is the focus of this research. Detailed calculations and derivations are omitted but can be referenced in previously published research literature and textbooks [4,5].

2.1 Receiver Architectures

The architecture of a wireless receiver is selected to meet particular electrical specifications as well as satisfy a number of design criteria that regularly include circuit complexity, power dissipation, and total number of required components. The following sections present information regarding heterodyne receivers and direct conversion, or homodyne receivers.

2.1.1 Heterodyne Receiver

The heterodyne receiver operates by down-converting incoming RF signals to a lower IF frequency, then filtering and amplifying the IF signal before demodulation takes place. The name heterodyne is derived from the Greek words for *other* and *power*, which aptly describes the heterodyne receiver characteristic of combining the power of one signal with another. The heterodyne receiver is often referred to as the superheterodyne receiver and was first introduced in 1918 by Edwin Armstrong.

Figure 2.1 shows a block diagram of the single-conversion heterodyne receiver architecture. The fundamental advantage in utilizing the heterodyne approach for signal reception is the conversion of multiple channels of various frequencies to a single down-converted frequency. This is accomplished by combining the incoming RF signal with a local oscillator (LO) signal in a non-linear device, or mixer, with one of the output products of the mixer being the IF signal at the predetermined frequency. This down-converted frequency translation of the information-carrying RF signal facilitates simplification of design for the processing, filtering, and demodulation circuits required to extract information signals from the received and converted RF.

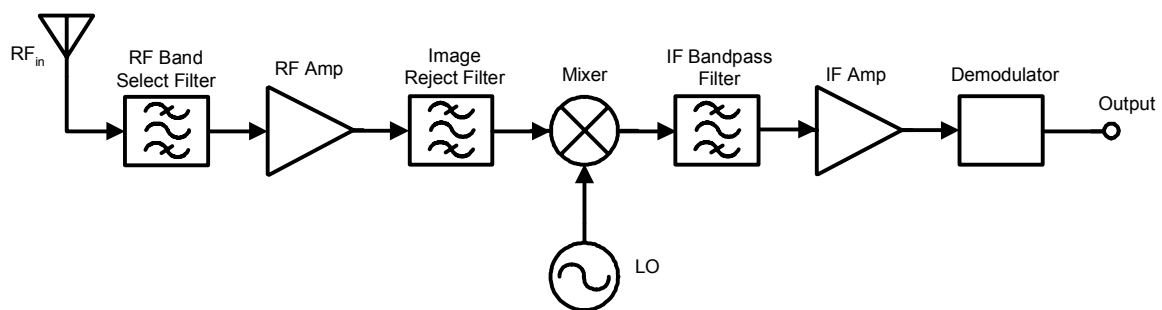


Figure 2.1. Single-conversion heterodyne receiver architecture.

As detailed in Figure 2.1, there are three different filter blocks normally incorporated into this type of receiver. Bandpass filtering is required for the band-select RF and channel-select IF filters, while the image reject filtering is often achieved with a bandstop notch circuit. Operationally, different channels can be selected by changing the frequency of the local oscillator (LO) that ‘beats’ or heterodynes with the RF signal in the mixer. Two signals are produced at the output of the mixer, $f_{LO} \pm f_{IF}$, where one is the wanted RF signal and the other an unwanted image frequency. By incorporating this heterodyning scheme, channel-select filtering can be performed at the lower fixed IF frequency. This narrow-band channel filtering requires a lower Q filter at the IF frequency than would be required for the same bandwidth at RF. However, the drawback is that a tradeoff is required between image rejection and channel selection that usually requires a relatively high IF. This makes the IF filter more difficult to integrate and increases the quality factor requirement of this block. Figure 2.2 shows two different frequency plans and the effects of changing the IF on the translated RF and image signal levels for a fixed RF input filter. In Figure 2.2, a prospective front-end RF filter passband response is indicated and shown with the lighter curve in the left most plots, and is identical for both of the frequency plans. However, notice that after the mixer stage, the frequency plan with the higher IF frequency shown in the lower plot has a greater attenuation of the image signal after the RF and LO are mixed. Also, this example does not take into account the possible use of an image-reject filter. An image reject filter might be utilized along with the RF band-select filter at the input of the receiver to reduce or ‘notch’ the image frequency level before mixing.

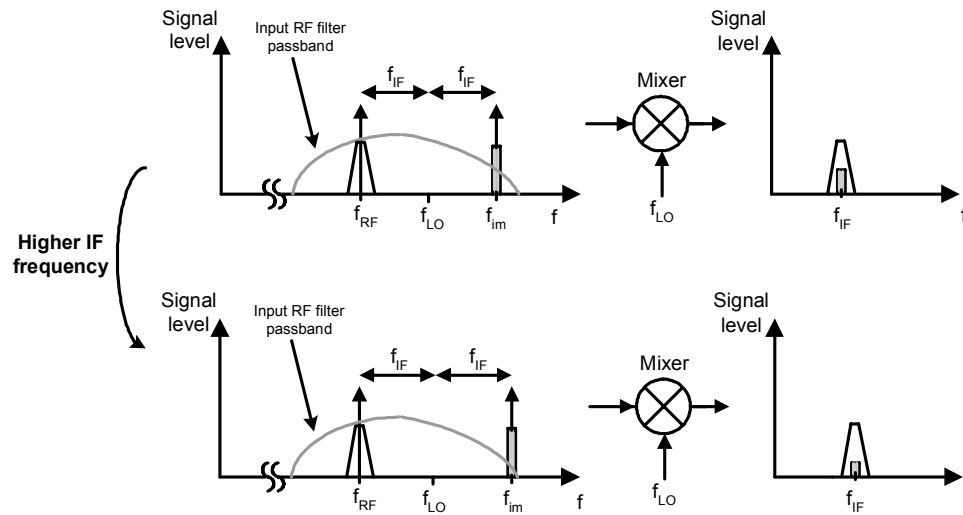


Figure 2.2. Translated RF and image signals.

A dual-conversion heterodyne receiver is shown in Figure 2.3. This topology allows the signal to be mixed down in two steps allowing for flexibility in the frequency planning, i.e. the selection of LO and IF frequencies. This adaptable frequency planning subsequently facilitates incorporation of RF and IF filters with less stringent operational specifications.

For either single or dual-conversion heterodyne architectures, it should also be noted that the generation of unwanted spurious frequencies, or spurs, induced by non-linear behavior in the mixers creates multiple interrelated harmonic signals that are dependant on the particular mixer used. The expected frequency and amplitude of these spurious signals, information normally supplied in manufacturer's data sheets, would be considered in determining two IF frequencies that would be least effected by the intermodulation products created by the mixing of these multiple frequencies.

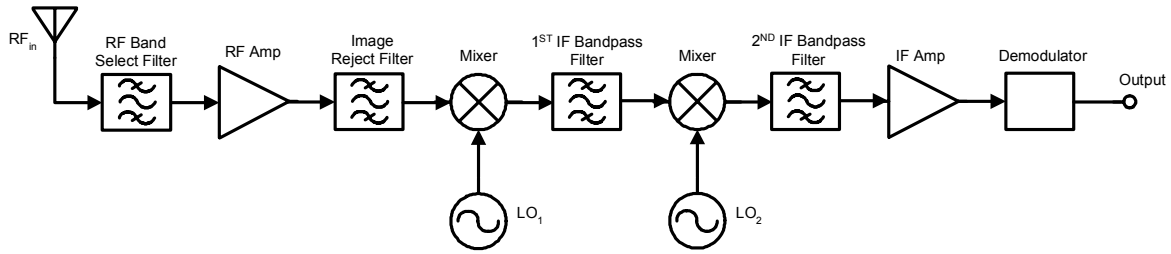


Figure 2.3. Dual-conversion heterodyne receiver architecture.

2.1.2 Direct Conversion Receiver

The direct-conversion receiver, also known as zero-IF or homodyne receiver, translates the incoming RF signal directly to baseband or zero frequency. This receiver block diagram is shown in Figure 2.4. The direct conversion architecture offers two main advantages over the heterodyne receiver. First the problem of image rejection is nullified because the IF frequency for this type of receiver is zero. Second, the IF filter and amplifier stages are replaced by low-frequency counterparts which are easily integrated on-chip.

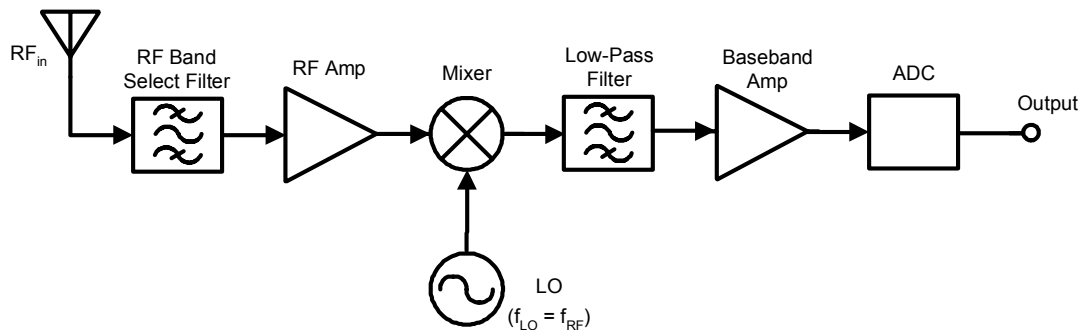


Figure 2.4. Direct conversion receiver architecture.

Alternately, there are several drawbacks to using the direct conversion receiver architecture. First, finite isolation from the LO port to the RF port of the mixer leads to dc offsets at the mixer output that results from LO self-mixing. This LO leakage leads to a requirement of offset cancellation in the receiver. LO leakage back to the antenna can also create interference output signals that can adversely affect other nearby users. Also, because of the limited gain in zero-IF receivers provided by the RF amp and mixer, the downconverted signal is very sensitive to noise. This is particularly problematic in CMOS technology, which suffers from a large flicker noise component generated by MOS transistors at low frequencies. One alternative to the zero-IF problem is the implementation of a ‘low-IF’ frequency plan. Both the zero-IF and low-IF direct conversion receivers are the subject of current academic and industrial interest [6,7].

2.2 Receiver Specifications

Receiver specifications provide the operational performance characteristics required to realize a prospective circuit or system for utilization in a commercially approved communications protocol. The receiver specifications presented in the following sections include dynamic range, noise, sensitivity, linearity, and selectivity.

2.2.1 Dynamic Range

Dynamic range (DR) is usually defined as the ratio of two input signal levels in a circuit or system, minimum detectable and maximum tolerable. The minimum signal detectable depends on the input referred noise level and the required system input signal-to-noise ratio (SNR) while the maximum input signal a circuit or system can accommodate is usually defined for a certain level of distortion or compression at the

output of the device. These circuit attributes can also be defined in terms of sensitivity (minimum signal) and linearity (maximum signal).

2.2.2 Noise and Sensitivity

Receiver sensitivity is an indication of the lowest signal level that a receiver can detect and process while meeting a minimum required SNR. For digital modulation schemes, the SNR is indirectly proportional to the Bit Error Rate (BER). The maximum BER indicates the amount of error the receiver's digital signal processing (DSP) circuitry can tolerate while still interpreting the incoming signal. The noise level, or noise floor, that would mask any incoming low-level signal and that dictates receiver sensitivity is the noise contributed by the receiver circuit and normally referred to the input of the system.

The integrated noise bandwidth, B_n , for a second-order bandpass filter is measured at the filter center frequency, f_o , and is given by

$$B_n = \frac{\pi f_o}{2Q} = \frac{\pi}{2} B_3 \quad (1)$$

where B_3 is the 3-dB bandwidth and Q is the quality factor of the filter [8]. The relationship of these parameters is illustrated in Figure 2.5.

The integrated filter noise is usually measured over the bandwidth of one channel (IF bandwidth) for a particular transmission standard to determine the minimum detectable signal for a receiver. Also, the noise over the entire filter band (RF bandwidth) is sometimes utilized as a reference when comparing different filter designs in the literature.

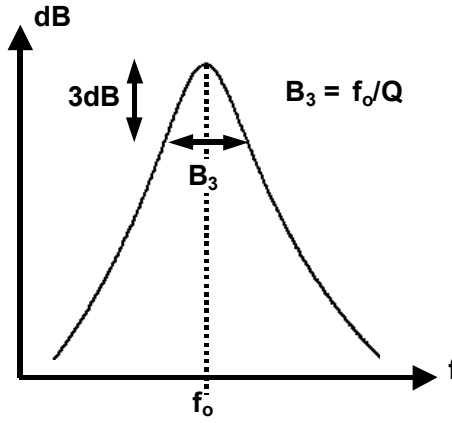


Figure 2.5. Graphical representation of bandpass filter Q and 3-dB bandwidth.

2.2.3 Noise Figure

Another specification commonly used for characterization of receiver blocks is the noise figure (NF). The noise figure is defined as the ratio of the input SNR to the output SNR and is usually expressed in units of decibels (dB). More detailed noise figure analysis methods pertaining to the characterization of differential circuits, specifically in the RF spectrum, have been investigated [9] and can be reviewed for more explicit information.

2.2.4 Linearity

The linearity of an RF circuit is normally described by the 1-dB compression point, (P_{1dB}), or the third-order intercept point, (IP_3), with these parameters normally expressed in units of dBm. P_{1dB} is defined as the input signal level that causes the small-signal gain of a circuit to decrease by 1 dB, and is an indication of the harmonic distortion created as the input level drives the circuit into a non-linear state, compressing the output signal. Figure 2.6 presents a log-log graph showing a comparison between an ideal input/output gain response (dB/dB) and a non-ideal gain curve where the output signal, P_{out} , does not

linearly ‘track’ the input signal, P_{in} , for all applied input levels. Figure 2.6 shows that the output signal is directly proportional to the input signal at lower levels of input power but begins to deviate from this linear relationship as the input power is increased. At a specific input power level, this non-ideal response produces a deviation in linearity of 1 dB and this power level is referred to as the 1-dB compression point, or P_{1dB} . This 1-dB compression point can be referred to the input *or* output power level, but is normally input-referred in documentation relating to filters.

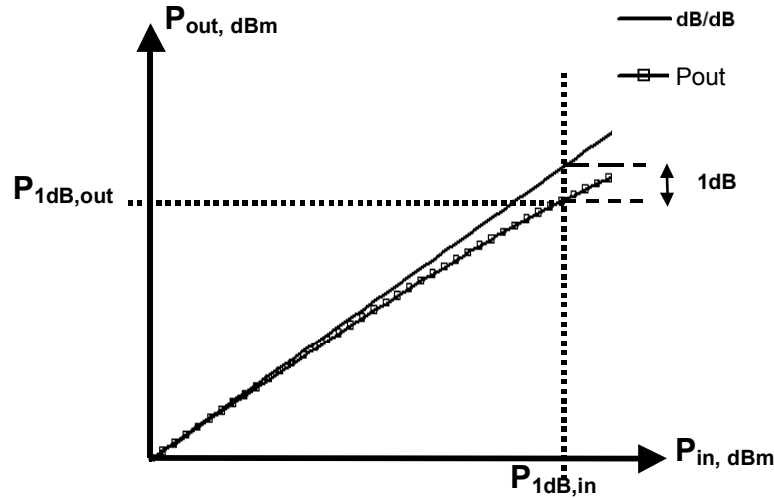


Figure 2.6. 1-dB compression point.

The IP_3 , or two-tone test, is a measure of intermodulation (IM) distortion based on the application of two separate signals that are very close in frequency and equal in magnitude. As the levels of these signals are increased, third-order intermodulation products are generated very near the frequency of the two original signals. The third-order intercept point is the input (IIP_3) or output (OIP_3) level where the *output* level of

one original signal and the third-order intermodulation signals are equal. For general reference, it can also be shown that P_{1dB} is normally around 10 dB less than IP_3 [4].

2.2.5 Spurious-Free and P_{1dB} Dynamic Range

The two-tone measurement technique, or IP_3 , is used when the spurious-free dynamic range (SFDR) is specified. The SFDR defines the upper end of the dynamic range for the maximum input level in a two-tone test at which the third-order IM products do not exceed the noise floor [10]. The lower end of the range is the integrated noise floor. The P_{1dB} dynamic range is the ratio of the noise floor and the 1-dB compression point, and based on previous linearity discussion, is approximately 10 dB less than the SFDR.

2.2.6 Noise and Linearity Tradeoffs

Tradeoffs exist between linear circuit operation and achievable sensitivity. For example, circuits with increased gain possess reduced input referred noise and increased sensitivity, but subsequently cause system distortion for smaller input signal levels.

2.2.7 Selectivity

Selectivity is defined as the ability of a receiver to select and process small incoming signals in the presence of simultaneous reception of interferers. This parameter is affected by the quality of the bandpass filters in all receiver structures and by frequency planning in heterodyne receivers specifically.

2.3 Wireless Standard Specifications

To illustrate the range of frequencies and IF bandwidths in current transceiver design, Table 2.1 shows allocation information pertaining to several commercially available wireless devices. The cellular telephone system, or wide area network (WAN), has many different operational modes and modulation schemes (AMPS, GSM, IS-95, TDMA,

Table 2.1. Frequency allocations for wireless devices.

Wireless Device	Frequency Allocation (MHz)		Channel BW (MHz)
	Receive	Transmit	
Cellular	869-894	824-849	0.030-1.25
PCS	1930-1990	1850-1910	1.25-5
WLAN 802.11.a	5725-5850	n/a	54
WLAN 802.11.b, (Wi-Fi)	2400-2484	n/a	5.5-11
Bluetooth (PAN)	2400-2484	n/a	1.0
GPS L1, civilian	1565.4-1585.4	n/a	1.0
GPS L2, military	1217.6-1237.6	n/a	1.0-10

CDMA, etc...), but all of these devices operate using the frequencies of the cellular or PCS wireless spectrums shown in Table 2.1.

With regard to wireless local area networks (WLAN), and personal-area networks (PAN), no specific transmit frequency is shown as these devices reuse frequencies via different modulation techniques, the details of which are beyond the scope of this work. Also, in view of the fact that the global positioning system (GPS) is receive only, no transmit frequency is shown for that standard.

Additionally, commercially available SAW filters are routinely incorporated for intermediate frequency (IF) discrimination in receiver architectures for cellular telephone standards, with these IF frequencies ranging from 85 MHz to 400 MHz [11]. Although required IF frequencies vary widely depending on the receiver type and frequency plan, this information provides a general idea of current commercial IF frequency requirements. Dynamic range requirements associated with some wireless standards for cellular telephone, WLAN, and PAN are presented in Table 2.2 for reference.

Table 2.2. Wireless standard dynamic range requirements.

Receiver Type	Dynamic Range (dB)
CDMA Cellular	79 (-104 to -25 dBm)
GSM Cellular	87 (-102 to -15 dBm)
Bluetooth PAN	50 (-70 to -20 dBm)

These specifications are important in determining the practicality of implementing front-end integrated RF CMOS filters as these filters have finite maximum input signals and minimum noise characteristics which fundamentally limit the dynamic range achievable in the overall receiver.

2.4 Wireless Receivers: Conclusion

This chapter has presented different wireless receiver architectures and specifications along with information regarding current wireless standards. One key observation should be highlighted at this point. For any of the receiver architectures or frequency plans implemented, and for all the passive discrete components that can be eliminated, off-chip RF filtering is a continuing requirement at the front-end of any receiver and is still typically implemented using discrete SAW filters. These facts justify and motivate continued research in regards to the on-chip implementation of RF filters with the potential of eventually contributing to the integration of complete RF systems into prospective single-chip RF and microwave receiver solutions.

CHAPTER 3

CONTINUOUS-TIME INTEGRATED FILTERS

Continuous-time integrated filters have been the focus of research and development for decades, and different implementations of this type of filter are applied in circuits spanning near-dc frequencies to the gigahertz microwave spectrum. The motivation for the integration of filters in RF systems, as with other circuit blocks, is generally to eliminate discrete off-chip components in the goal of creating single chip circuits or systems. The following sections discuss several types of integrated filters and evaluate circuit topologies, the components that make up these types of circuits, and general design and performance challenges. The intent of this presentation is to continue the establishment of a foundation from which to base subsequent discussion regarding the RF filter design work that is the focus of this research.

First, four types of integrated filters that are studied and implemented in current commercial circuit designs and ongoing research efforts are discussed. These four types of circuits, which are presented in chronological order based on the date of their initial development and introduction, are Active RC, MOSFET-C, Gm-C, and Q -enhanced LC filters. Information regarding the operational theory for these filters as well as some specific design applications is provided. Given that the focus of this research effort is in

RF filters, greater coverage is given to Gm-C and LC Q -enhanced filters based on the applicability of these topologies to higher frequency band-selective circuits.

Next, the integrated components required to construct these filter circuits is outlined and discussed. The components reviewed include resistors, capacitors, inductors, and transformers.

Finally, the chapter concludes with a discussion of challenges that are unique to the design and implementation of CMOS integrated filters, particularly for RF and microwave applications. The challenges discussed include dynamic range, noise, linearity, tuning, and power consumption.

3.1 Active RC and MOSFET-C Filters

Active RC filters utilize resistors, capacitors, and operational amplifiers (op-amps) to realize integrator blocks that can be used to construct higher-order filters. This type of filter structure is practical for low and sub-megahertz frequencies, but the limited bandwidth of the required op-amps greatly prohibits usage in RF applications [12]. Also, the relatively low accuracy of capacitors and resistors in standard CMOS processes along with component drift attributable to environmental variations creates a necessity for tuning of this filter structure via device trimming.

The MOSFET-C filter is a different method for realizing similar integrator circuits that allows for electronic tuning of the circuit corner frequency, rather than tuning via device trimming [13]. An active RC integrator and the MOSFET-C counterpart are shown in Figure 3.1.

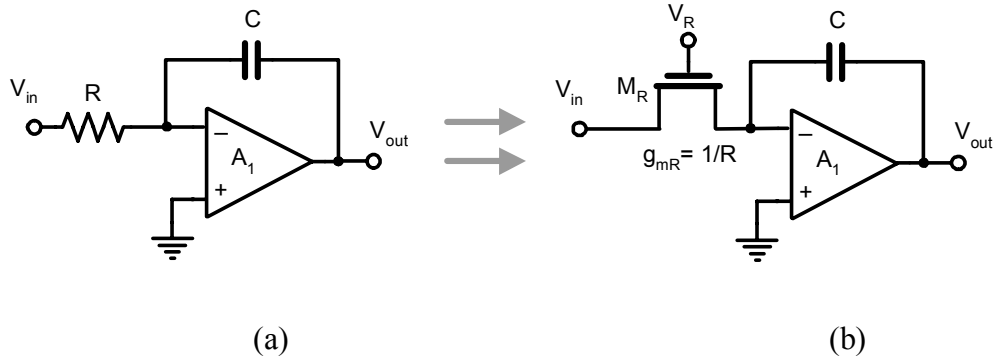


Figure 3.1. Integrators. (a) Active RC. (b) MOSFET-C equivalent circuit.

The MOSFET-C structure closely resembles the active RC integrator implementation but replaces the passive resistor with a metal-oxide semiconductor (MOS) transistor. The principle of using the transconductance of an active device as a tunable resistor was originally examined in bipolar and JFET processes [14] and was later refined to facilitate implementation in CMOS [15]. The MOS transistors, biased in the triode or linear region, are utilized to create the necessary resistance values. The transistor, M_R in Figure 3.1, for the MOSFET-C implementation directly replaces resistor, R , in the active RC circuit. Assuming that the op-amp, A_1 , in Figure 3.1 has an open-loop gain approaching infinity, the transfer function for the active RC integrator is given by

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sRC} = -\frac{\omega_c}{s} \quad (2)$$

where ω_c is the corner frequency. The transfer function for the MOSFET-C integrator is

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{g_m}{sC} = -\frac{\omega_c}{s}. \quad (3)$$

The control voltage, V_R , for the MOSFET-C filter can be varied to change the transconductance value, g_{mR} , of M_R , facilitating electrical adjustment of the corner frequency. The MOSFET-C filter is not only tunable, but allows realization of high effective resistance values with smaller required on-chip area by replacing a large integrated resistor with a MOS transistor. However, the incorporation of active devices introduces non-linearity in the MOSFET-C circuit, and like the active RC topology, the frequency range for this type of filter is still limited by the frequency response of the op-amps.

3.2 Gm-C Filters

Another method for implementing on-chip filters is by the use of Gm-C integrator blocks that are composed of transconductors and capacitors. The substitution of wide-band open-loop transconductors for the op-amps used in MOSFET-C filters allows for higher frequencies of operation in this filter structure, with the practical implementation of Gm-C filters being proven up to frequencies in the hundreds of megahertz [16]. At this frequency range, these types of filters could possibly be utilized as replacements for discrete IF filters, which commonly range in frequency from tens to hundreds of megahertz.

The limitations for this type of filter circuit are mainly in the non-idealities of the transconductors, specifically the finite output resistance and parasitic poles and zeros [17]. These intrinsic characteristics cause excessive phase shift and inherently limit the upper operational frequencies, restricting this type of filter from being used in gigahertz range applications.

3.2.1 Gm-C Integrator

Figure 3.2 represents the basic circuit diagram of a single-ended Gm-C integrator.

The transfer function for this circuit is given by

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{m1}}{sC} = \frac{\omega_c}{s}. \quad (4)$$

As detailed in Equation (4), this type of circuit facilitates electronic tuning of the integrator corner frequency via adjustment of the transconductance, g_{m1} . It is also clear from the transfer characteristics of this integrator that the frequency response of this circuit is dependant on C and g_{m1} , and the limits of these components now set the operational limits of the integrator circuit. Equation (4) also shows that in order to increase the corner frequency, the capacitance must be decreased or the value of the transconductance must be increased. This tradeoff between transconductance and capacitance sets one of the fundamental constraints in utilizing Gm-C integrator for RF applications: Increased transconductance requires increased power consumption and/or larger active device requirements with increased associated parasitic capacitance. Alternately, the minimum capacitance value is fundamentally limited by the intrinsic parasitic capacitors of active devices connected to the g_{m1}/C node.

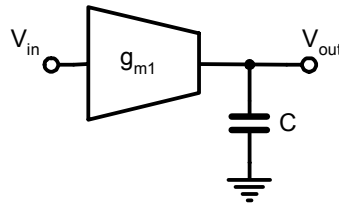


Figure 3.2. Gm-C integrator.

Previous research effort pertaining to filters based on Gm-C integrators has shown that these circuits are fundamentally limited to sub-gigahertz frequency bands [18].

3.2.2 Basic Transconductor Structure

A more detailed circuit diagram of a basic differential transconductor biased with a tail current source is shown in Figure 3.3. In Figure 3.3, V_{inp} and V_{inn} are the differential voltage inputs while I_{outp} and I_{outm} are the differential current outputs. A variation in the bias voltage, V_{bias} , creates a variance in the quiescent operating current of the differential pair, M_1 and M_2 . This variation of the dc operating current allows electrical adjustment of the transconductance of the device, which facilitates the tuning of the Gm-C filter structures that are designed around this type of circuit.

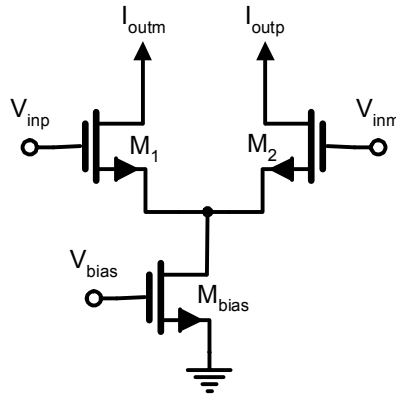


Figure 3.3. Differential transconductor circuit diagram.

3.2.3 Gm-C High-Pass Filter

Figure 3.4 shows the use of a differential transconductor connected as a pseudo-resistor to emulate the high-pass transfer function of a simple RC filter.

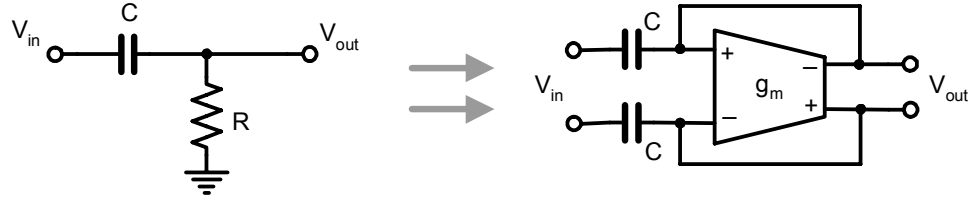


Figure 3.4. RC high-pass filter and differential Gm-C equivalent circuit.

As shown in the figure, connecting a transconductor with the current outputs fed back to the voltage inputs of opposite polarities creates a simulated resistance with the value of $R = 1/g_m$. The transfer function for the high-pass RC filter is given by

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{R}{R + \frac{1}{sC}} = \frac{1}{1 + \frac{1}{sRC}} = \frac{1}{1 + \frac{\omega_c}{s}} \quad (5)$$

while the transfer function for the high-pass Gm-C filter is given by

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1/g_m}{1/g_m + \frac{1}{sC}} = \frac{1}{1 + \frac{g_m}{sC}} = \frac{1}{1 + \frac{\omega_c}{s}}. \quad (6)$$

As detailed in Equation (5) and Equation (6), the resistor, R , is replaced by the inverse value of the transconductance, g_m .

3.2.4 Gyrator

Another Gm-C filter version uses a circuit structure called a gyrator, or active inductor. The gyrator synthesizes the behavior of an inductor at the input node of the circuit using a capacitor and two transconductors as detailed in the circuit configuration of Figure 3.5.

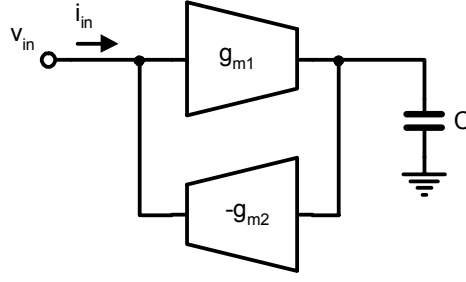


Figure 3.5. Gyrator schematic.

The gyrator topology has been an active subject of investigation [19] and exhibits the same operational limitations as the previously discussed Gm-C integrators, namely increased power consumption and reduced linearity. The input impedance, Z_{in} , of the gyrator is given by

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC}{g_{m1}g_{m2}} \quad (7)$$

while the effective inductance, L_{eff} , is given by

$$L_{eff} = \frac{C}{g_{m1}g_{m2}}. \quad (8)$$

A resonator can be realized by connecting a capacitor at the V_{in} node of the gyrator and this circuit structure can be utilized to implement tunable second-order bandpass filtering [20]. These second-order circuits, as is general for any biquads, can be cascaded to realize higher order filtering functions.

3.2.5 Gm-C Bandpass Filter Example

As an example of a Gm-C integrator being utilized as a building block for a higher order filter transfer function, a circuit topology for a second-order Gm-C bandpass filter is shown in Figure 3.6. The transfer function for this Gm-C second-order bandpass filter is described by

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{g_{m1}}{C_2} s}{s^2 + \frac{g_{m1}}{C_2} s + \frac{g_{m1}g_{m2}}{C_1C_2}}. \quad (9)$$

The standard form for a general second-order bandpass filter transfer function is given by

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A \frac{\omega_o}{Q} s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \quad (10)$$

where A is the filter gain at the center frequency, ω_o .

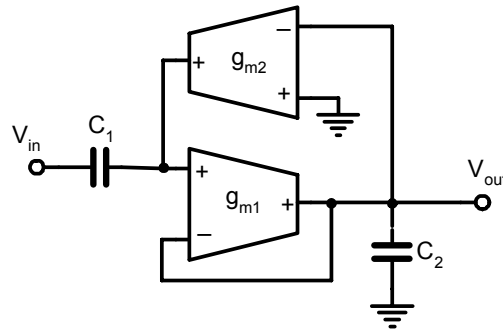


Figure 3.6. Gm-C second-order bandpass filter implementation.

From Equation (9) and Equation (10) it can be determined that the resonance frequency, ω_o , is given by

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \quad (11)$$

and the quality factor, Q , of this filter is given by

$$Q = \sqrt{\frac{C_2g_{m2}}{C_1g_{m1}}} \quad (12)$$

where Q is the ratio of the center frequency to the -3 -dB bandwidth of the filter as illustrated in Figure 3.7. As detailed in Equation (11) and Equation (12), the center frequency and quality factor of this bandpass filter can be adjusted electrically via g_{m1} and g_{m2} . Also, the center frequency can be independently adjusted without affecting Q in this particular circuit topology if g_{m1} and g_{m2} are both adjusted by the same margin.

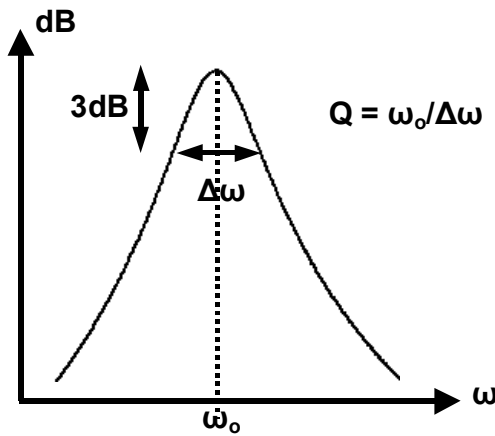


Figure 3.7. Graphical representation of bandpass filter Q .

3.3 Q -Enhanced LC Bandpass Filters Using On-Chip Inductors

As opposed to Gm-C filters, bandpass filters that utilize LC tank circuits have the advantage of being less sensitive to parasitic capacitance attributable to active device structures or on-chip signal routing. This allows for the implementation of filter circuits at higher operational frequencies, as these parasitic capacitors can actually be absorbed into the total reactance required for the design frequency. Alternately, filters based on Gm-C structures are fundamentally affected by the presence of these parasitics, where the inherent excessive capacitance values tend to increase the overall capacitance at a particular node, having the effect of reducing the highest achievable operational frequency, as previously detailed in Equation (4).

3.3.1 Q -Enhancement

Practical integrated filters rely on some form of energy restoration, or Q -enhancement, to increase the quality factor of resonators designed with lossy on-chip passive components. A primary method for increasing the Q of non-ideal on-chip resonators is through the use of active devices to create negative resistance. Although methods that include phase-shifted current feedback via coupled inductors [21] have been investigated, the direct use of active devices as negative resistors is the prevalent Q -enhancement technique. Series mode approaches for Q -enhancement have been investigated [22] that incorporate a negative resistor connected in series with a lossy on-chip inductor. However, the more commonly applied approach is through a parallel connection of the negative resistor with the non-ideal resonator circuit, a method that is more closely examined here. Single-ended negative resistance methods have been documented [23-25], while the more common differential method using a cross-coupled

transistor pair is presented in Figure 3.8. The voltage to current ratio indicates the effective negative resistance at the terminals of the cross-coupled MOSFET shown in the figure and is described by

$$\frac{v}{i} = \frac{-2}{g_{mQ}} = -R. \quad (13)$$

It is clear from Figure 3.8 and Equation (13) that the effective negative resistance can be adjusted by changing the bias source, I_Q , and thereby the transconductance, g_{mQ} , of the differential pair. This facilitates electronic tuning of this loss-canceling mechanism. The concept of Q -enhancement for an LC tank circuit with parallel-connected negative resistance is illustrated in Figure 3.9, with the series resistance inductor model utilized to simplify the analysis. The parasitic series resistance of the inductor is shown in the left of Figure 3.9, and is given by

$$r_s = \frac{\omega L}{Q_o}. \quad (14)$$

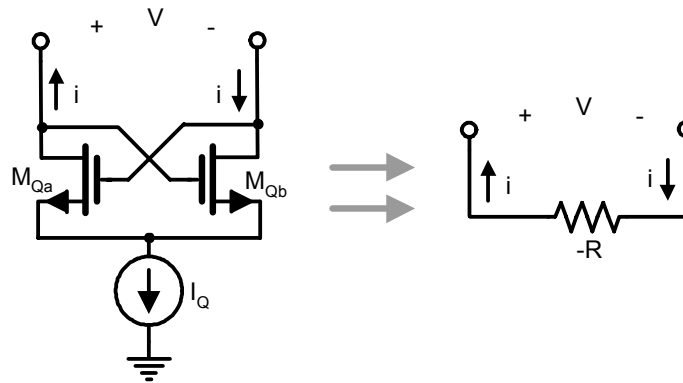


Figure 3.8. Cross-coupled MOSFET negative transconductance.

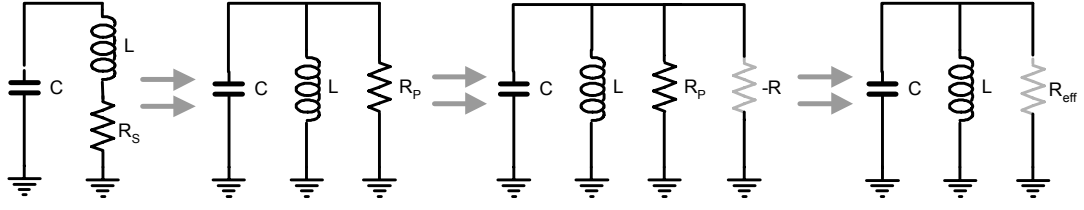


Figure 3.9. Q -enhanced LC tank circuit.

Assuming that the quality factor of the tank capacitance is much larger than the inductor, the equivalent parallel resistance of the tank is given by

$$r_p \approx r_s \times Q_o^2 = \omega L Q_o. \quad (15)$$

The negative resistance required to offset the losses and change the overall quality factor of the tank is

$$|-R| = \frac{1}{g_{mQ}} \quad (16)$$

where g_{mQ} is a transconductor utilized to generate the negative resistance. The required value for g_{mQ} is given by

$$g_{mQ} = \frac{1}{\omega L} \left(\frac{1}{Q_o} - \frac{1}{Q_{eff}} \right) \quad (17)$$

where Q_o and Q_{eff} are the intrinsic and enhanced quality factors of the tank circuit, respectively, and g_{mQ} is the value of transconductance necessary to achieve the required overall circuit quality factor. The equivalent tank resistance, R_{eff} , is the effective parallel resistance after Q -enhancement.

3.3.2 Q -Enhanced LC Bandpass Filter Example

An example differential Q -enhanced LC bandpass filter circuit that utilizes negative resistance via a cross-coupled transconductor element is illustrated in the simplified schematic of Figure 3.10. Transistors M_{Ia} and M_{Ib} provide the input stage to the filter while transistors M_{Qa} and M_{Qb} provide the tank loss restoration.

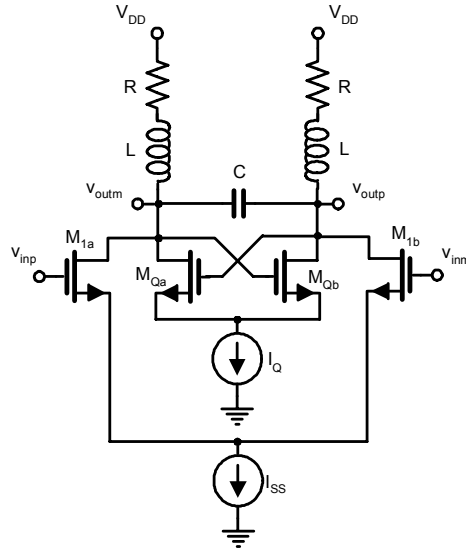


Figure 3.10. Q -enhanced LC filter schematic.

Recently investigated LC bandpass filters have implemented with circuits employing similar topologies, and the transfer function for this circuit is given by

$$T(s) = \frac{\frac{g_{mI}}{C} \left(s + \frac{R}{L} \right)}{s^2 + \left(\frac{R}{L} - \frac{g_{mQ}}{C} \right) s + \frac{1}{LC} (1 - g_{mQ} R)} \quad (18)$$

where g_{mI} and g_{mQ} are the transconductance values of the input and Q -enhancing differential pairs, respectively. If the series loss resistor, R , is replaced with an equivalent

parallel resistor, R_p , as derived in Equation (15), a simplified transfer function describing the circuit is given by

$$T(s) = \frac{\frac{g_{m1}}{C}s}{s^2 + \frac{1}{C}\left(\frac{1}{R_p} - g_{mQ}\right)s + \frac{1}{LC}}. \quad (19)$$

Now, comparing Equation (19) to the standard form for a second-order bandpass filter transfer function presented earlier in Equation (10), it can be determined that the resonance frequency, ω_o , and Q of the bandpass filter are given by the following:

$$\omega_o = \frac{1}{\sqrt{LC}} \quad (20)$$

$$Q = \frac{R_p C}{\sqrt{LC}(1 - g_{mQ}R_p)} \quad (21)$$

$$= \sqrt{\frac{C}{L}} \frac{R_p}{(1 - g_{mQ}R_p)}$$

$$= \sqrt{\frac{C}{L}} \frac{\omega_o Q_o L}{(1 - g_{mQ}R_p)}$$

$$= \frac{\sqrt{\frac{C}{L}} \frac{1}{\sqrt{LC}} Q_o L}{(1 - g_{mQ}R_p)}$$

$$Q = \frac{Q_o}{(1 - g_{mQ}R_p)} \quad (22)$$

From Equation (21) and Equation (22) it is evident that by increasing the value of g_{mQ} the overall quality factor of the filter structure is increased. The result in Equation (22) also shows that with g_{mQ} equal to zero, the value of Q is equal to the quality factor of the inductor, Q_o , as expected.

Also, there is one other issue pertaining to a design constraint in this circuit. If the dc losses in the inductors are assumed negligible, the bias voltages at the gate and drain for both transistors in the cross-coupled pair, M_{Qa} and M_{Qb} , are at identical dc levels. The equal bias levels cause these devices to approach the triode region of operation for large tank signal swings having a peak level of $V_T/2$ or greater, where V_T is the threshold voltage of M_{Qa} or M_{Qb} . This is a result of the signal voltages, superimposed on the dc levels of the gates and drains, maintaining equal magnitudes but opposite polarities.

3.3.3 Quantitative Comparison of Q -Enhanced LC and Gm-C Filters

The dynamic range of Gm-C filters has been quantitatively shown to be inherently limited [26] and inversely proportional to the quality factor, Q , of the designed filter circuit [27]. Although the dynamic range of an LC bandpass filter also exhibits this inverse Q proportionality, detailed analysis and comparison have been accomplished [28] which show that active LC filters exhibit a dynamic range improvement of Q_o compared to the Gm-C circuits designed for the same frequency response characteristics. Q_o is the intrinsic quality factor of the inductor, as noted previously, and is usually assumed to dominate the overall quality factor of the resonator in the filter circuit. It has also been shown [28] that with fixed bandwidth and power consumption, the dynamic range of a Gm-C filter structure is actually inversely proportional to the *square* of the filter Q and that an equivalent active LC filter exhibits a dynamic range improvement of Q_o^2 .

3.3.4 Qualitative Comparison of Q -Enhanced LC and Gm-C Filters

The dynamic range and power consumption of Gm-C and Q -enhanced LC bandpass filters can be qualitatively compared by examining the location of the poles extracted from the characteristic equations for the second-order order bandpass filters examined earlier: Equation (9), Equation (18), and Equation (19). Bandpass filter circuits using LC resonators create complex poles intrinsically as a result of the interaction of the two oppositely reactive components in the tank. In other words, the poles of this type of filter are naturally removed from the real axis ($Q > 1/2$) and lie in the complex plane. The active devices in the LC filter circuit are only required to rotate the poles closer to the imaginary axis to decrease circuit losses, or enhance the overall quality factor. This is advantageous in comparison to the Gm-C filter in which active circuit devices in this type of circuit have the burden of lifting the poles from the real axis into the complex plane. This necessity of active devices to create, rather than enhance, complex poles increases the power consumption of Gm-C filters and also raises the noise floor, which degrades the achievable dynamic range.

Figure 3.11 presents a general graphical comparison of two second-order bandpass filters, Gm-C and Q -enhanced LC, and how the poles of these circuits might lie in the complex plane. In Figure 3.11, the lighter plot represents the Gm-C bandpass circuit and is a general locus of pole locations for the transfer function of the second-order filter described previously in Equation (9).

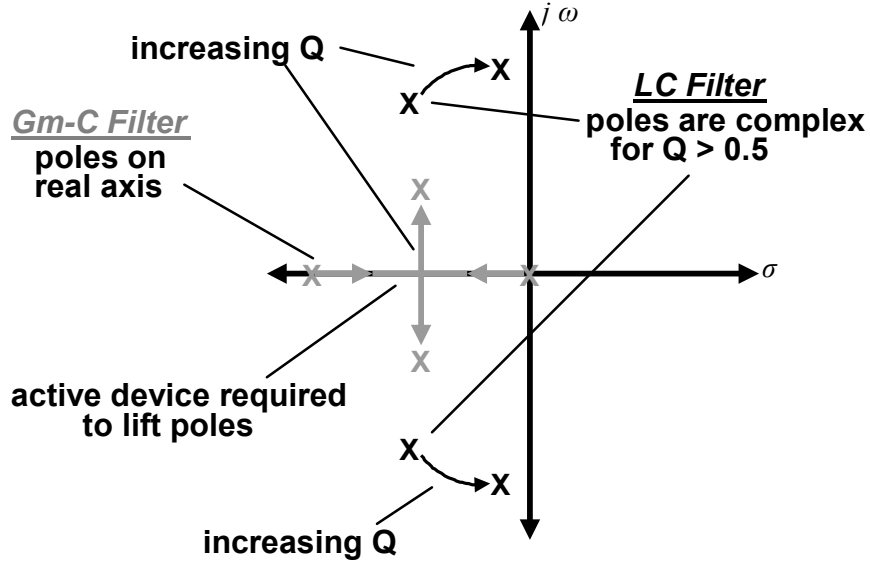


Figure 3.11. Location of poles for second-order Gm-C and LC bandpass filters.

For the plots shown in Figure 3.11, the values of capacitors C_1 and C_2 from Equation (9) are held constant, as is the value of g_{m1} . As g_{m2} is increased from zero to some finite value the poles are shifted together and then moved into the complex plane, increasing the Q and shifting the center frequency.

Alternately, the darker plot in Figure 3.11 shows the pole locations for a Q -enhanced LC tank filter. By increasing the value of g_{mQ} , refer to Equation (18) or Equation (19), the poles are rotated closer to the $j\omega$ -axis and the overall circuit Q is increased. The active device, g_{mQ} , in the LC filter takes on a supplementary rather than primary role leading to the intuitive conclusion that the non-idealities of this Q -enhancing element should have less of a factor in any degradation of the overall filter characteristics as compared to the transconductors in Gm-C filters.

3.4 Integrated Passive Components

This section backtracks somewhat and discusses the properties and characteristics of several integrated circuit passive components required to construct on-chip filters. This discussion includes an overview of integrated capacitors, resistors, inductors, and transformers. A thorough coverage is specifically provided for on-chip inductors and transformers, as these are key components in the operation of the transformer-feedback Q -enhanced bandpass filter that is the focus of this research. Other component characteristics such as specific achievable values as well as relative and absolute component value accuracy are omitted, but can be referenced in texts dedicated to CMOS circuit analysis and design [29,30].

3.4.1 Integrated Capacitors

Integrated capacitors are used in IC designs for their frequency-specific impedance characteristics or as signal coupling and bypass components. Although integrated components have characteristics unique to the IC process, general rules governing the values of capacitance apply. The following paragraphs present information for lateral inter-trace capacitors, vertically oriented metal-insulator-metal (MIM) capacitors, polysilicon capacitors, and MOS capacitors.

To begin the discussion on integrated capacitors, general formulas for calculating simple parallel plate capacitance are presented. The formula for a simple parallel plate capacitor is given by

$$C \cong \frac{A\epsilon_o\epsilon_r}{d} \quad (23)$$

where C is the capacitance in pF, A is the smallest area of two facing conductive plates in μm^2 given by the conductor thickness (t) and length (l), and d is the distance between conductors in micrometers. Also, ϵ_o is the permittivity of free-space and ϵ_r is the relative permittivity of any material present between the plates of the capacitor. The capacitance value given by Equation (23) does not account for fringing effects. These effects can normally be neglected when both the width and height of the capacitor plates are significantly larger than the plate separation. In cases where the dimensions of the capacitor plate area are not significantly larger than the spacing, a non-exact first-order approximation for the capacitance is given by [31]

$$C \cong \epsilon_o \epsilon_r \frac{(t + 2d)(l + 2d)}{d}. \quad (24)$$

Two closely spaced parallel conductors fabricated from a single IC process layer generate a laterally oriented electrical field. Figure 3.12 presents a graphical representation of a lateral inter-trace capacitor formed from two traces in a single metal layer.

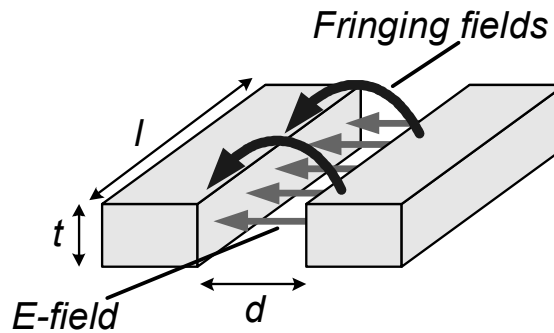


Figure 3.12. Graphical representation of lateral inter-trace capacitor.

This capacitance would normally be considered parasitic when associated with integrated circuit signal paths. In Figure 3.12, the area of the capacitor plates is the product of the conductor thickness (t) and length (l), while the distance (d) is the spacing between conductors. Designations for the electric field between the conductors and the fringing fields shown for the topside of the conductors are also shown for reference. The lower fringing fields are omitted for visual clarity. Also, in the case of the small dimensions of the ‘side’ of the metal traces that act as the plates of the parasitic lateral capacitors examined in the adjacent traces used for signal conduction in an IC layout, fringing effects must be taken into account, and Equation (24) may be a more accurate method of calculating this parasitic capacitance.

The physical structure of metal-insulator-metal capacitors would be similar to the diagram presented in Figure 3.12, with the difference being in the metal traces from two different metal layers creating a vertical electrical field with the dielectric insulator between the metals determined by the particular IC process. Figure 3.13 shows the orientation along with associated physical dimensions references and electric fields of a MIM capacitor composed of adjacent process metals.

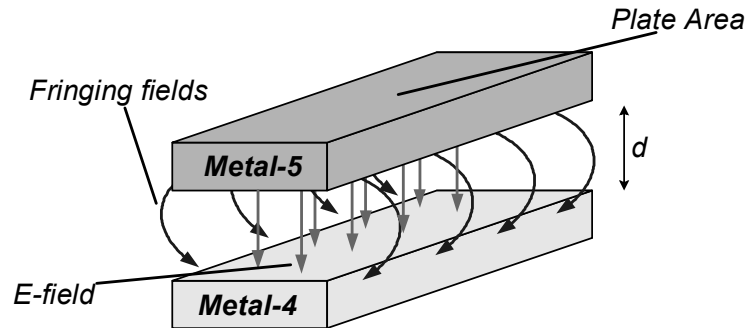


Figure 3.13. Graphical representation of a MIM capacitor.

Either Equation (23) or Equation (24) can be used, based on the dimensions discussed previously, to make rough predictions of the MIM capacitance value between closely spaced metals residing in different layers of the IC. Additionally, polysilicon process layers can also be used as capacitor plates with an orientation similar to the MIM capacitor.

MOS transistors can also be utilized to implement integrated capacitors. With this type of capacitor, variations in bias potentials at the bulk, gate, drain, and source connections allow different modes of implementation. Dynamic variation of these potentials also provides a method to create an electrically adjustable capacitor, or varactor, that would be commonly used to adjust the frequency of an integrated oscillator or filter. Figure 3.14 shows cutaway views of two different MOS capacitors in an n-well process: Standard mode and accumulation mode. Figure 3.14(a) shows a standard mode MOS capacitor. As shown in the figure, the bulk (B), source (S), and drain (D) of the device are connected together and would normally be tied to ground with the gate (G) connected to a bias supply to invert the positively doped substrate underneath the gate.

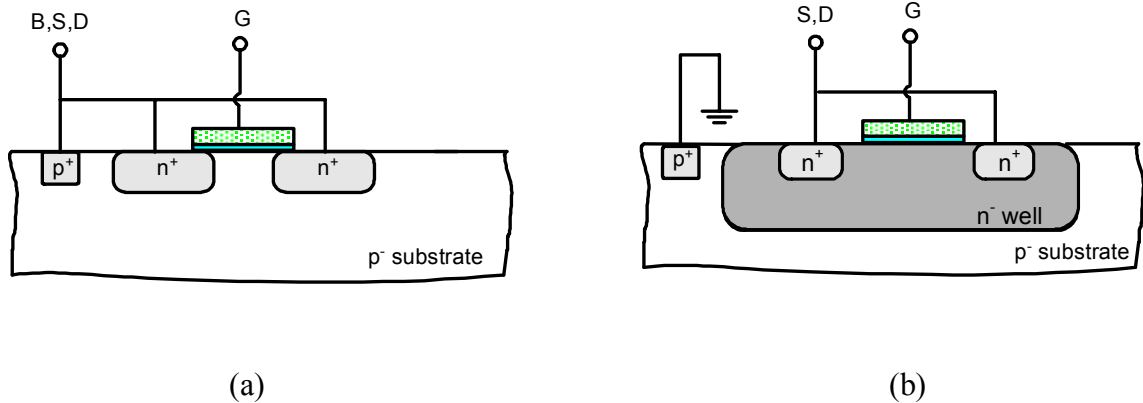


Figure 3.14. MOS capacitors: (a) Standard mode. (b) Accumulation mode.

With the channel inverted, the capacitance is proportional to the gate area and inversely proportional to the gate oxide thickness, with the gate and inverted channel acting as the plates of the capacitor. This infers that shrinking process dimensions, and subsequent inherently thinner gate oxides, facilitate increasing capacitance. Figure 3.14(b) shows an accumulation mode MOS capacitor. This device also uses the transistor gate as one of the capacitor plates, but the advantage over standard mode is that the device remains in accumulation mode for larger gate/source voltage swings. Additionally, the accumulation mode MOS capacitor can be implemented omitting the drain and source diffusions with the gate and n-well acting as a two-terminal device.

For the transformer-coupled RF bandpass filter that is the subject of this research work, the relatively large integrated capacitance provided by standard mode MOS capacitors is specifically used for small-signal bypass of bias supplies. Also, the two-terminal device is utilized for a relatively small capacitor in the resonant tank of the filter. All other circuit capacitance is primarily attributable to parasitics associated with circuit transistors as well as any closely spaced metal traces that are used for signal routing.

3.4.2 Integrated Resistors

CMOS integrated resistors are usually implemented with three devices. An n-well resistor is constructed using n-wells formed at specific lengths and widths with drain/source diffusion contacts at each end. This type of resistor generally provides the largest resistance per square available in a typical CMOS process. A MOS resistor is created using source and drain diffusions with varying doping levels and provides a medium range of resistance per square. Finally, the polysilicon resistor is formed using process

poly and provides the lowest range of resistance per square. A more rigorous analysis of these integrated components including typical values and accuracies can be found in [29].

Although design of RF circuits and systems generally calls for a reduction of resistors to minimize induced noise, the RF bandpass filter in this research uses one $50\ \Omega$ polysilicon resistor at the front-end of the circuit. This component is used to provide input matching for interface to test signal generators and other required measurement and source instruments. This simple and accurate matching method was used to alleviate any potential filter response alteration arising from a frequency-dependant reactive-based matching network that might be typically implemented in an RF front end.

3.4.3 Integrated Inductors

At frequencies in the tens to hundreds of megahertz, on-chip inductors in the lower nanohenry range are impractical for integrated bandpass filter designs. This is a result of the low inductive reactance exhibited at these sub-gigahertz frequencies and high values of capacitance needed to resonate with these inductors. Also, increasing the inductance to values of practical application in this sub-gigahertz frequency range requires a prohibitively large use of chip area. However, as the frequency of interest for signal filtering increases into the gigahertz range, the reactance of lower value inductors becomes significant enough to allow the utilization of these components in circuit designs. The availability of these on-chip inductors with steadily increasing quality factors along with the necessity to create filters at gigahertz frequencies has led to active research and development of on-chip filters in CMOS based on integrated LC resonant tank circuits [32-34].

The analysis, simulation, and fabrication of on-chip inductors in standard CMOS processes are currently active areas of research [35-41] as is the development of software modeling tools for these components [42]. Recent work has yielded inductors with values ranging from 1-10 nH at operational frequencies up to 10 GHz utilizing Aluminum conductors in a standard silicon process [43]. This same work also details quality factors, Q_o , at levels between five and ten at these inductance values and frequencies, where Q_o represents the inductor quality factor and is defined as the ratio of the imaginary part to the real part of the total impedance of the inductor. With these points established, it is logical to assume that the quality and reliability of integrated inductors will only continue to increase. Given this fact, existing or developing designs utilizing on-chip LC resonators can be used as templates on which to base future circuit topologies with inductors possessing predictably increasing quality factors. The following paragraphs provide information on integrated inductor layout, lumped-element modeling, and simulation methods for extracting inductor electrical properties.

The integrated inductor is composed of traces formed from one or more metal layers in an IC process. Usually, the thickest metal available in the process is utilized for inductor design to take advantage of the lowest sheet resistance and permit the highest inductor quality factor. This is normally the top-most metal layer. To construct the inductor, a metal trace is normally wound in a specific geometric form in the chosen metal, and connection to a lower metal layer is used as an underpass to provide an exit path out of the center of the coil or allow overlap of interwound traces. Two typical integrated inductor layouts utilizing a single-layer coil and a second metal underpass are presented in Figure 3.15.

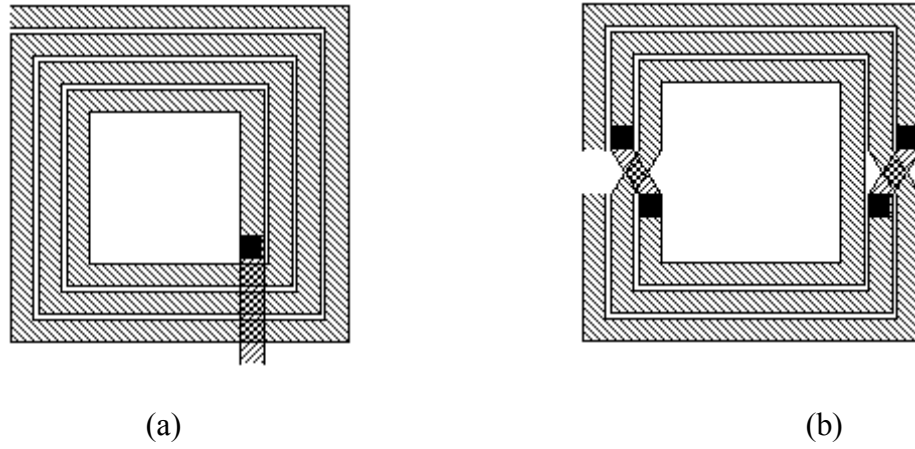


Figure 3.15. Inductor layouts. (a) Square spiral. (b) Square symmetric.

In Figure 3.15, the underpass metal is not highlighted, but is used whenever traces cross paths, while the vias connecting the two metals are shown as solid black squares.

For simplification of circuit analysis and initial filter design, on-chip inductors can be approximately modeled with the inductance value and a series resistor, as shown in Figure 3.16. This is similar to the modeling of discrete inductors, which generally only requires an accounting for the resistive losses in the coil. The inductor quality factor for this simplified series resistance model is given by

$$Q_o = \frac{\omega_o L}{R_s} \quad (25)$$

where ω_o is the center frequency of operation and $\omega_o L$ is the reactance of the inductor.

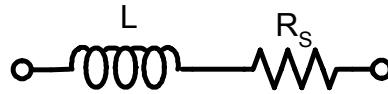


Figure 3.16. Simple series resistor model for the inductor.

In practice, integrated inductor electrical characteristics are generally frequency dependent and are more precisely described with a lumped-element model of greater complexity. A commonly used square-spiral IC layout and a more accurate electrical model for the inductor, the π -model, are shown in Figure 3.17. In this model, R_s represents the resistive losses in the metal traces of the inductor, any contact losses, and losses attributable to eddy currents in the substrate. Note that the top branch of Figure 3.17(b), which is composed of series resistor, R_s , along with the inductance, L , represents the simplified series resistance model for the inductor shown in Figure 3.16. The metal-to-substrate capacitance is modeled by C_p , and R_p represents loss caused by substrate conductance. A capacitor connected in parallel with L and R_s is sometimes incorporated to model interwinding capacitance between inductor traces [38], but is not shown in this model. For a general frame of reference, values reported for these π -model schematic components for one particular on-chip spiral inductor [44] are given in Table 3.1.

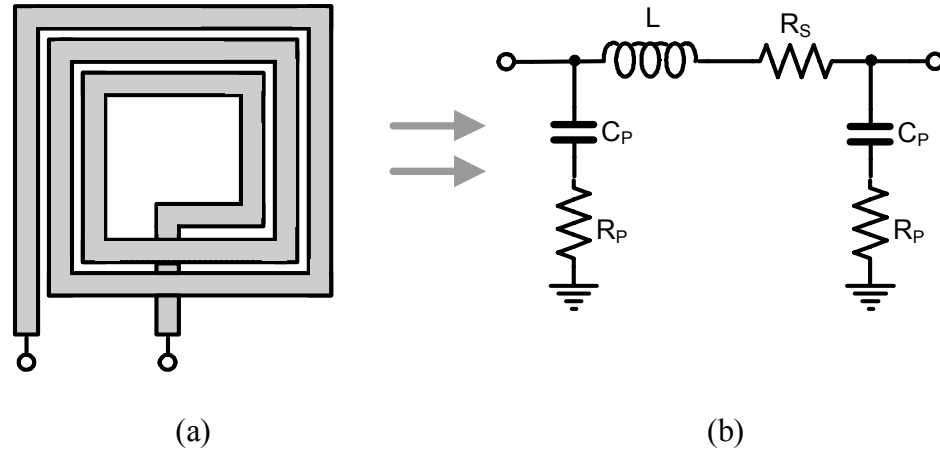


Figure 3.17. Integrated inductor. (a) Layout. (b) π -model schematic.

Table 3.1. Integrated inductor example values.

Component	Value
L	4 nH
R_s	6 Ω
R_p	90 Ω
C_p	200 fF
Q_o	~ 6

It is intuitively evident from the π -model, based on the inclusion of the additional reactive components in this more detailed lumped-element representation, that an actual integrated inductor possesses a complex characteristic frequency response. This leads to the conclusion that the simple inductor model is only precise for a narrow band of frequencies, and though useful for initial filter analysis and design, has limited wideband practicality.

Finally, to extract the lumped-element component values for the π -model, the ASITIC simulation program (Analysis and Simulation of Spiral Inductors and Transformers for ICs) was employed. This program is a well-established simulation tool that calculates the parameters for the π -model taking into account skin effect, crowding effects, and eddy current losses. For the purposes of the circuit designs and associated simulations used in this research effort, all inductors used lumped element π -models extracted from ASITIC analysis of the utilized layout topologies.

For the transformer-coupled RF bandpass filter that is the subject of this research work, the square-spiral inductor is used for transistor degeneration and linearization of the circuit Q -enhancement transistor while a variation of two square symmetric inductors are used as part of the integrated transformer in the circuit resonant tank.

3.4.4 Integrated Transformers

Integrated circuit transformers are the focus of ongoing research [45-47] and are generally realized with two different physical layouts. These ‘monolithic’ transformers can be constructed from interwound conductors residing in the same plane, i.e. ‘planar’ transformers using the same metal layer, or can also be created from conductors residing in different metal layers, i.e. ‘stacked’ transformers. Either design method relies on multiple circuit traces located within a proximity that allows magnetic coupling to produce mutual inductance between the conductors. Mutual inductance and the associated coincident mutual capacitance produced are generally proportional to the peripheral length of each winding so interleaving or stacking of metal traces maximizes the physical periphery and subsequently increases achievable inductance and capacitance. The coupling coefficient, k , between two or more conductors is determined by the mutual and self-inductances and is dependant on the width and spacing of the traces and the substrate thickness.

The following sections present three different planar integrated transformer implementations in chronological ordering based on the original introduction date of each topology along with a discussion of the associated electrical properties of these components. These electrical properties are extracted from ASITIC simulations using National CMOS-9 process parameters. All of the planar transformer layouts presented are designed with similar coil dimensions and spacing, creating similar inductance values and allowing for a direct comparison of the electrical properties of these three layout topologies. Also, the primary and secondary coils of the planar transformers shown in Figure 3.18, Figure 3.19, and Figure 3.20 would be fabricated in the same metal layer,

but are shown in different shades to allow clear visual distinction between the two coils. Additionally, a brief discussion regarding some of the operational characteristics of stacked monolithic transformers is undertaken to conclude this section. Finally, the information presented in this section is not intended to be an exhaustive study of all integrated transformer implementations, but introduces and discusses planar and stacked transformers with additional details presented regarding the characteristics of transformer topologies that relate more specifically to the efforts of this research work.

A layout diagram and simulated electrical characteristics of a planar parallel conductor transformer are shown in Figure 3.18. This layout was first introduced as a microstrip design in 1981 by Kobi Shibata et al. [48] and is referred to here as the ‘Shibata transformer’. In the figure, the primary (P+, P-) and secondary (S+, S-) designators describe the polarities of the transformer connections.

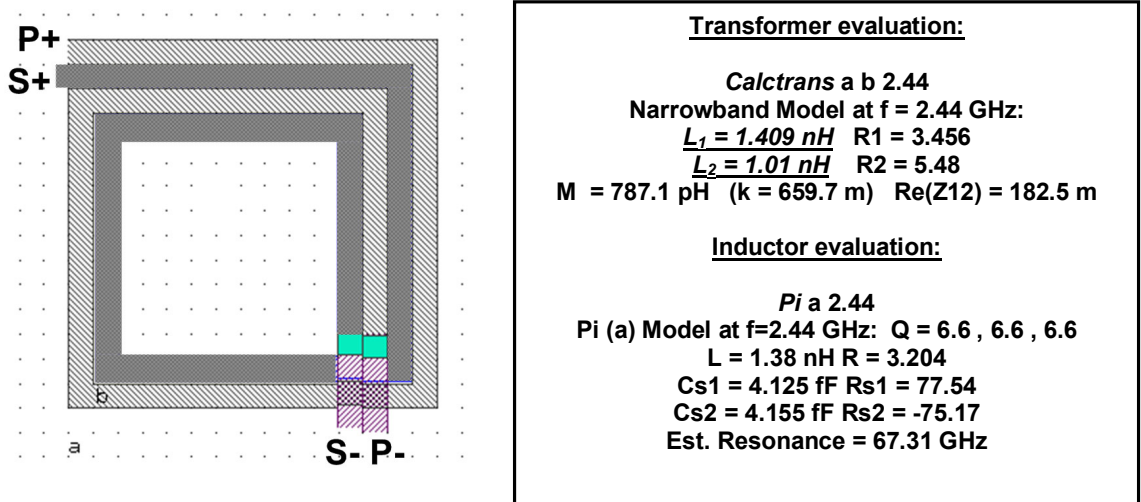


Figure 3.18. Shibata transformer layout and ASITIC simulation results.

The simulation results presented in Figure 3.18 detail the electrical characteristics of the Shibata transformer as well as the properties of one of the transformer coils. As illustrated in the figure, inherent differences in primary and secondary winding lengths make the Shibata transformer layout physically and electrically asymmetric, and a transformer ratio of 1:1 is not achievable. This non-symmetric property subsequently produces coupled coils with different inductance values, as indicated by the underlined L_1 and L_2 component values shown in the ‘Transformer Evaluation’ section of the figure.

An improvement on the Shibata transformer topology is the planar interwound transformer shown in Figure 3.19. This layout was introduced in 1989 by E. Frlan et al. [49] in one of the earliest analysis of monolithic transformers and is referred to here as the ‘Frlan transformer’. In the figure, the primary (P+, P-) and secondary (S+, S-) designators describe the polarities of the transformer connections.

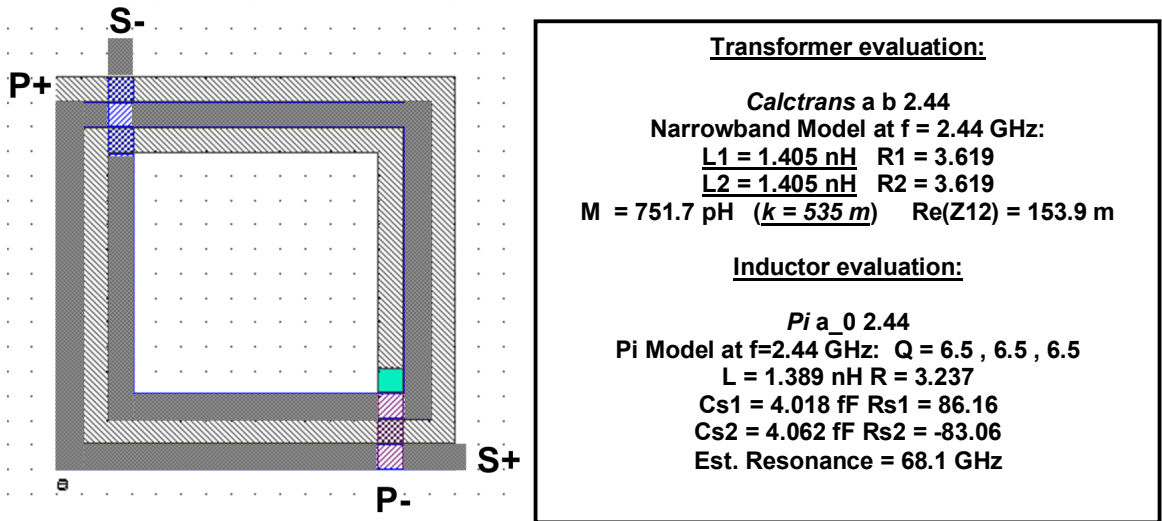


Figure 3.19. Frlan transformer layout and ASITIC simulation results.

The simulation results presented in Figure 3.19 detail the electrical characteristics of the Frlan transformer as well as the properties of one of the transformer coils. As illustrated in the figure, the Frlan transformer layout uses identical interwound spirals that facilitate symmetry from primary to secondary, allowing the realization of a 1:1 turns ratio. This symmetric property produces coupled coils with equal inductance values but produces a lower coupling coefficient than the Shibata transformer. These characteristics are underlined in the ‘Transformer Evaluation’ section of the figure.

A third planar transformer topology is the symmetric-square layout shown in Figure 3.20. This layout was introduced as an integrated 4:5 balun in 1991 by Rabjohn [50] and is referred to here as the ‘Rabjohn transformer’. In the figure, the primary (P+, P-) and secondary (S+, S-) designators describe the polarities of the transformer connections.

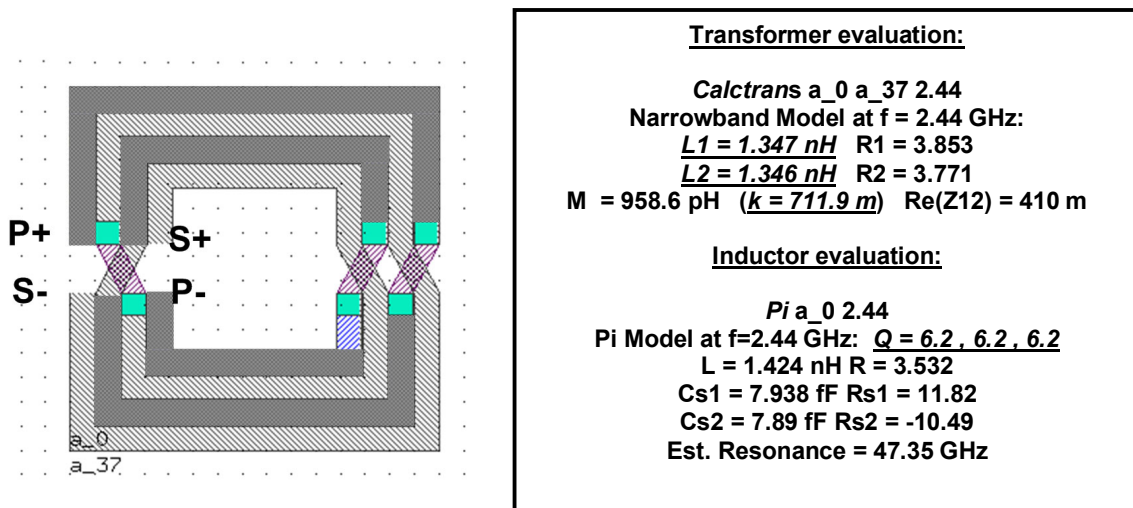


Figure 3.20. Rabjohn transformer layout and ASITIC simulation results.

The simulation results presented in Figure 3.20 detail the electrical characteristics of the Rabjohn transformer as well as the properties of one of the transformer coils. As illustrated in the figure, the Rabjohn transformer consists of two interwound coils that are symmetric to the horizontal center axis of the device. This topology maximizes the adjacent periphery of the coils leading to an increased coupling coefficient and the symmetric properties of this layout produce coupled coils with equal inductance values. These characteristics are underlined in the ‘Transformer Evaluation’ section of the figure.

The last monolithic transformer type discussed is the stacked inductor topology. This implementation can provide large inductor coupling coefficients but also suffers from increased interwinding capacitance. This capacitance is a result of the close spacing between surface areas of the top and bottom parallel conductors existing in adjacent metal layers, which effectively creates metal-insulator-metal (MIM) capacitors. However, it has been shown that this increased capacitance can be mitigated without significant mutual inductance degradation by offsetting the coils [45]. Also, intrinsic quality factors in these devices can be increased by connecting contiguous metal layers in parallel to serve as a single conductor, decreasing the overall effective sheet resistance. For example, in the CMOS-9 process, the top metal layer (Metal-5) would be utilized as one transformer coil while the more lossy metal layers, Metal-3 and Metal-4, could be connected in parallel to act as the second transformer coil.

Additionally, it should be noted that any of the discussed transformer topologies have inherently low intrinsic quality factors. This is a result of the lower conductance properties inherent to the thin-layer aluminum used in typical CMOS processes. Also, patterned ground shields for transformers and inductors may be utilized to isolate the

coils from the substrate and increase component Q , but any use of integrated transformers for high- Q designs requires some additional compensation for the intrinsic losses of these components.

Finally, for the transformer-coupled RF bandpass filter that is the subject of this research work, the Rabjohn topology is utilized in a slightly modified implementation to create a 1:1 transformer. This particular layout was chosen for the intrinsic symmetrical inductance characteristics and comparatively large coupling coefficient.

3.5 Challenges of Integrated Filters

Like analog circuits in general, radio-frequency integrated circuit (RFIC) designs suffer from required tradeoffs that include linearity, noise, power, frequency, gain, and supply voltage [5]. Additionally, integrated filters present a further specific challenge in that automatic tuning is also required. The following sections will present information regarding the challenges and tradeoffs of integrated filter implementation.

3.5.1 Dynamic Range: Noise and Linearity

As defined earlier, dynamic range is the ratio of the minimum and maximum signals that a circuit or system can accurately process. The utilization of Gm-C filters requires the use of active devices in order to achieve particular pass-band characteristics while LC filters require active devices for the Q -enhancement of intrinsically lossy on-chip passive components. This inclusion of active devices increases the noise floor of the circuit, which can be a detriment to overall receiver sensitivity. Also, compression effects in the transistors limit the maximum input signal level, and as the supply potentials shrink along with device geometries in newer IC processes, this compression problem becomes increasingly prohibitive in overall circuit operation.

To lessen the impact of dynamic range degradation inherent in active filter circuits, the implementation of integrated filters is normally accomplished using differential circuit topologies that enhance both linearity and sensitivity. Utilizing differential circuits, as opposed to single-ended designs, provides the advantage of reducing noise attributable to common-mode interferers. These interference signals might be caused by power supply fluctuation or substrate noise coupled from digital circuits that coexist on the IC. This leads to an overall lowering of the input noise level and decreases the level of detectable input signals, which by definition increases sensitivity. Also, well-matched balanced circuits reduce the effects of even-order distortion, most notably the dominant second-order effects inherent to MOS transistors, thereby effectively increasing the linearity of the active devices even at high frequencies [51].

Generally, replacing passive off-chip components with on-chip filters would seem to have an inherent negative impact on overall receiver dynamic range because of the necessity for active device incorporation into these filters. However, it has been demonstrated that incorporating an active Q -enhanced RF front-end LC bandpass filter in receiver designs can comparably perform with a typical front-end consisting of a passive filter and low-noise amplifier (LNA) [33]. On the other hand, this work also shows that the overall gain of the filter is a factor in determining the range of Q -enhancement that is beneficial to the overall performance. If the quality factor enhancement exceeds this gain-imposed maximum limit, the dynamic range for the overall receiver is comparatively worse.

For the RF bandpass filter that is the subject of this research work, maximization of linearity is one of the specific primary goals.

3.5.2 Tuning

Integrated passive components suffer from low absolute tolerances, age-induced component value drift, and variation in component values attributable to environmental variations. Consequently, continuous-time integrated filters require some post-fabrication adjustment to ensure repeatable response characteristics. Although designs that require trimming of components are still of some interest [52], the bulk of current work utilizes electronic, rather than physical, circuit component value adjustment. The topology of MOSFET-C and Gm-C filters intrinsically allow for tuning of the gm values of transistors or transconductors, which in turn allows for the adjustment of the corner frequency of integrator blocks used to derive the required filter functions. Alternately, filters that use on-chip inductors in LC tank circuits rely on a variable capacitance to tune the center frequency of the tank circuit. This variable capacitance can be achieved by integrated varactors [53], MOSFET switched-capacitor arrays (SCA's) [54], or by the utilization of the Miller Effect with fixed capacitors [55].

For practical application of integrated filters, automatic-tuning schemes must be employed. This automatic tuning is not only required for low-tolerance or drifting component value compensation as described previously, but also to enable filter topologies that can accommodate multi-mode or variable frequency operation. Automatic tuning circuits are required for frequency adjustment as well as a correction of the filter quality factor.

Two different general tuning methods of automatically adjusting the filter circuit, direct and indirect, have been developed [56]. Both of these methods normally utilize

auxiliary circuits that employ a phase-locked loop (PLL) to adjust frequency and an amplitude-lock loop (ALL) to adjust the quality factor.

In the direct tuning method, the filter that does the actual signal processing for the circuit or system is monitored and adjusted. A block diagram of a filter utilizing direct tuning is presented in Figure 3.21. In most direct tuning techniques, the filter is periodically removed from the circuit and tuned. One method involves the use of two equivalent filter circuits, but alternately switches the filters in and out of the signal path allowing periodic tuning of the off-line filter [57]. Another application of this tuning method has been achieved by monitoring the time domain step response of the circuit during the period that the filter is removed from the signal path [58]. The direct method has also been utilized where the primary filter structure is periodically switched out to act as the resonator in an oscillator circuit [59]. In this method, the oscillator is compared to a reference signal for tuning and switched back to filter mode after automatic adjustment. One other alternative direct tuning idea allows the filter to process the incoming signal while tuning is in progress [60].

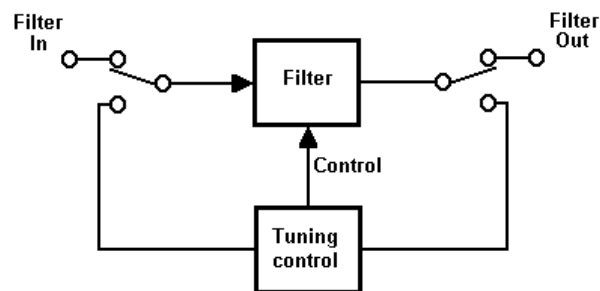


Figure 3.21. Block diagram of direct tuning scheme.

This method applies an orthogonal reference signal along with the signal of interest to the filter and separates the reference at the output, allowing the signal of interest to pass into the next stage of the system while the auxiliary tuning circuit monitors the reference signal output. This allows uninterrupted tuning of the filter, no replicate filter circuitry, and continuous operation and tuning.

In the indirect tuning method, a master filter is monitored and tuned while the slave filter, which does the actual signal processing, follows the tuning of the master [61]. A block diagram of a filter utilizing indirect tuning is presented in Figure 3.22. As shown in the figure, the master filter and tuning circuit are comprised of a phase-locked loop implemented with the phase/frequency detector, a loop filter, and a master oscillator. The master and slave filters in the indirect method are theoretically identical, allowing for simultaneous tuning. The frequency and Q of the master circuit are tuned via control signals provided by auxiliary circuits that monitor the response of the master output to an input reference signal. Alternately, the master filter can be employed as a resonator in a voltage-controlled oscillator (VCO) and this output monitored and tuned [62].

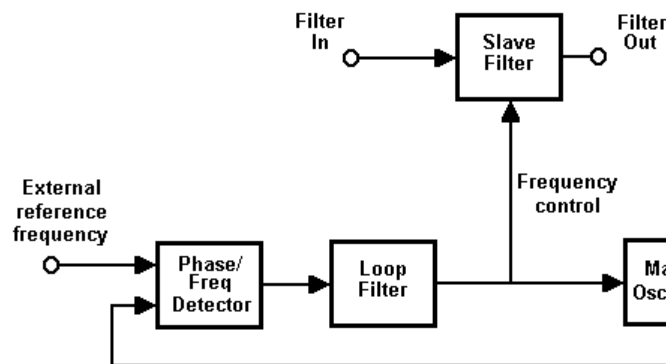


Figure 3.22. Block diagram of indirect tuning scheme.

The control signals that drive the master circuit are simultaneously applied to the slave, which does the actual processing of the incoming signal.

The transformer-coupled RF bandpass filter that is the subject of this research work does not include any type of tuning element and operates at a single fixed frequency. Tuning circuitry was omitted to facilitate isolated evaluation of the novel Q -enhancement technique that is the operationally unique portion of the circuit.

3.5.3 Power Consumption

One of the tradeoffs suffered when incorporating active on-chip filters to replace the passive off-chip counterparts is in the required power consumption. While this may not be an issue in fixed base station receivers, in battery powered wireless handsets and other portable or remote devices, circuit topologies that maximize the time of operation are a primary concern.

Previously discussed MOSFET-C and Gm-C filters require active devices in the form of transistors, transconductors, and/or op-amps to achieve integrator topologies that can be used to construct higher-order filters. This inclusion of active devices requires biasing, and consequently, a consumption of power that would not be required for a passive filter. Alternately, LC bandpass filters that utilize on-chip inductors and capacitors have naturally resonating tanks, but the intrinsically low quality factors of these resonators, particularly in the inductor, require active circuitry to reduce losses and enhance the overall quality factor to a level conducive to the required parameters of the system.

In addition, the requirement for automatic tuning of integrated filter circuits for any of the previously discussed active topologies requires auxiliary circuits, including

amplitude and phase locked loops, which warrant consideration when calculating the power budget of the design.

Another issue, as discussed previously, is the implementation of higher gain in the integrated filter to decrease input referred noise levels. This leads to the necessity of higher gm values in active amplifying circuits, which increases quiescent bias currents leading to additional power consumption.

Also, the point can be made that by eliminating the requirement for receivers to periodically drive characteristically low-impedance ($50\ \Omega$) passive devices, such as SAW IF filters, the power consumption can be reduced. However, the requirement for transconductors and tuning circuits for active integrated filters ultimately consumes a similar amount of energy for overall circuit operation, and these points must be considered as part of an overall RF system design.

To conclude, minimization of power consumption is not a primary goal of the transformer-coupled RF bandpass filter that is the subject of this research work, but this parameter is evaluated to allow for direct comparison of the operational characteristics of this circuit with other Q -enhanced integrated LC filter research.

3.6 Continuous Time Integrated Filters: Conclusion

This chapter has presented an overview of integrated filter components, topologies, and challenges with the intent of providing an outline of background information useful as a prelude to the subsequent detailed description of the RF bandpass filter that is the focus of this research. Based on the information presented in this chapter, it is reasonable to conclude that the Q -enhanced LC topology is the practical choice for implementing fully integrated RF frequency bandpass filters. Specifically, the high-dynamic range, reduced

active component count, and immunity to on-chip parasitic capacitance make LC filters particularly attractive for low voltage and low power active gigahertz range filters. With the acknowledgment of these conclusions, effort was undertaken to develop and implement a novel approach to achieving a unique method for realizing integrated RF and microwave bandpass filtering using an LC resonator topology with on-chip loss restoration or Q -enhancement.

CHAPTER 4

TRANSFORMER-COUPLED Q -ENHANCED RF BANDPASS FILTER

The circuit design investigated in this work introduces a loss-compensated second-order RF filter that is implemented in a standard digital 0.18 μm CMOS process. This filter utilizes an on-chip resonant tank comprised of the inductance of integrated transformer coils and capacitance that is a combination of circuit parasitics as well as specifically incorporated passive components. Loss compensation in the inherently low- Q LC resonator is achieved by a novel level-shifted Q -enhancement technique that allows for independent adjustment of the quality factor and overall gain of the circuit. This particular topology is also a prospective solution for utilizing low- Q integrated transformers as key components in Q -enhanced active single-to-differential converters. This prospective method could eliminate the need for a separate off-chip balun or facilitate a sharing of components for both filtering and single-to-differential conversion that would enhance the operational characteristics of a prospective integrated balun. With proper matching, this topology may allow for single-ended input signal, as from an antenna, to be directly amplified and filtered, then subsequently converted to a differential signal for low-noise processing in successive receiver blocks.

One specific technical approach that makes this work unique is the utilization of integrated transformers via on-chip magnetically coupled inductors to develop a novel circuit topology that facilitates filter Q -enhancement and signal amplification. Recent study has shown that on-chip transformers in standard CMOS can achieve coupling coefficients, k , of up to 0.9 [45] with self-resonant frequencies in the gigahertz frequency range. These previous findings, along with the aspiration to create novel integrated RF filter topologies, motivate the use of on-chip transformers and coupled inductors to create the novel Q -enhanced LC filter topology that is the focus of this research.

An operational objective of this research is to implement a transformer-coupled Q -enhanced LC filter in a prospective receiver front-end amplifier with the focus on maximizing the dynamic range through increased linearity. With this objective in mind, and in order to implement circuits with practical industrial application, wireless industry standards and associated specifications were evaluated to determine a feasible area in which to work. After review of several commercial specifications, the Bluetooth Wireless Personal Area Network (PAN), possessing a relaxed dynamic range and moderate quality factor requirements, was used to guide the filter design parameters. As detailed previously, in Section 2.3, filters employed for Bluetooth applications are required to operate at a center frequency of 2.44 GHz with a quality factor of approximately 30, a dynamic range of 50 dB, and input sensitivity or detectable power level of -70 dBm. Although the prospective applications of the filter examined in this research should not be limited, the more moderate specifications of Bluetooth were chosen as a target with the expectation of implementation in receiver configurations with more rigorous

specifications possible as this particular filter topology is validated and possibly refined for future work.

The following sections provide details regarding the transformer-coupled Q -enhanced LC filter including conceptual development, circuit operational characteristics, design methodology, physical layout considerations, simulation results, and experimental results. To conclude the chapter, the operational characteristics of this design are compared with RF filters of similar topology that have been the subject of other recent research activity.

4.1 Development of Concept

The following sections present information to provide insight into the conceptual development of the transformer-coupled Q -enhanced RF bandpass filter. This information begins with an evaluation of the Q -enhanced bandpass filter topology that is prevalent in other current and previous filter research, including the inherent functional constraints of this topology. Next, preliminary objectives for the current research that may provide functional improvement or the reduction of operational constraints for the typically implemented bandpass filter are outlined. Finally, based on the outlined objectives, the successive steps leading from initial conception to final design for the filter that is the subject of this research are presented.

4.1.1 Commonly Utilized Q -Enhanced LC Filter Topology

As discussed in Section 3.3.2, the Q -enhanced LC bandpass filter topology prevalent in recent research incorporates a single input stage and provides loss restoration using a transconductor that emulates negative resistance via positive feedback. A simplified circuit diagram showing a single-ended version of this topology is shown in Figure 4.1.

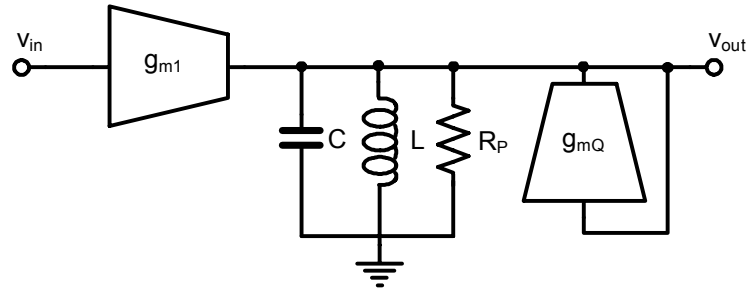


Figure 4.1. Typical single-ended Q -enhanced LC bandpass filter.

In Figure 4.1, the parallel tank resistor, R_P , represents the intrinsic inductor losses. This is based on the assumption that the quality factor of the tank inductor is much lower than that of the parallel capacitor. The transconductor connected to the output node of the circuit, g_{mQ} , serves as the tank loss restoration component and provides an effective tank negative resistance with an absolute value given by $1/g_{mQ}$.

In practice, the loss restoration transconductor is realized using a cross-coupled transistor pair, constraining this filter circuit to a differential topology. A simplified circuit diagram showing the commonly implemented differential version of the typical Q -enhanced bandpass filter is presented in Figure 4.2.

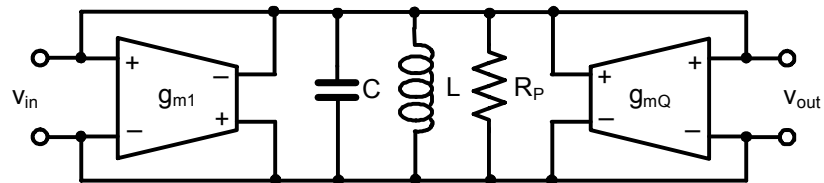


Figure 4.2. Typical differential Q -enhanced LC bandpass filter.

For reference, a more detailed schematic of this differential filter circuit is repeated from Section 3.3.2 and shown in Figure 4.3. The connections in Figure 4.3 highlight the second distinct constraint of the typically implemented Q -enhanced bandpass filter. This restriction is in the identical levels of bias voltage applied to both the gate and drain of loss-restoration transistors M_{Qa} and M_{Qb} when the cross-coupled transconductor is connected to the filter resonator. As shown in the figure, both gate and drain of the Q -enhancement transistors are connected to V_{DD} .

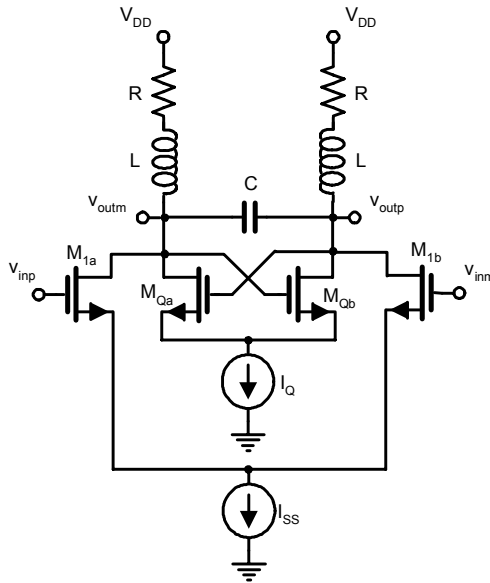


Figure 4.3. Differential Q -enhanced LC bandpass filter: Detailed schematic.

4.1.2 Design Objectives and Prospective Improvements

The discussed constraints of the typical Q -enhanced LC bandpass filter motivate the examination of filter topologies that might provide alternate circuits to achieve similar results. Four primary prospective modifications to the typical topology were identified for analysis in this research. The objectives of these design alternatives are outlined below:

- Implement an alternative to the cross-coupled transistor Q -enhancement technique that would allow variations in bias levels based on optimum circuit operation, *not* the constraints of the Q -enhancement technique itself.
- Harness the existing and normally unused magnetic energy from the inductor or inductors of an integrated LC filter resonant tank to facilitate prospective novel bandpass filtering and/or loss compensation techniques.
- Provide a filter input that might accommodate a single-ended source, prospectively moving the filter functional boundary out to a simple antenna connection.
- Create a circuit topology that would prospectively facilitate single-to-differential signal conversion while simultaneously providing amplification and frequency-selective operation.

The intent is to successively or concurrently examine and experiment with the objectives outlined above with the goal of developing an alternate Q -enhanced RF bandpass filter topology that captures and incorporates any or all of these operational modifications in a final functional design. Figure 4.4 shows a simplified graphical representation of the prospective modifications for the typical Q -enhanced filter presented in Figure 4.2.

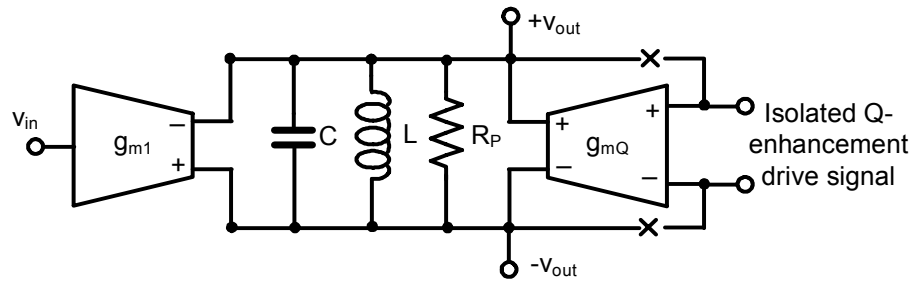


Figure 4.4. Prospective modifications to typical Q -enhanced LC filter.

4.1.3 Design Progression

The circuits presented in Figure 4.5 illustrate the conceptual development of the transformer-coupled Q -enhanced RF bandpass filter circuit.

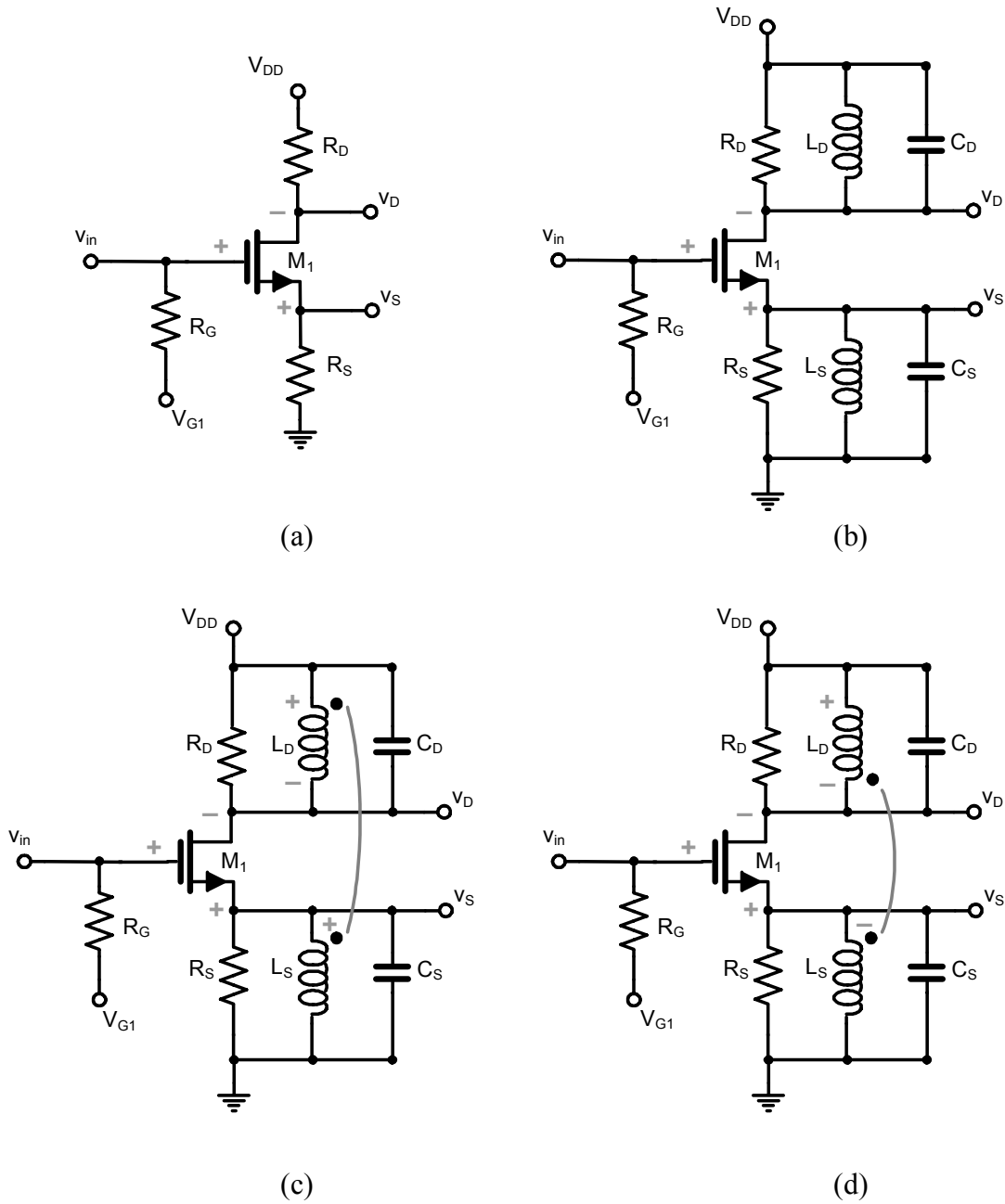


Figure 4.5. Development of transformer-coupled Q -enhanced RF bandpass filter.

First, in Figure 4.5(a), the simplest form of a single-to-differential circuit is shown. This topology utilizes a single NMOS amplifier connected as a source follower, but with output signals taken from identical loads connected to the source and drain. Note that this circuit exhibits negative feedback from source to gate via source degeneration, which is inherent to this topology. Next, to implement frequency selectivity, resonators are incorporated as loads for the source and drain. This topology is shown in Figure 4.5(b) with the losses in the identical source and drain coils, L_S and L_D , being represented by parallel resistors R_S and R_D . Although bandpass filtering is established with this topology, the circuit still provides negative feedback via source degeneration, particularly at the resonance frequency. Now, in Figure 4.5(c), the idea of utilizing magnetic coupling between the source and drain inductors to augment the operational characteristics of the circuit is examined. In Figure 4.5(c), it can be seen that the polarity of the coupling in the transformer, which consists of L_S and L_D , produces an increase in the source degeneration, as indicated by the feedback polarities notated by the '+' and '-' symbols. In Figure 4.5(d), the transformer coupling has been reversed to investigate the possibility of introducing positive feedback and prospective cancellation of losses in the resonators. Although the feedback from drain to source does create an overall regenerative effect, this is cancelled by the equal and opposite source degeneration, as transistor M_I is providing identical drive to both the source and drain coils. It is now clear that in order to provide independent adjustment of the transformer-coupled positive feedback, an additional active device is required. This component is implemented with a single NMOS transistor that is connected in a circuit configuration that provides the required independently adjustable Q -enhancement while also utilizing variable voltages at several

nodes in the circuit to allow for bias level shifting. A simplified schematic of this final design is presented in Figure 4.6. In the figure, the signal polarities attributable to M_I are shown with the lighter '+' and '-' symbols while the signal polarities attributable to M_Q are shown circled. Note that the loop provided by M_Q provides the positive feedback necessary for circuit loss restoration.

Also, it is significant that the source and drain capacitors in Figure 4.6, C_S and C_D , are connected to separate power supplies, permitting bias level adjustment flexibility while ideally maintaining a *signal* ground path through these bias supply nodes. As a result of the inherent symmetry provided by these connections, these two capacitors can be realized with a single component, which is $\frac{1}{4}$ the value (and physical size) of the combined capacitance value for C_S and C_D . Figure 4.7 presents two small signal equivalent circuits illustrating this concept.

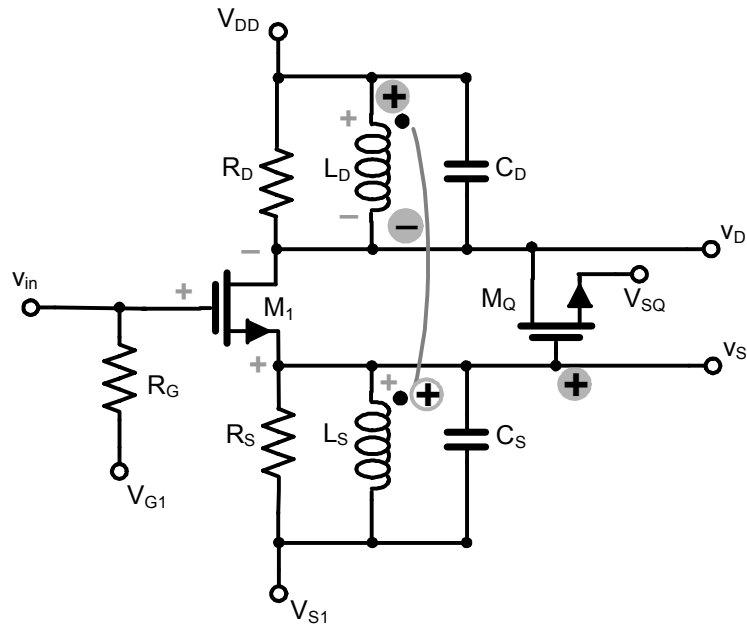


Figure 4.6. Final topology of transformer-coupled Q -enhanced filter.

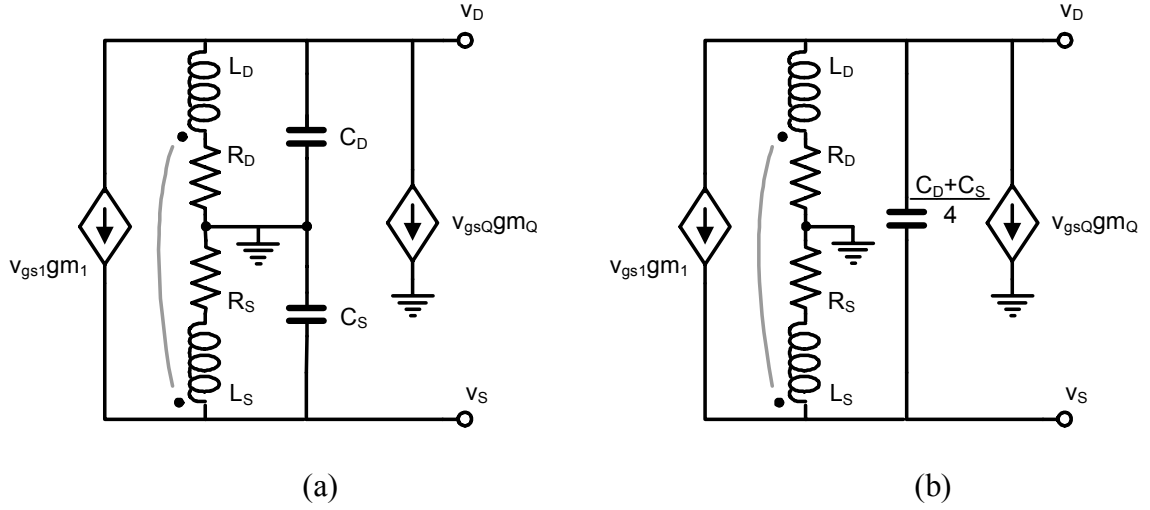


Figure 4.7. Small-signal equivalent circuit of transformer-coupled RF filter.

The capacitor connections shown in Figure 4.7(a), combined with the pseudo push-pull behavior of the transformer-coupled circuit, make this topology electrically equivalent to the single capacitor resonator circuit shown in Figure 4.7(b).

The analysis presented in this section has shown that the concurrent contemplation and evaluation of prospective single-ended operation, possible single-to-differential conversion, elimination of the cross-coupled negative resistor topology (and the associated fixed bias levels), and utilization of integrated transformers has culminated in a distinct filter circuit topology. The resultant transformer-coupled Q -enhanced RF bandpass filter circuit succeeds in capturing and incorporating all of the characteristics outlined as target modifications to the typically implemented Q -enhanced LC bandpass filter. Subsequent sections of this chapter provide an operational description of this topology, detailed circuit functional analysis, and results of simulated and experimental test and evaluation.

4.2 Circuit Operational Description

Figure 4.8 shows a simplified schematic for the final version of the transformer-coupled Q -enhanced RF bandpass filter incorporating all of the outlined operational characteristics and circuit connections described in Section 4.1. However, the circuit shown in Figure 4.8 utilizes a single output connected to the drain of M_I . The single output is utilized for the initial evaluation of this circuit to facilitate more simplified connection of measurement instrumentation. Also, an inductor, L_{degen} , has been connected to the source of M_Q to provide additional linearization for that device, and all inductor losses are shown with series resistors. This final design topology provides moderate input amplification along with frequency selectivity and incorporates a novel technique for magnetically coupled loss restoration. Note that the schematic in the figure depicts a signal generator as the circuit input source. However, the circuit input could generally be connected to the output of other preceding off-chip or integrated components or circuits.

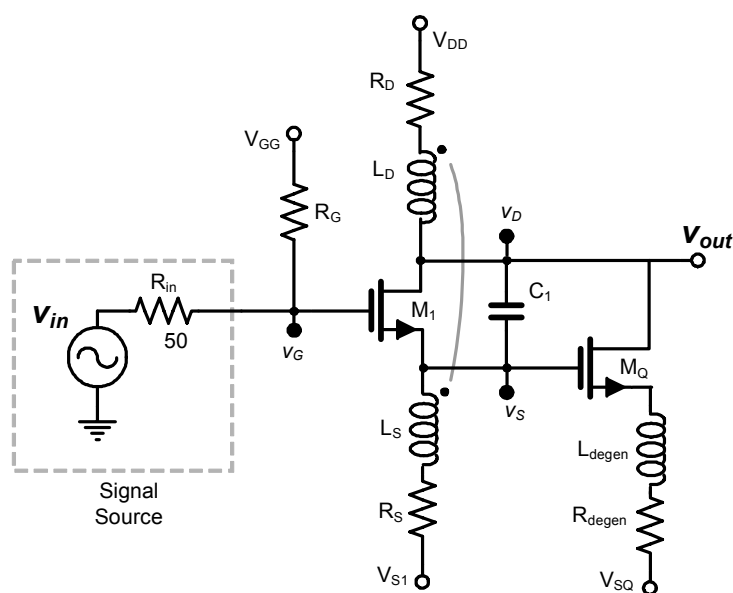


Figure 4.8. Transformer-coupled Q -enhanced RF bandpass filter.

Ideally, the filter design would be refined to connect to an off-chip antenna via a simple matching network. Additionally, the signal output is shown at the drain of M_I but a phase-inverted version of the signal is available at the source of M_I as well. Also, it is expected that the output signal from this circuit would subsequently drive the high-impedance following stage of an integrated receiver, such as the image-reject filter or mixer described in Section 2.1.1.

The polarity of the transformer, comprised of coupled inductors L_D and L_S , creates a source degenerative effect in combination with input transistor M_I , but enables Q -enhancement when combined with the positive feedback loop through M_Q . Resistors R_D and R_S represent losses in the inductors. Control voltage V_{SI} sets the gate level of M_Q and the source voltage of M_I . Tuning voltage V_{SQ} can then be used to adjust the transconductance of the active loss-restoring device, M_Q , for the desired enhanced quality factor. Bias voltage V_{GG} can also be adjusted to change the overall circuit gain. Also, tradeoffs in P_{1dB} and input referred noise are adjustable by changing the overall gain with V_{SI} or V_{GG} and readjusting the quality factor with V_{SQ} .

The transfer function describing the single-ended response of the circuit from gate to drain is given by

$$T(s, k=1) = \frac{v_d}{v_g} = \frac{\frac{-2g_{m1}}{C} \left(s + \frac{R}{L} \right)}{s^2 + \left[\frac{R}{L} + \frac{(2g_{m1} - g_{mq})}{C} \right] s + \frac{1}{LC} (1 + 2g_{m1}R - g_{mq}R)}. \quad (26)$$

This transfer function was derived from a rigorous analysis of the multiple feed-forward and feedback loops in the circuit, the details of which are presented in Section

4.3.1. The derivation of this transfer function is also based on the assumption the inductors making up the transformer are symmetric, i.e. $L_D = L_S = L$, and the series resistance for each of these inductors is also equal and represented by R . These assumptions are based on the symmetric-square layout of the transformer utilized for the design and evaluated previously. Also under the same assumption of symmetry, the values for R and C in (26) are given by the following equations:

$$R = R_D \parallel \frac{R_D}{k^{1/2}} = R_S \parallel \frac{R_S}{k^{1/2}} \quad (27)$$

$$C = 2C_1(1 + k) \quad (28)$$

Note that an assumed transformer coupling coefficient, k , of unity is used to derive Equation (26). The analysis presented in Section 4.3.1 indicates that less than ideal values for k result in the appearance of distant third-order and higher poles caused by the feedback from v_d to v_s through the transformer along with any inherent circuit asymmetries. The ideal case of $k = 1$ is used here in order to keep the transfer function presented in Equation (26) in the simplest second-order form, facilitating clearer operational insight. This second-order bandpass form allows an intuitive understanding of this circuit and a direct comparison to the cross-coupled implementation presented previously in Section 3.3.2. Also, referring to Equation (26), notice that an increasing value of g_{mQ} improves the overall quality factor, similar to Equation (18) or Equation (19) for the previously presented cross-coupled Q -enhanced circuit.

4.3 Detailed Circuit Functional Analysis

This section presents an examination of the functional characteristics for the Q -enhanced transformer-coupled RF filter. This includes a derivation of the filter transfer function, which allows for an understanding of the circuit frequency response and quality factor characteristics. Also, an analysis of the expected dynamic range improvement for the design is also performed and discussed. Additionally, the effects of non-unity transformer coupling on circuit operation are addressed. Finally, the Q -enhancement tuning response will be examined. This will include an evaluation of achievable quality factor adjustment along with the characteristic sensitivity of circuit Q -enhancement with respect to the adjustment of the loss restoring circuit active devices.

4.3.1 Frequency Response

The transfer function of the transformer-coupled RF bandpass filter is extracted to gain insight into the circuit operational characteristics. This facilitates an understanding of the effects of each circuit component on filter response and quality factor as well as allowing direct comparison with standard second-order bandpass filter characteristics.

Given the topology of the non-standard transformer-feedback Q -enhancement, several feed-forward and feedback paths exist. This intrinsically multi-path topology requires a circuit model that captures characteristics of all the significant passive and active components and combines the effects of each into one simplified transfer function. In order to derive the characteristic equations for the transformer-coupled RF filter, a simplified small-signal model of the circuit is utilized. In the following paragraphs, the components of the circuit model are presented followed by the integration of these components into the overall circuit model. The model is then used to derive the formulas

for the multiple signal paths in the circuit and these formulas are combined in a system-level model to produce the overall filter transfer function.

The basic small signal model for a MOS transistor is shown in Figure 4.9. For simplification, this model neglects the channel-length modulation effect and omits the gate-to-source and gate-to-drain parasitic capacitors.

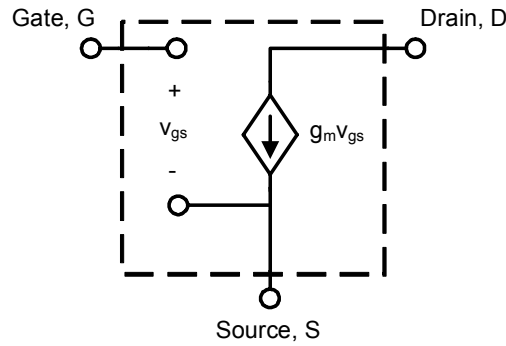


Figure 4.9. Small signal model for MOS transistor.

In order to facilitate a simplified *overall* circuit model, and owing to the comparative accuracy of results from previous integrated transformer studies [47,63], an h -parameter transformer model was used to capture the functional characteristics of the coupled inductors in the RF filter. A block diagram of an h -parameter transformer model is presented in Figure 4.10.

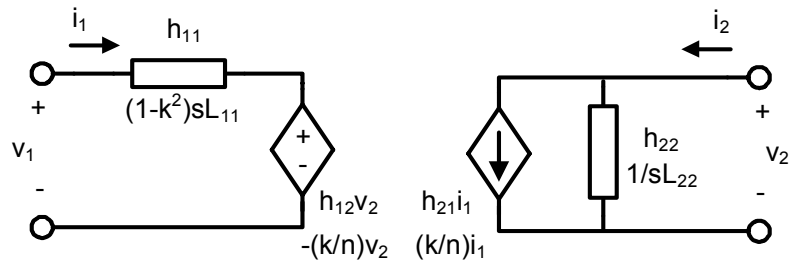


Figure 4.10. Transformer h -parameter model.

The values for the h -parameter components shown in Figure 4.10 are presented in the following equations:

$$h_{11} = (1 - k^2)sL_{11} \quad (29)$$

$$h_{12} = \frac{k}{n} \quad (30)$$

$$h_{21} = \frac{-k}{n} \quad (31)$$

$$h_{22} = \frac{1}{sL_{22}} \quad (32)$$

For Equation (29), L_{11} is the primary coil of the modeled transformer and is representative of the bandpass filter source inductor, L_S , while L_{22} , in Equation (32), is the secondary coil of the modeled transformer and is representative of the filter drain inductor, L_D . These values are assumed equal based on the symmetrical design of the transformer utilized in the filter design. The value for n in Equation (30) and Equation (31) is the transformer turns ratio and is equal to one, also as a result of transformer symmetry. Additionally, in Equation (30) and Equation (31), the value for the transformer coupling coefficient, k , is assumed to be unity to simplify the mathematical derivation process. (Further details pertaining to the non-ideal effects of the coupling coefficient are presented in a following section). A small-signal model of the overall circuit that includes the transformer and active device model components is presented in Figure 4.11.

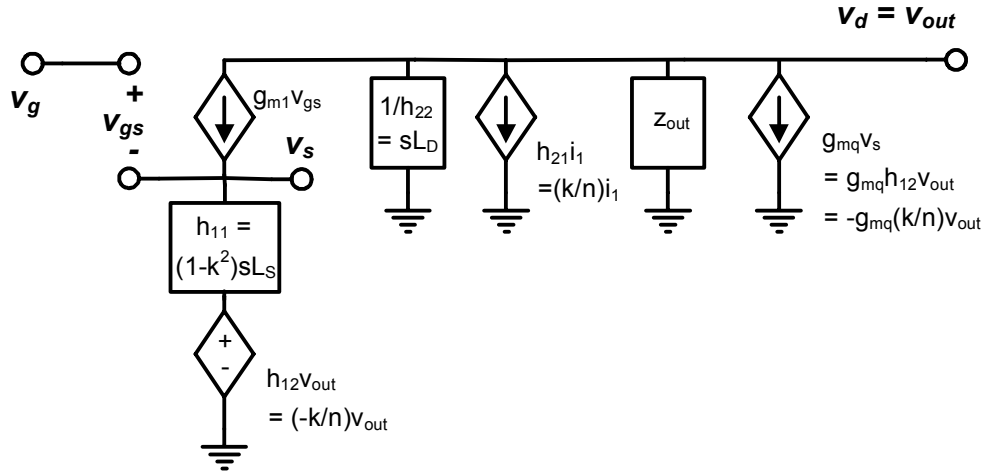


Figure 4.11. Transformer-coupled filter: Small-signal model.

Figure 4.11 illustrates the topology of the circuit model that provided the most accurate transfer function of several configurations that were evaluated.

In Figure 4.12, a simplified circuit diagram is presented that shows the feedback and feed-forward paths of the transformer-coupled filter.

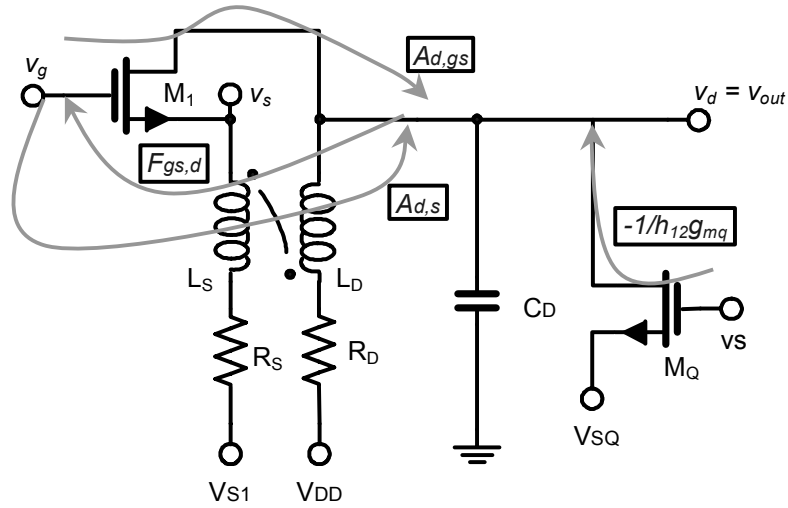


Figure 4.12. Transformer-coupled filter: Feed-forward and feedback signal paths.

In Figure 4.12, the ‘ A ’ designators refer to feed-forward signals while the ‘ F ’ designator denotes feedback. The subscripts for the designators refer to the signal output and input. For example, $A_{d,gs}$ refers to the signal at the drain resulting from stimulus at the transistor gate/source. However, the signal path from the loss restoration component, M_Q , does not adhere to this signal path reference nomenclature because this device transfers signals ‘across’ the resonant tank of the circuit, between M_I source and drain. After the evaluation of various circuit configurations, it was determined that the most accurate representation for the contribution of M_Q would be as an addition to the load at the output node, v_d . Also, capacitance C_D takes on the value of twice the drain to source capacitor as a result of circuit symmetry (refer to Section 4.1.3) and the gate-to-source and gate-to-drain capacitance of M_I are omitted because of their comparatively low values and to facilitate a concise analysis of the primary filter operational characteristics.

Next, a system level model is assembled to allow for a mathematical combination of the various signal path transfer functions. This model is presented in Figure 4.13.

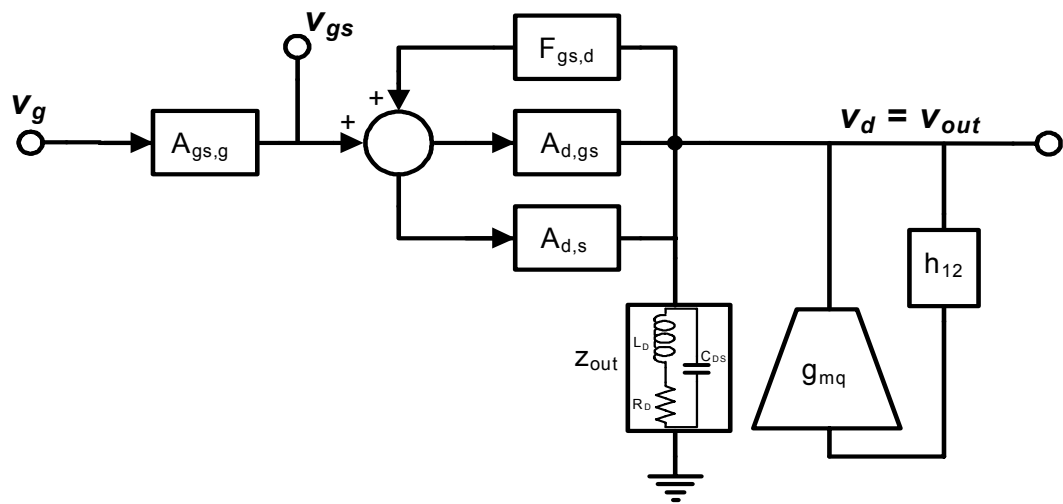


Figure 4.13. Transformer-coupled filter: System-level model.

In Figure 4.13, the transfer function block $A_{gs,g}$ refers to the effective signal across the gate to source junction of M_I as a function of the applied gate to ground voltage, but is not shown in the small-signal model.

Now, the equations describing each of the transfer function blocks shown in Figure 4.13 and based on the small-signal models and signal paths presented in Figure 4.11 and Figure 4.12 can be extracted. These equations, along with the total output impedance, Z_T , which consists of the resonant tank in parallel with $1/h_{12}g_{mq}$, are presented in the following equations:

$$A_{gs,g} = \frac{v_{gs}}{v_g} = \frac{1}{1 + g_{m1}h_{11}} \quad (33)$$

$$A_{d,s} = \frac{v_{out}}{v_s} = -h_{21}g_{m1}(sL_{22} \parallel Z_{out}) = -h_{21}g_{m1}Z_T \quad (34)$$

$$A_{d,gs} = \frac{v_{out}}{v_{gs}} = -g_{m1}(sL_{22} \parallel Z_{out}) = -g_{m1}Z_T \quad (35)$$

$$F_{gs,d} = \frac{v_{gs}}{v_{out}} = \frac{-h_{22}}{1 + g_{m1}h_{11}} \quad (36)$$

$$Z_T = -(1/g_{mq}h_{12}) \parallel Z_{out} \quad (37)$$

Using system analysis reduction techniques, the *overall* transfer function of the system, $T(s)$, can be written in terms of the *individual* signal transfer function blocks as

$$T(s)_{Qenh} = \frac{v_{out}}{v_g} = \frac{A_{gs,g}(A_{d,gs} + A_{d,s})}{1 - F_{gs,d}(A_{d,gs} + A_{d,s})} Z_T. \quad (38)$$

Finally, utilizing the formulas for the individual system blocks and substituting the component reference designators for the h -parameter values produces the overall transfer function of the circuit. Assuming the coupling coefficient, k , is equal to unity, the transfer function, after term consolidation and reduction, is given by

$$T(s, k=1)_{Qenh} = \frac{v_d}{v_g} = \frac{\frac{-2g_{m1}}{C} \left(s + \frac{R}{L} \right)}{s^2 + \left[\frac{R}{L} + \frac{(2g_{m1} - g_{mq})}{C} \right] s + \frac{1}{LC} (1 + 2g_{m1}R - g_{mq}R)}. \quad (39)$$

As mentioned previously, the assumption is made that $L_D = L_S = L$, and the series resistance for each of these inductors is equal and represented by R . Also the values for R and C in Equation (39) are given by the following equations:

$$R = R_D \parallel \frac{R_D}{k^{1/2}} \quad (40)$$

$$C = 2C_1(1+k) \quad (41)$$

Next, to extract the center frequency from Equation (39), recall the standard form of the transfer function for a second-order bandpass filter:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A \frac{\omega_o}{Q} s}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2}. \quad (42)$$

Now, comparing Equation (39) to Equation (42), the value for filter center frequency is

$$\omega_o = \frac{\sqrt{(1 + 2g_{m1}R - g_{mq}R)}}{\sqrt{LC}}. \quad (43)$$

It is clear that the numerator term in Equation (43) is close to one, given that the comparative values for $g_m R$ and $g_{mq} R$ are very small, so the center frequency is primarily set by the values for L and C , similar to the cross-coupled filter. For reference, the value of the center frequency for the cross-coupled filter presented in Section 3.3.2 and described by Equation (18) is given as

$$\omega_o = \frac{\sqrt{(1 - g_{mq} R)}}{\sqrt{LC}}. \quad (44)$$

Observe that Equation (43) and Equation (44) differ only in the g_{ml} term included in Equation (43).

To investigate the parameters affecting Q -enhancement, assuming ω_o is strictly a function of L and C , and again comparing Equation (39) to Equation (42), the value for the filter quality factor is given by

$$Q = \frac{1/\sqrt{LC}}{\frac{R}{L} + \frac{(2g_{ml} - g_{mq})}{C}} \quad (45)$$

where Q is the enhanced quality factor of the circuit. The value for Q described by Equation (45) does not facilitate a particularly clear understanding of the quality factor enhancement and the effect of specific related components. However, if Equation (45) is rewritten in terms of the intrinsic, non-enhanced quality factor, Q_o , additional insight can be gained. After substitution of terms and algebraic reduction, the enhanced quality factor of the circuit can be described by the following equation:

$$Q = \frac{Q_o}{1 + \frac{L}{RC}(2g_{m1} - g_{mq})}. \quad (46)$$

Note that as g_{mq} exceeds $2g_{m1}$, the denominator of Equation (46) decreases to below one and the overall circuit quality factor is enhanced. The reduction of Equation (45) to Equation (46) is based on the assumptions and relationships shown in the following equations:

$$\omega_o \cong \frac{1}{\sqrt{LC}} \quad (47)$$

$$R = \frac{1}{\omega_o C Q_o} = \frac{\omega_o L}{Q_o} = \frac{\sqrt{L/C}}{Q_o} \quad (48)$$

$$L(Q_o) = \frac{Q_o R}{\omega_o} \quad (49)$$

$$C(Q_o) = \frac{1}{\omega_o Q_o R} \quad (50)$$

Observe that the mathematical description of the filter quality factor for the transformer-coupled filter given in Equation (45) and Equation (46) is similar to the quality factor that would be extracted from Equation (18) for the cross-coupled filter. Similar to the formulas for center frequency, a comparison of the equations for the quality factor of the two filter implementations differ only by the inclusion of the g_{m1} term, which is unique to the transformer-coupled bandpass filter Q description.

Next, quality factor enhancement is examined as the coefficient for s in the denominator of Equation (39) approaches zero, i.e Q approaches infinity. This exercise provides calculation of the g_{mq} values required for maximum Q -enhancement relative to the integrated passive components of the circuit resonant tank. This facilitates intuitive understanding of the fundamental limits of the transformer-coupled filter design while allowing direct comparison to the cross-coupled filter. The following formula for g_{mq} under these limits is given as

$$g_{mq} = \frac{RC}{L} + 2g_{m1} \Rightarrow \lim_{\frac{\omega}{Q} \rightarrow 0} \Rightarrow \lim_{Q \rightarrow \infty} . \quad (51)$$

For comparison, the formula for g_{mq} under the same limits imposed for the cross-coupled filter presented in Section 3.3.2 is given as

$$g_{mq} = \frac{RC}{L} \Rightarrow \lim_{\frac{\omega}{Q} \rightarrow 0} \Rightarrow \lim_{Q \rightarrow \infty} . \quad (52)$$

The g_{m1} term that is included in Equation (51) is a result of the negative feedback inherent to the transformer-coupled circuit caused by the source degeneration of M_1 . This source degeneration is provided by the signal developed across source inductor, L_S . After the magnitude of g_{mq} surpasses the value of $2g_{m1}$ in Equation (51), the Q -adjustment properties are identical to the cross-coupled filter implementation detailed in Equation (52). This requirement for increased g_{mq} in the transformer-coupled filter, and the subsequent required power increase, although small, is one of the tradeoffs of this design.

To conclude and validate the derivations of the characteristic equations for the transformer-coupled Q -enhanced filter, the transfer function presented in Equation (39) was compared to circuit simulations using ideal transistor models, varying values of transformer coupling coefficients, and ideal S-parameter functional blocks. These simulations provided qualitative operational verification of the mathematically produced transfer functions.

Finally, it is important to note that the preceding analysis presents a relatively coarse examination of the circuit. A more rigorous and exacting analysis would need to include the gate-to-source and gate-to-drain capacitors of all circuit transistors along with any other possible parasitic components. However, for the purpose of this work, the goal is to arrive at a fundamental mathematical description of the primary circuit functional characteristics in order to provide an intuitive understanding of this unique filter topology.

4.3.2 Dynamic Range Improvement

The topology of the transformer-coupled Q -enhanced filter allows the gate bias level of the negative resistance generator, M_Q , to be set independent of the drain, a significant difference when compared to the cross-coupled circuit shown previously in Figure 3.8. This flexibility in bias adjustment allows M_Q to be set at a quiescent point that facilitates the maximum positive and negative signal swings and increases circuit dynamic range through increased input compression point or P_{1dB} . For reference, Figure 4.14 shows simplified circuit diagrams of the transformer-coupled filter and cross-coupled filter with the loss restoration components for each of the filter topologies designated.

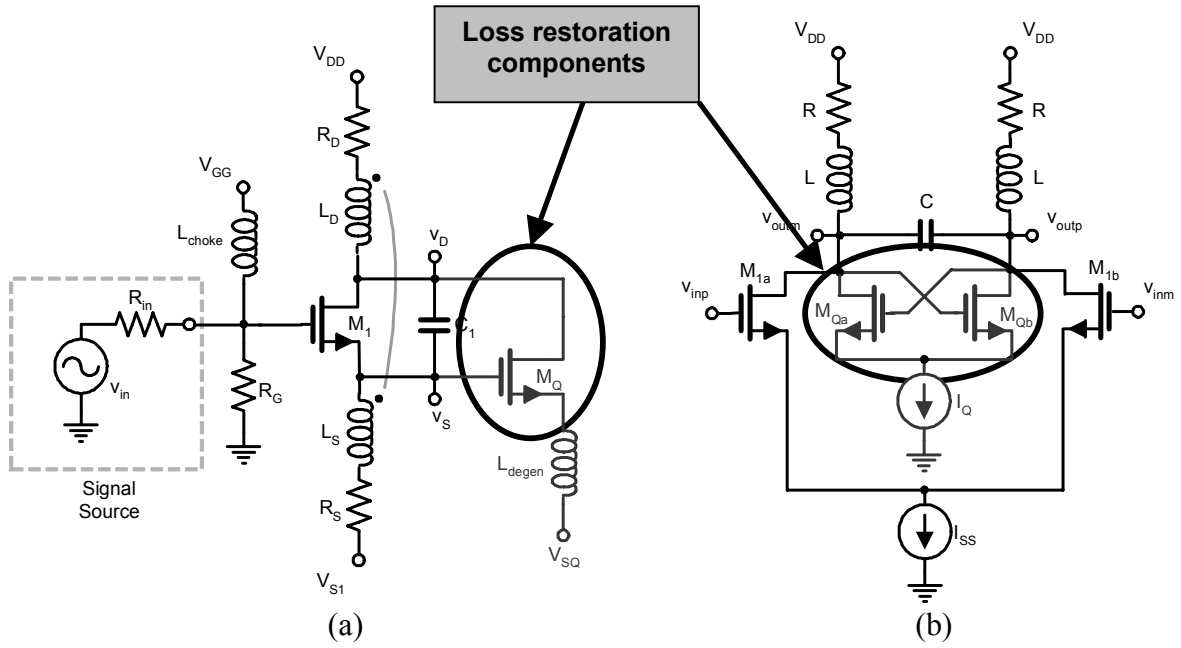


Figure 4.14. Bandpass filter loss restoration. (a) Transformer-coupled. (b) Cross-coupled.

A clear distinction between the two circuits shown in Figure 4.14 exists in the applied bias voltages: The drain and gate of the loss restoration transistor, M_Q , in Figure 4.14(a) have different bias sources, and subsequent independent adjustment, while the drain and gate of the cross-coupled enhancement transistors, M_{Qa} and M_{Qb} , in Figure 4.14(b) are connected to the same bias source, and inherently constrained to the same quiescent point.

To graphically illustrate the difference in allowable signal swings, Figure 4.15 presents simplified circuit diagrams of the cross-coupled filter and transformer-coupled filter with waveforms that show transient signals superimposed on the associated bias levels for each of the circuits.

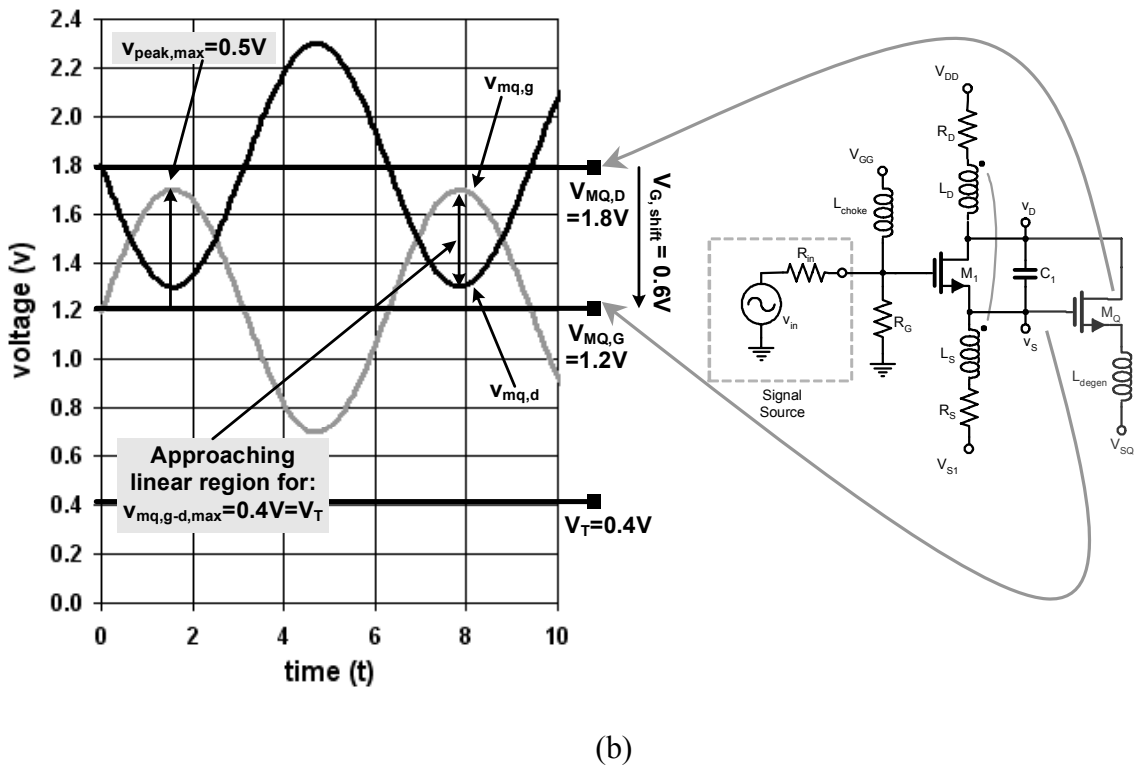
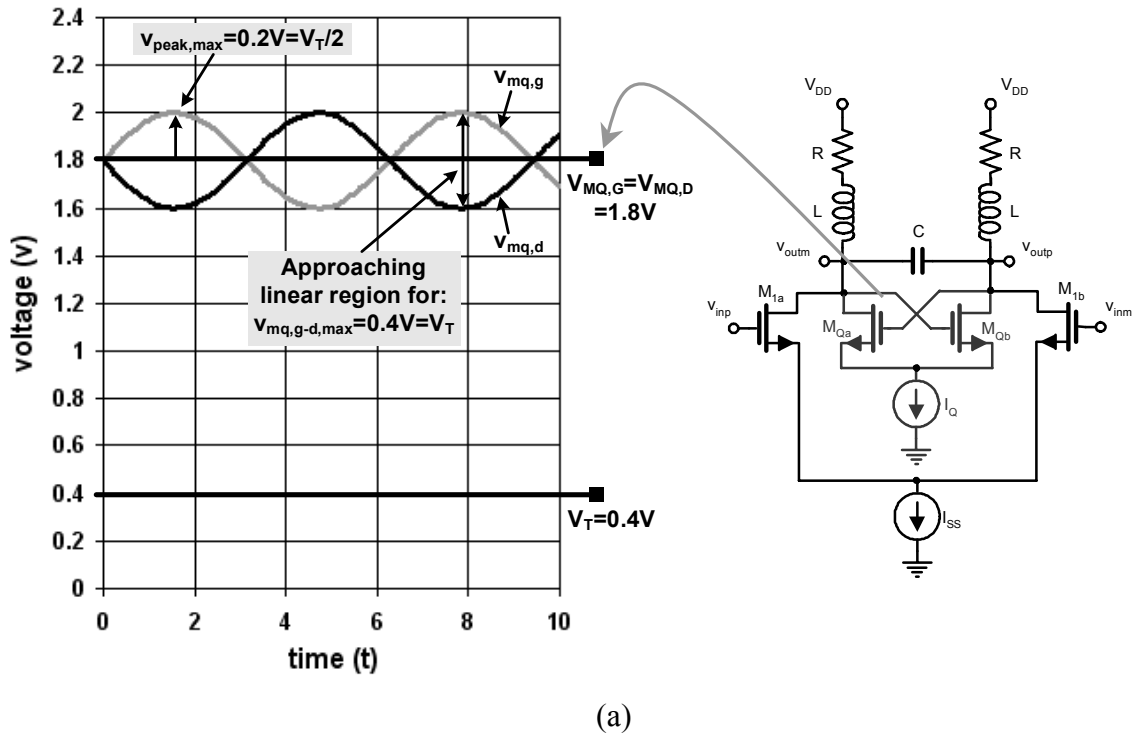


Figure 4.15. Transient signal and bias level plots for Q -enhancement topologies. (a) Cross-coupled. (b) Transformer-coupled.

For the plots in Figure 4.15, the lighter signal traces represent gate voltage of the associated Q -enhancement transistor(s) while the darker traces represent drain voltage.

For each of the circuits, a transistor threshold voltage, V_T , of 0.4 V was assumed to allow direct comparison and facilitate quantitative comparison. Also, both circuits are constrained to a 1.8 V_{DC} level for the drain bias. Now, based on the knowledge that the MOS transistor terminal voltages are constrained by $v_D \geq (v_G - V_T)$ for these active devices to operate in saturation mode, analysis of the potential increased signal swing for the transformer-coupled filter circuit can be undertaken. Note that v_D represents the bias voltage plus signal voltage at the drain of the Q -enhancement transistors in either circuit, while v_G is the gate bias voltage plus signal voltage.

For the cross-coupled filter in Figure 4.15(a), the drain and gate of the Q -enhancement devices, M_{Qa} and M_{Qb} , have both drain and gate bias levels, $V_{MQ,D}$ and $V_{MQ,G}$, set at 1.8 V_{DC} in accordance with normal connections for the cross-coupled configuration. As illustrated in the figure, this constrains the maximum peak signal swing to $V_T/2$, or 0.2 volts in this example, at the edge of transition from saturation mode to linear mode in M_{Qa} or M_{Qb} . Alternately, the transformer-coupled filter in Figure 4.15(b) shifts the gate voltage of the Q -enhancement transistor, M_Q , down to 1.2 V_{DC} via the independent gate bias. This facilitates a greater signal swing while maintaining operation of M_Q in saturation mode. It can be shown that the maximum allowable signal voltage swing increase is the amount of the shift divided by two, or $V_{G,shift}/2$. This implies that a gate bias decrease of V_T volts from the level of V_{DD} increases the allowable saturation mode signal swing from $V_T/2$ to $(V_T/2 + V_T/2)$, for a maximum signal swing increase of 6 dB. However, note that the shifted gate voltage is constrained to a mid-point between

V_{DD} and V_T to ensure the negative going peak of the signal does not dip below V_T and cause the transistor to enter the sub-threshold or weak inversion region.

Additionally, as transistor threshold voltage V_T decreases, the maximum swing of the *cross-coupled* circuit is detrimentally affected. However, a lower value of V_T is beneficial and facilitates even greater allowable values for $V_{G,shift}$, and produces a subsequent increase in the allowable tank voltage swing for the transformer-coupled Q -enhanced filter implementation. The increase in allowable gain as a function of $V_{G,shift}$ is generally described by

$$Gain_{increase,dB} = 20 \log \left(\frac{V_T / 2 + V_{G,shift} / 2}{V_T / 2} \right) = \left(1 + \frac{V_{G,shift}}{V_T} \right). \quad (53)$$

Utilizing Equation (53), it can be shown that for the circuit bias levels shown in Figure 4.15(b), a potential allowable signal increase and subsequent dynamic range improvement of ~ 8 dB is realized with the gate voltage shift of 0.6 V that is shown.

4.3.3 Effects of Non-Unity Transformer Coupling Coefficient

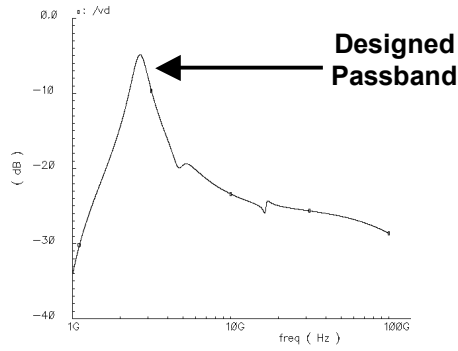
If a non-unity coupling coefficient is utilized for the analysis presented in Section 4.3.1, then the primary effect on the circuit transfer function is the appearance of s^3 and higher order terms in the denominator of Equation (39), implying the introduction of additional poles in the filter response. After simplification, these higher order ‘ s ’ terms include a coefficient of $(1-k^2)$, which implies that these terms, and subsequent response characteristic effects, vanish in the case of unity transformer coupling coefficient, $k = 1$.

Additionally, the simplified model becomes less accurate because of the symmetry loss caused by the uncoupled resonators at the drain and source nodes of M_I .

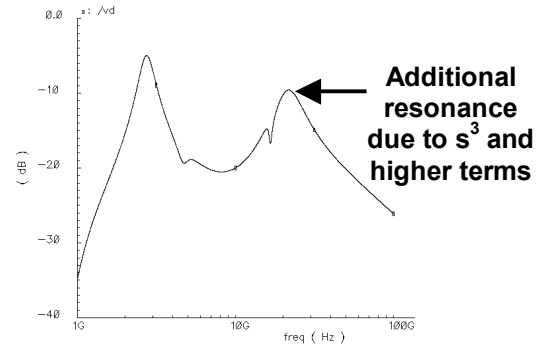
In the event that ideal transformer coupling is *not* achieved, this decoupling of resonators creates a significant increase in circuit operational complexity, resulting in the appearance of distant pole pairs and the creation of additional response peaks at outlying resonance frequencies. Non-unity coupling also has an effect on other circuit characteristics, such as filter center frequency and circuit Q -enhancement, but the impact of these effects is mostly negligible.

The exact transfer function, including non-unity k and the resultant decoupled resonators, becomes somewhat complex and obscures intuitive understanding of the designed filter circuit response. However, linear ac simulations of the circuit *do* provide some insight into the filter behavior. These types of simulations were performed for non-ideal transformer coupling and to provide a qualitative understanding of the circuit response for changing non-unity k values with all other parameters held constant. Several plots from these simulations that graphically demonstrate the effects of coupling coefficient values ranging from zero to one are presented in Figure 4.16.

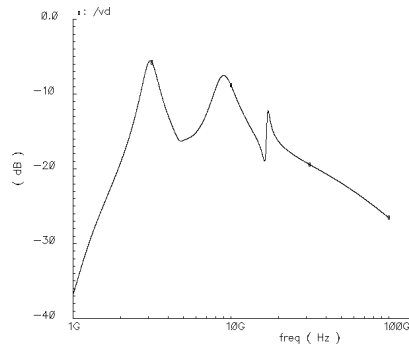
Referring to Figure 4.16(b), the appearance of an additional passband is evident at approximately 30 GHz for a value of $k = 0.9$ and this response peak moves towards the designed passband as the coupling coefficient continues to decrease. Also, the presence of a zero, or notch, at just below 20 GHz is evident in Figure 4.16(c) and Figure 4.16(d). This notch is primarily a result of low-impedance paths created by parasitic capacitors and inductive components used to model non-ideal external power supply connections.



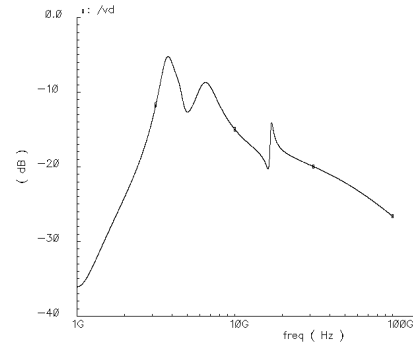
(a)



(b)



(c)



(d)

Figure 4.16. Transformer coupling effects. (a) $k = 1$. (b) $k = 0.9$. (c) $k = 0.5$. (d) $k = 0$.

To conclude, the effect of the non-ideal coupling coefficient in itself might warrant more investigation for future work, but notice that the designed passband in the response curves of Figure 4.16 is not significantly affected by this phenomenon. With these facts established from the simulation results, and in order to keep the information regarding the transformer-coupled RF bandpass filter concise and focused on the designed filter, further investigative work was not performed and is not presented regarding these effects attributable to the non-unity coupling coefficient.

4.3.4 *Q*-Enhancement: Tuning and Sensitivity

For the RF filter analyzed in this work, the quality factor enhancement of the circuit resonant tank is dependent on positive feedback provided by transistor M_Q via the coils of the circuit transformer. More generally, and as discussed in Section 3.3.1, the loss in a resonant tank can be transformed from a series resistor to a parallel resistor for the simplified model of a lossy inductor. Using this parallel resistor loss approximation, a mathematical analysis is undertaken to provide an intuitive understanding regarding the sensitivity (S) of a resonant tank circuit to the introduction and adjustment of an active, loss-restoring device.

Recall from Section 3.3.1 the circuit showing the transformation to a simplified parallel resonant tank. This circuit is repeated for reference in Figure 4.17. In the third circuit from the left in the figure, the component labeled ‘- R ’ is the loss restoration device. Now, assuming that this component is realized with an active device, referenced as g_{mq} , the total effective parallel tank resistance, R_{eff} , is given by

$$R_{eff} = R_p \parallel \frac{1}{-g_{mq}} = \frac{R_p \times \frac{-1}{g_{mq}}}{R_p - g_{mq}} = \frac{R_p}{1 - R_p g_{mq}}. \quad (54)$$

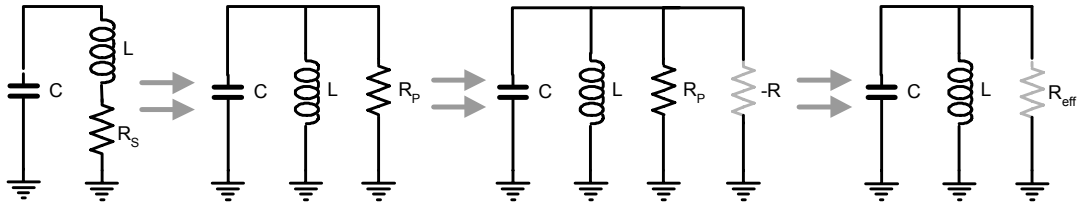


Figure 4.17. *Q*-enhanced LC tank circuit.

It can be determined from Equation (54) that when g_{mq} is equal to zero, R_{eff} is equal to R_p as would be expected. However, as g_{mq} is increased and approaches a value of $1/R_p$, i.e. $g_{mq}R_p = 1$, the denominator goes to zero, and R_{eff} approaches infinity, pushing the resonant tank quality factor to infinity. It should also be noted that as the value of g_{mq} continues to increase, R_{eff} becomes negative, and the circuit theoretically (and practically) become an oscillator. Now, substituting the appropriate variables for R_{eff} and R_p , the total effective quality factor is given by

$$Q_{eff} = \frac{Q_o}{1 - g_{mq}\omega_o L Q_o} \quad (55)$$

where Q_{eff} and Q_o are the enhanced and non-enhanced resonator quality factors, respectively. Finally, the sensitivity of Q_{eff} to changes in g_{mq} is described by

$$S_{g_{mq}}^{Q_{eff}} = \frac{\partial Q_{eff} / Q_{eff}}{\partial g_{mq} / g_{mq}} = \frac{g_{mq}}{Q_{eff}} \frac{\partial Q_{eff}}{\partial g_{mq}} = \frac{g_{mq}\omega_o L Q_o}{1 - g_{mq}\omega_o L Q_o}. \quad (56)$$

A graphical representation of the theoretical enhanced quality factor and Q -tuning sensitivity plotted as a function of the resonance frequency, tank inductance, non-enhanced quality factor, and g_{mq} is presented in Figure 4.18. It is evident from the plots in Figure 4.18 that the value for Q_{eff} and S begin to converge, as might be intuitively expected, and both approach infinity as the loss in the tank is completely negated by a value of $g_{mq} = 1/\omega_o L Q_o$. Also, if R_p is assumed equal to one, i.e. $\omega_o L Q_o = 1$, then Q_{eff} is a relative quantity, Q_{eff}/Q_o , representing the ratio of enhanced to non-enhanced resonator quality factor.

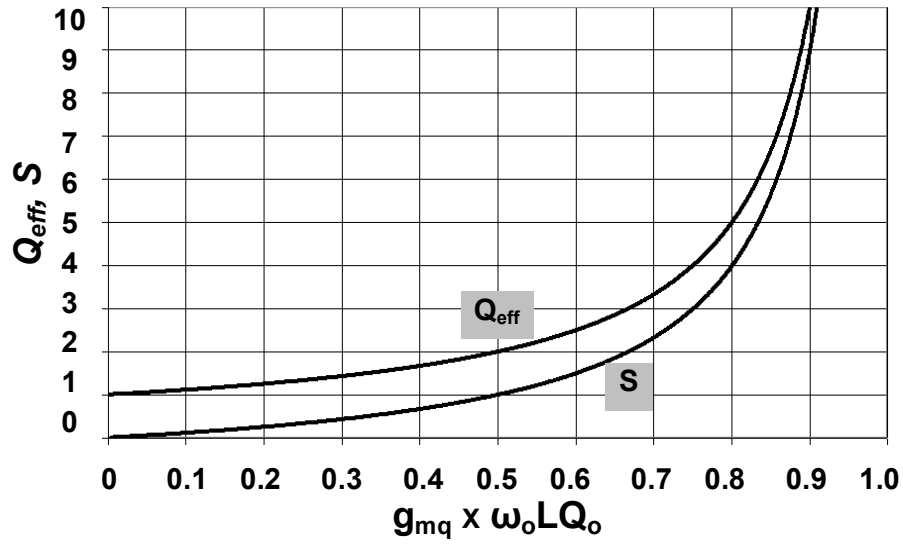


Figure 4.18. Q_{eff} and Sensitivity as a function of g_{mq} , ω_o , L , and Q_o .

The information in this section has been provided to establish a general understanding of the effects of loss restoration and quality factor enhancement on parallel LC resonators. This examination of Q and S can be specifically applied without any loss of accuracy to the transformer-coupled RF bandpass filter which is the focus of this research by assuming the values for g_{mq} shown in this section are relative to, and greater than, the value of $2g_{ml}$ that was presented in Equation (51).

4.4 Detailed Circuit Description and Design Methodology

Figure 4.19 shows a complete schematic of the transformer-coupled Q -enhanced RF bandpass filter circuit, including off-chip components connected for interface to measurement instrumentation. In the schematic, connection nodes denoted with the ‘O’ symbol are each labeled with a reference designator and represent bondwire pads that are included in the subsequent fabrication of the circuit.



The circuit reference designators in Figure 4.19 are also utilized in following sections for additional circuit schematics or IC layout diagrams. Any components shown ‘outside’ of the pads in Figure 4.19 are external components connected to the circuit via wafer probes for ensuing experimental verification. Also, the standard notation of upper-case letters or symbols for dc nodes or connections and lower-case letters or symbols for ac nodes or connections is used.

In the circuit, the transformer is comprised of inductors L_D and L_S while an additional inductor, L_{degen} , is connected to the source of the Q -enhancement transistor, M_Q , to provide negative feedback and resultant linearization for this device. Notice that although the simplified ‘series-resistance’ model for the inductors is shown in the schematic, the more exact π -model for the inductors was extracted using ASITIC and incorporated for the purpose of circuit simulation. The inductor values selected for the transformer coils were chosen in part based on the projected maximum signal deflection at the tank node, i.e. the drain of M_Q and M_I . This signal swing projection was derived from maximum expected input signal requirements and mandatory quality factor for Bluetooth operation as well as the effective parallel tank resistance that would be present at the prescribed quality factor of approximately thirty. Details pertaining to this effective parallel resistance were presented in Section 3.3.1 and additional detailed design information is outlined in Appendix A.

The transistors included in the design and shown in Figure 4.19 were employed to facilitate three distinct circuit operational requirements, and the W/L ratios for each device are shown in the schematic for reference. Transistor M_I is the circuit input buffer and was designed for a moderate transconductance to drive the expected tank impedance

within the voltage swing constraints described previously. The smaller area of M_I also intrinsically provides reduced gate-to-source and gate-to-drain component parasitic capacitance, thereby increasing input bandwidth. This reduced parasitic capacitance also increases isolation from the filter resonant tank node, v_D , back to the input of M_I . The transconductance for M_Q was designed for the expected required loss restoration, with margin for reasonable adjustments. The output buffer, M_{out} , does not provide a specific function for the operation of the filter. This component is a source-follower designed for a transconductance of approximately 20-25 mS to drive the 50 Ω input impedance of connected measurement instrumentation while providing isolation for the circuit resonant tank.

Two types of integrated capacitors were employed in the design. The signal bypass capacitors, C_{BP} , are NMOS transistor capacitors, each with total area of 2154 μm^2 . The size for these components was chosen based on the parameter for capacitance per area provided in the electrical design rules of the utilized National Semiconductor CMOS process, and in order to provide sufficiently low impedance at the operating frequency of the filter. This low impedance was required to facilitate signal bypass for connected power supplies. The tank capacitor, C_I , was implemented with an accumulation mode poly to N-well device included as a model in the National Semiconductor model library. The value of this component was chosen to augment existing circuit parasitic capacitance and resonate with the designed transformer coils at the required operational frequency of the filter.

The off-chip components shown in Figure 4.19 include input/output signal coupling capacitors, and inductive loads. The capacitors, C_{coup} , are implemented with

commercially supplied SMA feedthrough components that contain high- Q capacitors with values of ~ 4 nF, providing a sufficiently low impedance signal path for the frequency of operation. The inductor, L_{Sout} , is a commercially manufactured 47.7 μ H device, and is utilized as an RF choke for the supply connected to the source of M_{out} . This component provides extremely high impedance at the frequency of operation, allowing the low-impedance source output of M_{out} to effectively match with the subsequent 50 Ω input of connected RF measurement instrumentation. All of these off-chip reactive components were experimentally measured for lower frequency (~ 10 MHz) operation to confirm component and quality factor values. Manufacturer supplied data was referenced to confirm specific operation at the gigahertz frequency ranges of operation.

4.4.1 Output Buffer: Additional Details

Additional information regarding the output buffer circuit utilized to facilitate isolated connection for circuit test is described in this section. This further discussion is warranted as subsequent filter measurements and operational analysis reference the projected and calculated gain for this part of the circuit.

As previously described, transistor M_{out} is included as a buffer for the designed filter circuit to provide an interface to any output connection and minimize loading of the resonant tank. M_{out} is configured as a source-follower amplifier in order to provide a high-impedance input to the resonant tank and a low-impedance output to drive and match the 50 Ω input of the any microwave or RF measurement instrument connected to the output of the circuit. Figure 4.20 shows a simplified schematic diagram and small-signal model of an NMOS source follower driving a prospective load, Z_s .

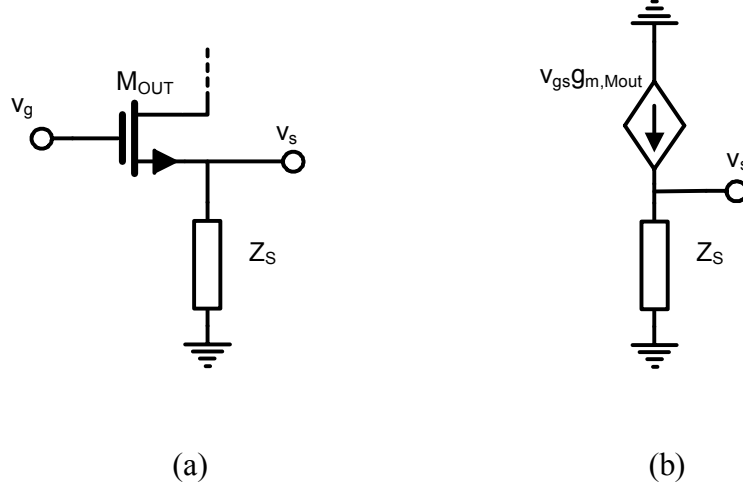


Figure 4.20. Source-follower topology for M_{out} . (a) Schematic. (b) Small-signal model.

The gain from gate to source of the source follower circuit shown in Figure 4.20 is given by

$$\frac{v_s}{v_g} = \frac{g_m Z_s}{1 + g_m Z_s}. \quad (57)$$

For M_{out} , the transconductance was experimentally measured at a value of 25 mS for the bias levels used during test of the circuit. Now, assuming that the driven impedance Z_s corresponds to the characteristic input impedance of an RF measurement instrument, i.e. 50 Ω , the gain from gate to source is calculated at 0.556 or -5.11 dB. These figures for the source-follower gain are referenced later during measurement results analysis, and details of the bias measurement for M_{out} , as well as M_I and M_Q are also presented in subsequent sections.

4.5 Layout Considerations and Implementation

The layout of the Q -enhanced RF bandpass filter circuit is shown in Figure 4.21. This diagram includes references to circuit physical dimensions, pad size, and spacing (in μm). Signal reference designators are also presented, corresponding to nodes identified with the ‘O’ symbol in Figure 4.19. Several components are identified in the figure including inductors, transistors, and one of four RF signal bypass capacitors. The three other non-referenced bypass capacitors can also be seen connected to ground pads on the left side of the layout, and test inductors are present in the upper-right corner of the circuit.

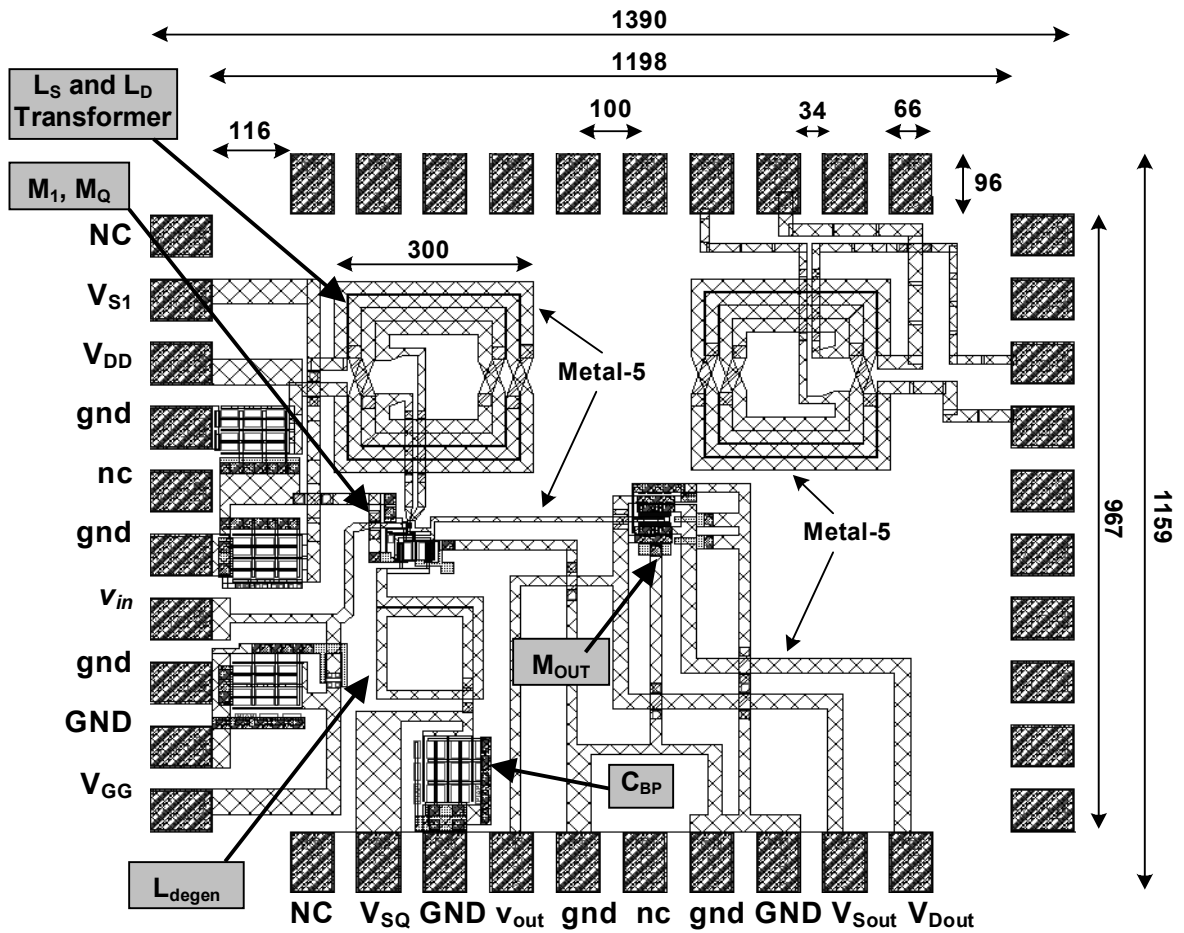


Figure 4.21. RF bandpass filter circuit layout.

For clarity, Figure 4.21 omits the fill blocks that were necessary in the final layout. These fill blocks are required to allow the circuit to pass National Semiconductor Design Rule Checks (DRC) for chip surface metal density, and are added to the layout as a last step before the design is submitted for fabrication.

The transformer metal traces were fabricated using the top-most process conductor, Metal-5, while transformer underpasses utilized the next underlying process conductor, Metal-4. Metal-5 was also used for signal routing paths throughout the circuit and was incorporated as the primary signal-carrying conductor because of greater thickness and associated lower intrinsic resistance. This aluminum layer is 859.5 nm thick and has a sheet resistance of $36 \text{ m}\Omega/\square$, which is less than or equal to one-half the resistance of the lower metal layers. Additionally, this top-level metal is least affected by substrate losses because of the physical location of this material near the ‘surface’, and away from the grounded substrate, of the progressively stacked CMOS-9 process layers.

Based on the fact that wafer probe testing was intended for verification of the fabricated circuit, the size and spacing of the pad layout was guided not only by the required circuit dimensions, but also by constraints dictated by the test probe manufacturer, Cascade-Microtech. In the Cascade design guide outlining layout rules for gigahertz probing [64], certain constraints regarding the physics of the input, output, and bias line pads warrant consideration. These constraints were considered for this particular test circuit where perpendicular adjacent ten-pin probes would be required to connect, or ‘land’, on the pads lining the ‘west’ and ‘south’ periphery of a small die that contained the fabricated circuit. The orientation of the probes in relation to the circuit die is depicted in Figure 4.22.

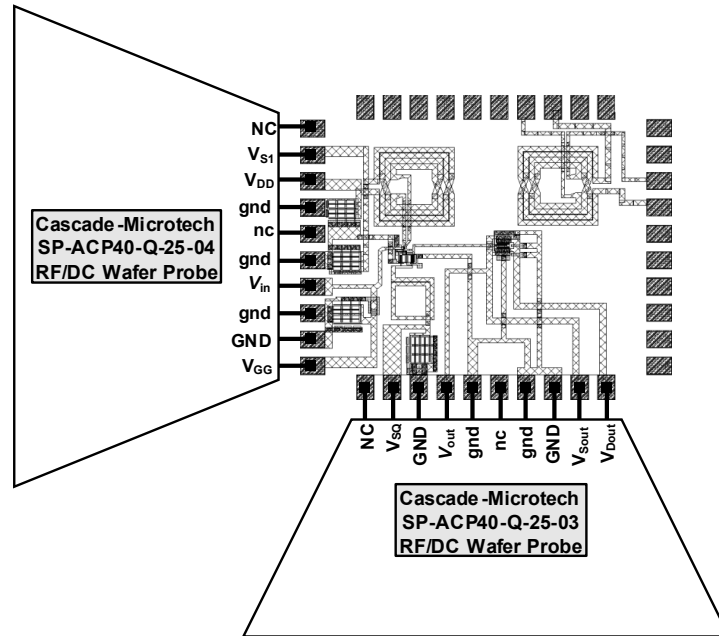


Figure 4.22. Orientation of wafer probes and circuit die.

A summary of the applicable design constraints and expected probe ‘landing’ characteristics from [64] is outlined below:

- Pad size: 50 μm x 50 μm minimum.
 - Corresponds to minimum tip size for 100 μm spaced probes.
- Pad pitch or spacing: 50 μm minimum.
- Passivation window over the pad: 96 μm x 96 μm minimum.
 - This window allows access to the pad metal for probe contact.
 - It is acceptable for passivation window size to exceed pad dimensions.
- Corner spacing for orthogonally oriented probes: 200 μm minimum.
- Nominal probe ‘skating’ or ‘overtravel’: 50 μm minimum.
 - Continued forward probe movement required to assure probe/pad contact.

4.5.1 Layout Detail: Transformer and Bypass Capacitors

A magnified portion of the circuit layout presented in Figure 4.21 is presented in Figure 4.23. This diagram provides a closer examination of the circuit transformer and one of the four large RF signal bypass capacitors. Also in Figure 4.23, the reference to the area labeled 'A' highlights a section of the layout subsequently expanded and detailed in Figure 4.24.

As detailed in Figure 4.23, the circuit transformer is comprised of two inductors, one coupling a bias supply to the input transistor source (V_{S1} to $M_{1,S}$), and the other coupling a bias supply to the input transistor drain (V_{DD} to $M_{1,D}$).

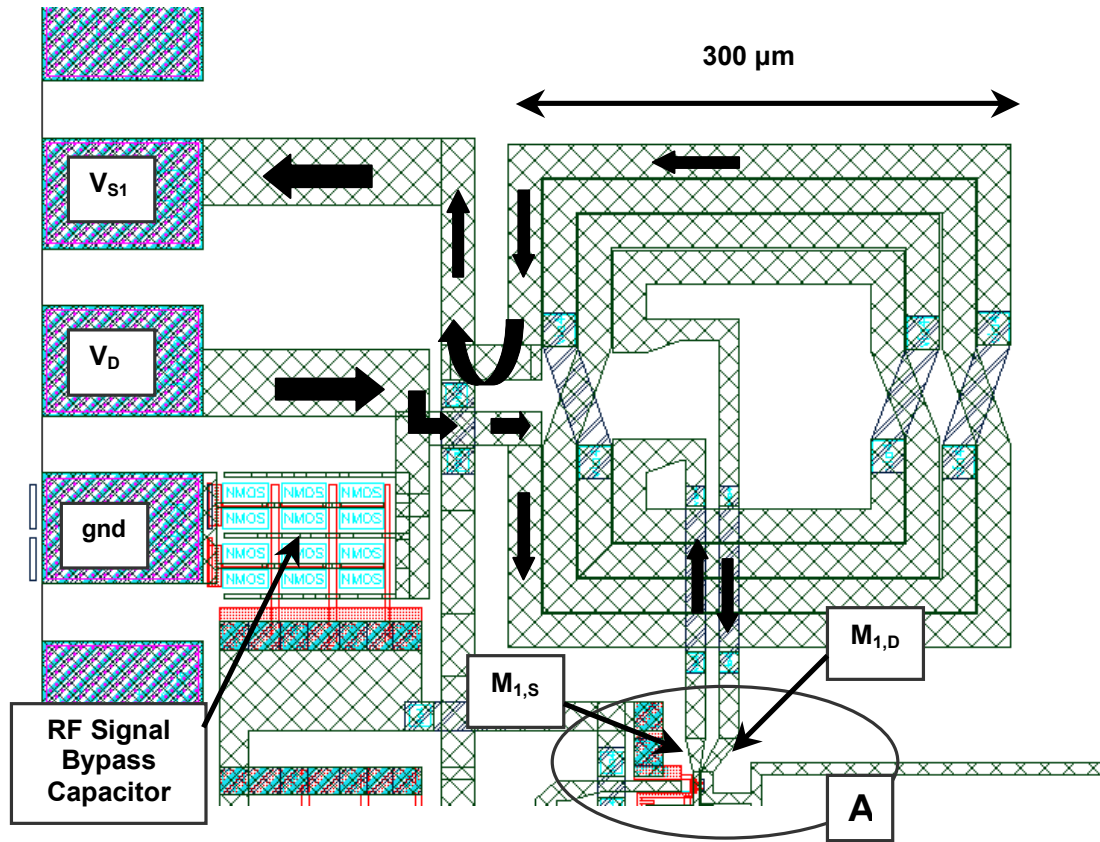


Figure 4.23. Circuit layout details: Transformer and RF signal bypass capacitors.

The current flow directions for the bias supplies are identified in the figure by the arrows and shown here to underscore the polarity of the transformer windings. This transformer polarity is critical in facilitating the positive feedback loop consisting of M_I , M_Q , L_S , and L_D . The transformer is implemented with a square-symmetric topology in the top-most process metal, Metal-5, with underpasses fabricated using the lower adjacent metal, Metal-4. This symmetric transformer topology facilitates source and drain inductors, L_D and L_S , of equal values and quality factors. The total width of the transformer is 300 μm , the trace widths of the coils are 20 μm , and the spacing between coils is 1 μm . These dimensions were selected to balance the required inductance and quality factor with a maximized coupling coefficient while attempting to minimize the total area of the component. Each of the inductors and the transformer were simulated using ASITIC with CMOS-9 process parameters provided by National Semiconductor. These process parameters are imported into ASITIC to provide the physical and electrical characteristics of the metal layers and substrate.

The RF signal bypass capacitors are required at all chip bias inputs to provide a low-impedance path to ground for the high-frequency signals. These bypass capacitors serve the purpose of negating the high-frequency loading effects of the bias cables and the bias supplies inherent to the single-ended nature of the design. Each bypass capacitor was implemented using twelve NMOS transistors, each having sixteen gate fingers with W/L dimensions of 11.0/1.02 μm . The multi-finger layout was used to minimize required chip area. These bypass capacitors could be incorporated external to a packaged chip, but because the signal measurements of this circuit were to be accomplished via wafer probe testing, external capacitor connections were impractical. Also, in regards to the bypass

capacitors, a differential version of this circuit would have an intrinsic virtual ground, thereby theoretically alleviating, or greatly reducing, the signal bypass requirement.

4.5.2 Layout Detail: Transistors and Signal Routing

Figure 4.24 provides a close-in view of the connections from the transformer to the input transistor with several trace width dimensions shown for reference. Transistor M_I is also shown along with the majority of the two transistors that make up M_Q . Also in Figure 4.24, the reference to the area labeled ‘B’ highlights a section of the layout subsequently expanded and detailed in Figure 4.25.

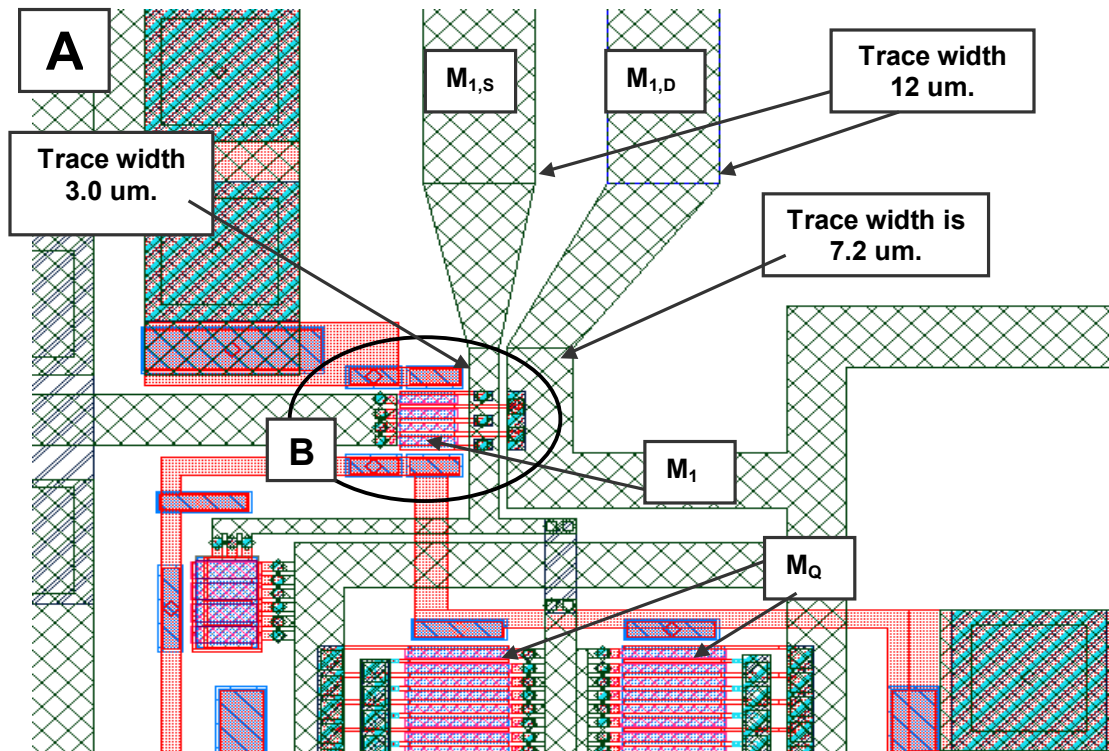


Figure 4.24. Circuit layout details: Input transistor and transformer connections.

Transistors M_I and M_Q were designed using multi-finger layouts to allow for a physically efficient use of chip real estate. M_I was fabricated using a single device with four fingers each and W/L ratios of 6.0/1.02 μm for each finger. M_Q was fabricated using two parallel devices with sixteen fingers each and W/L ratios of 11.0/1.02 μm for each finger. Although the CMOS-9 process used in this design allowed transistor gate lengths down to 0.18 μm , the active devices in this design utilized 1.0 μm gate lengths. These larger lengths were deliberately incorporated to mitigate the MOSFET short-channel effect of reduced drain-to-source resistance and also allow accurate prediction of transistor functional characteristics via the CMOS transistor square-law model. Additionally, at the moderate operating frequency of the filter, the parasitic capacitance of the medium sized transistors was small enough to be negligible. Finally, although the decreased threshold voltage inherent to shrinking MOSFET channels would facilitate larger prospective tank voltage swings, as described in Section 4.3.2, the added potential advantage of the smaller V_T values was determined non-essential in this initial implementation of the transformer-coupled bandpass filter, but could warrant future investigation for any subsequent development of this concept.

Figure 4.25 provides a close-in view of the input transistor and some additional detail pertaining to dimensions and spacing of the connecting metal traces and integrated components. As mentioned, particular attention was warranted in this part of the chip layout because component proximity and signal amplification would create significant voltage differences between adjacent signal lines. Notice that the smallest spacing with the largest dynamic voltage potential difference is the 0.8 μm spacing between the traces that connect the transformer to the drain and source of input transistor M_I .

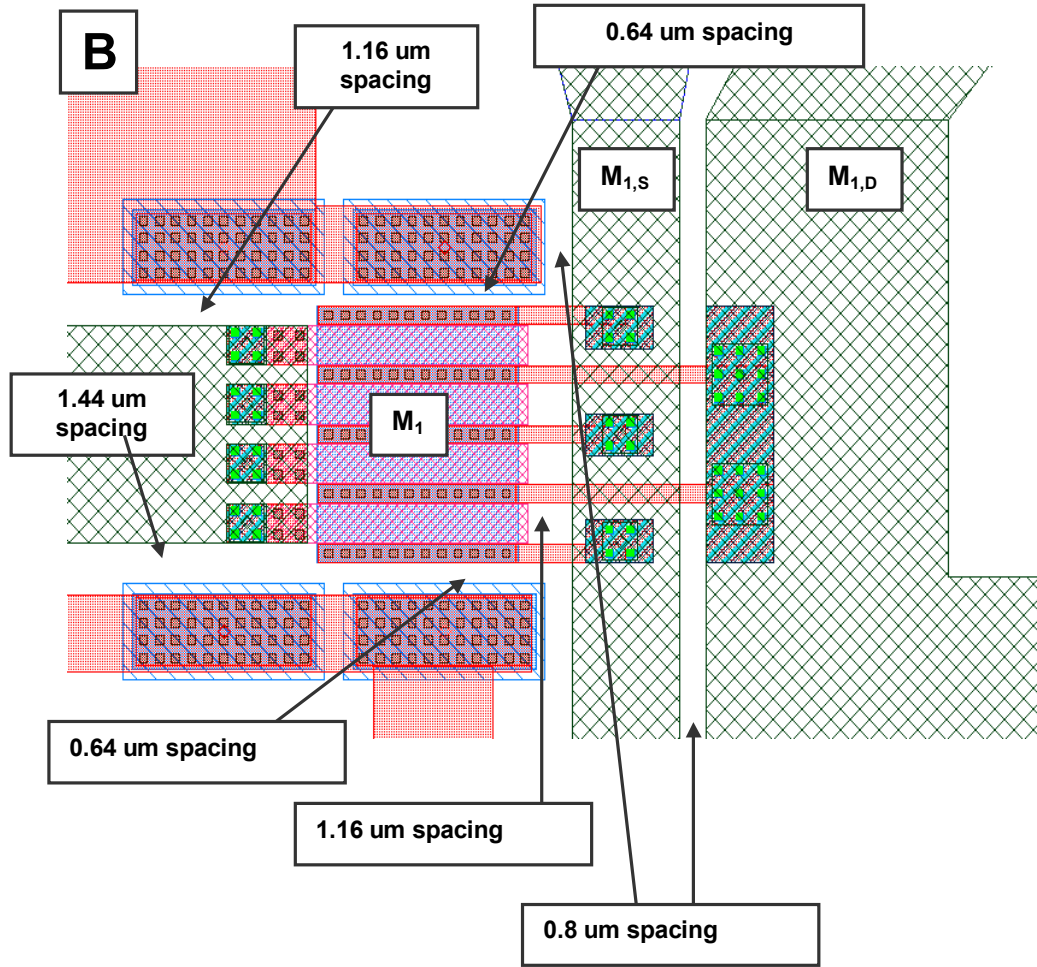


Figure 4.25. Circuit layout details: Input transistor and connection dimensions.

Some of the critical trace widths and spacing dimensions have been presented in this section to provide an idea of the spacing and dimensions used in this portion of the circuit, which has the most dense layout and highest voltage variation with respect to physical proximity between traces. Quantitative information regarding the analysis undertaken regarding parasitic capacitance effects resulting from signal path physical layout is provided in the following section.

4.5.3 Layout Detail: Parasitic Capacitance Evaluation

Layout topology in an RF or microwave integrated circuit is a critical part of the design process. Distributed parasitic components, usually capacitors, can be created by improper routing of signal paths, leading to unexpected or less than ideal circuit response. The effects of these distributed reactive components can normally be disregarded for low-frequency circuits, but exhibit significant admittance at the increased operational frequency ranges utilized in communications circuits. To verify no detrimental lateral parasitic capacitors were present in the layout of the current design, calculations for plate capacitance for closely spaced conductors of any significant length were performed.

The unit capacitance value provided by National Semiconductor for the CMOS-9 process [65] for Metal-5 to Metal-5 trace ‘coupling capacitance per side’ for traces of Metal-5 on poly is given as $111.3 \text{ aF}/\mu\text{m}$, where $\text{aF}/\mu\text{m}$ is a the unit measure per micrometer of trace length at the process-specified minimum conductor spacing of $0.4 \mu\text{m}$. For the purpose of comparison, and an independent verification of the capacitance value given by National, the Metal-5 dimensions and minimum spacing given in [65] were used to calculate an estimated unit capacitance using the simple formula for parallel plate capacitance presented in Section 3.4.1. A unit capacitance value of approximately $74.16 \text{ aF}/\mu\text{m}$ using Equation (23) was calculated. As expected, this value was lower than the experimentally extracted National values because of the omission of fringing field effects. However, this lower value was reasonably close (within one order of magnitude) and provided satisfactory verification of the National specification. For reference, Figure 4.26 shows capacitance values for parallel Metal-5 conductors with varying trace spacing and lengths at $111.3 \text{ aF}/\mu\text{m}$.

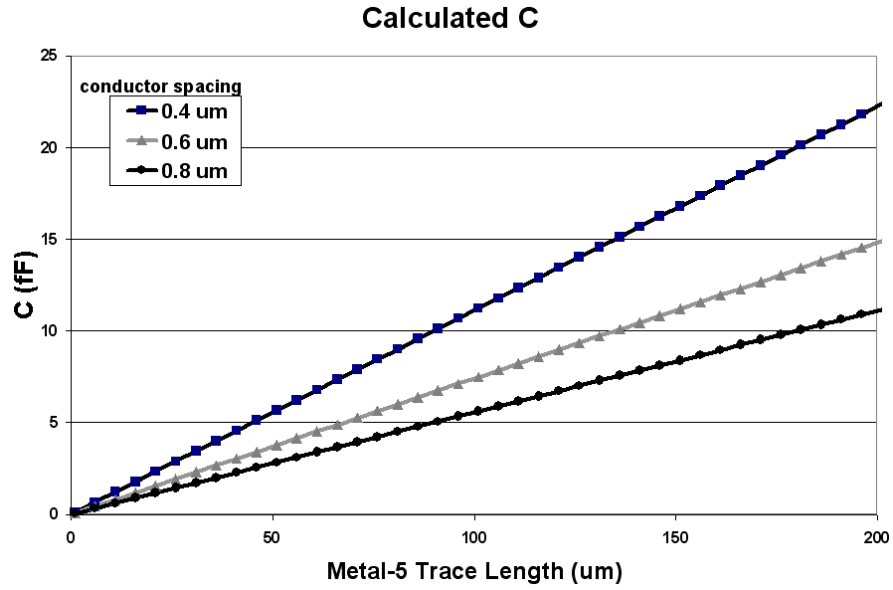


Figure 4.26. Capacitance for parallel Metal-5 conductors.

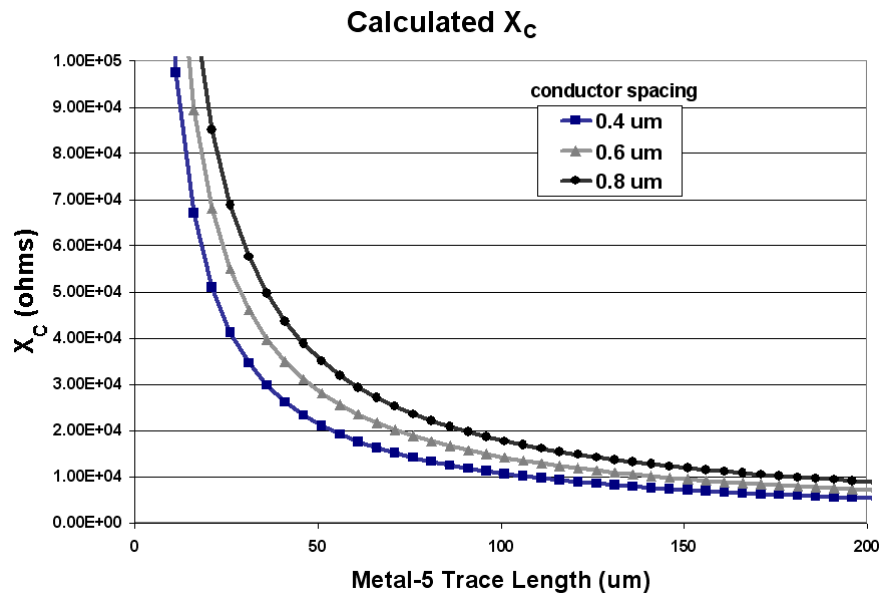


Figure 4.27. Capacitive reactance for parallel Metal-5 conductors at 2 GHz.

Additionally, Figure 4.27 shows associated capacitive reactance values for parallel Metal-5 conductors with varying spacing and lengths at a frequency of 2 GHz.

The plots in Figure 4.26 and Figure 4.27 were generated and used as a graphical reference to provide quick and approximate estimates as well as an intuitive understanding of inter-trace capacitance that could be expected for the design layout. It can be concluded from the values presented in Figure 4.26 and Figure 4.27 that the parasitic capacitance values between any parallel Metal-5 traces in the transformer-coupled bandpass filter layout should be negligible for the lengths and spacing utilized in this design. In fact, the most significant source of inter-trace capacitance in this design is attributable to the windings of the integrated transformer, as might be expected. However, these capacitance values are captured in the circuit model utilized in simulations by using the inductor π -model topology for the transformer windings that was presented in Section 3.4.3.

4.6 Simulation Results

The circuit was implemented in a 0.18 μm standard CMOS process using models provided by National Semiconductor and simulated using Analog Artist and SpectreS in the Cadence design environment. Results of the simulations provided in this section include passband response and linearity. Additionally, transient response of the circuit is analyzed to verify circuit stability. Finally, different bias settings are utilized to examine the circuit at various operating points with these simulation results being compared to other Q -enhanced RF LC filters that have been the focus of recent research.

The simulation results presented in this section are based on ideal measurement instrument characteristics and lossless circuit/instrumentation connection interfaces. Experimental results, presented in later sections, were accomplished using dc and RF wafer probes and possessed some intrinsic non-idealities. With this in mind, additional

simulation results and parameters with these non-idealities incorporated into the simulated circuits are introduced as applicable in the subsequent sections of this work dealing with experimental results. The results in these ensuing sections present comparisons between these ‘non-ideal’ simulated circuit characteristics and experimental results extracted from actual circuit wafer probe tests, with the intent of correlating the expected and measured responses of the circuit. However, for this section, the ideal simulated ‘test’ conditions are examined to determine the prospective characteristics of the circuit assuming integration into a larger system and without regard for other anomalous losses or the need to interface the filter with any external measurement instrumentation. It should also be noted that this section presents condensed information from a previously published work [66], which can be referenced for additional details.

Three versions of the circuit shown previously in Figure 4.6 were implemented and simulated to validate operation with different supply voltages and to investigate the effects of L_{deg} on the circuit operation. Component values for the inductors and capacitors of the resonant tank were chosen to realize a circuit with prospective operation as a front-end bandpass filter for a Bluetooth receiver with a center frequency of 2.44 GHz and a bandwidth of 84 MHz. These different implementations of the circuit were simulated and presented to highlight the adaptability of the design for specific targeted specifications of dynamic range, power consumption, and low-voltage operation. The component values for three variations of the circuit are shown in Table 4.1. The inductor values shown were extracted using the ASITIC modeling program and National Semiconductor 0.18 μm IC process parameters. Values of $Q > 5$ were achieved for the simulated 1nH inductors, but a value of $Q = 4$ was used in the simulation.

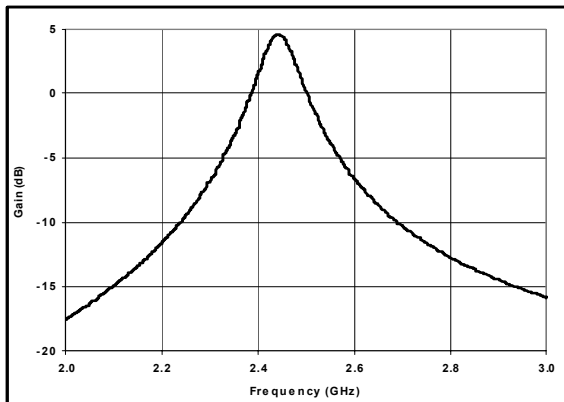
Table 4.1. Circuit component values for transformer-coupled RF filter.

Circuit	V _{DD} (volts)	L _D , L _S (nH)	C (pF)	L _{degen} (nH)
1	1.6	1	0.60	1.1
2	1.6	1	0.76	0
3	1.2	1	0.60	1.1

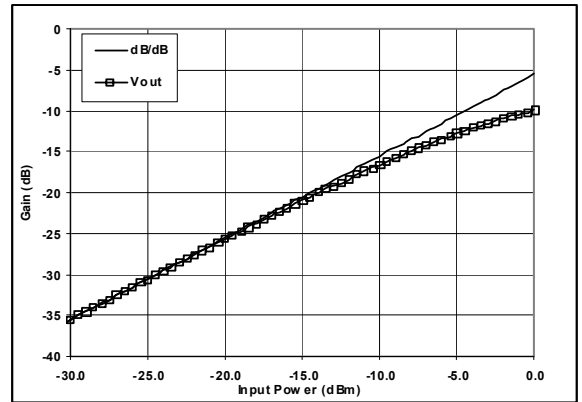
Also, integrated transformer coupling coefficients of 0.9 have been achieved [45], but a value of $k = 0.8$ was used. The lower values for k and Q were utilized to maintain conservative estimates for circuit response characteristics.

4.6.1 Simulated Passband Response and Linearity

The circuit was simulated with the bias values for the gate and source of M_Q adjusted to provide a quiescent point and loss restoration for a quality factor of approximately 29, which corresponds with the required Bluetooth bandwidth of 84 MHz. Figure 4.28 shows the simulated passband response and input compression point, P_{1dB} , for the transformer-coupled RF bandpass filter circuit referenced as Circuit #2 in Table 4.1.



(a)



(b)

Figure 4.28. Response for circuit #2. (a) Passband. (b) P_{1dB} .

These results show that the Circuit #2 implementation with the component values and supply voltage detailed in Table 4.1 and tuned for an 84 MHz bandwidth provides a gain of 5 dB, an input compression point of approximately -10.5 dBm, and a relatively symmetrical second-order passband response.

4.6.2 Simulated Stability Response

In order to determine correct circuit operation upon initial start-up or application of the dc bias supplies, the stability of the circuit was investigated. The stability of the filter was tested by simulating an initial stepped current of 100 μ A in the circuit transformer. This initial inductor current was used to emulate power supply turn-on and the higher than expected value of 100 μ A was used to simulate worst-case circumstances, thus providing the most conservative estimates for proper operation. A transient analysis was run in Cadence and the filter output was analyzed to verify that the initial perturbation of the resonant tank, resulting in an initial oscillation at the fundamental frequency of the filter, would eventually dissipate to zero. This eventual damping of the initial sine wave validated the required non-oscillatory and stable behavior of the circuit. The resultant transient response of this simulated experiment is shown in Figure 4.29.

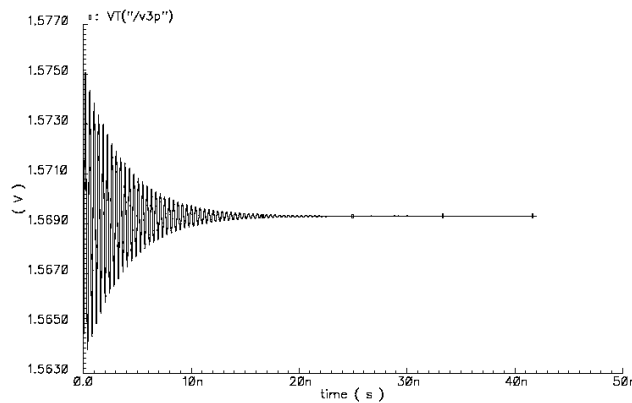


Figure 4.29. Transient response for transformer-coupled filter stability verification.

Additionally, and to provide related reference information, it can be shown that other circuit characteristics may be extracted from the transient response. The quality factor, Q , of the circuit is determined from the decaying waveshape shown in Figure 4.29 by measuring the decay times and amplitudes of the response and applying this data to

$$A(t) = A(t = 0) \times e^{-\alpha / 2Q} \quad (58)$$

and

$$Q = \frac{\omega(t_2 - t_1)}{2 \ln(A_1 / A_2)} \quad (59)$$

where $A(t)$ is the amplitude with respect to specific times of $t > 0$, and Q is the quality factor of the filter. This information is provided for general reference and no detailed calculations for the filter circuit presented in this research are performed or presented.

4.6.3 Simulation Comparison With Recent Research

A summary of the filter performance characteristics (Ref. 1, 2, and 3) along with a comparison to recently published CMOS integrated filters is detailed in Table 4.2 with the targeted specifications of dynamic range, power consumption, and low-voltage operation for each of the three circuit implementations highlighted in bold text.

The data in Table 4.2 shows that all three filters analyzed in this section achieve input referred noise power below -70 dBm over the 84 MHz filter bandwidth. This translates to a maximum input noise power of -89 dBm for a 1 MHz Bluetooth IF bandwidth. With these sensitivity levels and the presented input compression points, all of the designs meet the Bluetooth input dynamic range specification of 50 dB, i.e. -70 dBm to -20 dBm, with comfortable margin.

Table 4.2. Transformer-coupled RF filter performance and comparisons.

Ref	V _{DD} (volts)	f _o (GHz)	BW (MHz)	Gain (dB)	PD (mW)	P _{1dB} (dBm)	DR (dB)
1	1.6	2.44	84	4.2	14.9	-4.9	65
2	1.6	2.44	84	4.6	2.35	-10.6	63
3	1.2	2.44	84	4.2	6.24	-16.2	56
[67]	1.3	2.19	53	7	5.0	-30	38
[21]	2.5	2.14	60	0	17.5	-13.4	56
[55]	3	0.89	30	17	78	-47	-

4.7 Measurement Results and Comparison

The operational characteristics of the filter circuit were measured to validate circuit response at dc and RF. The dc quiescent points measured were the transistor drain currents versus applied gate and drain voltages. The RF characteristics measured included passband response, linearity, and noise. The following sections present details of the test setups used for these measurements, the measured circuit response characteristics, and a comparison of the measured parameters and the expected values predicted from simulation results. The simulation results presented in these sections differ from the results in Section 4.6 in that additional components have been added to the previously presented circuit to emulate the non-ideal characteristics of the circuit-to-instrument interface, i.e. wafer probes. The results in these sections compare experimental data extracted from circuit wafer probe tests and these ‘non-ideal’ circuit simulations, with the intent of correlating circuit measured and expected responses. Justification for the insertion of any components required to emulate test condition parasitic characteristics are presented as applicable. To conclude, the experimental results of this work will be compared with other recent research involving integrated RF filters.

4.7.1 Test Setup and Methodology

A photograph of the wafer probe test station used to facilitate dc and RF measurements is shown in Figure 4.30. The connections in the figure show the probes positioned for calibration of the network analyzer. The wafer probe station used to facilitate connection of the device under test (DUT) to the dc supplies and RF stimulus/measurement instrumentation is a hybrid combination of components selected specifically for gigahertz frequency testing of RF filters, oscillators and amplifiers. As shown in Figure 4.30, the main platform is a REL-4300 wafer probing station using an Allesi probe positioner bolted to the left or ‘west’ side and a Cascade-Microtech MPH Series removable micropositioner/extender on the right or ‘east’ side.

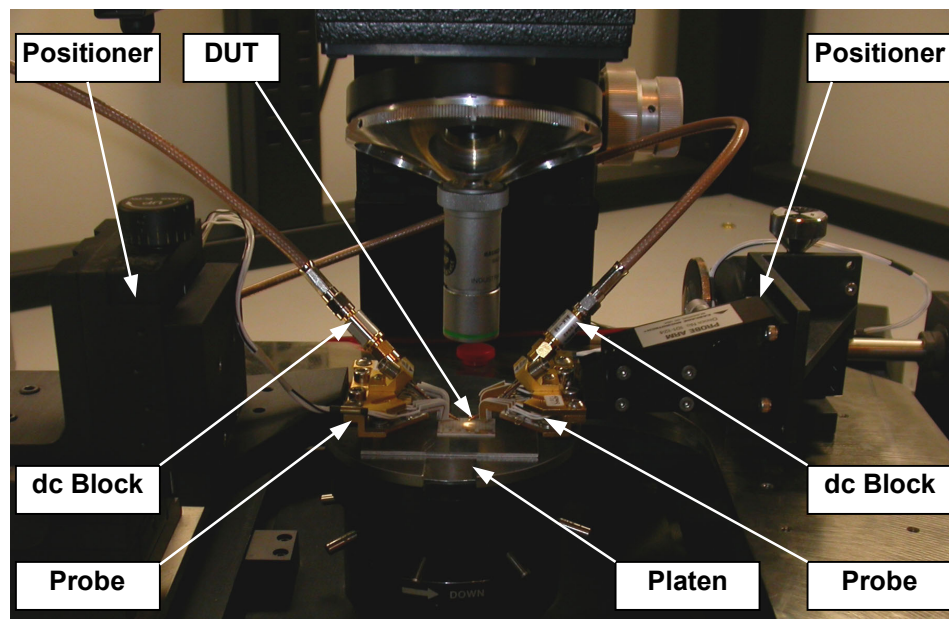


Figure 4.30. Photograph of probe test station with RF/dc probes connected.

The removable Cascade positioner utilizes a vacuum base for attachment to the station at variable locations on the station platform that surrounds the DUT on three sides. The Cascade probe is shown on the east side of the platform but was also positioned at the top or ‘north’ side of the station as necessary for test. A platen, or platform to accommodate the DUT, is located between the two probe platforms. This platen is designed with a small opening and peripheral indentations in the top metal surface that facilitates introduction of a vacuum to secure an entire IC wafer for probe test. However, given that the fabricated integrated circuits provided by National Semiconductor were diced to a size of approximately 4 mm², a brushed aluminum adapter plate was fabricated to interface to the platen and allow attachment of a single die via the platen vacuum. To isolate the input dc bias voltages from connected RF instrumentation, SMA dc blocks (MCL P/N 15542 BLK-18) were connected between the probe 3.5 mm female connectors and the RF cable male connector ends. A Bausch & Lomb MicroZoom II high-performance microscope was used to view the probe tips and DUT, facilitating alignment and connection of the probes with the circuit die. As shown in Figure 4.30, the microscope is attached to the probe station and oriented for a top view of the DUT and platen.

A microphotograph which shows a magnified view of the circuit die along with a view of the wafer probes positioned for test execution is presented in Figure 4.31. In the figure, the circuit inductors and transistors are identified and the pads are labeled with the signal and bias reference designations. Also, the view in Figure 4.31 has been rotated 90° counter-clockwise (CCW) when referenced to the view in Figure 4.30 to correspond with the orientation of the layout diagrams presented in Section 4.5.

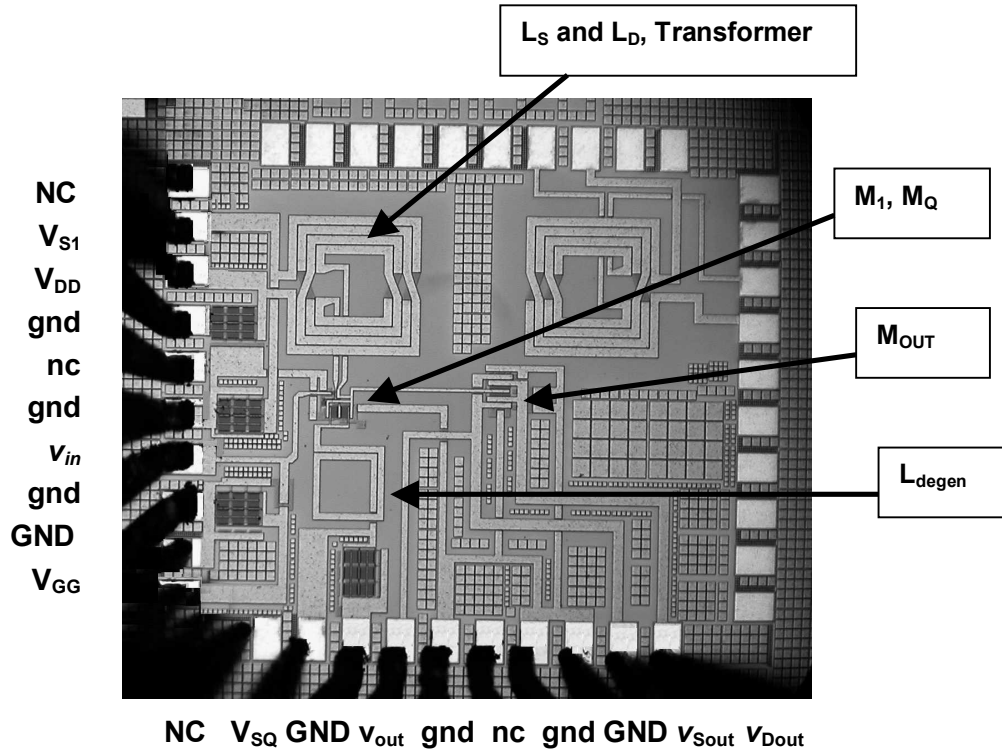


Figure 4.31. Microphotograph of circuit showing layout and test probe position.

The probe positioners were actually mounted on the west and north sides of the probe station platform when the circuit was connected for test.

Figure 4.32 shows a block diagram of the complete test setup connected for RF calibration or passband response measurements. The figure also includes the required dc supplies along with RF components and instruments not shown in Figure 4.30. The DUT is shown connected for test in the figure; however, a Cascade-Microtech impedance standard substrate (P/N 101-190) would be connected in the DUT location for required network analyzer calibration. For noise measurements, the HP 8714C Network Analyzer and HP 8496A Variable Attenuator were removed from the setup shown in the figure, and a Rohde & Schwarz Model FSU-8 spectrum analyzer was connected.

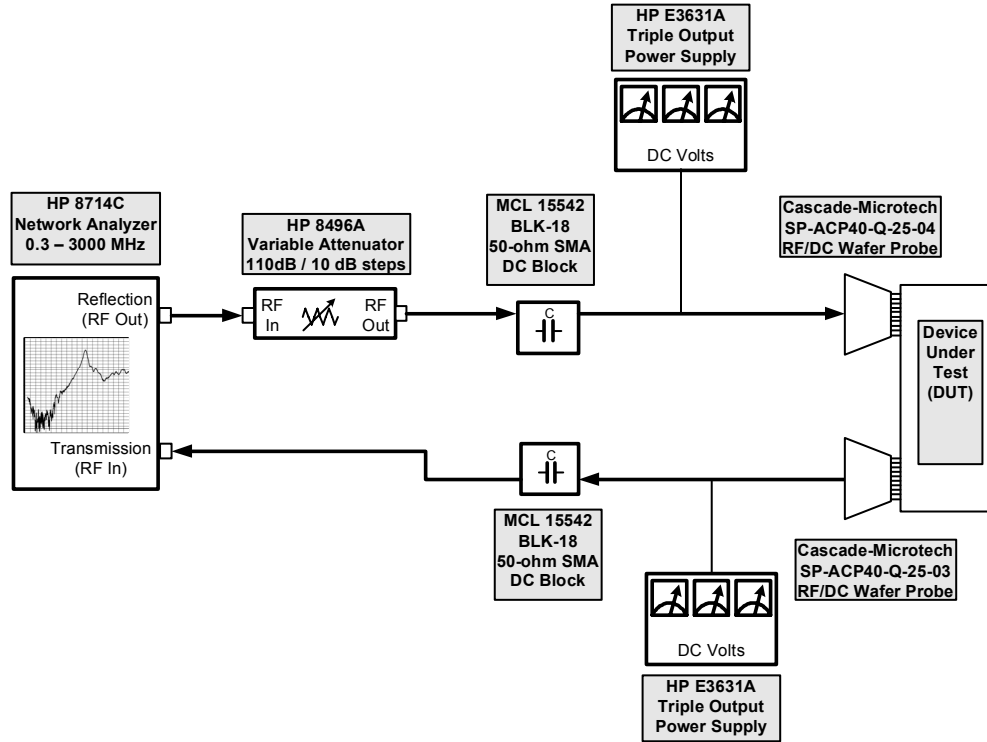


Figure 4.32. Block diagram of complete test setup.

Additional details pertaining to instrument setups utilized for specific low frequency and RF tests are detailed in subsequent measurement results sections as applicable. These details include setup block diagrams as well as measurement and stimulus equipment calibration and settings.

4.7.2 Low-Frequency Bias and Transconductance Measurements

As a preliminary test step to validate circuit operation at low frequency, the dc quiescent points and the transconductance values of the circuit transistors were measured and calculated for comparison with expected results extracted from circuit simulations. Figure 4.33 presents a block diagram of the test setup used to perform characterization of the drain current versus gate voltage and transconductance for M_I , M_Q , and M_{out} .

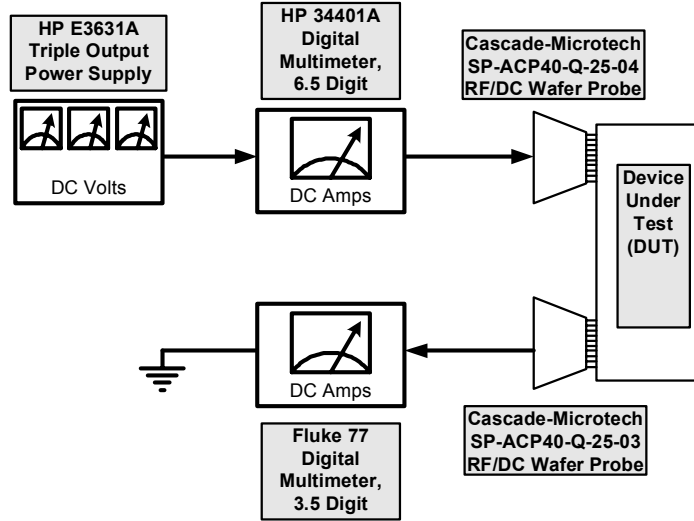


Figure 4.33. Block diagram of dc test setup.

A simplified schematic of the filter circuit showing the paths for the three measured quiescent currents, $I_{D,I}$, $I_{D,Q}$, and $I_{D,out}$ is presented in Figure 4.34. This diagram is a simplified version of the detailed schematic presented in Figure 4.19 with external components that would have no significant effect at low frequencies omitted. As previously detailed, the nodes identified with the ‘O’ symbol represent points in the circuit where pads are connected to external components or measurement instruments.

Table 4.3 details the value or range of voltages provided by the four variable power supplies shown in Figure 4.34. These supplies were selectively connected and adjusted to extract the values of the drain currents for the three circuit transistors. In Table 4.3, where the indicated voltage value is zero, the supply was removed, and a direct ground connection was applied. Additionally, and as detailed in the table, the selection of bias voltage application to isolate and test each transistor independently while electrically disabling the other two untested active devices is evident.

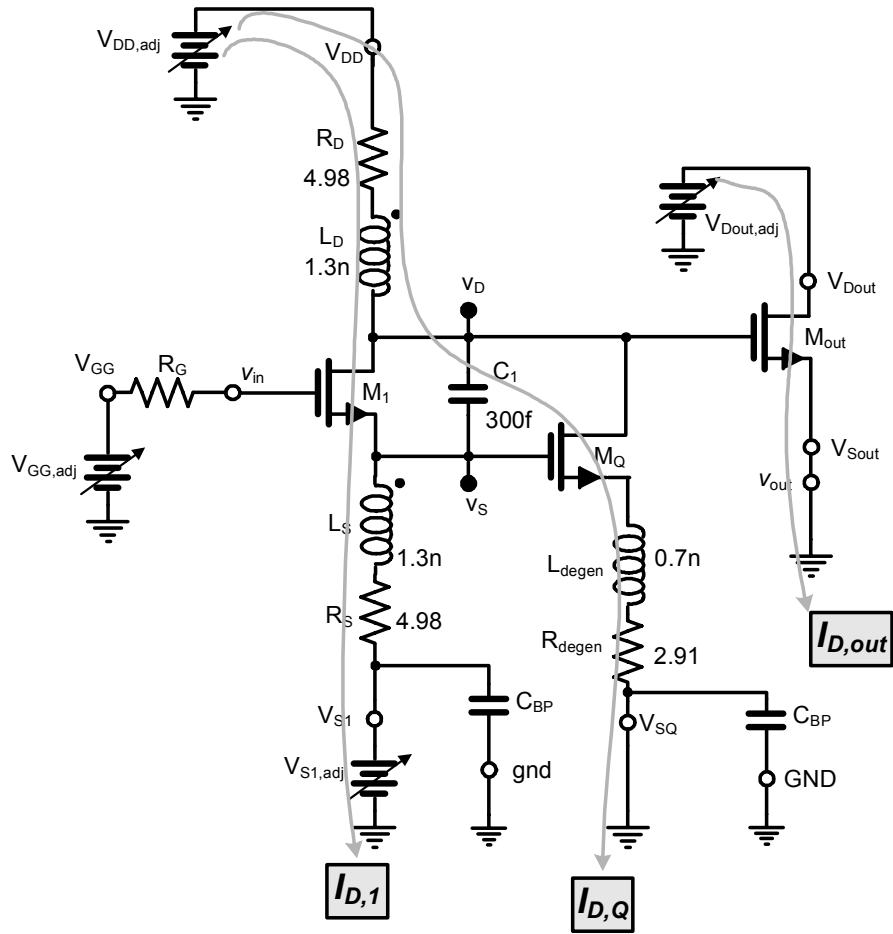


Figure 4.34. Schematic showing paths for measured dc currents.

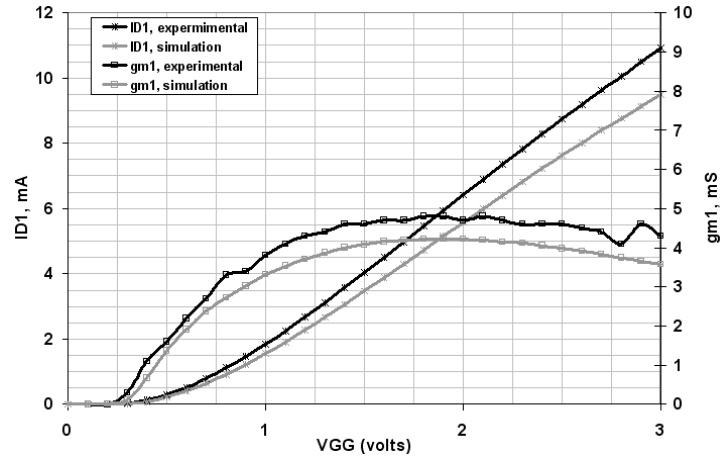
Table 4.3. dc voltages for bias current measurements.

Parameter	V_{GG} (volts)	V_{DD} (volts)	V_{S1} (volts)	V_{Dout} (volts)
$I_{D,1}$	0 to 2.2	2.2	0	0
$I_{D,Q}$	0	2.2	0 to 2.2	0
$I_{D,out}$	0	0 to 2.2	0	2.2

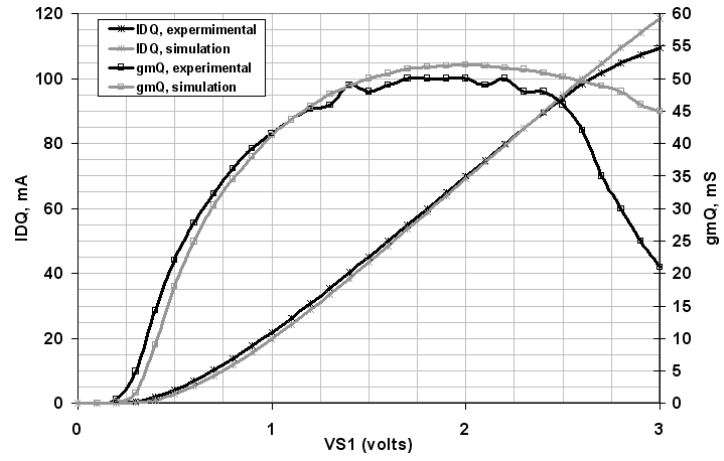
Several discrete points of data were taken for the drain current and corresponding gate voltage for each of the three transistors. The drain current and gate voltage were then recorded and used to calculate the transconductance for each transistor at successive measurement points using

$$gm_{b-a} = \frac{I_{D_b} - I_{D_a}}{V_{G_b} - V_{G_a}}. \quad (60)$$

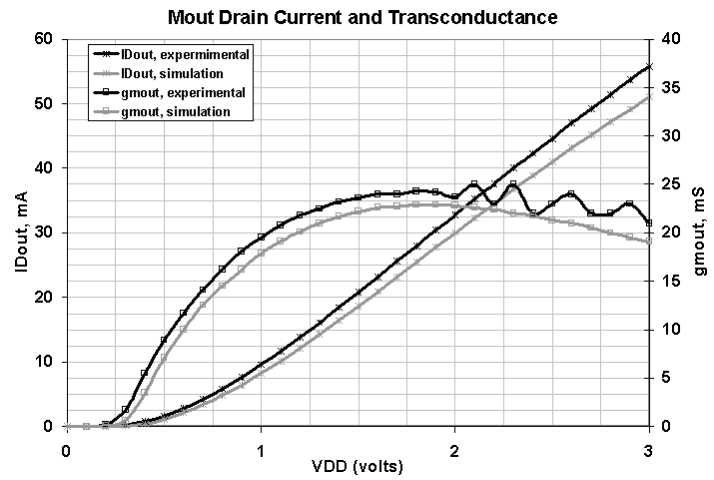
In Equation (60), gm_{b-a} is a single transconductance value for two successive data recordings, I_{D_a} is the measured dc current value corresponding to the applied gate voltage, V_{G_a} , and I_{D_b} is the next value of measured dc current corresponding to a slightly increased gate voltage, V_{G_b} . Several discrete values were calculated using Equation (60) and the measured values of drain current to produce a curve representing the transconductance of each transistor. Simulated current measurements and subsequent calculated transconductance values were also extracted from dc simulations performed with Cadence using incremental bias levels similar to those utilized in the experimental method. Figure 4.35 presents a graphical comparison of the experimental and simulated drain current and transconductance values for the three circuit transistors. As the plots in the figure detail, all of the circuit transistors exhibited experimental electrical characteristics very similar to the predicted simulation results in both drain current and transconductance.



(a)



(b)



(c)

Figure 4.35. Experimental and simulated I_D and gm values (a) M_1 . (b) M_Q . (c) M_{out} .

4.7.3 RF Passband Response

A block diagram of the RF test setup connected for measuring filter passband response and input compression point is shown in Figure 4.36. The dc bias supplies are also connected for this test, but are omitted from this figure for clarity. The HP 8714C Network Analyzer output power is set for 0 dBm and the HP 8496A Variable Attenuator is set to reduce the power level by 30 dB. This provides an input power level of -30 dBm to the MCL 15542 SMA dc Block, and subsequently to the device under test (DUT) via the Cascade-Microtech wafer probe. The -30 dBm input power was chosen based on simulation results indicating that this level would be well below the predicted circuit 1-dB input compression point of approximately -3 dBm. Additionally, the setting of the variable attenuator for -30 dB allowed enough increase adjustment in the level to push the circuit into distortion and extract input compression point measurements.

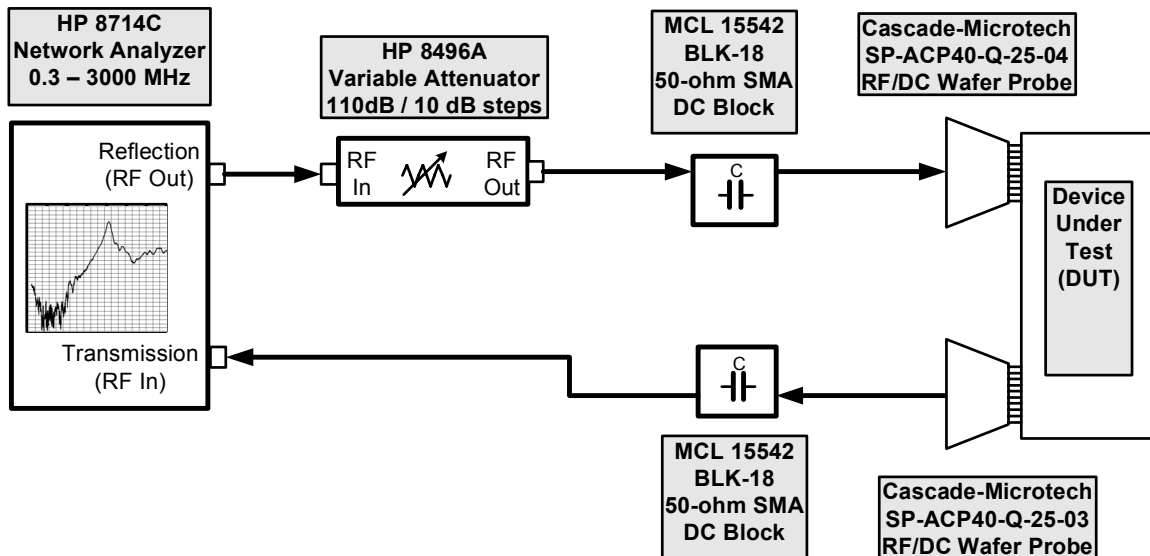


Figure 4.36. Block diagram of RF passband test setup.

The dc blocks shown in Figure 4.36 provide dc isolation of bias levels that are present at the input and output of the DUT while providing a low-impedance path for the RF energy between the network analyzer and the wafer probes.

Prior to testing the passband response of the RF filter, the measurement setup was calibrated by connecting the wafer probes to low-loss ‘thru’ lines on an impedance standard substrate provided by Cascade-Microtech and designed specifically for the dimensions of the probes used in the test setup. This normalization of the signal path effectively removes losses and frequency-dependent characteristics of the components and cables connected for routing the RF signal between the network analyzer and DUT, including the RF wafer probes.

The filter passband response tuned for the maximum achievable quality factor of 31 is shown in Figure 4.37. Also shown in the figure are simulated passband response measurements performed using ac analysis in the Cadence Analog Artist simulator. The simulation data presented shows ideal response plots and response plots with small values of resistance distributed at circuit/probe connection points to emulate non-ideal probe contact with the circuit die pads or other non-specific loss. These loss components were iteratively distributed in the simulated circuit to replicate the losses encountered during experimental measurement. Through this iterative distribution, the placement of these small-valued loss-emulating resistors was validated in part by correlation between simulated and measured filter gain as well as the transconductance value required for specific Q -enhancement factors. Although these losses are mainly distributed at circuit dc power supply connection nodes, other factors such as less than ideal high-frequency component models could have also been contributors to this anomalous circuit behavior.

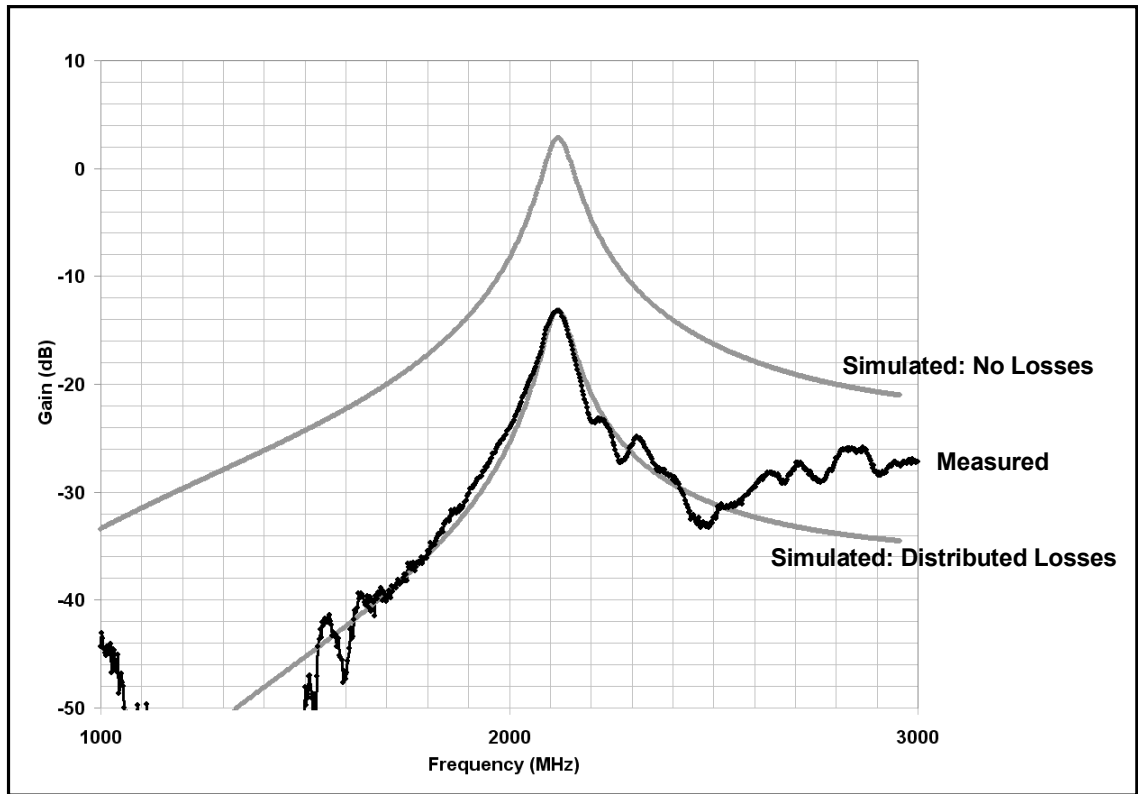


Figure 4.37. Filter passband response at maximum Q : Measurement vs. Simulation.

In Figure 4.37, labels indicate the measured response plot as well as lossy and lossless simulated response plots. The measured gain of -13.1 dB at the center frequency of 2.12 GHz is lower than the originally designed filter gain of approximately 5 dB shown in the lossless simulation plot as a result of the presumed losses outlined previously. However, the measured gain and passband response are comparable to the simulated results when both the simulated and measured circuits are tuned to a quality factor of 31 and the other anomalous losses are taken into account.

Figure 4.37 also illustrates that the filter center frequency is shifted slightly lower than the required f_o of 2.44 GHz specified for the targeted Bluetooth application. The

filter was intentionally designed for a slightly lower center frequency of 2.20 GHz in order to ensure that any deviation of the expected center frequency, possibly attributable to passive component value variation, would not push the center frequency of the passband outside the range limitations of the available measurement instrumentation. Specifically, the center frequency was chosen lower than 2.44 GHz to provide ample margin for measurement with the HP 8714C network analyzer, which is limited to an upper range of 3 GHz. With this criteria established, it is apparent that the measured frequency of 2.12 GHz falls within 4% of the expected 2.20 GHz center frequency.

Also observable in Figure 4.37 is the appearance of resonant peaks and nulls away from the filter center frequency. It was deduced that these unexpected response characteristic were a result of parasitic reactive components distributed throughout the single-ended dc power supply connecting wires, as well as the dc tips on the Cascade RF/dc probes. Experiments were performed with variations induced in the physical spacing of bias supply lines between the dc probes and power supplies with erratic insertion loss behavior observed while monitoring the passband on the network analyzer. These test observations provided experimental verification of the predicted cause for these anomalous out of band test results.

The filter passband response tuned for the maximum achievable quality factor of 31 at the center frequency of 2.12 GHz is again presented in Figure 4.38. This figure presents the data shown in Figure 4.37 with the magnitude and frequency scales decreased to provide greater detail. Despite the out of band resonances discussed previously, the filter displays a relatively symmetrical passband response, comparing well with simulated response characteristics.

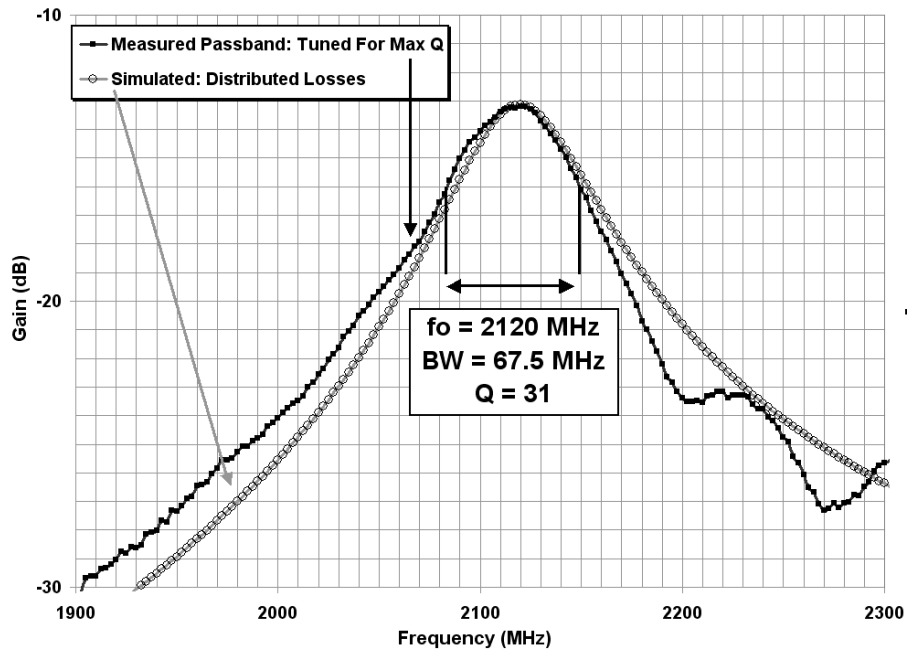


Figure 4.38. Filter passband response at maximum Q : Measurement vs. simulation.

4.7.4 Q -Tuning Response

A log-log plot of the filter passband response for varying values of applied Q -tuning voltages is presented in Figure 4.39. The reference voltage, V_{SI} , indicated in the plot legend is the voltage applied simultaneously to the source of M_I and the gate of M_Q in the circuit diagram presented previously in Figure 4.19. This plot is presented to provide a qualitative demonstration of the experimentally achieved Q adjustment and center frequency response for changing values of the Q -tuning voltage.

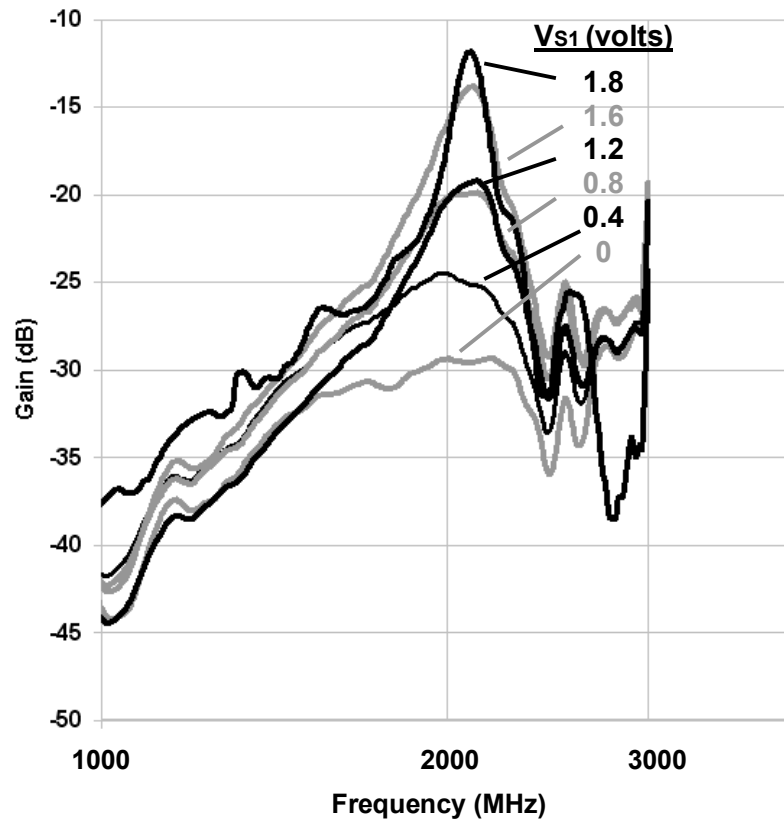


Figure 4.39. Filter passband response for varying Q -tuning voltages

4.7.5 RF Passband Response: Common Grounding

An additional passband test was conducted with the intention of validating the conclusions drawn regarding losses in probe/pad connections. For this experiment, the electrically isolated dc and RF signal ground planes on the Cascade-Microtech ACP40 RF/dc probes were manually connected together at the probe body and in physical proximity of the base of the dc and RF needle connections on the device. This ground jumper connected on the Cascade ACP40 RF/dc probes was accomplished using a solder-affixed short length of 18 AWG wire physically oriented and attached as shown in Figure 4.40.

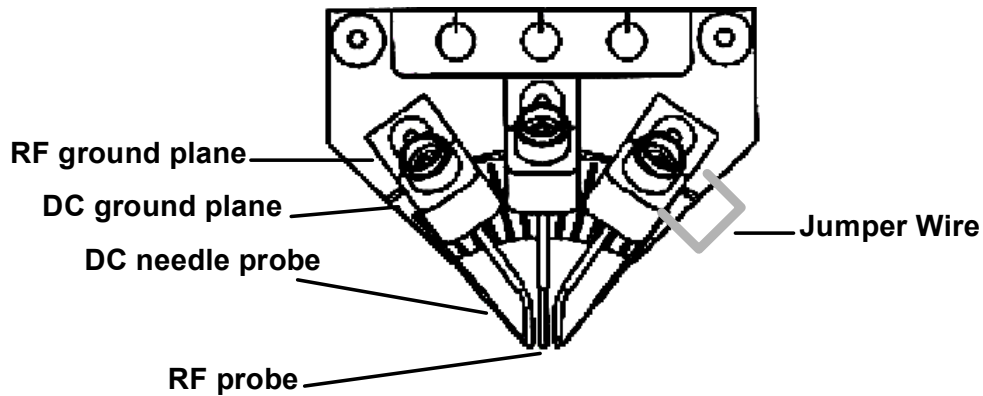


Figure 4.40. Top view of Cascade ACP40 probe with RF and dc grounds connected.

Figure 4.41 presents a comparison of the measured passband response, with the jumpered grounds, and the results predicted by an ac analysis performed using the Analog Artist simulator in the Cadence design tool. In this simulated response test, no distributed losses were utilized. The darker trace in the figure represents the measured response characteristics while the lighter trace represents the simulated filter response. The gain at center frequency is approximately 4 dB for both simulated and measured responses tuned to a quality factor of 30. As mentioned, the gain in this circuit is much closer to the predicted and simulated gain of 4 dB, but the response away from the passband is more erratic than the previous measurements. The conclusion was drawn that the direct dc to RF ground connection and the subsequent introduction of the unpredictable parasitic impedance attributable to the power supplies and the connecting cables was a primary contributor to this phenomenon. Despite the more erratic out-of-band response, the narrow passband at center frequency is essentially symmetric.

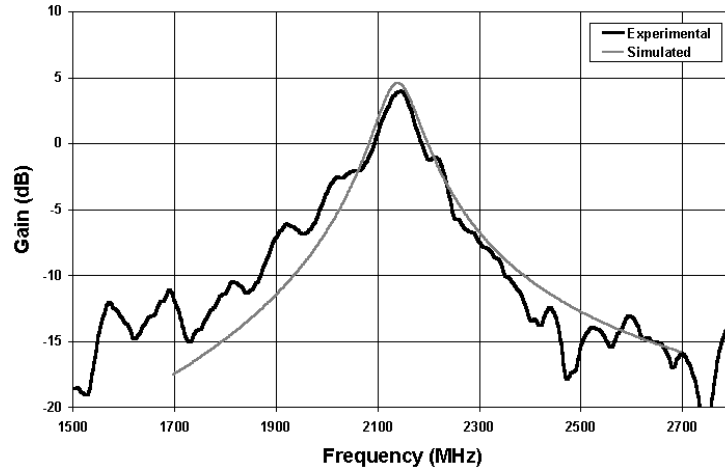


Figure 4.41. Experimental and simulated passband response with gain = 4 dB.

Also note that measurements for input compression and power consumption were performed at this higher gain to provide a conservative measure of these filter characteristics. These measurement results are detailed in Section 4.7.6.

The filter passband response with the jumpered grounds and tuned for the maximum achievable quality factor of 30 is shown in Figure 4.42 with the magnitude and frequency scales decreased to provide greater detail.

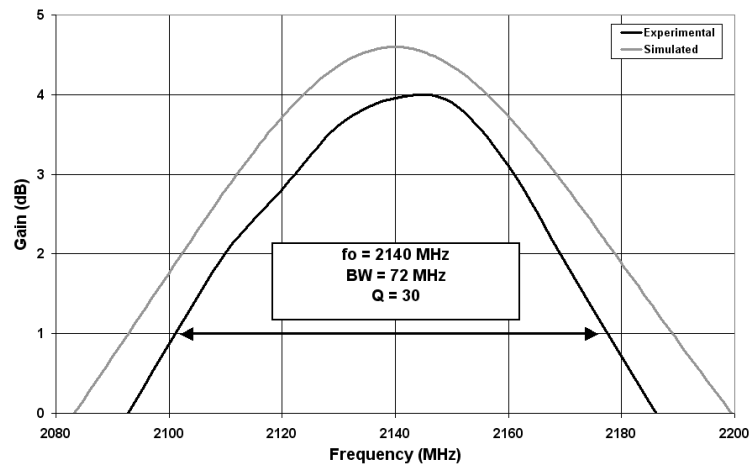


Figure 4.42. Experimental passband response with gain = 4 dB.

In Figure 4.42, some asymmetry is observed in the filter passband, however, the measured passband shape matches reasonably well with simulation results.

The measurements with modified probe grounds presented in this section aid in validating the hypothesis regarding greater than expected dc probe tip losses and other associated ground inconsistencies that created decreased filter gain. However, because of the quality factor adjustment being limited to 30 when values of approximately 100 were expected, other losses in the circuit, perhaps a result of insufficient high-frequency models and less than ideal ground tap placement, were not ruled out as prospective contributors to the discrepancies between simulated and measured circuit characteristics.

4.7.6 Linearity Measurements

The input 1-dB compression point was measured to determine filter linearity. The measured value of $P_{1\text{dB},\text{in}}$ was -3.5 dBm with the filter tuned for the maximum achievable Q of 30 and gain of 4 dB. The results of these measurements are shown in Figure 4.43.

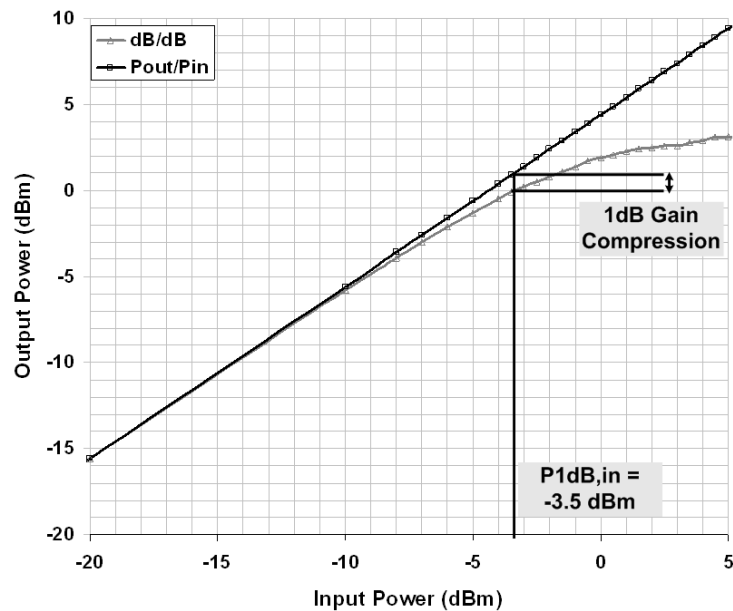


Figure 4.43. $P_{1\text{dB},\text{in}}$ for circuit with measured overall gain of 4 dB.

To validate the assumptions made in Section 4.3.2 regarding the relationship between input compression point and tank voltage swing, the circuit bias levels with a maximum ‘saturation-mode’ signal level were examined. A plot of this expected maximum level is shown in Figure 4.44. In the figure, the threshold voltage, V_T , of M_Q is set for a level of 0.298 volts. This value was extracted from transistor dc operational characteristics for M_Q in simulations using the experimentally utilized bias levels. Also, the drain voltage is $2.2 V_{DC}$ and the gate voltage is shifted down, but only to $1.8 V_{DC}$. These levels were constrained by the greater than expected g_{mq} required to achieve the loss restoration needed for the desired filter quality factor of $Q = 30$.

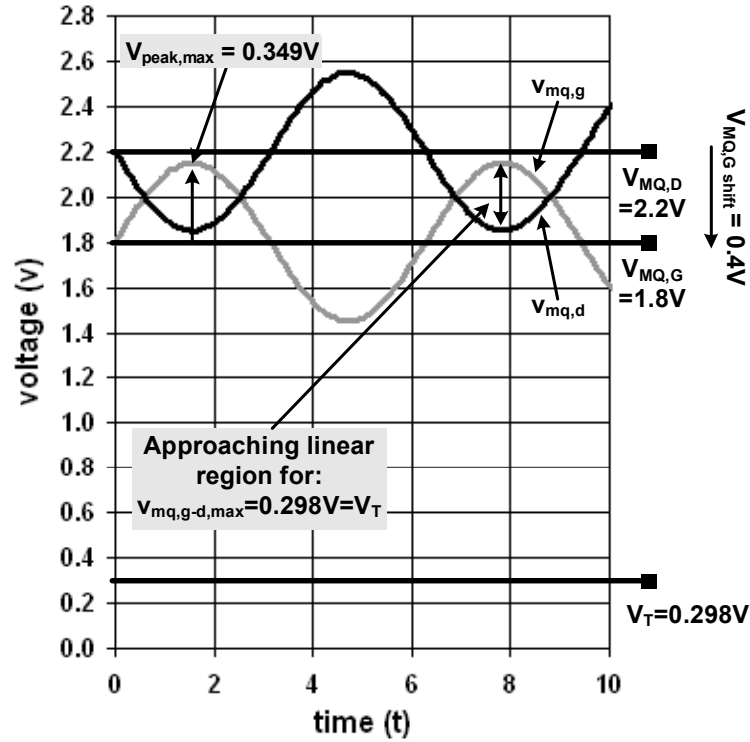


Figure 4.44. Expected maximum signal swing for saturation mode operation.

As discussed previously, the maximum peak signal swing for saturation-mode operation has a theoretical limit of $V_T/2 + V_{G,shift}/2$. This peak voltage, for the utilized bias voltages, is equal to $(0.149 + 0.2) = 0.349$ volts. For analysis with the input and output of the circuit referenced to the standard 50Ω system impedance, the power in the resonator can be computed from

$$P_{dBm} = 10 \log \left(\frac{v_{peak}^2 / 2}{50} \times 1000 \right) dBm. \quad (61)$$

For the expected acceptable peak voltage of 0.349 V, the power level is computed at 0.856 dBm. Now, with the overall gain of the circuit measured at 4 dB, the gain from M_I gate to drain, $G_{M1,dg}$, can be calculated using

$$G_{M1,dg} = G_{Total} - G_{Mout,sg} \quad (62)$$

where G_{Total} is the overall gain, 4 dB, and $G_{Mout,sg}$ is the source follower gain of M_{out} that was discussed previously and calculated at approximately -5.11 dB. For the values presented, the value for $G_{M1,dg}$, is calculated at 9.11 dB. If the calculated value for the acceptable power in the tank, 0.856 dBm, is now referenced to the input, the circuit input power level that would produce the tank signal swing on the threshold of saturation-to-linear mode transition would be -8.25 dBm. This value is lower than the measured P_{1dB} input point of -3.5 dBm. However as shown in Figure 4.45, at the input power level of -8.25 dBm, the filter *is* beginning to exhibit a measurable gain compression of 0.5 dB. This observation provides a qualitative verification of the previous assumptions regarding maximum acceptable tank voltage deviations, as the filter is entering a non-linear

operational region at these predicted bias and signal levels. For additional clarity, Figure 4.45 presents a magnified version of the compression data shown in Figure 4.43 with the area of the onset of compression indicated.

For comparison and validation of the experimental and simulation results, the input P_{1dB} plot for a *simulated* filter with gain equal to approximately 4 dB is shown in Figure 4.46. As detailed in the figure, the value of P_{1dB} extracted for the simulated circuit is -4.5 dBm.

In conclusion, the comparison of input compression performance for the experimentally measured filter, Figure 4.43, and the simulated filter, Figure 4.46, display reasonable accuracy based on the 1 dB difference in the measurements of these parameters.

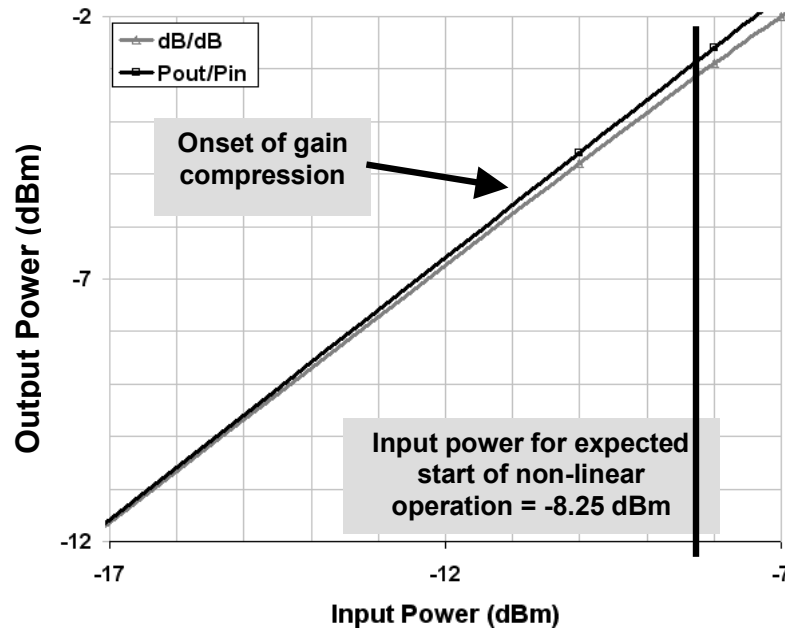


Figure 4.45. Measured $P_{1dB,in}$ for circuit with measured overall gain of 4 dB.

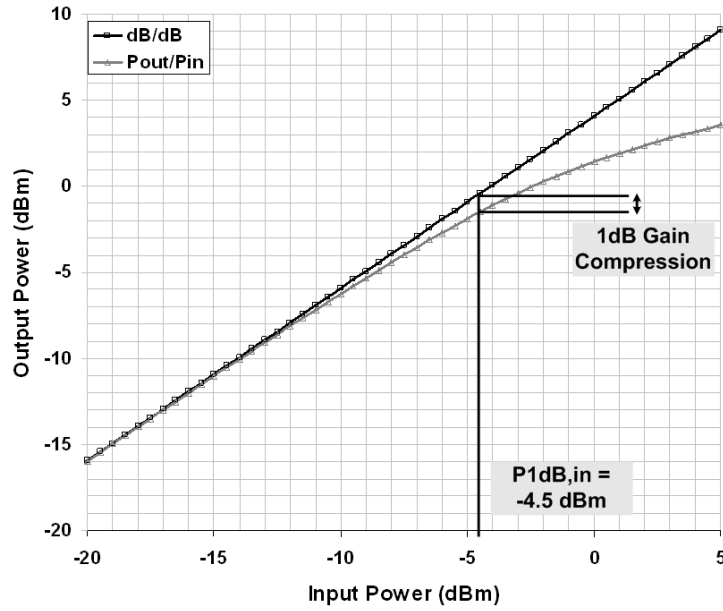


Figure 4.46. Simulated $P_{1\text{dB},\text{in}}$ for circuit with measured overall gain of 4 dB.

4.7.7 Noise Measurements

Filter noise output was measured using a Rhode & Schwarz FSU-8 20 Hz to 8 GHz spectrum analyzer. A block diagram of the noise measurement test setup is shown in Figure 4.47. The dc bias supplies are also connected for this test, but are omitted from this figure for clarity. Note that all noise measurements were performed with the non-jumpered wafer probes (filter gain of -13.1 dB, Section 4.7.3) to provide the most conservative measure of circuit input-referred noise characteristics.

The filter noise was measured by connecting the output of the Q -tuned filter to the input of the spectrum analyzer via a wafer probe, then providing a short at the filter signal input connection. The spectrum analyzer was set for a resolution bandwidth (RBW) of 3 MHz, video bandwidth (VBW) of 10 kHz, sweep time of 20 mS, and input attenuation of 0 dB.

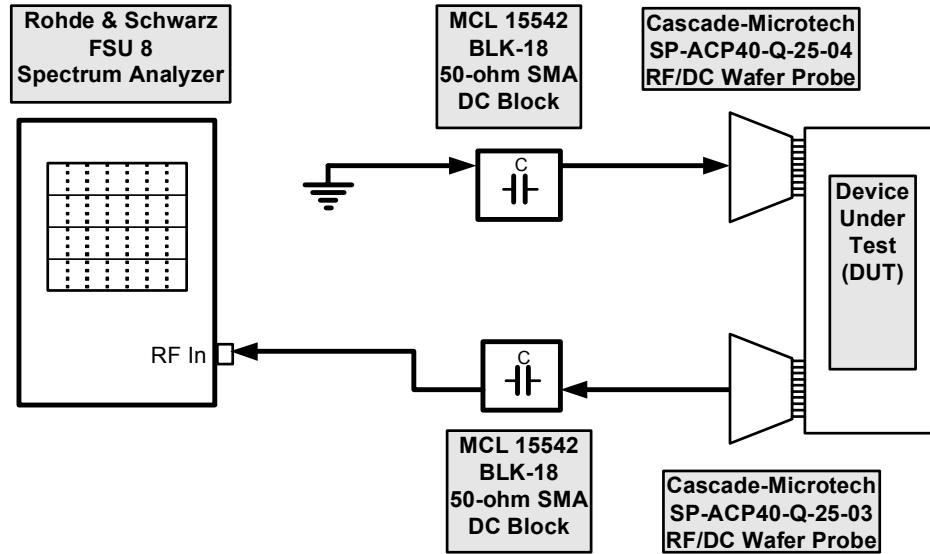


Figure 4.47. Block diagram of noise measurement test setup.

With the filter tuned for the maximum achievable quality factor of 30 and the circuit input grounded, several measurements were executed. These measurements were taken using different frequency spans to capture spot noise power at a 1 Hz bandwidth, as well as integrated noise power at 1 MHz and 84 MHz bandwidths. For the purpose of normalization, power measurements were also performed to determine the intrinsic noise floor of the spectrum analyzer. These analyzer noise floor measurements were required for the Rohde & Schwarz FSU-8 in order to facilitate normalization of the instrument [68], permitting corrected and accurate filter noise power values.

A linear magnitude plot of the spectrum analyzer output for extraction of the filter spot noise voltage at $f_o = 2.12$ GHz is presented in Figure 4.48. The spot noise at center frequency was measured at 4.471 nV/sqrt(Hz).

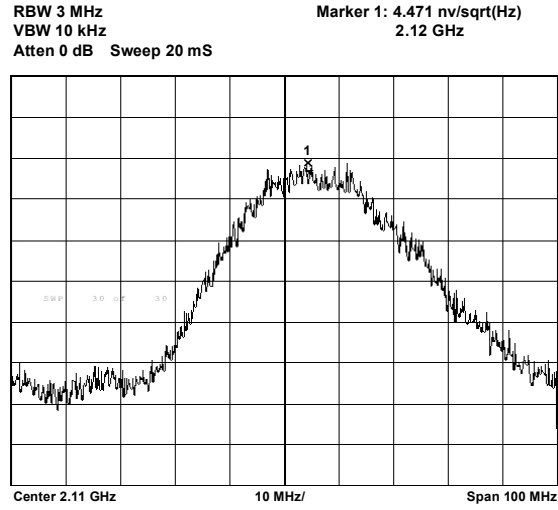


Figure 4.48. Filter spot noise voltage: 1 Hz bandwidth.

Utilizing the 1 Hz bandwidth spot noise voltage measurement, spot noise power is given by

$$P = 10 \log \left[\left(\frac{v^2}{50} \right) \times 1000 \right] \text{ dBm} \quad (63)$$

where v is the voltage reading from the spectrum analyzer in volts/sqrt(Hz). This value is then adjusted by the filter gain, measured just prior to the noise reading for maximum accuracy, to calculate an input-referred noise power value. Given the filter gain of -13.1 dB, the non-normalized input spot noise power was calculated at -140.9 dBm/Hz.

A logarithmic magnitude plot of the spectrum analyzer output for extraction of the filter integrated noise power centered at $f_o=2.12$ GHz with a bandwidth of 1 MHz is presented in Figure 4.49. The integrated power, at this Bluetooth IF bandwidth, was measured at -92.58 dBm. This 1 MHz bandwidth measurement was performed for general comparison and to verify that the measured noise would generally emulate the

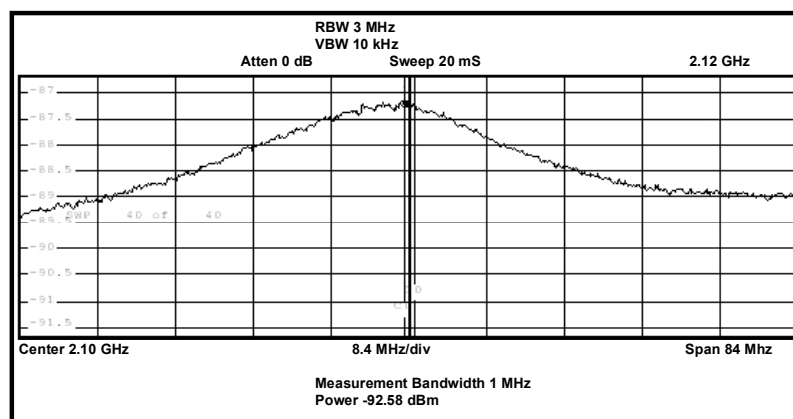


Figure 4.49. Integrated filter output noise power: 1 MHz bandwidth.

expected filter frequency response shape. However, the spot noise power is used for subsequent filter specification calculations and comparison, based on the accuracy achievable when referring spot noise power levels to the circuit input as a function of filter center frequency gain.

A logarithmic magnitude plot of the spectrum analyzer noise floor centered at $f_o = 2.12$ GHz with a measured integrated noise bandwidth of 1 MHz is shown in Figure 4.50.

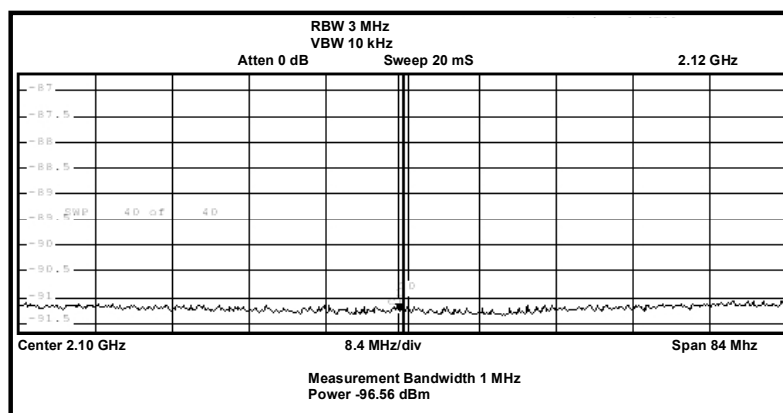


Figure 4.50. Integrated spectrum analyzer noise floor power: 1 MHz bandwidth.

The integrated noise power was measured at -96.56 dBm while the spot noise power was measured at -156.6 dBm. All intrinsic spectrum analyzer noise floor measurements were executed with the input to the instrument grounded.

Now, with the measured input referred filter spot noise power and the spectrum analyzer intrinsic spot noise power, the actual filter input referred noise power normalized to the analyzer noise floor is calculated using

$$P_{noise} = P_{measured} + 10 \log(1 - 10^{\Delta/10}) \text{ dBm} \quad (64)$$

where P_{noise} is the corrected or *actual* filter noise power, $P_{measured}$ is the *uncalibrated* filter noise power, and Δ is the difference in decibels between the measured filter noise power and spectrum analyzer noise floor. For example, the 2.62 dB difference in the power readings for filter output noise power and analyzer noise power measured for this circuit results in a correction of -3.44 dB to the actual filter noise power, giving an accurate filter input referred spot noise power of -144.34 dBm/Hz.

For comparison, the noise performance of the simulated circuit was also extracted using analysis tools provided in Cadence. A linear magnitude plot of the simulated input and output noise over a 1 GHz bandwidth is presented in Figure 4.51. The input referred simulated spot noise at center frequency was measured at approximately 42nV/sqrt(Hz), or -134.52 dBm/Hz spot noise power.

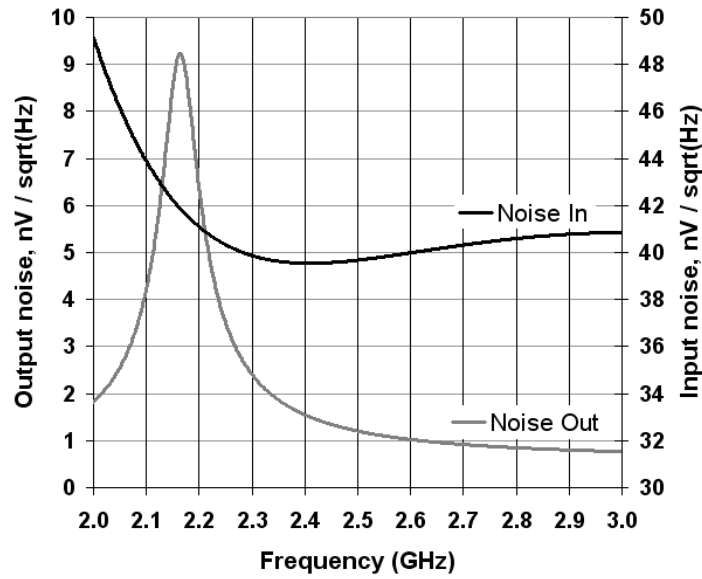


Figure 4.51. Simulated output and input referred filter noise.

Table 4.4 summarizes the experimentally measured noise along with filter noise characteristics extracted from circuit simulations. The results in the table show input and output spot noise as well as calculated integrated input noise values over the IF filter bandwidth of 1 MHz and the second-order noise bandwidth of the entire filter passband, which is equal to the filter bandwidth of 84 MHz multiplied by a factor of $\pi/2$. In Table 4.4, Reference 1 is the experimentally measured and normalized filter noise while Reference 2 represents the simulated noise of the filter implementations discussed in this section that incorporate distributed losses. Reference 3 provides simulated noise values for an identical filter without the additional distributed losses, and is presented to demonstrate the prospective characteristics of the filter under ideal test or circuit implementation conditions. Reference 3 is only presented for completeness, comparison to the other two cases, and as a measure of prospective performance.

Table 4.4. Filter noise: Measurement and simulation.

Ref	Noise Data Source	Output Noise	Input Referred Noise				Filter Gain (dB)
		Spot Noise (V/sqrt(Hz))	Spot Noise (V/sqrt(Hz))	Spot Noise (dBm)	Integrated Noise, 1 MHz BW (dBm)	Integrated Noise, 132 MHz BW (dBm)	
1	Measured	4.471 nV	20.16 nV	-144.3	-84.28	-63.08	-13.1
2	Simulated	9.236 nV	41.88 nV	-134.6	-74.55	-53.31	-13.1
3	Simulated	5.317 nV	4.243 nV	-154.4	-94.43	-73.18	5.0

The measurement data from Reference 1 is used to characterize the filter for subsequent dynamic range and comparison to other similar RF filter work. The results in Table 4.4 show that the experimentally measured noise, at the Bluetooth IF bandwidth of 1 MHz, is -84.28 dBm. This exceeds the Bluetooth sensitivity specification of -70 dBm by over 14 dB, but breaks specification by 6.7 dB when compared to the required Bluetooth noise figure 23 dB. Also, the results show that the experimentally measured noise power is approximately 10 dB lower than simulated values. Although this difference might seem counter intuitive, recall that the simulated circuit uses hypothetical distributed losses placed in the circuit to mimic measurement setup losses. As discussed earlier in this work, the values selected for these loss components were estimated and the placement of these components was chosen, in part, based on circuit nodes with presumed contact losses, i.e. probe/pad connections. Additionally, the noise power differences might be partly attributable to non-ideal noise characterization for the BSIM3v3 active device models used in the simulation. One final explanation might lie in the noise inducing resistors used to model losses for the inductors in the Cadence

simulation. These component values were extracted from ASITIC simulations and imported into Cadence and contribute significantly to the overall circuit noise.

For reference, Table 4.5 provides a list of the circuit components that are significant contributors to the overall noise of the circuit. Components that account for 98.5% of the overall noise are shown along with the percentage of noise power contributed by each component. Note that the component R_{losses} is a summation of multiple small-valued resistors (1-4 Ω) that were distributed at relevant points in the circuit to emulate expected and experimentally observed losses attributable to non-ideal wafer probe to circuit pad contacts. Also, the noise contributions of R_S , R_D , and R_{degen} capture the intrinsic resistance of their associated inductors along with trace resistance connecting these inductors to M_I and M_Q . As mentioned, these components contribute a sizeable percentage to the overall circuit noise. Refer to the detailed circuit schematic presented in Figure 4.19 for the locations and values of these and other components listed in the table. Additionally, and as might be reasonably expected, the loss restoration component, M_Q , is the primary source of noise in the circuit.

Table 4.5. Filter noise: Contributing components.

Component	Noise Contribution (%)
M_Q	48.8
R_S	17.6
R_{degen}	8.3
R_D	3.4
R_G	2.3
R_{losses}	18.1

4.7.8 Stability

In order to verify correct circuit operation upon initial start-up or application of the dc bias supplies, circuit stability was investigated. The stability of the filter was experimentally tested by stepped application of the dc power supplies for the filter tuned to the maximum achievable quality factor of thirty. The output of the filter was monitored on the network analyzer, as well as the spectrum analyzer, as each supply was successively cycled on and off. In addition to the successive application of bias voltages, all supplies were cycled on and off simultaneously. Filter stability was verified when the tuned filter output decayed and then reappeared with no change in response characteristics and no observable additional power in or out of band during the power supply cycling. This method of experimental verification was performed as opposed to transient analysis, as time-domain measurements at the filter center frequency would be impractical with the utilized measurement equipment. Although no quantitative results could be extracted from this test method, the verification of circuit stability was confirmed through this exercise, which emulated realistic conditions for the circuit functioning in an actual operational environment. Also note that the simulated circuit, with and without additional distributed losses, was tested and verified for stable operation following the procedure outlined in Section 4.6.2.

4.7.9 Dynamic Range

Filter dynamic range is defined for total filter bandwidth as well as operational bandwidth. For a second-order bandpass circuit, the *total* filter bandwidth is equal to the frequency span between the 3-dB attenuation points above and below the filter center frequency multiplied by a factor of $\pi/2$. The *operational* or IF bandwidth is determined

by the channel bandwidth utilized for a specific filter application. For the Bluetooth wireless standard, which is the specific operational target for the current filter, the IF bandwidth is 1 MHz.

Table 4.6 summarizes the noise power, input compression point, P_{1dB} , and dynamic range for the measurement of the fabricated circuit along with the data extracted from simulations. In the table, Ref. 1 presents measured filter characteristics, Ref. 2 presents simulation measurements incorporating distributed losses, while Ref. 3 represents an identical filter without additional losses.

As the experimental data illustrates, and despite the additional losses inherent to the test setup and circuit anomalies discussed previously, the Q -enhanced transformer-coupled RF filter meets the majority of the noise, linearity, and dynamic range specifications for the Bluetooth standard. For reference, the associated Bluetooth specifications are outlined in Table 4.7. In Table 4.7, ‘Sensitivity’ is associated with the filter ‘Input-Referred Noise Power’ in Table 4.6, while ‘Maximum Input Signal Level’ is associated with filter input compression, or ‘ P_{1dB} ’.

Table 4.6. Filter dynamic range: Measurement and simulation.

Ref.	Dynamic Range Data Source	Input Referred Noise Power (dBm)			P_{1dB} (dBm)	Dynamic Range (dB)		
		Spot Noise	Integrated Noise, 1 MHz BW	Integrated Noise, 132 MHz BW		Spot	1 MHz BW	132 MHz BW
1	Measured	-144.3	-84.28	-63.08	-3.5	140.8	80.78	59.58
2	Simulated	-134.6	-74.55	-53.31	-4.5	130.1	70.05	48.81
3	Simulated	-154.4	-94.43	-73.18	-7.5	146.9	86.93	65.68

Table 4.7. Bluetooth wireless standard operational specifications.

Sensitivity (dBm)	Maximum Input Signal Level (dBm)	Dynamic Range (dB)
-70	-20	50

4.7.10 Transconductance vs. Q

The filter quality factor as a function of transconductance provided by the loss restoration transistor, M_Q , is presented in Figure 4.52. Notice that several discrete points, shown in the darker trace of the figure, were extracted from measured bias current values and plotted for filter quality factor tuning between approximately 2 and 31. The lighter trace in the figure is a calculated trendline for the measured data. The discrete values for transconductance were extracted from plots of associated experimentally measured bias current values detailed in Section 4.7.2. These plots of M_Q drain current and transconductance were used to ‘look up’ transconductance values associated with current values measured while adjusting circuit quality factor. It can also be observed from Figure 4.52 that the relationship between the required transconductance of M_Q and the subsequent loss restoration generally possesses the expected exponential characteristics previously discussed in Section 4.3.4.

4.7.11 Power Consumption vs. Q

For reference, the filter quality factor as a function of power dissipated in the loss restoration transistor, M_Q , is presented in Figure 4.53. Notice that several discrete points, shown in the darker trace of the figure, were extracted from measured bias current values and plotted for filter quality factor tuning between approximately 2 and 31. The lighter trace in the figure is a mathematically calculated trendline for the measured data.

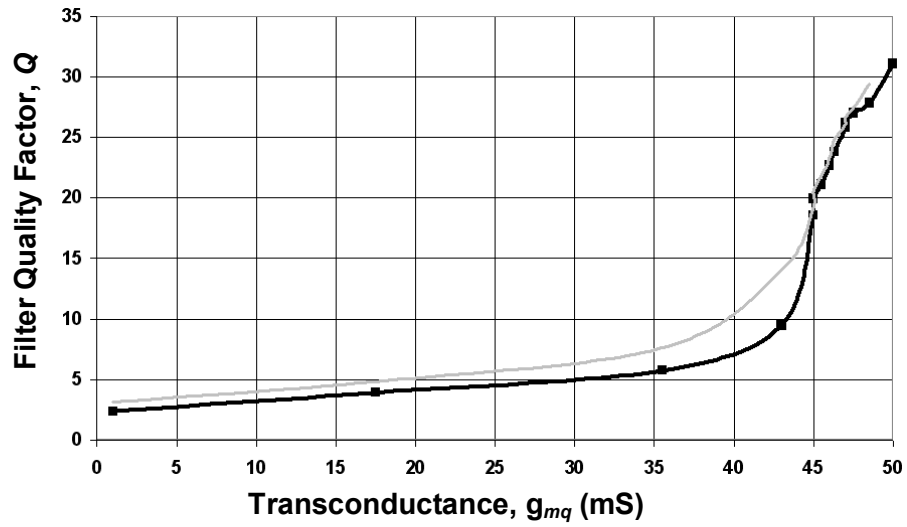


Figure 4.52. Filter quality factor as a function of M_Q transconductance.

In Figure 4.53, the discrete values for power dissipation were calculated from the dc voltage and current values measured and obtained from the power supply connected to the drain of M_Q via the V_{DD} connection in the circuit.

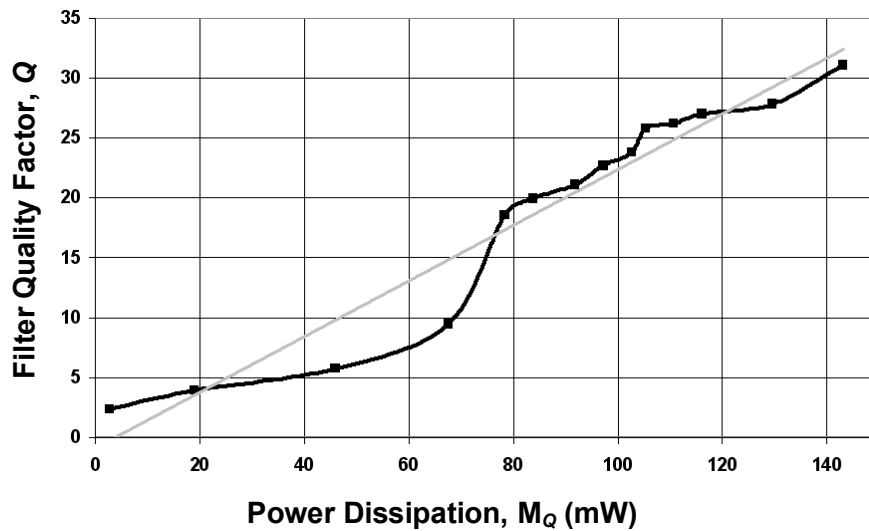


Figure 4.53. Filter quality factor as a function of M_Q power dissipation.

4.7.12 Comparison With Recent Research

Table 4.8 presents a figure-of-merit (FOM) comparison of recently published Q -enhanced LC filter designs with the transformer-coupled Q -enhanced filter detailed in this work. This figure-of-merit comparison is based on recent research and comparison [69] and is derived from several key circuit operating parameters including dynamic range (DR), power consumption or dissipation (PD), and linearity ($P_{1\text{dB},\text{in}}$). Table 4.9 provides details of the references indicated in Table 4.8, and is duplicated from the ‘Reference’ section of this document for convenience.

Referring to Table 4.8, the figure-of-merit for the circuit presented in this work compares favorably with other recent research results shown in the table, lagging only two other designs. The FOM is particularly competitive when compared to other filters operating at operational frequency ranges in the gigahertz spectrum. Also, it should be noted that [69] incorporates a silicon-on-insulator (SOI) process that uses a non-standard insulating sapphire bulk. This SOI process possesses greatly reduced substrate losses and provides high- Q integrated inductors that require significantly decreased Q -enhancement, facilitating inherent advantages in regards to the final FOM.

Finally, the specifications outlined in the FOM comparison table show that a principal design goal outlined for the transformer-coupled circuit in this work is achieved. As previously discussed, a specific target of the Q -enhanced transformer-coupled RF filter examined in this research effort was the improvement of the input compression point via the bias shifted characteristics of the circuit. This prospective improvement is verified in the achievement of the optimum $P_{1\text{dB}}$ rating when compared to operational specifications reported for other recently investigated LC filter designs.

Table 4.8. Figure-of-merit comparison with other recent Q -enhanced LC filter designs.

Ref	Year	Type	f_0 (MHz)	BW (MHz)	Gain (dB)	Q (f_0 /BW)	$P_{1dB,in}$ (dBm)	Input noise 1Hz BW, (dBm)	DR, 1Hz BW (dB)	DR, Filter BW (dB)	PD (mW)	FOM
This work	2005	CMOS LC	2120	69	5	31	-3.5	-144.3	140.8	59.6	143.1	119.2
[69]	2003	CMOS LC	900	20	11	45	-5.5	-142.0	136.5	61.5	39.0	120.6
[67]	2003	CMOS LC	2190	55	-5	40	-30.0	-147.0	117.0	37.6	5.2	109.8
[33]	1998	CMOS LC	840	18	0	47	-18.0	-153.0	135.0	60.5	207.9	111.8
[70]	1996	CMOS LC	200	2	-5	100	-12.0	-119.0	107.0	42.0	8.8	97.5
[71]	1996	CMOS LC	1800	51	7	35	-12.0	-131.0	119.0	40.0	24.4	105.1
[72]	1998	CMOS LC	1000	25	7	40	-10.7	-130.0	119.3	43.4	68.0	101.0
[21]	2002	CMOS LC	2140	60	0	36	-13.4	-155.0	141.6	61.9	7.0	133.1

Table 4.9. Figure of merit references.

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[67]	F. Dülger, E. Sánchez-Sinencio, and J. Silva-Martínez, "A 1.3-V 5-mW Fully Integrated Tunable Bandpass Filter at 2.1 GHz in 0.35 μ m CMOS," <i>IEEE J. Solid-State Circuits</i> , vol. 38, pp. 918928, June 2003.
[33]	W.B. Kuhn, N.K. Yanduru and A. S. Wyszynski, "Q-Enhanced LC bandpass filters for integrated wireless applications," <i>IEEE Transactions on Microwave Theory and Techniques</i> , vol. 46, no. 12, pp. 2577 – 2586, December 1998.
[70]	W. B. Kuhn, F. W. Stephenson, and A. Elshabini-Riad, "A 200 MHz CMOS Q -enhanced LC bandpass filter," <i>IEEE J. Solid-State Circuits</i> , vol. 31, pp. 1112–1122, Aug. 1996.
[71]	S. Pipolos, Y. P. Tsvividis, J. Fenk, and Y. Papananos, "A Si 1.8 GHz RLC filter with tunable center frequency and quality factor," <i>IEEE J. Solid-State Circuits</i> , vol. 31, pp. 1517–1525, Oct. 1996.
[72]	W. Gao and W. M. Snelgrove, "A linear integrated LC bandpass filter with Q -enhancement," <i>IEEE Trans. Circuits Syst. II</i> , vol. 45, pp. 645–639, May 1998.
[21]	T. Soorapanth and S. S. Wong, "A 0-dB IL 2140 \pm 30 MHz bandpass filter utilizing Q -enhanced spiral inductors in standard CMOS," <i>IEEE J. Solid-State Circuits</i> , vol. 37, pp. 579–586, May 2002.

CHAPTER 5

CONCLUSION AND DISCUSSION

This chapter completes the documentation of the current research effort with a summary of circuit operational results as well as an outline of the contributions of this work to Q -enhanced RF bandpass filter research. Additionally, an outline of prospective future effort that might be expended to build on and further develop the accomplishments of this work is presented.

5.1 Summary of Operational Results

The experimental results of this research effort proved the feasibility of the concept incorporating transformer-coupled Q -enhancement as a novel method for realizing loss restoration in RF and microwave integrated receiver front-end bandpass filters, specifically for filters utilizing lossy on-chip inductors in a standard digital CMOS process. Although some of the test results suffered from unexpected parasitic effects due in part to test equipment and circuit/instrumentation interface inconsistencies, the outcome of the research effort proved that this unique concept for loss restoration in RF circuits is viable, and these results may serve to motivate prospective future development of the concepts and circuit topologies presented in this work. An outline of the experimentally measured operational characteristics for the transformer-coupled Q -enhanced RF bandpass filter is presented below:

- Filter center frequency: 2.12 GHz.
- Quality factor tuning range: 2-30.
- Maximum filter gain: 4 dB.
- Input P_{1dB} : -3.5 dBm.
- Input referred noise power, 1Hz bandwidth: -144.3 dBm.
 - Dynamic range, 1Hz bandwidth: 140.8 dB.
 - Noise figure: 29.7 dB.
- Input referred noise power, Bluetooth IF bandwidth (1 MHz): -84.3 dBm.
 - Dynamic range, Bluetooth IF bandwidth (1 MHz): 80.8 dB.
- Input referred noise power, filter noise bandwidth (132 MHz): -63.1 dBm.
 - Dynamic range, filter noise bandwidth (132 MHz): 59.6 dB.
- Power dissipation at maximum Q : 143.1 mW.

As the measured experimental data illustrates, and despite the additional unforeseen losses inhibiting maximum filter quality factor tuning, the operation of the Q -enhanced transformer-coupled RF filter was validated and the performance compared well with other current research in the area of RF filters incorporating dynamic loss restoration. Additionally, the target goal of linearity improvement facilitated by the intrinsic bias level shifting of the circuit was validated as the transformer-coupled RF filter exhibited superior P_{1dB} performance when compared to other currently investigated RF integrated LC bandpass filters.

5.2 Contributions to Integrated Q -Enhanced LC Filter Research

The contributions of this work to the overall knowledge base regarding implementation of integrated RF Q -enhanced filters in standard digital CMOS processes are outlined below:

- General proof of concept for the utilization of magnetically coupled loss restoration for RF filters and LNAs.
- Implementation of unique method for using feedback via drain to source transformer coupling to enable single transistor magnetically coupled Q -enhancement for an integrated RF filter / LNA. Design flexibility in adjusting bias levels for Q -enhancement circuit components is part of this contribution. This unique and additional ‘degree of freedom’ for filter design and tuning is not achievable with the commonly utilized cross-coupled transconductor Q -enhancement topology.
- Experimental validation of predicted filter improvement for input compression point and linearity.
- Demonstration of novel circuit topology that promotes possible development of magnetically coupled circuits for active integrated Q -enhanced baluns or single-to-differential converters.

5.3 Prospective Continuation of Research

An outline of the prospective continuation of this research work for improved or alternate transformer-coupled Q -enhanced RF bandpass filter circuits is presented below:

- Experimental extraction of accurate device models at RF and microwave frequencies for required on-chip components. In particular, the transformer inductance and coupling coefficient values and transistor behavior at high frequencies would assist in selection of components to achieve experimental results that closely emulate expected circuit behavior derived from simulations.
- Implementation and addition of integrated manual and automatic frequency-tuning circuits using on-chip varactors to facilitate filter center frequency adjustment.
- Packaging of the chip to facilitate more efficient power supply decoupling for the single-ended design.
- Development of a more sophisticated input matching circuit. This prospective matching circuit could be designed for simultaneous gain and noise figure optimization.
- Design and development of a differential version of the single-ended circuit presented in this work.
- Design and implementation of alternate circuits using the concept of transformer-coupled Q -enhancement could be investigated including variations in the current topology as well as implementation of an image reject ‘notch’ filter.
- Investigation and methodical isolation and correction of the measurement inconsistencies caused by the non-ideal characteristics of the RF test setup.

APPENDIX A

DESIGN PROCEDURE: Q -ENHANCED LC FILTER

For reference, a prospective design procedure utilizing the transformer-coupled Q -enhanced RF filter that has been presented in this work is introduced. This design procedure takes advantage of the bias level shifting facilitated by the transformer-coupled filter, and is based around quiescent points that facilitate the maximum resonator tank signal swing. The input variables that set the constraints for this design procedure are supply voltage, transistor threshold voltage (V_T), filter center frequency, level of Q -enhancement needed to facilitate required bandwidth, selected integrated inductance value, and intrinsic quality factor of inductors available for the utilized IC process. Additionally, the maximum required input signal that the filter is expected to process is considered. The output products of the procedure include required tank bias levels and maximum allowable filter gain as well as values of transconductance required for the input and Q -enhancement transistors. This fundamental procedure, based on the analytical evaluation of the transformer-coupled circuit provided in Section 4.3.2, does not address all design issues, i.e. input matching or subsequent stage loading, and should not be considered a completely rigorous design method. However, this procedure *does* provide a methodical approach to achieve a fundamental preliminary design from which a

more refined circuit topology might be based. The fundamental design procedure is outlined below:

1.) Based on the determination of supply voltage (V_{DD}), and the threshold voltage (V_T) of the loss-restoration transistor (M_Q), and assuming a bias value of V_{DD} at M_Q drain, the bias voltage at M_Q gate that allows the maximum signal swing at the resonant tank node is determined from

$$V_{MQ,G} = V_T + \frac{V_{DD}}{3}. \quad (65)$$

2.) The maximum allowable peak voltage swing in the resonant tank can be shown to have a fundamental limit based on the value for V_{DD} ., and is given by

$$V_{pk,Tank} = V_{MQ,G} - V_T = \frac{V_{DD}}{3}. \quad (66)$$

3.) Given the maximum input power level that the circuit must process, $P_{in,dBm}$, the maximum input peak voltage swing can be calculated from

$$V_{pk,in} = \sqrt{\frac{10^{\frac{P_{in,dBm}}{10}}}{10}}. \quad (67)$$

4.) Now, using the calculated values for maximum peak input voltage and the maximum allowable tank voltage swing, the maximum gain of the circuit can be calculated by

$$G_{\max} (dB) = 20 \log \frac{V_{pk,\max}}{V_{pk,in}}. \quad (68)$$

5.) Next, using the values for tank inductance and the intrinsic inductor quality factor (Q_o) for the process utilized in the circuit design, as well as the center frequency and associated quality factor (Q_{enh}) required for the filter bandwidth, the transconductance value for the input transistor, M_I , designed for maximum allowable gain, can be determined from

$$g_{m1} = \frac{V_{pk,\max} / V_{pk,in}}{\omega_o L Q_{enh}}. \quad (69)$$

6.) Finally, the transconductance of M_Q needed to achieve the required loss restoration can be calculated using

$$g_{mQ} = \frac{1}{\omega_o L Q_o} + \frac{1}{\omega_o L Q_{enh}} + 2g_{m1}. \quad (70)$$

These calculated circuit parameters provide a starting point for a design with maximum allowable gain. However, tradeoffs in this particular topology warrant detailed examination to allow for optimization of the circuit for specific applications.

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VITA

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