CMOS RF TRANSMITTER FRONT-END MODULE FOR HIGH-POWER MOBILE APPLICATIONS

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CMOS RF TRANSMITTER FRONT-END MODULE FOR HIGH-POWER MOBILE APPLICATIONS

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LIST OF ABBREVIATIONS

2G	second generation
3G	third generation
4G	fourth generation
ADS	advanced design system
AM-AM	amplitude-amplitude modulation
CG	common gate
CMOS	complementary metal-oxide-silicon
CS	common source
DNW	deep N-well
DUT	device under test
EDGE	enhanced data rates for GSM evolution
FET	field-effect transistors
GaAs	gallium arsenide
GPRS	general packet radio service
GSM	global system for mobile communications
HB	harmonic balance
HBT	hetero-junction bipolar transistors
HP	high power
HPF	high pass filter
IC	integrated circuit

IEEE	institute of electrical and electronics engineers
InGaP	Indium gallium phosphide
IS-95	interim standard 95
ITT	impedance transformation technique
LP	low power
LPF	low pass filter
MEMS	micro-electro-mechanical systems
MN	matching network
MP	medium power
$P_{\_1dB}$	1-dB gain variation point
P_{1dB}	1-dB gain compression point
PA	power amplifier
PAE	power-added-efficiency
PCB	printed circuit board
PHEMT	pseudomorphic high electron mobility transistors
P_{sat}	saturation output power
Q	quality factor
RF	radio frequency
SiGe	silicon germanium
SOI	silicon-on-insulator
SOS	silicon-on-sapphire
SPDT	single-pole-double-throw

VSWR	voltage standing-wave ratio
WCDMA	wideband code division multiple access
WLAN	wireless local area network

SUMMARY

With the explosive growth of the wireless market, the demand for low-cost and highly-integrated radio frequency (RF) transceiver has been increased. Keeping up with this trend, complimentary metal-oxide-semiconductor (CMOS) has been spotlighted by virtue of its superior characteristics. However, there are challenges in achieving this goal, especially designing the transmitter portion. The objective of this research is to demonstrate the feasibility of fully integrated CMOS transmitter module which includes power amplifier (PA) and transmit/receive (T/R) switch by compensating for the intrinsic drawbacks of CMOS technology.

As an effort to overcome the challenges, the high-power handling T/R switches are introduced as the first part of this dissertation. The proposed differential switch topology and feed-forward capacitor helps reducing the voltage stress over the switch devices, enabling a linear power transmission. With the high-power T/R switches, a new transmitter front-end topology – differential PA and T/R switch topology with the multi-section PA output matching network – is also proposed. The multi-stage PA output matching network assists to relieve the voltage stress over the switch device even more, by providing a low switch operating impedance. By analyzing the power performance and efficiency of entire transmitter module, design methodology for the high-power handling and efficient transmitter module is established. Finally, the research in this dissertation provides low-cost, high-power handling, and efficient CMOS RF transmitter module for wireless applications.

CHAPTER 1

INTRODUCTION

1.1. Background

Since the mobile handsets are open to the public in 1990s, the wireless market has experienced an explosive growth and is welcoming the second golden age with the emergence of smartphones recently as indicated in Figure 1. The demand for the mobile terminals has been consistently increasing during the past a few decades, as a result, the cost of the mobile terminals became a main concern for both of manufacturers and consumers. From the perspective of the cost, the most powerful solution in implementing a mobile transceiver integrated circuit (IC) has been CMOS technology, thanks to its low cost and high feasibility of integration [1].

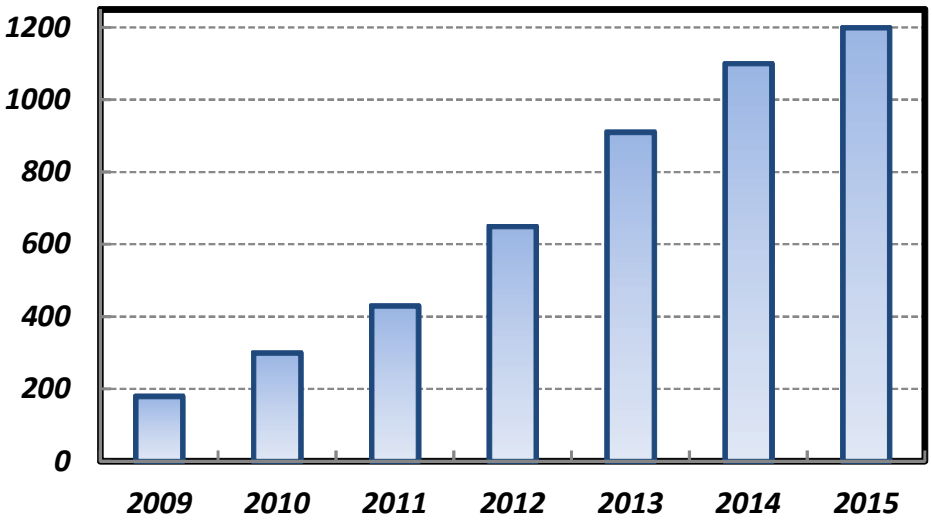


Figure 1. Annual shipment of smartphones (source: NGT Research Series)

As described in Figure 2, most of functional blocks in mobile transceivers, including digital, analog, and RF components are already successfully integrated using CMOS. However, high-power handling components such as PAs and T/R switches are difficult to be put on the same silicon die due to the intrinsic drawbacks of CMOS technology itself. For example, a significant amount of distortions are accompanied when a high-power signal is transmitted because the MOS devices cannot sustain the large voltage swing and generate various nonlinear characteristics. Furthermore, there exist many unwanted signal paths through the parasitic capacitors and a conductive silicon substrate, resulting in poor linearity and efficiency. The low quality factor (Q) of passive and active devices is a main source of signal loss as well. Accordingly, most commercial products are based on compound semiconductor technologies such as gallium arsenide (GaAs) and indium gallium phosphide (InGaP), as shown in Figure 2.

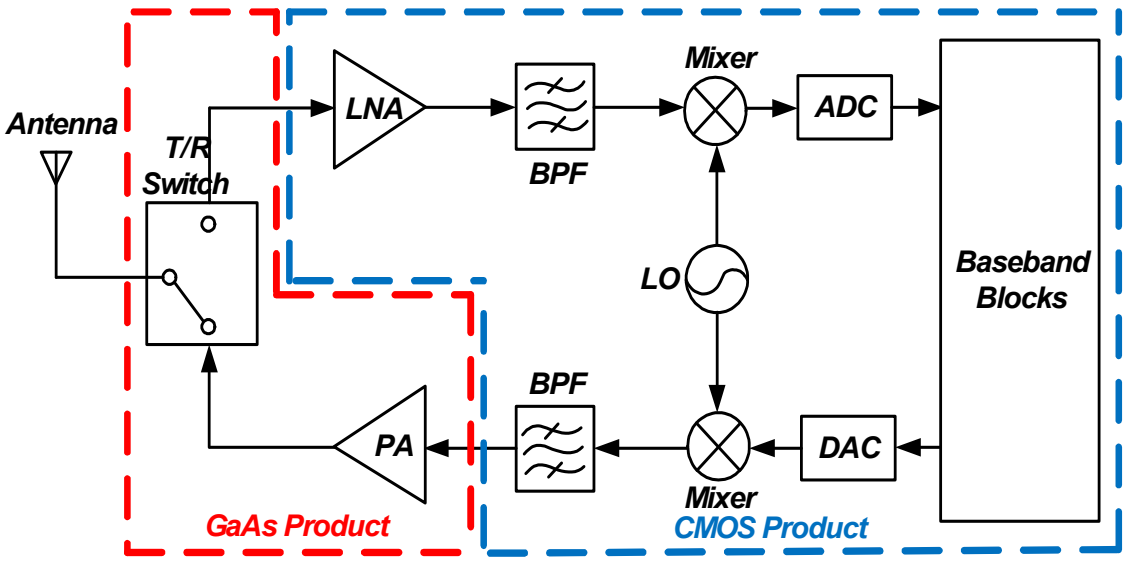


Figure 2. Block diagram of a typical RF transceiver

The challenges for the CMOS transceiver are even more prominent with today's RF transceiver structure, which is demanded to cover the multiple standards. As shown in Figure 3, the number of the PAs is significantly increased, unless the multi-band PAs are not available, and T/R switch is required to satisfy the various kinds of standard specifications at the same time. Furthermore, performance requirements of the up-to-date wireless standards are getting tougher, following the transceiver evolves, as shown in Figure 4. In sum, CMOS technology is facing lots of huge obstacles to meet the key specifications of commercial PA and T/R switch products (high output power, high efficiency, high linearity, and port isolation).

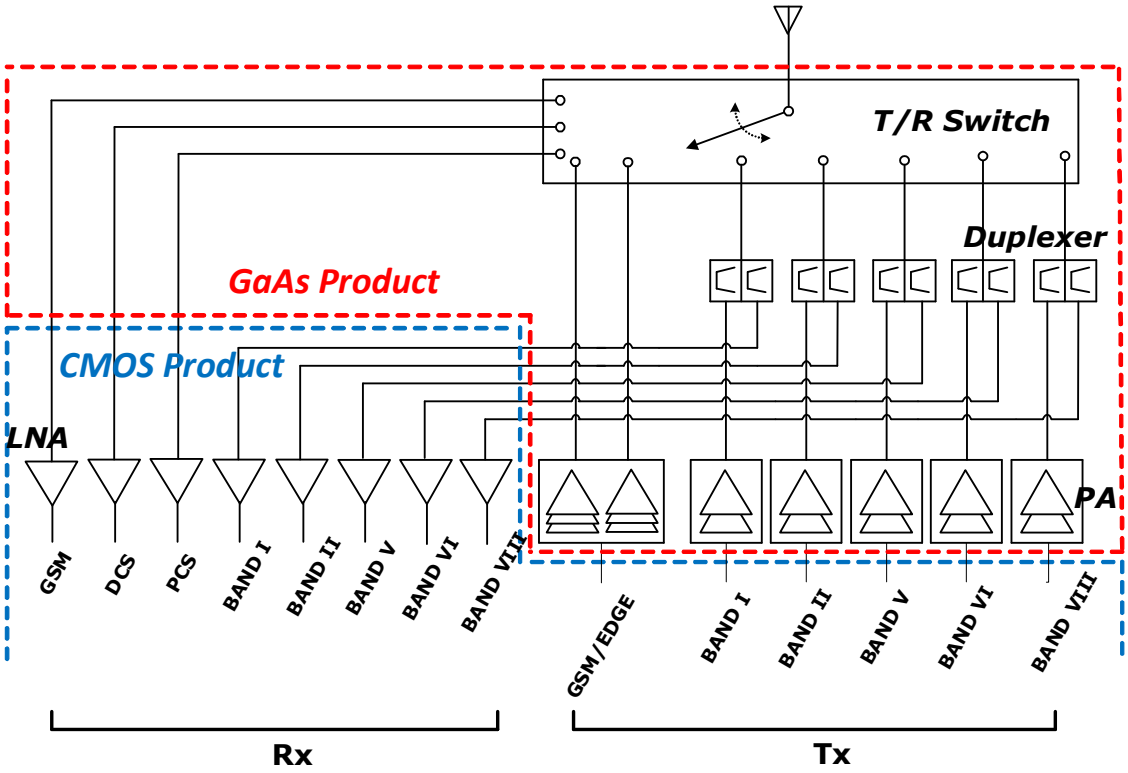


Figure 3. Block diagram of an up-to-date RF transceiver

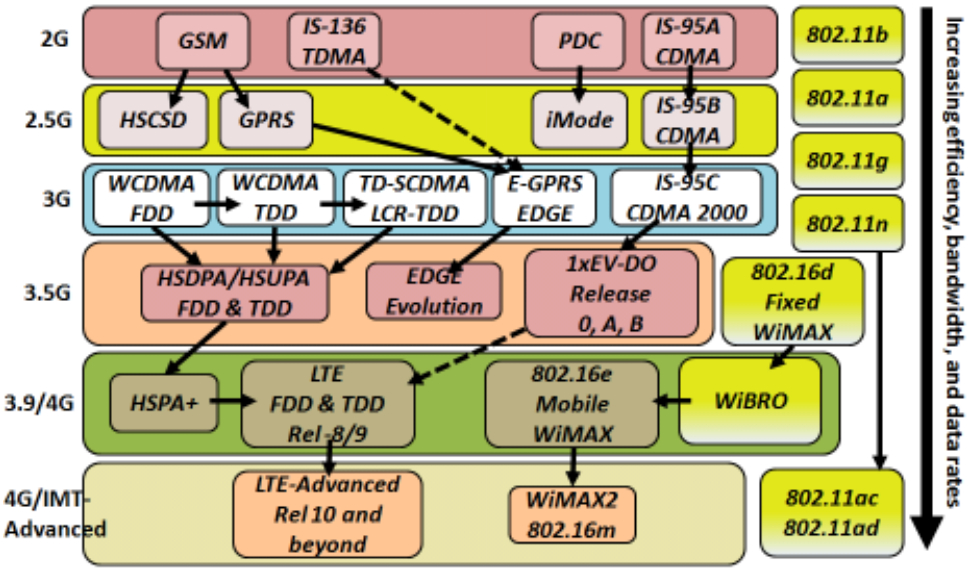


Figure 4. Evolution of wireless communications (source: Agilent Technology)

1.2. Motivation

The front-end module market grows constantly as illustrated in Figure 5, and most of these solutions are implemented by using compound semiconductor technologies such as III-V hetero-junction bipolar transistor (HBT), III-V pseudomorphic high electron mobility transistor (PHEMT), silicon germanium (SiGe) HBT, and Si-MOSFET (silicon-MOS field effect transistor) technologies. However, CMOS transmitter modules keep staying as an attractive issue not only to the research institutions, but also to the industrial world. That is because although the implementation of the fully integrated CMOS transmitter modules is very challenging, the CMOS solutions are worthy to research and implement, considering the recent front-end market trends as mentioned earlier.

Summarizing the motivation in detail regarding the trends, the need for low-cost, multi-functional mobile devices brought two aspects as shown in Figure 6: the system

integration and the performance improvement. To achieve the system integration, silicon-based semiconductor is necessary since all the digital and most of the RF components are already integrated in CMOS. For the performance improvement, on the other hand, low signal loss and high-power handling capability are essential. By combining these two aspects, low-cost and high-performance transmitter front-end module can be achieved.

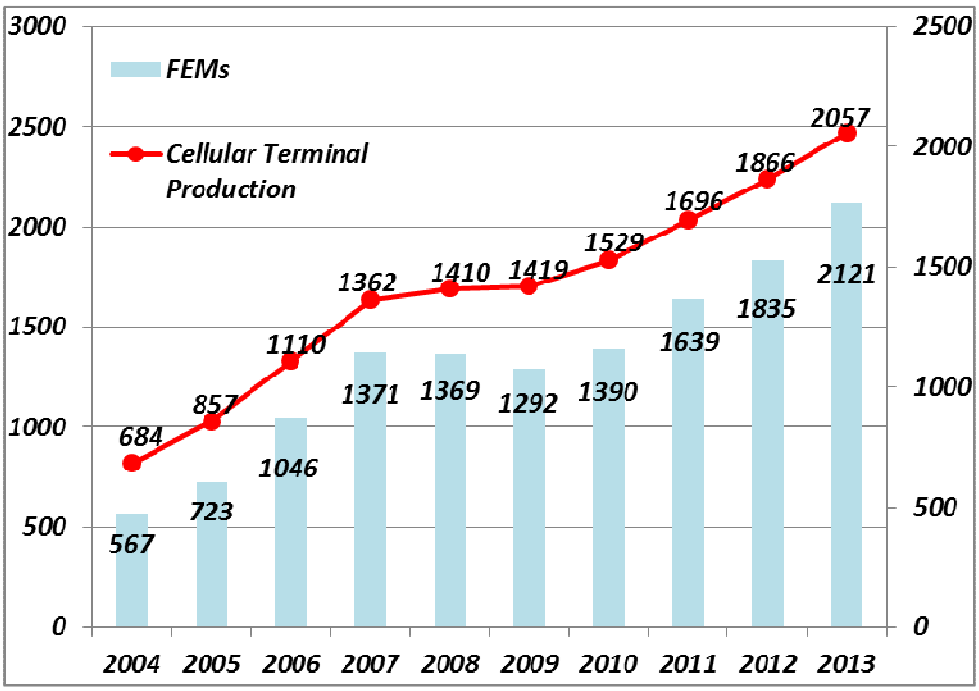


Figure 5. Front-end module market forecast (source: Strategy Analytics 2008)

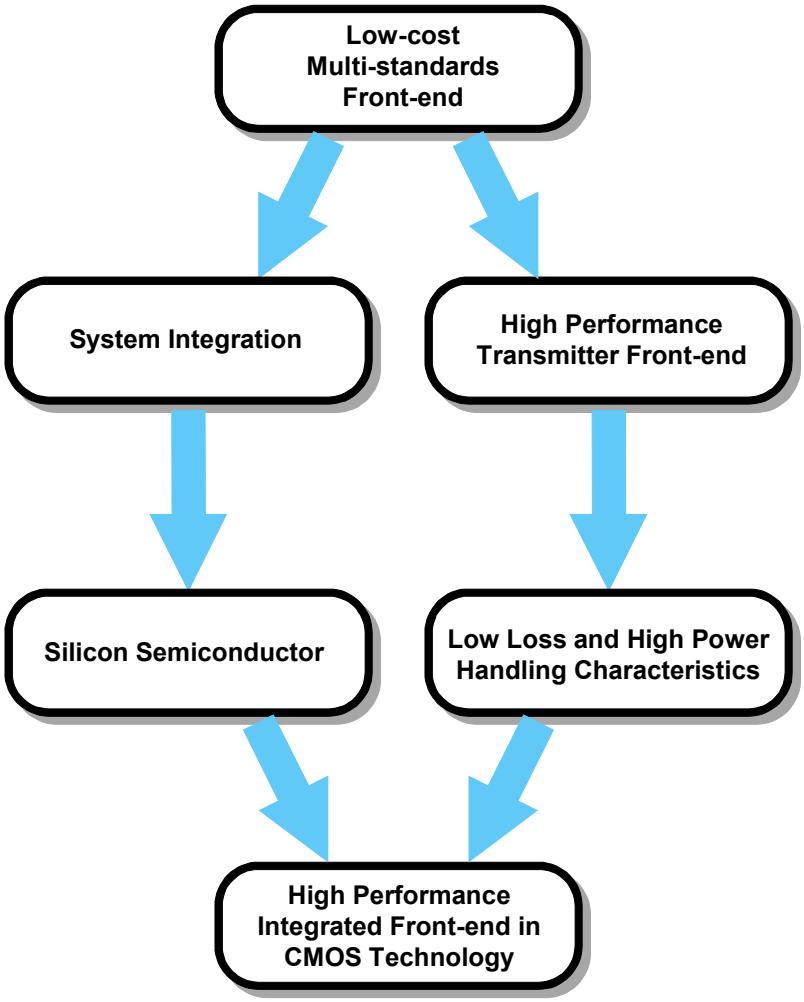


Figure 6. Research motivation and approach

1.3. Organization of the Thesis

Based on the background and motivation, the objective of this research is to exploit standard CMOS technologies for developing RF transmitter front-end modules that can overcome various challenges which will be discussed in detail soon.

Chapter 1 includes an introduction to the market and trends, and the motivation for this work. Chapter 2 contains an explanation of the basic concept and background

knowledge on RF PAs and T/R switches. The measurement methods of those blocks are also included in the Chapter 2. Chapter 3 deals with the challenges and techniques in designing the CMOS PAs and T/R switches and design methodology to overcome the drawbacks. Chapter 4 presents high-power T/R switch designs with differential structure and feed forward capacitors, and Chapter 5 presents PA design and its integration with the proposed T/R switch design, employing multi-section output impedance matching network, based on the knowledge from Chapter 2 and 3. Also, switch controller design is introduced here. Finally, Chapter 6 summarizes and concludes the work in this dissertation.

CHAPTER 2
A HIGH-POWER RF TRANSMITTER FRONT-END COMPONENTS

2.1. Introduction

Before advancing to the topic of CMOS RF T/R switch and PA, this dissertation will present an overview of the functional blocks, which will serve as a guideline for the remainder of this research. A prerequisite for the design of those two blocks is a thorough understanding of the meaning and the significance of their key characteristics, such as output power, gain, efficiency, and linearity for PAs and insertion loss, isolation, and P_{1dB} for T/R switches.

Section 2.2 introduces the key characteristics of RF T/R switches, and Section 2.3 presents the general design procedures for T/R switches. Similarly, Section 2.4 and 2.5 deal with those of RF PAs. Finally, the general measurement setups for T/R switches and PAs are introduced in Section 2.6.

2.2. Characteristics of RF T/R Switches

2.2.1. Insertion Loss

Insertion loss of T/R switch directly affects to the total efficiency of transmitter front-end module. In Figure 7, a typical series-shunt switch schematic is shown. As illustrated in Figure 7, there are two factors which cause the insertion loss through the switch

devices. The first factor of the insertion loss is the on-switch on-resistance, R_{on}, which is calculated by the equation (1) [2]. Since a Watt-level power is going through the on-switch, even a small resistance can cause huge loss. In a given technology, μ, and C_{OX} are fixed, so the width of transistors should be enlarged, and the overdrive voltage, V_{GS}-V_{TH} should be large to reduce R_{on}. However, another important characteristic for T/R switches, isolation, degrades as the width of the switch device enlarges.

Even though its effect is weak, compared to R_{on}, the leakages through shunt switch and off-switch also increase insertion loss of the T/R switch.

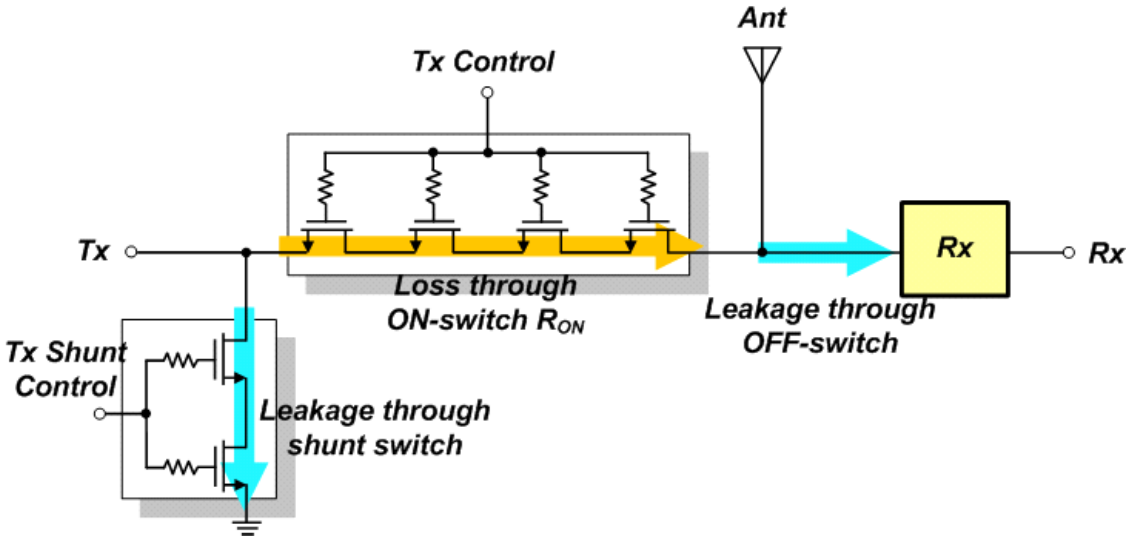


Figure 7. T/R switch insertion loss mechanism

$$R_{on} = \frac{L}{\mu C_{ox} W (V_{GS} - V_{TH})} \quad (1)$$

2.2.2. Tx/Rx Isolation

Port isolations are another T/R switch design issue. If the port isolation in receive mode is not secured, the large signal from the transmitter might degrade the sensitivity and the selectivity of receiver by lifting up the noise level. On the other hand, a bad port isolation in transmit mode causes a signal leakages. For the T/R switches, isolation is finite because of the imperfection of switch devices which have various parasitic capacitances [3]. That is, as mentioned earlier, there is a trade-off relation between the port isolation and the switch insertion loss since the larger devices have the larger parasitic components. Furthermore, due to the effect of parasitic components, achieving the high port isolations for the multiple throw switches, such as SP7T or SP10T covering multi-band or multi-mode, is much more challenging, comparing to the SPDT switches [4,5].

2.2.3. Power-Handling Capability

Power-handling capability is also represented by linearity, since it is the index that shows how large power signal can be handled without distortion. Non-linearity of the T/R switch mainly comes from the active characteristics. Parasitic elements of the transistors, especially junction diodes and gate capacitors are the major contributors for the non-linearity. With the elements, the power-handling capability of T/R switches is dominated by the maximum voltage swing over the off-state switch devices as shown in Figure 8. In other words, channels and junction diodes of the off-state switch devices can be formed or forward biased, respectively, by a large voltage swing and it causes undesirable power losses. Hence, the positive peak of the voltage swing over a switch device is limited by

the threshold voltage of the device and the negative peak of the voltage swing is bounded by the junction diode turn-on voltage as shown in Figure 8.

Particularly, the relatively low breakdown voltage of CMOS devices, comparing to the other competitors such as Gallium Arsenide (GaAs) and Silicon Germanium (SiGe), limits the voltage swing as well[6]. Since the most of mobile PAs are required to transmit more than 1-W as indicated Table 1, and even the PAs with less than Watt-level typical output power have much higher peak power than that, RF T/R switches should be able to handle those high power signals linearly. For example, the peak-to-peak voltage for 30-dBm (1-W) power is 20-V with a 50Ω load. This voltage swing is too large to be sustained by a single CMOS active device, resulting in not only the device breakdown but also leakages through the switch device and substrate.

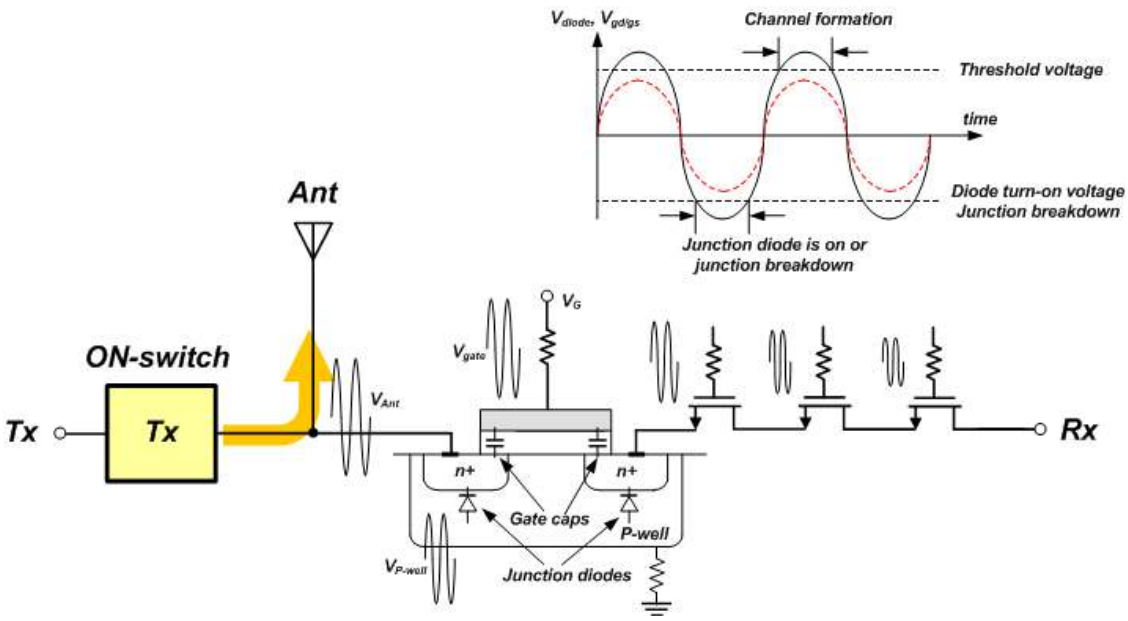


Figure 8. T/R switch power-handling capability

2.3. RF T/R Switch Design

Since the T/R switches come at the last stage of the transmitter chain, and the first stage of the receiver chain, insertion loss of the T/R switch directly affects the efficiency of the transmitter and the noise figure of the receiver at the same time. As introduced earlier, the most straightforward method to minimize the insertion loss is enlarging the size of switch devices. However, the parasitic capacitances also increase as the size of device enlarges, resulting in bad isolation characteristic. Furthermore, the large device is not desirable from the perspective of power-handling capability, as well. The enlarged junction diodes can provide a low-resistance signal path by forward-biased when a large signal flows, deteriorating the power performance, eventually. Therefore, the trade-off relation should be understood clearly to design a high performance T/R switches.

In order to implement T/R switches with a minimum loss and reasonable port isolations, the most widely used circuit topology is the series-shunt switch configuration [7]. The simplest type of T/R switches with the series-shunt structure is shown in Figure 9. Series switches, M1 and M2, carry signals from a transmitter to an antenna and from the antenna to a receiver, respectively. On the other hand, shunt switches, M3, and M4, are added on Tx and Rx ports, to improve the isolation characteristics. For example, in the transmit mode, M1 and M4 are turned on, while M2 and M3 are turned on in the receiver mode. The sizes of M1 and M2 devices are determined by balancing the loss from on-resistances and the loss from parasitic components. The resistances at gate ports should be reasonably large, i.e. larger than 10kΩ, to secure the reliability by achieving the AC isolation.

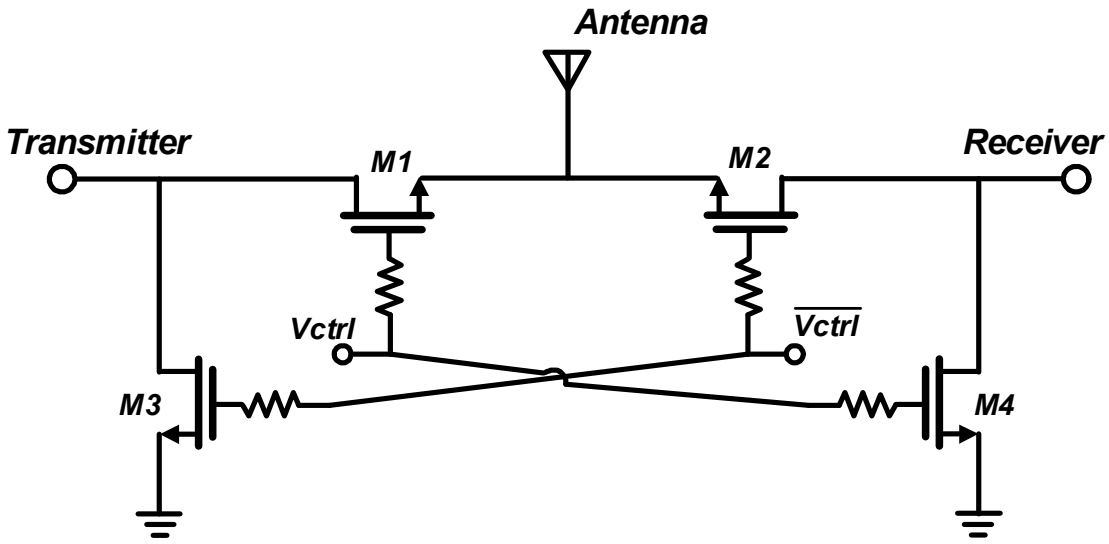


Figure 9. Typical series-shunt T/R switch structure

Most of design parameters such as μ, C_{OX}, and parasitic elements which impact on insertion loss and isolation are determined by process. Therefore, the only parameters we can control are the bias voltage, device size and substrate networks at the device level. As shown in Figure 10, insertion and isolation of switch devices can be optimized according to the device size with respect to the frequency.

Regarding to the size of switch device, substrate networks should be taken account, especially in case of MOS switch design. In MOS switch design, the body floating technique is very usual to improve the T/R switch linearity without any penalties [8]. To do that, deep N-well (DNW) devices should be employed to bias the body of device (i.e. P-well). For a given size, the amount of substrate leakage of DNW devices is determined by value of parasitics, that is, p-n junction capacitors between P-well, DNW, and P-substrate.

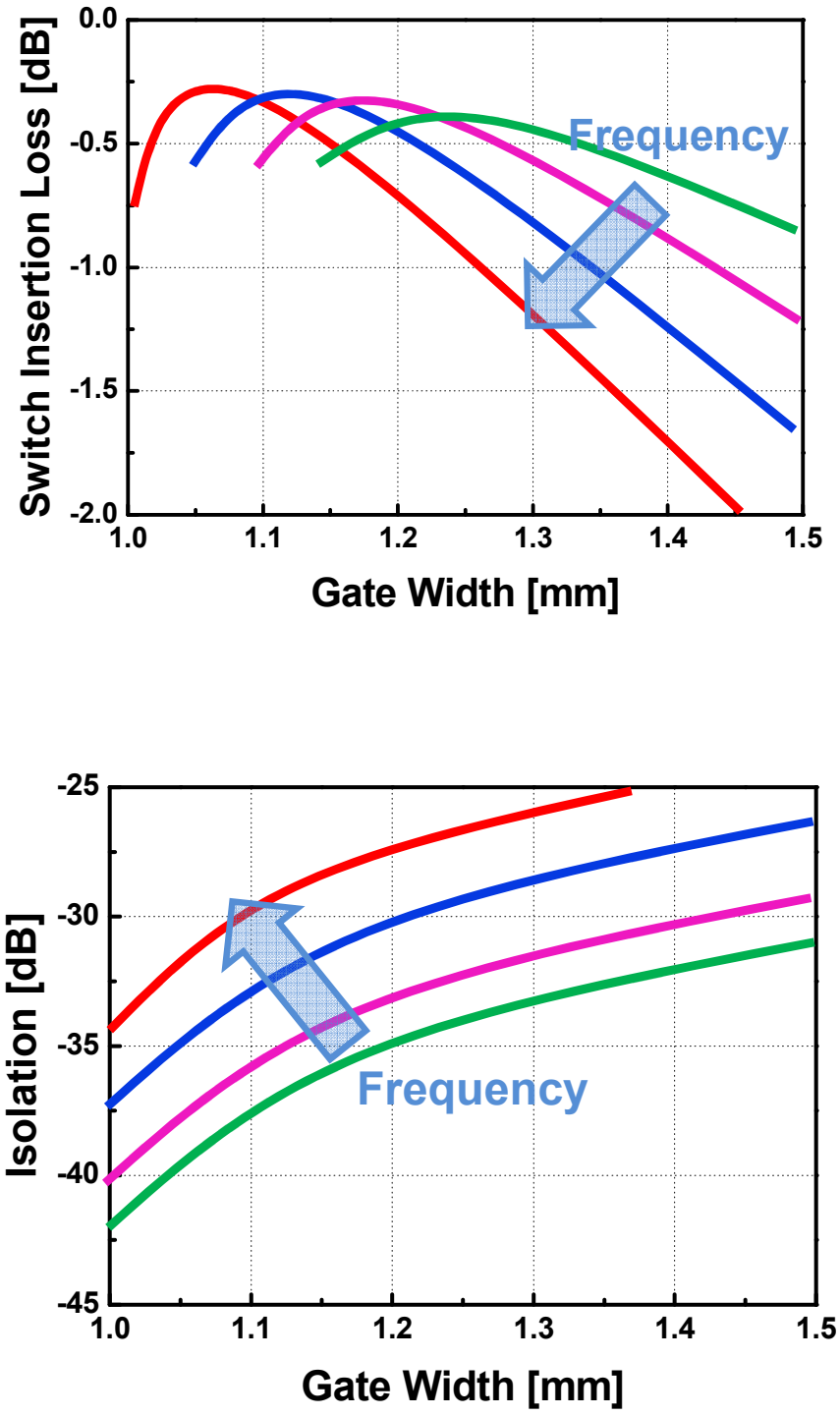
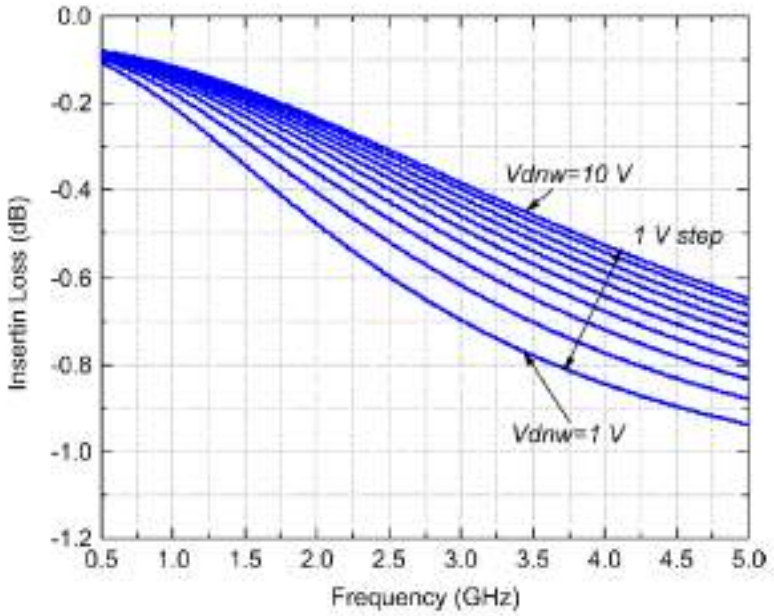


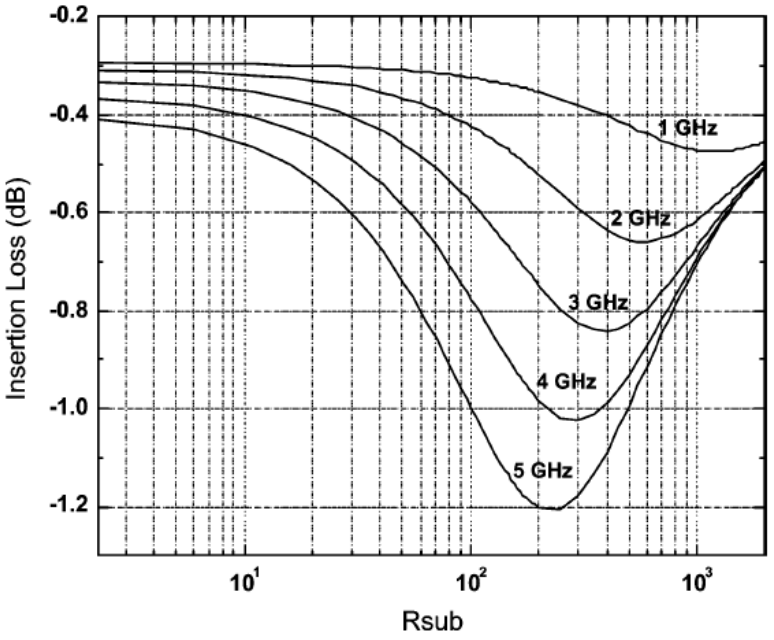
Figure 10. T/R switch size determination

By biasing the substrate ports, that is, P-well, DNW, and P-substrate ports, the values of parasitic can be controlled and optimized for the low loss [9]. In Figure 11 (a), switch insertion loss is plotted by controlling the bias at the DNW port. As shown in the Figure, the switch insertion loss is improved by strong reverse bias over junction diodes. Furthermore, the switch linearity is also optimized by the strong reverse bias, preventing the junction diodes from unwanted forward biasing. The effect of substrate resistance is also demonstrated in Figure 11 (b). By controlling the area and the location of ground contact, the substrate resistance can be manipulated and it should be extremely high or low to obtain low loss, according to the Figure 11 (b) [9,10].

To obtain low loss and high-power handling capability, switch device layout should be done carefully, as well. As explained earlier, all kind of the switch performances can be degraded by parasitic components. For example, the port isolation is deteriorated by parasitic components of off-switch, especially by C_{DS} [3]. The junction capacitance between P-well and DNW, and the junction capacitance between DNW and P-substrate influence switch linearity [9]. Finally, all kind of junction diodes and parasitic components corrupt the insertion loss by forming the unwanted signal paths. Therefore, the inter-digit type of switch layout needs to be employed as illustrated in Figure 12 [3]. Also, the area of P-well and DNW should be minimized referring a given process design rules.

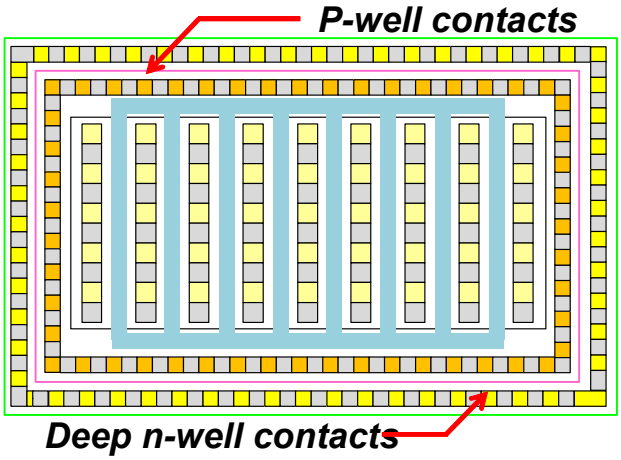


(a)

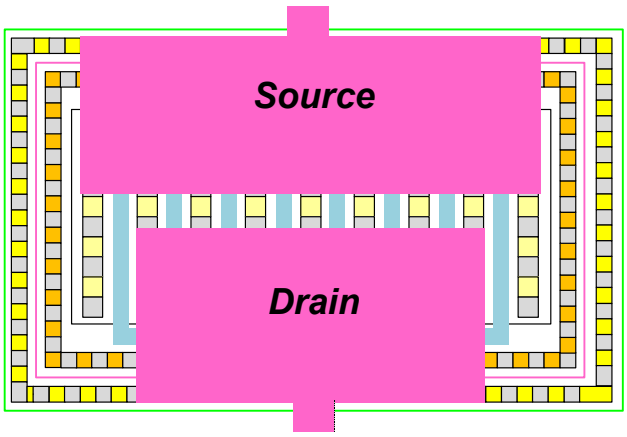


(b)

Figure 11. Effects of substrate network on insertion loss by (a) junction capacitance (b) substrate resistances



(a)



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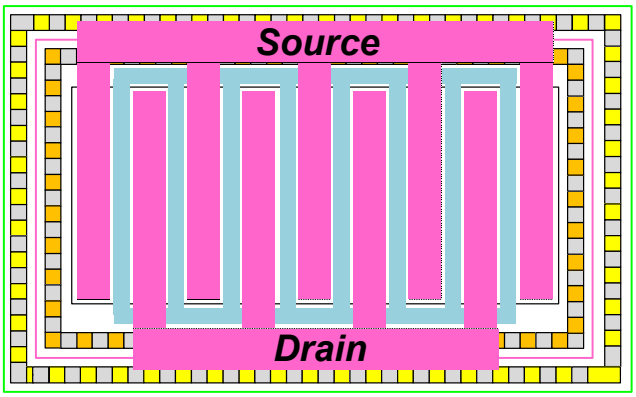


(c)

Figure 12. T/R switch layout (a) typical MOS device (b) conventional layout (c) layout with inter-digit type S/D fingers

2.4. Characteristics of RF Power Amplifiers

There are many characteristics to consider in designing the PAs. For example, output power, efficiency, linearity, stability, and so on. In this chapter, however, the discussion is only focused on the output power and the efficiency which are the most important features in designing the high-power transmitter module with the saturated PAs.

2.4.1. Output Power

The output power from transmitter is supposed to travel through the lossy material – the air, and it must be strong enough when it reaches to the destination. The output power is mainly dominated by PAs, so the output power is the most important design parameter in PA design. Particularly, the mobile transmitters are usually required to transmit high power (i.e. more than 1-W) to remote base stations. For instance, the typical output powers of PAs for mobile handset applications are listed in Table 1.

Table 1. Typical output power of PAs for some wireless applications

Standard	Frequency (MHz)	Typical Output Power (dBm)	Modulation
GSM 850	824-849	35	GMSK
E-GSM 900	880-915	35	GMSK
DCS 1800	1710-1785	33	GMSK
PCS 1900	1850-1910	33	GMSK
CDMA (IS-95)	824-849	28	O-QPSK
PCS (IS-98)	1710-1910	28	O-QPSK
WCDMA (UMTS)	1920-1980	27	HPSK

From the perspective of design, the only design parameter for the PA output power is the amount of current since a supply voltage is given as a fixed value usually. Assuming

a normal output load with resistance, R, the PA in Figure 13 has an output power of the following expression:

$$P_{OUT} = \frac{\left(\frac{V_{peak\ to\ peak}}{2}\right)^2}{2R} \quad (2)$$

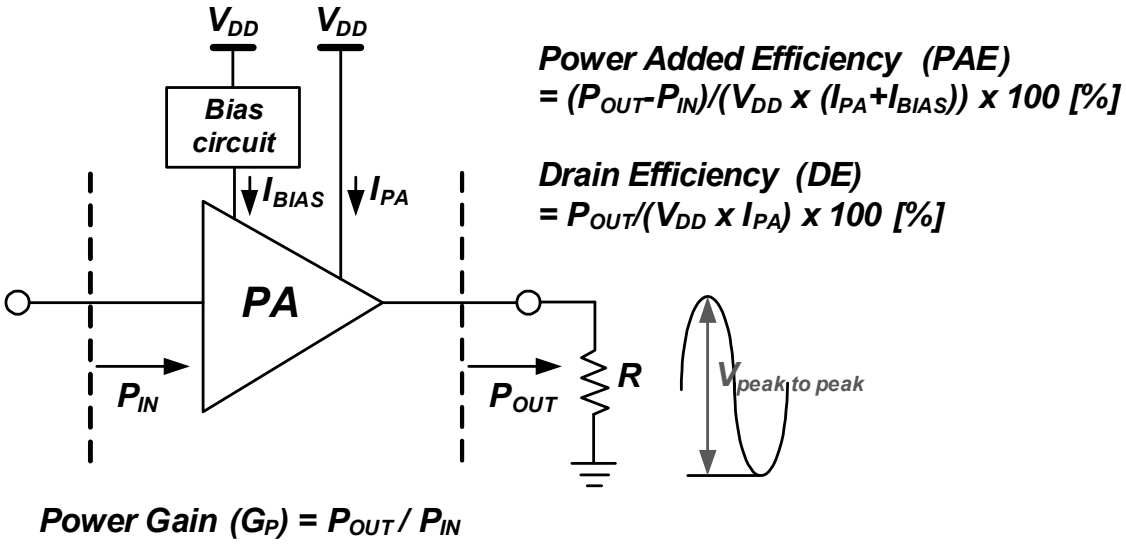


Figure 13. Various PA characteristics

2.4.2. Efficiency

The battery life of mobile device is mainly governed by the efficiency of the transmitters. To transmit high output power, a significant amount of current is supposed to flow through the PAs, resulting in the huge power dissipation. As the functions of mobile devices are getting diversified, the battery life is getting more important. Therefore, a great deal of endeavor is being made to improve the PA efficiency. For example, a device resizing technique and a reconfigurable matching network are utilized to improve the overall PA efficiency [11,12].

There are two primary ways to define the PA efficiency. The first one is power-added efficiency (PAE), and the other one is drain efficiency (DE). The equations for these efficiencies are shown in Figure 13. As shown in these equations, the equation for the PAE includes the gain (P_{OUT}-P_{IN}) information while the equation for the DE does not. Meanwhile, in calculating the efficiency, PAE is mainly used for its obviousness. For example, if the PA gain is not enough to meet the transmitter specifications, one or more stages of PA are supposed to be implemented. In those cases, the total PA efficiency is ambiguous with the DE definition since it does not carry the gain information in its expression.

2.5. RF Power Amplifier Design

The design of PA starts from selecting a device for power cell. In this phase, the transistor characteristics are evaluated by the load-line analysis, and device size is determined. Once the circuit topology and size of power cell is decided, load-pull and source-pull simulations are executed iteratively to reach to the PA specifications. If gain of this power stage is not enough, one or more amplifier stages are required, and the same load-pull and source-pull simulations need to be done for each stage. After finishing the design of amplifier stages, matching networks - the output matching (between output and the last stage of PA), the inter-stage matching (between amplifiers), and the input matching (between input and the first stage of PA) – are designed. With the full PA design, the performance of PA is optimized. Like RF T/R switch design, trade-off between the characteristic should be considered carefully.

In this research, as mentioned earlier, the output power and the efficiency are mainly discussed among various PA characteristics. In order to generate a high output power, the

most intuitive approach is to enlarge the size of power cell. However, the size cannot be enlarged unlimitedly since heat cannot be distributed equally over the large device, causing problems in long-term reliability. Moreover, an extremely low load impedance is required for the large device, which eventually leads to the degradation in efficiency of the output matching network with the large impedance transformation ratio. Therefore, when a single power cell cannot provide a sufficient output power, the powers from multiple PAs are combined to generate the required output power [13-15]. However, since the power combiner may introduce an additional loss, its implementation should be fulfilled carefully. Besides, there is another concern about the high output power – device breakdown. To transmit the high output power, the devices suffer from the large voltage stress and it can threaten the device reliability. As an approach to resolve this issue, cascode PA is widely utilized [16].

Meanwhile, the total PA efficiency is mainly influenced by the output impedance matching network, especially in high power applications. The output impedance of PA is usually low, enabling to drive more current at the PA output to generate a high output power [13]. Therefore, the efficiency of the PA output matching is low due to the large impedance transformation ratio between the PA output and the PA load. As the required power level increases, the more loss might be generated from the matching network increasing the burden of the impedance transformation. On the other hand, a good PA back-off efficiency is required in low power region. Most of PAs in recent market are demanded to support various power modes, and multi-mode PAs are spot-lighted instead of implementing multiple PAs for the modes. Since load-pull and source-pull simulations are oriented to fit the peak power condition, the efficiency is usually very low at the low

power region. To improve the back-off efficiency, its matching, supply, or biasing conditions need to be reconfigurable somehow. In order to improve the efficiency at low and medium power modes for linear PAs, a device resizing technique and a reconfigurable matching network are utilized. The efficiency improvement concept is illustrated in Figure 14.

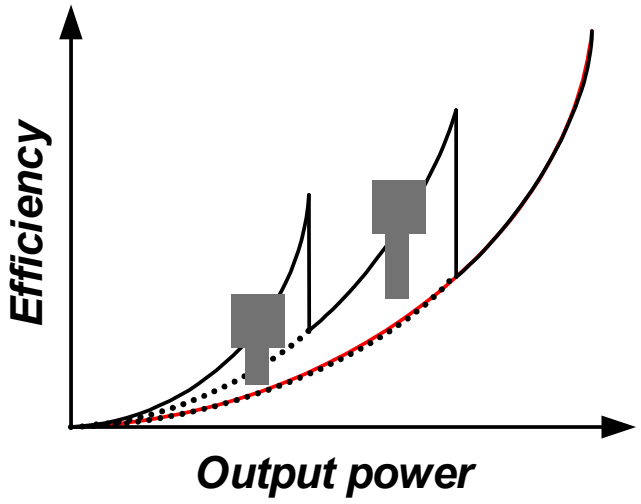


Figure 14. Low power efficiency improvements

2.6. Measurements of T/R Switches and Power Amplifiers

The measurement setups for T/R switches, PAs, and even for transmitter module are identical. To measure these components, a vector signal generator, high-power linear PA, low pass filter (LPF), couplers, power meter, two power sensors, attenuators, and spectrum analyzer are needed as shown in Figure 15.

For T/R switches, P_{1dB} and harmonic components are measured with this setting, and to measure the harmonic components from T/R switch alone, LPF is additionally is

implemented at the output of PA suppressing the harmonic components from PA. The insertion loss and the port isolations are measured by network analyzer. As shown in the Figure 16, in Tx mode, insertion loss is measured by S21 and isolation is measured by S32 while port1, port2, and port3 are Tx, antenna, and Rx, respectively. S-parameters in Rx mode are also obtained in the same manner.

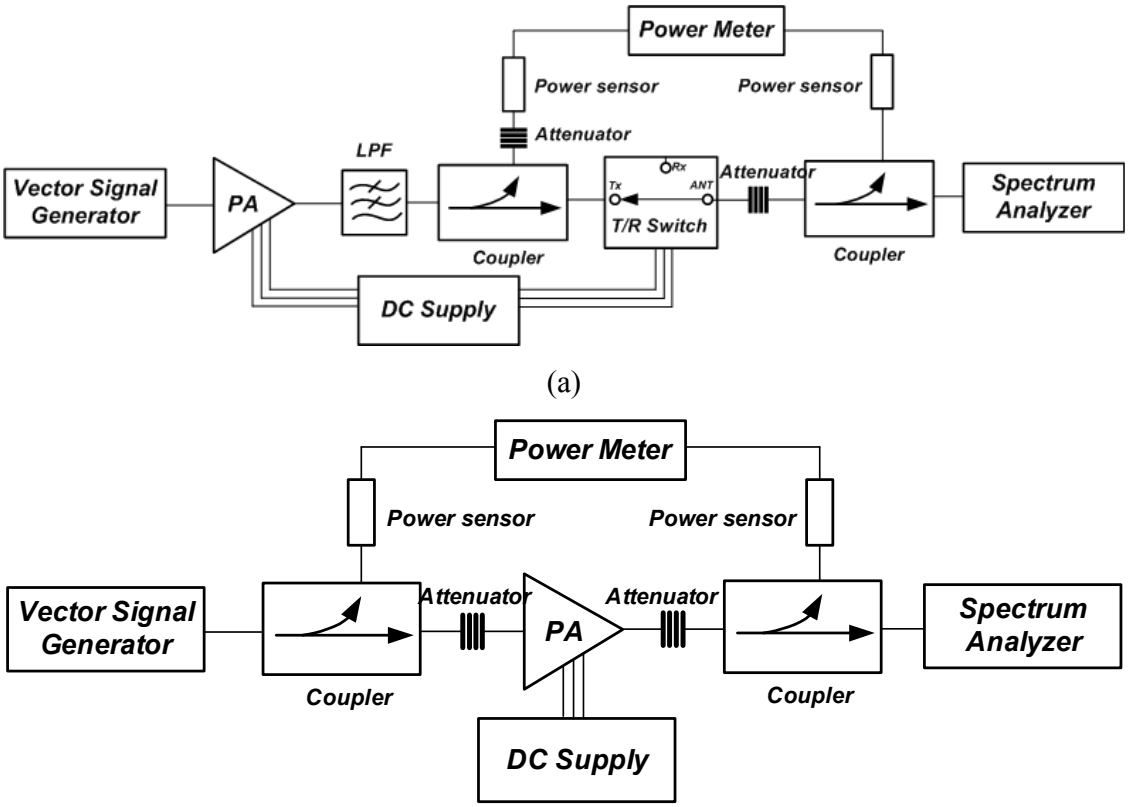


Figure 15. Measurement setups for (a) T/R switches (b) PAs

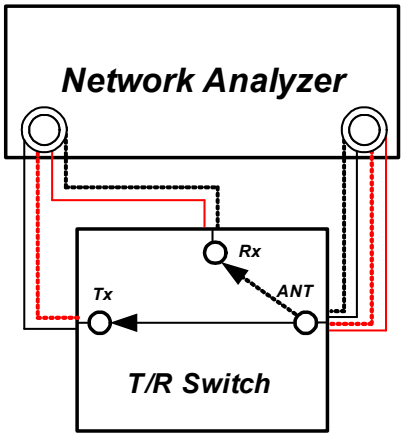


Figure 16. S-parameter measurements for T/R switch (solid line: Tx mode, dotted line: Rx mode, black line: insertion loss, and red line: isolation)

For PAs, output power, P_{1dB}, efficiency, gain, and harmonic components are measured with this setting. Efficiency is calculated by equation introduced earlier, by measuring bias voltage and current flowing.

2.7. Conclusions

In this chapter, general indicators and background knowledge for designing T/R switch and PAs have been covered. In sum, insertion loss, isolation, and P_{1dB} are simulated in designing the T/R switches, while gain, output power, efficiency, and P_{1dB} are simulated in designing PAs. Also, the design issues for those blocks have been introduced considering trade-off among the characteristics. Finally, measurement setups for the blocks have been explained.

CHAPTER 3
CHALLENGES AND TECHNIQUES IN DESIGNING HIGH-POWER CMOS TRANSMITTER FRONT-END

3.1. Introduction

As discussed previous sections, there are numerous concerns in designing high-power handling components – PAs and T/R switches. In case of CMOS designs, these concerns are even more critical. First of all, the device breakdown voltage is too low to sustain the high-power signal [17]. Furthermore, the substrate of CMOS device is very lossy, comparing to other devices such as silicon-on-insulators (SOI), silicon-on-sapphire (SOS), and compound semiconductor devices [18-20]. Lastly, quality factors (Q) of passive are low causing a high loss [6].

In this Chapter, the drawbacks of CMOS process while designing high-power handling RF building blocks are presented in Section 3.2, and challenges in actual CMOS design are discussed in detail in Section 3.3. The prior arts to tackle the challenges are introduced in Section 3.4.

3.2. Challenges of CMOS Process for High-Power Applications

3.2.1. Low Device Breakdown Voltage

The most apparent intrinsic drawback of CMOS technology is the low breakdown voltage. While GaAs hetero-junction bipolar transistors (HBTs) have high breakdown voltage sustaining up to 20V, CMOS transistors endure only up to the twice the supply

voltage [13], severely limiting the range of the supplying voltage. Since PAs and T/R switches experience the high-power signal at the end of transmitter, the low breakdown voltage directly affects to the performance and reliability of them. For example, 20-V peak-to-peak voltage (V_{pp}) swing is required to transmit 1-W power with 50-Ω load impedance and it cannot be endured by a single CMOS device. Therefore, cascode topology for PAs and stacked the multiple switch devices for T/R switches [16, 21]. If the reliability is not secured, even if all kind of PA and T/R switch performances are satisfied, they are not functioning normally. Therefore, the reliability should be the first priority in designing those blocks.

3.2.2. Lossy Substrate and Low Passive Quality Factor of CMOS

As discussed earlier, the lossy substrate prevents T/R switches and PAs from not only their linear but low loss operations. Since the substrate of CMOS devices is supposed to be shared with the other functional blocks, it cannot be biased or floated arbitrarily, of course. Moreover, it is very hard to define the substrate network structure because it strongly depends on numerous variables layouts, device sizes, and so on.

Figure 17 shows the loss mechanism of passive structures in CMOS technology. The main concerns here are eddy current and capacitive coupling current. The eddy current which caused by the magnetic field and the substrate conduction current flow through the lossy substrate resulting in losses, degrading the Q of passive, eventually. Therefore, in addition to reduce the ohmic loss by enlarging the passive dimension, maximizing the quality factor by minimizing the parasitic capacitances, and reducing the eddy current are the main design goals of the passive components in CMOS technology [22].

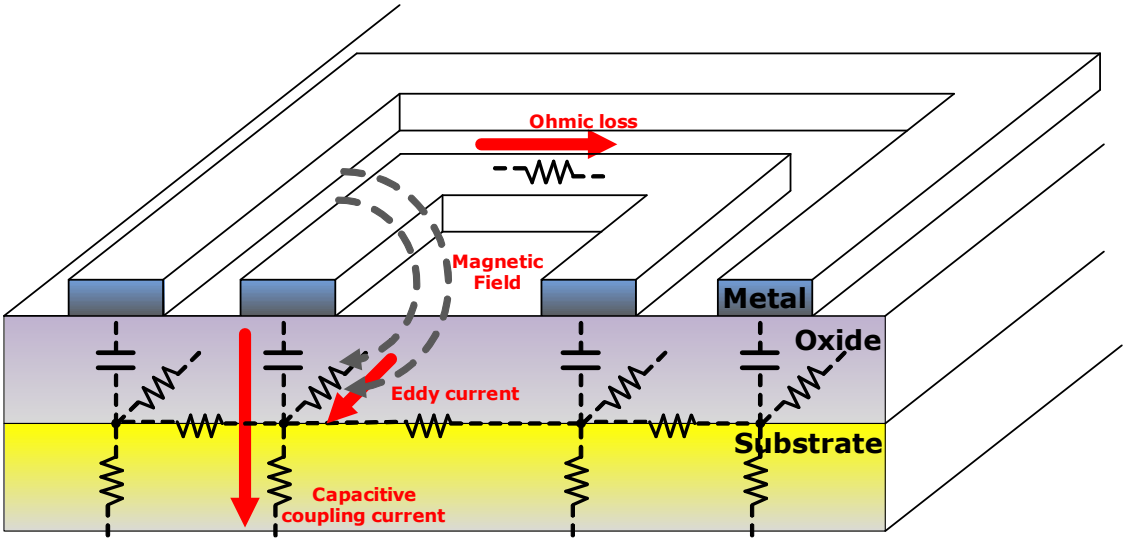


Figure 17. Loss mechanism of CMOS passive structure

3.3. Challenges of CMOS T/R Switches and Power Amplifiers

3.3.1. Challenges of CMOS T/R Switch Design

As introduced in Chapter 2, the most popular T/R switch structure is series-shunt type to improve the isolation functioning as a T/R switch. Also, DNW devices are usually employed to control local substrate, which is so called P-well [8]. In this section, challenges of CMOS T/R switches are discussed, assuming this switch structure and device.

3.3.1.1. Insertion Loss and Isolation of CMOS T/R Switches

To understand the loss mechanism of T/R switches, the actual equivalent circuit of switch device is worth to be known first. The typical switch device structure is found in Figure 18. As shown in the Figure, many parasitic components and junction diodes are placed around even though this is a significantly simplified active switch device model.

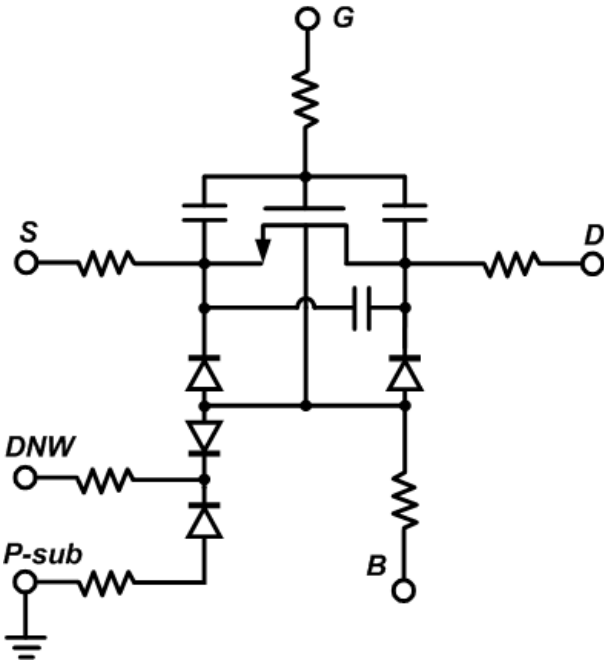


Figure 18. Simplified equivalent model of CMOS devices

As already mentioned, two main loss mechanisms over the switch devices are on-resistance, and leakage through the substrate or off-switches. Although the on-resistance is dominant factor determining the total switch insertion loss, it is not always true in the case of CMOS T/R switches. Since the CMOS device cannot endure the large voltage swing to carry the high-power signal, multiple devices should be stacked inevitably. In that case, the loss through the substrate dominates the loss mechanism, and this is why the CMOS T/R switch has the poor insertion loss characteristic. On the other hands, bi-polar junction transistors or SOI devices are relatively free from the limitation of substrate coupling, thus, a lot more devices can be stacked obtaining the power handling capability and the low insertion loss at the same time.

CMOS T/R switch is inferior to its competitors in port isolation, as well. The lossy substrate network provides the low impedance path through the substrate or even through the off-switches degrading the isolation characteristic. Therefore, a certain treatment is required at device level to improve the switch insertion loss and isolation characteristics with the CMOS devices [23, 24]. Otherwise, the power-handling capability of T/R switch should be sacrificed in exchange for the low loss.

3.3.1.2. Power-Handling Capability of CMOS T/R Switches

The power-handling capability of CMOS T/R switches is dominated by the maximum voltage swing over the off-switch devices. The channels and junction diodes of the off-switch devices, also shown in Figure 18, can be formed or forward biased, respectively, by a large voltage swing and it causes undesirable power losses. In other words, the power-handling capability of CMOS T/R switches is influenced not only by the device characteristic (threshold voltage) but also by the lossy silicon substrate. Hence, the positive peak of the voltage swing over a switch device is limited by the threshold voltage of the device and the negative peak of the voltage swing is bounded by the junction diode turn-on voltage. Additionally, the relatively low breakdown voltage of CMOS devices, comparing to the other competitors such as GaAs and SiGe, limits the voltage swing as well.

Since the most of mobile PAs are required to transmit more than 1-W as indicated Table 1, and even the PAs with less than Watt-level typical output power have much higher peak power than that, RF T/R switches should be able to handle those high power signals linearly. The voltage swing to carry the Watt-level power is too large to be sustained by a single CMOS active device, resulting in not only the device breakdown

but also leakages through the switch device and substrate. Therefore, the most important design consideration in designing CMOS RF T/R switches is to relieve the voltage swings over off-switch devices to secure the linear power transmission.

3.3.2. Challenges of CMOS Power Amplifier Design

3.3.2.1. Output Power of CMOS Power Amplifiers

By enlarging the device size, the current-handling capability of power cell is increased, enabling the PAs to transmit the high output power. However, the generated heat inside the power cell is hard to be distributed uniformly over the large device, causing a long-term reliability problem. More seriously, PA load impedance gets lower as the load-line gets steeper with the large device. In other words, the burden of impedance transformation of PA output matching increases. As discussed earlier, passive Q of CMOS process is very low and it leads to serious deterioration in efficiency. In order to reach to the target output power, various kinds of power combining techniques have been employed. In applying the power combining technique, achieving the good combining efficiency is the key concern.

3.3.2.2. Efficiency of CMOS Power Amplifiers

PAs are characterized by the "classes" according to their waveforms. The PAs are divided into two categories with the classes, and one of them is the linear PA and the other one is the switching PA as indicated in Table 2. For the envelop-varying systems, such as wideband code division multiple access (WCDMA), wireless local area network (WLAN), and worldwide interoperability for microwave access (WiMAX), PAs are implemented by using the linear PAs since the amplitudes of the signals should be modulated linearly, sacrificing the efficiency. On the other hands, for the constant

envelop systems, such as general packet radio service (GPRS), and global system for mobile (GSM), PAs are designed by employing switching PAs with the highly efficient operation because the linearity is not important in these systems.

In case of the switching PAs, the efficiency is measured at the peak output power because these PAs always operate at the maximum output power. Meanwhile, the efficiency of the linear PAs is measured at the maximum linear output power since the linear operation is the top priority for these PAs. Nevertheless, the efficiency at the peak output power is important even for the linear PAs to secure the margin of the power back-off for the linear operation. In order to improve the efficiency at low and medium power modes for linear PAs, a device resizing technique and a reconfigurable matching network are utilized. For the efficiency at high power mode, on the other hand, the design of the output matching network of PAs should be optimized since the impedance transformation ratio and Q factor of the output matching network mainly affect to the PA efficiency. Accordingly, a low impedance transformation ratio and a high Q factor of the output matching network are necessary here and the needs conflict to the characteristics of CMOS process, especially for the high power applications.

Table 2. Classes of PA

Class	Linear Amplifiers			Switching Amplifiers		
	A	B	AB	D	E	F
Max Efficiency (%)	50	79	50~79	100	100	100
Conduction Angle (˚)	360	180	180-360	0	0	0

3.4. Prior Arts in CMOS T/R Switches and Power Amplifiers

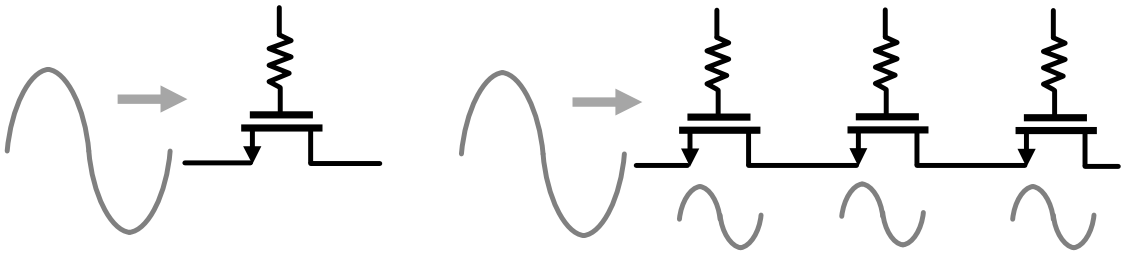
3.4.1. CMOS T/R Switch Power-Handling Capability Enhancement

There have been numerous attempts to improve the power-handling capability of RF CMOS T/R switches. As a typical approach to achieve this goal, multiple transistors are stacked to relieve the voltage stress over switch devices [21]. As shown in Figure 19 (a), large signals are distributed over the multiple devices, enabling to transmit a high power signal linearly. However, the insertion loss is degraded by the stacked transistors since the loss due to the on-resistance and substrate leakage is increased by the series connection of switch devices.

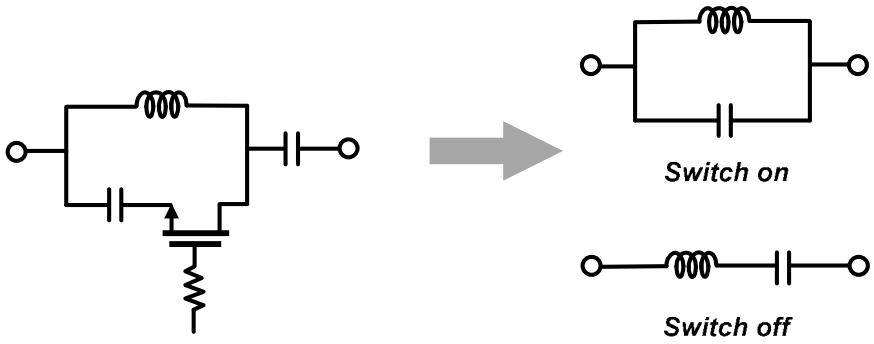
On the other hand, the LC resonance has been utilized to set the off-switch device free from the voltage stress [25] as presented in Figure 19 (b). Nonetheless, this method is not proper for cellular applications where the circuits operate at relatively low frequency, i.e. 1-2 GHz, since the Q factor of the inductor is proportional to the frequency.

As another approach to enhance the power performance of T/R switches, the impedance transformation technique (ITT) is presented [26]. By employing this technique, however, the insertion loss of T/R switches is sacrificed in exchange for the improvement of the power-handling capability with two additional matching networks.

And aside from these, body floating technique [8], LC substrate biasing [27], and feed-forward capacitor [28] are proposed to enhance the power performance of CMOS T/R switches, and the body floating technique is one of the most widely used techniques in recent CMOS T/R switch design.



(a)



(b)

Figure 19. Simplified equivalent model of CMOS devices

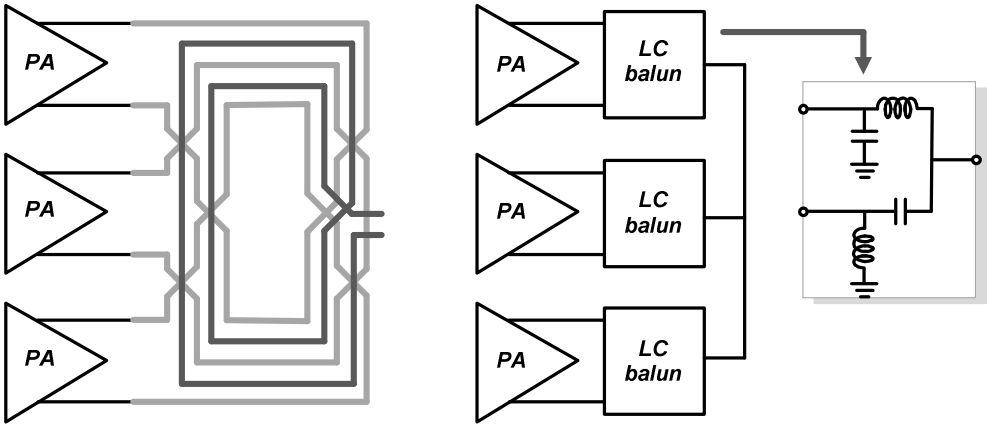
3.4.2. Low Insertion Loss T/R Switches

Since CMOS devices have a low resistivity substrate and a high on-resistance comparing to GaAs devices, the insertion loss of CMOS T/R switches is naturally worse than that of GaAs switches [29]. Therefore, the loss of CMOS T/R switches has been researched and analyzed to overcome the intrinsic flaws. For the circuit level, as mentioned before, the on-resistance and parasitic capacitances of switch devices should be balanced to obtain the optimal insertion loss [10]. To improve the insertion loss further, a specific devices are used [21,28], and modified substrate structures are introduced to reduce the insertion loss of T/R switches [30]. However, the loss optimization is very difficult since an accurate control of the substrate resistance is very challenging, as well as the device and the substrate modeling for large signal operations is not perfect. For

these reasons, switches using a SOI process have been presented recently to improve the insertion loss characteristic of RF switches [5, 18, 31].

3.4.3. PA Output Matching Networks

In cellular applications, a power combining at the output of PAs is necessary to generate a high output power. One of the most popular power combining techniques is based on a Wilkinson power combiner, which requires quarter-wavelength transmission lines [6]. For the cellular applications, this type of power combiner is not suitable, since a very long transmission line is required for the operating frequency below 2 GHz. Instead, power combining networks that are valid for a single chip radio transmitter are presented by utilizing a transformer or a lattice-type LC balun [32]. Moreover, both of these power combining networks can be functioned as an impedance transformer at the output of PAs [13,33]. From the perspective of the size, the transformer-based power combining is more compact than the LC counterpart. However, the design procedure of the transformer is less straight-forward comparing to the LC network due to various design parameters such as coupling factor, turn ratio, and mutual inductance (Figure 20 (a)). In case of LC-type power combiners, the size gets larger as the number of PA cells increases as shown in Figure 20 (b).



(a) (b)

Figure 20. Simplified equivalent model of CMOS devices

3.5. Conclusions

As discussed in this Chapter, there are numerous challenges in implementing CMOS T/R switches and PAs. For CMOS T/R switches, the trickiest qualification to meet is the power-handling capability. Thus, the voltage swing over the switch devices is the main approach to enhance the power performance while securing the low insertion loss. On the other hand, for CMOS PAs, high output power and high efficiency are the main design concerns. In other words, high power should be transmitted from the PA and the loss through the signal path, particularly through the passive structure, should be minimized while guaranteeing the reliability.

CHAPTER 4
A HIGH-POWER HANDLING CMOS T/R SWITCHES FOR MOBILE APPLICATIONS

4.1. Introduction

The typical output powers of PAs for mobile handset applications fairly exceed the Watt-level as indicated in Table 1. Meanwhile, T/R switches are expected to have even higher P_{1dB} than these PA output power levels, to transmit a high power signal to the antenna linearly demanding a high-power handling T/R switches.

Large voltage swing from a PA is the main cause of the degradation of power performance of T/R switches. Channel and junction diodes of off-switches are unintentionally turned on by the large signal, resulting in undesired power losses. Moreover, devices cannot even sustain over a certain level of voltage swing. Therefore, reducing the voltage swing over the off-switch devices is essential to improve overall power-handling capability of T/R switches.

In Section 4.2, a basic structure for high-power T/R switch – multi-stack T/R switch structure – is introduced, and the substrate network of CMOS device is analyzed to understand loss mechanism and large signal behaviors. In Section 4.3, based on the multi-stack T/R switch structure, the differential switch design and measurement results are followed. As another approach to enhance the power-handling capability of T/R switches, impedance transformation technique (ITT) and T/R switch with feed-forward capacitors are discussed in Section 4.4 and 4.5, respectively.

4.2. Basic High Power-Handling T/R Switch Structure

4.2.1. Design of the Multi-Stack T/R Switches

Since the switch devices cannot sustain the large voltage swing, the stress should be reduced somehow. Maintaining the same size of voltage swing to transmit high power, the only way to guarantee the reliable switch operation is stacking the devices to distribute the stress over multiple devices. Needless to say, this structure is essential for CMOS T/R switch because the CMOS devices have very low breakdown voltage comparing to other devices.

Even though the multi-stacked FETs in the Rx path can enhance the power-handling capability of T/R switches, the insertion loss in the Rx mode is inevitably sacrificed by the increased on-resistance. Unfortunately, the damaged insertion loss cannot be compensated by enlarging the device, especially at a high frequency, because of the effects of parasitic components on the insertion loss. Furthermore, signal leakages through the conductive substrate become more critical as the number of stacked transistors increases, resulting in a degradation of the power performance as shown in Figure 21[9].

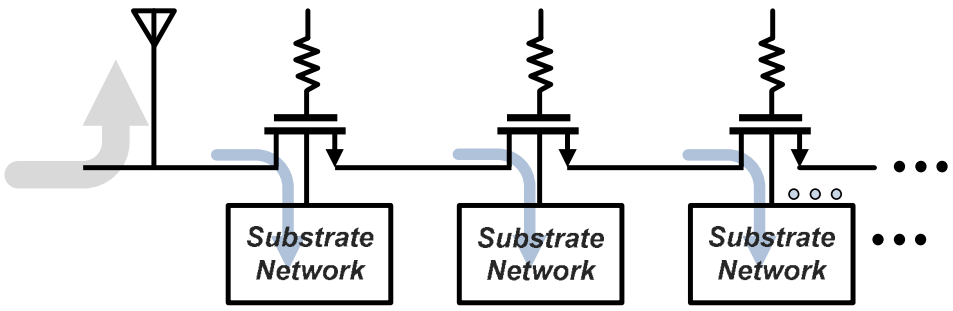


Figure 21. Signal leakages through CMOS substrates

In contrast, T/R switches that are implemented in GaAs PHEMT technology or SOI CMOS technology can be designed with much larger switch devices, and much more stacked devices, e.g., 12 stacks, since there are much less parasitic and substrate leakage effects [34, 35]. Because of this inferior characteristic of the CMOS process, the number of stacked devices and their gate widths should be chosen carefully balancing the power performance and the insertion loss of T/R switches.

4.2.2. Substrate Network of CMOS Devices

To understand the effect of substrate network of CMOS devices, device test patterns have been measured with the various bias conditions on the substrate ports (P-well, DNW, and P-substrate ports) as shown in Figure 22. For a given size of switch device, the amount of substrate leakage of DNW devices is determined by values of C_{pwell_DNW}, C_{DNW_psub}, and R_{psub} in Figure 23. The effect of R_{psub} has been analyzed in [9], and it should be extremely low or high to minimize the substrate leakage. R_{psub} is usually controlled by the layout, the amount of ground contacts and the distance between the chip and contacts. In the proposed design, the low substrate resistance is chosen since the low R_{psub} provides not only low substrate leakages, but also a low impedance path between the signal and the ground, leading to better isolation [36].

Meanwhile, C_{pwell_DNW} and C_{DNW_psub} should be minimized as much as possible, and it can be done by biasing the junction diodes between P-well/DNW, and DNW/P-substrate reversely. In [9], the substrate network of switch device was modeled with reasonable simplifications, as presented in Figure 23, and measured to find out the values of those capacitors in various bias conditions. As expected, Figure 24 shows that these capacitances are reduced by a negative bias at the P-well and a positive bias at the DNW

ports. The negative bias at the P-well also helps to prevent the junction diodes from turning on between the source/drain and the P-well. These bias voltages cannot go over the reverse breakdown voltage of the junction diodes, of course.

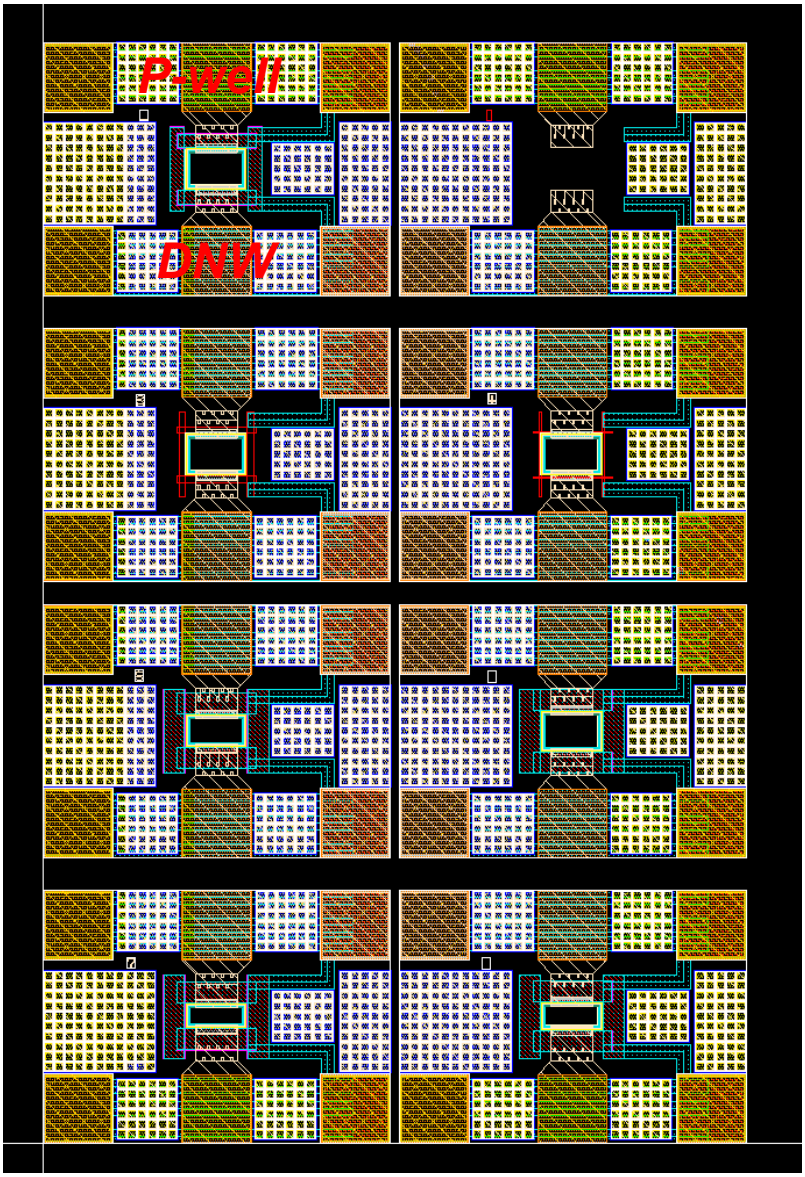


Figure 22. Device layouts for CMOS devices with various gate widths

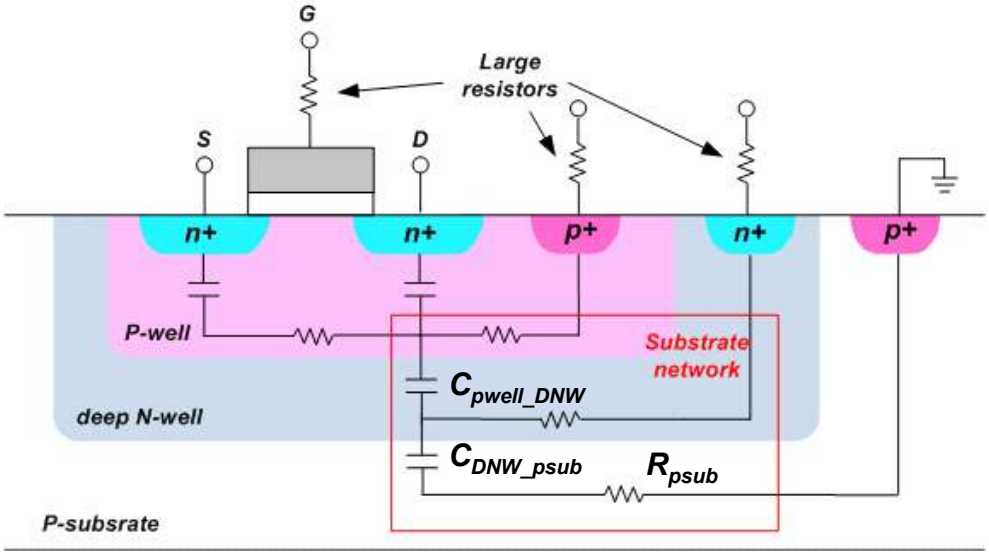


Figure 23. Simplified model of substrate network

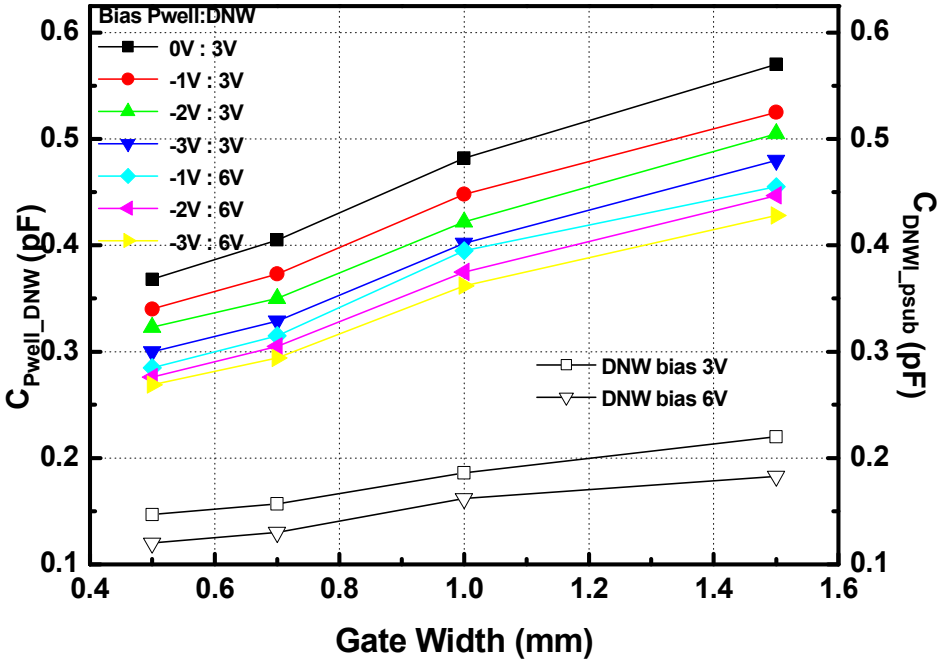


Figure 24. Junction capacitances according to various bias conditions

In summary, the substrate leakage is minimized by (1) implementing substrate ground contacts as many as possible, and (2) biasing the P-well and DNW ports with negative and positive supplies, respectively. With these approaches in designing multi-stack FETs, the limitations on the switch device sizes and the number of stacked devices can be much relieved.

4.3. Differential CMOS T/R Switch Schematic and Operations

4.3.1. Schematic and Operations of Differential CMOS T/R Switch

The differential architecture has superior characteristics in linearity, robustness, and noise immunity to the single-ended configuration [3]. By virtue of these advantages, many state-of-the-art transceiver building blocks such as low noise amplifier, mixers, and even power amplifiers are designed using differential configurations. Particularly, in case of the T/R switch design, the differential architecture helps to divide the voltage stress in half with two identical paths, transmitting twice of power. Taking these into account, the differential architecture is chosen for the T/R switch design aiming to the full-differential front-end solution with a high power-handling capability. The proposed differential switch structure is shown in Figure 25. By implementing the differential switch with two of the single-ended switches, the voltage swing over the off-state receive switches is decreased in half as shown in Figure 26.

In designing the receive switch, the LC resonant circuit is one of the best candidates for high-power applications, but Q factor of on-chip inductors is not high enough to be implemented at 2 GHz of frequency range. Instead, a stacked transistor structure has been used to relieve the voltage stress over the Rx switch devices. Three thick-gate-oxide transistors are stacked at Rx series paths to improve the power-handling capability by

protecting the switches from a device breakdown and unwanted channel formations. Furthermore, Tx shunt switches are designed with four stacks to sustain the large voltage swing in the OFF-state. Since Tx series and Rx shunt switches are free from the large voltage stress, single thin-gate-oxide devices can be used for these switches to enhance the insertion loss in the transmit mode. All switch devices are NMOS devices since the on-resistances are important to achieve a low-loss operation. Also, all of them employs the DNW structure to utilize the body floating technique [8]. The P-well and DNW ports of the devices are biased at the negative and the positive supply, respectively, to prevent junction diodes from turning-on. Resistors at the gate, body, and deep N-well port are all 10 kΩ to achieve high AC isolations.

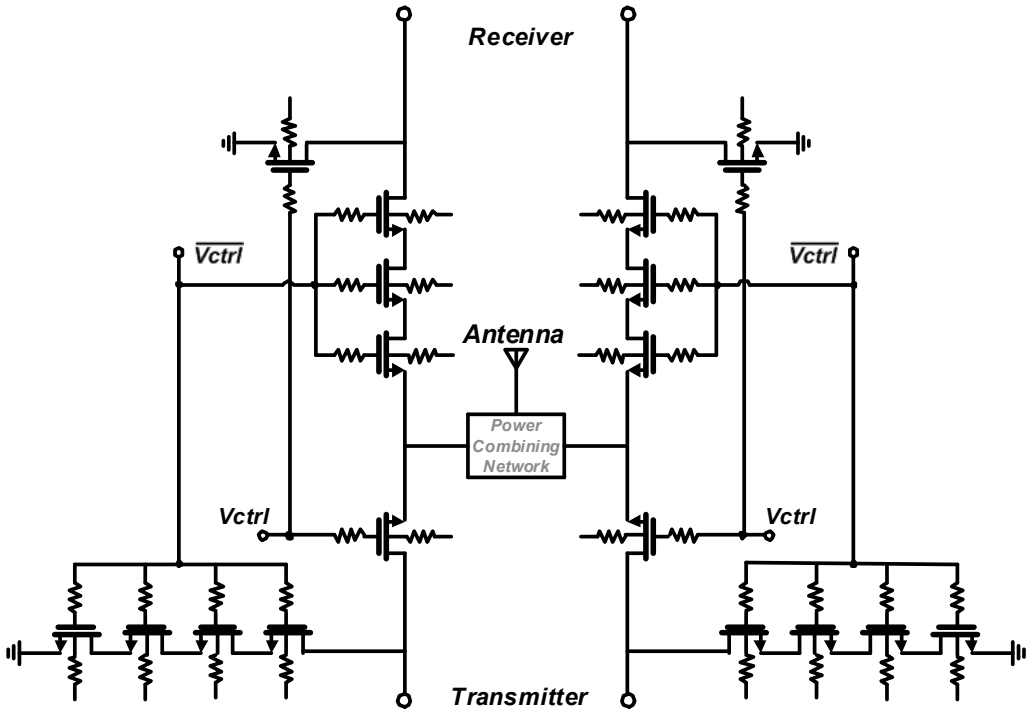


Figure 25. Schematic of the proposed differential T/R switch

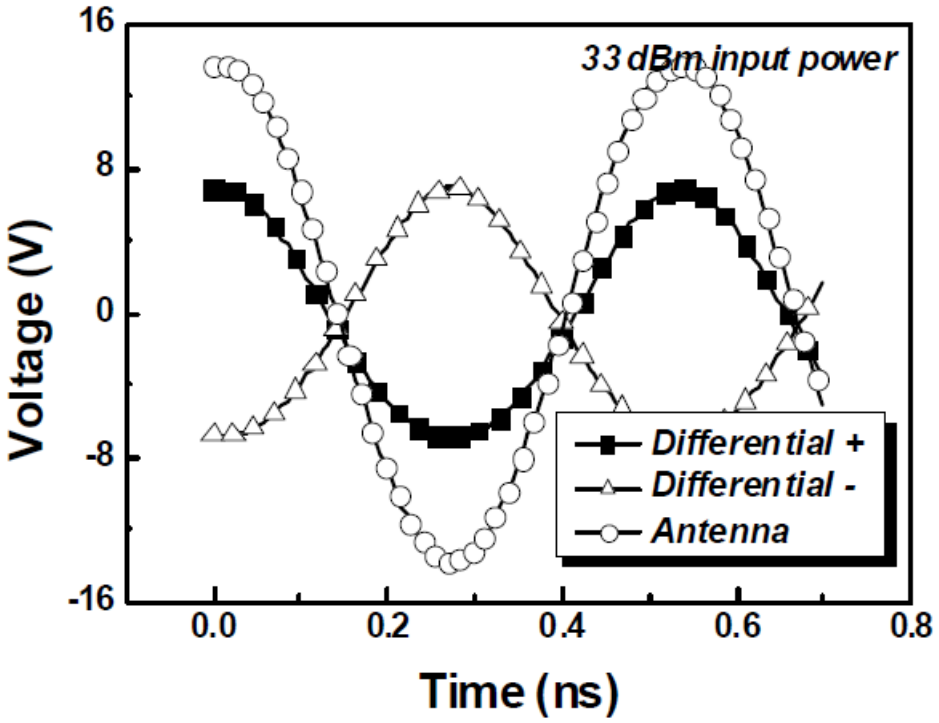


Figure 26. Voltage swing reduction by differential architecture

4.3.2. Measurement Results

Insertion loss, return loss, isolation, and power-handling capability were measured to verify the performance of the proposed switch. All of these measurements were performed in chip-on-board (COB) test set-up. Loss and isolation of Tx and Rx switch were measured by S-parameters between each single or differential ports using a 4-port network analyzer as shown in Figure 27. The power-handling capability was characterized by P_{1dB}, and measured by the output power corresponding to the input power. For the power measurements, off chip baluns were used to apply the input power and combine the differential power at the input and the output of the differential T/R switch, respectively. The losses of printed circuit board (PCB) and baluns were de-embedded. The measurement for the switch power performance is shown in Figure 28.

The micro-photograph of differential T/R switch design is presented in Figure 29. It was fabricated with a standard 0.18-µm CMOS process, and the total size is 0.58 × 0.35 mm².

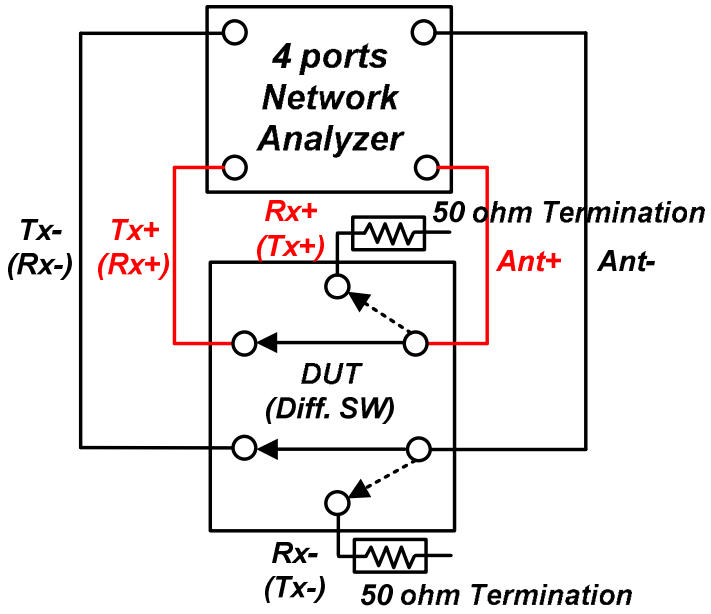


Figure 27. S-parameter measurements for differential T/R switch

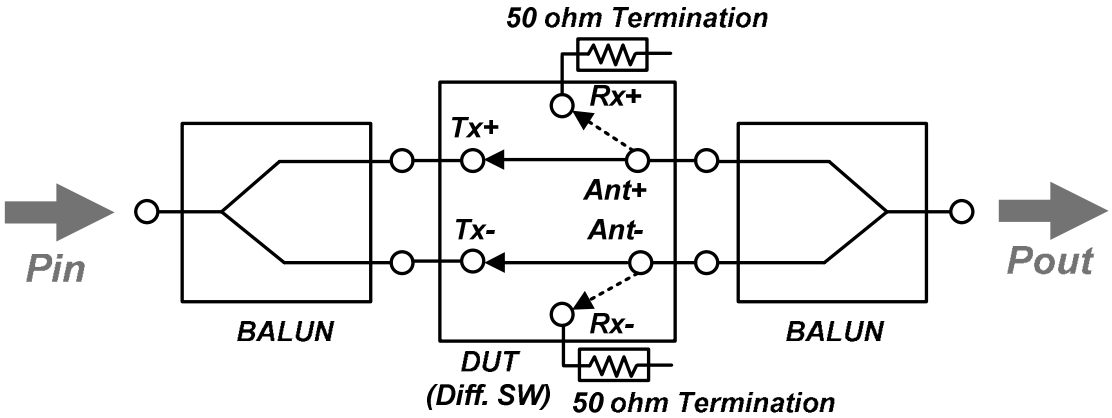


Figure 28. T/R switch power performance measurement set-up

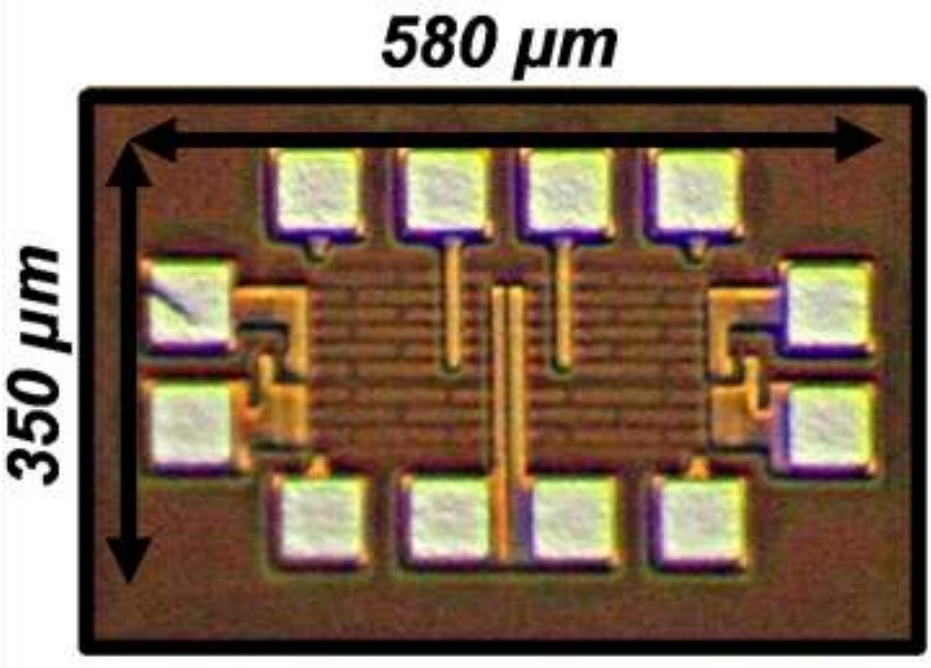


Figure 29. Micro-photograph of differential T/R switch

Figure 30 and 31 show S-parameter measurement results for Tx and Rx modes of the differential switch. At 1.9 GHz, the measured insertion loss of Tx mode is 0.5 dB, return loss is less than 20 dB, and isolation is 23 dB with four stacked shunt switches. On the other hand, insertion loss of 1.1 dB, return loss of 17 dB, and isolation of 33.5 dB has been measured in the Rx mode at 1.9 GHz. In figure 32, the power-handling capability of the differential switch has been compared to that of the single-ended switch. Input P_{1dB} for the single-ended switch was 32.3 dBm with 3-stacked Rx switch devices and input P_{1dB} has been increased by 1.5 dB with the differential switch.

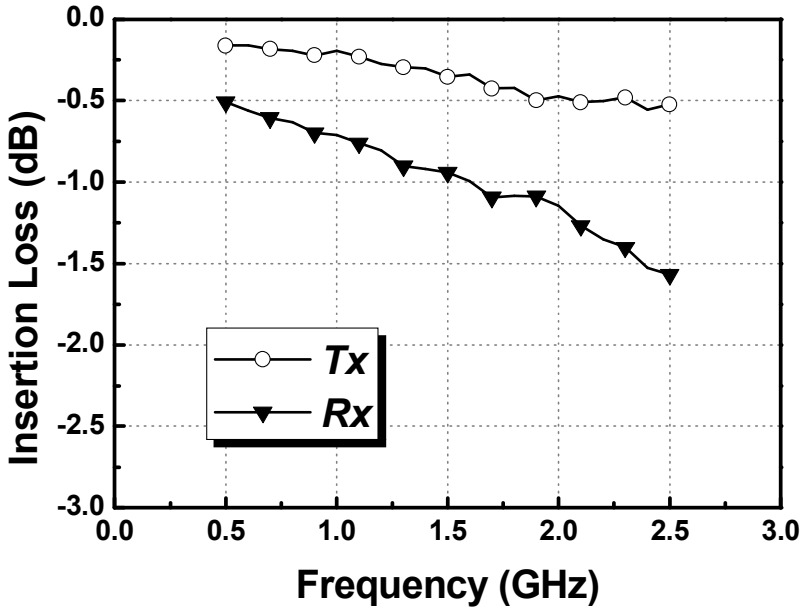


Figure 30. Measured insertion loss of differential T/R switch

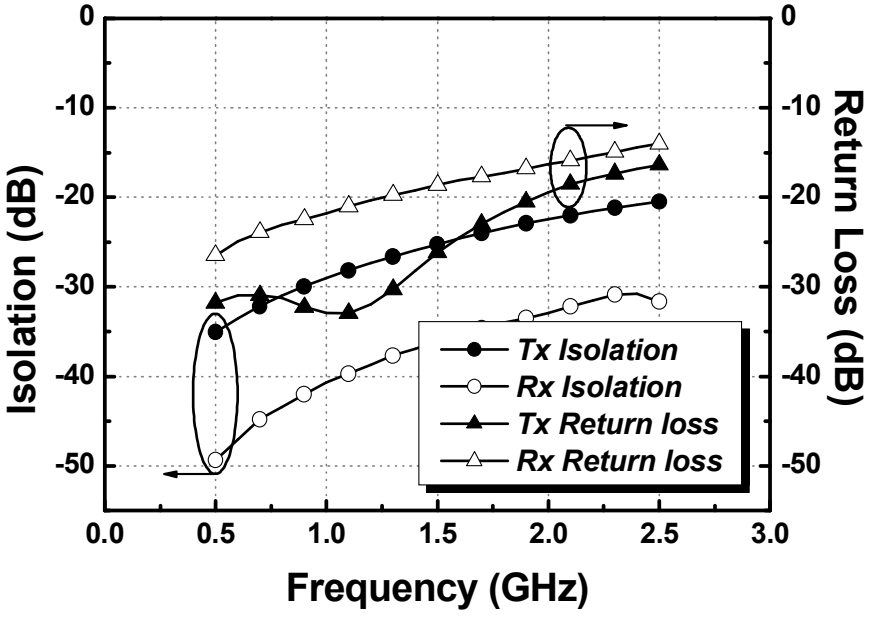


Figure 31. Measured isolation of differential T/R switch

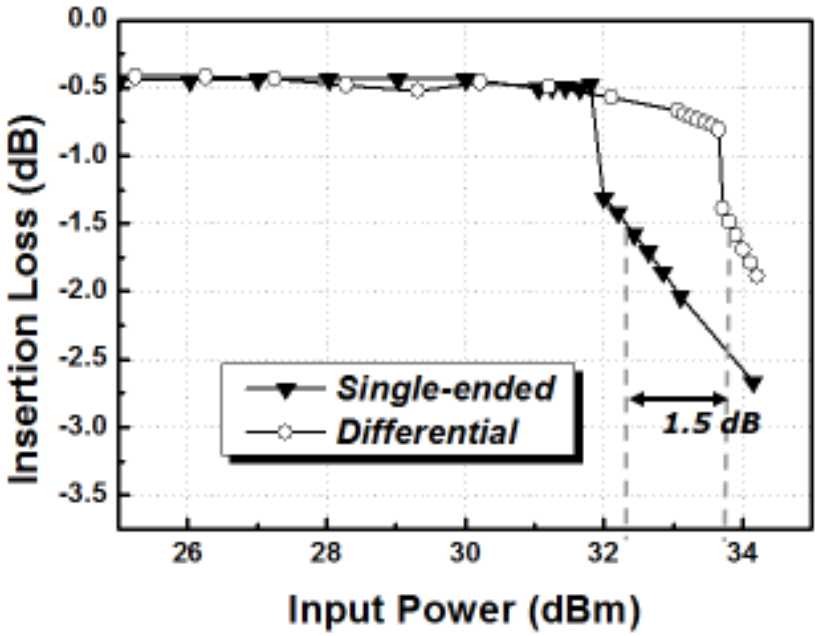


Figure 32. Measured power-handling capability of single-ended and differential T/R switch

4.4. Impedance Transformation Technique for High-Power CMOS T/R Switches

4.4.1. Impedance Transformation Technique

As discussed earlier, the number of stacked transistors is limited because of insertion loss issues at Rx mode and the additional substrate losses through junction diodes [37]. As another approach to improve the power performance of T/R switches, the impedance transformation technique (ITT) can be utilized, instead of increasing the number of stacked switch devices [26]. The large voltage swing which is required to transmit a certain level of power is relaxed by stepping down the load impedance seen by the T/R switch as shown in Figure 33. The amount of voltage reduction can be quantified by equations (3) and (4).

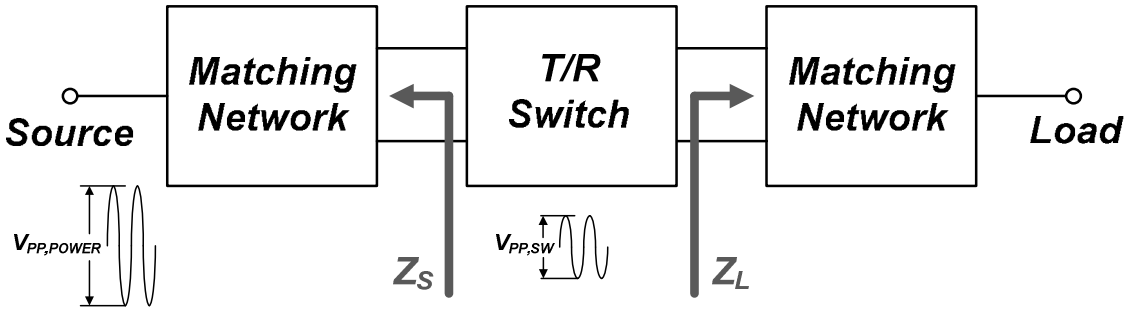


Figure 33. Impedance transformation technique

$$Z_S = Z_L = Z = \frac{V^2}{P} \tag{3}$$

$$\frac{Z}{50\Omega} = \frac{V_{PP,SW}^2}{V_{PP,Power}^2} \tag{4}$$

However, additional matching blocks should be implemented to obtain a desired switch operating impedance for the high-power operation, and this causes an increment in loss. Even worse, the insertion loss of T/R switches is also exacerbated by lowering the switch operating impedance [26].

In order to resolve the loss degradation issue, the ITT is employed aiming to the fully-integrated transmitter front-end. As discussed before, the output matching networks of PAs are very lossy due to the high impedance transformation ratio in the high-power operation. Since the T/R switch positioned right after the PAs, the impedance transformation ratio of the matching network can be reduced by lowering the switch operating impedance. By doing so, not only the efficiency of PA output matching network is enhanced, but also the unnecessary matching block does not need to be implemented to obtain a switch operating impedance. In actual PA designs, the multi-

sectional output impedance matching is required to optimize the efficiency of PA, and utilized frequently [15]. In that case, ITT can be applied by locating the T/R switch between the multi-sections.

In order to match to the 50Ω antenna, however, one matching network is still required between the antenna and the T/R switch, inevitably. In sum, the burden of the PA output matching network is distributed to two matching networks providing desired impedance for the T/R switch. From the perspective of the power-handling capability, the proposed topology is obviously better than the conventional one. However, to justify the usefulness of this topology, the loss of the multi-section matching network should be compared to that of the single-section matching network. In [15], the efficiency of the output matching network of PA was analyzed, and from the analysis, the efficiency of the multi-section matching is better than the efficiency of the single-section matching, in high-power operation. In proposed case, T/R switch insertion loss should be included as well, and the analysis will be shown in the following after dealing with the circuit design.

4.4.2. Schematic and Operations of Proposed CMOS T/R Switch with ITT

A circuit schematic of the single-pole-double-throw (SPDT) T/R switch is shown in Figure 34. Like the previous switch design in Section 4.3, the series-shunt switch structure is chosen [7], and the off-switch in Tx mode, are stacked with multiple thick gate-oxide devices to sustain a high voltage stress [21]. Considering the balance between on-resistance and parasitics of switch device, gate width of 1.5mm for Tx series switch, 1.2mm for Rx series switch, 600μm for Tx shunt switch, and 200μm for Rx shunt switch have been chosen.

As mentioned in Section 4.4.1, an output matching network of a PA can be utilized as the matching networks by splitting it into two matching networks as shown in Figure 34. Since the impedance looking into the PA ooutput matching network (R_{PA}) are typically low, especially for the Watt-level high-power PAs, to drive more current, the switch operating impedance (R_{SW}) can be adjusted between the R_{PA} and the antenna impedance 50Ω. That is, the low R_{PA} is transformed to the R_{SW} with the first matching network (MN1 in Figure 34) and it is matched to the 50Ω antenna by the second matching network (MN2 in Figure 34). By doing so, not only the total insertion loss can be optimized by the multi-sectional impedance matching, also a desired R_{SW} can be obtained to enhance the switch power-handling capability.

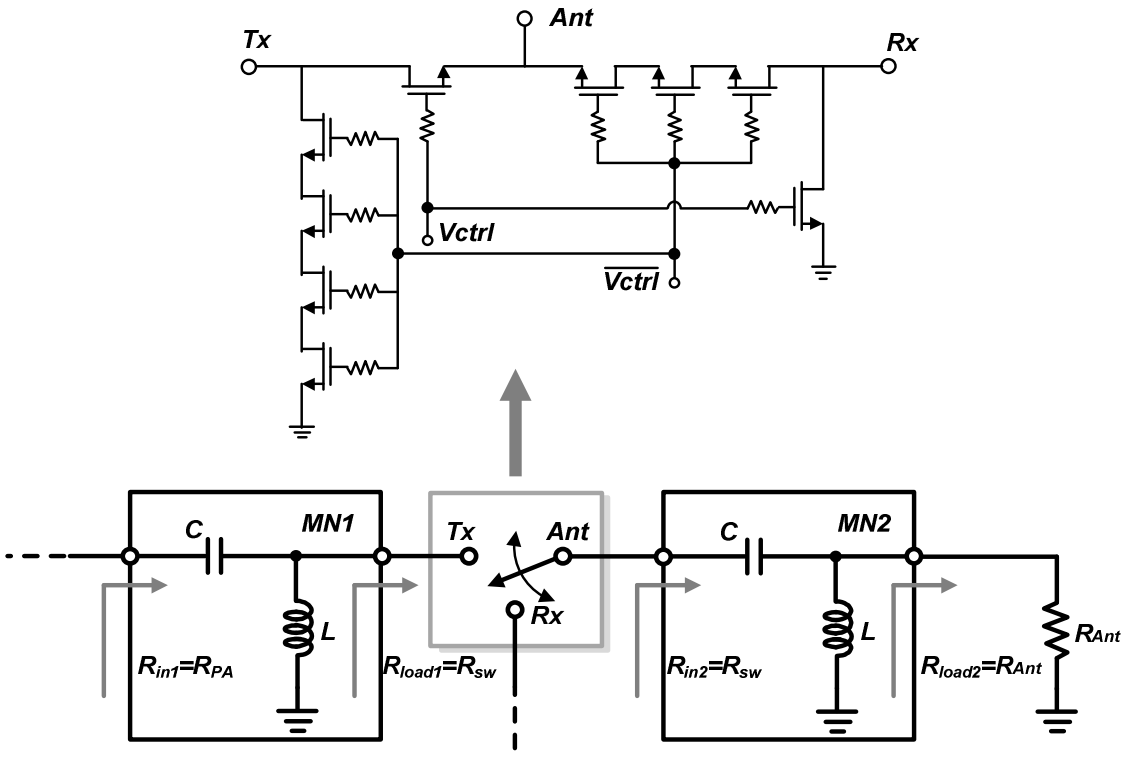


Figure 34. Schematic of the CMOS T/R switch with the impedance transformation technique

4.4.3. Insertion Loss Analysis

From the perspective of power-handling capability of the T/R switches, the ITT has an obvious advantage reducing the large voltage swing over off-switch devices. However, the insertion loss of T/R switches with the ITT has to be preserved while improving the power performance. In this section, the total insertion loss and the power-handling capability of the T/R switch including multi-section PA output matching network are analyzed and compared to those of the conventional structure which consists of a T/R switch and a single-section matching network.

The PA output matching can be realized either by using LC, transformer, or transmission lines as occasion demands. Among these candidates, the LC-type matching is assumed in this analysis since it is the most straightforward impedance matching method, and widely used. A simple schematic of the LC matching is shown in Figure 34, and the efficiency of the matching network, defined by the ratio between the input power and the power delivered to the load, is calculated by the equation (5), where Q is the quality factor of the inductor used in the matching network and r is the impedance transformation ratio which is R_{load}/R_{in} [15].

$$\eta_{LC} = \frac{Q^2 + 1}{Q^2 + \frac{r + \sqrt{r^2 + 4Q^2(r-1)}}{2}} \tag{5}$$

On the other hand, the efficiency of T/R switch is calculated by using a simplified device model, based on the physical structure of DNW devices, which is illustrated in Figure 35 [10]. The derived efficiency is presented in the equation (8), where ω is the operating frequency.

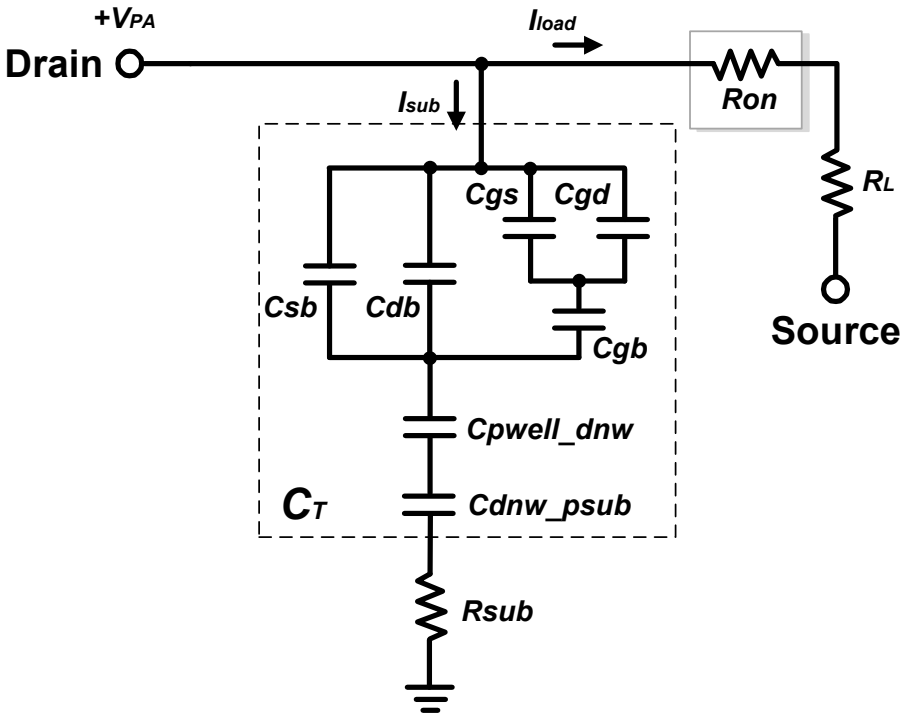


Figure 35. Simplified equivalent device model of DNW device

$$P_{diss} = I_{load}{}^2 R_{on} + I_{sub}{}^2 R_{sub} \tag{6}$$

$$P_o = I_{load}{}^2 \frac{R_L}{2} \tag{7}$$

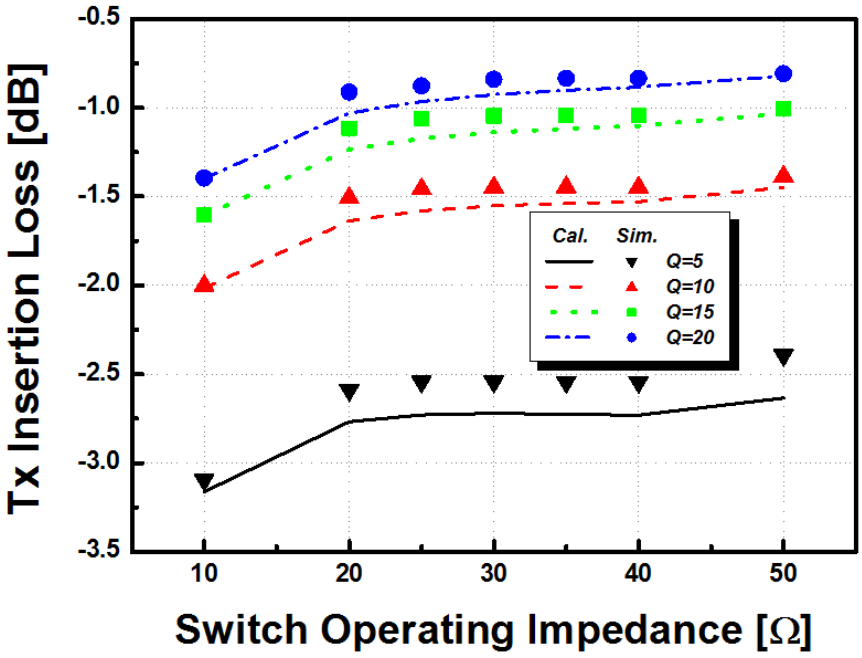
$$\eta_{SW} = \frac{P_o}{P_{diss} + P_o} = \frac{R_{SW}}{2R_{on} + 2R_{sub}(\omega C_T)^2 \dfrac{\left(\frac{1}{2}R_{SW} + R_{on}\right)^2}{1 + \left(\omega C_T R_{sub}\right)^2} + R_{SW}} \tag{8}$$

As illustrated in Figure 36 (a), Tx insertion loss is reasonably even over the various R_{SW}, compensating the degraded loss of T/R switch with the multi-section impedance matching. However, Rx insertion loss is inevitably worse than that of the T/R switch with a single matching network as shown in Figure 36 (b), since an additional matching is implemented between the antenna and the T/R switch. Moreover, the loss is degraded monotonously as R_{SW} decreases because the loss of the matching gets worse as the R_{SW} lowers, increasing the impedance transformation ratio of the matching network. Since the high Rx insertion loss causes deterioration in noise figure of the receiver chain, the degraded loss must be compensated. This can be done by reducing the number of stacked devices on the Rx series path, as a result, the power performance and the insertion loss of the T/R switch can be balanced by selecting an optimal R_{SW}, and the number of stacked devices.

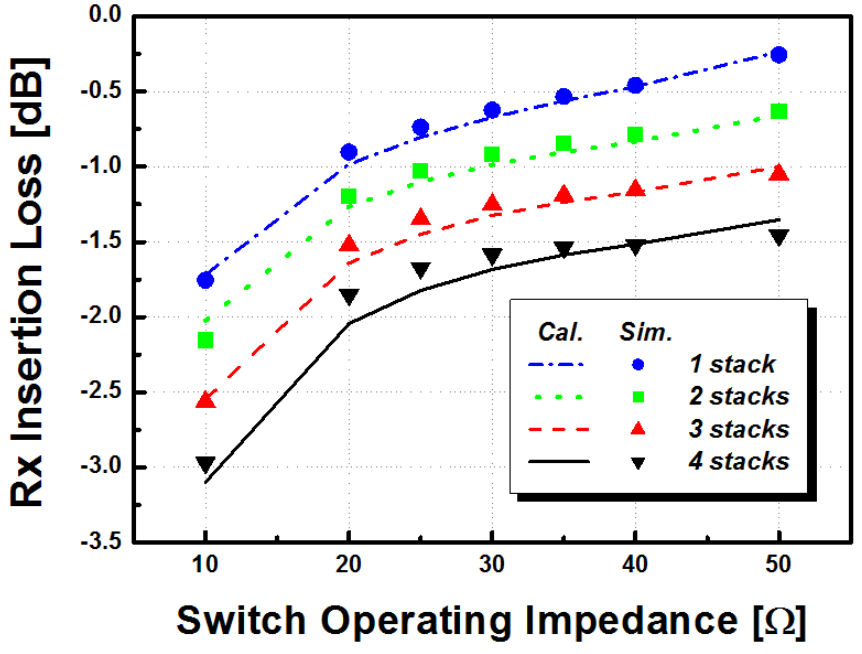
4.4.4. Design Example and Measurement Results

As a design example, an SPDT T/R switch was fabricated in 0.18-μm CMOS process. All measurements were done in chip-on-board (COB) setting, and the load-pull measurements were executed with two impedance tuners at input and output sides of the T/R switch to adjust the impedance seen by the source/load of T/R switch. The block diagram for the measurement setting is shown in Figure 37.

Meanwhile, according to the analyses and the simulations addressed in earlier Section, one stack of device is not enough to handle a Watt-level power. Also, the degradation in Rx insertion loss is too large, when four devices are stacked, comparing to the amount of power performance improvement as shown in Figure 36 (a) and (b).



(a)



(b)

Figure 36. Calculated and simulated insertion loss (50Ω of R_{SW} indicates the single-section matching case) (a) Tx insertion loss (b) Rx insertion loss

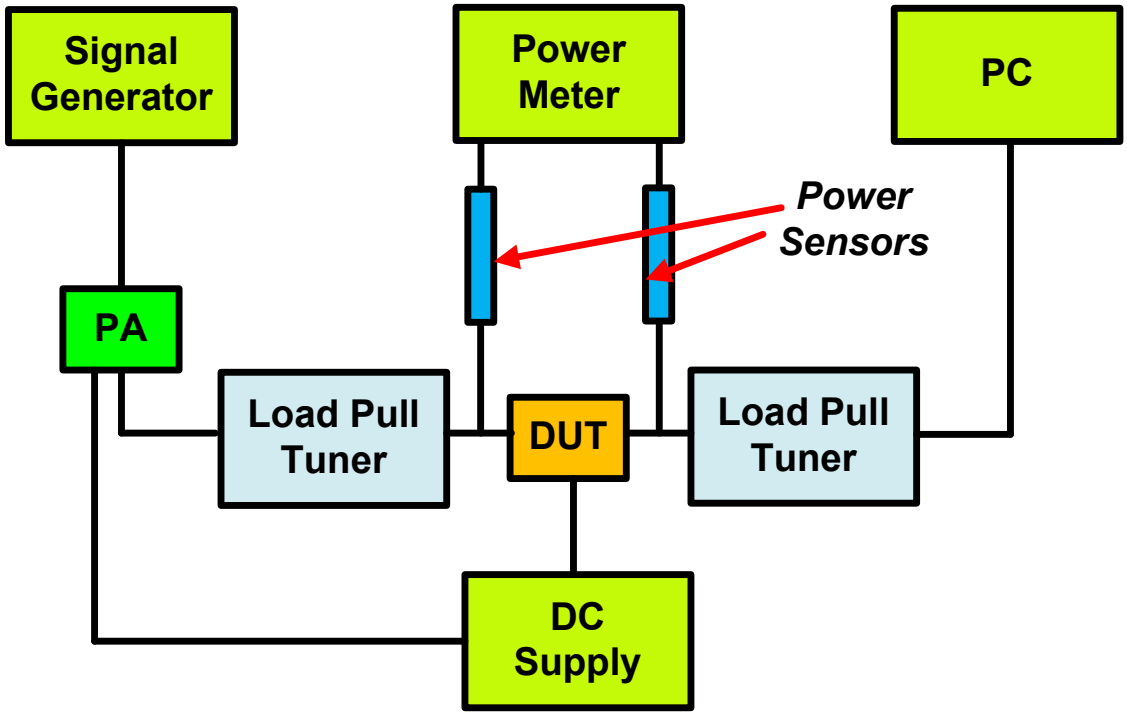


Figure 37. Load-pull measurement setting for T/R switch with ITT

Therefore, in actual implementation, three devices were stacked on Rx series path targeting the P_{1dB} higher than 2-W. Because of the matching issue and the limitation on the PA output power, the measurements were only possible as far as around 30Ω and P_{1dB} of the T/R switch has increased by lowering the R_{SW}. With 35Ω of R_{SW}, the measured P_{1dB} was over 2-W, 33.7 dBm, after de-embedding the board loss as presented in Figure 38. The simulated total losses including matching networks were 1.5 dB, and 1.2 dB in Tx and Rx mode, respectively, when Q of inductors used in the matching networks is assumed as 10, as shown in Fig. 36 (a) and (b). In Figure 39, the micro-photo of the fabricated T/R switch is presented.

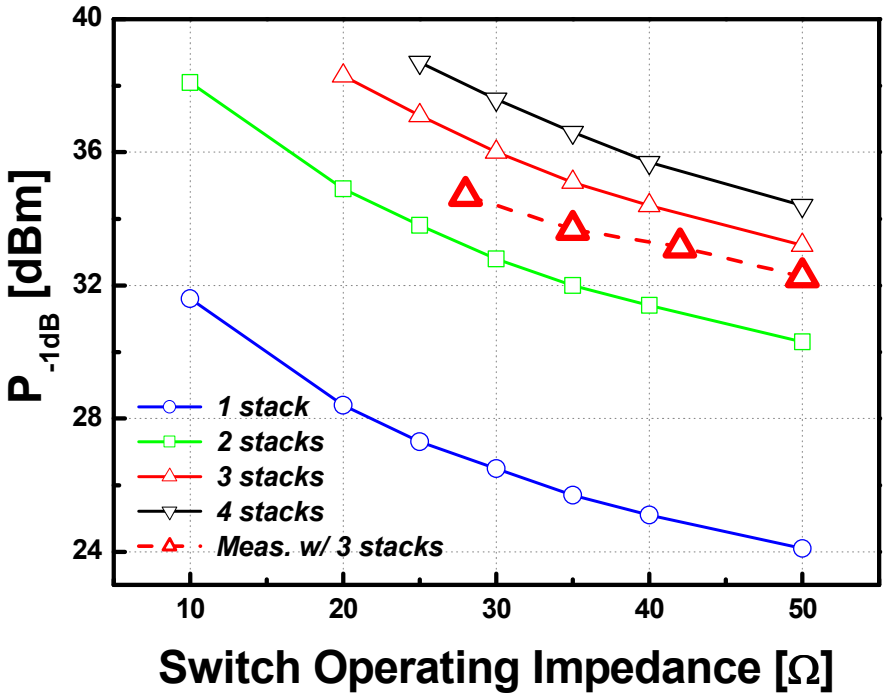


Figure 38. Simulated and measured P_{1dB} (Q of inductors is assumed as 10)

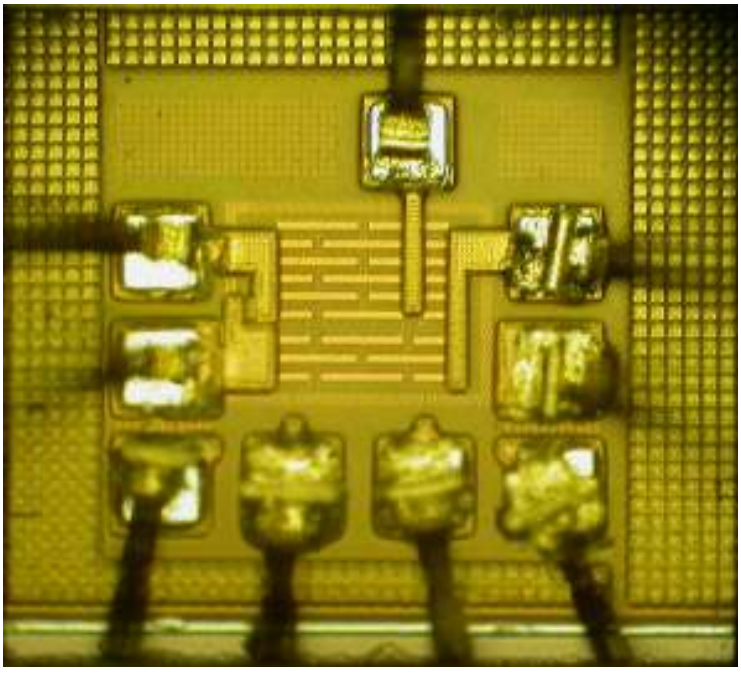


Figure 39. Micro-photo of the SPDT T/R switch (410µm x 370µm)

4.5. High-Power CMOS T/R Switches with Feed-Forward Capacitors

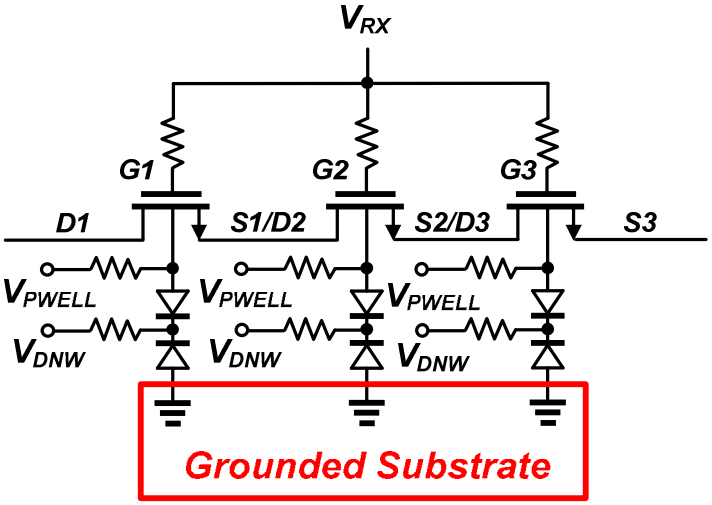
4.5.1. Feed-Forward Capacitors

As discussed earlier, the voltage difference between the gate and source/drain of the T/R switch device in off-state should not be larger than the threshold voltage of the device, diode turn-on voltage, and device breakdown voltage. Thus, while the multi-stack switch structure is widely utilized, the key concern in designing a T/R switch is how to distribute the voltage swings over the multiple switch devices evenly. Based on the idea, an effective method to enhance the linearity of the T/R switch is to use feed-forward capacitors [28].

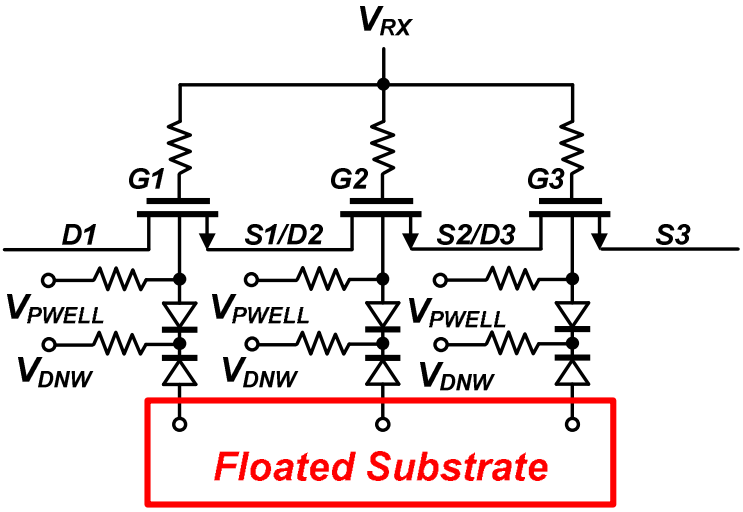
The parasitic capacitors between the gate and drain/source, and parasitic components in substrate of the multi-stacked switch devices cause the voltage swing at the antenna port to be unequally distributed to the source-gate and gate-drain of the stacked off-switch devices. In other words, the advantage of multi-stacked switch structure cannot be maximized due to the parasitic components. The feed-forward capacitors are utilized to mitigate this problem. By balancing the total impedance values between the junctions with the feed-forward capacitors, the voltage stress can be distributed effectively.

As the number of stacked devices increases, the substrate network dominates the switch power performance. For example, three stacked T/R switches with the grounded substrate and with the floated substrate are shown in Figure 40 (a) and (b), respectively, to identify the effect of substrate network on the switch power performance. As shown in Figure 41 (a) and (b), voltage swing is not distributed evenly for the stacked switch with the grounded substrate, while the swing is effectively distributed over the multiple devices for the switch with the floated substrate. As a result, not only the insertion loss,

but power-handling capability is also worse in the case of switch with the grounded substrate than that with the floated substrate, as demonstrated in Figure 42. Since the actual CMOS devices have a relatively low substrate resistance, the grounded substrate case is closer to the reality. Therefore, feed-forward capacitors are required to balance the voltage stresses over the multi-stacked T/R switch devices.

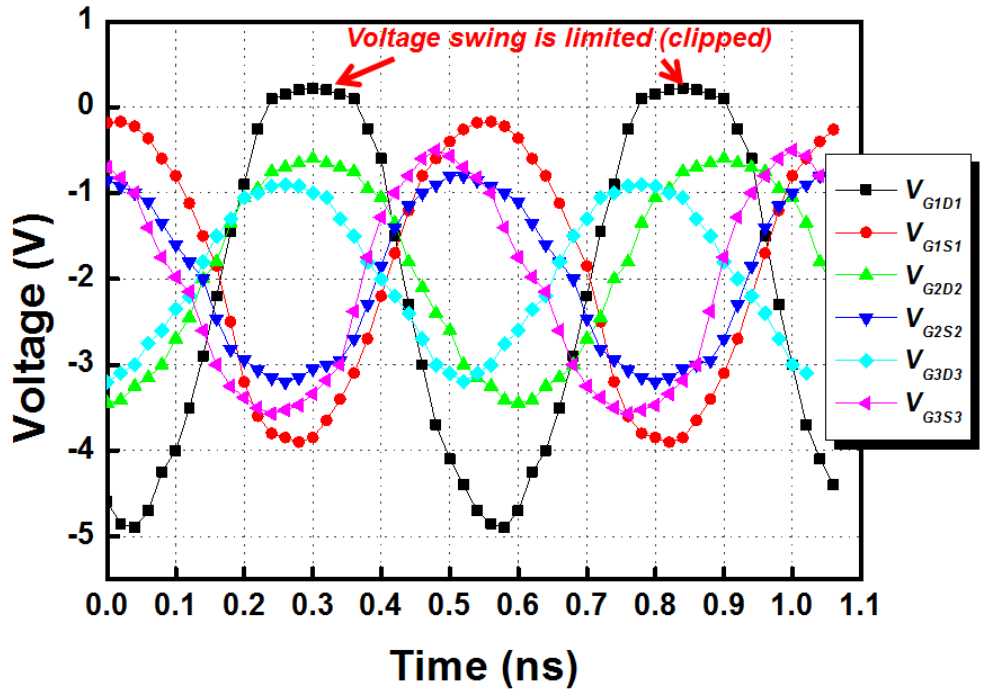


(a)

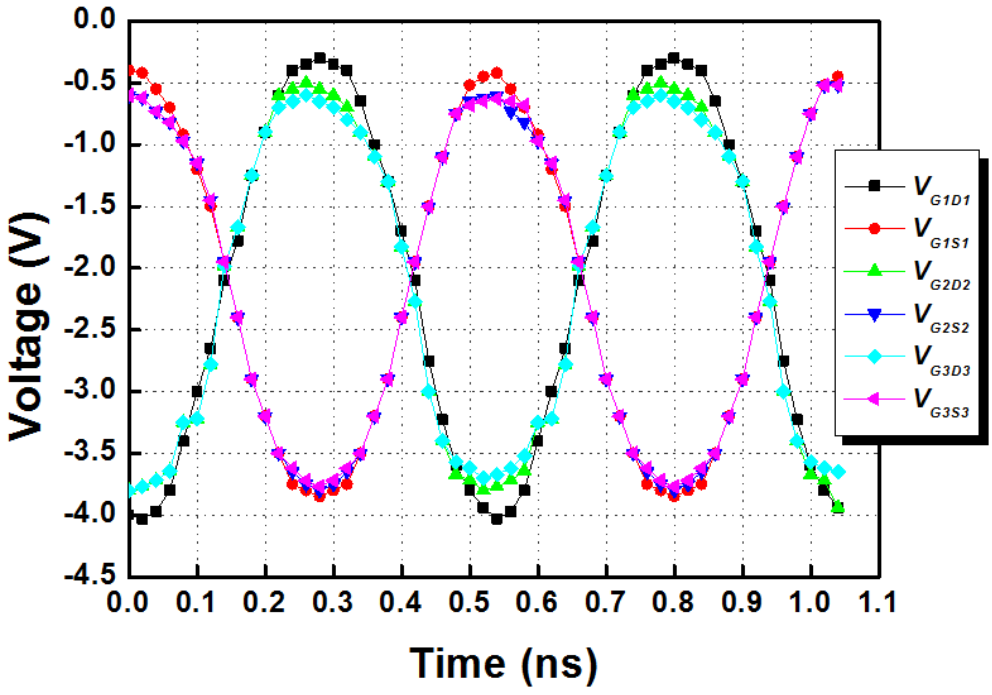


(b)

Figure 40. Effect of substrate network on switch power-handling capability: Multi-stacked T/R switch (a) with the grounded substrate (b) with the floated substrate



(a)



(b)

Figure 41. Voltage distribution of multi-stacked switch: (a) with the grounded substrate (b) with the floated substrate

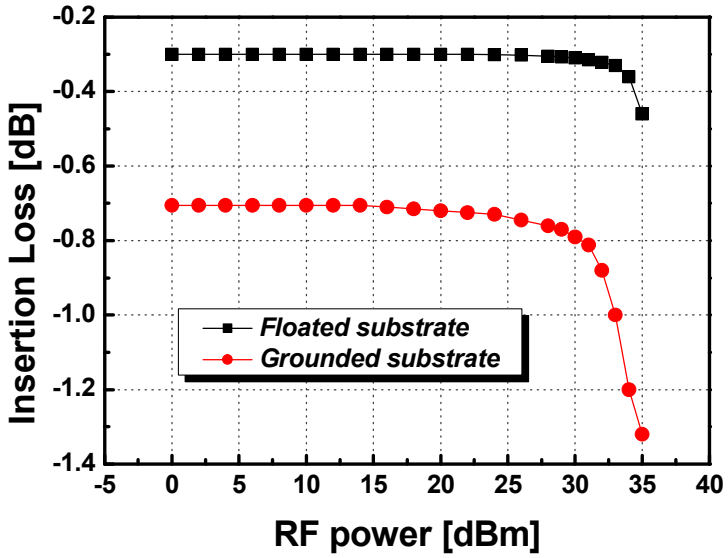


Figure 42. Power-handling capability of switch with two types of substrate

4.5.2. CMOS T/R Switch Design with Feed-Forward Capacitors

Because the even voltage distribution is getting harder as the number of stacked devices increases, the enhancement of switch power-handling capability by increasing the number of stacked devices is very limited. Thus, stacking devices is meaningless from a certain point.

In proposed designs, feed-forward capacitors are implemented for two, three, and four stacks switch devices to distribute the voltage stress effectively. In Figure 43, schematics for the proposed design are illustrated. As shown in the Figure, one, three, and six feed-forward capacitors have been employed for two, three, and four stacks, respectively. To maximize the power performance of the proposed T/R switch, negative bias at P-well ports and positive bias at DNW ports have been applied, as well.

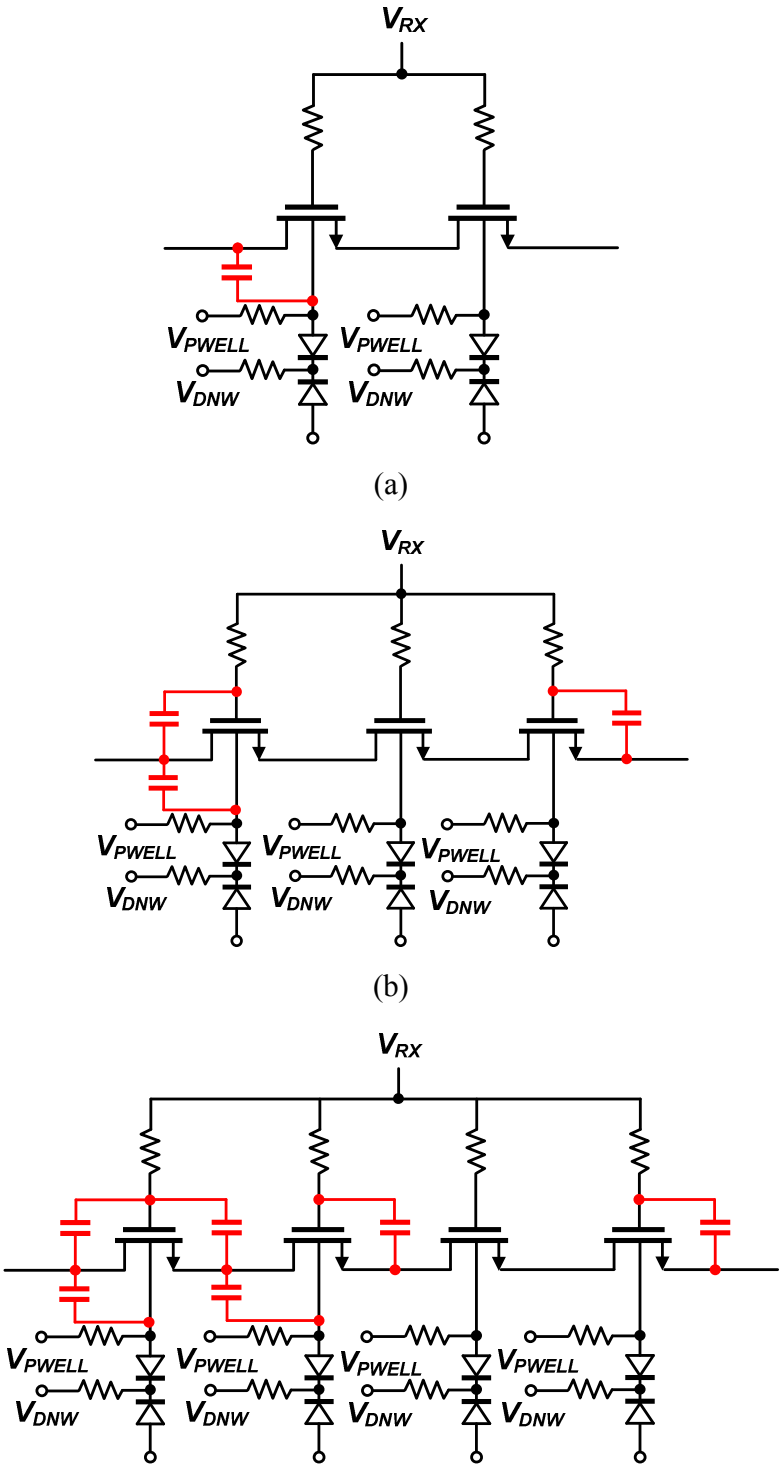


Figure 43. Multi-stacked switch with feed-forward capacitors: (a) 2 stacks (b) 3 stacks (c) 4 stacks

The simulated switch power-handling capability is shown in Figure 44. According to the results, power performance of switch is improved with the feed-forward capacitors, and the gap of improvement is also getting wider as the number of stacks increases. In other words, even voltage distribution is getting harder as the number of stacked devices increases, and the advantage of stacking can be taken by utilizing the feed-forward capacitors. However, the Rx insertion loss is still sacrificed more with the more stacked devices, trade-off between insertion loss and power performance should be considered here. Furthermore, impedance matching at Tx, Rx, and antenna ports should be implemented carefully, considering the effects of feed-forward capacitors.

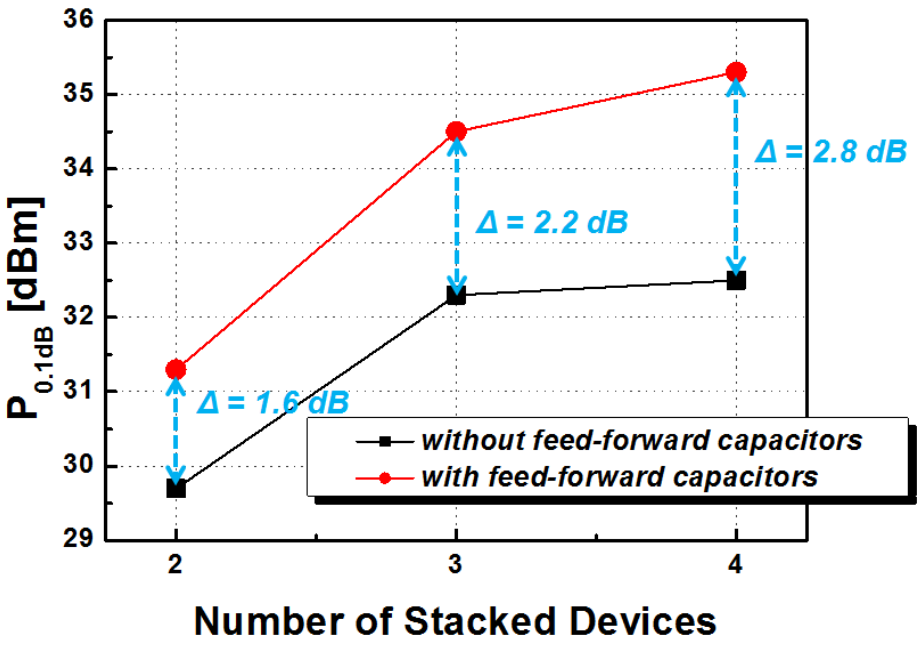


Figure 44. T/R switch power performance improvement with the feed-forward capacitors

4.6. Conclusions

In this Chapter, high-power handling CMOS T/R switch designs, maintaining reasonable insertion losses, have been presented with the substrate structure analysis of CMOS device.

Mainly, power-handling capability of T/R switch is improved by reducing the voltage stress over the off-switch devices. To relieve the voltage stress, as the first approach, the differential T/R switch structure has been introduced. With the structure, voltage stress is divided in half with two identical signal paths enhancing the switch P_{1dB}. Also, the possibility to be integrated in the fully-differential transmitter makes this work more valuable.

Secondly, impedance transformation technique using the PA output matching networks has been introduced. With the PA output matching networks, additional lossy matching blocks are not required while the switch operating impedance is lowered. By doing so, efficiency and power-handling capability of transmitter module can be secured at the same time. Furthermore, this technique is also valid for the integrated transmitter front-end module which includes PA and T/R switch.

Lastly, T/R switch with the feed-forward capacitors has been presented. For high-power applications, transistor stacking is essential. However, power performance is not improved easily by simply increasing the number of stacked devices since the voltage stress is not distributed over the multiple devices effectively. As the number of stacks increases, the feed-forward capacitors are required to distribute the voltage stress evenly. With the feed-forward capacitors, the advantage of device stacking can be fully taken.

The performance results of the proposed work are summarized and compared to other T/R switch works in Table 3.

Table 3. Summary and comparison of CMOS RF T/R switches

Technology	Frequency	IL	Linearity (P_{1dB})	Reference
0.18-µm triple well CMOS	1.9 GHz	0.4 dB (Tx) 1.1 dB (Rx)	32.3 dBm	This work (single-ended)
0.18-µm triple well CMOS	1.9 GHz	0.5 dB (Tx) 1.1 dB (Rx)	33.8 dBm	This work (differential)
0.18-µm triple well CMOS	1.9 GHz	1.4 dB* (Tx) 1.2 dB* (Rx)	33.7 dBm	This work (ITT)
0.18-µm triple well CMOS	1.9 GHz	1.5 dB (Tx) 1.8 dB (Rx)	31.5 dBm	[46]
0.18-µm triple well CMOS	1.9 GHz	2.0 dB (Tx) 2.0 dB (Tx)	27 dBm	[47]
90-nm CMOS	2.4 GHz	0.4 dB (Tx) <0.2 dB (Rx)	31 dBm	[30]
0.18-µm triple well CMOS	1.8 GHz	0.75 dB (Tx) 1.1 dB (Rx)	33 dBm	[9]
0.18-µm triple well CMOS	1.9 GHz	1.5 dB (Tx) 1.9 dB (Rx)	33.5 dBm	[29]
0.13-µm triple well CMOS	0.9 GHz	0.5 dB (Tx) 1.0 dB (Rx)	31.3 dBm	[28]
0.18-µm triple well CMOS	5.2 GHz	1.52 dB (Tx) 1.42 dB (Rx)	28 dBm	[27]
0.13-µm triple well CMOS	10 GHz	0.5-0.7 dB (Tx) 0.5-0.7 dB (Rx)	26.2 dBm	[48]
0.13-µm triple well CMOS	20 GHz	2.0 dB (Tx) 2.0 dB (Rx)	27 dBm	[3]

CHAPTER 5
HIGH-POWER AND HIGHLY EFFICIENT TRANSMITTER FRONT-END

5.1. Introduction

Since the required output powers of the transmitters for mobile applications are relatively high due to the long communication distances, PAs should be able to generate a high power. However, even if high power is generated from the PAs, the power cannot be transmitted to the air efficiently if T/R switch at the end of the transmitter cannot properly handle the high power. Therefore, both of these two high-power-handling components need to be able to handle the large power with as small losses and distortions as possible.

In this Chapter, a design of the transmitter front-end module which employs the proposed structure – a differential T/R switch with the multi-section PA output matching – is discussed. The block diagram of the transmitter front-end module is shown in Figure 45. In Section 5.2, an overview of the proposed transmitter front-end is presented. In Section 5.3, the design of matching networks that have been utilized in the module and their losses are addressed, and practical saturated PA design is followed in Section 5.4. In Section 5.5, T/R switch control circuitry to generate the negative supply voltage is presented. Lastly, simulation and measurement results are presented in Section 5.6. All of the RF and analog functional blocks have been designed by using a standard 0.18-μm bulk CMOS process.

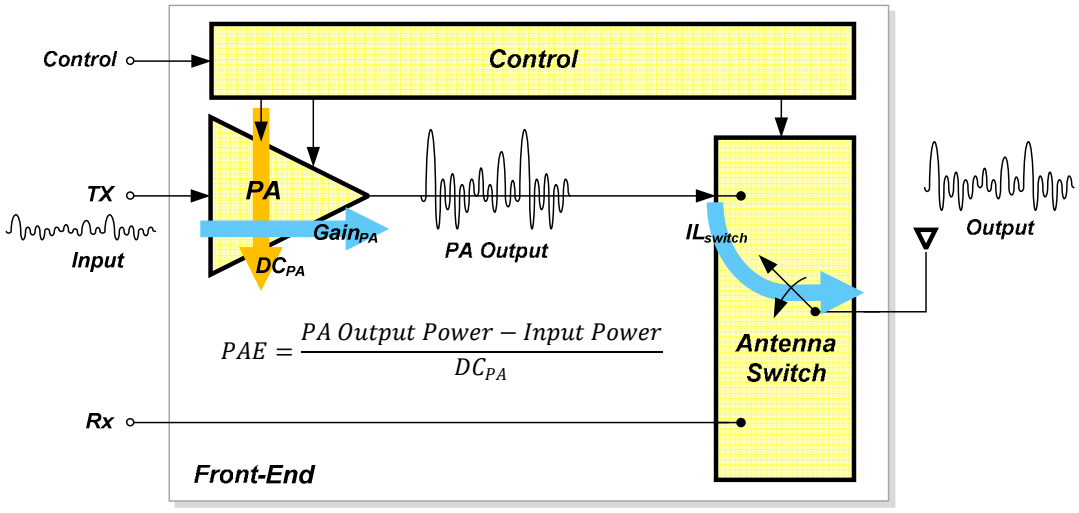
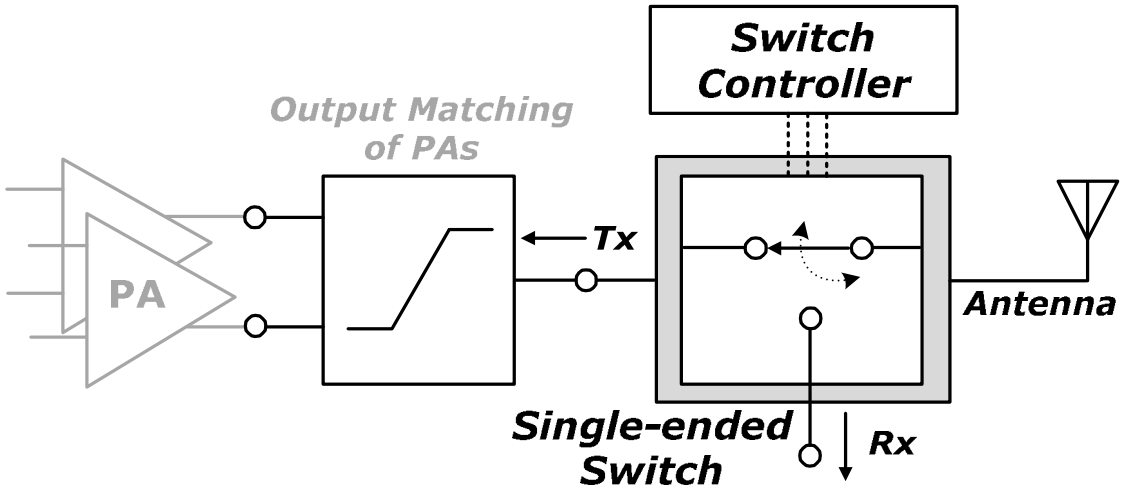


Figure 45. Block diagram of the transmitter front-end module

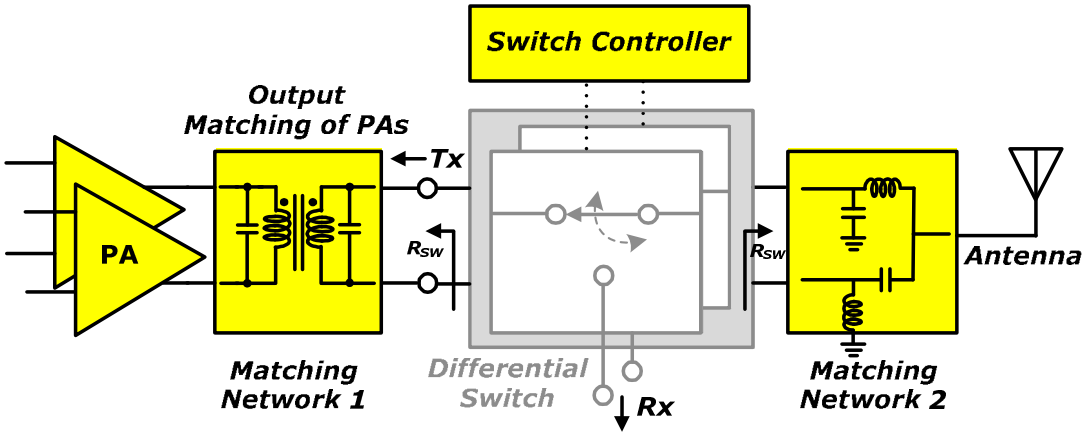
5.2. High-Power and Highly Efficient Transmitter Front-End Module

In the research contributions introduced earlier in this dissertation, the CMOS T/R switch with the differential topology was proposed to enhance the power-handling capability of the T/R switch by relieving the voltage swing over off-switches [37]. Also, the switch power performance improvement by lowering the switch operating impedance, R_{SW}, was presented as well. Combining these advantages, unlike the conventional front-end structure which is shown in Figure 46 (a), a multi-section PA output matching network is implemented with the differential T/R switch, as shown in Figure 46 (b), to maximize the power-handling capability of T/R switch. The reduced voltage swings are demonstrated in Figure 47, and the improved switch power performance is presented in Figure 48. With this topology, not only the power performance of T/R switches, but also the total efficiency of the entire transmitter front-end module which consists of PAs and

T/R switches, can be optimized by controlling the R_{SW}, since the efficiencies of the matching networks depend on their impedance transformation ratios.



(a)



(b)

Figure 46. Block diagram of transmitter front-end: (a) conventional structure with a single-ended switch and (b) proposed structure with a differential switch employing ITT

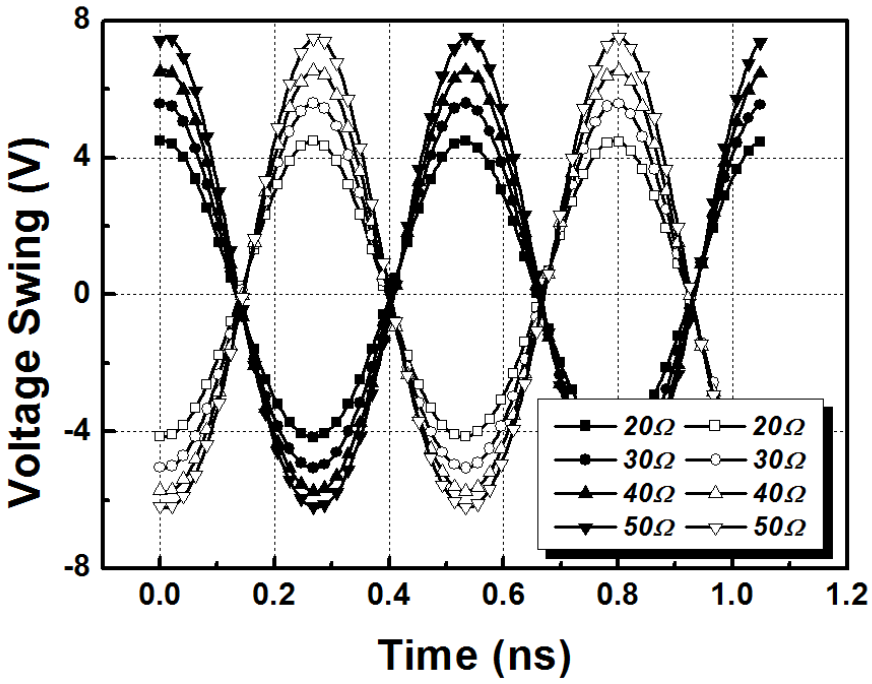


Figure 47. Simulated voltage swing over each single-ended switch (vacant symbols are for path1, and solid symbols are for path2, 33 dBm of input power is applied at 1.9 GHz)

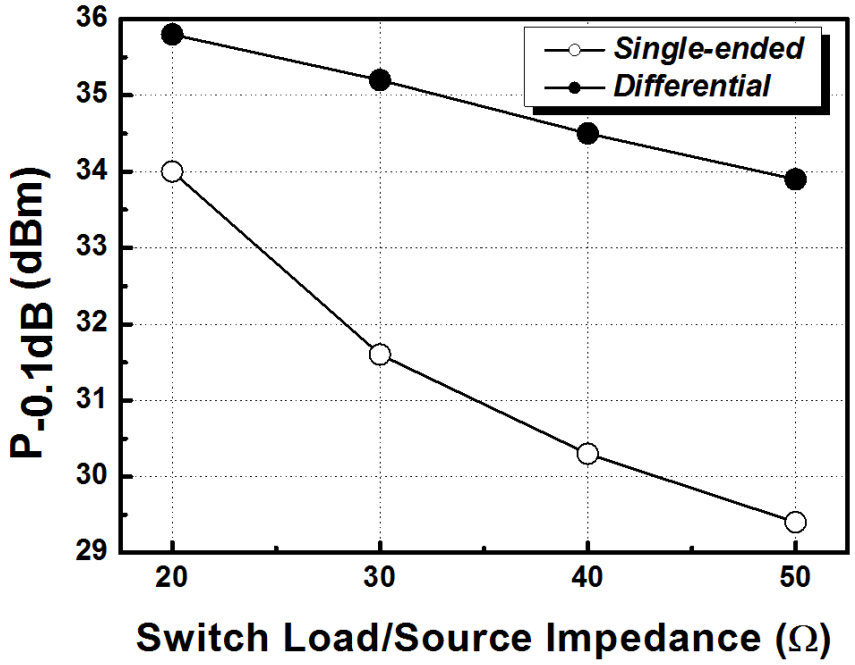


Figure 48. Simulated $P_{0.1dB}$ of antenna switches (control voltages are 3V/-2V at 1.9 GHz)

For the practical implementation, a transformer is utilized as the matching network at the transmitter side (MN1 in Figure 46 (b)). While the transformer functions as a matching network, it also combines output powers transmitted from multiple PAs compactly, comparing to the LC counterpart. Since power combining is essential to transmit higher power than a Watt-level, transformer can be a good candidate for the output matching network of high-power PAs. For another matching network between T/R switch an antenna (MN2 in Figure 46 (b)), LC balun is implemented. It converts a differential port to a single-ended port to match the unbalanced antenna as well as transforms impedance. LC balun is preferred to transformer for this matching since it is easy to achieve the accurate switch operating impedance with the LC balun by manipulating it.

Even though all of these functions – power combining and converting from differential to single-ended – can be done by one matching network [13], multi-section matching is chosen to lower the switch operating impedance, in other words, to apply the impedance transformation technique. In spite of the additional matching network in the proposed structure, loss of the multi-section matching network can be lower than that of the single section matching network, according to its impedance transformation ratio and transformation efficiency [15]. Proving that, the losses of the proposed matching blocks are analyzed and compared to the loss of the single matching case in following Sections.

5.3. Design of Matching Networks

5.3.1. On-Chip Transformer

5.3.1.1. Transformer Design

For the first matching network between the PA and the T/R switch, a transformer is selected. In order to generate a Watt-level output power, multiple output powers from PA cells are usually combined. By implementing the transformer as the output matching network of the PA, both power combining and impedance transformation are possible at the same time. Although LC networks can be utilized to fulfill these functions as well, the size is getting too bulky as the number of PA cells increases. In case of the proposed design, two pairs of differential PA output should be combined to generate a sufficient power, and four inductors are required to combine the powers with the LC network.

In implementing the output matching network of the high-power PAs, the most important design concern is the efficiency. First of all, the efficiency of the output matching network is poor due to the high impedance transformation ratio. Secondly, when the output power reaches Watt-level, even a small parasitic resistance at the output matching network can cause a huge loss since the current flowing through the network can hit the Ampere-level easily.

Hence, in the proposed design, the burden of large impedance transformation ratio is distributed to multi-section matching networks. Moreover, the matching network is designed to minimize the DC resistance to enhance the efficiency. Figure 49 shows the cross-sectional view of the standard CMOS process which was used in the proposed design. In order to minimize the DC resistance, both of top two metals, a 3-mm of

alumina MA layer and a 4-mm of copper E1 layer are utilized to implement transformer windings.

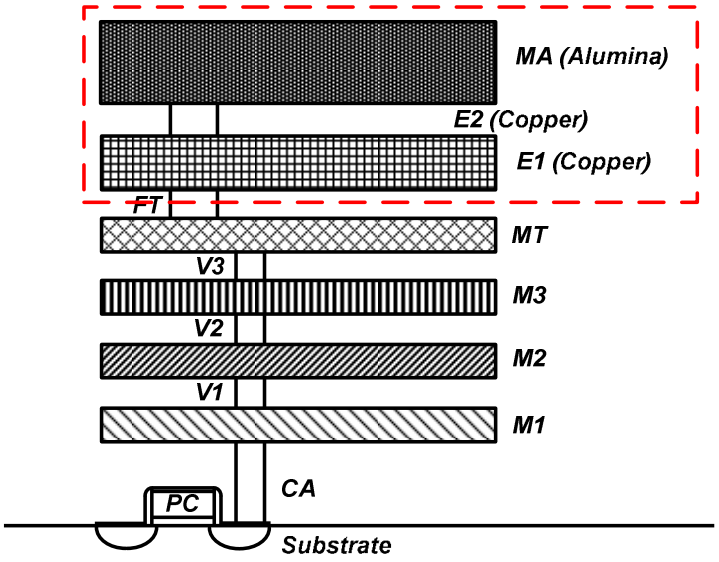


Figure 49. Cross-sectional view of the metal layers in IBM CMOS process

5.3.1.2. Transformer Efficiency

Figure 50(a) shows an 1:n transformer, and the transformer is modeled by equivalent T-model as shown in Figure 50(b), for the efficiency analysis. From the T-model analysis, the efficiency is influenced by various parameters, such as Q-factors of inductor windings, turn ratio, n, and coupling coefficient, k. Q-factors of primary and secondary winding, Q_1 and Q_2, are defined by inductances of windings, L_1 and L_2, and parasitic resistances of the windings, R_1 and R_2. Coupling coefficient k is related to mutual inductance, M, and inductances of primary/secondary windings, and calculated by an equation $k = M / \sqrt{L_1 L_2}$ to validate this T-model simplification. Also, there is one more assumption, $n = \sqrt{L_2 / L_1}$, in this analysis. In order to analyze the efficiency of transformer only, tuning capacitors to optimize the matching and loss are not included. From this model, R_{in} is derived to define the impedance transformation ratio r, R_{load}/R_{in}, and total efficiency is solved by circuit

analysis below. As obtained from previous work [33], R_{in} and η are represented by equation (9) and (13), respectively. P_{R1}, P_{R2}, and P_L represent dissipated power due to R_1, and R_2, and delivered power to load, respectively. As shown in Figure 51(a), a fixed load impedance is transformed to lower R_{in}, as turn ratio increases, generating higher output power. However, Figure 51(b) and (c) show that the efficiency of transformer is worsened by the increased turn ratio, resulting in the high impedance transformation ratio.

In sum, a high turn ratio is demanded to generate a high power, and it causes the loss degradation. For the proposed structure, the required low R_{in} can be obtained with a relatively small turn ratio, by reducing the switch operating impedance. By doing so, efficiency of the transformer can be enhanced.

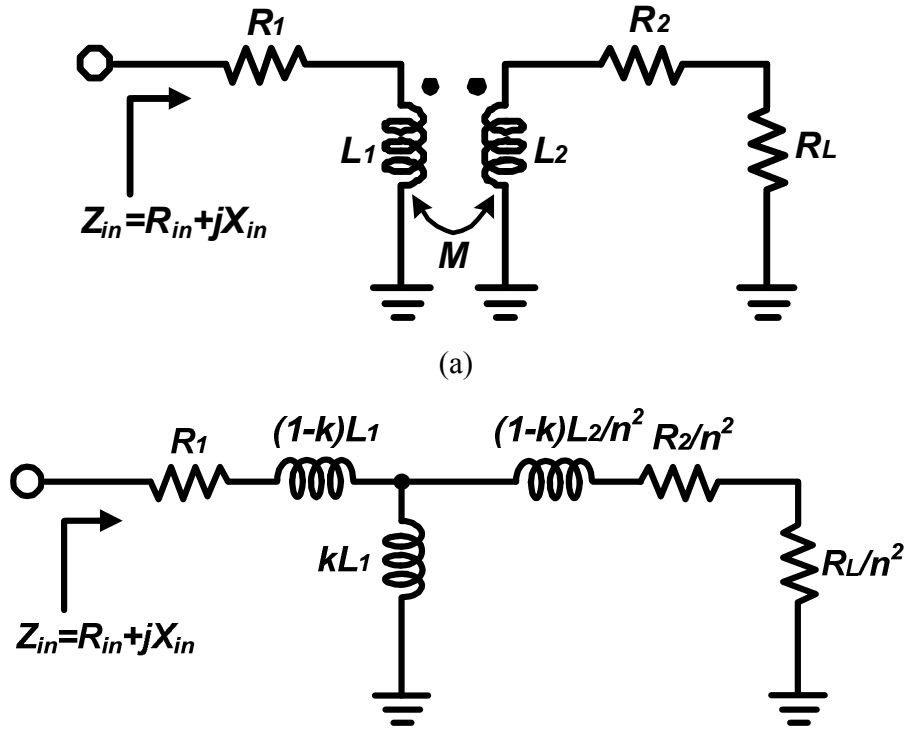


Figure 50. (a) 1:n transformer model and (b) 1:n Transformer equivalent T-model

$$R_{in} = R_1 + \frac{\omega^2 n^2 k^2 L_1^2 (R_2 + R_L)}{(R_2 + R_L)^2 + (\omega n^2 L_1)^2} \tag{9}$$

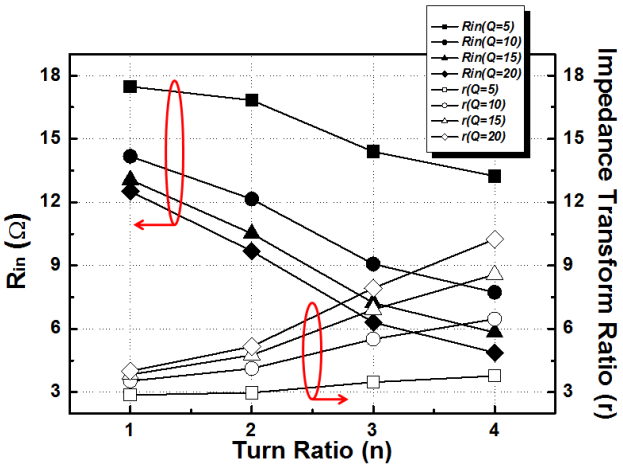
$$P_{R1} = \frac{R_1}{R_{in}} P_{in} \tag{10}$$

$$P_{R2} = \frac{(\omega n^2 k L_1)^2}{(R_2 + R_L)^2 + (\omega n^2 L_1)^2} \cdot \frac{(R_2 / n^2)}{R_{in}} P_{in} \tag{11}$$

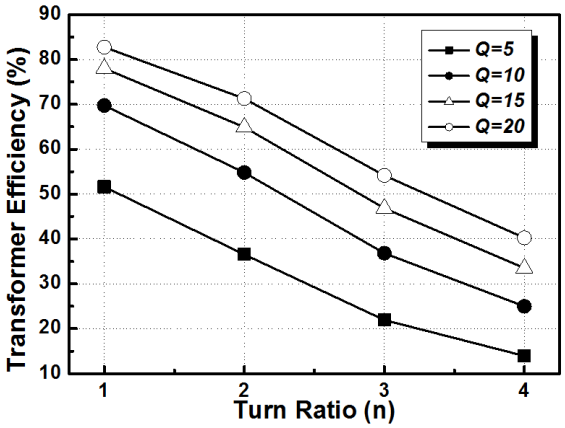
$$P_L = \frac{(\omega n^2 k L_1)^2}{(R_2 + R_L)^2 + (\omega n^2 L_1)^2} \cdot \frac{(R_L / n^2)}{R_{in}} P_{in} \tag{12}$$

$$\begin{aligned} \eta_{xfmr} &= \frac{P_L}{P_{in}} = \frac{P_L}{P_{R1} + P_{R2} + P_L} \\ &= \frac{1}{1 + \frac{1}{R_L} \cdot \frac{\omega n^2 L_1}{Q_2} + \frac{\omega L_1}{Q_1 R_L} \cdot \frac{\left(\frac{\omega n^2 L_1}{Q_2} + R_L \right)^2 + (\omega n^2 L_1)^2}{(\omega n k L_1)^2}} \end{aligned} \tag{13}$$

In other words, comparing to the conventional transformer design with a 50Ω of load impedance, the efficiency of the transformer can be enhanced in the proposed design with the low load impedance, R_{SW}. Furthermore, the transformer can be connected to the T/R switch differentially since the differential switch is available. In the differential drive, the transformer winding gives a higher Q factor than when a single-ended source is used [38]. As a result, the transformer efficiency can be enhanced. In Figure 52, the maximum available gain of the designed transformer is demonstrated.



(a)



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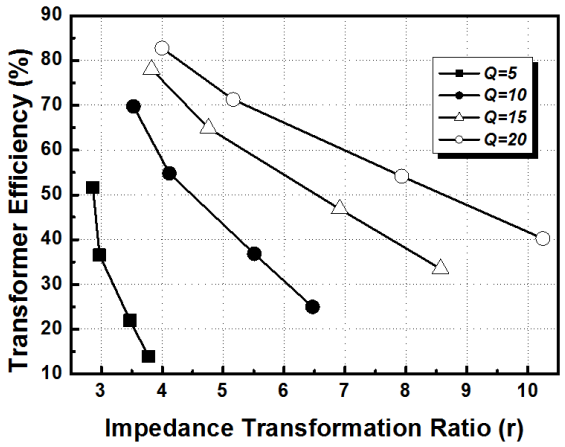


(c)

Figure 51. Transformer efficiency: (a) R_{in} and r vs. n, (b) η vs. n and (c) η vs. r

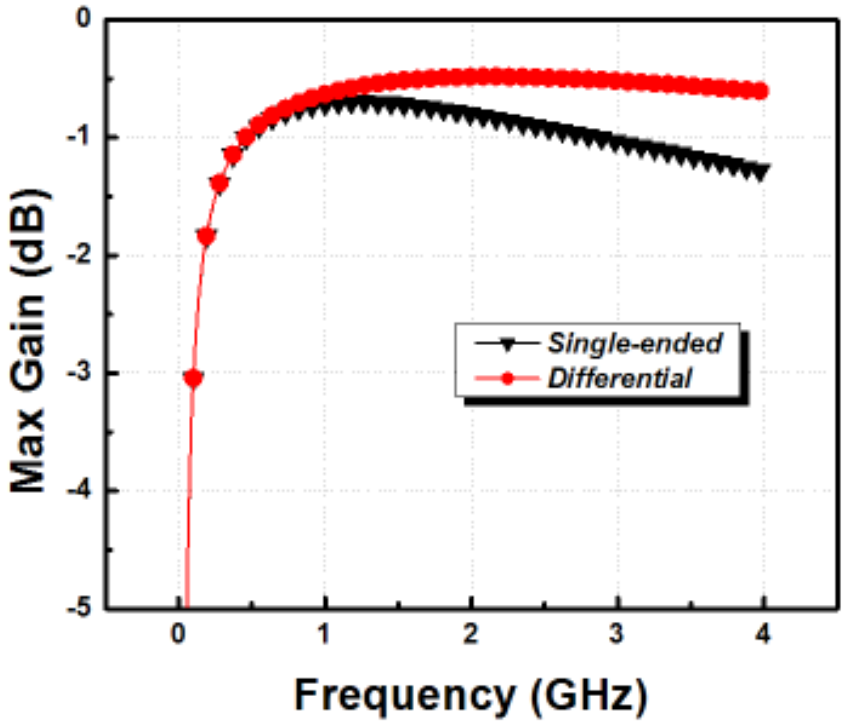


Figure 52. Simulated transformer max gain for single-ended and differential cases

5.3.2. Lattice-Type LC Balun

5.3.2.1. LC Balun Design

The second matching network is implemented between the antenna and the T/R switch providing a low switch operating impedance, R_{SW}, for better switch power performance. Since the differential T/R switch is integrated to this matching directly, the matching has to be functioned as a balun as well as an impedance transformer, unless a differential antenna is available. Therefore, a lattice-type LC balun is implemented for the matching network [32]. Comparing to the transformer, there are much fewer design parameters in implementing the LC balun, so it is more straightforward to control the

transformed impedance. The structure of the LC balun is shown in Figure 53. In order to maximize the output voltage swing at the antenna port, inductor and capacitor used in the LC balun resonate at the operating frequency and their absolute values determine the switch operating impedance, functioning as an impedance matching network.

The values of inductance and capacitance according to the objective impedances are presented in Table 4. To achieve the exact impedance matching, the effects of bonding-wires are considered and all the metal lines which are used in the LC balun are electromagnetic(EM)-simulated in the practical design. From the results of EM simulations, values of inductance and capacitance are tuned for the desired matching point.

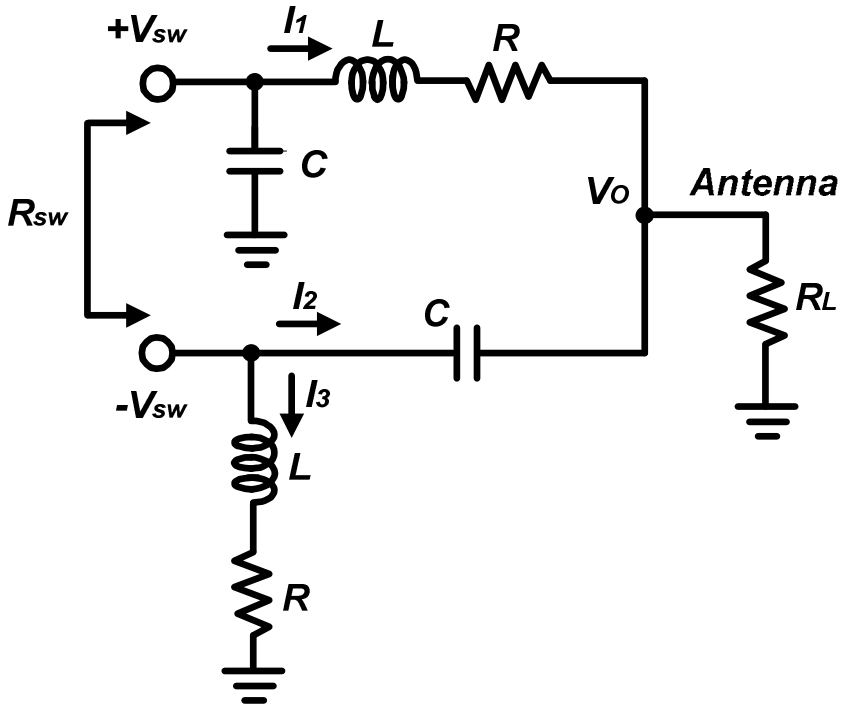


Figure 53. Schematic of lattice-type LC balun

Table 4. Transformed impedances by LC balun at 1.9 GHz

Transformed Impedance (Ω)	Inductance (nH)	Capacitance (pF)
5	1.32	5.3
10	1.87	3.75
15	2.29	3.06
20	2.65	2.65
25	2.96	2.37
30	3.24	2.16
35	3.5	2
40	3.75	1.87
45	3.97	1.77

5.3.2.2. LC Balun Efficiency

The efficiency of the LC balun can be expressed by (16), where the Q factor of inductors $Q = \omega L/R$, and the impedance transformation ratio $r = R_L/R_{SW} = (R_L/\omega L)^2$ [32]. As the first observation from the analysis, Q factors of inductors used in the LC balun directly affect to the efficiency of the LC balun. Since the Q factors of capacitors are much higher, losses due to the capacitors are neglected here. With IBM 0.18-µm CMOS process, the Q factor of inductors can be reached up to 15. Secondly, the efficiency of the LC balun is also inversely proportional to the impedance transformation ratio, in the same manner with the transformer case. Figure 54 shows these. That is, the efficiency of this matching network is deteriorated as the R_{SW} decreases. Therefore, the optimal efficiency

of the entire multi-section impedance matching, which is composed of a transformer and an LC balun, should be achieved by selecting the proper R_{SW} in the proposed design.

$$P_{diss} = I_1^2 R + I_3^2 R \tag{14}$$

$$P_o = \frac{V_o^2}{R_L} \tag{15}$$

$$\eta_{balun} = \frac{P_o}{P_{diss} + P_o} \approx \frac{1}{1 + \frac{1}{2Q\sqrt{r}} + \frac{5\sqrt{r}}{4Q^3} + \frac{1}{2Q^2} + \frac{\sqrt{r}}{Q}} \tag{16}$$

where $Q = \frac{\omega L}{R}$ and $r = \frac{R_L}{R_{SW}} = \left(\frac{R_L}{\omega L}\right)^2$

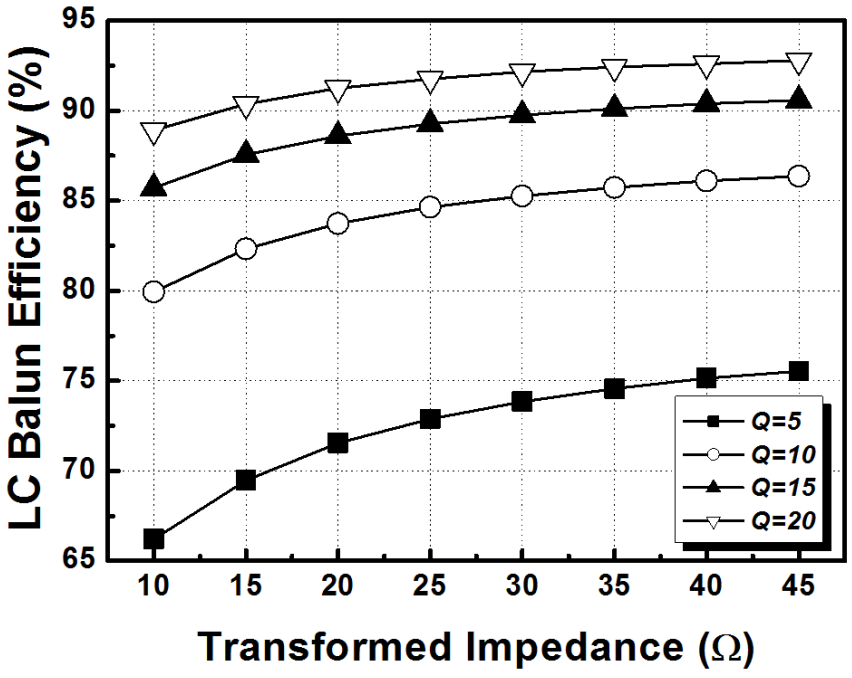


Figure 54. LC balun efficiency

5.4. CMOS Power Amplifier Design

5.4.1. Power Amplifier Schematic Overview

The proposed PA is composed of three parts, (1) an input matching network including an input balun, (2) a power stage which consists of two pairs of CMOS differential cascode amplifiers, and (3) an on-chip transformer as an output matching network. The PA block diagram is illustrated in Figure 55.

Assuming the single-ended input to PA, an input balun is implemented at the very first stage of the PA. By using the input balun, the single-ended input RF signal is converted into the differential signal to feed the differential PA. To reduce losses due to reflections, capacitors are included at the input and the output ports of the balun.

For the power stage, two pairs of differential cascode topology are utilized to generate a high output power as shown in Figure 56. The cascode amplifier consists of a common-gate (CG) stage at the top and a common-source (CS) stage at the bottom. This cascode structure is widely used to relieve the reliability issues due to the high voltage stress, and particularly the CG device is implemented by using thick-oxide devices. In order to achieve a high gain, cross-coupled capacitors are included between the drain of one CS device and the gate of the other CS device of the differential pair, forming a positive feedback. The unstable characteristic due to the increment in gain can be resolved by the RC feedback network between the drain of the CG device and the gate of the CS device of each differential pair. This also helps to reduce the voltage stress of CG device [39].

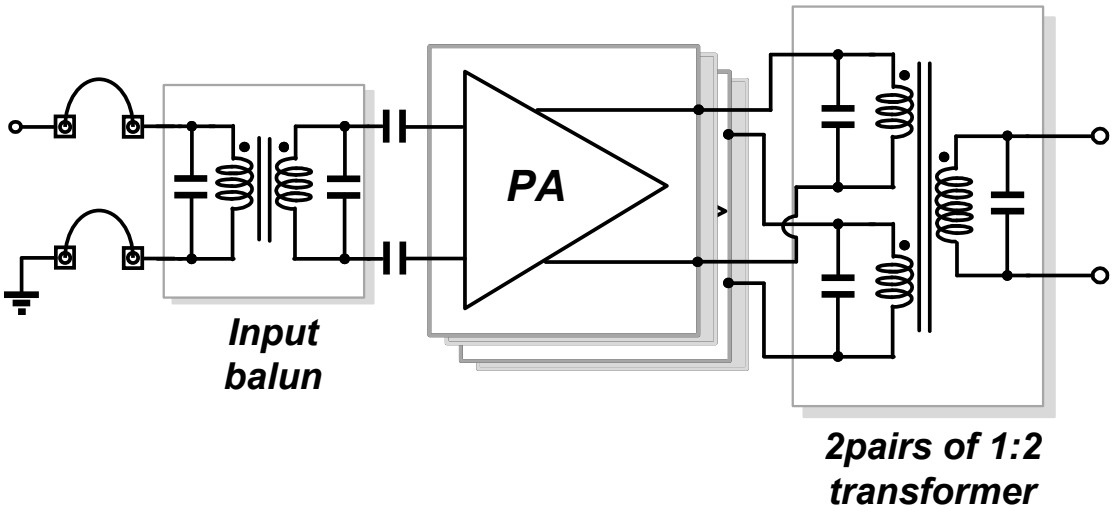


Figure 55. Block diagram of PA

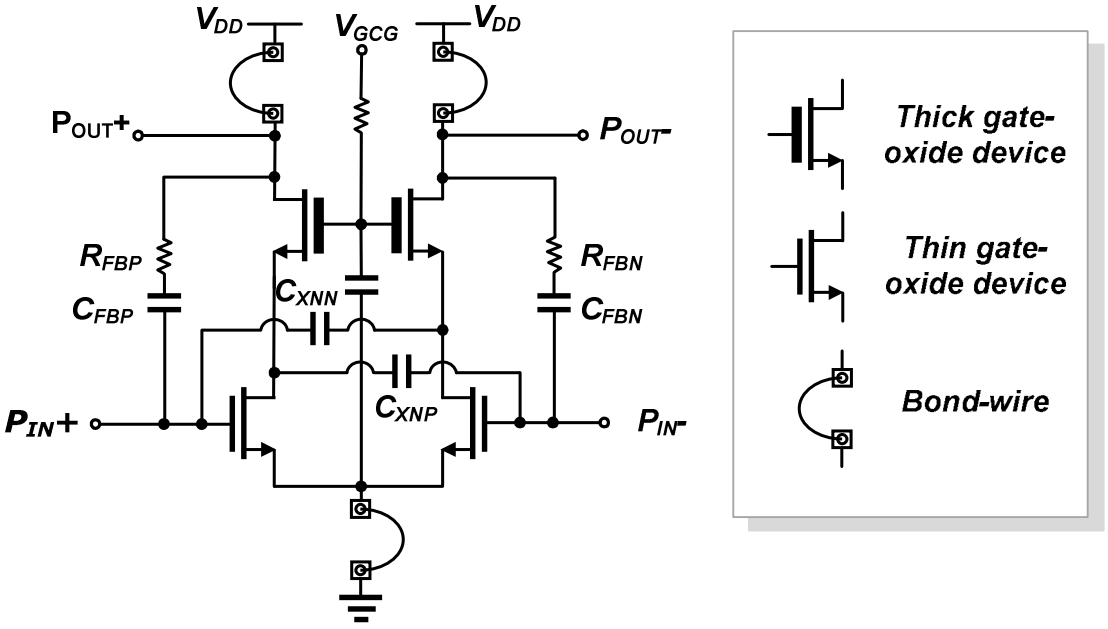


Figure 56. Schematic of PA core - cascode power stage

5.4.2. Power Amplifier Features

The proposed standard 0.18-μm bulk CMOS PA has several features to notice as indicated in Figure 56.

- Differential topology
- Cross-neutralized capacitors (C_{XNP} and C_{XNN})
- Feedback network

As the first feature of this PA design, differential topology has various advantages. First of all, the effect of bond-wire can be significantly reduced, comparing to the single-ended counterpart, by forming a virtual ground. Furthermore, the even order harmonic components can be suppressed effectively. Beside these, the differential PA shows a better linearity than the single-ended PA. In the proposed design, full-differential design can be achieved with the differential T/R switch as explain earlier.

For a higher gain of the PA, cross-neutralized capacitors (CXNP and CXNN), which are connected between the gate of the CS device at one differential branch to the drain of the CS device at the other differential branch. This feature is also available with the differential structure. Furthermore, these capacitors can cancel out the effect of C_{GD} (gate-drain parasitic capacitance), which deteriorates the PA linearity, enabling the PA to operate linearly [40]. However, PA stability can be threatened depending on the value of the cross-neutralized capacitances. Thus, their values should be chosen carefully.

Finally, the feedback networks have been added on each differential branch to secure the stability. The RC feedbacks form a negative feedback from the output side to the input side and helps to improve the stability. Since this feedback network can reduce the

gain, as opposed to the effect of cross-neutralized capacitors, the impedance of this networks also should be selected carefully.

For the design details, 2.5 pF of C_{XNP} and C_{XNN} are utilized and 500Ω of resistors and 0.5 pF of capacitors are employed for the feedback network, R_{FBP} and C_{FBP}, respectively. The gate widths of both CS and CG devices are 4-mm, and it consists of 64 unit cells * 8 fingers * 8-μm width/finger.

5.5. CMOS T/R Switch Controller

5.5.1. CMOS T/R Switch Controller Overview

As discussed earlier, a negative supply voltage is required for T/R switches to enhance the power-handling capability. In order to extract the negative voltage from a supply voltage, a charge pump based switch controller is implemented in the proposed design. The block diagram of the switch controller is shown in Figure 57. It consists of an oscillator, a charge pump, and a level shifter. The oscillator generates two out-of-phase clock signals to drive the charge pump. Before the charge pump, there are inverter chains as a clock buffer to provide an adequate drive to the charge pump. Using the clock signals out of the buffer, the charge pump generates a negative voltage. The magnitude of negative voltage is controlled by capacitors in the charge pump. This charge pump output is connected to the level shifters, and the level shifters select the proper DC output level between V_{DD} and the negative charge pump output. With this switch controller, a negative supply voltage can be obtained from the V_{DD}.

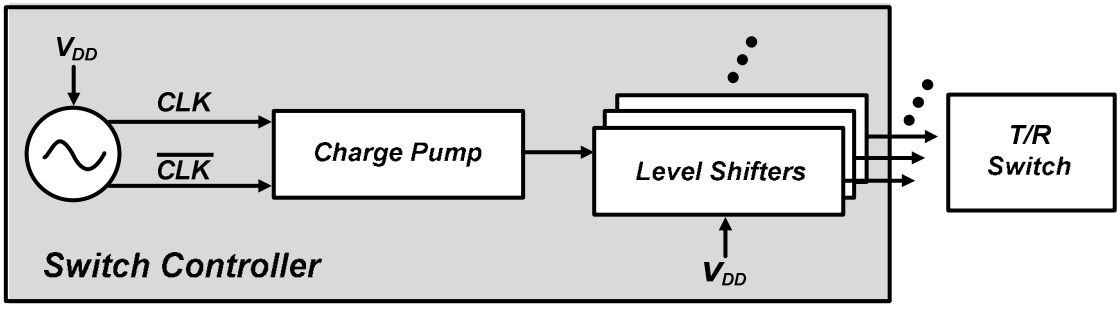


Figure 57. Block diagram of CMOS T/R switch controller

5.5.2. Oscillator (Clock Generator)

To feed the charge pump with the clean clock signals, an oscillator is designed. The block diagram of designed oscillator is shown in Figure 58. A traditional ring type oscillator structure is employed, and a transmission gate is added on clock-bar path to compensate the signal delay.

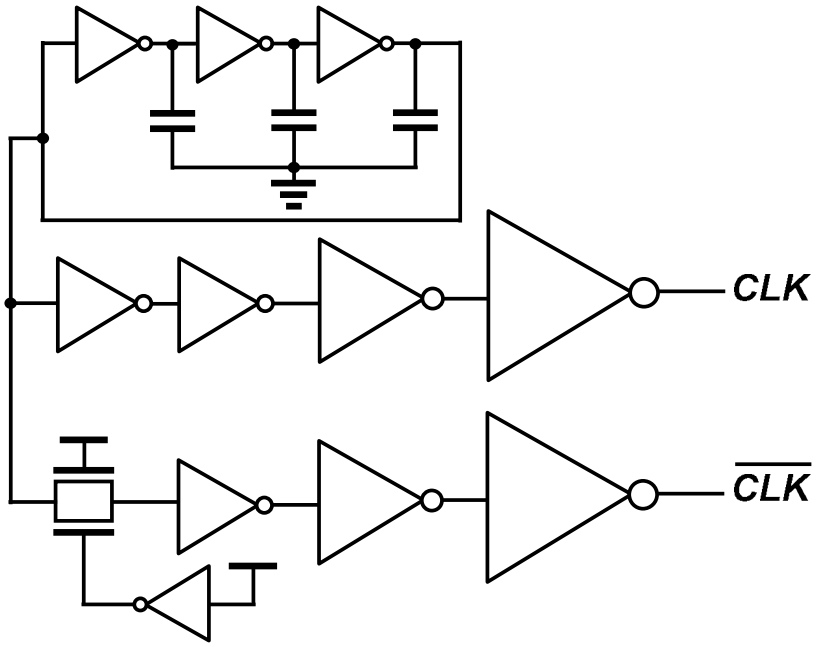


Figure 58. Block diagram of clock generator to feed the charge pump

5.5.3. Charge Pump

In the proposed T/R switch controller, the charge pump is the most important block among the functional blocks shown in Figure 57, since it generates the desired voltage to the T/R switch. Figure 58 is the circuit diagram of a single stage charge pump with MOS switches only [41].

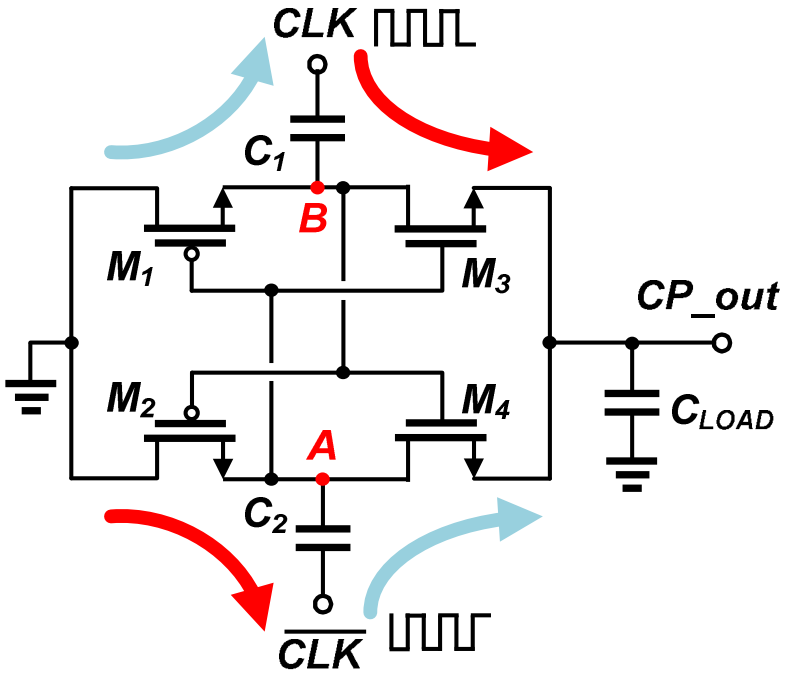


Figure 59. Schematic of charge pump with MOS switches only

As shown in Figure 58, the charge pump is composed of four MOS switches, M_1-M_4, and two charging capacitors C_1 and C_2. In the first clock period, for example, when CLK is low, M_1 and M_4 are open while M_2 and M_3 are closed, charging the capacitor C_2 until CLK goes to high. In the next clock period, M_2 and M_3 are open while M1 and M4 are closed, in the same manner, charging the capacitor C_1 until the next clock period comes. During this period, the generated negative voltage at node "A" is transferred to the charge pump output through the M_4, while M_2 is open to prevent the current from going back to

wrong direction. This charge pump operation is easily understood by referring Figure 58. For the first clock period, charge moves through the red arrows and it moves through the blue arrows for the next clock period. At the output of charge pump, there is a load capacitance, C_L, acting as a filter that reduces the ripples generated by the charge pump.

The size of active devices and the values of C_1 and C_2 are also area of interest. The voltage drop depends on the charging capacitances and the on-resistance of the MOS switches, influencing on the accurate charge pump operations. Thus, it is important to choose proper values of the charging capacitances and the gate width of MOS devices in designing the charge pump.

5.5.4. Level Shifter

To choose the proper DC supply for both Tx and Rx operations, level shifters are implemented. The schematic of level shifter is shown in Figure 58.

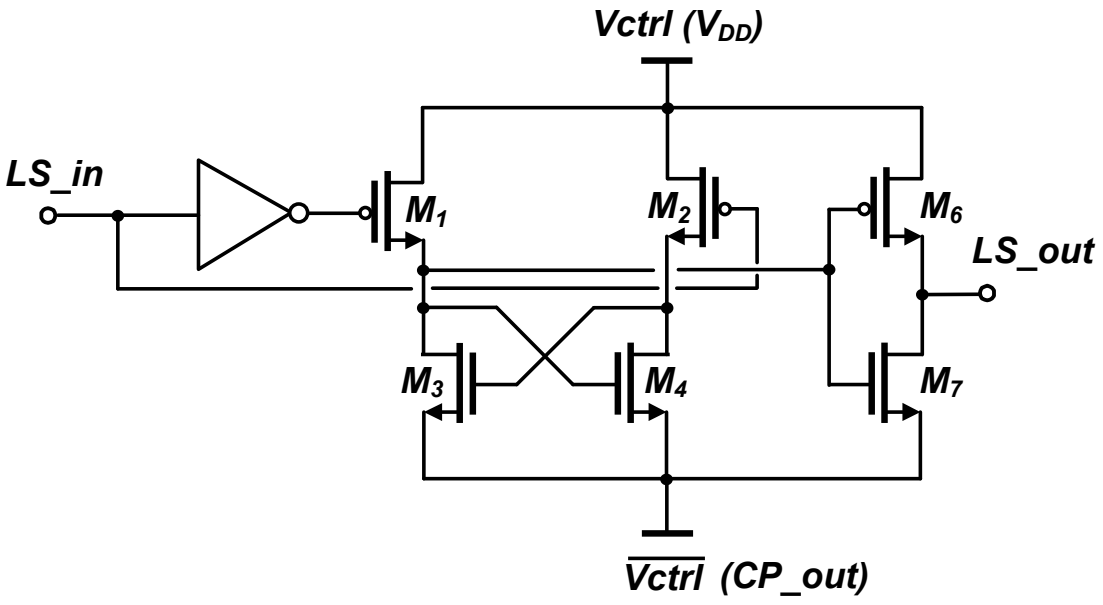


Figure 60. Schematic of level shifter for T/R switch biases

When LS_in is low, M_1 is open and M_2 is closed. Thus, M_3 is closed and LS_out port is connected to V_{DD} through the M_6, and the bias is usually used as a switch turn-on voltage. Similarly, when LS_in is high, M_1 is closed and M_2 is open. As a result, M_4 is closed and M_3 is open. Finally, LS_out port is connected to the "low" supply voltage which is generated by the charge pump. Since this logic is only able to choose one bias as an output, multiple level shifters are required to control multiple switch modes. For example, in the proposed design, two level shifters have been implemented to control Tx and Rx modes separately.

5.6. CMOS Transmitter Front-End Module

A transmitter front-end module which includes a PA, a T/R switch, and a T/R switch controller is designed for the mobile handset applications. The schematic for the proposed design is shown in Figure 61. A multi-sectional impedance matching network with a transformer and an LC balun, and a high-power-generating PA are integrated with the differential T/R switch which was introduced in earlier Chapter. From the perspective of the total efficiency and the power-handling capability of the front-end module, the R_{SW} is chosen carefully, considering the analyses of matching loss and T/R switch insertion loss discussed in earlier Chapters. The damaged switch insertion loss by implementing an unnecessary matching network in Rx path is compensated by reducing the number of the stacked switch devices on the Rx series path and Tx shunt path. According to the simulation results, two stacks of Rx series devices are adequate to handle the high power signals from the PAs, since the large voltage swing has been already reduced by employing the differential switch architecture, stepping down the R_{SW} once [37].

The simulation results for the fully-integrated transmitter front-end module are shown in Figure 62. As shown in the Figure, the proposed transmitter front-end module shows the saturated output power of approximately 2-W across the band (from 1.7-GHz to 1.9-GHz) and peak PAE of 45% with 21-dB of gain. Since the T/R switch in the proposed design is able to handle the high power linearly, the efficiency of the module at the high power region is not deteriorated much. If the T/R switch cannot, the load impedance of the PA is deviated and it degrades the output power as well as the efficiency. Figure 63 shows the micro-photograph of the proposed transmitter front-end module using a standard CMOS 0.18-μm process. The total size including wire-bonding pads is 2500 μm x 1100 μm.

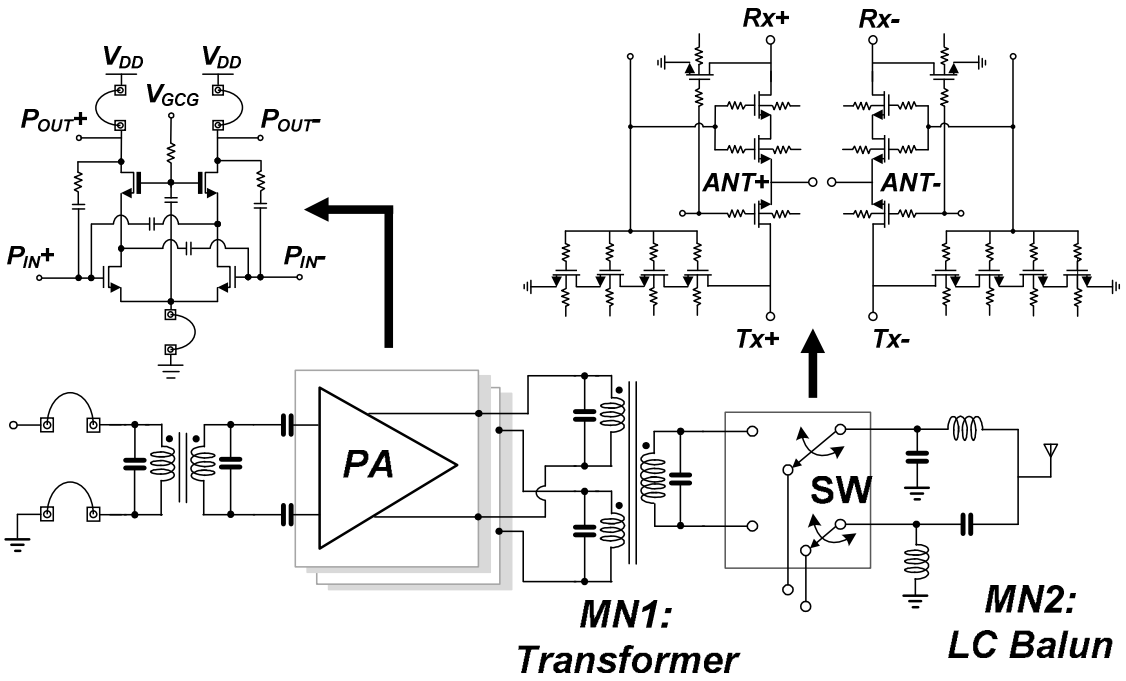
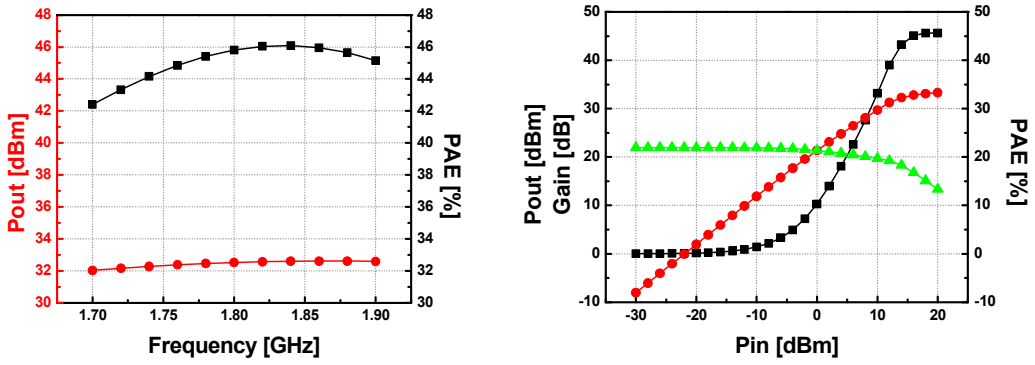


Figure 61. Schematic of proposed transmitter front-end module



(a) (b)

Figure 62. Performances of the proposed transmitter front-end module: (a) Frequency sweep with 15-dBm input power and (b) Power sweep at 1.9 GHz

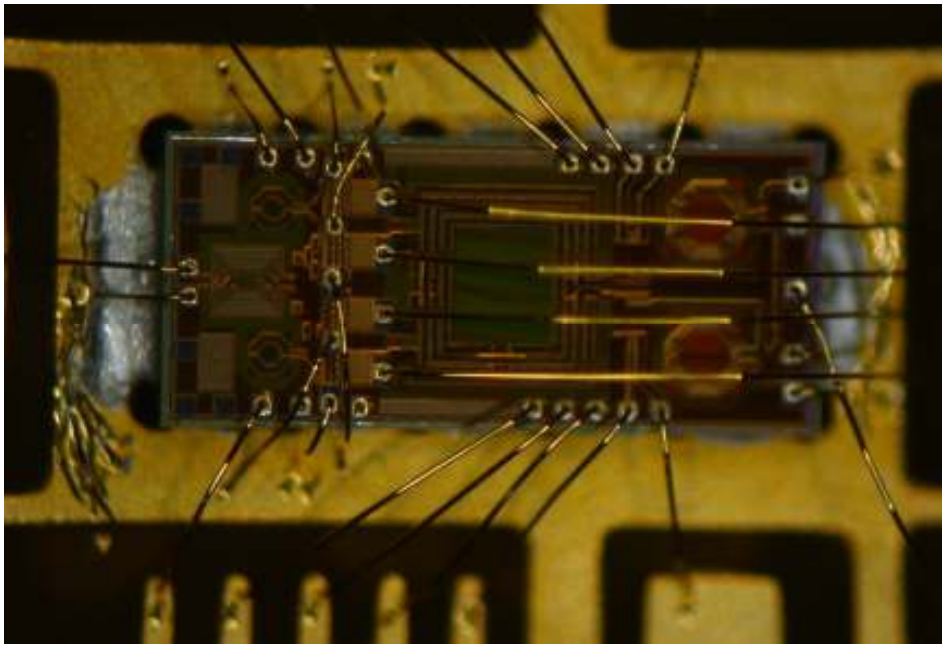


Figure 63. Micro-photo of the CMOS transmitter front-end module

5.7. Conclusions

In this Chapter, a high-power and highly efficient CMOS transmitter front-end module is presented. The power-handling capability of the module is improved with differential T/R switch structure and with the multi-section impedance transformation technique [37]. By utilizing the multi-section output impedance matching, the efficiency of the module is enhanced with the proper R_{SW}. According to the analyses through this dissertation, 35Ω of R_{SW} is chosen for the T/R switch operating impedance for high-power and highly efficient operation. The proposed module also includes the CMOS T/R switch controller which includes oscillator, charge pump, and two level shifters. The module transmits 32.3-dBm of output power to antenna, with the 45% of PAE. As shown in the Table 5, this work shows the best performance among the CMOS implementations, and comparable to the GaAs counterpart.

Table 5. Transmitter front-end performance summary

	Process	Frequency	Features	Supply Voltage	Performances
GaAs Symposium 2003 [42]	GaAs/pHEMT	900 MHz	-GaAs HBT PA - pHEMT switch	5 V	Pout: 34 dBm Efficiency: 45%
BCTM 2006 [43]	BiCMOS	870 MHz	-BiCMOS PA -pHEMT switch	3.5 V	Pout: 32 dBm Efficiency: 35%
RWS 2007 [44]	CMOS SOI	400 MHz	-Resonant switch -UHF application	3.3 V	Pout: 29 dBm Efficiency: 29%
APMC 2008 [45]	0.18 µm CMOS	2GHz	-Transistor stacking - LNA design included	3.3 V	Pout: 29.7 dBm Efficiency: 35%
Proposed transmitter front-end	0.18 µm CMOS	1.81 GHz	-Differential topology - Multi-section impedance matching	3.3 V	Pout: 32.3 dBm Efficiency: 45%

CHAPTER 7
CONCLUSIONS

In recent years, the demand of a transmitter front-end module is getting increased. Furthermore, CMOS implementations are getting more interests from both academia and industry aiming to take advantage from the perspective of manufacturing cost. Although there are critical intrinsic shortcomings in CMOS process, especially for the high-power applications, it is definitely worthy to develop the one chip radio, keeping up with the recent explosive wireless market growth. In this dissertation, the most difficult CMOS implementations among the RF functional blocks in transceiver, T/R switches and PAs, are discussed and new solutions are presented to enhance their performances.

The achievements can be summarized as follows:

- The substrate network of CMOS devices is analyzed to understand its behaviors. The substrate of CMOS devices is not well-modeled, and its effects on the performance of high-power handling RF functional blocks, T/R switches and PAs, are critical, unfortunately. By modeling the substrate network simply with capacitors and resistances, the effects of substrate networks corresponding to the device size, port biasing, the amount of substrate contacts, and the distance between chip and substrate contacts are predicted.
- A new CMOS differential T/R switch structure for high-power applications is proposed. The proposed structure demonstrates considerably improved power handling capability and linearity over the conventional structure by relieving the

voltage stress over the switch devices. Furthermore, since the differential topology is favored due to its various superiorities, differential design takes merits. Consequently, it will be a promising structure to implement a CMOS T/R switches. The proposed structure is integrated with the proposed PA to achieve the high performance transmitter front-end module.

- The CMOS T/R switch utilizing the impedance transformation technique is presented. Unlike the conventional switch with ITT, the possibility of utilizing PA output matching network as the impedance matching networks for T/R switch is proposed. With the approach, an implementation of additional lossy block can be avoided, optimizing the total loss (efficiency). The insertion loss of T/R switch and the loss of matching blocks are analyzed with equations, enabling the proper switch designs with ITT.
- A high-power handling T/R switches with feed-forward capacitors are presented. The feed-forward capacitors help multi-stack switch devices taking equal amount of voltage stresses. To enhance the power performance, more devices are required to be stacked and the feed-forward capacitors are more effective as the number of stacked switch devices increases. The T/R switches with two stacks, three stacks, and four stacks for Rx series switch are implemented as design example, and the effects of feed-forward capacitors are presented.
- A CMOS T/R switch controller is presented. To design the high-power T/R switches, negative supplies are required for off-switch and P-well ports. The proposed charge pump based T/R switch controller enables to generate the negative supplies internally.

- A CMOS transmitter front-end module, which consists of CMOS T/R switch and CMOS PA, is proposed with the proposed differential T/R switch and multi-section PA output matching networks. A high output power is generated by combining the output powers from two cascode PAs with transformer and the high-power signal is transmitted through the differential T/R switch to the antenna, in the proposed structure. In the proposed design, power-handling capability of module is improved by relieving the voltage stress over switch devices with the differential architecture and ITT, while its efficiency is optimized with the multi-section output impedance matching by distributing the burden of impedance transformation with the multiple matching networks.

REFERENCES

[1] A. A. Abidi, "RF CMOS comes of age," *IEEE J. Solid-State Circuits,* vol. 39, pp. 549-561, 2004.

[2] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. 4th ed. New York: Wiley, 2001.

[3] Q. Li, and Y. P. Zhang, "CMOS T/R switch design: Towards ultra-wideband and higher frequency," *IEEE J. Solid-State Circuits,* vol. 42, pp. 563-570, 2007.

[4] M. D. Yore, C. A. Nevers, and P. Cortese, "High-isolation low-loss SP7T pHEMT switch suitable for antenna switch modules," *in European Microwave Conference (EuMC), 2010 IEEE,* 2010, pp. 69-72.

[5] M. Ahn, J. Cha, C. Cho, C. -H. Lee, and J. Laskar, "Ultra low loss and high linearity SPMT antenna switch using SOI CMOS process," *in European Microwave Conference (EuMC), 2010 IEEE,* 2010, pp. 652-655.

[6] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* 2nd ed. Cambridge, U. K.: Cambridge Univ. Press, 2004.

[7] F. -J. Huang, and K. O, "A 900-MHz T/R switch with a 0.8-dB insertion loss implemented in a 0.5-μm CMOS process," *in Custom Integrated Circuits Conference (CICC), 2000 IEEE,* 2000, pp. 341-344.

[8] M. -C. Yeh, Z. -M. Tsai, R. -C. Liu, K. -Y. Lin, Y. -T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 54, pp. 31-39, 2006.

[9] M. Ahn, H. -W. Kim, C. -H. Lee, and J. Laskar, "A 1.8-GHz 33-dBm P0.1-dB CMOS T/R switch using stacked FETs with feed-forward capacitors in a floated well structure," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 57, pp. 2661-2670, 2009.

[10] F. -J. Huang, and K. O, "A 0.5-μm CMOS T/R switch for 900-MHz wireless applications," *IEEE J. Solid-State Circuits,* vol. 36, pp. 486-492, 2001.

[11] J. Kim, H. Kim, Y. Yoon, K. H. An, W. Kim, C. -H. Lee, K. T. Kornegay, and J. Laskar, "A discrete resizing and concurrent power combining structure for linear CMOS power amplifier," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2010 IEEE*, 2010, pp. 387-390.

[12] Y. Yoon, H. Kim, K. H. An, J. Kim, C. -H. Lee and J. Laskar, "A fully-integrated dual-mode tunable CMOS RF power amplifier with enhanced low-power efficiency," *in European Microwave Conference (EuMC), 2010 IEEE,* 2010, pp. 982-985.

[13] K. H. An, O. Lee, H. Kim, D. H. Lee, J. Han, K. S. Yang, Y. Kim, J. J. Chang, W. Woo, C.-H. Lee, H. Kim, and J. Laskar, "Power-combining transformer techniques for fully-integrated CMOS power amplifiers," *IEEE J. Solid-State Circuits,* vol. 43, pp. 1064-1075, 2008.

[14] R. Brama, L. Larcher, A. Mazzanti, and F. Svelto, "A 30.5 dBm 48% PAE CMOS class-E PA with integrated balun for RF applications," *IEEE J. Solid-State Circuits,* vol. 43, pp. 1755-1762, 2008.

[15] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri, "Distributed Active Transformer- A new power-combining and impedance-transformation technique,"

Microwave Theory and Techniques, IEEE Transactions on, vol. 50, pp. 316-331, 2002.

[16] P.-C. Wang. K.-Y. Huang, Y.-F. Kuo, M.-C. Huang, C.-H. Lu, T.-M. Chen, C.-J. Chang, K.-U. Chan, T.-H. Yeh, W.-S. Wang, Y.-H. Lin, and C.-C. Lee, "A 2.4-GHz +25dBm P-1dB linear power amplifier with dynamic bias control in a 65-nm CMOS process," in *Proc. ESSCIRC.,* Jun. 2008, pp. 490-493.

[17] B. Razavi, *RF Microelectronics,* New Jersey: Prentice Hall, 1998.

[18] M. Carroll, D. Kerr, C. Iversen, A. Tombak, J. –B. Pierres, P. Mason, and J. Costa, "High-resistivity SOI CMOS cellular antenna switches," in *Compound Semiconductor Integrated Circuit (CSIC) Symposium, 2009 IEEE*, 2009, pp. 1-4.

[19] A. Scuderi, C. D. Presti, F. Carrara, B. Rauber, and G. Palmisano, "A stage-bypass SOI-CMOS switch for multi-mode multi-band applications," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2008 IEEE*, 2008, pp. 325-328.

[20] D. Kelly, C. Brindle, C. Kemerling, and M. Stuber, "The state-of-the-art of silicon-on-sapphire CMOS RF switches," in *Compound Semiconductor Integrated Circuit (CSIC) Symposium, 2005 IEEE*, 2005, pp. 200-203.

[21] T. Ohnakado, S. Yamakawa, T. Murakami, A. Furukawa, E. Taniguchi, H. Ueda, N. Suematsu, and T. Oomori, "21.5-dBm Power-handling 5-GHz transmit/receive CMOS switch realized by voltage division effect of stacked transistor configuration with depletion-layer-extended transistors (DETs)," *IEEE J. Solid-State Circuits,* vol. 39, pp. 577-584, 2004.

[22] K. H. An, Y. Kim, O. Lee, K. S. Yang, H. Kim, W. Woo, J. J. Chang, C. –H. Lee, H. Kim, and J. Laskar, "A monolithic voltage-boosting parallel-primary

transformer structures for fully integrated CMOS power amplifier design," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, 2007, pp. 419-422.

[23] C. –T. Fu, S. S. Taylor, and C. –N. Kuo, "A 5-GHz, 30-dBm, 0.9-dB insertion loss single-pole-double-throw T/R switch in 90nm CMOS," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2008 IEEE*, 2008, pp. 317-320.

[24] C. Tinella, J. M. Fournier, D. Belot, and V. Knopik, "A high-performance CMOS-SOI antenna switch for the 2.5-5-GHz band," *IEEE J. Solid-State Circuits,* vol. 38, no. 7, pp. 1279-1283, Mar. 2003.

[25] J. -H. Wang, H. -H, Hsieh, and L.-H. Lu, "A 5.2-GHz CMOS T/R switch for ultra-low-voltage operations," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 56, pp. 1774-1782, 2008.

[26] F. -J. Huang, and K. O, "Single-pole double-throw CMOS Switches for 900-MHz and 2.4-GHz applications on p- silicon substrates," *IEEE J. Solid-State Circuits,* vol. 39, pp. 35-41, 2004.

[27] N. A. Talwalkar, C. P. Yue, H. Gan, and S. S. Wong, "Integrated CMOS transmit-receive switch using LC-tuned substrate bias for 2.4-GHz and 5.2-GHz applications," *IEEE J. Solid-State Circuits,* vol. 39, pp. 863-870, 2004.

[28] H. Xu, and K. O, "A 31.3-dBm bulk CMOS T/R switch using stacked transistors with sub-design-rule channel length in floated p-Wells," *IEEE J. Solid-State Circuits,* vol. 42, pp. 2528-2534, 2007.

[29] M. Ahn, C. -H. Lee, B. S. Kim, and J. Laskar, "A high-power CMOS switch using a novel adaptive voltage swing distribution method in multistack FETs,"

Microwave Theory and Techniques, IEEE Transactions on, vol. 56, pp. 849-858, 2008.

[30] A. A. Kidwai, C. -T. Fu, J. C. Jensen, and S. S. Taylor, "A fully integrated ultra-low insertion loss T/R switch for 802.11b/g/n application in 90 nm CMOS process," *IEEE J. Solid-State Circuits,* vol. 44, pp. 1352-1360, 2009.

[31] J. Costa, M. Carroll, J. Jorgenson, T. McKay, T. Ivanov, T. Dinh, D. Kozuch, G. Remoundos, D. Kerr, A. Tombak, J. Mcmaken, and M. Zybura, "A silicon RF CMOS SOI technology for integrated cellular/WLAN RF TX module," in *Microwave Symposium Digest, 2007. IEEE MTT-S International*, 2007, pp. 445-448.

[32] P. Reynaert, and M. S. J. Steyaert, "A 2.45-GHz 0.13-µm CMOS PA with parallel amplification," *IEEE J. Solid-State Circuits,* vol. 42, pp. 551-562, 2007.

[33] O. Lee, K. H. An, H. Kim, D. H. Lee, J. Han, K. S. Yang, C. -H, Lee, H. Kim, and J. Laskar, "Analysis and design of fully integrated high-power parallel-circuit class-E CMOS power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 57, pp. 725-734, 2010.

[34] K. Miyatsuji, and D. Ueda, "A GaAs high power RF single pole dual throw switch IC for digital mobile communication system," *IEEE J. Solid-State Circuits,* vol. 30, pp. 979-983, 1995.

[35] T. -Y. Lee, and S. Lee, "Modeling of SOI FET for RF switch applications," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2010 IEEE*, 2010, pp. 479-482.

[36] Z. Li, H. Yoon, F. -J. Huang, K. O, "5.8-GHz CMOS T/R switches with high and low substrate resistances in a 0.18-μm CMOS process," *Microwave and Wireless Components Letters, IEEE,* vol. 13, pp. 1-3, 2003.

[37] H. -W. Kim, M. Ahn, O. Lee, C. -H. Lee, and J. Laskar, "A high power CMOS differential T/R switch using multi-section impedance transformation technique," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2010 IEEE*, 2010, pp. 483-486.

[38] J. R. Long, "Monolithic transformer for silicon RF IC design," *IEEE J. Solid-State Circuits,* vol. 35, pp. 1368-1382, 2000.

[39] T. Sowlati, and D. M. W. Leenaerts,"A 2.4-GHz 0.18-μm CMOS self-biased cascode power amplifier," *IEEE J. Solid-State Circuits,* vol. 38, pp. 1318-1324, 2003.

[40] N. Wongkomet, L. Tee, and P. R. Gray, "A +31.5 dBm CMOS RF Doherty power amplifier for wireless communications," *IEEE J. Solid-State Circuits,* vol. 41, pp. 2852-2859, 2006.

[41] R. Pelliconi, D. Iezzi, A. Baroni, M. Pasotti, and P. L. Rolandi, "Power efficient charge pump in deep submicron standard CMOS technology," *IEEE J. Solid-State Circuits,* vol. 38, pp. 1068-1071, 2003.

[42] P. DiCarlo, S. Boerman, R. Burton, H. –C. Chung, D. Evans, M. Gerard, J. Gering, I. Khayo, L. Lagrandier, I. Lalicevic, P. Reginella, S. Sprinkle, and Y. Tkachenko, "A highly integrated quad-band GSM TX-front-end-module," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 2003 IEEE*, 2003, pp. 280-283.

[43] A. J. M. de Graauw, A. van Bezooijen, C. Chanlo, A. den Dekker, J. Dijkhuis, S. Pramm, and H. K. J. ten Dolle, "Miniaturized quad-band front-end module for GSM using Si BiCMOS and passive integration technologies" in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2006 IEEE*, 2006, pp. 1-4.

[44] J. Jeon, and W. B. Kuhn, "A UHF CMOS transceiver front-end with a resonant TR switch," in *Radio and Wireless Symposium (RWS), 2007 IEEE*, 2007, pp. 71-74.

[45] M. Ahn, K. H. An, C. –H. Lee, J. Laskar, and H. Kim, "Fully integrated high power RF front-end circuits in 2 GHz using 0.18μm standard CMOS process." in *Asia-Pacific Microwave Conference (APMC), 2008 IEEE*, 2008, pp. 1-4

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