ABSTRACT

SONG, WENCHAO. Design and Control of Distributed Power Flow Controller. (Under the direction of Dr. Alex Q. Huang.)

Electricity is the one important energy form used in industrial, commercial, and residential areas. The power transmission system is essential for the power utility system to transmit electricity. Now the transmission lines in the modern interconnected power system are heavily loaded to meet the growing demands. The aggregate demand for electricity has grown by about 25% over the last decade and is expected to grow no less than 20% for the next decade. At the same time, however, the annual investment in transmission facilities has declined, leading directly to severe power congestion in the transmission lines. Construction of new transmission facilities could alleviate congestions, but it is cost-prohibitive and time-consuming. The way of using passive components and Flexible AC Transmission System (FACTS) to manage the power flow on transmission lines is efficient but not very effective. While low-cost ($15–25 per kVar as for static capacitors) and easy-to-use, passive components are inadaptable and slow for control purpose. The FACTS devices can control the power flow on transmission lines with flexible control and fast response through the use of large power converters (10-300 MW), but high expenses, typically exceeding $100 per kVA, together with reliability concerns constitute substantial obstacles for the widespread application of FACTS.

Recently ETO Light modular voltage source converter (VSC) has been developed. It has lower cost, higher reliability and high power density and can be completely housed in an enclosure without additional user intervention. Accordingly, ETO Light converter has

the potential to widely spread the use of the modular voltage source converter in FACTS applications and other high power industry applications.

This dissertation introduces a new concept of distributed power flow controller (DPFC) based on the development of ETO Light converter. Unlike the conventional lumped high rating (10-300MVA) series compensation converter, the proposed distributed power flow controller uses multiple scaled-down (1-2MVA) single-phase power converters to dynamically control the impedance of the power transmission line, thus control the active power flow. The power density is enhanced and the cost is reduced by applying the ETO Light converter. The distributed power flow controller has the self-power, self-protection and self-control functions. It only accepts the command from external system level controller, and then injects compensating voltage to control the current and active power flow through the power transmission line. The standard modular design of DPFC enables the high reliability, short design cycle and the easy installation/maintenance of power converter. This dissertation demonstrates the principles of the modular distributed power flow controller based on the ETO light converter. The modeling and controller design are proposed and verified by the simulation and experimental results. The applications in the transmission system and distribution system are proposed and verified by simulation. The fault tolerant design for DPFC are discussed and presented and verified by the simulation and experimental results. The research work for the design and control of DPFC sheds the light for the practical intelligent and distributed high power converter applications in the power grid.

Design and Control of Distributed Power Flow Controller

by
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DEDICATION

To my wife and daughter,

Caifeng and Siyan

and my parents,

Shaoguang Song and Xiufeng Chen

BIOGRAPHY

Wenchao Song was born in Lushuihe, Jilin province, China, in 1978. He received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 2000 and 2003 respectively.

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Chapter 1. Introduction

This chapter introduces the background of this dissertation including the power flow control demands and methods, series compensation applications, modular power converter and modular controller design, and semiconductor devices. The motivation and outline of this dissertation are discussed as well.

1.1. Power Flow Control

Electricity is the one of the most popular sources of energy used in industrial, commercial and residential areas among all of the energy forms [1]. Fig. 1.1 shows the energy flow trend of the United States. Generating clean and renewable electricity, transmitting and distributing electricity effectively and efficiently have been important concerns all over the world. “The country that harnesses the power of clean, renewable energy will lead the 21st century.” exclaimed President Barack Obama, February 24th, 2009. Currently the US government is devoted to building a new economy that is powered by clean and secure energy, including the generation of more renewable electricity, to manufacturing more plug-in hybrid vehicles, and to saving more oil and reducing greenhouse gas emissions. President Barack Obama on Oct 28, 2009 announced $3.4 billion in government grants to help build a "smart" electric grid that will save consumers money on their utility bills, reduce blackouts and carry power supplies generated by solar and wind energy [2] – [3].

Power electronics is one of the most important technologies to apply in industrial applications such as Flexible Alternating Current Transmission Systems (FACTS), High

Voltage DC (HVDC) systems for the control of the power grid in order to achieve stable, efficient and effective power systems [4] - [9]. It is very important to develop power electronics technology for application in the power grid to control and manage the energy system.

Power electronics technology based FACTS applications are widely utilized in power utilities to supply increased loads, to improve reliability, and to deliver energy at the lowest possible cost and with improved power quality [10] - [11].

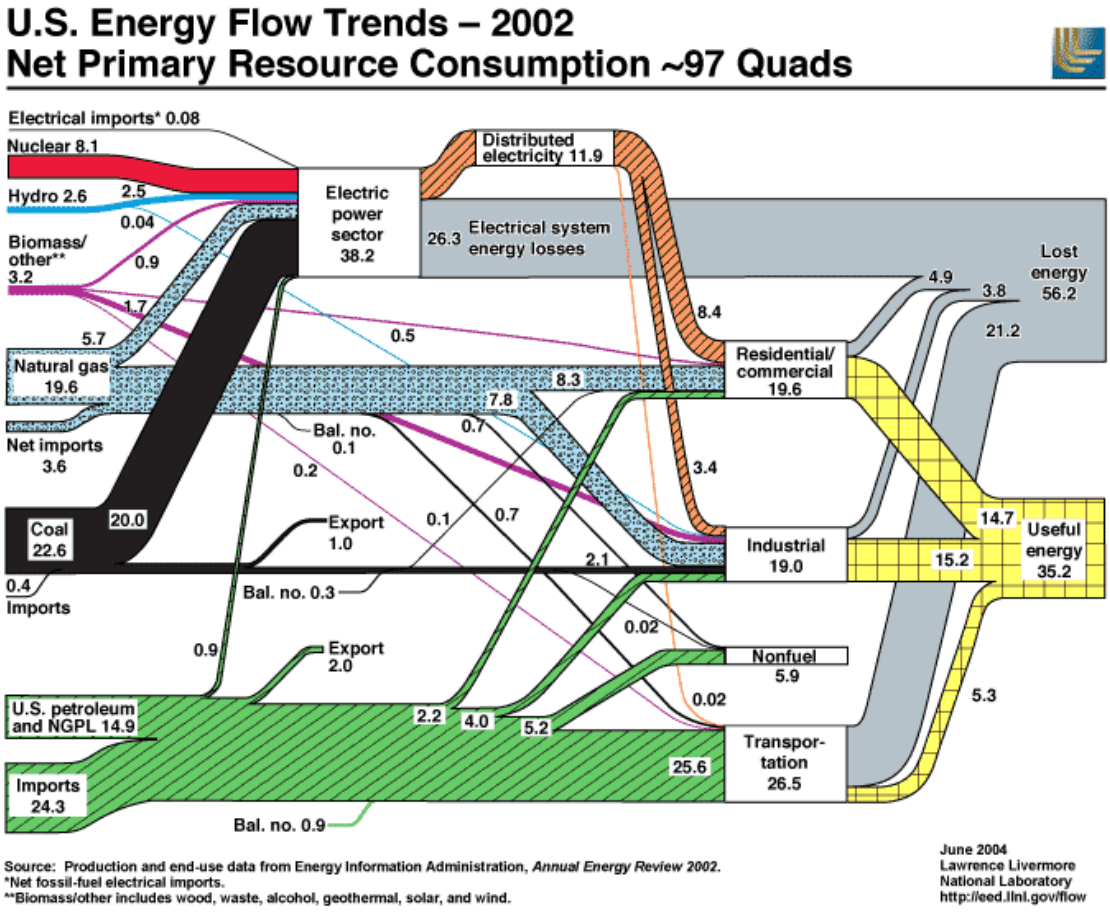


Fig. 1.1 Energy flow trends of the United States

FACTS has been defined by the IEEE as follows:

"A power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability."

In general, FACTS controllers can be divided into three categories:

1. Series controllers,
2. Shunt controllers and
3. Combined series-shunt controllers

The world's first series compensation on transmission level, currently recognized by manufacturers as a FACTS-device, went into operation in 1950. Series compensation is used in order to decrease the transfer reactance of a power line at a given rated frequency. Among FACTS controllers, series compensation controllers have shown feasibility in terms of cost-effectiveness in a wide range of problem-solving efforts from transmission to distribution levels. For decades, it has been recognized that the transmittable power through transmission lines could be increased, and the voltage profile along the transmission line could be controlled by an appropriate amount of compensated reactive voltage. Moreover, the series compensation controller can improve transient stability and can damp power oscillation during a post-fault event. Using a high-speed power converter, the series compensation controller can further alleviate asymmetrical currents and fault current issues after failure or disturbance [11].

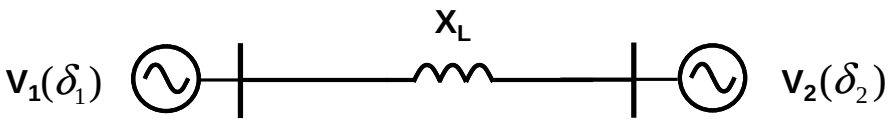


Fig. 1.2 Power transmission line model

For the simple two-generator one-line system shown as Fig. 1.2, the transmitted active power through the line can be expressed by equation 1.1.

$$P = \frac{V_1 - V_2}{X_L} \sin(\delta_1 - \delta_2) \qquad (1.1)$$

where V_1 and V_2 are the voltage amplitude of generators; δ_1 and δ_2 are the voltage angle of generators; X_L is the inductive line impedance.

We can find that the transmitted active power through transmission lines are determined by generator voltage magnitude, angle difference and line impedance. It is effective to control the line impedance, thus control the active power flow through transmission lines.

1.2. Series Synchronous Compensator

The Static Series Synchronous Compensator (SSSC) is a reactive series compensator employing a Voltage-Sourced Converter (VSC) in series with the transmission line, as shown in Fig. 1.3. This operating mode emulates a controlled series reactive compensation (such as one obtained with the Thyristor-Controlled Series Capacitor), but provides a wider control range and equal capacitive and inductive operating domains [10] – [12].

The VSC within the SSSC is operated in synchronism with the transmission line *current*. The voltage generated by the VSC is kept in quadrature with the line current, lagging or leading it by 90 degrees. The injection of a lagging voltage with respect to the line current emulates a series capacitor, whereas a leading voltage emulates a reactor in series with the line. Thus, the SSSC can provide either series capacitive or series inductive compensation, without any rating increase or additional reactive components,

by its inherent capability to reverse the polarity of the output voltage it generates. The quadrature relationship between the output voltage of the SSSC and the line current ensures substantially zero real power exchange between the SSSC and the ac system, except for the small amount (about 1% at full output) required to replenish the internal losses of the converter. This power is drawn from the line by the converter, using a small (typically less than one degree) deviation from the ideal 90°, to keep the dc capacitor charged without an external dc power supply.

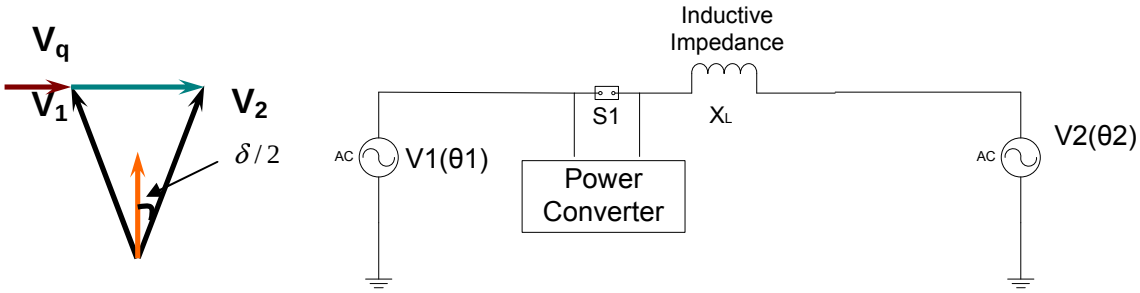


Fig. 1.3 Schematic diagram of SSSC

Normally we assume $V = V_1 = V_2$ and $\delta = \delta_1 - \delta_2$.

In SSSC, the transmitted active power verses transmitted phase angle relationship is shown in equation 1.2.

$$P = \frac{V^2}{X_L}\sin\delta + \frac{V}{X_L}V_q\cos\frac{\delta}{2} \qquad (1.2)$$

where V_q is the compensating voltage, negative means capacitive compensation and positive means inductive compensation.

If the SSSC is used for power flow control then the SSSC has an effective rating of twice the rating of the power converter. This means that the SSSC can increase or

decrease the power flow to the same degree in either direction simply by changing the polarity of the injected AC voltage. Fig. 1.4 shows the transmitted power verses transmitted angle as a function of series compensation.

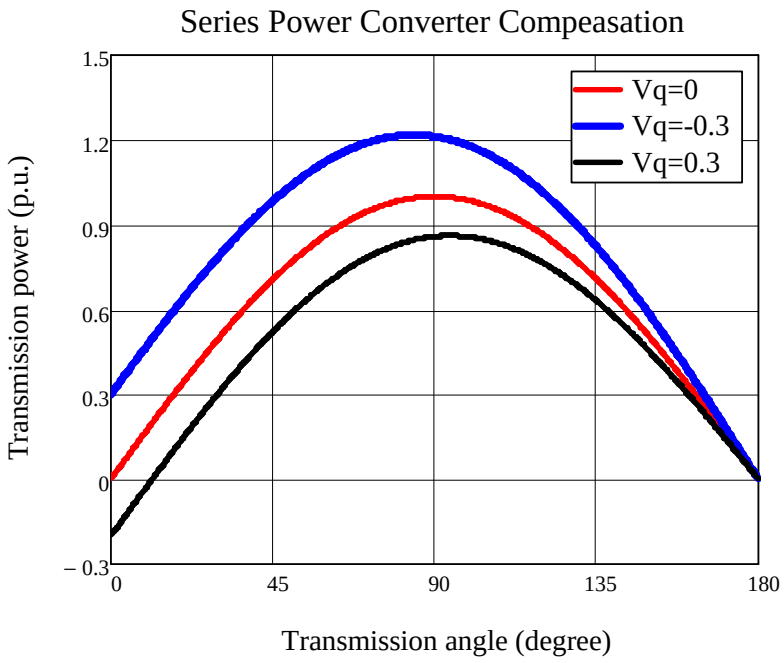


Fig. 1.4 Transmission line active power flow by series converter compensation

SSSC operation

The SSSC is one of the most powerful FACTS Controllers for power flow control. Although it can provide transmission line voltage regulation through the control of the effective line impedance, particularly for the end-voltage of a radial line, the primary purpose of the SSSC is usually the direct, and dynamic, control of the transmitted power in a given line. The main applications within the broad area of adjustable or dynamic power flow control are as follows:

(1) Compensation of long transmission lines.

(2) Equalization of power flow in lines and prevention of loop-flows of real power.

(3) Receiving end voltage regulation of a radial line.

(4) Improvement of transient stability and dynamic stability (power oscillation damping).

1.3. Series Compensation Solutions Comparision

1.3.1. Fixed Series Capacitor

Fig. 1.5 shows a transmission system with fixed series capacitive compensation, which has no controllability and no flexibility. The operating area of an SSSC is a rectangle in the V x I plane and for the fixed capacitive compensation we have only a fixed line for each value of the compensation capacitance. In this compensation, the larger the capacitive reactance the larger will be the transmitted power.

Although fixed series capacitor compensation is simple and lack of flexibility, it is still the lowest cost and most popular series compensation solution for the power flow control in the current market.

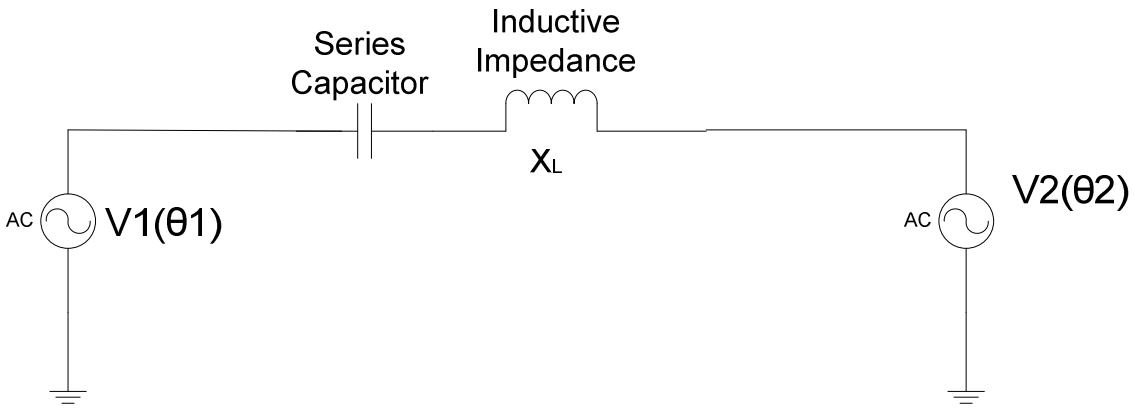


Fig. 1.5 Fixed capacitor compensation

1.3.2. Fixed Series Reactor

Fig. 1.6 shows a transmission line with fixed inductive compensation, which is not very common as it operates to decrease the transmitted power. As in the case of fixed capacitive compensation the power transmission characteristic is given just by a line for each compensation level and the larger the reactance the smaller the transmitted power.

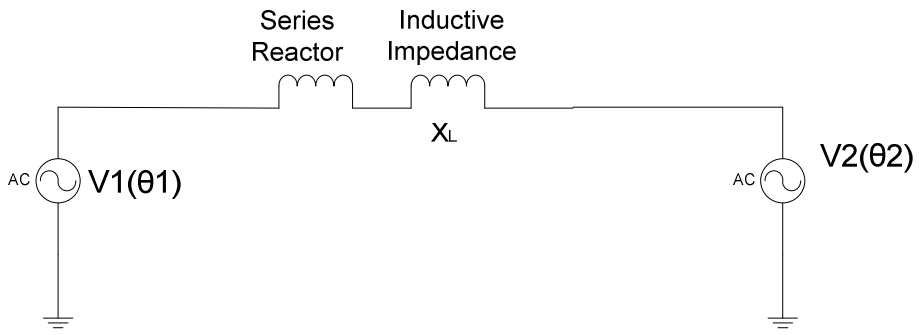


Fig. 1.6 Fixed inductive compensation

1.3.3. Thyristor-Controlled Series Capacitor

The Thyristor-Controlled Series Capacitor (TCSC) was proposed by Hingorani and Gyugyi [11]. It is a device based on the concept of impedance control. The control device is the thyristor semiconductor switch. Due to its relatively low cost, there are various examples of actual applications around the world for power oscillation damping or power flow control. Gama, Angqüist, and Ingeström [13] presented a paper on the commissioning of a TCSC for power oscillation damping in the Brazilian North-South transmission line.

Fig. 1.7 shows a transmission system with a TCSC in series. It shows that this series device is composed of a fixed series capacitor in parallel with a Thyristor Controlled Reactor (TCR).

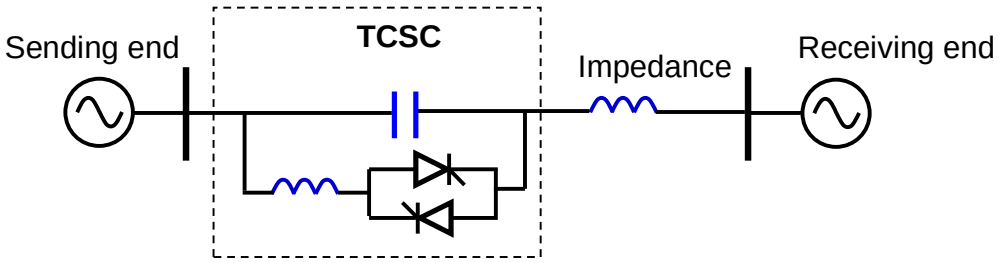


Fig. 1.7 Transmission line with TCSC

Comparing the TCSC with SSSC with the information given above allows us to conclude that:

(1) the operating area of the TCSC is much smaller than the SSSC in the capacitive region;

(2) TCSC operating characteristics is reduced to a line only in the inductive region as compared to a rectangle in the case of SSSC;

(3) TCSC may present problem of internal resonance which must be avoided.

Despite the advantages of the SSSC as compared with the TCSC, this thyristor-based device is still used as a practical option when wide range of controllability of the SSSC is not necessary. When low cost is an objective the TCSC is also a good option.

1.3.4. Gate-Controlled Series Capacitor

Fig. 1.8 shows a transmission line with a Gate-Controlled Series Capacitor (GCSC) connected in series. This is a device also based in the concept of variable impedance and it was originally presented by Karady, Ortmeyer, Pilvelai, and Maratukulam [14] and they called it as “continuously regulated series capacitor”. Later, Souza, Watanabe, and Aredes [15] introduced the name “GTO-Controlled Series Capacitor” which was adopted by Hingorani and Gyugyi [10]. However, due to the fact that different switching devices can be used, provided they can be turned off, Edris [16] has recently changed “GTO-Controlled” to “Gate-Controlled”. In all cases the acronym GCSC was kept to maintain a contrast with TCSC.

The diagram in Fig. 1.8 shows that the GCSC has a very simple structure with one capacitor and parallel switches. These switches operate as a dual thyristors. These dual thyristors and the capacitor in parallel is exactly the dual circuit of a thyristor controlled reactor (TCR), where a reactor is in series with a thyristor valve. In the case of TCR the control is done by the firing angle. However, in the case of GCSC the switches are turned on automatically the voltage always crosses zero and they must be turned off to insert the capacitor in series with the line. Therefore, instead of firing angle, in the GCSC the turn-off angle is used.

One interesting point is that the TCR is a device theoretically well-matched for shunt connection whereas the GCSC is well-matched for series connection. One advantage of the GCSC over the TCSC is the fact that it does not need a reactor and, therefore, it may be a more compact device. Souza, Watanabe, Alves, and Pilotto [17] presented a detailed

comparison between GCSC and TCSC. If a perfect TCSC dual circuit is to be produced, then a reactor has to be connected in series with the capacitor in parallel with the switches. However, this option may not be necessary as the line is normally inductive and putting more series inductance has no value except to increase the cost of the compensation device.

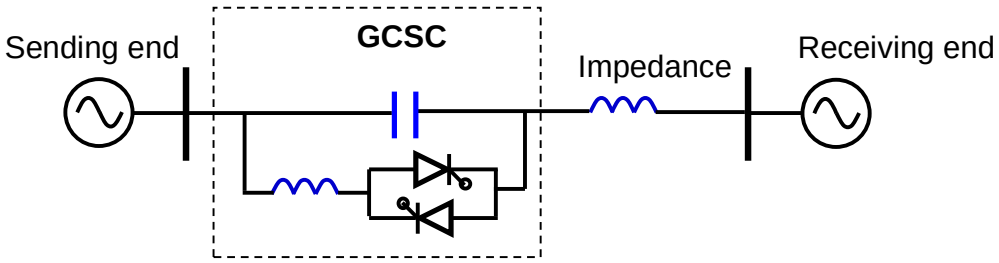


Fig. 1.8 Transmission line with GCSC

1.3.5. Magnetic Energy Recovery Switch

The Magnetic Energy Recovery Switch (MERS) is a new configuration that has been recently proposed in power system transmission applications for controlling power flow [18], [19].

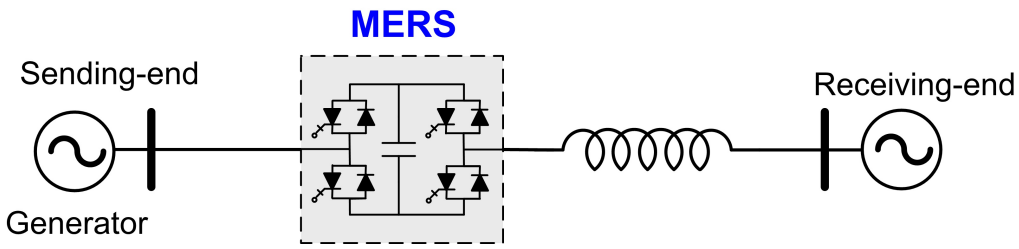


Fig. 1.9 Configuration of the Magnetic Energy Recovery Switch

The configuration of the MERS is shown in Fig. 1.9. It has four forced commutated switches and a DC capacitor in each phase. The configuration is similar to a single phase full bridge, but the operation differs and the size of the capacitor is several times smaller.

MERS switching patterns are shown in Fig. 1.10. By controlling the current path through the device, the device can behave like a controllable capacitive voltage source. This is performed by using line frequency switching; that is, one switch is turned on and off only once during an electrical 50 or 60 Hz cycle.

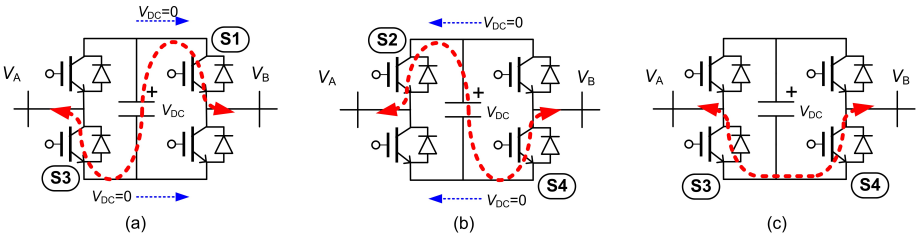


Fig. 1.10 MERS switching pattern

The comparisons of SSSC and MERS are:

(1) The operating range of the MERS is just the operating range of the SSSC in the capacitive range (half of the total SSSC operating range).

(2) The MERS has a simpler and more compact configuration than the SSSC, with no series injecting transformer and small capacitor.

(3) The injected harmonics are potentially lower for the SSSC than for the MERS.

(4) The basic control of the MERS is equivalent to a capacitor and a reactive voltage source in series, while the SSSC is equivalent to a pure reactive voltage source.

1.3.6. Distributed Static Series Compensator

Recent researches are focus on designing and realizing cost-effective FACTS device by applying distributed concept instead of the conventional lumped solution. A Distributed Static Series Compensator (DSSC) was proposed by Divan [40], [41]. Small rated (1 – 20kW) inverter with light weight (45kg) and single turn transformer (75:1) are applied to form a DSSC module that can be clamped to the transmission conductor to control the active power on the line. The schematic of DSSC is shown as Fig. 1.11.

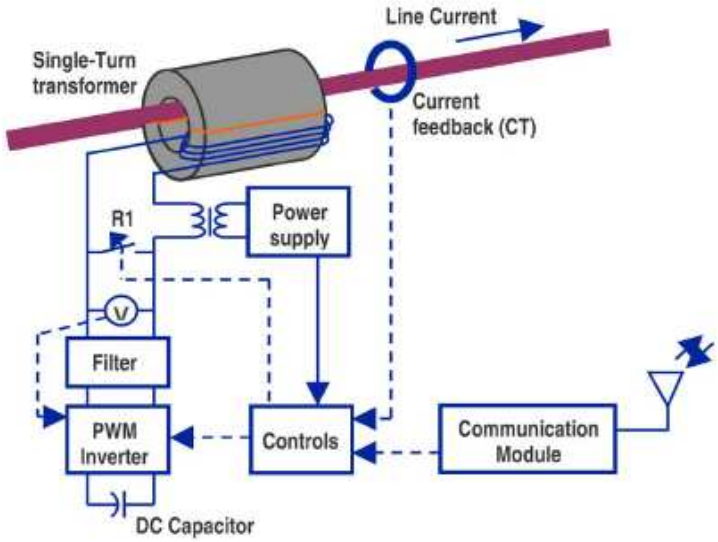


Fig. 1.11 DSSC configuration

DSSC concept is simple and low-cost, thus shows advantages for active power flow control compared with lumped solution. While the high transformer turns ratio increase the current level, the compensating voltage ability and power inverter rating are limited as well. As a result, a large number of DSSC modules are required to control the certain active power flow through the power transmission line.

1.4. Semiconductor Power Devices

Thyristors were first introduced in early 1960s and became popular semiconductor devices in high voltages and currents applications. Silicon Controlled Rectifiers (SCRs) were widely used in HVDC systems due to its high power ratings. However, SCR has a limited application because it lacks controlled turnoff capability. Today, most FACTS controllers utilize the gate turn-off (GTO) thyristor as the main power semiconductor switch, due to its advantages over other available devices in power handling capacity, reliability, and cost. Because of the slow speed determined by the turn-on and turn-off processes, the switching frequency of GTO devices is typically below 500 Hz. The low switching frequency increases the power converter's output harmonics that will have to be reduced by a large passive filter.

The insulated gate bipolar transistor (IGBT) device has been developed in the 1990s. Based on integration of fine-pattern metal oxide semiconductor field effective transistor (MOSFET) and vertical bipolar transistor, its performance has improved dramatically in power ratings and reliability. The weak conductivity modulation in the IGBT results in significantly higher conduction loss, thereby limiting the upper voltage rating that the IGBT can feasibly penetrate. Furthermore, the reliability of a high-current IGBT module is a major concern. Although an accurate number is hard to obtain, it is generally believed that the thermal cycling reliability of today's high power IGBT module is still much worse than a traditional press pack device such as the GTO.

Recent research developments have focused to improve the GTO's switching. Two most notable innovations are the integrated gate commutated thyristor (IGCT) developed

by ABB and the emitter turn-off thyristor (ETO) developed by semiconductor power electronics center (SPEC), North Carolina State University. Both of them concentrate on reducing the GTO's gate drive power consumption and eliminate the dV/dt snubber. The IGCT and ETO differ in their approach, performance, and cost. The IGCT relies on a proprietary, expensive, special GTO wafer design plus a custom designed low inductance press pack housing. Due to reduced gate inductance, the IGCT turn-off is performed in transistor mode instead of thyristor mode, hence the dV/dt snubber is reduced or eliminated. The speed of the device is also increased to allow higher frequency operation. The emerging ETO thyristor combines the advantages of thyristor's high voltage/current capability and MOSFET's easy gate control. Due to high silicon utilization and simplified drive circuit, it has lower cost than other high power competing semiconductor devices, such as GTO, IGCT, and IGBT [20] - [22].

1.5. Multilevel Converters

In recent years, the requirement of higher power rating equipment in industry has begun to increase. The family of multilevel converters is considered as the solution for operating with high voltage levels because single semiconductor device can not connect directly to medium voltage grid [23] – [25].

Multilevel converters use an array of semiconductors and capacitor voltage sources to generate staircase output waveforms. Fig. 1.12 shows a simplified schematic diagram of one-phase converter with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions [24].

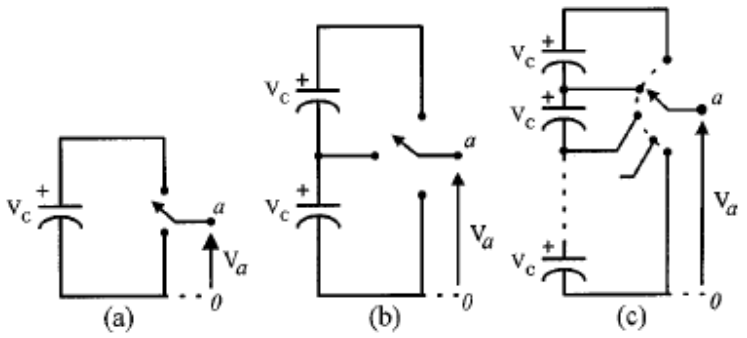


Fig. 1.12 Single phase converters (a) two-level. (b) three-level (c) n-level

The multilevel converters can generate output voltages with low distortion and lower dv/dt and operate with a lower switching frequency, thus reduce the switching losses and improve electromagnetic current (EMC).

The first multilevel converter circuit appeared in 1975 [26], in which the cascade converter was first defined with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped inverter was also the derived [27]. The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s [28]. Although the cascade inverter was invented earlier, its application did not prevail until the mid-1990s. Two major patents [29], [30] were filed to indicate the superiority of cascade inverters for motor drive and utility applications. The capacitor-clamped multilevel inverter came in the 1990s [31], [32].

1.6. Distributed Modular Converters

For high power electronics applications, modular converters will greatly reduce engineering development cost. Power Electronics Building Block (PEBB) and H-Bridge Building blocks (HBBB) are possible modular converters that could be easily reconfigured to various applications [33] – [34].

For multi-level converter topologies shown above, cascaded multilevel converter is the most modularized topology. Besides its modularity, it has also many advantages such as the following:

- The least number of components compared with other multi level topologies
- Easy expansion
- Easily achievable higher power rating
- Easy to add redundancy

1.7. Fault Tolerant Design for High Power Applications

Fault tolerant design is widely applied to improve system reliability, maintainability and survivability. Reliability deals with the period of time over which that ability is retained. A control system that allows normal completion of tasks after component failure will improve reliability. Maintainability concerns the need for repair and the ease with which repairs could be made, without a premium placed on performance. Fault tolerance could increase time between maintenance actions and allow the use of simpler repair procedures. Survivability relates to the likelihood of conducting an operation safely, whether or not the task is completed. Degraded performance following failure might be

permitted, as long as the system can be brought to an acceptable state of rest [35].

In the fault-tolerant design, all operations before the fault, in the fault and after the fault should be considered throughout the entire design procedure. In summary, the issues of fault-tolerant design can be addressed as below.

The first thing that should be considered in a fault-tolerant system is to identify and address the causes of failure. Device failure is the primary contingency from which the converter has to be protected. Device misoperation events can be classified as

(1) Device short circuit

(2) Device open circuit

Both these conditions can arise due to a variety of reasons such as

(1) Failure of the gate drives

(2) Excessive voltage and current stresses on the device

(3) Response to another fault event

In most high power applications, the failed state of devices is short due to the press pack package of the device.

In most cases, a fault device event can be detected by measuring the voltage across the device and current through DC capacitors or devices. Many integrated commercial drive chips have detection and protection functions which can be used fault-tolerant converter systems. The fault detection and diagnosis of a multilevel converter is still an open area for further research.

Normally because of the loss of failed devices, the voltage stress of the remaining devices will increase. So the rating of devices in the fault-tolerant system must be over-designed at the expense of other considerations.

Reliability, maintainability and survivability can be improved by different fault-tolerant designs for different topologies. In the most cases, the protection of the converter will improve survivability by isolating the failed part and stopping the operation of the system to prevent failure cascade.

Usually, it is not easy to find general solutions for a specific topology limited by complex structure and control. To design a fault-tolerant multilevel converter system is an effort still open to all researchers.

However, compared with all the multilevel converter topologies characteristics and the proposed fault-tolerant designs of multilevel converters, the cascaded multilevel converter's modular design has the potential to simplify protection schemes and to improve maintainability. The cascaded structure also can be used to achieve N+1 redundancy to improve reliability [36] – [38]. Further study in this area can be a promising potential topic.

1.8. Motivation and Major Contributions

The transmission lines in the power system are heavily loaded due to growing electricity demands. Construction of new transmission facilities could alleviate congestion, but it is cost-prohibitive and time-consuming [2], [3]. The Static Synchronous Series Compensator (SSSC) is one of the solid state Flexible AC Transmission System (FACTS) devices to effectively control the active power flow through the power transmission lines. It applies large power converters (10-300MW) to alter the power line impedance, thus control the active power flow through the transmission lines [10].

However, higher cost, long building cycle and low reliability still limit its widespread application because the high power converter design is still customized and non-standard.

The distributed power flow controller (DPFC) module based on ETO Light converter with the rating of 1 - 2 MVA single phase configuration is proposed in this dissertation. It has lower cost and higher reliability compared with existing high power converter designs. The standard modular design of DPFC enables easy installation and maintenance. Transformerless connection is enabled by high voltage/current capability and the control power self-generation function of ETO Light converter [33]. The medium rating (1-2MVA) is very suitable for distributed applications. The fault tolerant capability made possible by redundancy can be achieved to enhance reliability and availability . The modular design of megawatt DPFC raises a good opportunity of high power converter applications in the power transmission system. Unlike the traditional three-phase power converter-based SSSC, the DPFC applies distributed per-phase control, which means the DPFC module only measures the current and voltage information in one phase transmission line and controls the active power through this single-phase line. This DPFC concept can also be applied to distribution systems and even in Demands Side management (DSM).

The major contributions of this dissertation include:

(1) A proposal of the DPFC concept using the standard low-cost, high-reliability and short-building-cycle high power converter, combining the emerging semiconductor device, modular converter topology and modular digital controller techniques;

(2) Designed and developed digital local controller system. The feasibility of this local controller has been verified by experimental tests. The local controller subsystem has been applied to multilevel converter based STATCOM projects.

(3) Developed the single-phase power flow controller modeling development and control design methodology. The proposed modeling and controller design is verified by calculations, simulations and experimental tests.

(4) Proposed the applications of DPFC in transmission systems, distribution systems and demand side management applications. The DPFC application interfaced with renewable energy sources was considered and studied. The feasibility of the proposed applications was verified by the simulation results.

(5) Developed fault tolerant designs of the protection scheme and redundancy control strategy for high utility applications such as STATCOM and SSSC. Multilevel solution and distributed solution were proposed by simulations and experimental tests.

1.9. Outline

The dissertation has six chapters:

The first chapter is the introduction, which gives the background of this dissertation and presents the motivation and outline of this research work.

Chapter 2 introduces the power stage design of DPFC. Based on the industrial demands and requirements for high power converter application, the DPFC concept and design consideration of DPFC are introduced. To design the low-cost, high-efficiency, short-building-cycle standard power converter for different applications, the digital local controller and the layered control structure based on modular power converter are

proposed. The feasibility of the control structure and power converter is validated by the experimental results.

Chapter 3 presents the model development and controller design of DPFC. The model development sequence and procedure are introduced. The system models are derived by transfer functions. Based on these transfer functions, the well-designed compensator can be applied so that the controller can achieve good stability and transient response performance of the DPFC. The simulation results and experimental results verify these model development and control design.

Chapter 4 presents the new proposed applications of DPFC in the transmission system, distribution system and demand side management area based on the unique characteristic of DPFC. The DPFC application combined with renewable energy sources are proposed and studied. The implementation and the benefits of this DPFC application are discussed. The simulation results verify the feasibility of DPFC application for active power flow control in different application fields.

Chapter 5 presents the fault tolerant design of DPFC for utility applications. Redundancy is used to achieve fault tolerance in FACTS applications to improve the reliability and availability. Two solutions; multilevel solution and distributed solution are introduced. The fault tolerant strategies are presented in detail. The simulations and experimental results validate the proposed fault tolerant control strategy.

Chapter 6 summarizes the conclusion of the dissertation and proposes future work based on current work and research demands.

Chapter 2. Distributed Power Flow Controller Design

The power transmission system is essential for the power electricity utility system. The transmission lines in the modern interconnected power system are more heavily loaded than ever before to meet the growing demands. Over the last decade, the demand for electricity has increased approximately 25% and is expected 20% increase during the next 10 years. However the annual investment in transmission facilities has declined during this period of vigorous growth the same time [2] – [3]. This has resulted in the increase of power congestion in the transmission line, which costs the power systems a great deal.

Construction of new transmission facilities could alleviate congestion, but the cost is too high and the construction cycle is long. Another effective solution to this issue has been through the use of passive components and Flexible AC Transmission System (FACTS) to manage the power flow on transmission lines [10] – [11]. Passive components such as the static capacitor is low-cost ($15–25 per kVar) and easy to use, but unadaptable and slow for control. FACTS devices can control the power flow on transmission lines by applying large power converters (10-300 MW) with flexible control and fast response. But the cost of the FACTS device is high, typically higher than $100 per kVA. The high cost and reliability concerns become substantial obstacles for the widespread application of FACTS.

Recent researches are focused on designing and realizing cost-effective FACTS devices by applying a distributed concept instead of the conventional lumped solution. A Distributed Static Series Compensator (DSSC) was proposed in [40], [41]. Small rated (1 – 20kW) inverter and single turn transformer are applied to form a DSSC module that can be clamped to a transmission conductor to control the active power on the line. It is simple and low-cost and thus has advantages for active power flow control over the lumped solution. While the high transformer turns ratio increases the current level, the compensating voltage ability and power inverter rating are limited as well. As a result, a large number of DSSC modules are required to control the certain active power flow through the power transmission line.

Recently, the Semiconductor Power Electronics Center (SPEC) of North Carolina State University developed ETO Light modular voltage source converter (VSC) [39]. It has lower cost, higher reliability, and high power density can be completely housed in an enclosure without additional user intervention. The ETO light converter has the potential to spread the use of the modular voltage source converter in FACTS applications and other high power industry applications.

This chapter introduces a new concept of distributed power flow controller (DPFC) based on the development of the ETO light converter. Unlike the conventional lumped high rating (10-300MVA) series compensation converter, the proposed distributed power flow controller uses multiple scaled-down (1-2MVA) single-phase power converters and dynamically controls the impedance of the power transmission line, thus controlling the active power flow. The distributed power flow controller has self-power, self-protection

and self-control functions. It only accepts commands from an external system level controller to inject compensating voltage to the power line, thus controlling the current and active power flow through the power transmission line. The standard modular design of DPFC facilitates installation and maintenance of the power converter. This chapter details the principles of ETO light converter based modular distributed power flow controller. The benefits to power utilities will be presented. The control design, simulation results and experimental results of the distributed model operation will be introduced in the next chapter.

2.1. Series Compensation Power Flow Control

Static Synchronous Series Compensator (SSSC) was proposed by Dr. Gyugyi in 1989 based on the use of three-phase VSC as its main building block to compensate the required voltage. The VSC can be controlled in such a way that the output voltage can either lead or lag the line current by 90 degrees. For example, during normal capacitive compensation, output voltage lags the line current by 90 degrees, and is operating only as a series capacitor to reduce line impedance and increase line current. The SSSC controls the transmitted active power across transmission lines by altering or changing the characteristic impedance of the transmission line irrespective of the line current [10].

For the simple two-generator one-line system, the transmitted active power through the line can be expressed by equation 2.1.

$$P = \frac{V_1 - V_2}{X_L} \sin(\delta_1 - \delta_2) \qquad (2.1)$$

where V_1 and V_2 are the voltage amplitude of generators;

δ_1 and δ_2 are the voltage angle of generators;

X_L is the inductive line impedance.

Normally we assume $V = V_1 = V_2$ and $\delta = \delta_1 - \delta_2$. In SSSC, the transmitted active power verses transmitted phase angle relationship is shown in equation 2.2.

$$P = \frac{V^2}{X_L}\sin\delta + \frac{V}{X_L}V_q\cos\frac{\delta}{2} \qquad (2.2)$$

where V_q is the compensating voltage, negative means capacitive compensation and positive means inductive compensation.

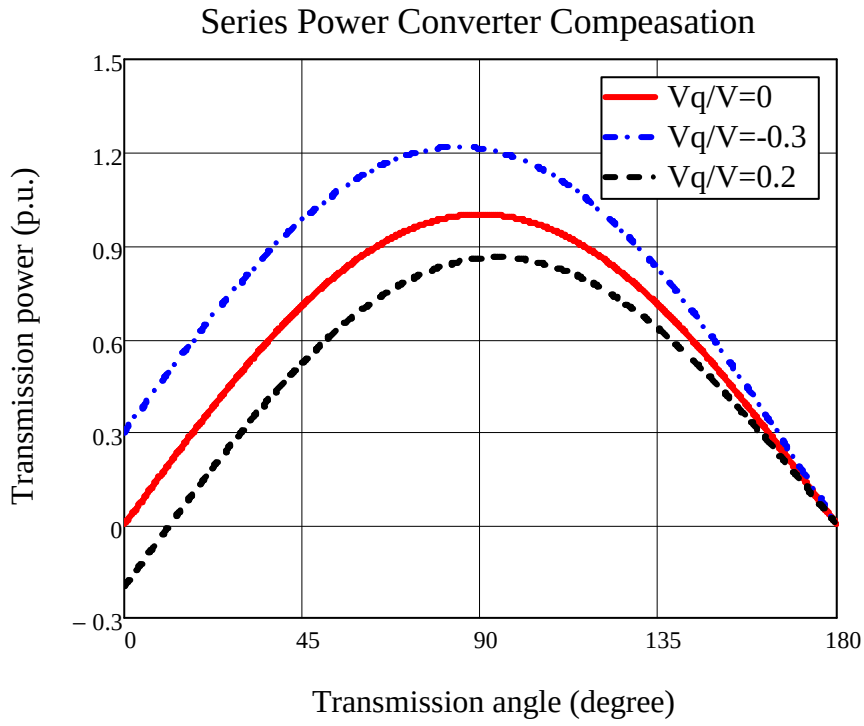


Fig. 2.1 Transmission line active power Flow by series converter compensation

If an SSSC is used for power flow control then the SSSC has an effective rating of twice that of the power converter. This means that the SSSC can increase or decrease the power flow to the same degree in either direction simply by changing the polarity of the injected AC voltage. Fig. 2.1 shows the transmitted power verses transmitted angle as a function of series compensation

Power converter based series compensation has the advantages of flexible and fast compensating voltage control compared with the static capacitor, but significant barriers limit widespread implementation of the conventional series compensator. These include:

(1) High cost due to mass components and maintenance requirement;

(2) Low reliability resulting in the lack of single fault tolerant design in a large rating converter system;

(3) Long design and build cycle because of non-standard custom design.

The modular designs of the power converter and controller have emerged as an effective solution to these obstacles.

2.2. ETO Light Power Converter

The emitter turn-off thyristor (ETO) is a novel family of high power devices with additional breakthroughs in the area of turn-off capability, power consumption and functionality [42]-[44]. Combined the thyristor's high voltage/current capability and MOSFET's easy gate control, the ETO has the following advantages: high voltage and current ratings; low conduction loss and high switching speed, allowing kHz switching.

Recently a new generation emitter turn-off thyristor was presented [46] with the following unique features: built-in device voltage, current and temperature sensors and

control power self-generation capability to remove external auxiliary power supply.

In high power applications, the standard modular design can not only simplify hardware packaging, installation and maintenance, thereby reduce the system costs and improving the system reliability, but also make the system scalable and expandable in terms of power capability, thus reducing the length of the design and build cycle.

In order to truly benefit from the modular concept, the converter circuit topology, the cooling system, auxiliary power system and the digital controller are required to be modular in substance.

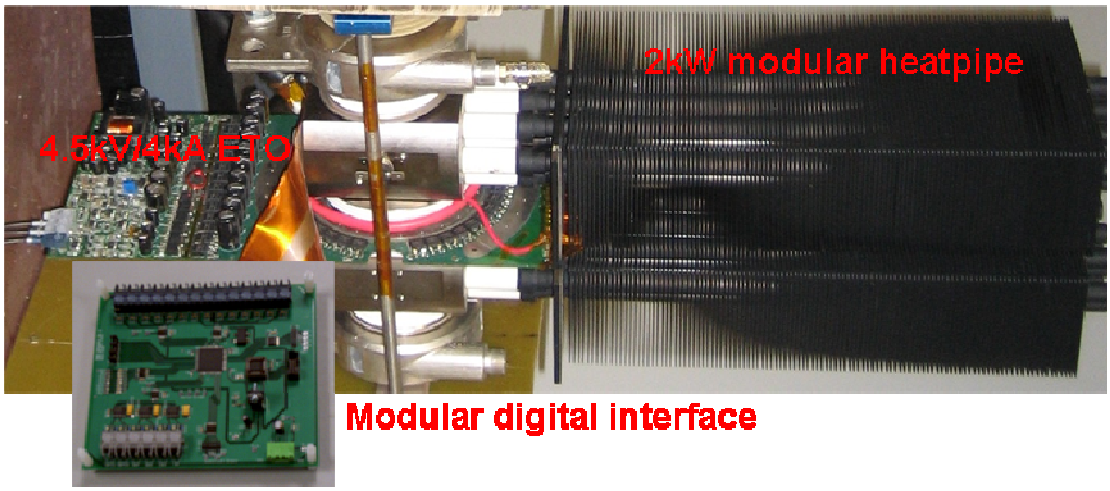


Fig. 2.2 Modular ETO converter

Based on these concerns, a megawatt modular VSC, named ETO Light power converter has been developed. Combining ETO technology, modular heat-pipe cooling system, and intelligent digital interface, an ETO VSC promises to have lower cost and higher reliability, and will have significantly reduced size and weight.

Fig. 2.2 shows the three key techniques of the ETO Light converter: 4.5kV/4kA ETO device, 2kW modular heatpipe and modular digital controller.

The ETO Light converter specifications are shown in Table 2-1.

Table 2-1 ETO Light Converter Specifications

Main Device	4 kA/4.5kV ETO
Cooling system	2kW air cooling heat pipe
Dimension (m^3)	~0.6
Weight (LB)	~350
Power Rating (MVA)	1.0~2.0
Intelligence	Sensorless V, I, T sensing, Programmable self-protection
Electrical Connection	Two DC ports, Two AC ports
Control Connection	Two optical fiber inputs, Two optical fiber outputs

Because of the high silicon utilization of ETO device, the size and the power density of ETO Light converters are reduced. The interface connections are simplified. There are only two DC ports, two AC ports for electrical connection and two optical inputs and two optical outputs for the control connection. By applying intelligent digital interface, the control architecture of an ETO Light converter application can be significantly simplified [45]. The control connection between the external controller and an ETO Light converter has only two optical inputs for switch commands and two optical outputs for detection sensor signals. Including all of the modular design, the direct material cost of an ETO Light converter is only about $50k.

The intelligent functions of ETO light converter: sensorless voltage, current sensing and programmable self-protection are tested in a boost converter test bed. The input voltage is set to 150V, the duty cycle of the switch signal is expanded to increase the output voltage and peak value of current until one of them reaches the protection point.

Fig. 2.3 shows the 450A over-current protection test results. When the current reaches the protection point, the digital interface can accept and process the information from the ETO device, then generate a fault signal and block all input switching signals to protect the ETO light converter. It is noted that the real switch operation occurs slightly after the input switch signal due to the control circuit delay (2-4us).

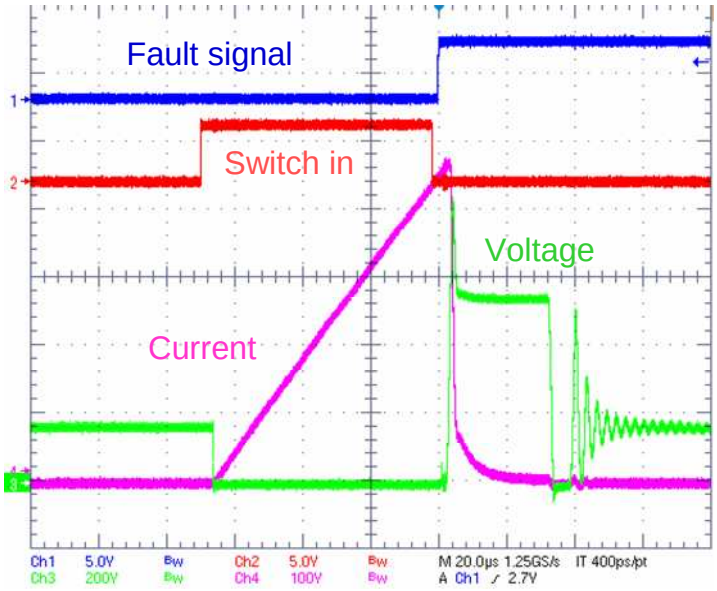


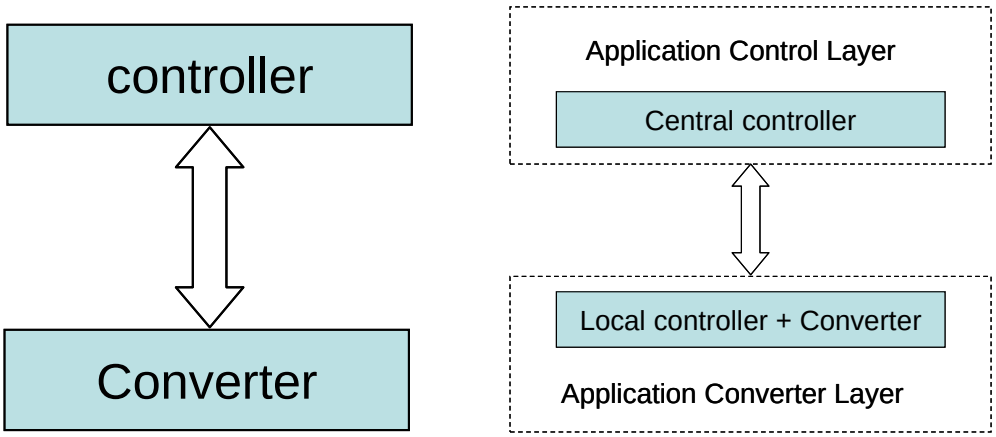
Fig. 2.3 450A over current protection function of ETO converter in boost converter (1) Fault signal (2) input switch signal (3) voltage across switch (4) current through switch

2.3. Modular Layered Controller

Conventionally, the controller and converter are separated in the power converter application, as shown in Fig. 2.4. The converter can only accept switching signals from the controller. This introduces inefficiency and complexity into the multilevel converter

especially for multilevel converter applications. Because the controller implements all control, sensor and switch functions, the controller will exceed its capability when higher power levels and more power converters are applied. In addition the power converter can function simply, even if number of converters is large. The solution to the burden polarization problem of control structure in the multilevel converter is the key point.

OSI (Open System Interface) reference layer model is a standard model for network communication. The layered design separates the design effort into smaller and more manageable slices and the different layers can be modified without affecting other layers [46].



(a) (b)

Fig. 2.4 Control structure for power converter (a) conventional (b) proposed layered structure

In this section, the modular controller design is inspired by the layered model of OSI. Three layers are designed for this model of OSI: the system control layer, the application control layer and the application converter layer. These three layers are independent of each other. It is possible to design and modify each layer separately.

The system control layer implements control strategies from the system point of view such as power flow control of the transmission line and voltage support control for the power grid. The system control layer implements the control arithmetic based on information from the application layer and sends operation signals such as duty cycle or control angles to the application layer. The detailed converter operations will be implemented in the application layers. Compared with the conventional solution, the controller operation is split into two parts, the central controller and the local controller. To modularize the controller, some functions of the controller are distributed to a local controller which is integrated with an HBBB based converter. The central controller continues to implement all of the control strategy. It sends the switch states only to local controllers instead of switch signals. That greatly reduces the fiber connection requirement. The local controller can also collect the converter information, such as voltage, current and temperature, and then send it back to the central controller via serial communication to implement the control strategy. More importantly, the local controller can process all of this converter information and protect the converter in fault situations, such as excessive voltage, excessive current and excessive temperature. The local controller and converter are combined into an intelligent converter which can protect itself regardless incorrect control inputs or interference and support the central controller with enough information for control. Based on these design considerations, the converter design is modularized, standardized and intelligent. The control calculation burden is distributed and balanced between controller and converter.

The proposed layered control structure for the power converter is shown in Fig. 2.5.

The new control structure concept breaks up the traditional boundaries of control level definitions and forms a more independent layered structure. This modular standard layer design will simplify power converter applications.

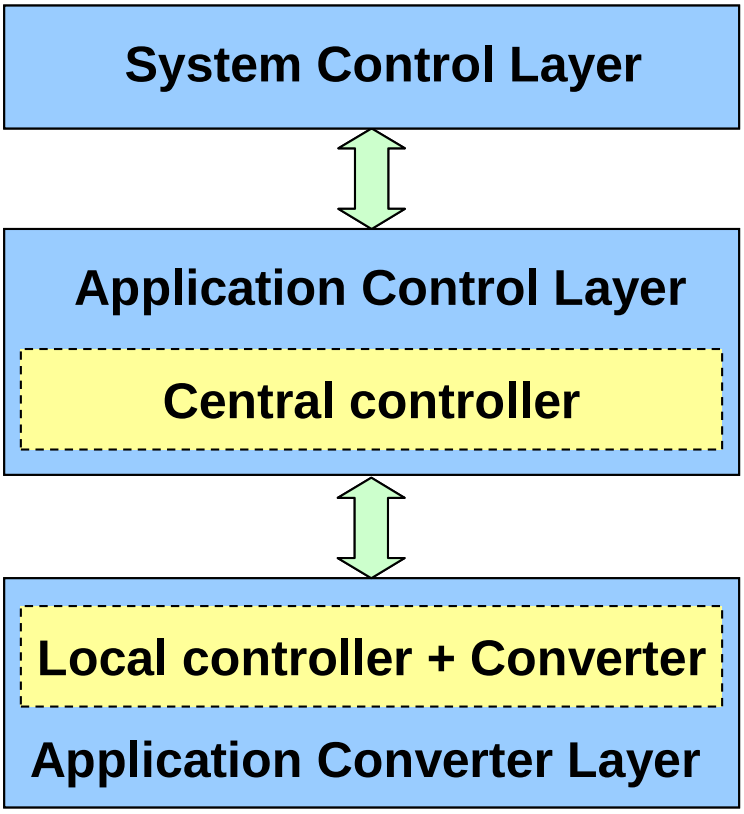


Fig. 2.5 Layered power converter control structure

A digital modular local controller is the key component of the modular converter. In this paper, a FPGA (ALTERA FLEX10KA) based digital controller is developed as a local controller. It is fully optical interface compatible, which is suitable for all optical

trigger devices, especially for the Emitter Turn-off Thyristor (ETO) device with the build-in sensor functions [44]. That design greatly increases communication reliability.

The prototype of the local controller and its interface are shown as Fig. 2.6

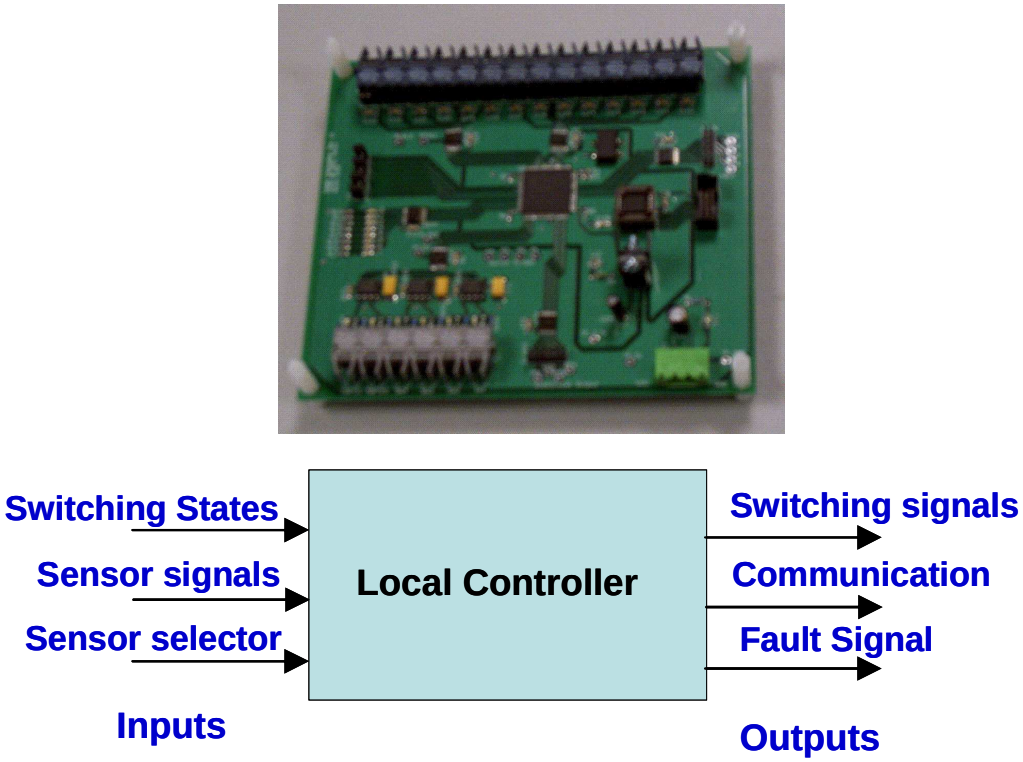


Fig. 2.6 Modular local controller prototype and its interface

The main functions of the local controller are:

·To accept the switch states from central controller and transfer them to switching signals, meanwhile flexible dead time is added to prevent shoot through.

·To gather sensor signals from the converter and translate them into digital signals and send them back to the central controller through serial communication.

·To detect sensor information and implement protection locally.

Fig. 2.7 shows the function flow chart of a local controller.

Instead of connecting all of the switch signals from central controller to converter, two switch state signals are sending from central controller to local controller. A three-level converter requires three states to produce three-level output. Two switch states can support four states. An extra state, which is usually used in diode charge mode or in shut down situations, can be used to turn off all the switches.

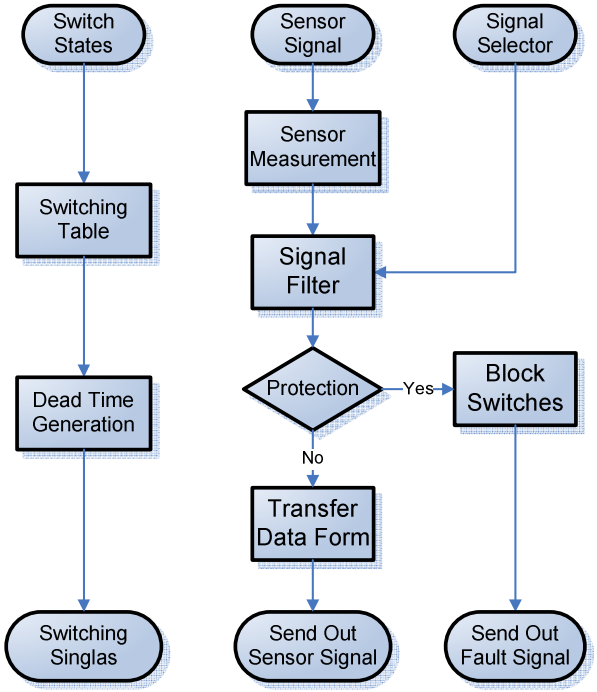
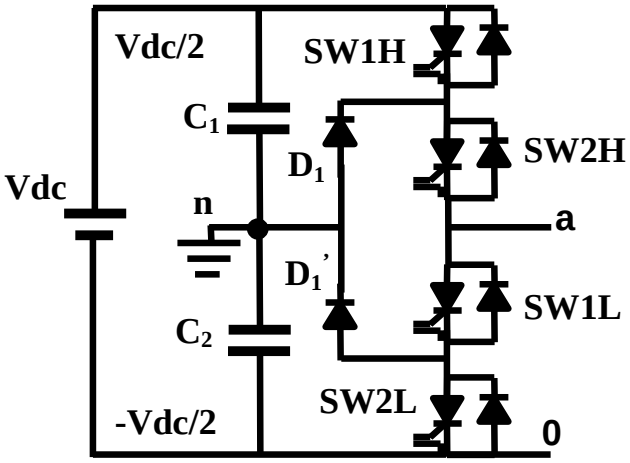


Fig. 2.7 Function diagram of local controller

This adaptation simplifies the interface greatly. Not only is it suitable for an HBBB based converter, the switch state's definition of the local controller is also compatible with NPC (Neutral Point Clamped) topology, and is called diode clamped topology. The switch states and three level outputs of these two topologies are shown in Fig. 2.8 and Fig. 2.9.



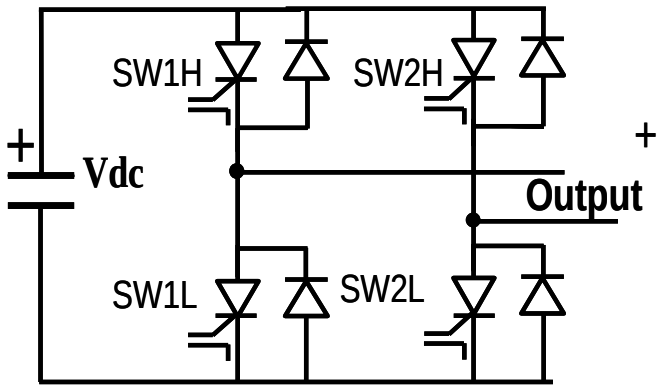
SW STATES	00	01	10	11
SW1H	0	0	0	1
SW1L	1	1	0	0
SW2H	0	1	0	1
SW2L	1	0	0	0
V_{an}	-Vdc/2	0	X	Vdc/2

Fig. 2.8 3-leve NPC converter and switch states

Table 2-2 Communication Protocol of Digital Local Controller

0-1	2 - 5	6- 14	15	16 -17
Start bit	Sensor selector	Converter voltage, current and temperature information	Parity	Stop bit

The local controller is able to send all of the information back to the central controller using serial communication via optical fiber. The optical connection increases the reliability of feedback information. Serial communication has a simple protocol and high reliability, the data protocol is shown in table 2-2.



SW STATES	00	01	10	11
SW1H	0	0	1	1
SW1L	0	1	0	0
SW2H	0	1	0	1
SW2L	0	0	1	0
Output	X	-Vdc	+Vdc	0

Fig. 2.9 3-level H-bridge converter and switch states

Since the sensor information of the converter is converted and transmitted by the local controller, the local controller can process these signals to implement the protection function.

Fig. 2.10 shows the over-voltage protection. When the voltage exceeds the protection point, all of the switch signals from the central controller will be blocked and all of the switches will be shut off. When the local controller detects the voltage is below a safe level, it will unblock all of the switches. This over-voltage protection and recovery function can limit the voltage stress across the power device. On the other hand, it can also prevent the lockup of the converter and mis-trigger of the protection function.

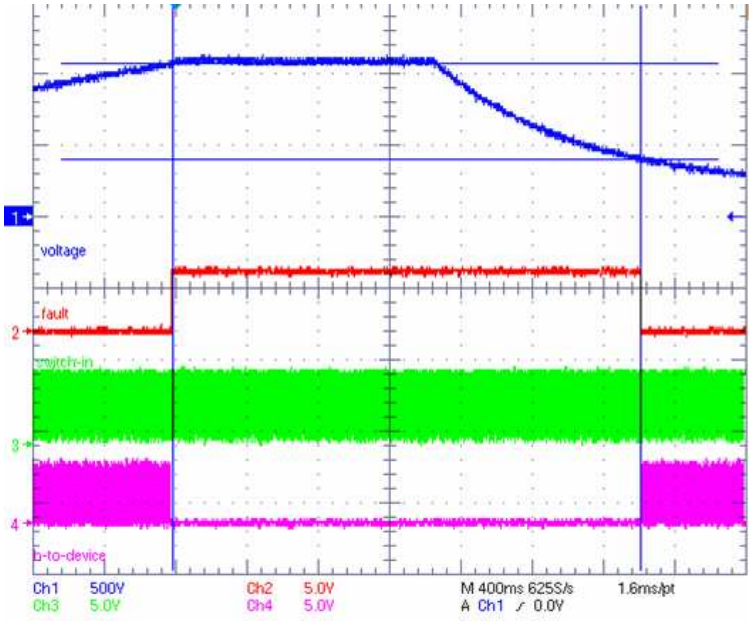


Fig. 2.10 Local over-voltage protection function of modular controller (1) voltage (2) fault signal (3) switch in (4) switch to device

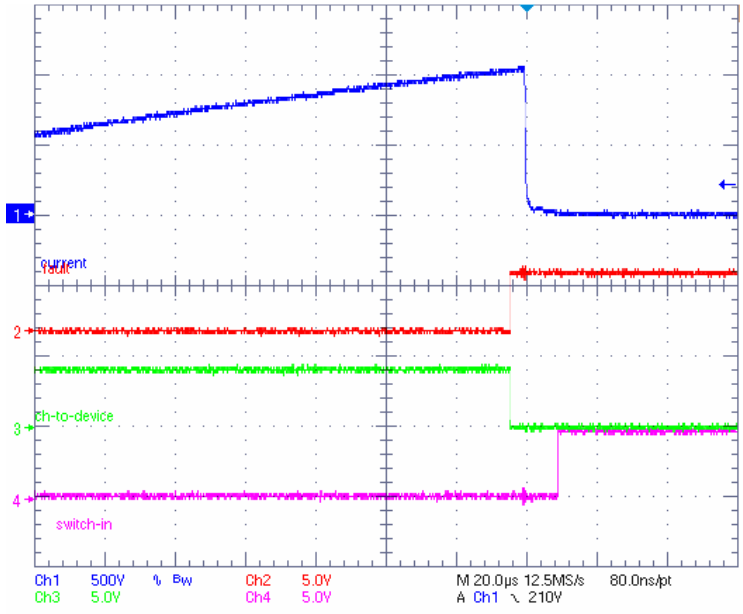


Fig. 2.11 Local over-current protection function of modular controller (1) current (2) fault signal (3) switch to device (4) switch in

Fig. 2.11 shows the over-current protection. When the current exceeds the protection point, all of the switch signals from central controller will be blocked and the converter will be shut off until the central control sends the command to release the protection.

Having all of these functions, the local controller can be integrated with a three-level power converter to form a new converter structure. This modular design makes the modularization and standardization of converter design possible. With the modular design of converter and controller, the cost of the power converter control system can be reduced significantly. Consider the converter in the Flexible AC Transmission System (FACTS) as an example, the conventional converter costs $120 - $150 per kVA, while by using the proposed control structure, the estimated cost of converter will be reduced to less than $50 per kVA.

2.4. Distributed Power Flow Controller Design

The proposed converter-based distributed power flow controller has a single phase H-bridge based ETO light converter, modular controller and communication links.

Unlike conventional solutions, it connects to the power line directly without a transformer because of its high voltage and current capability. The rating of ETO light converter (1-2 MVA) is suitable for typical 138kV-500kV power transmission line applications. The communication between distributed power flow controller and station control can be through either optical or wireless communication. Fig. 2.12 shows the concept diagram of single phase distributed power flow controller.

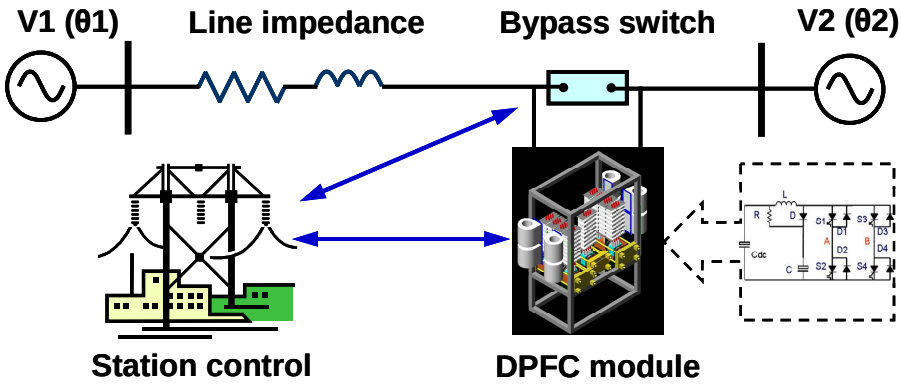


Fig. 2.12 Single phase distributed power flow controller

Because of the fully modular design, the proposed distributed power flow controller can be installed to the transmission line flexibly based on the power transmission requirement, for example, one DPFC module per 30 miles. Fig. 2.13 shows the DPFC application diagram in a three phase power transmission system.

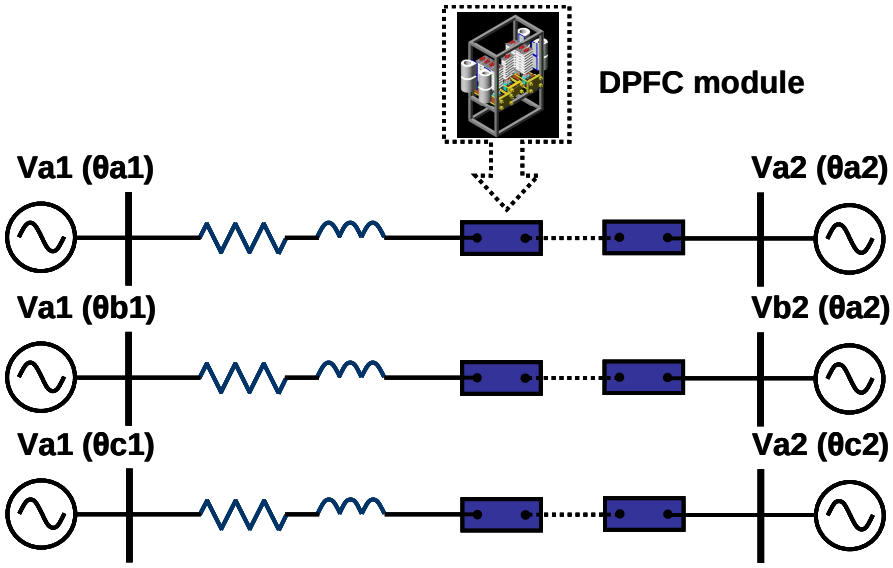


Fig. 2.13 DPFC application diagram

A controlled power transmission line implemented with multiple distributed power flow controllers can result in significant benefits:

- Enhancement of the transmission line capability and stability by changing the line impedance characteristic.
- Reduction of the cost comparing with existed FACTS series compensator
- Enhancement of reliability by applying multiple applications thus achieving redundancy
- Reduction of the time required to design and build by using standard modular design

This modular design and modular control of megawatt distributed power flow controller creates important opportunities in the power transmission system.

2.5. Operations of DPFC

The DPFC have five operation modes

(1) Stand by mode: the controller is out of service, the bypass switch S1 is turned on to pass the line current

(2) Diode Charge mode: when the operation command arrives, S1 is turned off and line current will go through converter and charge the capacitor

(3) PWM charge mode: when the voltage of DC capacitor is charged to some level, the controller has power and the voltage loop of DC voltage is working and regulating DC voltage to the reference value.

(4) Service mode: power converter is operating in the capacitive mode and acts as a capacitor, the line impedance decreases and the line current and active power flow increases.

(5) Discharge mode: power converter is operating in the inductive mode and acting as inductor, the line impedance increases and the line current and active power flow decrease.

2.6. Summary

The ETO light converter based distributed power flow controller is proposed in this chapter. The ETO Light modular VSC has a very simple configuration and fully modular design, allowing for flexible and widespread use in FACTS and other industry applications requiring high power converters. The modular digital local controller is developed. The feasibility is verified by experimental tests. The ETO light converter based distributed power flow controller concept overcomes some serious limitations of FACTS devices such as high cost, low reliability and long building cycles. The new approach shed lights on high power converter applications in FACTS. The controller of DPFC is simulated and verified. The modeling development and control design of DPFC will be presented in the next chapter. More simulation and experimental results will be presented later.

Chapter 3. Distributed Power Flow Controller Modeling and Control

The power flow controller is a reactive series compensator employing a voltage source converter in series with the transmission line. An effective feedback control relies on a well-defined model of the target system. However a general model development for the power flow controller has not been shown in the previous work. In this chapter, a simple and accurate converter and system model development for power flow controller based on per phase control, both in stationary and synchronous (DQ0) frames, are proposed and introduced. By deriving an accurate switching, average and small signal models and determining the transfer functions, feedback control laws can be well designed and applied to the controller in order to realize good static and dynamic performance of the power flow controller.

3.1. Operation Principles of the Power Flow Controller

The schematic of a single phase distributed power flow controller is shown in Fig. 3.1. The DFPC system is comprised of two main parts: a modular H-bridge voltage source converter with a separate dc link capacitor and a digital controller with measurements.

As previously discussed, modular voltage source converters are identical H-Bridge converters, whose output is connected in series directly with the transmission line. To make the entire system work effectively and perform properly, a carefully designed controller is required. All the necessary line voltages and currents are measured and fed

into the controller to be compared with controller commands. The controller then performs feedback control and outputs a set of switching signals driving the main power semiconductor devices of the power converter.

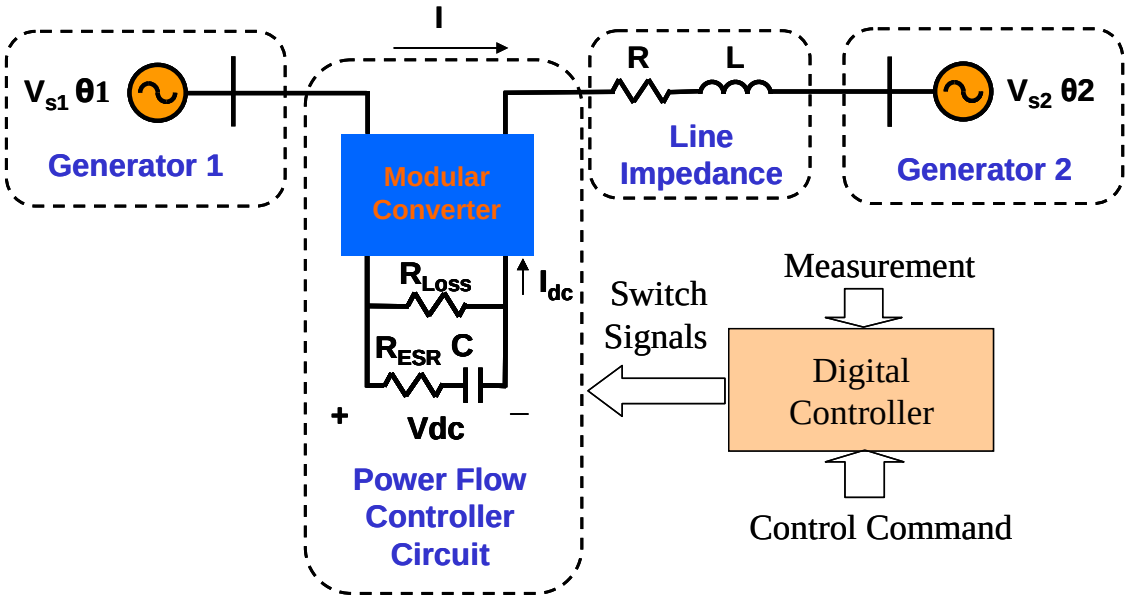


Fig. 3.1 Schematic of DPFC control system

One of the primary functions of a power flow controller is the provision of active power flow control for the transmission line. The power flow on a transmission line can be controlled by changing the converter's output voltage to affect transmission line impedance. If the converter is to be operated in capacitive mode, +Q, the converter output voltage lags the line current by 90º and the power flow controller acts as a series capacitor to reduce line impedance and increase the transmitted active power. If the converter is to be operated in inductive mode, -Q, the converter output voltage leads the line current by 90º and the power flow controller acts as a series inductor to increase line impedance and reduce transmitted active power..

For practical applications, the converter is associated with internal losses caused by connection loss and the power semiconductor devices used as the converter's passive components. As a result with no control, the dc capacitor voltage will decrease. In order to regulate the capacitor voltage and maintain regular operation of DPFC, a phase shift of the current and the voltage will be applied to ensure a small amount of real power exchange between the converter and the power grid.

3.2. Distributed Power Flow Controller Model Development

This section proposes and introduces a development procedure of the model and control development of the single phase distributed power flow controller. Fig. 3.2 illustrates the control development block diagram, showing the relationship between the modeling and feedback control design. This process starts with model development which can provide key transfer functions of the control parameters to state variables such as DPFC (transmission line) currents and DC capacitor voltage. Feedback control is designed and evaluated based on derived transfer functions to ensure good performance of the entire distributed power flow controller system. Based on the proposed modeling method, the stability of the feedback loops can be systematically evaluated and guaranteed. The loop gains are then modified to achieve as much stability as possible, while dynamic response is not sacrificed. These control techniques are validated by both computer simulations and experimental test results.

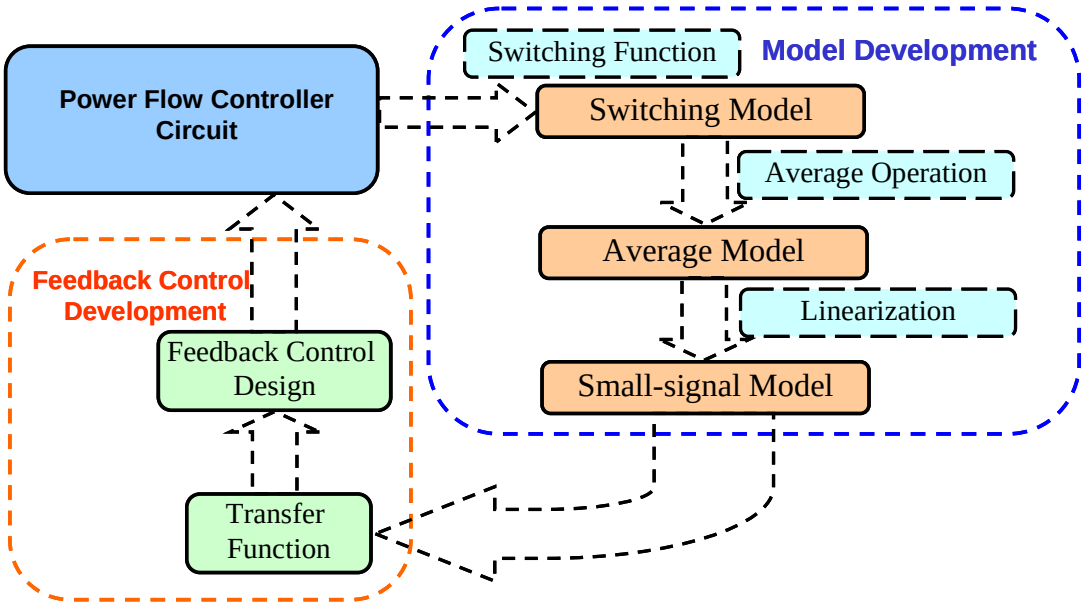


Fig. 3.2 Control development for the power flow controller

3.3. Model Development

Model development process starts with generating a switching model of the power converter and then an average model in a single-phase coordinate. The average model is integrated with a linear model of an AC power system. The linear model of the AC power system includes one equivalent ac source. In order to implement the decoupling controller, the average model of the power flow controller in single-phase coordinate is transformed into a model in DQ0 coordinates. To design feedback control loops using linear compensators, a small signal model of the ac system in DQ0 coordinates is derived for its average model in the same coordinates. Fig. 3.3 shows a diagram of the model development of the modular converter based DPFC.

The model development flow chart is shown in Fig. 3.3. The modeling process starts with a definition of the switching functions of each converter cell in the CMC. The CMC

is represented by a switching model in an abc coordinate system. The next step in the modeling process is to apply the average operator to the switching functions. During this step all of the switching functions are neglected and only the fundamental components are considered. Duty cycles are the main control parameters that are derived from the average model. Duty cycles are used to provide switching signals to the CMC. First, a generalized average model is derived in abc coordinates. This model can be used in any type of power-conversion system. The derived average model of the SSSC is combined with the linear model of a three-phase ac system. The combined model constitutes the equivalent average model for the system under study.

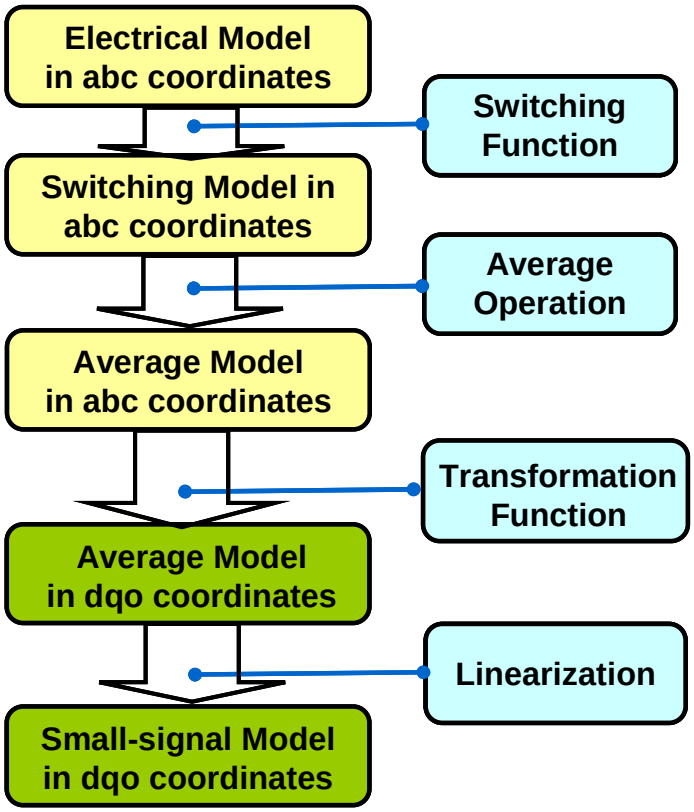


Fig. 3.3 Model development procedures

According to the flow chart, the average in the single phase coordinate frame must be transferred to an average model in the DQ0 frame for AC system. Once the average model in single-phase coordinate has been transferred into DQ0 coordinates, a linearization step is necessary to derive the small signal model for the power flow controller. Transfer functions for the system are then derived from the small signal model. In the synchronous frame, all ac parameters become dc parameters. In other words, the converter behaves similar to a dc-to-dc converter. As a result, classical linear control techniques can then be applied to the H-bridge voltage source converter. Since simple linear control techniques can be applied, the stability and feedback loops can be evaluated and the control parameters can be optimized for peak performance. Also, the real and reactive components of the system can be controlled independently of one another.

Switching Sequence

The H-Bridge converter is the basic converter topology we are using for analysis. The simplified structure of the H-Bridge is shown in Fig. 3.4.

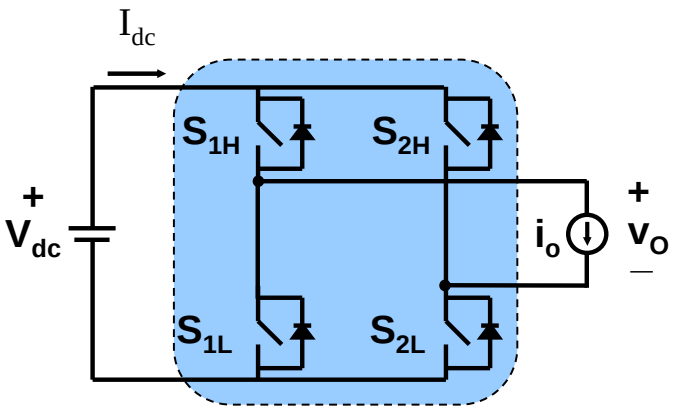


Fig. 3.4 Basic structure of one H-Bridge converter

There are three possible output voltage levels that can be synthesized from the possible switching combinations. These voltage levels are shown in Fig. 3.5.

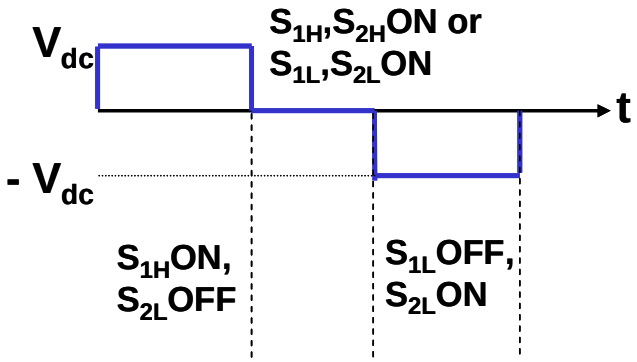


Fig. 3.5 Output voltage of H-Bridge converter

In order to prevent a short-through circuit, the top and bottom switches in the same phase leg of the H-bridge cannot be turned on at the same time. That means that the top switch and the bottom switch must be complementary. The equivalent circuit of the H-Bridge is shown in Fig. 3.6. Then we can get the switching model of H-bridge converter which is shown as Fig. 3.7. To illustrate the relationship between the output current and voltage on the dc side of the converter and on the ac side of the converter, four possible switch combinations and switching model are shown in Table 3-1.

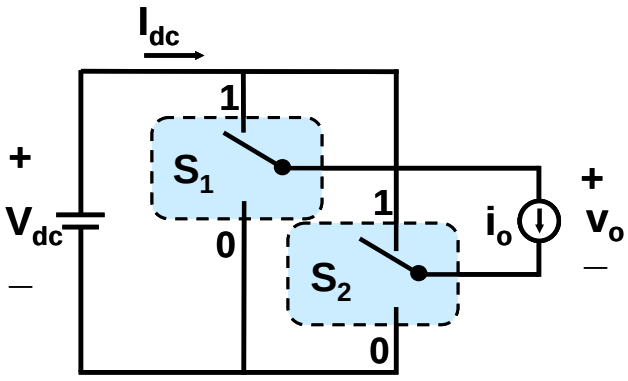


Fig. 3.6 Equivalent circuit of the H-Bridge converter

Table 3-1 H-bridge Converter Switching Combinations

S_1	S_2	S	V_o	I_{dc}
0	0	0	0	0
1	0	1	Vdc	i_o
0	1	-1	-Vdc	$-i_o$
1	1	0	0	0

The relationship between the dc voltage and the converter output voltage as well as the capacitor current and the converter output current are represented in equations 3.1 and 3.2. The converter output current equation must be equal to the line current of the power system because the SSSC is connected in series with the power system.

$$V_o = (S_1 - S_2)V_{dc} \qquad (3.1)$$

$$i_E = (S_1 - S_2)i_o \qquad (3.2)$$

S_1 can be defined as the difference between the statuses of the two top switches.

$$S = S_1 - S_2 \qquad (3.3)$$

By substituting equation 3.3 into equations 3.1 and 3. 2

$$V_o = SV_{dc} \qquad (3.4)$$

$$i_E = Si_o \qquad (3.5)$$

The derived switching model for the H-Bridge converter is shown in Fig. 3.7. Each H-Bridge converter shown in Fig. 3.6 can be replaced by the switching model. The result is the final switching model of the CMC shown in Fig. 3.7.

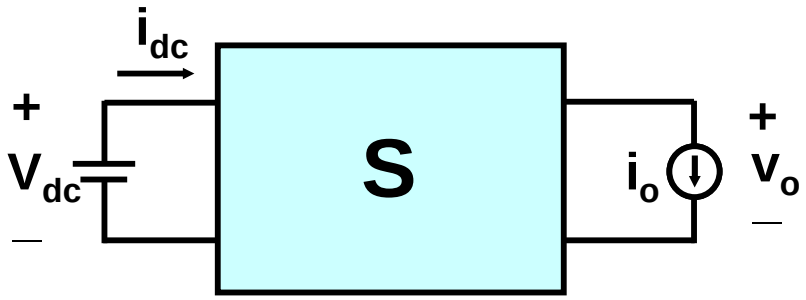


Fig. 3.7 Switching model of the H-Bridge converter

Average Model in single phase Coordinate

In order to develop the average model of the H-Bridge Converter, the switching functions are averaged to take into account the switching behavior and the harmonic components for all parameters. The average operator is expressed in equation 3.6.

$$d = \overline{S}(t) = \frac{1}{T}\int_{t-T}^{t} S(\tau)d\tau \qquad (3.6)$$

S(τ) in equation 3.6 is defined as the switching function of the VSC and d and are defined as the average values of the switching function defined here as the duty $\bar{S}(t)$ cycles.

The average operator is applied to equation 3.4, and equation 3.5, the duty cycle for the switching function S(t) is d_1 from time 0 to T. The behavior of the average switching function is shown in Fig. 3.8.

From Fig. 3.8, it can be stated that the average switching function for time T to 2T is $-d_2$. The green line represents the average switching cycle of a switching function.

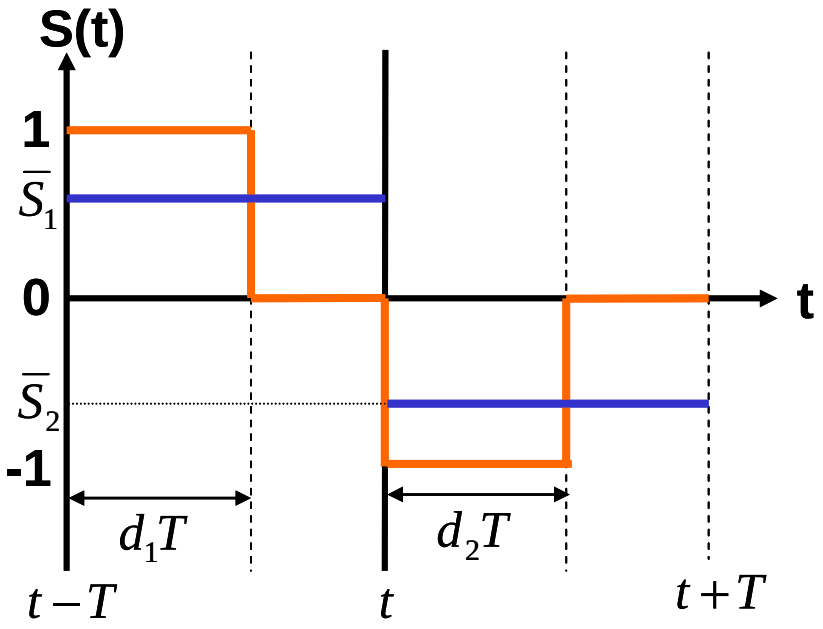


Fig. 3.8 Average switching function over a switching cycle

The next step in the development of the average model of the H-Bridge Converter is to apply the average operator to the voltages and currents of equation 3.4 and equation 3.5. The right hand side of both the current and voltage equations consists of two quadratic terms. These quadratic terms are to the result of the multiplication of two time-dependent terms. Before the average operator can be used on equation 3.4 and equation 3.5, something must be done to simplify the quadratic terms on the right-hand side of both equations. To do this, several assumptions must be made. First, the dc voltages must be reasonably assumed to be constant during one switching cycle. Second, the output currents must be reasonably assumed to be constant during one switching cycle. These assumptions are valid for two reasons. First, the dc-link capacitors are relatively large for high power applications such as the series compensation; therefore, their voltages do not

change very much over a switching period. Second, the switching frequencies of the high power semiconductor devices used in the power flow controller are significantly higher than the fundamental frequencies of the power system. For example, the switching frequency of the H-bridge voltage source converter is in the range of 300 Hz to 2 kHz; whereas, the fundamental switching frequency of the power system is in the range of 50 Hz to 60 Hz.

If the average operator is applied to equation 3.4, the average voltage equation becomes:

$$\bar{v} = \frac{1}{T}\int_{t-T}^{t} S(\tau)d\tau * V_{dc} = d * V_{dc} \qquad (3.7)$$

If the average operator is applied to the current equation 3.5 the result is as follows:

$$\overline{i_{dc}} = d * i_o \qquad (3.8)$$

The converter's output current is as same as the line current of the power grid because the power flow controller is connected in series with the transmission line.

The average model in single-phase coordinate for the distributed power flow controller is shown in Fig. 3.9. The ESR of the high-power dc capacitors is neglected in the average model because it is relatively small compared to the impedance of the dc capacitors.

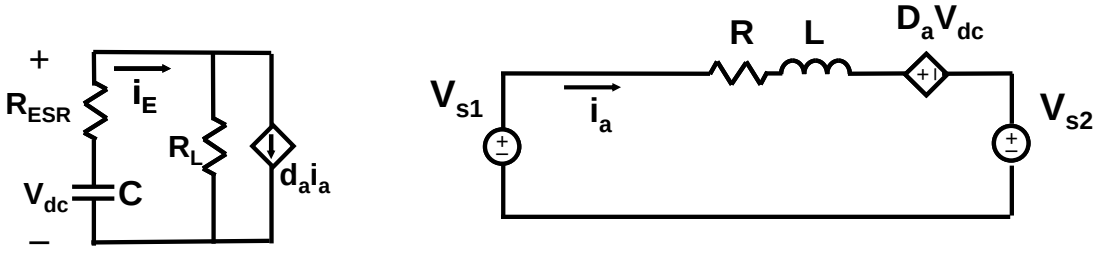


Fig. 3.9 Average model of single phase power flow controller

The single-phase output-current differential equation matrix for the average model is:

$$\frac{di_a}{dt} = \frac{V_{dc} * d_a}{L} - \frac{V_{eq}}{L} - \frac{R}{L} i_a \qquad (3.9)$$

The three-phase dc-link voltage differential equation matrix for the CMC is:

$$\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_L C} - \frac{d_a i_a}{C} \qquad (3.10)$$

Average Model in DQO Coordinates

Normally the Park's transformation is widely used to transform AC of the abc stationary frame to DC of the DQ0 synchronous frame in the three-phase system to simplify the control system and apply the decoupled control.

Park's Transformation Matrix is defined as follows:

$$\vec{T}_{dq0/abc} = \sqrt{\frac{2}{3}} * \begin{bmatrix} -\sin\theta & -\sin(\theta - \frac{2}{3}\pi) & -\sin(\theta + \frac{2}{3}\pi) \\ \cos\theta & \cos(\theta - \frac{2}{3}\pi) & \cos(\theta + \frac{2}{3}\pi) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \qquad (3.11)$$

where ω(τ) is the angular velocity $\theta = \int_0^t \omega(\tau) d\tau + \theta(0)$.

In a single phase system, it is possible to create a second quantity in quadrature with the real one so as to apply the transformation from the static to the synchronous frame.

The transformation to the synchronous frame DQ requires two orthogonal components. In three-phase systems the abc components are transferred to the orthogonal and stationary α β frame system and then to the synchronous frame DQ as shown as Fig. 3.10.

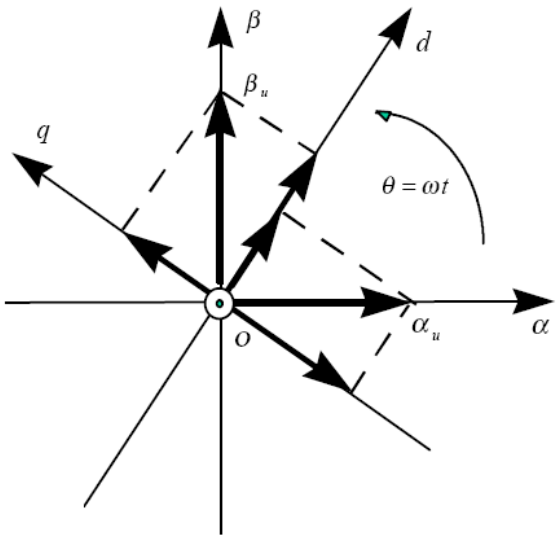


Fig. 3.10 Stationary frame to synchronous frame transformation

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \qquad (3.12)$$

Another simple way to implement single phase DQ transformation, an accurate extraction of single ac information can be used to find the dc information in a single phase ac signal.

For a single phase signal

$$X(t) = X_m \times \sin(\omega t - \phi) \qquad (3.13)$$

can be broken down in two orthogonal sinusoidal signals

$$X(t) = X_d \sin(\omega t) + X_q \cos(\omega t) \quad (3.14)$$

where

$$X_d = X_m \cos(\phi)$$
$$X_q = -X_m \sin(\phi) \qquad (3.15)$$

According to the decoupling control scheme, the control variables in DQ0 can be derived from the differential equations for the voltage and current which are represented in Fig. 3.11.

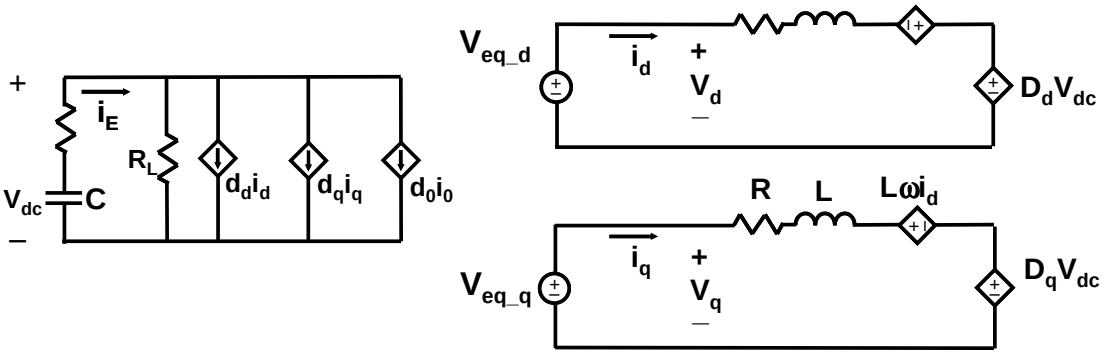


Fig. 3.11 Simplified average model for the DPFC in DQ0 coordinates

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{E}{L} * \begin{bmatrix} d_d \\ d_q \\ d_0 \end{bmatrix} - \frac{1}{L} * \begin{bmatrix} V_{d_eq} \\ V_{q_eq} \\ V_{0_eq} \end{bmatrix} - \frac{R}{L} * \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} \omega * i_q \\ -\omega * i_d \\ 0 \end{bmatrix} \qquad (3.16)$$

$$\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_L C} - \frac{1}{C}\begin{bmatrix} d_d & d_q & d_0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \qquad (3.17)$$

Using equation 3.16 and equation 3.17 the small signal model for the DPFC System is shown in Fig. 3.11.

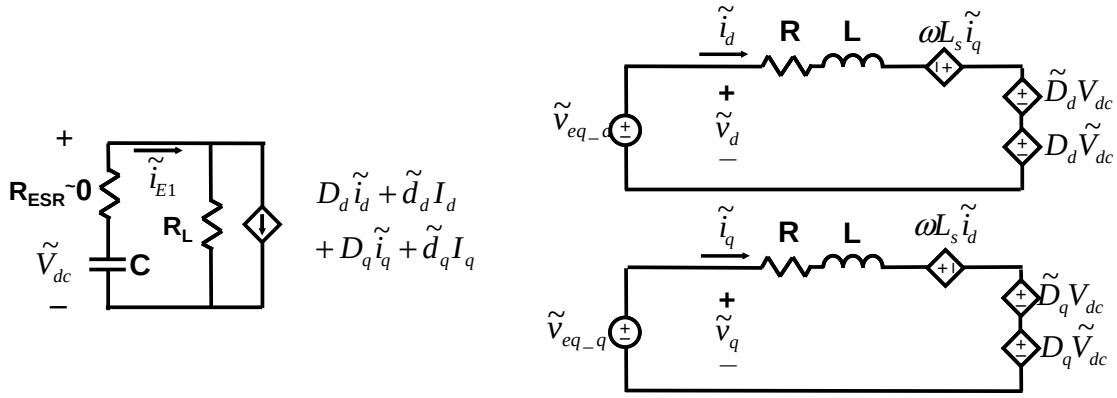


Fig. 3.12 Small-signal model of DPFC in DQ0 coordinates

The small signal transformation can be derived as

$$\frac{d}{dt}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{i}_0\end{bmatrix}=\frac{E}{L}\begin{bmatrix}\tilde{d}_d\\ \tilde{d}_q\\ \tilde{d}_0\end{bmatrix}-\frac{1}{L}\begin{bmatrix}V_{d_eq}\\ V_{q_eq}\\ V_{0_eq}\end{bmatrix}-\frac{R}{L}\begin{bmatrix}\tilde{i}_d\\ \tilde{i}_q\\ \tilde{i}_0\end{bmatrix}+\begin{bmatrix}\omega\ \tilde{i}_q\\ -\omega\tilde{i}_d\\ 0\end{bmatrix} \tag{3.18}$$

$$\frac{d\tilde{E}}{dt}=-\frac{\tilde{E}}{R_L C}-\frac{1}{C}(\tilde{d}_d i_d+d_d\tilde{i}_d+\tilde{d}_q i_q+d_q\tilde{i}_q) \tag{3.19}$$

Since DPFC only supplies reactive power to the network and not active power, the decision was made to align the voltage in the DQ0 frame with the Q axis because the Q axis is responsible for the reactive components of the DPFC.

As a result, the average output-current differential equation matrix in DQ0 coordinates for the HBBB-Based DPFC is expressed as follows:

$$\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\\ i_0\end{bmatrix}=\frac{E}{L}*\begin{bmatrix}d_d\\ d_q\\ d_0\end{bmatrix}-\frac{1}{L}*\begin{bmatrix}V_{d_eq}\\ V_{q_eq}\\ V_{0_eq}\end{bmatrix}-\frac{R}{L}*\begin{bmatrix}i_d\\ i_q\\ i_0\end{bmatrix}+\begin{bmatrix}\omega*i_q\\ -\omega*i_d\\ 0\end{bmatrix} \tag{3.20}$$

The differential equation matrix in the DQ0 coordinates for the dc-link voltage is as follows:

$$\frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R_L C} - \frac{1}{C}\begin{bmatrix} d_d & d_q & d_0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \qquad (3.21)$$

Open-Loop Transfer Function Derivation

Using equation 3.20, and equation 3.21, there are four possible open-loop control transfer functions that can be derived. They are as follows:

Control-to-Output-Current considering the cross coupling transfer functions:

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d + \tilde{i}_q \omega L / V_{dc}} \text{ and } G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_d - \tilde{i}_d \omega L / V_{dc}}$$

Control-to-DC-voltage transfer function

$$G_{vdd} = \frac{\tilde{V}_{dc}}{\tilde{d}_d}$$

Current-to-DC voltage transfer function

$$G_{vid} = \frac{\tilde{V}_{dc}}{\tilde{i}_d}$$

We can get the control to D-channel output current transfer function:

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d + \tilde{i}_q \omega L / V_{dc}} = \frac{\frac{V_{dc}}{L}}{s + \frac{R}{L}} \qquad (3.22)$$

Likewise, the transfer function G_{iq} is:

$$G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_d - \tilde{i}_d \omega L / V_{dc}} = \frac{\frac{V_{dc}}{L}}{s + \frac{R}{L}} \qquad (3.22)$$

Using the DC capacitor circuit shown in Fig. 3.12, with perturbations of the D-channel and Q-channel currents, yield:

$$G_{vdd} = \frac{\tilde{V}_{dc}}{\tilde{d}_d} = -\frac{\frac{I_d}{C}}{s + \frac{1}{RC}} \qquad (3.23)$$

$$G_{Vid} = \frac{\tilde{V}_{dc}}{\tilde{i}_d} = -\frac{\frac{D_d}{C}}{s + \frac{1}{R_L C}} \qquad (3.24)$$

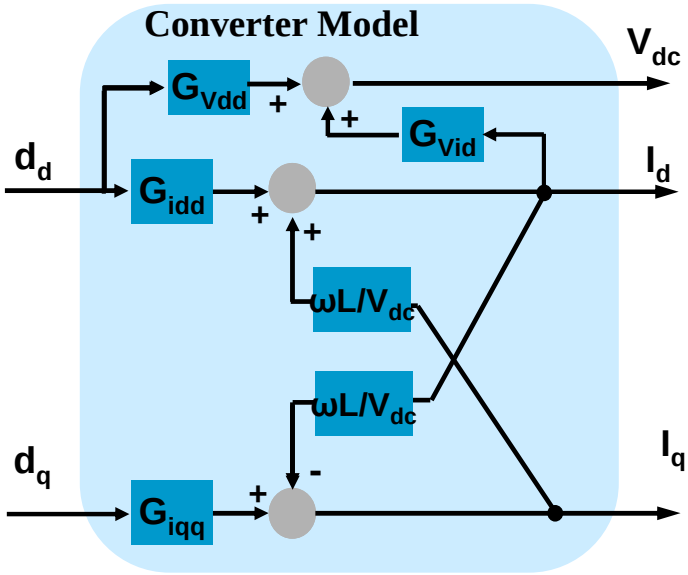


Fig. 3.13 Open-loop transfer function of single phase power flow controller

The block diagram of the open-loop transfer functions of single-phase power flow controller is shown as Fig. 3.13.

3.4. Closed-loop Control Design

The derived power flow controller model above is used in the design process. Real and reactive power exchanged between the power flow controller and the power grid can be controlled independently by decoupling the real and reactive components of the power flow controller into d-Channel and q-Channel components.

The proposed SSSC system, as shown in Fig. 3.14.

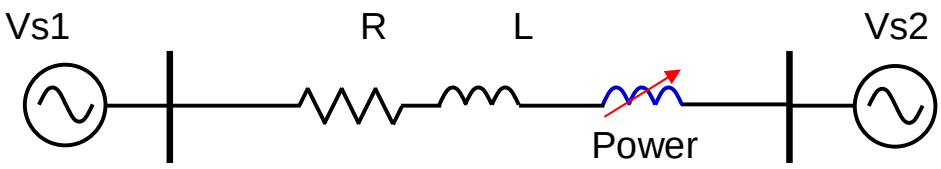


Fig. 3.14 Proposed DPFC System

It is formed by a modular voltage source converter based DPFC, power sources and line impedance.

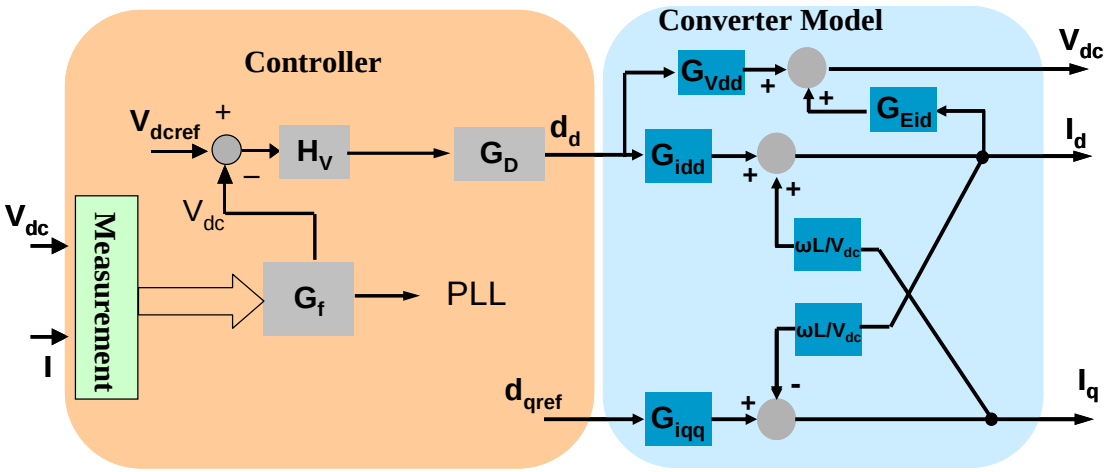


Fig. 3.15 Open-loop block diagram for the direct voltage control scheme

Fig. 3.15 shows the proposed direct voltage control diagram of DPFC.

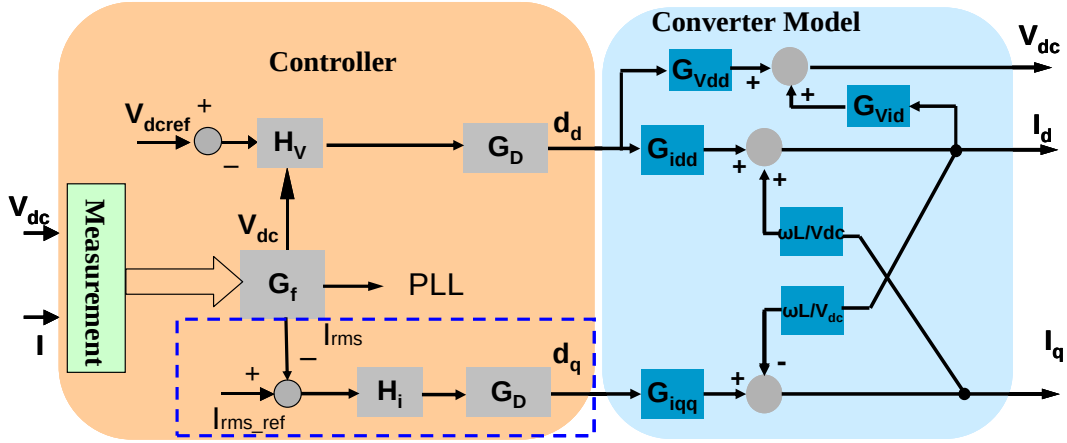


Fig. 3.16 Indirect curernt control block diagram

Fig. 3.16 demonstrates the indirect current control block. The d axis duty cycle is given by the error of the current reference and the measured current. The line current and the DC capacitor voltage are regulated.

For a real digital controller based control system, the digital delay and low pass filter for sensor signals influence for the controller design are considered.

$$\text{Digital delay: } G_D = \frac{1-\frac{sT_D}{2}}{1+\frac{sT_D}{2}} \tag{3.25}$$

where Td is the total digital delay including calculation, A/D conversion and switching delay.

$$\text{Low pass filter: } G_f = \frac{1}{1+sRC} \tag{3.26}$$

Based on the above description, the control loop can be described as:

Current loop gain

$$T_{id} = H_{id} G_{id} G_D \qquad (3.27)$$

Voltage loop gain

$$T_v = H_{vd} (G_{Vdd} + G_{idd} G_{Vid}) G_D G_f \qquad (3.28)$$

Since $G_{idd} G_{Vid}$ has the higher order information compared with G_{Vdd}, The voltage loop gain could be simplified as:

$$T_v = H_{vd} G_{Vdd} G_D G_f \qquad (3.29)$$

In order to verify the control performance of distributed power flow controller, a single phase two machine system is introduced shown as Fig. 3.17.

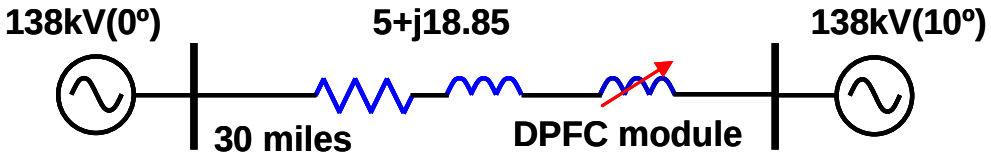


Fig. 3.17 Single phase power flow control diagram

Table 3-2 Simulation Specifications

Line to line voltage of generator 1 (kV)	138
Voltage phase of generator 1	0
Line to line voltage of generator 2 (kV)	138
Voltage phase of generator 2	10
Line impedance of 30-mile line(ohm)	5+j18.85
Line current (A)	870
Switching frequency (Hz)	1020
DC voltage of total converter (V)	2500
Injection voltage	2%
DC capacitance(mF)	16.2
Internal converter loss (kW)	1

The simulation parameters are shown in Table 3-2.

The current loop gain plot is shown as Fig. 3.18.

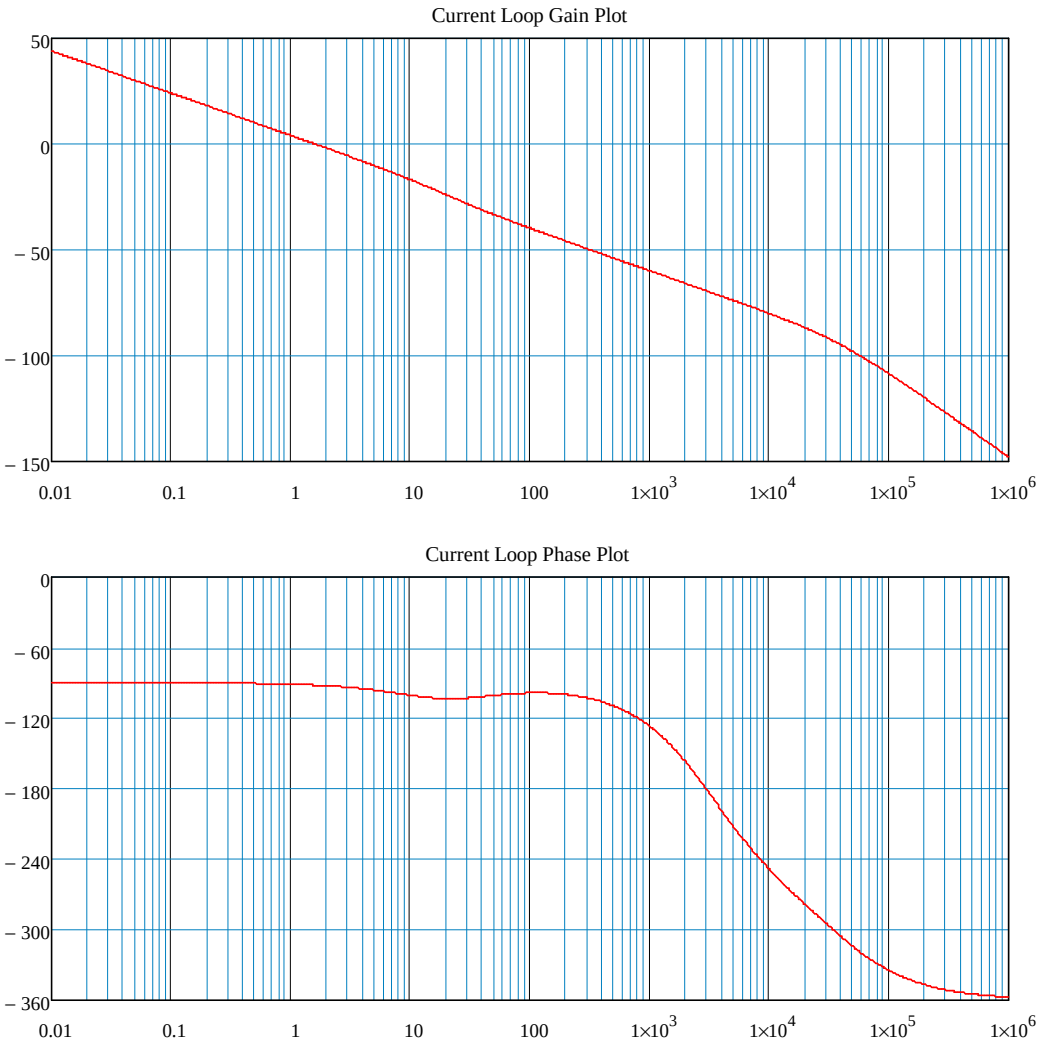


Fig. 3.18 Current loop bode plot

The cross-over frequency is about 200Hz which is about the one fifth of the switching frequency 1020Hz and the phase margin is about 90^{o} .

The voltage loop gain plot is shown as Fig. 3.19.

The cross-over frequency is about 20Hz and the phase margin is about 110^{o} .

The voltage loop is much slower than the current loop to get the good control performance.

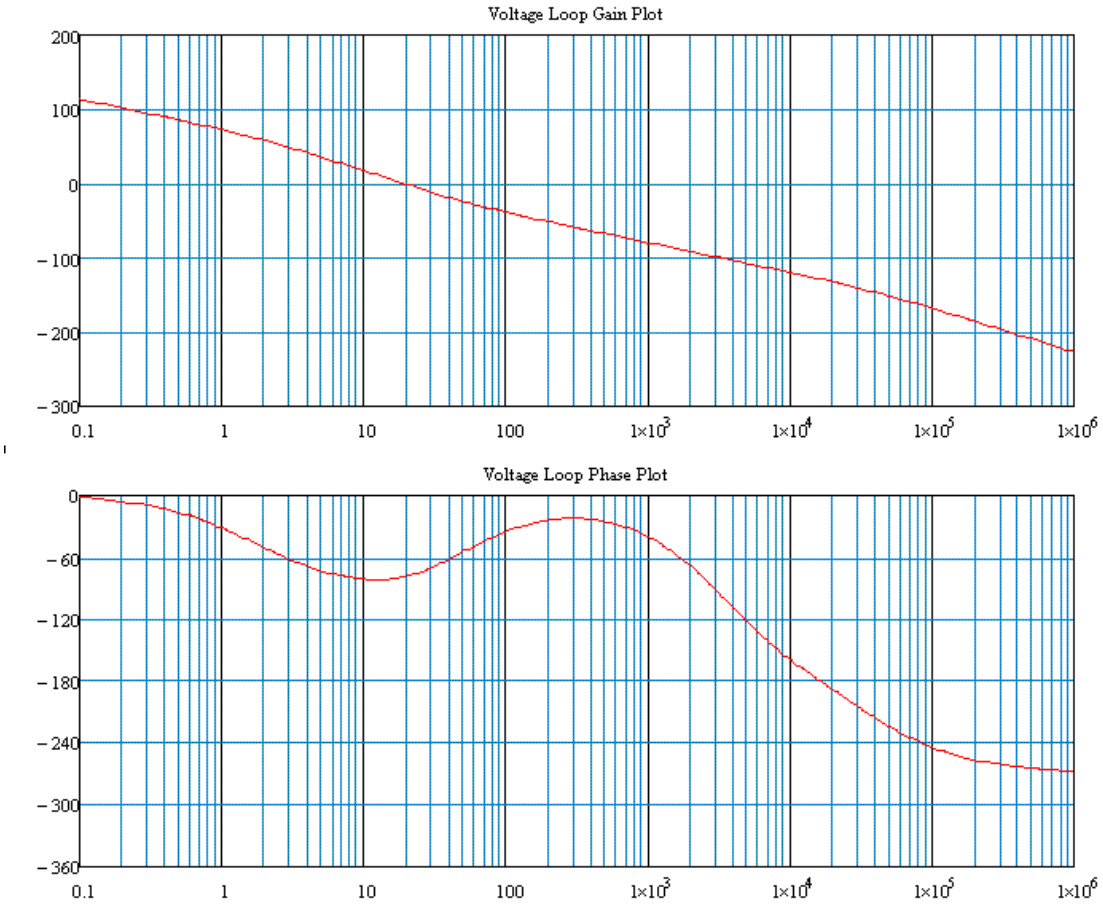


Fig. 3.19 Voltage loop bode plot

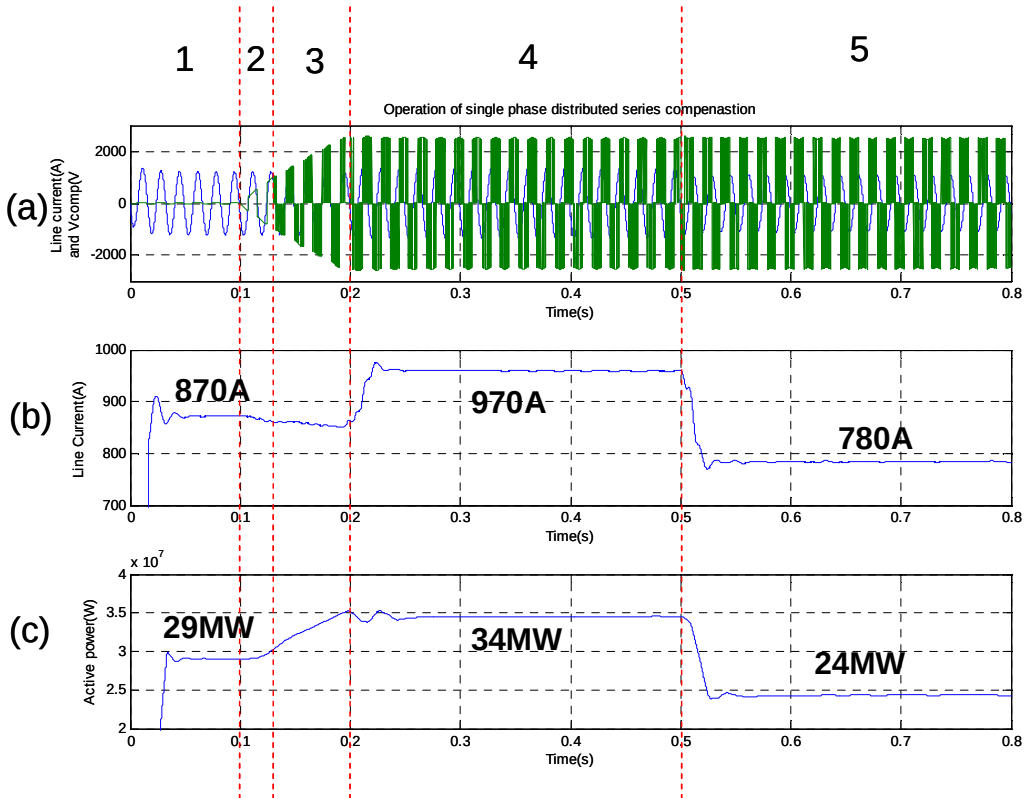


Fig. 3.20 Simulation results of DPFC (a) line current and compensating voltage. (b) line current RMS value. (c) transmitted active power.

A single phase power flow controller is designed to control the power flow through the transmission line. Sinusoidal Pulse Width Modulation (SPWM) is used to control the power converter. Controller is designed to support the voltage in DC capacitor and generate the compensating voltage to the power line. Then the designed distributed power flow con

The simulation results are shown as Fig. 3.20.

The operations of DPFC have five steps

(1) The controller is out of service, the bypass switch S1 is turned on to pass the line current

(2) When the operation command is coming, S1 is turned off and line current will go through converter and charge the capacitor

(3) When the voltage of DC capacitor is charged to some level (1000V in the simulation), the controller has the power supply, and then the voltage loop of DC voltage is working and regulate the DC voltage to the reference value.

(4) Power converter is operating in the capacitive mode and acting as capacitor, the line impedance decrease and the line current and active power flow increase.

(5) Power converter is operating in the inductive mode and acting as inductor, the line impedance increase and the line current and active power flow decrease.

From the simulation results, we can notice that the control parameters work fine for the DPFC controller to achieve the expected control performance.

Gain scheduling controller design for operating condition variation

From equation 3.23 and 3.29, we can find that the voltage loop is related to the line current value which is one important measurement of the DPFC application. When the current is small, the low frequency gain of the voltage loop is getting small. That will slow down the voltage loop speed and affect the control loop transient performance, even the stability. It is an important control issue in the real industrial application. Fig. 3.21 shows the voltage loop bode plot with the variation of the line current. Although the controller is designed to have 60° phase margin at the 1000A operating point, the phase margin decreases to about 30° and bandwidth goes to 1Hz when the current changes to 100A.

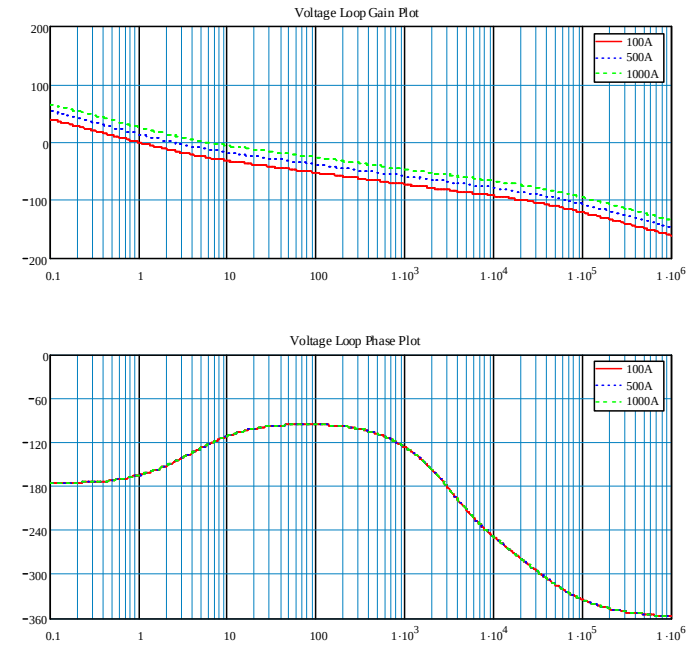


Fig. 3.21 Bad feedback design with variation of line current (insufficient phase margin)

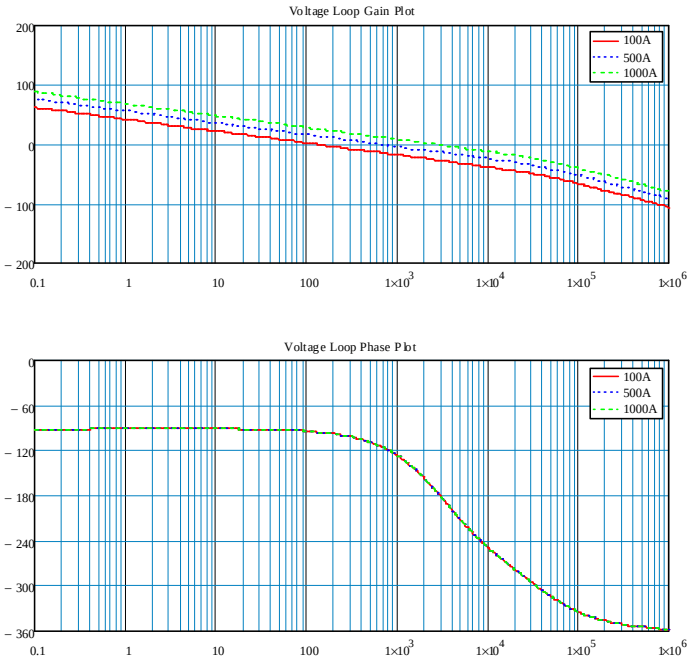


Fig. 3.22 B Bad feedback design with variation of line current (high crossover frequency)

Fig. 3.22 shows another bad design of voltage loop bode plot with the variation of the line current. The crossover frequency of controller at the 1000A operating point is 3kHz, which is too close to the switching frequency.

Fig. 3.23 shows the simulation results with the bad voltage loop design. The DC voltage could not be regulated well since the feedback controller could not provide enough phase margin.

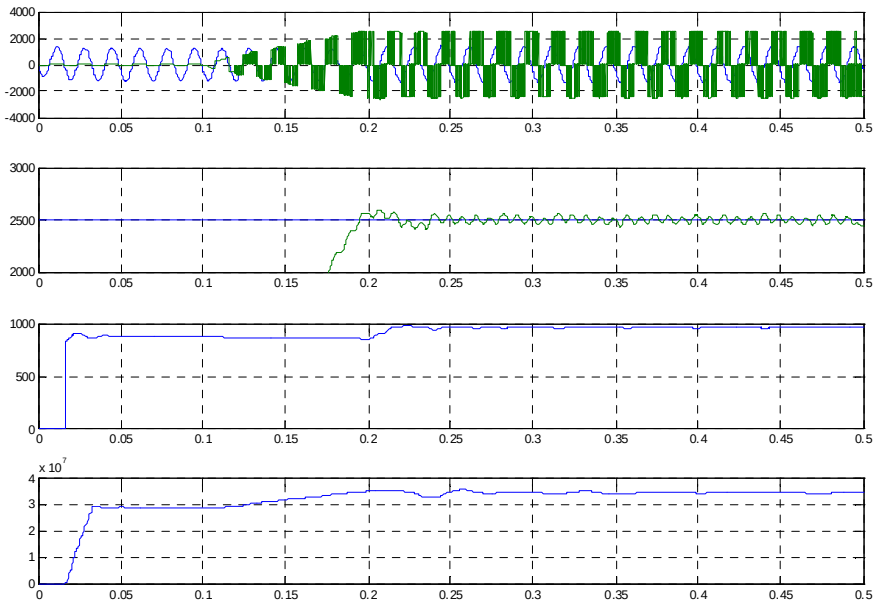


Fig. 3.23 Bad design simulations

To solve this issue, one possible solution is to design the feedback controller carefully based on the real operating situation (e.g. the full range line current). Fig. 3.24 displays one possible customized feedback controller design to provide the sufficient phase

margin and reasonable crossover frequency in all operation range of line current from 100A to 1000A.

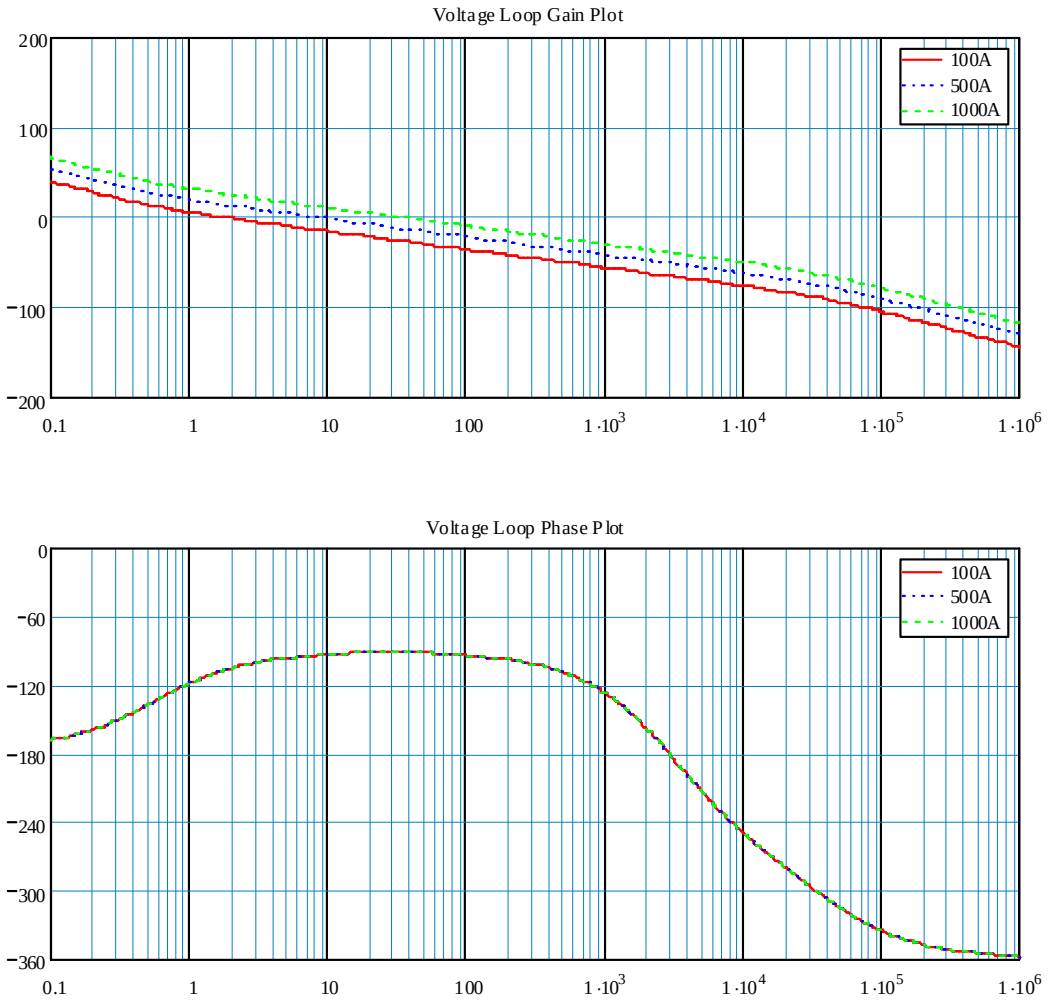


Fig. 3.24 Customized controller design

Another good solution to improve this issue is the gain scheduling controller design for the voltage loop. The gain scheduling compensation is introduced instead of conventional digital PI controller $H_{Vadp} = H_V / I_d$. The measured line current information is applied to the voltage loop to make the voltage loop independent with the line current. The

influence of current is compensated to achieve the better control speed and transient performance.

Fig. 3.25 shows the simulation results with the gain scheduling feedback controller design. The DC capacitor voltage and the line current are regulated very well.

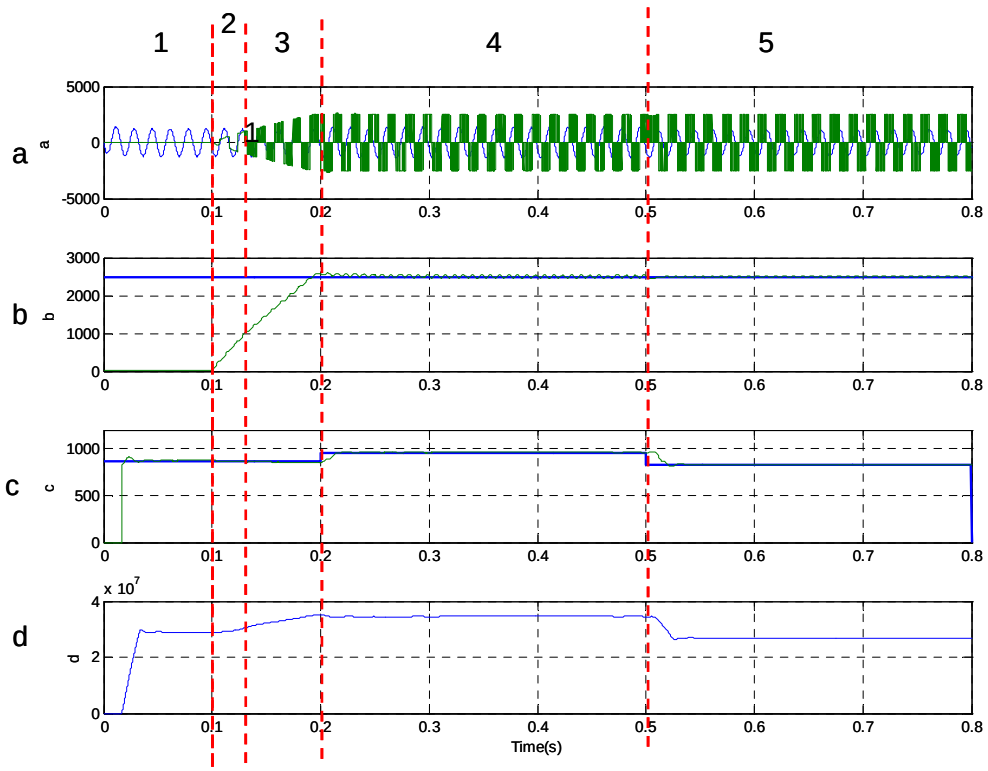


Fig. 3.25 Simulation results

Experimental Test Results

To verify the controller of DPFC, a single phase DPFC hardware prototype has been built in the laboratory as shown in Fig. 3.26. IGBT-based IPEM modules are used as H-bridges. The H-bridge is controlled by an Altera FLEX 10k30A FPGA-based local controller through a drive board and optical fibers. The central controller is connected to

six local controllers. The central controller includes a TMS320C6701 DSP board and an AED 106 FPGA daughter board. The controller system is fully compatible with any optical triggered device (e.g., ETO) –based H-bridge.

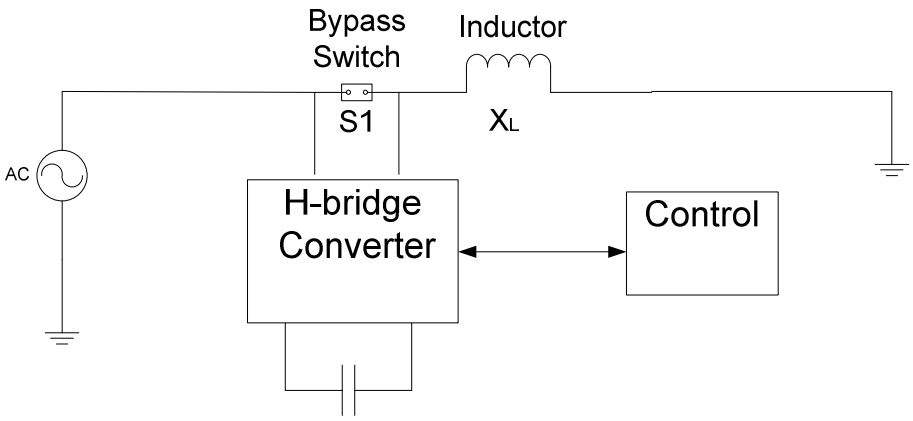


Fig. 3.26 Single pahse DPFC schematic circuit

The schematic of the experimental setup is shown as Fig. 3.27.

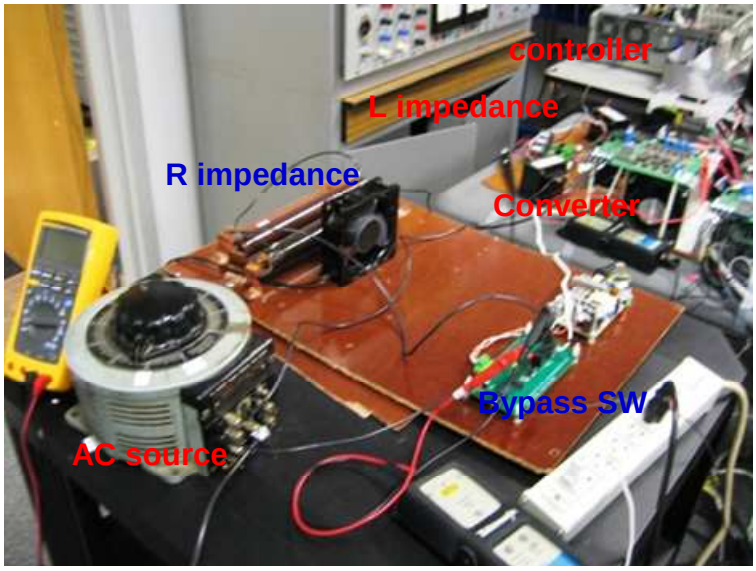


Fig. 3.27 Single pahse DPFC prototype prototype

The specification of the DPFC prototype is shown as Table 3-3

Table 3-3 Experimental Specifications

Line voltage of AC source RMS(V)	90
Resistive line impedance (ohm)	50
Inductive line impedance (mH)	7.5
Line current (A)	1.8
Switching frequency (Hz)	300
DC voltage of total converter (V)	12
DC capacitance(mF)	2.7
Internal converter loss estimation (W)	5

The current loop controller design is shown below.

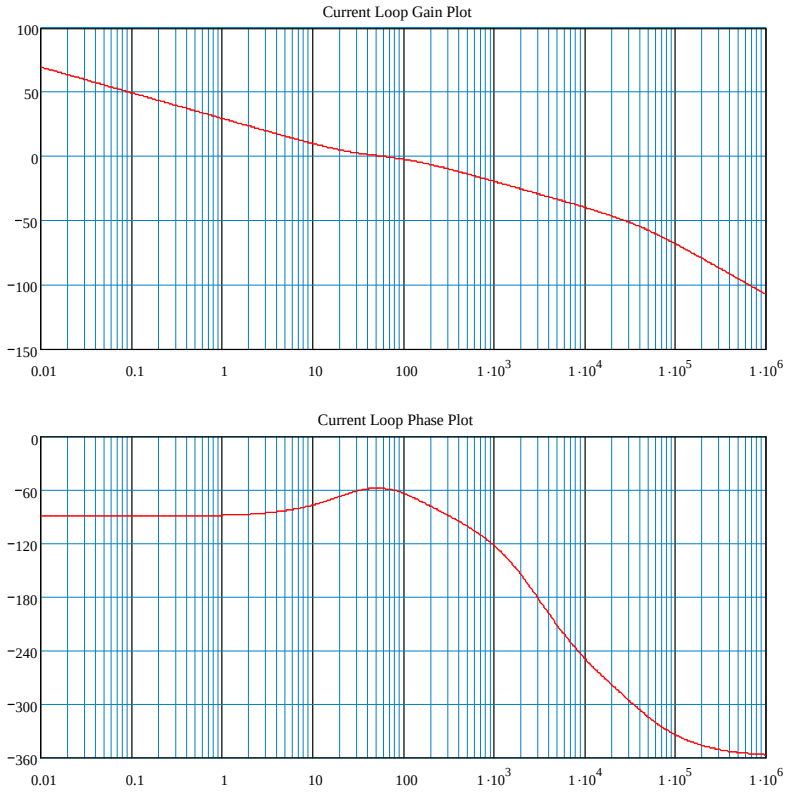


Fig. 3.28 Current loop bode plot

The cross over frequency is 50Hz which is the one sixth of the switching frequency 300Hz. The phase margin is 120^{o} .

The voltage loop controller design

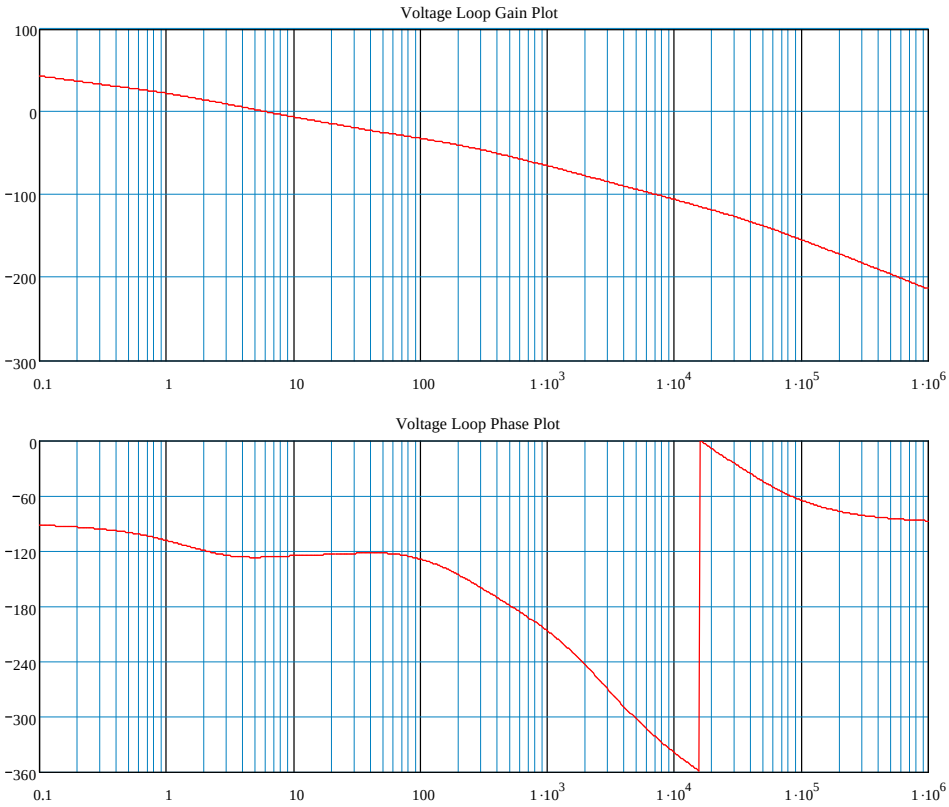


Fig. 3.29 Single phase DPFC prototype schematic

The crossover frequency is 5Hz which is 10 times slower than the current loop. The phase margin is 50^{o}

The test results are shown in the figures below.

Fig. 3.30 and Fig. 3.31 show the Phase Lock Loop (PLL) operation. We can find that the converter output voltages have 90° difference with the line current information to implement the reactive voltage injection.

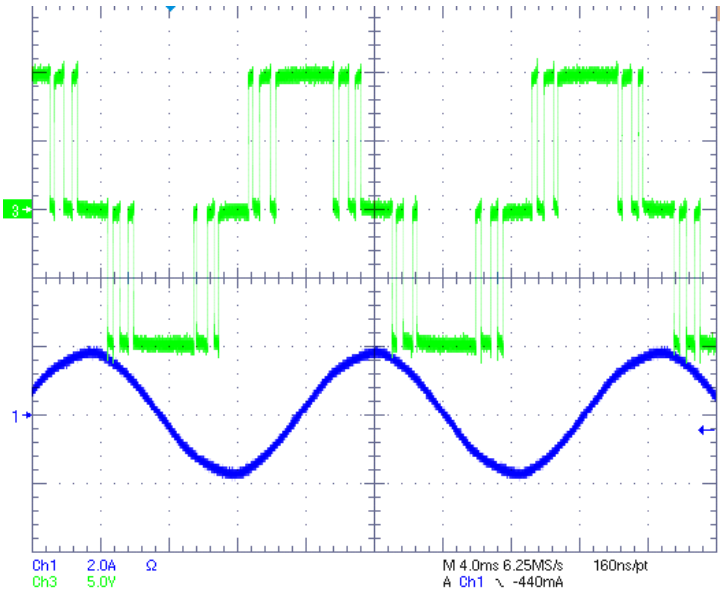


Fig. 3.30 Phase Lock Loop in capacitive mode

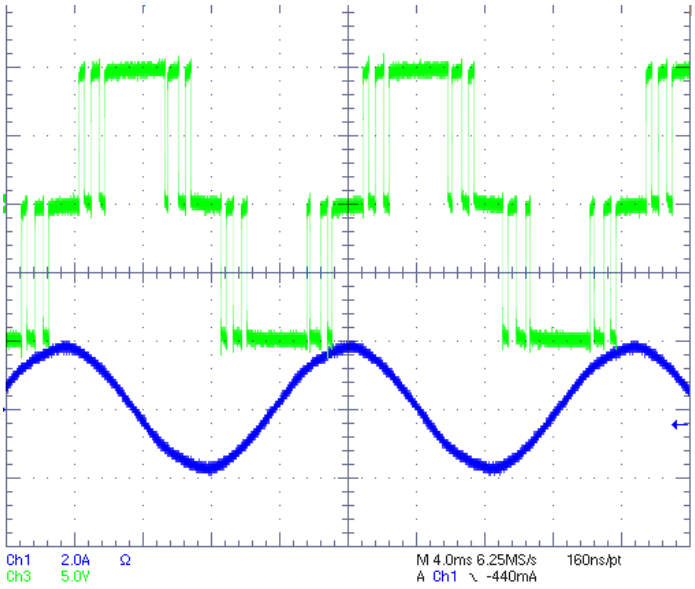


Fig. 3.31 Phase Lock Loop in inductive mode

Fig. 3.32 shows the operation sequence. It shows PWM charge mode, capacitive mode, inductive mode and discharge mode in sequence.

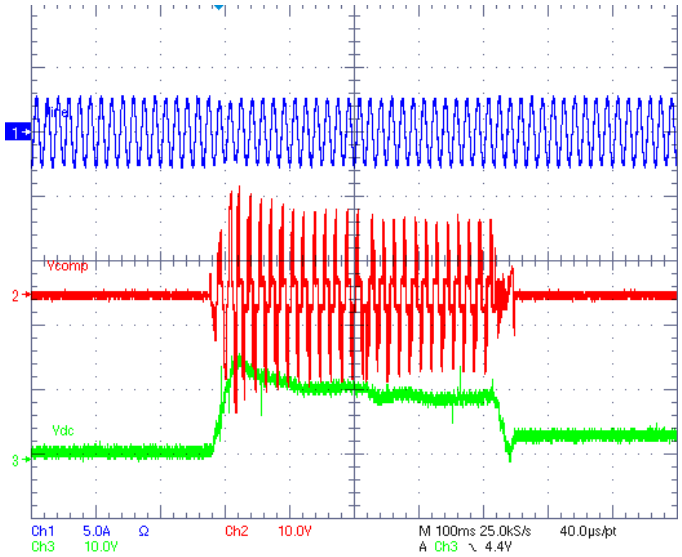


Fig. 3.32 Experimental results of DPFC (a) line current and compensating voltage. (b) converter output. (c) DC capacitor voltage.

Fig. 3.33 shows the charging operation.

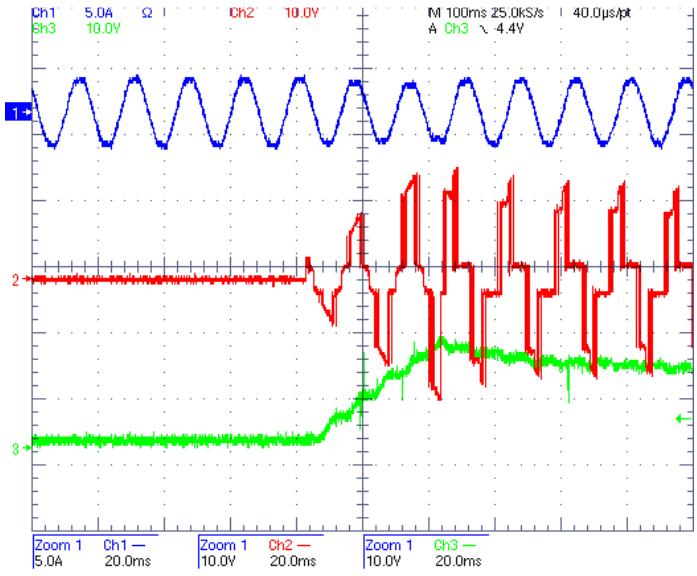


Fig. 3.33 Charging operation of DPFC (a) line current and compensating voltage. (b) converter output. (c) DC capacitor voltage

Fig. 3.34 shows the capacitive operation.

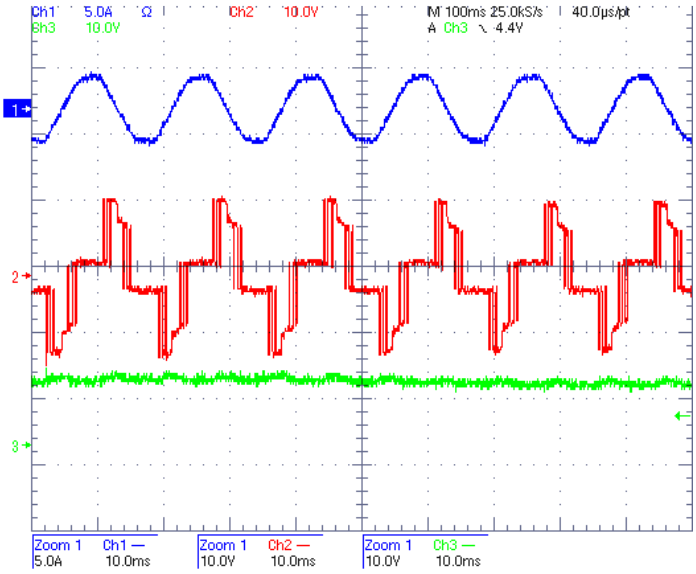


Fig. 3.34 Capacitive operation of DPFC (a) line current and compensating voltage. (b) converter output. (c) DC capacitor voltage.

Fig. 3.35 shows the inductive operation.

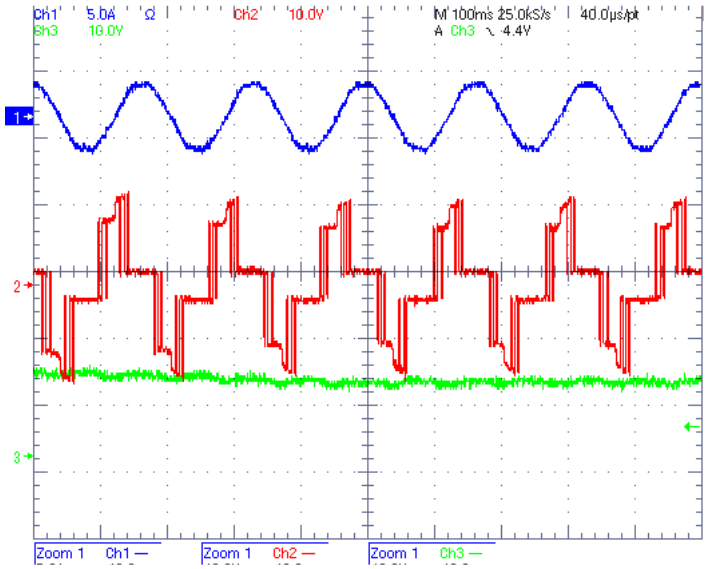


Fig. 3.35 Inductive operation of DPFC (a) line current and compensating voltage. (b) converter output. (c) DC capacitor voltage

Fig. 3.36 shows the discharging operation

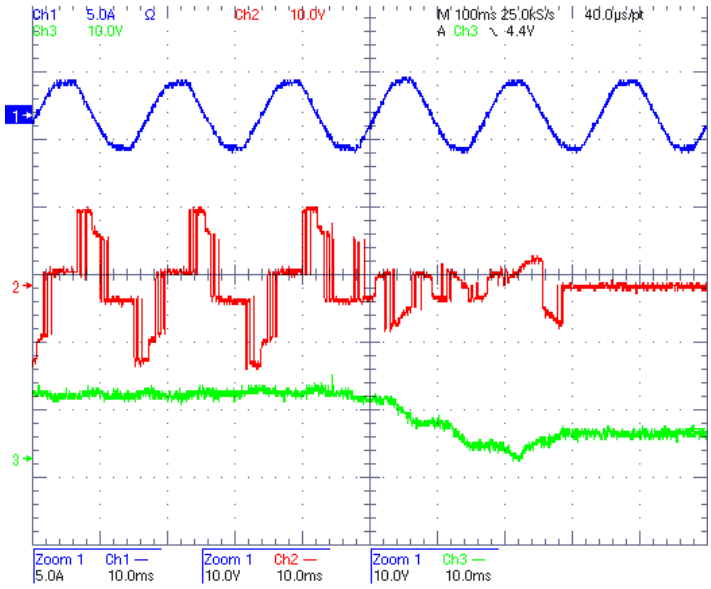


Fig. 3.36 Discharging operation of DPFC (a) line current and compensating voltage. (b) converter output. (c) DC capacitor voltage.

From the experimental results, two control targets could be verified: the PLL control works well and the DC capacitor voltage is well regulated by voltage loop.

The experimental results verify the feasibility of the controller for the single phase distributed power flow controller and the validation of the proposed operations.

3.5. Summary

This chapter presented the model development and controller design for the distributed power flow controller. The model of the DPFC was proposed. The key transfer functions were derived. The compensation parameters were well designed for the digital controller. The simulations and experimental results verify the feasibility of the model development and the control design.

Chapter 4. Distributed Power Flow Controller Applications

The converter-based series compensator is one of the most useful FACTS controllers for power flow control. The major application of the series compensation is to directly control of the transmitted power in a given transmission line. It can also provide transmission line voltage regulation by the control of the effective line impedance, particularly for the end-voltage of a radial line. The conventional applications for power flow control are for transmission lines [79]-[82]. The main applications within the broad area of adjustable or dynamic power flow control are as follows:

(1) Compensation of long transmission line

(2) Balance the power flow in lines to prevent the active power loop flow

(3) Improvement the stability

This chapter will propose the applications of DPFC in the conventional transmission system, the extended application in the distribution system especially in the demand side management (DSM) to control the power usage for the end user. Besides the traditional active power flow control, the advanced functions of DPFC are also presented and analyzed.

4.1. Transmission Line System Applications

The proposed DPFC could implement the functions of the conventional power flow controller:

(1) Active power flow control;

(2) Transient stability improvement;

(3) Power oscillation damping (power converter-based power flow control);

In order to verify the system effects of DPFC to a transmission line system, a 5-bus transmission system is introduced shown as Fig. 4.1. DPFC is designed to control the power flow through the transmission line. The simulation parameters are shown in Table 4-1.

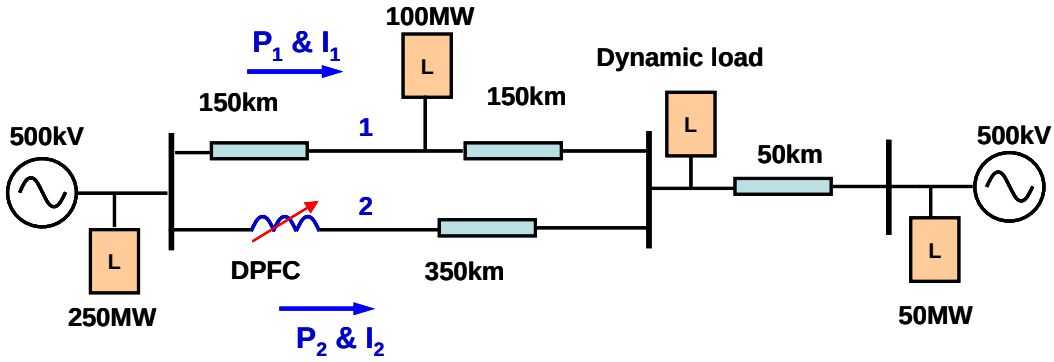


Fig. 4.1 DPFC system simulations

Table 4-1 Simulation Specifications

Phase to phase voltage of generator (kV)	500
Resistance per unit length (ohm/km)	0.02546
Inductance per unit length (H/km)	0.9337*10e-3
Capacitance per unit length (F/km)	1.274*10e-10
Compensation voltage	3%-7%
Simulation time (s)	10

The DPFC series compensation results are shown in Fig. 4.2. The more current and power flow goes through branch 1 because of the unbalanced line impedance and load condition. When the DPFC is put into service in branch 2, the line impedance characteristic is changed and the more power flow goes through branch 2. When the compensation voltage is 7%, the power flow of branch 1 and branch 2 are almost balanced. That helps to achieve high transmission line utilization. The simulation results verify the feasibility of DPFC for the power flow control in the transmission line system.

Since the power converter based series compensation can operate in either capacitive mode or inductive mode, the DPFC can operate in the inductive mode to increase the line impedance at the fault condition to damp the over current. That is one of the advantages of converter based series compensation solution comparing with the current capacitor based series compensation.

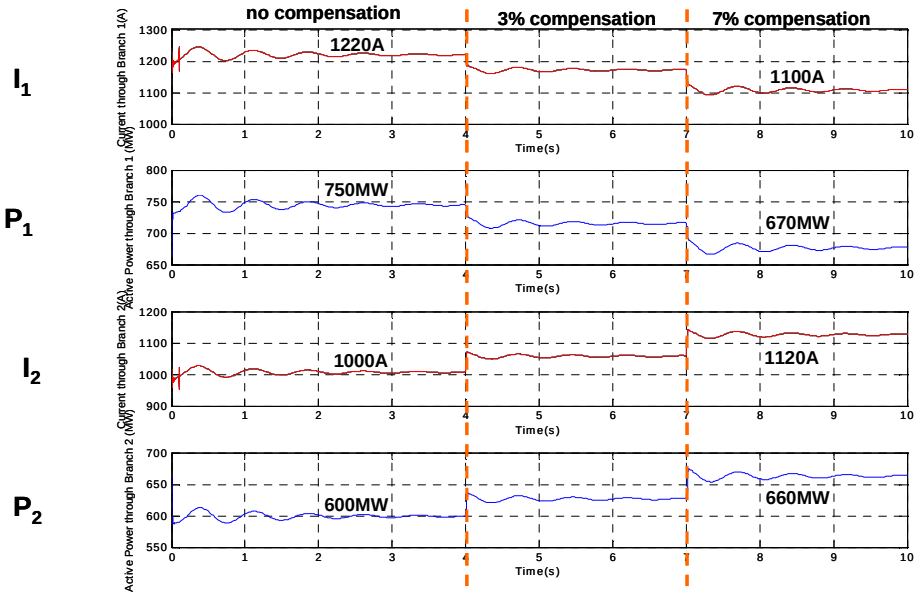


Fig. 4.2 Simulation results of DPFC influence to the transmission line

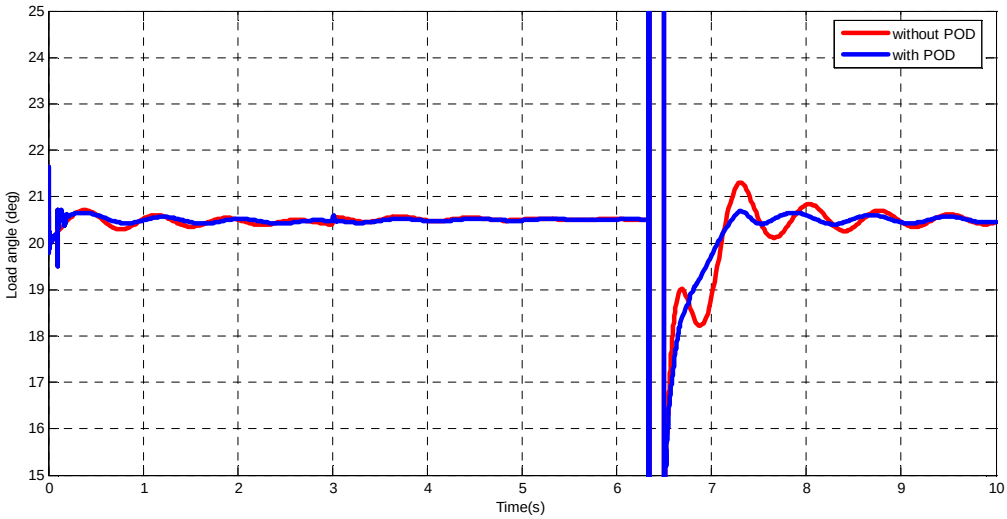


Fig. 4.3 Generator angle oscillation damping

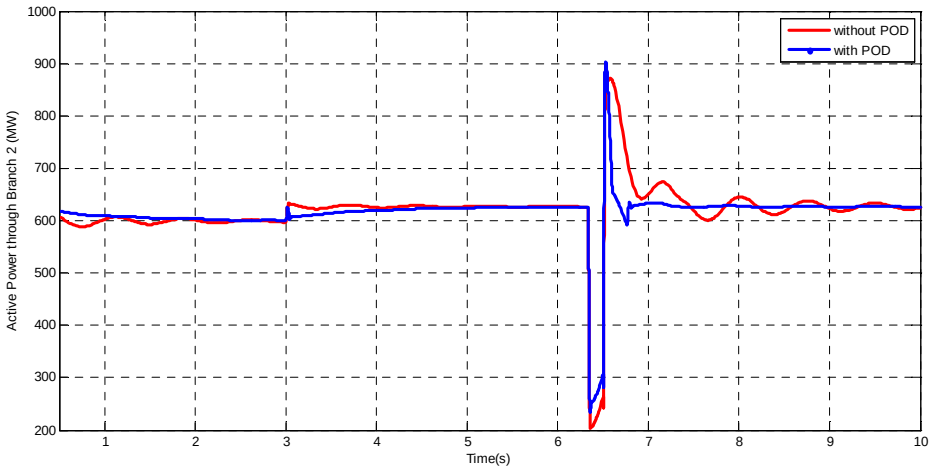


Fig. 4.4 Active power oscillation damping

Fig. 4.3 and Fig. 4.4 show the generator angle oscillation damping and active power oscillation damping functions of DPFC separately. With the power oscillation damping application of DPFC, the oscillation after the disturbance will be damped effectively.

The ETO-based DPFC also has some advanced functions which could benefit to the power system and the application aspects:

(4) Unbalanced current compensation;

(5) Possible series protection capability;

(6) Fault tolerant design.

Because the DPFC operation is based on per phase control, the phase current and active power flow in each phase is controlled independently. It provides the good opportunity to deal with the unbalanced current issue in the transmission line. Fig. 4.5 illustrates the function of DPFC to compensate the unbalanced three phase current. After the detection of the current sag in phase A, the DPFC module in phase is starting up and operating in the capacitive mode to balance the current. The current sag in phase A is compensated by the DPFC module in phase A.

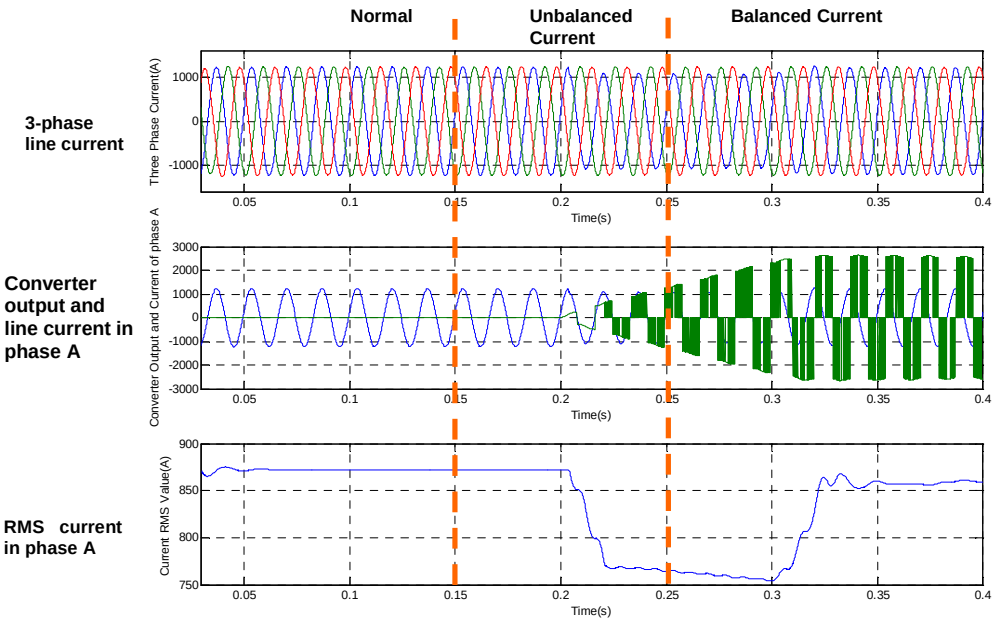


Fig. 4.5 DPFC unbalanced current compensation

The conventional SSSC has one mechanical bypass switch to sustain high fault current. While the mechanical switch has slow response time (20 – 60ms), it is not enough to protect the converter. The solid state switch could response fast (5-100us) but has the higher power loss. Fig. 4.6 shows the possible function of DPFC bypass scheme to achieve the fast switching to protect the converter and save the time for the mechanical switch to operate.

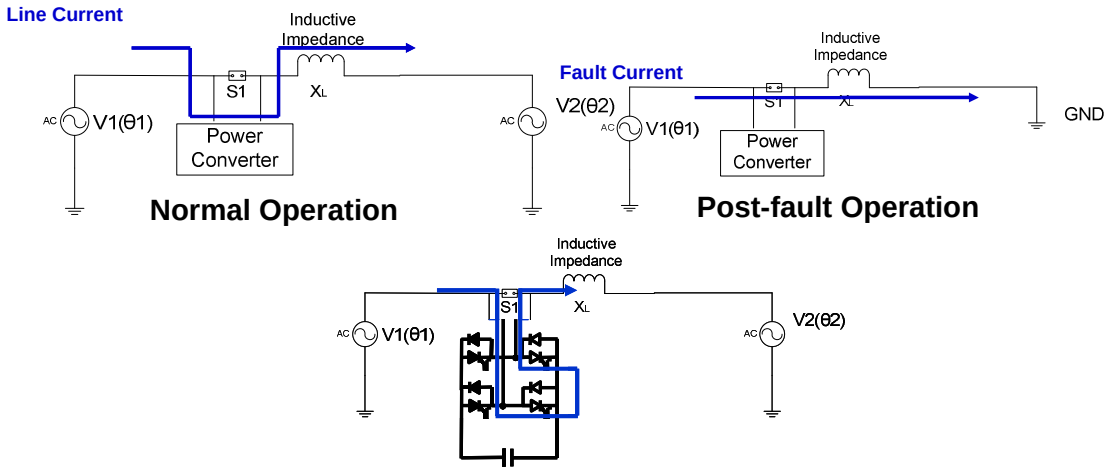


Fig. 4.6 The series protection of DPFC

Because of the fully modular design, the proposed distributed power flow controller can be installed to the transmission line flexibly based on the power transmission requirement. The flexible series connection provides the good opportunity to achieve redundancy for fault tolerant design. The redundant DPFC can be installed in the power line for each phase. At the normal operation, the redundant will be bypassed by the bypass switch. When one operating DPFC is failed, the failed DPFC module will be bypassed after the fault detection and the redundant DPFC will be put into the power line

and inject voltage to the power grid to control the active power through the power line as normal operation. The transmitted active power is maintained by applying the redundant DPFC module. The reliability of DPFC application is improved greatly by using this fault tolerant design. The more analysis and verification of fault tolerant design will be demonstrated in the next chapter.

4.2. Distribution System Applications

With the development of renewable energy and smart grid, more efforts have been put on the study of distribution system [85] – [86]. The proposed DPFC has the advantages to apply in the distribution system.

Since DPFC has the single phase controller, it has natural advantage to be applied in distribution system. Fig. 4.7 shows a 7.2kV distribution study system.

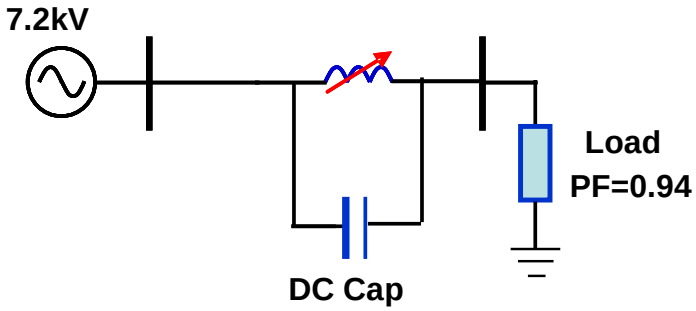


Fig. 4.7 DPFC application in 7.2kV distribution system

The simulation parameters are shown in Table 4-2.

Table 4-2 Simulation Specifications

Substation voltage (kV)	7.2
Active power of load (MW)	22
Power factor	0.94
DC voltage of DPFC converter (V)	500
DPFC injection voltage (V)	400

The phasor diagram of this operation could be demonstrated in Fig. 4.8.

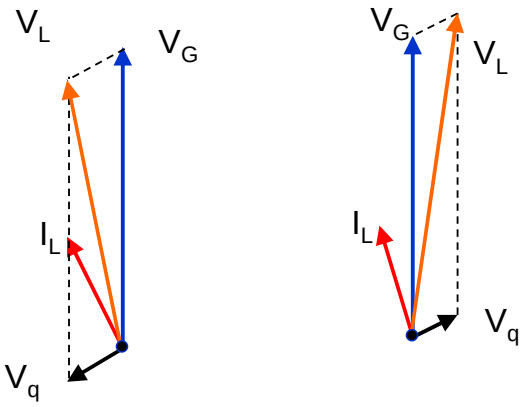


Fig. 4.8 Phasor diagram of DPFC application in distribution system

In the phasor diagram, V_G is the grid voltage, I_L is the line current, V_q is the DPFC compensating voltage. With the application of DPFC compensating voltage, the effective load voltage will be modified, thus the power consumption in the load side will be modified. We can also find that the power factor will be affected too.

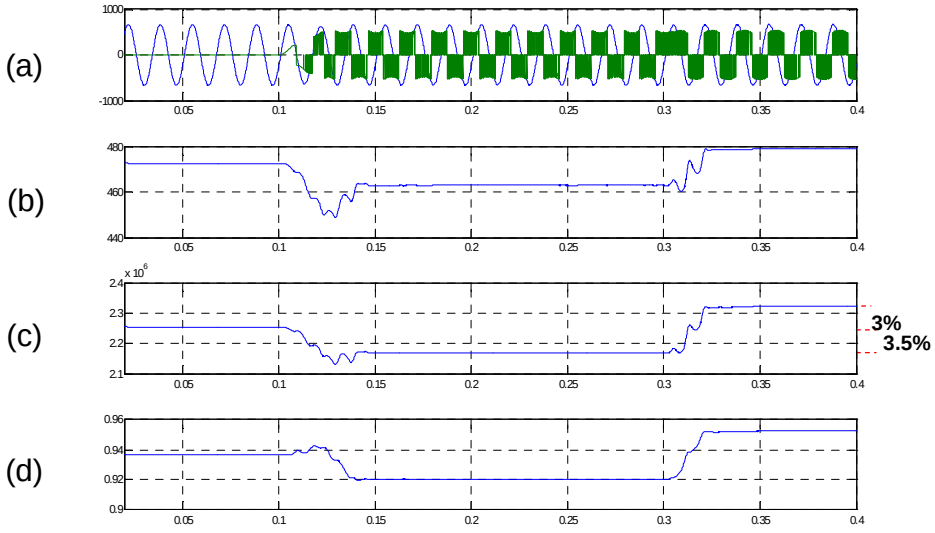


Fig. 4.9 Simulation results (a) current and converter output (b) load current RMS value (c) active power (d) power factor

The simulation results are shown as Fig. 4.9. DPFC is effective to control the power flow in the single phase distribution system.

Another study system for DPFC application in 240V distribution system with the renewable energy sources is shown as Fig. 4.10. The distributed generator is one renewable energy source connected to load 1 and load 2. One DPFC module is installed in line 2 to redistribute the active power flow between DG and two loads.

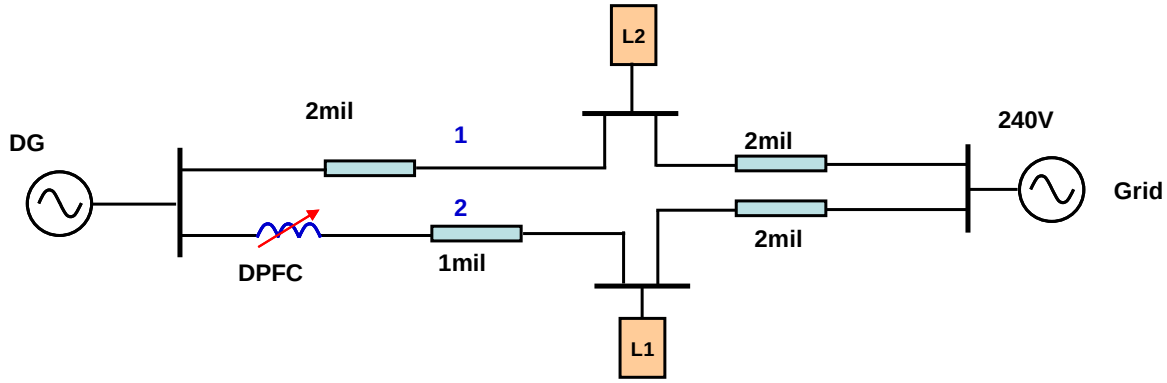


Fig. 4.10 DPFC application in distribution system

Table 4-3 Simulation Specifications

Generator Voltage RMS	240V
Line impedance of branch 1	1Ω + 0.01H
Line impedance of branch 2	0.5Ω + 0.005H
Load 1	20kW
Load 2	30kW
DG rating	25kW

The simulation results are shown as Fig. 4.11. The power flow could be redistributed by the application of DPFC.

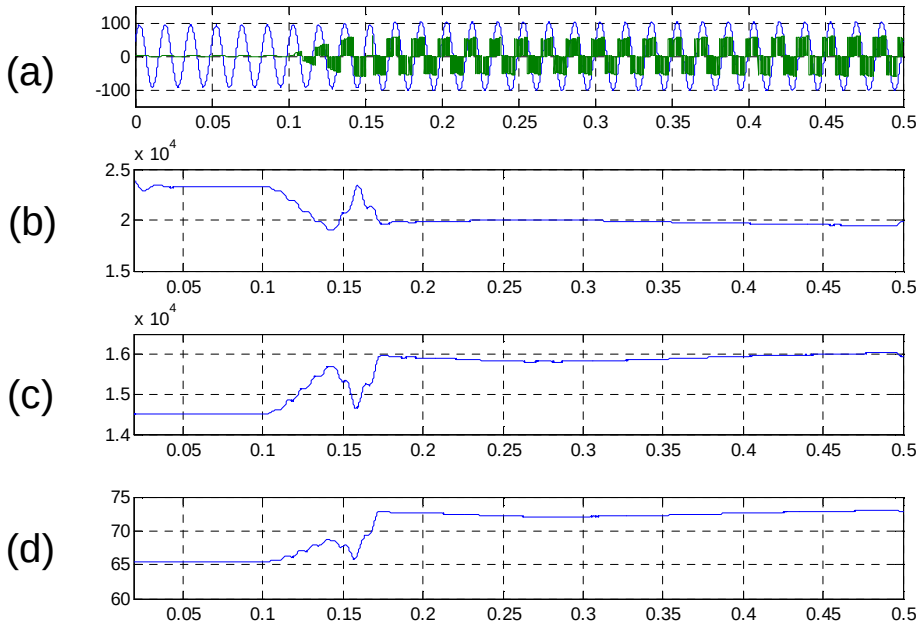


Fig. 4.11 Simlation results current and converter output (b) power flow on branch 1 (c) power flow on branch 2 (d) current on branch 2

Demand side management (DSM) encompasses “systematic utility and government activities designed to change the amount and/or timing of the customer’s use of electricity” for the collective benefit of the society, the utility and its customers. As such, it is an umbrella term that includes several different load shape objectives, including load management (LM), energy efficiency (EE) and electrification [83] – [84].

Peak clipping, valley filling and load shifting are classified as load management objectives. Energy efficiency involves a reduction in over all energy use and is sometimes referred to as energy conservation. Technically speaking, the two are different since the level of energy service (e.g., the level of lighting in a room) is preserved under

energy efficiency but declines under energy conservation. Electrification involves load building over all hours and is often associated with customer retention programs from the perspective of the utility. It can also involve the development of new markets and customers. Flexible load shape involves making the load shape responsive to reliability conditions.

DPFC has the ability to control the active power flow which is a good candidate for the demand side management.

The simulation system for DPFC in DSM application is shown as Fig. 4.12

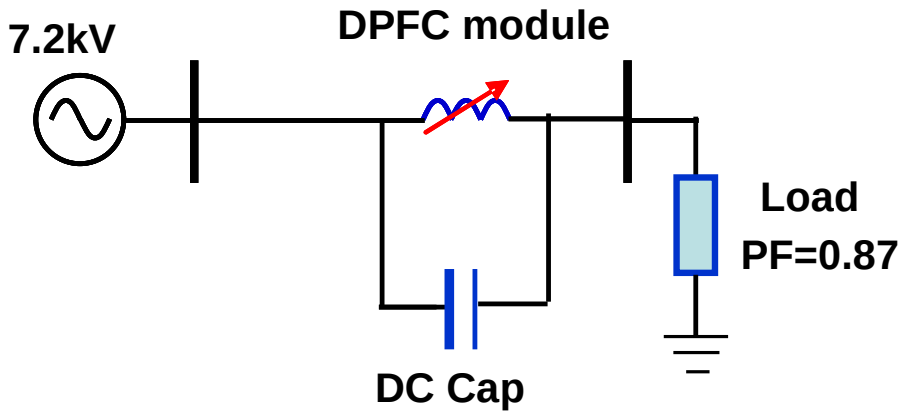


Fig. 4.12 Simulation system

The simulation parameters are listed in Table 4-4.

Table 4-4 Simulation Specifications

Substation voltage (kV)	7.2
Active power of load (MW)	1.95
Power factor	0.87
DC voltage of DPFC converter (V)	500
DPFC injection voltage (V)	400

The simulation results are shown as Fig. 4.13.

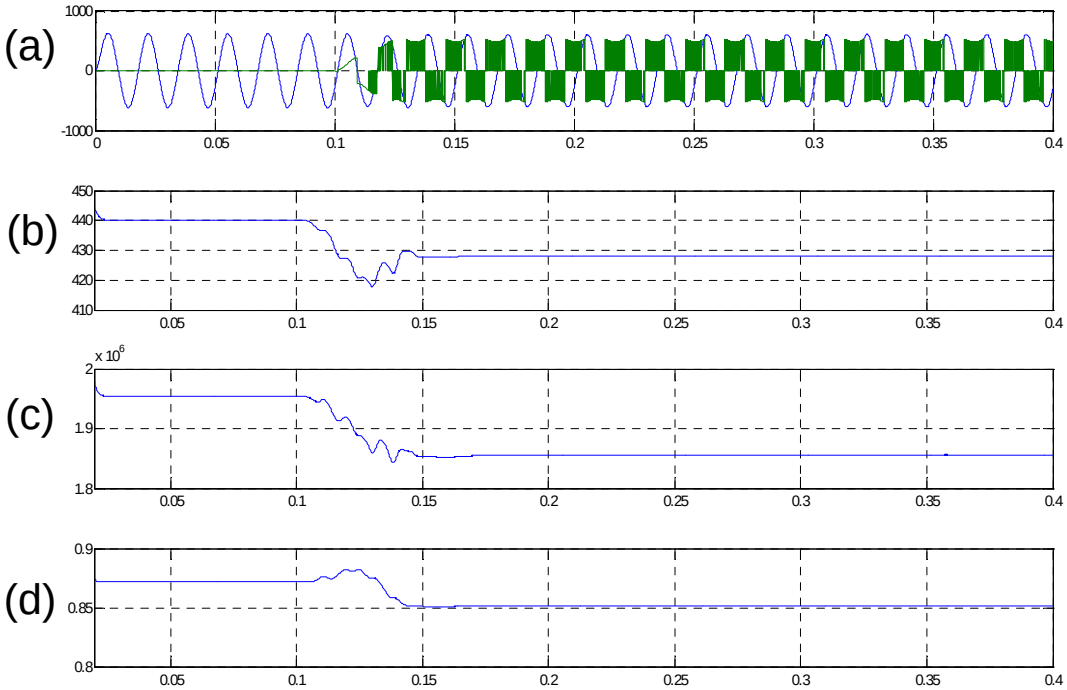


Fig. 4.13 Simulation results (a) current and converter output (b) load current RMS value (c) active power (d) power factor

The load side voltage magnitude could be effectively controlled by DPFC.

If DPFC DC link is interfaced with renewable energy sources, the transmitted active power could be controlled by DPFC and the active power from renewable energy sources could be transferred to load.

Fig. 4.14 shows one 110V study system of DPFC applied in DSM. The simulation parameters are shown as Table 4-5

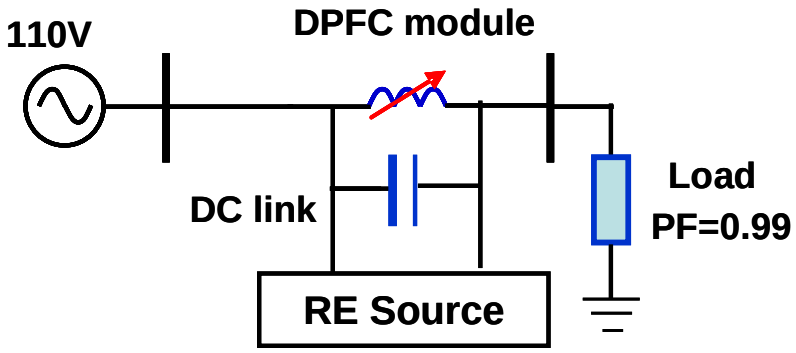


Fig. 4.14 DPFC with renewable energy srources simulation system

Table 4-5 Simulation Specifications

Grid Voltage	110V
Load	6KW
Power Factor	0.99
DPFC DC link	15V
DPFC injection voltage	10V
Renewable energy injection	10V

The phasor diagram of this operation could be demonstrated in Fig. 4.15.

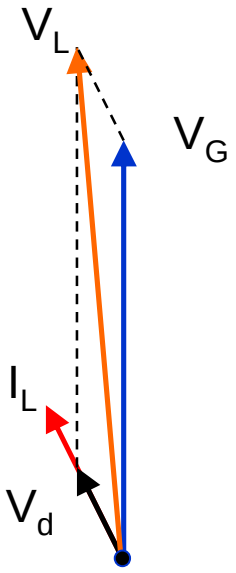


Fig. 4.15 Phasor diagram of series energy storage to supply active power

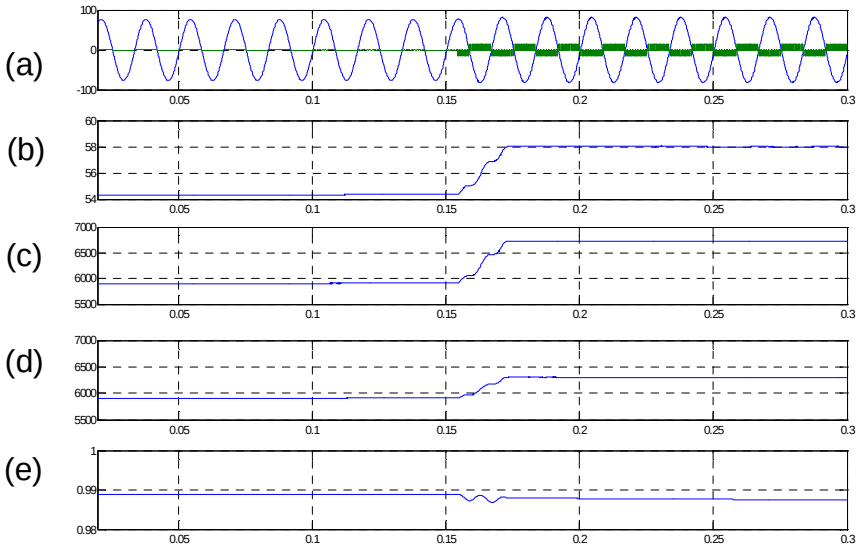


Fig. 4.16 Simulation results – renewable energy source only (a) load current and converter output (b) load current RMS value (c) active power from grid (d) load active power (e) power factor.

Fig. 4.16 shows the simulation results. The renewable energy is transmitted to the load with the interface of DPFC.

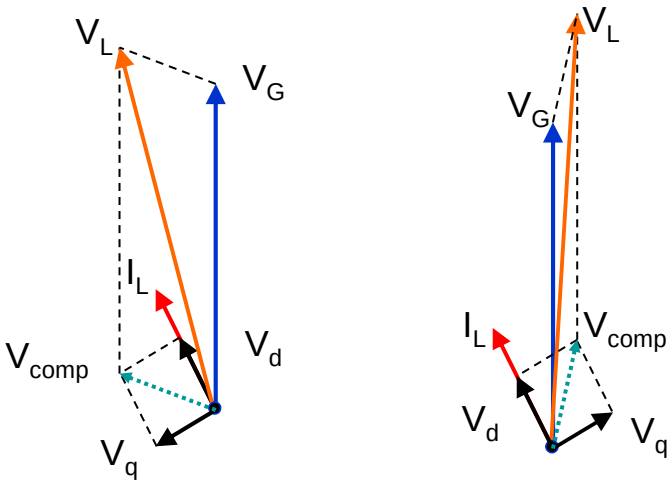


Fig. 4.17 Phasor diagram of DPFC interface with energy storage

Considering the DPFC is operating with the renewable energy source together, the output of DPFC could inject not only reactive voltage but also active voltage to the load. The phasor diagram is shown as Fig. 4.17. This application has more flexibility to control the load voltage and improve the load power factor.

The simulation results are shown as Fig. 4.18 and Fig. 4.19 with PF=0.99 and PF=0.94 respectively.

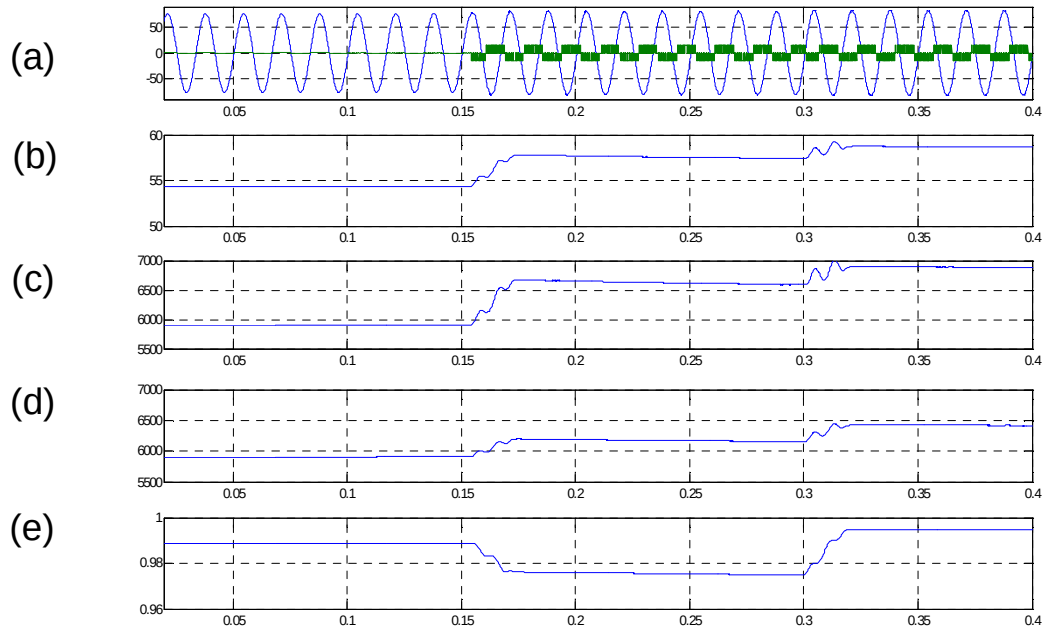


Fig. 4.18 Simulation results PF=0.99 (a) load current and converter output (b) load current RMS value (c) active power from grid (d) load active power (e) power factor.

DPFC could operate with renewable energy source to control the end user active power demand. Fig. 4.20 shows the possible applications of DPFC from high voltage transmission system to low voltage residential area. DPFC is a promising smart grid component candidate.

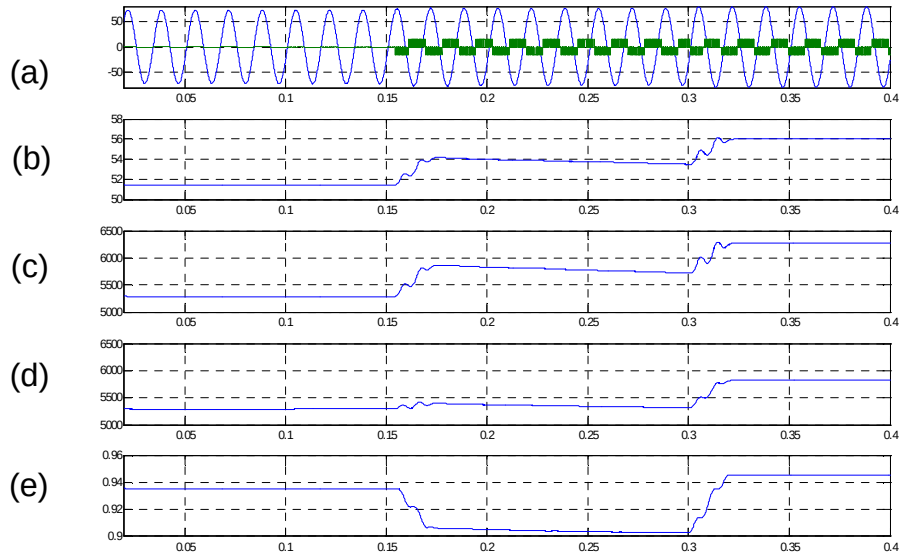


Fig. 4.19 Simulation results PF=0.94 (a) load current and converter output (b) load current RMS value (c) active power from grid (d) load active power (e) power factor.

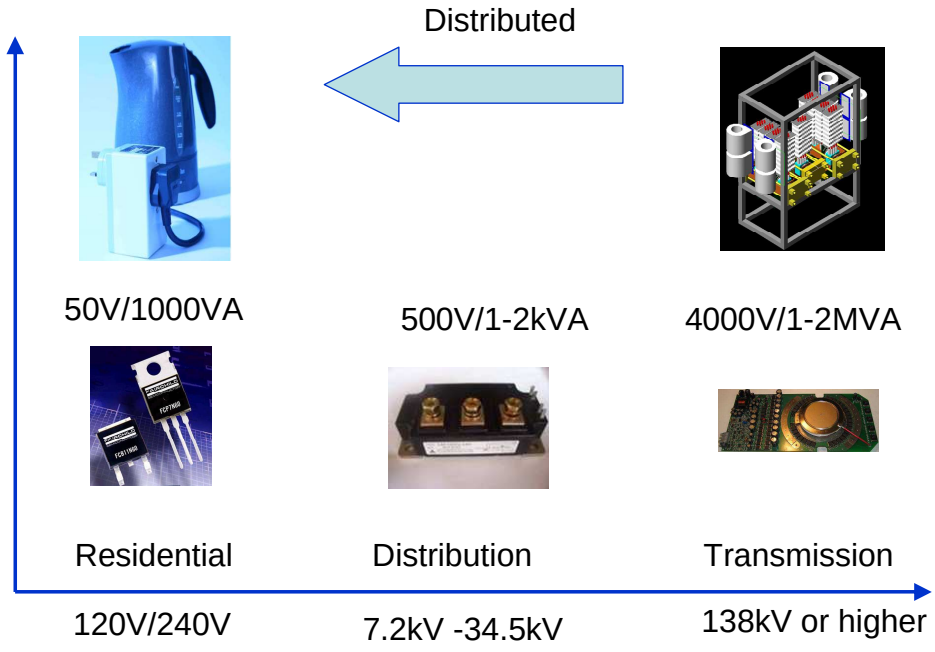


Fig. 4.20 DPFC prospective applications

4.3. Summary

This Chapter proposed the DPFC application in the conventional transmission system. Besides the traditional active power flow control and transient damping functions, DPFC is also capable to deal with the unbalanced current, fault current limit and inherent fault tolerant design. The new applications for distribution system and demand side management have been proposed and verified by the simulation results.

Chapter 5. Fault Tolerant Design

High cost, series protection requirement and low reliability still limit widespread converter-based power flow controller applications. Recent research has put more effort on the design and realization of low-cost and high-reliability high power converters. Fault tolerant design is an effective solution to achieve higher reliability and availability. The operation of the cascaded H-bridge multilevel inverter with faulty cells for drive systems was discussed in [50], [51]. Additional switches were used to bypass faulty cells. Despite the control strategies applied to minimize the load voltage distortion and balance the line-to-line output voltage, some phase output levels are lost. While applicable for increasing the reliability of a drive system, this solution is, however, unsuitable for the reactive power compensation applications such as the series compensation power flow control. A fault tolerant control strategy for cascaded multilevel converter based STATCOM (Static synchronous compensator) is proposed in [38]. It avoids the bypass switch by using the failure characteristic of a high power semiconductor device and maintains the converter output by applying a suitable fault tolerant control method. It sheds light on the fault tolerant design in reactive power compensation applications.

The distributed concept, as opposed to, the conventional lumped solution was recently introduced to design cost-effective FACTS devices. References [40], [41] proposed a Distributed Static Series Compensator (DSSC). Low rated (1-20kW) inverter and single turn transformer (STT) were applied to form a DSSC module that can be clamped to the transmission conductor to control the active power. Simple and low cost, the DSSC is

advantageous over the lumped solution for active power flow control. Although the high transformer turns ratio could increase the current level, the compensating voltage capability and power inverter rating are limited at the same time. As a result, a large number of DSSC modules are required to control the certain active power flow through the power transmission line. A new power electronics configuration called Magnetic Energy Recovery Switch (MERS) was introduced to control the active power flow as a variable series capacitor by using low switching frequency, simple converter topology and simple control, which lead to low cost and low losses [18], [19]. While its application is limited by injecting the capacitive series voltage only and lacks the flexibility in power flow control applications such as the damping function after the transience or disturbance in the power transmission line.

The “Smart Grid” was promoted by the US government by using decentralized systems with digital technologies, renewable and distributed equipment etc. enabling electricity delivery to save energy, reduce cost and increase reliability [63], [54]. This provides a large number of research opportunities to develop low-cost, high-reliability technologies for the distributed and fault tolerant study of power utilities. This chapter proposes two low cost fault tolerant designs for a transformerless power flow controller using series compensation based on the newly developed ETO Light converter. The first is to achieve the N+1 redundancy in a cascaded multilevel converter based power flow control system. Redundant HBBB is designed to deal with switching device failures and to increase reliability. Compared with aforementioned fault tolerant solutions, this strategy saves bypass and isolated switches and keeps the same converter output by applying the proper

control scheme. The other solution is using the Distributed Power Flow Controller (DPFC) module to achieve series redundant design proposed in [55]. The DPFC module using a single ETO Light converter with the rating of 1 -2 MVA is an applicable and practical solution to lower the cost and increase the reliability of power flow control applications. The availability and reliability is improved by implementing fault tolerant designs and cost is reduced by using a modular ETO Light converter. The transformerless connection is possible because of the high voltage/current capability and the control power self-generation function of ETO Light converter. The medium rating (1-2MVA) is very suitable for distributed applications in the transmission system. The operation principles and control strategies of these two fault tolerant designs are presented. In this chapter, the feedback controller designs for the fault tolerant operations are introduced. The feasibility of the proposed fault tolerant designs for the series compensation is verified by simulation and experimental results.

5.1. Fault Tolerant Design

A safe critical system is the system whose failure may cause injury or death, which should have the ability (fault-tolerance) to respond to an unexpected hardware or software failure.

Fault-tolerance may be called upon to improve system reliability, maintainability and survivability. Reliability deals with the period of time over which that ability is retained. A control system that allows normal completion of tasks after component failure improves reliability. Maintainability concerns the need for repair and the ease with which repair can be made, with no premium placed on performance. Fault tolerance could

increase time between maintenance actions and allow the use of simpler repair procedures. Survivability relates to the likelihood of conducting an operation safely, whether or not the task is completed. Degraded performance following failure might be permitted, as long as the system can be brought to an acceptable state of rest.

Reliability is essential in high power applications, which are the main application areas of multilevel converters. It is important to maintain normal operation under fault conditions because failed operation of high power applications could cause tremendous losses to the power grid due to high voltage and current. As higher level multilevel converters are required in high output power rating applications, a large number of power switching devices will be used. Each of these devices is a potential failure point, which will dramatically reduce the reliability of the system. It is therefore a key issue to design a fault-tolerant multilevel-converter system.

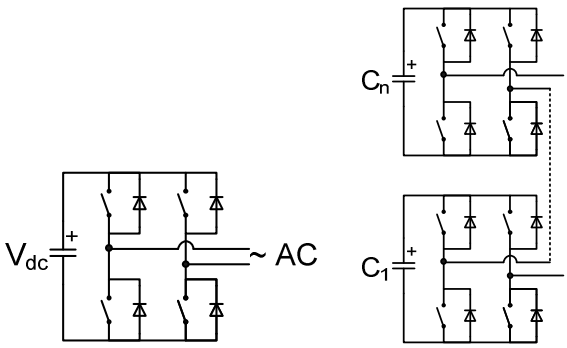
For a fault-tolerant system, the basic ability is to continue operation in the event of a power failure. One of the most useful tools in the fault-tolerant design system is redundancy. Many fault tolerant systems should mirror all the operations, that is, every operation should be performed on two or more duplicate systems, such that if one fails, the other can take over. For modular systems with redundancy, the structure of the system is usually a mixture of series and parallel modules. In traditional two level converters with high output voltages, the redundancy is achieved by series connection of more power devices. In this way, redundancy can be achieved when one device fails shorted. Converter operation is not affected and no additional control is needed to maintain normal operation since the failed device acts like a short circuit. By this method,

reliability will increase greatly, but the number of devices will double. Normally because of cost, size and complexity concerns, duplicate systems or modules are not practical. So the topology configuration redundancy is considered as a practical solution.

5.2. Multilevel Solution

5.2.1. Method

Recently the cascaded H-bridge multilevel converter (CHMC) has become an increasingly attractive converter topology for FACTS applications due to its simple structure and modularity. The CHMC requires the least number of components among all multilevel converter topologies. The modularized design of an H-bridge building block (HBBB) makes it much easier to implement the converter with a large number of levels and achieve higher power capability and flexibility [23]-[25]. Fig. 5.1 (a) illustrates a typical HBBB used in the CHMC application. Fig. 5.1 (b) shows the circuit diagram of the CHMC with separate DC sources. Each HBBB can generate 3-level voltage output and the CHMC with N HBBBs can generate 2N+1-level voltage output.



(a) (b)

Fig. 5.1 Modular converter (a) one HBBB (b) cascaded H-bridge multilevel converter

Reliability is essential for high power applications and thus is a major concern in CHMC applications where a large number of power switching devices are used. It is important to restore the normal operation under fault conditions because the failed operation of FACTS controller could cause tremendous losses for the power grid. As higher level multilevel converters are required in the higher power rating application, a large number of power switching devices are used. Each of these devices is a potential failure point, which will dramatically reduce the reliability of the system. It is therefore a key issue to design a fault tolerant system to enhance the system reliability.

Relevant research of the fault tolerant design for multilevel converters mainly focuses on motor drive systems [56]-[57]. [58] introduces the fault tolerant solutions of the capacitor-clamped and the asymmetric multilevel converters, which in fact sacrifice the output level. The references [59], [60] propose one multilevel converter topology with redundant switches and one adopted capacitor-clamped topology for the fault tolerant design to maintain the output voltage level whenever switch fault occurs. Too many additional switches are applied, which limits the practical value in industry. [61], [62] discuss the operations of cascaded H-bridge multilevel inverter with the faulty cells for the motor drive system. Additional switches are used to bypass faulty cells. Despite the control strategies applied to minimize the load voltage distortion and balance the line-to-line output voltage, some phase output levels are lost. Applicable for increasing the reliability of a motor drive system, this solution is however, unsuitable for power utility applications such as power flow control and STATCOM.

Based on the control strategy presented in [68], this paper proposes a fault tolerant control strategy to achieve the N+1 redundancy in a CHMC based STATCOM system. Redundant HBBB is designed and applied to deal with switching device failure and improve reliability and availability. Compared with aforementioned solutions, this strategy saves the bypass and isolated switches by using the failure characteristics of high power devices while keeping the same output converter voltage. The output quality – total harmonic distortion (THD) is also improved because of the increasing output level by using redundant HBBB. The operating principle and controller design method are introduced and illustrated in this paper. The fault tolerant control strategy is designed and verified by simulations. The hardware demonstration is built to verify the proposed control strategy and the experimental results prove the feasibility of the fault-tolerant design and control strategy.

In traditional 2-level converters with high output voltages, the redundancy is achieved by series connection of more power devices. In this way, redundancy can be achieved when one device fails short. Converter operation is not affected and no additional control is needed to maintain normal operations since the failed device acts like a short circuit. We call this “device redundancy”. With this method, the reliability will increase greatly, but the number of devices will double. For example, for a three-phase 5-level CHMC converter, normal operation requires $6 \times 4 = 24$ power device sets (considering the main switch and anti-parallel diode as one device set). With duplicate redundancy, we would need 48 devices. Normally because of cost, size and complexity concerns, the duplicate

systems or modules are not easy to apply. So topology configuration redundancy is considered a practical solution.

The modularized HBBB is very suitable for the fault tolerant design because all HBBBs are modular and identical in the CHMC application. One additional HBBB can be added to CHMC as a backup to maintain normal operation even in case of one HBBB failure. We call this redundancy "HBBB redundancy". The HBBB redundancy is achieved if one uses 2N+1 level CHMC to implement the converter operation instead of 2N-1 level CHMC. In this way, each phase has one additional HBBB. Redundancy is realized if we can bypass the HBBB which contains the failed device so that the cascaded failure is prevented and normal operation is maintained.

There are two major advantages of using this redundancy approach: one is the savings in the number of the power devices compared with the device redundancy. For example, a 5-level CHMC plus one redundant HBBB will be implemented as a 7-level CHMC. The total number of power devices will be $9 \times 4 = 36$ instead of 48 for the duplicated system.

Table 5-1 Reliability Comparison of CHMC with and without Redundancy

Conditions of HBBBs per phase	**Reliability per phase**	**Numbers of devices per phase**	**Size&cost**
2 HBBBs (5-level) without redundancy	85.1%	8	Small
3 HBBBs (7-level) with one HBBB redundancy	99.3%	12	Medium
2 HBBBs (5-level) with the duplicate power device redundancy	99.7%	16	Big

Another major advantage is that during normal operation, the output voltage waveform will be 7-level instead of 5-level. This will improve the output voltage waveform quality during normal operation. Meanwhile the power devices are over designed and more devices are applied in a fault tolerant system. The balance of reliability enhancement and cost augmentation should be considered.

To further analyze the reliability of a CHMC application, it is supposed that a CHMC application is designed to have N HBBBs per phase. If the reliability of one power device set during a specific time interval is R and only one switch fault can be allowed for purposes of simplicity, the reliability of one-phase CHMC with N HBBB is R^{4N}, the number of power device sets per phase is $4N$. The reliability of one-phase CHMC with N+1 HBBB (one HBBB redundancy) is $[R^4 + 4(1-R)R^3]^{(N+1)}$, the number of power device sets per phase is $4(N+1)$.The reliability of one-phase CHMC with the device redundancy is $(2R-R^2)^{4N}$, the number of power device sets per phase is $8N$.

For example, if the reliability of each power device set is $R = 98\%$, the comparison of a 5-level CHMC without redundancy, a 7-level CHMC with one HBBB redundancy, and a 5-level CHMC with the device redundancy is shown in Table 5-1. Although this simple comparison does not take into account the effect of the reliability introduced by the extra components to detect the failure event, it assures reliability improvement by using different redundant strategies.

In the above comparison, the reliability is improved greatly with the application of redundancy. At the same time, the numbers of devices used for converters also increase.

Both the device redundancy and the HBBB redundancy can benefit the reliability of CHMC greatly. But compared with device redundancy, the method of HBBB redundancy will reduce the number of devices, therefore, the cost and size, especially for high-level CHMC applications. The HBBB redundancy can achieve the applicable balance between the reliability improvement and cost augmentation. The HBBB redundancy with an acceptable additional size and cost is therefore an effective and applicable way to improve the reliability of CHMC application.

When one power semiconductor device fails, the key to achieving the above proposed HBBB redundancy is to bypass and protect the failed HBBB. This requires that the failed HBBB DC side is open and the AC side is short.

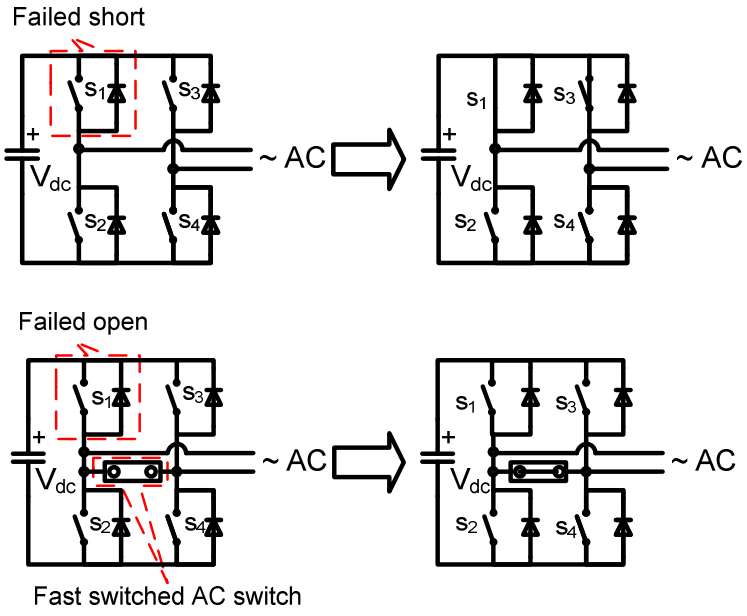


Fig. 5.2 HBBB bypass schemes after the device failures

Currently, the state-of-the-art high power semiconductor devices such as integrated gate commutated thyristors (IGCT) and high voltage insulated gate bipolar transistors

(IGBT) have the potential to substitute for conventional gate turn-off thyristors (GTO) in high power industrial applications due to their lower cost, higher power density and higher performance because of the snubberless operation at higher switching frequencies (up to 1kHz) [63], [64]. Fast switching capability, easy-to-use, and the reliable press pack, the IGCT and the press pack IGBTs are the desired semiconductor device candidates for utility active and reactive power compensation applications. Both IGCTs and press pack IGBTs will act as a short circuit after the destruction because of their press pack structures.

For wire bond package semiconductor devices such as module package IGBT, the failure state after destruction is open. In this case, one fast switched AC switch is required to bypass the failed HBBB. For press pack semiconductor devices such as IGCT and press pack IGBT, the failure mode is short. It is possible to use the failed state characteristic(s) of the power device to bypass the failed HBBB with no additional bypass power switch. Since press pack semiconductor devices are used widely in high power application(s), analysis of the short failure mode of the device will be the focus of this chapter.

Table 5-2 Detection of Failed Devices in HBBB

S1	S2	Voltage on S1	Current through S1	Failure detection	Action
ON	OFF	H	L	S1 failed open	All switches OFF and bypass switch ON
OFF	OFF	L	L	S1 anti-parallel Diode conduct	None
OFF	OFF	L	H	S1 failed short	S2, S4 OFF; S3 ON
OFF	ON	L	H	S1 failed short	S2, S4 OFF; S3 ON

Fig. 5.2 shows the two bypass schemes for a failed HBBB. For failed open semiconductor device application, all the switches are turned OFF after failure detection and the bypass AC switch is turned ON simultaneously in order to isolate the failed HBBB. For failed short semiconductor device application, if one top/bottom switch fails short, the complementary switch in the same leg is turned OFF instantaneously with the fault detection to protect the DC capacitor. Then turn ON another top/bottom switch in the other leg and turn OFF the other complementary switch to form a zero state. For instance, if the power switch S1 fails short, when the fault is detected, the two top switches receive ON signals and two bottom switches are given OFF signals.

Sensing a device failure and bypassing the failed HBBB promptly and accurately are very important to the prevention of failure propagation. Fault detection and diagnostic methods were presented in recent research [66]-[67]. In the strategy described in Fig. 5.2, a failure event of a semiconductor device can be unambiguously detected by the combination logic of the switching command, the complementary switching command, the voltage sensing signal across the device and the current sensing signal through the device. The power semiconductor switch under development will have built-in voltage and current sensing functions. Commercial IGBT driver modules have integrated fault detection and feedback functions. These capabilities could be used to achieve this goal. Table 5-2 illustrates the device failure detection in one HBBB. Since the four switches in one HBBB are identical, the failure detection and bypassing strategies are similar, only one switch failure detection and bypass strategy is discussed.

For example, when the switching command is off, but the sensed voltage across the device is low and sensed current through the device is high, then the short failure of this power semiconductor device is detected and a fault signal is generated to direct the controller to a) bypass the HBBB using this strategy shown in Fig. 5.2, and b) change the main CHMC control to fault tolerant CHMC operation. Because one HBBB is bypassed, the 2N+1-level converter is degraded to 2N-1-level converter. A major challenge, therefore, is to be certain that the main control system can gracefully migrate from a 2N+1-system to a 2N-1- system while the fault tolerant system is still performing its normal operation i.e., generating reactive power to support the voltage for a STATCOM system.

Consider a three-phase 7-level output STATCOM for example. When one HBBB in one phase is bypassed, the output level of this phase is lost. To maintain equivalent normal output, the converter degrades from 7-level operation to 5-level operation, then the individual DC bus voltage needs to be charged to a higher value in order to keep the total DC bus voltage same as the original value in all three phases. It is possible to apply this process in FACTS applications for active and reactive power compensation because the converter can obtain active power from the power grid to charge the DC link capacitors without requiring additional active power sources.

Because the loss of one HBBB will reduce the converter output voltage by 1/N at the moment of failure, a large current will be generated due to voltage difference and inductor impedance without proper control. This resulting large transient current is an important issue to consider in this fault tolerant design. Therefore, the voltage control

loop and the current control loop should be carefully designed. The current limit control and the DC voltage reference slope are introduced to smooth the transient current. The modulation index of the converter should be designed properly for both normal operation and fault tolerant operation to provide enough voltage allowing for the elimination of high transient current.

5.2.2. Case Study – Multilevel Converter-based Power Flow Control

In order to verify the feasibility and functions of the proposed fault tolerant power flow controller design, a two-machine one-bus transmission line system is introduced to the simulation setup shown in Fig. 5.3. The transmission line impedance parameters are typical for a 138kV 30-mile transmission line.

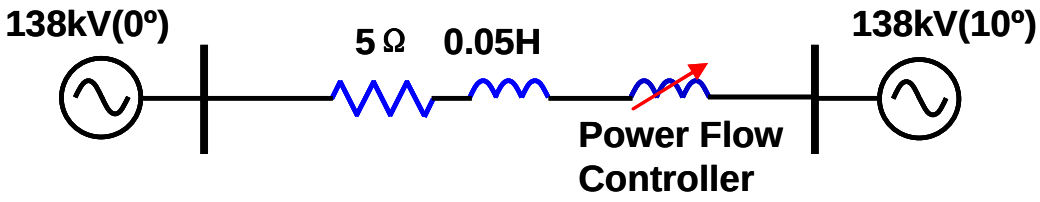


Fig. 5.3 Power flow control study case

The simulation test is implemented in Matlab. The simulation parameters are shown in Table 5-3.

The DPFC fault tolerant control development diagram is shown in Fig. 5.4. The digital controllers gather the information from the circuits, transmission lines and external commands, and then send the switching signals to the DPFC circuit according to the DPFC model development and the feedback controller design. The average model and small signal model of DPFC in DQ frame can be derived. Based on the small signal

transfer functions, the closed-loop controller can be designed. The controller is suitable not only for steady state operation but also for fault tolerant transition.

Table 5-3 Simulation Specifications

Phase voltage of generator 1 (kV)	$138/\sqrt{3}$
Voltage phase of generator 1	0
Phase voltage of generator 2 (kV)	$138/\sqrt{3}$
Voltage phase of generator 2	10
Line impedance of 30-mile line(ohm)	5+j*18.85
Line current (A)	710
Switching frequency (Hz)	1020
DC voltage of total converter (V)	2500
Injection voltage	3.5%
Digital Delay of controller (us)	100
Equivalent loss of each DPFC module (kW)	1.5
Low pass filter resistor (ohm)	4
Low pass filter capacitor (uF)	1
Simulation time (seconds)	1.2

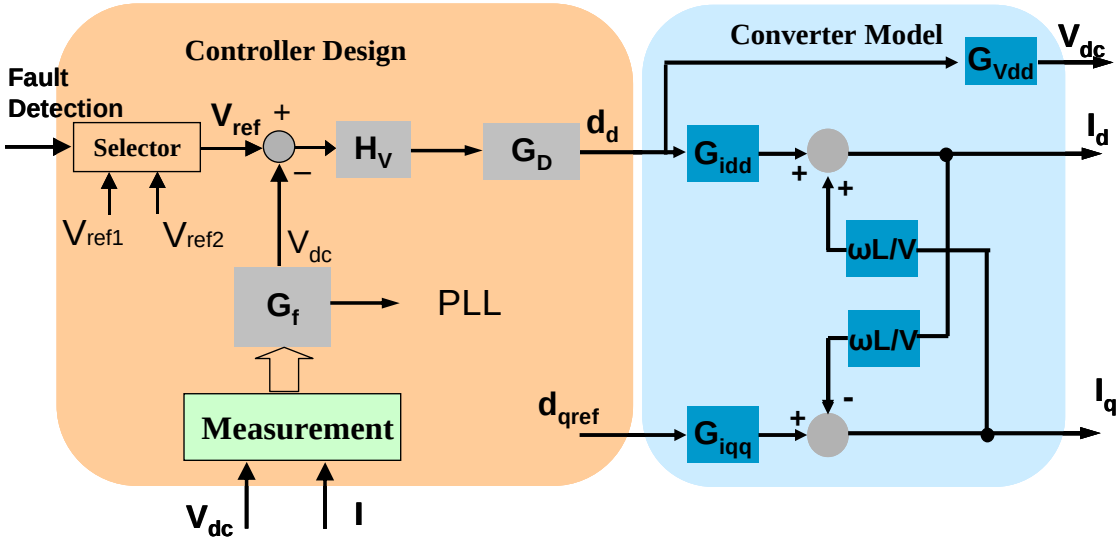


Fig. 5.4 Fault tolerant control of power flow controller

Fig. 5.5 shows the model development and control diagram of the power flow controller. The power flow controller measures the line current and the DC capacitor voltage of the converter. The line current provides the PLL (phase loop lock) information for the DQ0 frame calculation. The DC capacitor voltage is regulated by the d-axis control loop in order to implement energy transmission between the power grid and the converter. The series compensating voltage is given by the q-axis duty cycle to change the active power flow through the power transmission line. For the other control mode such current control, the q-axis duty cycle can be given by the external current loop or active power loop.

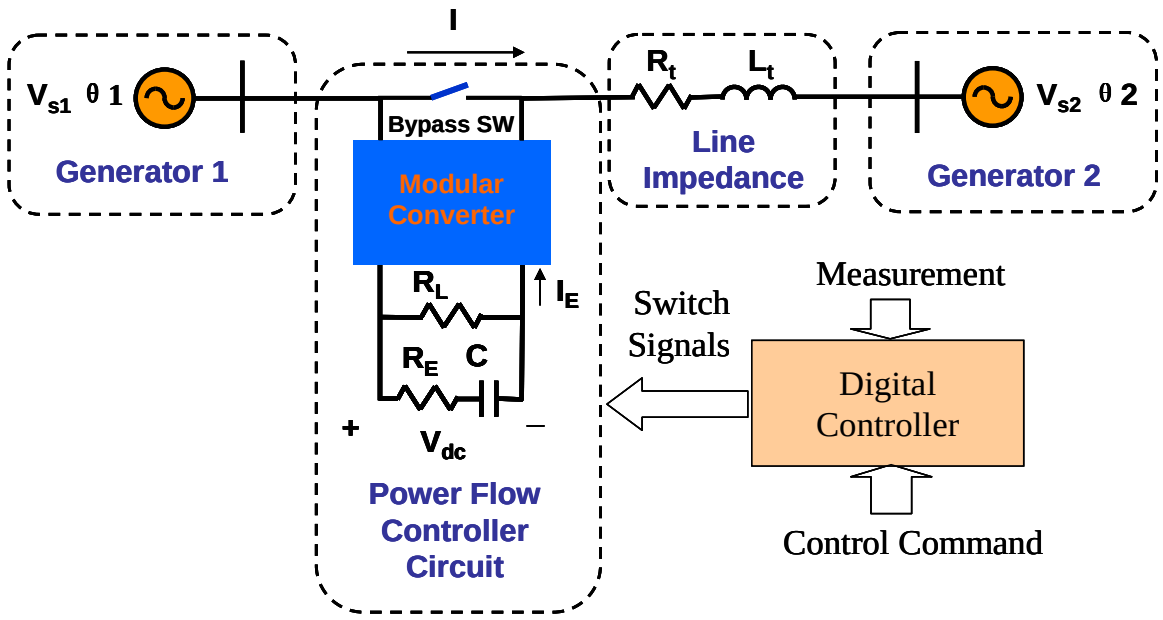


Fig. 5.5 DPFC control diagram

Based on the model development of the power flow controller using HBBB converter, small signal transfer functions can be derived.

The duty cycle-to-current transfer functions are:

$$G_{idd}(s) = \frac{\tilde{i}_d}{\tilde{d}_d + \tilde{i}_q \omega L / E} = \frac{V_{dc} / L_t}{s + R_t / L_t} \qquad (5.1)$$

The d-current to capacitor voltage transfer function is:

$$G_{vdd} = \frac{\tilde{V}_{dc}}{\tilde{d}_d} = -\frac{I_d / C}{s + 1 / R_L C} \qquad (5.2)$$

The feedback control loop compensation is applied to achieve stability and good transient performance. In this paper, the digital PI controller is used as the feedback control compensation. To simplify the feedback controller design, the coupling of DQ current influence will be ignored because the coefficient is relatively small.

The DC bus voltage loop gain is:

$$T_V = G_{vdd} H_V \qquad (5.3)$$

The digital delay of controller is modelled to emulate the real digital control system:

$$G_D = \frac{1 - T_D / 2}{1 + T_D / 2} \qquad (5.4)$$

The low pass filter of measurement to cancel the sensing noise is also considered:

$$G_f = \frac{1}{1 + sR_f C_f} \qquad (5.5)$$

where

V_{dc} – Total DC capacitor voltage

L_t – Transmission line inductance

R_t - Transmission line resistance

C – DC capacitance

P_L – Equivalent loss of each DPFC module

$R_L = V_{dc}^{\ 2} / P_L$ –Converter equivalent loss resistance

T_D – Digital controller delay

From the derived small signal transfer functions, the duty cycle to DC capacitor voltage gain is related to the line current. Because the designed feedback controller is suitable for only one operating point, when the line current changes, instability and poor transient performance may be introduced to the closed-loop controller, especially when the current is small. When the line current is too small in some cases, the control loop was unable to provide enough phase margin or the control loop bandwidth is too close to the switching frequency.

When the multilevel solution is applied to the power flow controller to achieve fault tolerant design, the simulation results are shown as Fig. 5.6. The CMC is operating in 7-level output at the normal operation mode. The CMC changes to 5-level operation mode after detection of the failure of one HBBB.

Fig. 5.6 (a) shows the transmission line current and injecting voltage (converter output) waveforms. The injecting voltage has 90º phase difference with the line current to operate as a reactive component and thereafter alter the line reactive impedance in order to

change the active power flow. Fig. 5.6 (b) and Fig. 5.6 (c) show the RMS line current and transmitted active power through the transmission line. The simulation results illustrate fault tolerant operations after one device or one HBBB failure is detected.

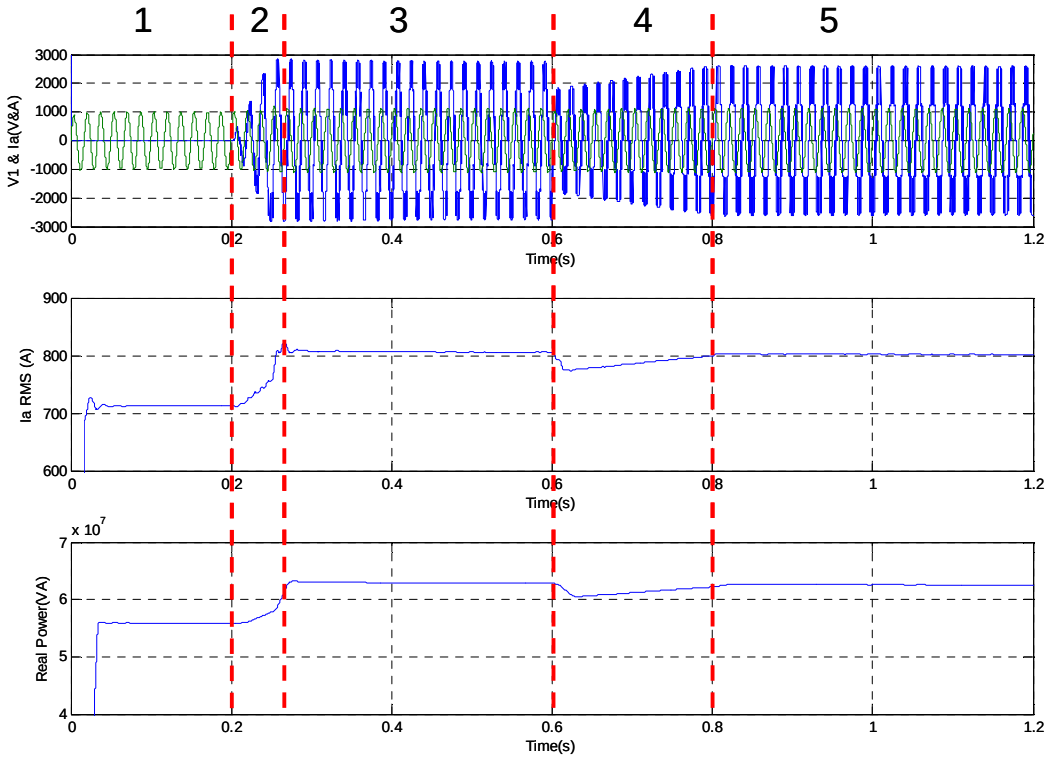


Fig. 5.6 Simulation results of CMC based power flow controller (a) line current and power flow controller converter output voltage. (b) line current RMS value. (c) transmitted active power.

The fault tolerant operations of CMC based power flow controller entail five steps:

(1) The power transmission system is operating without any series power flow control. The line current is 720A and the transmitted active power is 56MW.

(2) Initial charge of the DC capacitor voltage of power flow controller. The voltage regulation loop is working when the power flow controller is put into service. The total DC capacitor voltage is charged to 2500V, that is, the voltage of each DC capacitor voltage is approximately 833V.

(3) The power flow controller generates 7-level output voltage injection compensation. The line current and active power transmission are increased to 800A and 62.5MW since the equivalent reactive impedance of the transmission line is reduced.

(4) Fault tolerant charging mode. When a faulty event is detected, the faulty HBBB is bypassed, the converter operation mode changes from 7-level output operation to 5-level output operation, the total DC capacitor voltage is charged to 2500V as before, that is, each DC capacitor voltage is increased from 833V to 1250V. In this operation mode, the real power is flowing from the power grid to the power flow controller converter to charge the DC capacitor. The line current and transmitted active power will decrease slightly and then recover to the normal compensating operation.

(5) 5-level voltage injection compensation. After the fault tolerant transient operation, the equivalent total output of the power flow controller is restored to the pre-fault situation, the line current and active power transmission is restored to the pre-fault condition.

Fig. 5.7 shows the zoom-in waveforms of injecting voltage and line current in the transition between 7-level to 5-level output with the DC capacitor charge. The transition initiates the fault event detection. A 200ms DC capacitor voltage charge slope is applied to the controller to recover the output of the power flow control. After the transition, the power flow controller operates at a charged-up 5-level output and keeps the 90^{o} phase difference of voltage and current to compensate for line impedance and maintain the transmitted active power through the power line.

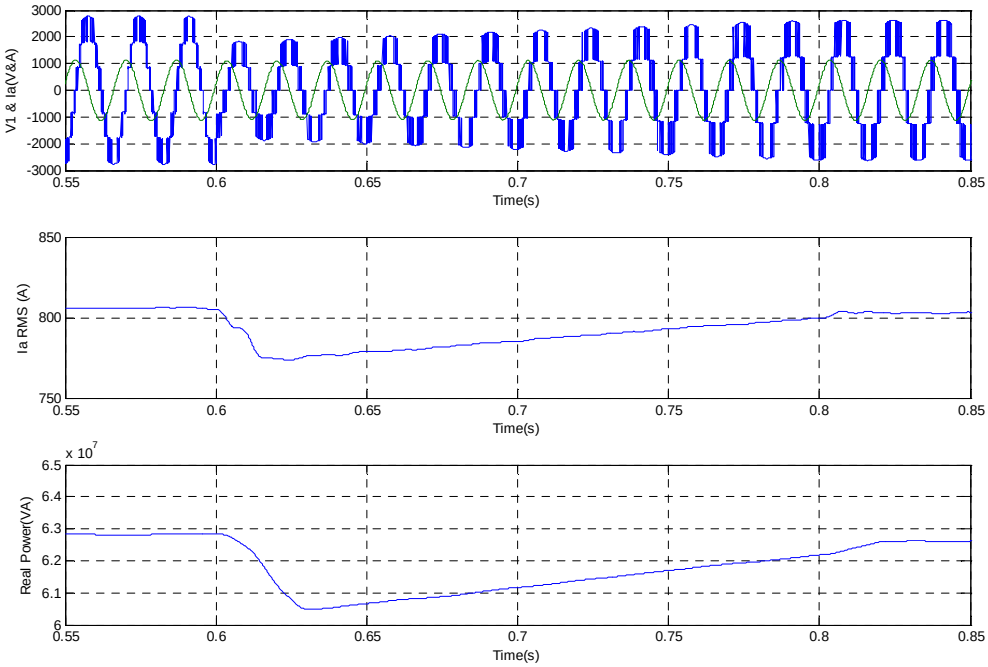


Fig. 5.7 Transient converter voltage output and line current (a) line current and power flow controller converter output voltage. (b) line current RMS value. (c) transmitted active power

5.2.3. Case Study – Multilevel based STATCOM

In order to study the validity of the proposed HBBB redundancy based fault tolerant control strategy, a 5-level plus one HBBB redundancy CHMC based STATCOM system is considered. In other words, it is a 7-level CHMC based STATCOM system.

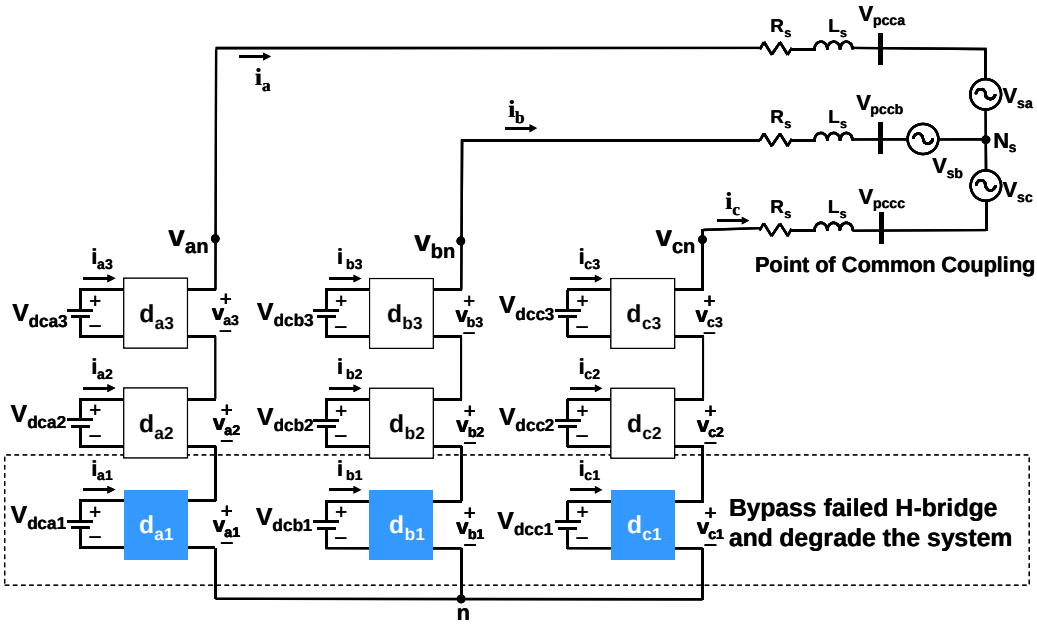


Fig. 5.8 Reconfiguration of three-phase 7-level to 5-level CHMC based STATCOM

Fig. 5.8 illustrates the system configuration of the 7-level CHMC-based STATCOM. This system is designed to have one HBBB redundancy. The 7-level CHMC can degrade to the 5-level CHMC when one device fails short. The specification of the studied STATCOM system is illustrated in Table 5-4. If the transformer is used at the point of common coupling (PCC), the transformer will contribute the reactor inductance and resistance. All control parameters are suitable for the 7-level system and the 5-level system. The DC bus voltage and DC capacitor design is based on the commercial

semiconductor device used in the high power application market. Based on the selection of power devices, the 5-level configuration can achieve the design rating. One HBBB is added to achieve redundant fault tolerant design and better harmonic performance with the 7-level output.

Fig. 5.8 also illustrates the control scheme to balance 3-phase output and maintain the output of the converter in the event of a device failure. Because of the ability of redundancy, the system can perform the STATCOM function continuously after a fault event until the next planned service outage.

Pertaining to the modelling of the HBBB based converter, the average model and small signal model of CHMC-based STATCOM in DQ0 frame can be obtained by the modelling process described in [69]. A closed-loop decoupled control can be designed based on the derived small signal models. Fig. 5.9 shows the converter model and the controller design strategy of a CHMC-based STATCOM system.

Table 5-4 Specification of Studied Statcom Simulation System

7-level CHMC based STATCOM	
Configuration	Balanced 3-phase 3-wire
Individual DC bus voltage in 7 level	1450 V
Individual DC bus voltage in 5 level	2175 V
Total DC bus voltage	4350 V
Rated reactive current	1000A
DC capacitor capacitance	16.2mF
Equivalent loss of each HBBB	1.5kW
Individual Switching frequency	1020 Hz
Coupling reactor inductance	0.69mH
Coupling reactor ESR	26mΩ
Point of the Common Coupling (PCC) line to line voltage	4160V
Power Rating of STATCOM	7.2MVA
Digital delay of controller	100us

The current and DC capacitor voltage information can be obtained from the STATCOM system of the controller. The output of the converter is controlled by the duty cycle and the suitable PWM scheme based on the closed-loop controller design. The current loops are designed to achieve a high bandwidth control to regulate the current. The I_d channel is utilized to control the DC bus voltage with a slow voltage loop regulator, and the I_q channel is directly utilized to respond to the reactive compensation command. The closed-loop current loop is regulated by the PI regulator H_{id} and H_{iq}. The closed-loop voltage loop is regulated by the PI regulator H_v. The phase-shifted carrier PWM is used to switch the power devices in the different H-bridges.

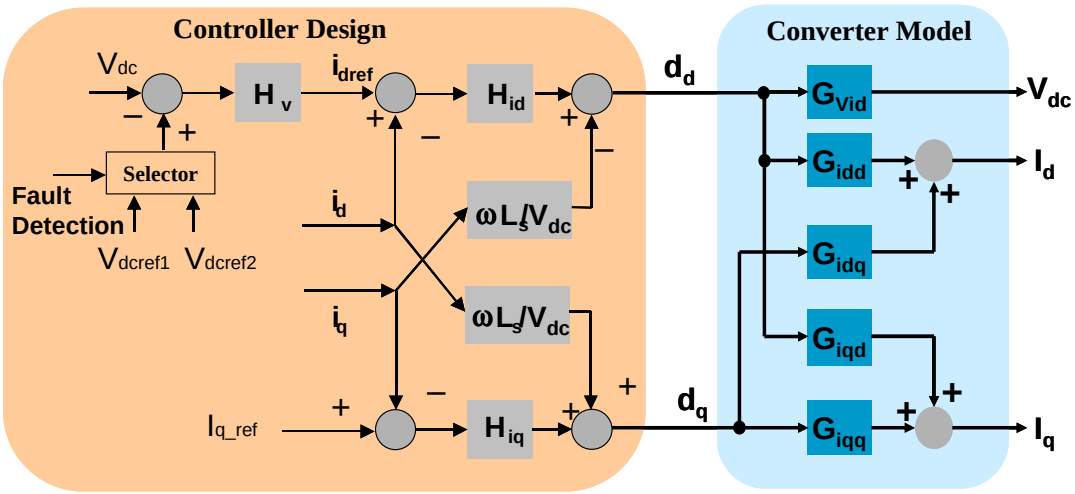


Fig. 5.9 Modeling and control diagram of CHMC-based STATCOM

Based on the model development, the converter model of STATCOM can be described as below.

The duty cycle-to-current transfer functions are:

$$G_{idd}(s)=\frac{\hat{i}_d}{\hat{d}_d}=G_{iqq}(s)=\frac{\hat{i}_q}{\hat{d}_q}=\frac{K_{idd}(\frac{s}{\omega_Z}+1)}{\left(\frac{s}{\omega_p}\right)^2+\frac{s}{Q\omega_p}+1} \qquad (5.6)$$

The current loop gain is:

$$T_{id}=G_{idd}H_{id} \qquad (5.7)$$

The d –current to capacitor voltage transfer function is:

$$G_{Vid}(s)=\frac{\hat{V}_{dc}}{\hat{d}_d}=\frac{-\frac{I_d}{C}}{s+\frac{1}{R_LC}} \qquad (5.8)$$

The voltage loop gain is:

$$T_V=G_{vid}H_{id}H_v \qquad (5.9)$$

The digital delay of controller is modelled to emulate the real digital control system:

$$G_D=\frac{1-sT_D/2}{1+sT_D/2} \qquad (5.10)$$

where

$$K_{idd}=\frac{V_{dc}R_S}{R_S^2+(\omega L_S)^2} \qquad Q=\frac{\sqrt{R_S^2+(\omega L_S)^2}}{2R_S}$$
$$\omega_p=\frac{\sqrt{R_S^2+(\omega L_S)^2}}{L_S} \qquad \omega_Z=\frac{R_S}{L_S} \qquad (5.11)$$

V_{dc} - Total DC capacitor voltage

L_S - Coupling reactor inductance

R_S - Coupling reactor ESR

C - DC capacitor capacitance

P_L - Equivalent converter loss of each HBBB

$R_L = V_{dc}^2 / P_L$ - Equivalent converter loss resistor

Based on the STATCOM model development and controller design, the control (duty cycle) of the reactive current and the DC capacitor voltage open loop bode plots can be expressed to determine the stability and transient performance. The bandwidth of the current loop is designed at 200Hz, which is about 1/5 of switching frequency in an effort avoid noise disturbance. The phase margin of the current loop is 60° to get good transience and stability performance. The bandwidth of the voltage loop is 20Hz which is much slower than the inner current loop bandwidth. The phase margin of the voltage loop is also designed to 60°.

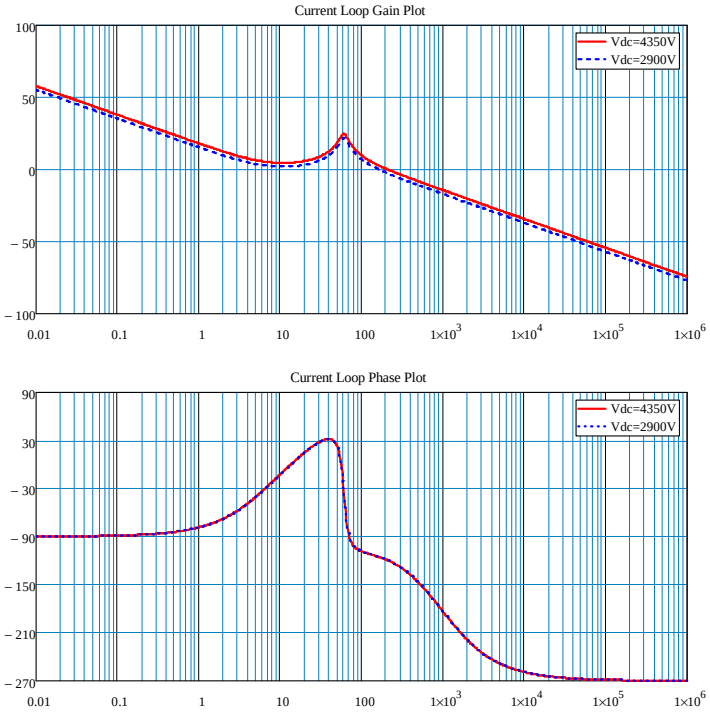


Fig. 5.10 Opent loop current loop bode plot in the fault tolerant transition

From the equations 5.6 and 5.8, when the STATCOM controller changes the operating mode from a 7-level output operation to a 5-level output operation, the total DC capacitor voltage will not change based on the proposed control strategy. Since the equivalent resistor for the converter loss dominates the zero of the voltage loop in the range of 0.1Hz, its effect to the voltage loop can be disregarded. The current loop and the voltage loop will not change from the 7-level operation to the 5-level operation, thus the control design is suitable for both the 7-level and the 5-level operation by using the proposed fault tolerant control strategy.

Although steady state operations can be guaranteed, it is important to analyze stability and transient performance during the fault tolerant transition from the 7-level operation to the 5-level operation.

In equations 5.6 and 5.7, the current loop in the fault tolerant transition is determined by the change of the total DC capacitor voltage. The open loop current loop bode plot during the fault tolerant transition is shown in Fig. 5.10. When the DC capacitor voltage varies between 2900V and 4350V during the fault tolerant transience, the controller bandwidth is around 200Hz and the 60° phase margin can be achieved.

In equations 5.8 and 5.9, the voltage loop in the fault tolerant transition is determined by the change of the d-axis current. When the d-axis current varies between 40A and 400A, the crossover frequency is around 7-20Hz and a phase margin higher than 60° can be achieved. The open loop voltage loop bode plot during the fault tolerant transition is shown in Fig. 5.11.

When the fault tolerant STATCOM controller is well designed based on the above analysis, this 7-level CHMC-based STATCOM can stably operate in both normal 7-level output operation and the 5-level output operation with the application of the fault tolerant design in the controller. Even in the fault tolerant transition from the 7-level operation to the 5-level operation, the proposed control will provide good stability and transient performance. This controller design method is applicable for the CHMC-based STATCOM fault tolerant design.

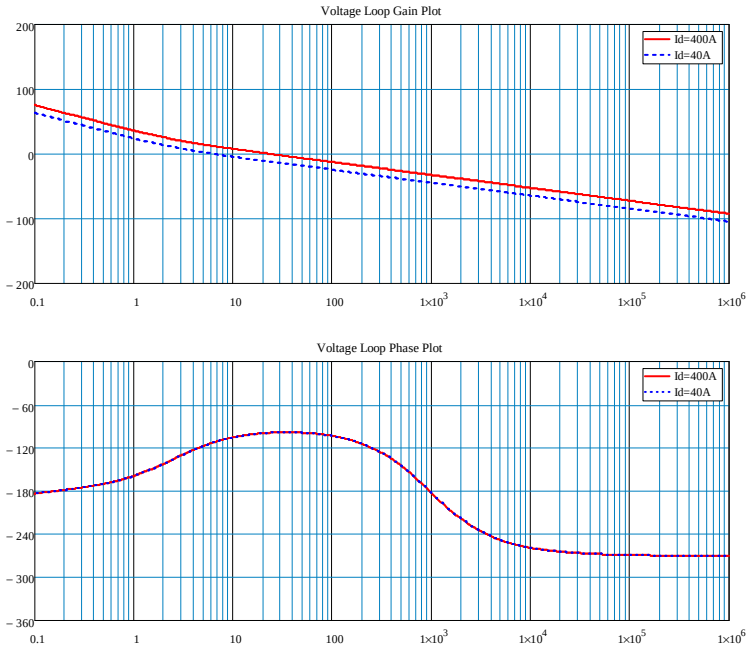


Fig. 5.11 Open loop voltage loop bode in the fault tolerant transition

The control performance of the study system is verified by simulation. The simulation investigation is implemented in Saber.

Fig. 5.12 shows the results of dynamic response of the studied STATCOM operating in full capacitive mode to inject reactive power to the power grid.

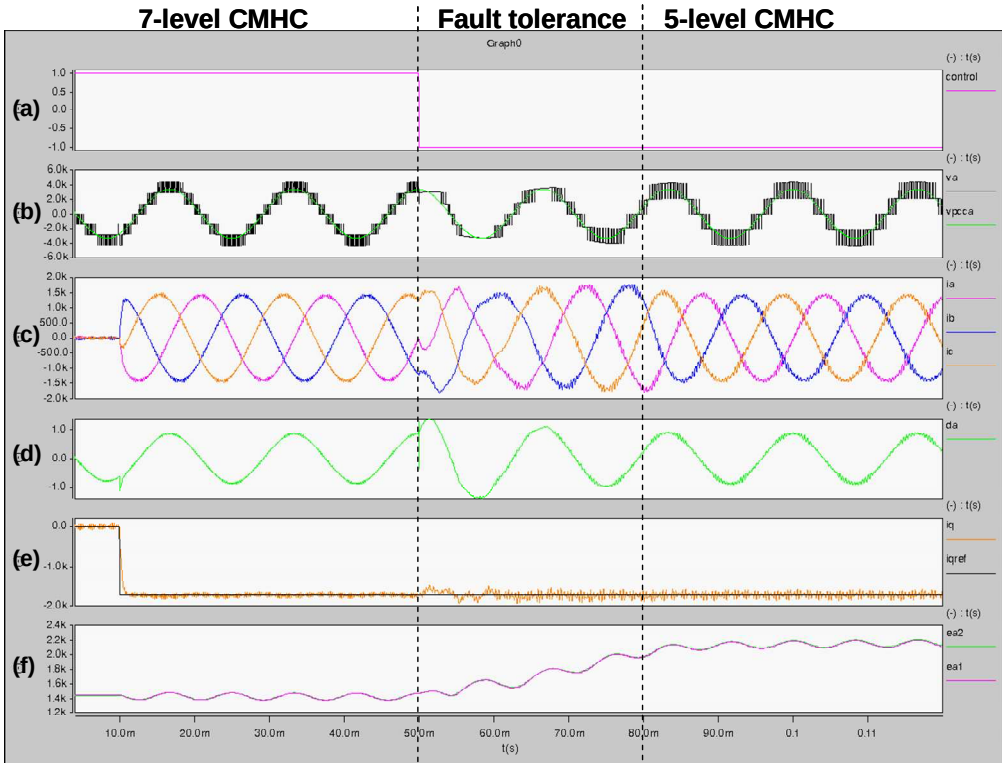


Fig. 5.12 Simulation of the fault tolerant STATCOM operation in full capacitive mode (a) fault detection signal (b) output voltage of converter and voltage at PCC (c) rhree phase current (d) duty cycle of the converter output (e) reactive current and reactive current reference (f) DC capacitor voltage

At 50ms, a fault is detected in one HBBB of one phase, and the failed HBBB is bypassed. Subsequently, the controller bypasses the two other HBBBs in the other two phases. The total system changes to a 5-level CHMC operation. The control strategy degrades the system from the 7-level output to the 5-level output. Since the total DC capacitor voltage does not change, the healthy DC bus voltages are charged. To avoid

excessive current during the fault tolerant transience while charging the DC capacitor, the current limit control is applied. In this simulation, the peak current limit is set to 2000A. While the output reactive power command does not change, the duty cycle will increase to meet the reactive power requirement due to the feedback controller operation. From the simulation results, we determine that the duty cycle increases immediately after the fault detection to retain the converter output, and therefore maintains reactive current generation. The duty cycle returns to the normal value after the DC capacitor charge. With the proper normal operating duty cycle and closed-loop controller design, excessive current can be avoided. A slope of DC voltage reference is introduced to improve the dynamic performance of the output current. The slope time step in this simulation is 30ms.

The relationship of maximum duty cycle and the normal operation duty cycle is shown in equations 5.12 and 5.13. When the converter output level is high (N is large), the change of duty cycle is relatively small. In this simulation, the normal capacitive mode operation is 0.8 and the maximum duty during the fault tolerant transience is 1.2. When the total capacitor voltage charges up to the normal value, the duty cycle decreases to 0.8 again.

$$N \times D_{normal} = (N-1) \times D_{TransMax} \qquad (5.12)$$

$$D_{TransMax} = \frac{N}{N-1} D_{normal} \qquad (5.13)$$

where

D_{Normal} - The duty cycle in the normal operation

$D_{TransMax}$ - The maximum duty cycle in fault tolerance

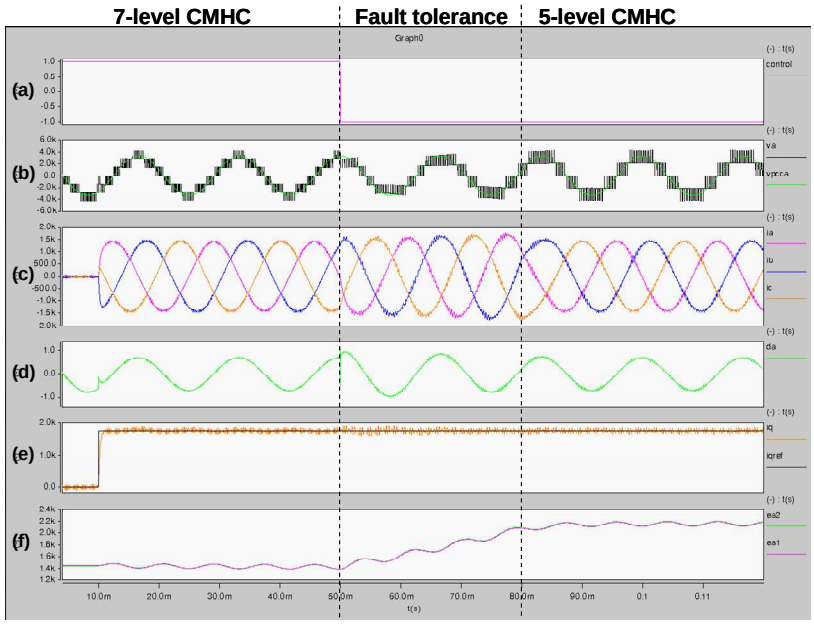


Fig. 5.13 Simulation of the fault tolerant STATCOM operation in full inductive mode (a) fault detection signal (b) output voltage of converter and voltage at PCC (c) three phase current (d) duty cycle of the converter output (e) reactive current and reactive current reference (f) DC capacitor voltage

Because the converter requires energy to charge the capacitor, active power flows into the converter from the power grid, the current does not lead the PCC voltage by exactly 90° and has little distortion because the STATCOM is absorbing active power from power grid during the charging time. During the fault clear period, the reactive power injecting into the grid is maintained.

Fig. 5.13 shows the results of dynamic response of STATCOM operating in full inductive mode to absorb reactive power from the power grid. The control strategy is the same. Absorbing reactive power is maintained during the fault detection and fault

recovery. The STATCOM system is transferred to an alternate safe operating mode smoothly.

Results in Fig. 5.12 and Fig. 5.13 indicate that the proposed fault tolerant control strategy operates successfully in the event of a device failure and HBBB redundancy is realized. Because the controller is well designed, the stability of STATCOM operation is achieved in the 7-level output mode, the 5-level output mode and the fault tolerant transient mode. By applying the DC capacitor voltage reference slope and the proper current loop controller design, the over current is avoided under the current limit control.

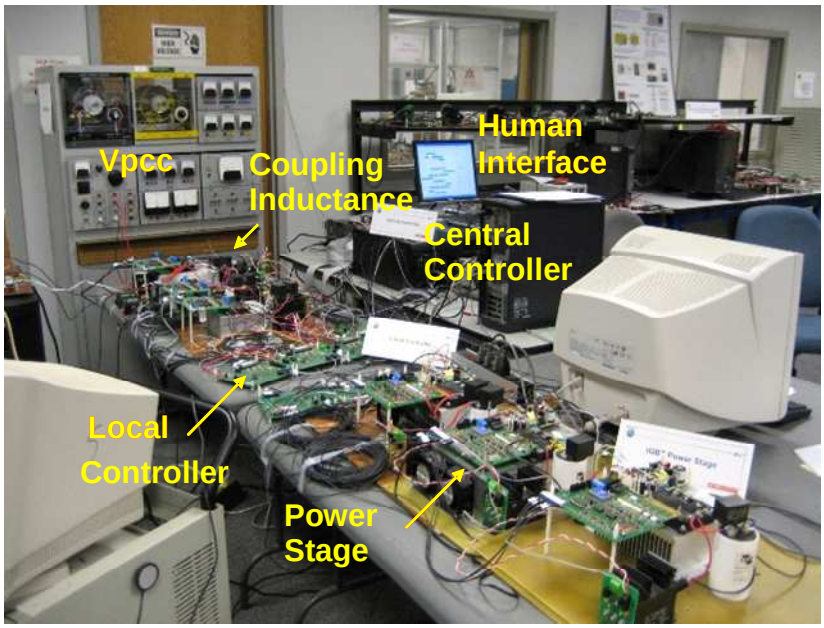


Fig. 5.14 5-level CHMC-based STATCOM prototype

To verify the proposed fault tolerant control strategy, a 5-level CHMC-based STATCOM hardware prototype has been built in the laboratory as shown in Fig. 5.14.

IGBT-based PM50RSA120 Intelligent Power Modules are used as HBBB-based converters. Each HBBB is controlled by an Altera FLEX 10k30A FPGA-based digital local controller through a driver board and optical fibers. The switching signals are generated by the digital central controller. The central controller includes a TMS320C6701 DSP board and an AED 106 FPGA daughter board. The controller system is a fully optical interface and is fully compatible with any optically triggered device-based power converter.

TABLE 5-5 specification of studied Experimental Statcom system

5-level CHMC based STATCOM	
Configuration	Balanced 3-phase 3-wire
Individual DC bus voltage in 5 level	29 V
Individual DC bus voltage in 3 level	58 V
Total DC bus voltage	58 V
Rated reactive current	4A
DC capacitor capacitance	2700uF
Equivalent loss of each HBBB	1W
Individual Switching frequency	300 Hz
Coupling reactor impedance	2.5mH
Coupling reactor resistance	180mΩ
PCC phase voltage	35V
Digital delay of controller	100us

For the experimental test, the 5-level CHMC based STATCOM will degrade to the 3-level STATCOM after the detection of the failure and bypass the failed HBBB. The controller is designed based on the specification of the experimental STATCOM prototype which is shown as Table 5-5.

Six IGBT-based H-bridges are built in the lab to achieve the basic three phase 5-level multilevel converter. Since the fault tolerant strategy is suitable for all different-level-output CHMC applications, the experimental setup is capable of verifying the proposed

fault tolerant control strategy. The switching frequency is 300Hz because of the calculation capability limitation of the applied FPGA resource utilization. Since the PWM method is not considered in the controller design, it will not affect the operation performance of the fault tolerant control design of the STATCOM system.

The controller design follows the controller design method previously presented. The current loop bandwidth is designed to 50Hz and the voltage loop bandwidth is designed to 5Hz. The phase margins are designed to greater than 60° for both 5-level and 3-level operations. The controller is carefully designed to provide enough phase margin in the fault tolerant transition from 5-level to 3-level operation.

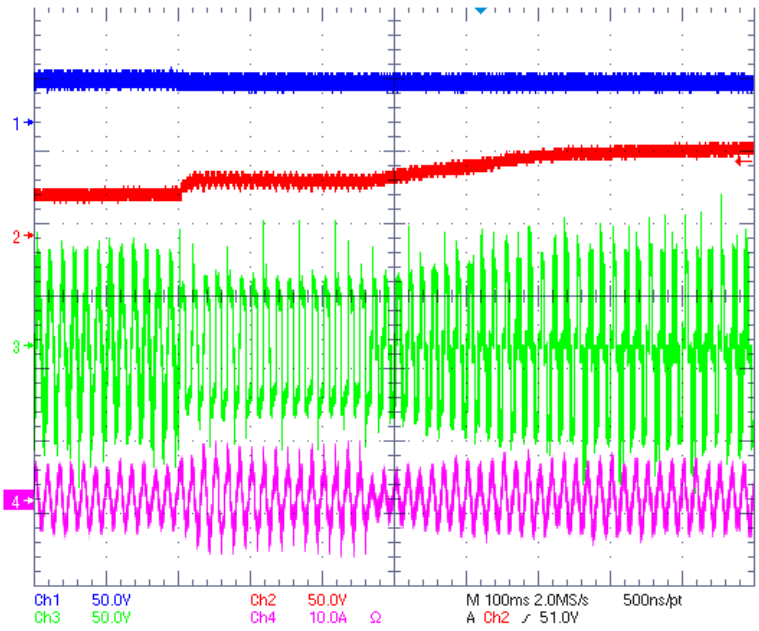


Fig. 5.15 STATCOM fault tolerant operation in the capacitive mode (1) DC capacitor voltage 1; (2) DC capacitor voltage 2; (3) converter output (4) reactive current

Fig. 5.15 and Fig. 5.16 demonstrate the experimental results of the fault tolerant design control strategy in the capacitive mode and the inductive mode of STATCOM separately.

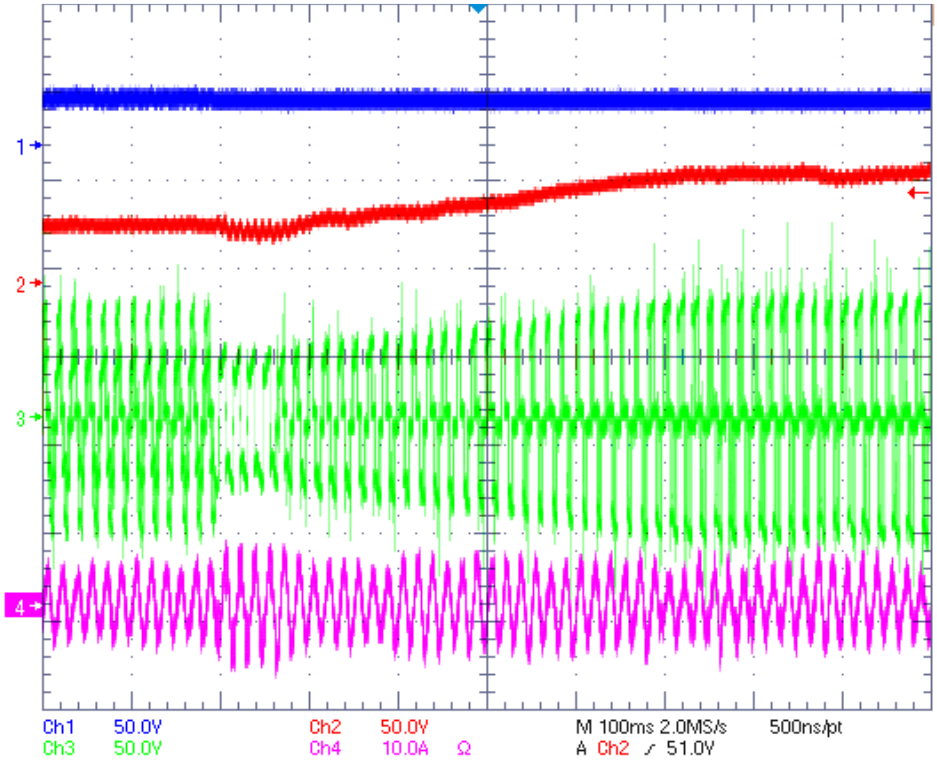


Fig. 5.16 STATCOM fault tolerant operation in the inductive mode (1) DC capacitor voltage 1; (2) DC capacitor voltage 2; (3) converter output (4) reactive current

Although one HBBB is lost because of the device failure, STATCOM can still inject/absorb reactive power to/from power grid to continue normal operation following the control commands by charging the DC capacitor voltage and adjusting the duty cycle of the converter output. The current waveforms are not consistent because the current sensor tolerance is large compared with the small current rating. In the experimental tests, the large reactive current occurs during the first few cycles of the fault tolerant transition.

Based on the above discussion of equation 5.12, the duty cycle will double and saturate in this 5-level output to 3-level output transition. The duty cycle is limited to 1.2 for a few cycles. The converter output is saturated too from the test results. After the DC capacitor voltage is charged up, the feedback control will adjust the duty cycle under the limit, and then the reactive current returns to normal operation. Because the inductive mode needs a smaller duty cycle, the over-current time interval is shorter than the capacitive mode. The charging time in the experimental test is longer than in the simulation because of the usage of a large DC capacitor and a small charging current. The application hardware limits the accuracy of the experimental test results, but the feasibility of the fault tolerant design for the CHMC-based STATCOM can be verified.

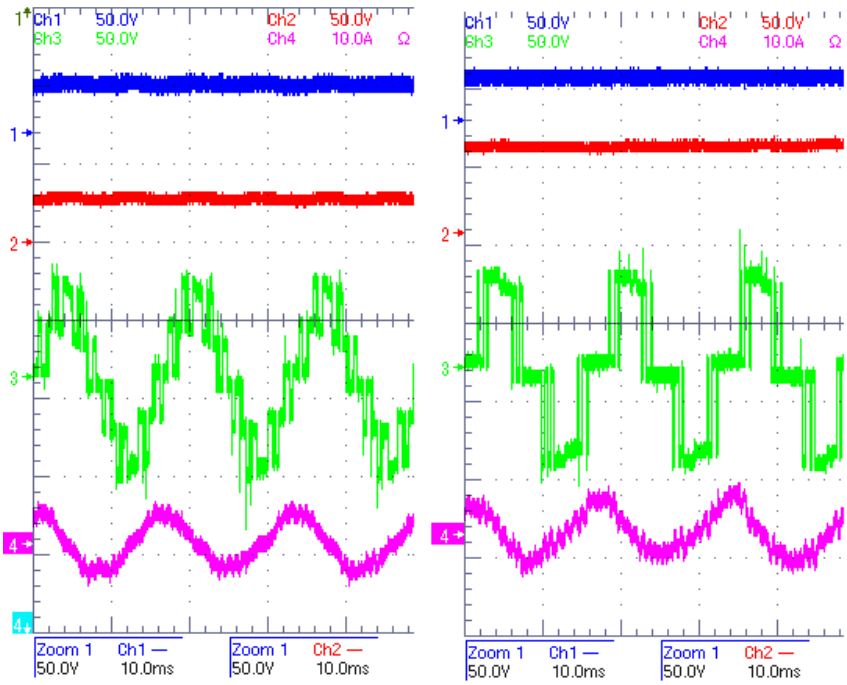


Fig. 5.17 STATCOM capacitive mode operation in (a) 5-level output (b) 3-level output

Fig. 5.17 shows the zoom-in capacitive operation waveforms of STATCOM at 5-level output operation and the 3-level output operation. The reactive current is maintained even though the STATCOM loses one HBBB and two output-levels.

From the experimental results, one can see that the DC capacitor voltage is charged from 29V to 58V after fault detection and the reactive current is maintained because of the implementation of fault tolerant strategy for STATCOM operation. During the fault tolerant transition the current loop works well to keep the reactive current steady by changing the duty cycle when the DC capacitor voltage is low, thus the large over-current is avoided.

The experimental results verify the feasibility of the proposed fault tolerant control strategy.

A fault tolerant control strategy to achieve HBBB redundancy in CHMC-based STATCOM system is proposed and verified by simulations and experiments. As a result, the reliability of the STATCOM is enhanced greatly with the redundant HBBB, and at the same time the output voltage waveform quality is improved. The extra cost and size are relatively small compared with the high output level. Even losing two output levels, the output (reactive power) still can be maintained by the proper control design. The controller design considerations are discussed to provide the necessary stability and transient performance during the fault tolerant transition. The simulation and experimental test results verify the feasibility of the proposed fault tolerant design. The proposed fault tolerant control strategy is suitable for any-level CHMC topology. This fault tolerant control strategy can be also applied to other CHMC-based FACTS

applications, such as Static Synchronous Series Compensation (SSSC) and Unified Power Flow Controller (UPFC).

5.3. Distributed Solution

The ETO-based DPFC was first proposed in [55]. It has a single phase HBBB based ETO light converter module, modular digital controller and communication links. Unlike conventional power converter based series compensation solutions, it connects to the power line directly without the necessity for a transformer because of its high voltage/current capability and the self-power generation functions. The rating of ETO light converter (1-2 MVA) is suitable for typical 138kV-500kV power transmission line applications. The DPFC module is controlled by the station control commands based on the compensation requirements via system information. The communication between DPFC module and the station control could use either optical fibers or wireless communications.

Because of the fully modular design, the multiple DPFC modules could be installed to the transmission line flexibly, based on power transmission requirements. A flexible series connection provides a good opportunity to achieve redundancy for the fault tolerant design.

Fig.5-18 shows the DPFC application diagram in the three phase power transmission system to achieve the fault tolerance. Redundant DPFC modules can be connected to the power line for each phase. During normal operation, redundant DPFC modules will be bypassed and out of service. When one operating DPFC failure is detected, the failed DPFC module will be protected by the bypass switch and the fault indication signal will

be sent to the station control. Then the redundant DPFC module will be series connected to the power transmission line and inject the compensating voltage into the power grid to control active power through the power line as normal operation.

The low cost, easy installation and easy maintenance are achieved because of the standard design, modularity and suitable power rating of the DPFC module based on the ETO Light converter. This modular design and the modular control of megawatt DPFC applications will provide good opportunities for the fault tolerant design in the power transmission system as an enhancement of reliability.

In order to verify the feasibilities and functions of the proposed fault tolerant power flow controller design, a two-machine one-bus transmission line system is introduced to the simulation setup shown as Fig. 5.3. The simulation parameters are shown in Table 5-3.

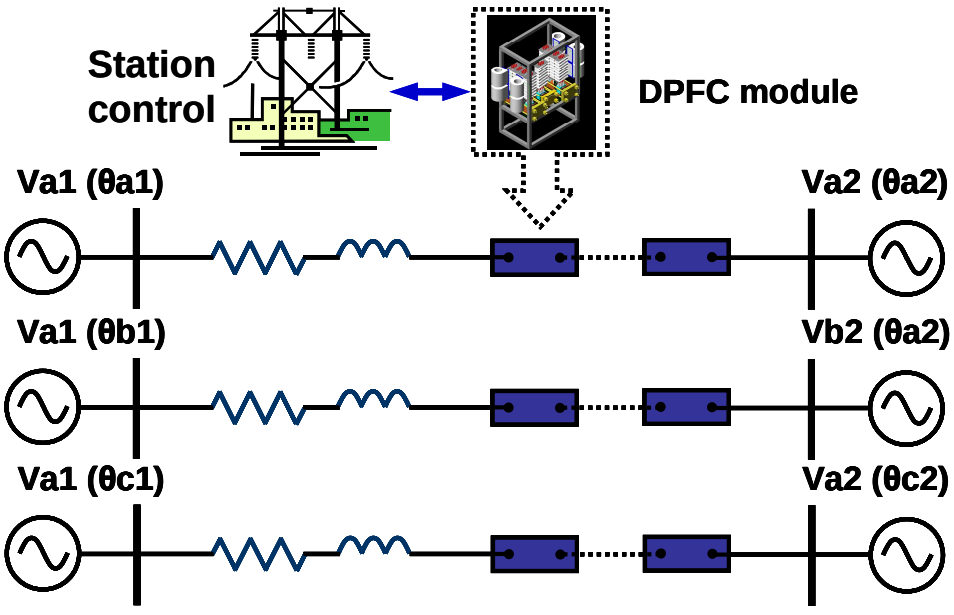


Fig. 5.18 DPFC redundancy design

The simulation results of the fault tolerant distributed solution for the power flow controller are shown in Fig. 5.19. Fig. 5.19 (a) and Fig. 5.19 (b) show the line current and the compensating voltages of the faulty DPFC and the redundant DPFC respectively. The DPFC module is operating in the capacitive mode to decrease line impedance and increase line current and the transmitted active power. Fig. 5.19 (c) shows the RMS line current and Fig. 5.19 (d) shows transmitted active power through the transmission line.

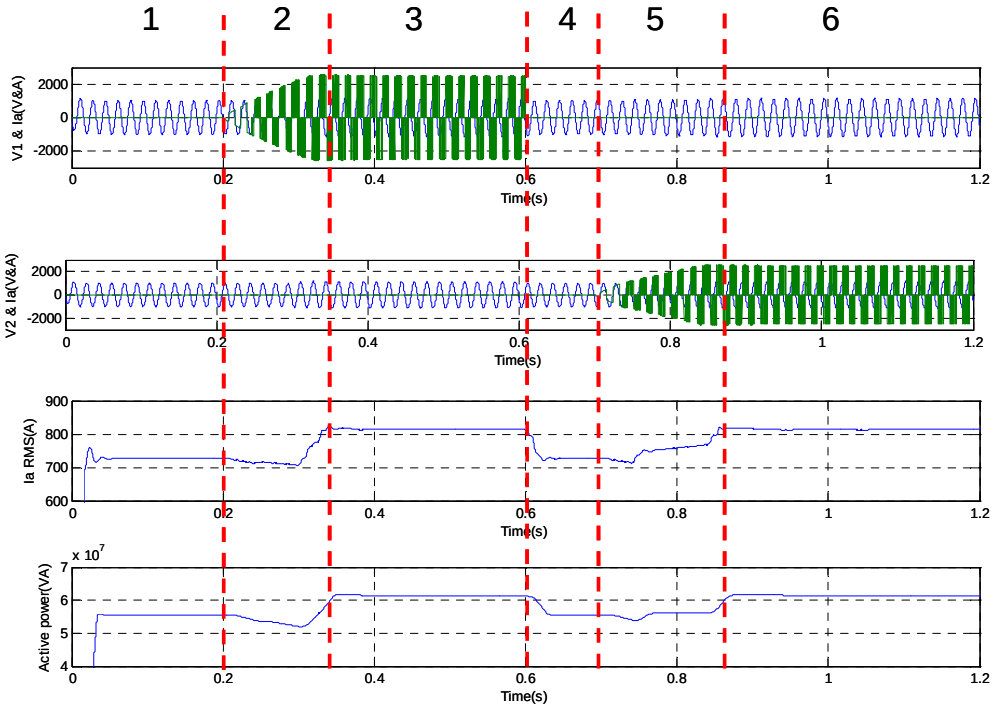


Fig. 5.19 Simulation results of distributed power flow controller (a) line current and injectting voltage of faulty DPFC. (b) line current and injecting voltage of redundant DPFC (c) line current RMS value. (d) transmitted active power.

The fault tolerant operations of distributed power flow controller have six steps:

(1) The power flow controller is out of service. The line current goes through the turned-on bypass. The line current is around 720A and the transmitted active power is around 56MW.

(2) When the operation command is immanent, the bypass switch is turned off and line current will go through the power flow controller converter and charge the capacitor. This charging operation has two modes: diode charge mode and PWM charge mode. At first, the control power is not built up; the DC capacitor voltage is charged automatically by the four anti-parallel diodes in HBBB. When the voltage of DC capacitor is charged to some predetermined level (1000V in the simulation), the controller has the control power and the voltage loop of DC voltage starts to generate the PWM switching signals to control the converter, then regulate the DC voltage to the reference value. In some cases, the PWM discharge mode can be applied to dissipate the energy in the bulk DC capacitor rapidly.

(3) A DPFC module is operating in the capacitive mode and acting as a controllable series capacitor, the equivalent line impedance decreases and the line current and the transmitted active power flow increase to the 800A and 62.5MW.

(4) One DPFC module converter failure is detected and the faulty DPFC is bypassed. Without compensating voltage, the line current and the transmitted active power through the transmission line is reduced to 700A and 56MW.

(5) The redundant DPFC is put into service to charge the DC capacitor voltage and initiate the control power, and then the controller regulates the DC capacitor voltage.

(6) The redundant DPFC is operating as a replacement to recover the line current and active power back to the pre-fault situation.

The simulation results validate the feasibility of these two fault tolerant design to improve the reliability and availability of the power flow controller. When the HBBB faults occur, the faulty HBBB will be bypassed and then the fault tolerant operation will start to recover the operation back to the pre-fault situation.

5.4. Summary

The two control strategies to achieve the fault tolerance in ETO Light converter based transformerless power flow controllers are proposed in this paper. The reliability and availability of the power flow controller could be improved and enhanced by the multilevel solution and the distributed solution. By applying the fault tolerant design, the injecting voltage (converter output) of the power flow controller can be maintained at the proper level under the fault condition. The gain scheduling compensation design is applied to cancel the current influence to the feedback control loop. The transformerless connection is possible due to the high voltage/current capability and control power self-generation function of the ETO Light converter. Therefore the proposed scheme is quite suitable for high power applications because of its low cost, modularity and high reliability. The simulation results and the experimental results verify the feasibility of the proposed fault-tolerant protection scheme of the power flow controller.

Chapter 6. Conclusion

The design and development of Distributed Power Flow Controller has been developed to improve the converter-based series compensation application performance

This dissertation discussed the design, modeling development, control design, applications and fault tolerant design of the DPFC.

Major contributions are achieved as follows:

(1) The DPFC concept using the standard low-cost, high-reliability and short-building-cycle high power converter, combining the emerging semiconductor device, modular converter topology and modular controller techniques, has proposed and developed.

(2) The digital local controller system has been designed and developed. The feasibility of this local controller has been verified by experimental tests in pulse tester and boost converter. The local controller subsystem has been applied to multilevel converter based STATCOM projects.

(3) The single-phase DPFC modeling development and control design methodology have been developed. The parameters influence to the controller was discussed. The gain scheduling control was proposed and verified. The proposed modeling and controller design is verified by calculations, simulations and experimental tests.

(4) The applications of DPFC in transmission systems, distribution systems and demand side management applications have been proposed. DPFC applications with renewable energy source were proposed and studied. The feasibility of the proposed applications was verified by the simulation results.

(5) The fault tolerant designs of the protection scheme and redundancy control strategy power flow control applications have been proposed and developed. Multilevel solution and distributed solution were proposed by simulations and experimental tests.

The future work for this research work of DPFC includes:

(1) Further investigation of the DPFC applications

The newly development of the semiconductor devices and the rising demands in utility application provide a lot of opportunities of power flow control. With the promotion and development of smart grid and renewable energy application in the power system, the DPFC applications will extend to different areas, from the high voltage transmission system to the residential distribution system.

(2) Further improvement of DPFC power stage design

Modular converter topology, ETO semiconductor device enable the low cost, high reliability and transformerless connection of DPFC in transmission system application. With the new proposal of the DPFC applications, the power stage design with different voltage/current rating in different application areas should be paid more attentions.

(3) Further DPFC control development

The controller response to the disturbance and parameter variation also need to be considered in the future study of DPFC applications.

(4) The DPFC fault detection and protection

Although the fault tolerant design has been proposed, the DPFC converter protection scheme is still one open research topic for real applications.

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