ABSTRACT

YIN, HONG. A Physics-based Large-signal Analytical Model for AlGaN/GaN HFETs. (Under the direction of Dr. Robert J.Trew and Dr. Griff L. Bilbro).

In this work, a complete physics-based large-signal model for AlGaN/GaN HFETs is developed. The model consists of two modules. An analytic DC model with no fitting parameters for both linear and saturated operation works as the DC module. Nonlinear analytic models for the I-V characteristics are developed in detail in this DC module.

Under linear operation, the AlGaN/GaN HFET structure is divided into three zones before saturation: two zones in the two access regions; and one zone beneath the gate. In the source and drain access regions, nonlinear resistances are investigated and modeled. The nonlinear resistances affect drain current compression, which leads to a bell-shape transconductance. The Gradual Channel Approximation (GCA) is assumed in the region beneath the gate. After saturation, two additional zones appear at the gate edge close to the drain. They are denoted Space-Charge-Limited (SCL) and Charge Deficit Zone (CDZ) because of their transport physics and are proven dominant in saturated operation. For verification purpose, variant sets of examinations are designed and executed to prove the accuracy of models for each zone. The resulting equations in the various zones are linked together by voltage and current continuity at the boundaries.

Good agreement between simulated and measured DC IV and transconductance is demonstrated without any adjustable fitting parameter. The RF module integrates the time-

domain non-linear device model and the frequency-domain circuit model to form the complete simulator. Good agreement between simulated and measured dc and RF data is obtained for a practical device. This model is proven to be much more suitable in device design than empirical models since it is capable of predicting the operation of a device before its characterization. Meanwhile, it is much faster than physics-based numerical simulators, such as ATLAS. A large-signal equivalent circuit is suggested for future improvement and integration into commercial circuit simulators.

A Physics-based Large-signal Analytical Model for AlGaN/GaN HFETs

by
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Dr. Doug Barlage	Dr. Mark Johnson

DEDICATION

Dedicated to my grandparents…

BIOGRAPHY

Hong Yin was born in Beijing, China in 1982. He attended Beijing Institute of Technology, China in 1997. There he graduated with a Bachelor of Science degree in Applied Physics, with minors in Electrical Engineering and Computer Sciences in 2001. In the same year, he enrolled in the Department of Electrical and Computer Engineering at North Carolina State University. After acquisition of a Master degree in Electrical Engineering in 2004, he started his research project under the supervision of Dr. Robert J. Trew and Dr. Griff L. Bilbro. His Ph.D. research focused on the large-signal physics-based analytical modeling of AlGaN/GaN HFETs. He works as a Device Modeling Engineer Intern at RF Micro Devices, Greensboro, NC during the spring semester of 2008. His research interests are analytical physics-based solid-state device modeling/simulation and III–V compound devices.

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I would like to thank other members of my research group, Yueying Liu, Danqiong Hou, Weiwei Kuang and Ryan Schimizzi, for their support. I benefit from the discussions with them. Ryan is the first reader and commenter of this thesis, I really appreciate his help.

Special thanks and appreciation are given to my good friends here at NC State University. Their encouragement, care and help made my life here enjoyable.

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CHAPTER 1

1.1 Overview

AlGaN/GaN HFETs promise performance advantages for next generation communications and radar systems [1]. These devices are advancing from the design prototype stage to system insertion in various applications. A compact large-signal model suitable for use in commercial microwave circuit simulators is required to take full advantage of this new technology. The most widely used AlGaN/GaN HFET large-signal models are large-signal empirical equivalent-circuit device models developed for GaAs MESFETs, with fitting parameters re-adjusted for AlGaN/GaN HFETs. Since equivalent circuit-based models are not physics-based, they cannot be used to predict the operation of a device before it has been characterized. Therefore they cannot be used to optimize the design of an existing device. An alternative is models based on two-dimensional physics-based numerical device simulators. However, this kind of model is computationally too complex for large-signal RF models.

In this project, we build a complete physics-based model for the AlGaN/GaN HFET suitable for use in circuit-level harmonic-balance simulators. The time domain part of the model is based upon our dc model [2]-[4] and the extension of the dc model to RF conditions [4]. The DC module generates lookup tables of components from the RF large-signal equivalent circuit for integration into the harmonic-balance simulator. After the DC module is implemented, it generates several lookup tables containing values of large-signal equivalent

circuit components throughout the entire ranges of voltage and current. These lookup tables supply the following RF module which carries out a harmonic balance simulation to complete the large-signal modeling. The simulator computation time is sufficiently short for automated optimization of the physical design of an HFET to maximize its large-signal RF performance while preserving good agreement with 2D numeric simulations. Good agreement at DC is preserved without adjusting empirical equivalent-circuit parameters. Parameters in the new model describe either a fabrication dimension or a material property. As a result, design can be optimized by changing the corresponding fabrication structure or material parameters. Good agreement is achieved between the simulator performance and experimental data for both DC IV parameters and RF large-signal operation. The structure for the device reported in this work is shown in Fig. 1.1, which shows the fabrication structure of an AlGaN/GaN HFET. This figure was generated by the ATLAS commercial simulator.

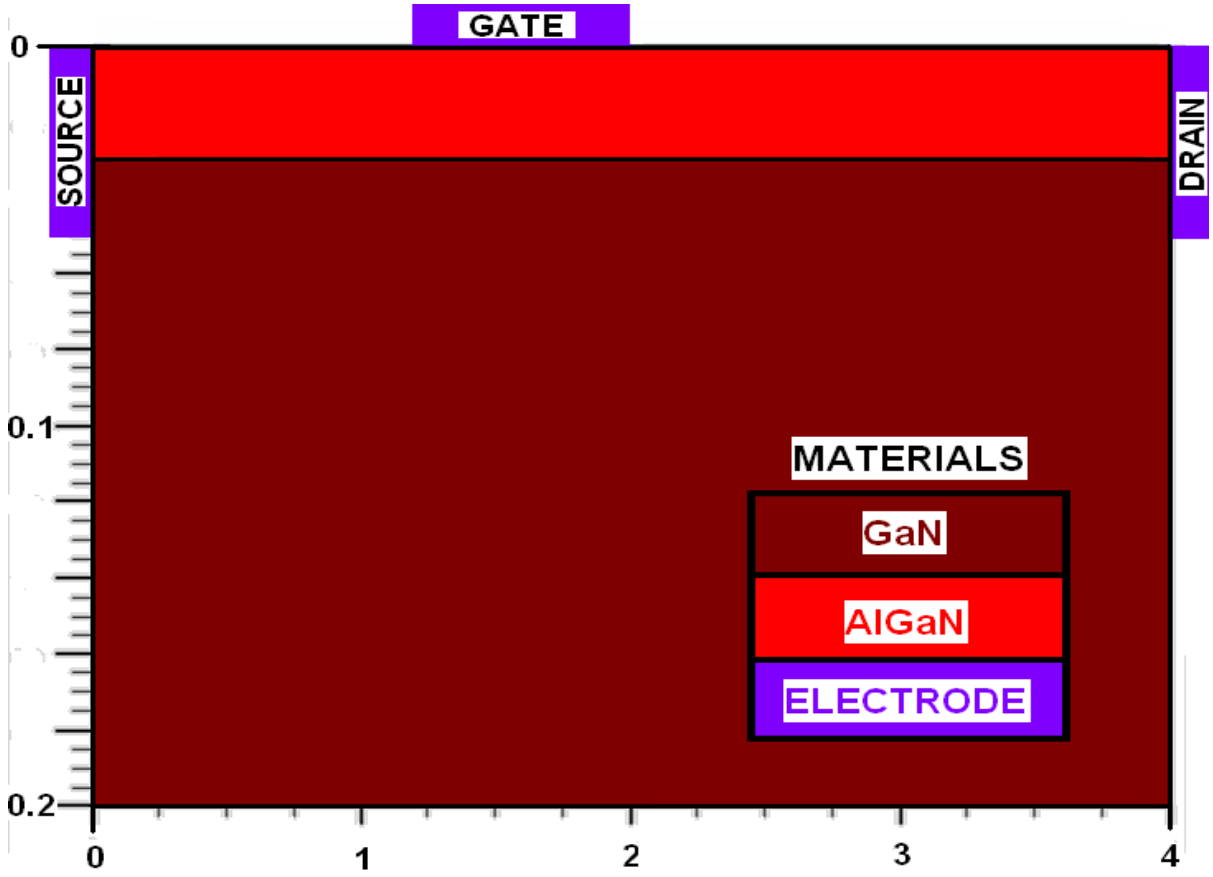

Fig 1.1: Device fabrication structure (generated by ATLAS). All units are in microns

1.2 Polarization charge in AlGaN/GaN HFETs

Nitride materials (GaN, AlN, InN and their ternaries) exist in two crystal structures: Wurtzite (WZ) and Zinc-Blende (ZB). Wurtzite is the most common crystal structure for nitridematerials used in electronic devices. It is a structure of hexagonal crystal systems where tetrahedrally coordinated Ga (Al, In) and N atoms are stacked in an ABABAB fashion.

Even when there is no external strain or electric field, nitride materials have spontaneous polarization inside themselves because of the non-centro-symmetric nature of the Wurtzite structure. Besides spontaneous polarization, piezoelectric polarization is present when Wurtzite-structure nitride materials are stressed along the [0001] direction. Stress is formed due to the difference of lattice constants between GaN and AlGaN. These polarization effects induce positive electrostatic charges at the AlGaN/GaN interface. This positive sheet charge results in a large amount of electrons confined in the quantum well at the GaN side of the AlGaN/GaN interface. This process is the main merit of the AlGaN/GaN heterojunction bringing AlGaN/GaN HFETs many advantages over other devices [1]. The typical device structure together with conduction band diagram and illustration of the polarization induced charges is shown in Fig. 1.2 [5].

Fig 1.2 also implies that the amount of electrons should be equal to the surface charge at the upper surface of AlGaN because the polarization charge in the AlGaN should neutralize itself. This is shown in Fig 1.3 and reported in detail [6].

In the modeling approach of this polarization effect, the polarization charge is considered to neutralize itself. Fig 2.4 shows usual polarization charge settings in AlGaN/GaN HFETs, which are considered equivalent to each other in terms of device performance [2]-[4], [7][8]. In all three settings, the 2DEG's electron density is equal to the amount of surface state's charge density. The third setting, however, has a potential problem of shifting the pinchoff voltage but the current and capacitances in the equivalent circuit keep their values. This project is employing the second setting.

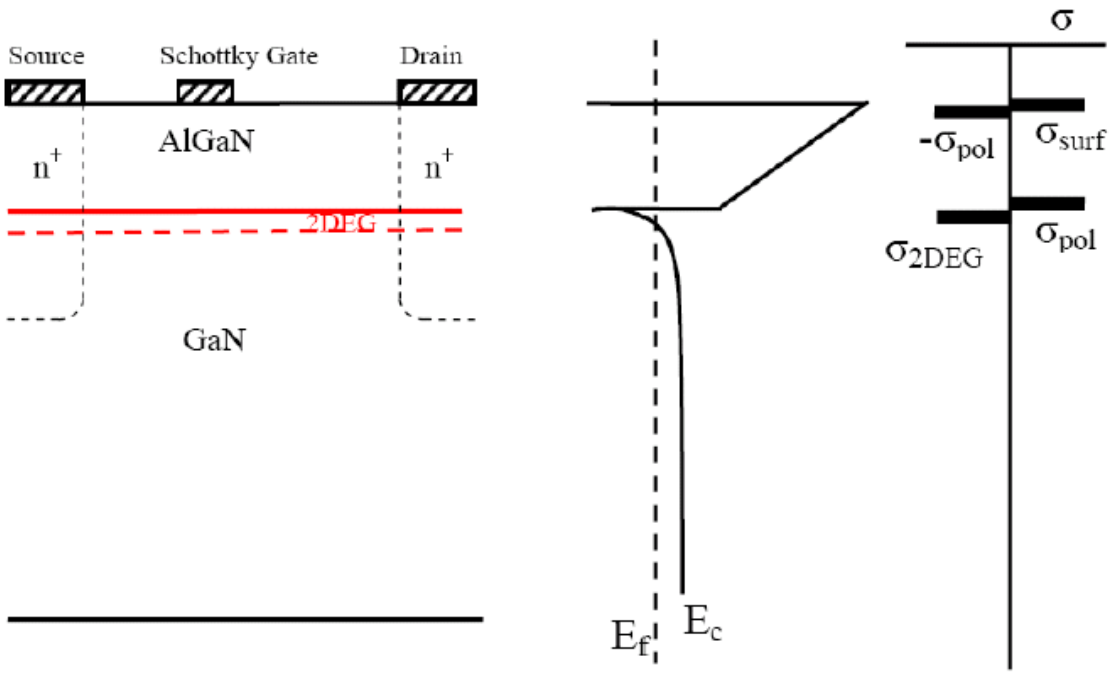

Fig. 1.2 (a) Cross section of an AlGaN/GaN HFET; (b) Corresponding energy band diagram; (c) Corresponding space charge components in the device [5]

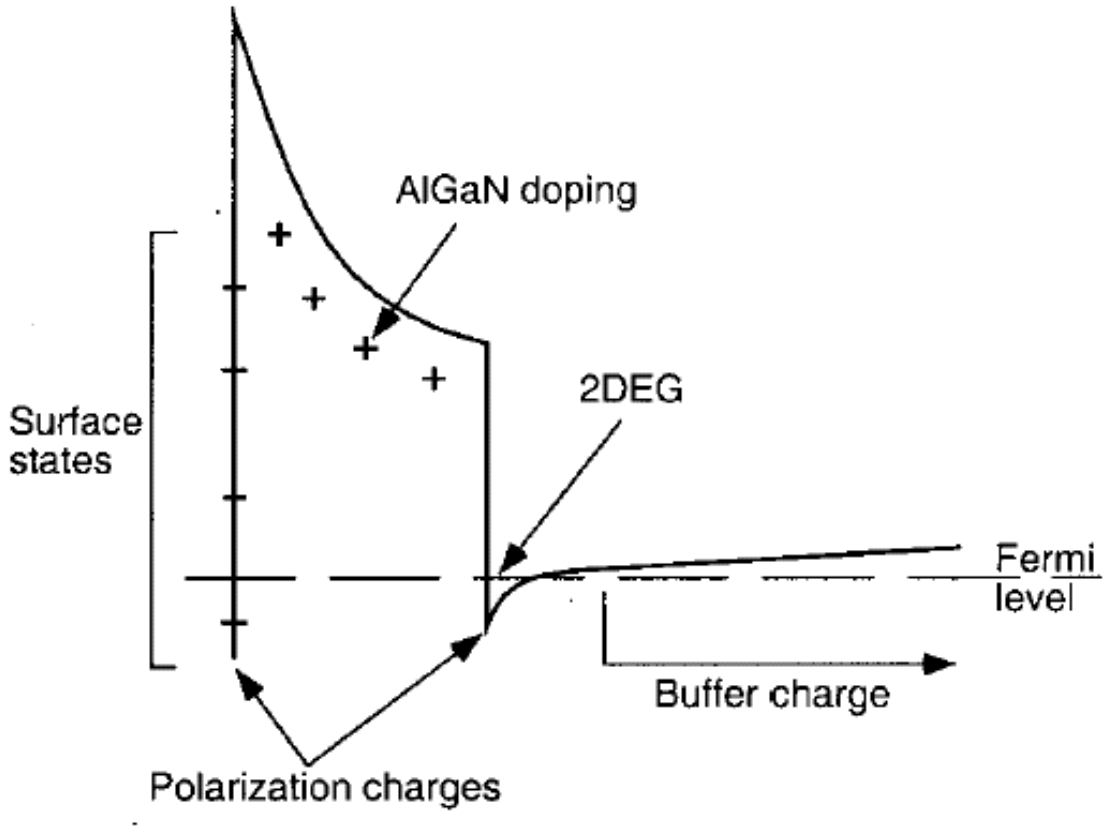

Fig. 1.3 Schematic conduction band diagram for an AlGaN/GaN HFET with space charge components in the device [6]

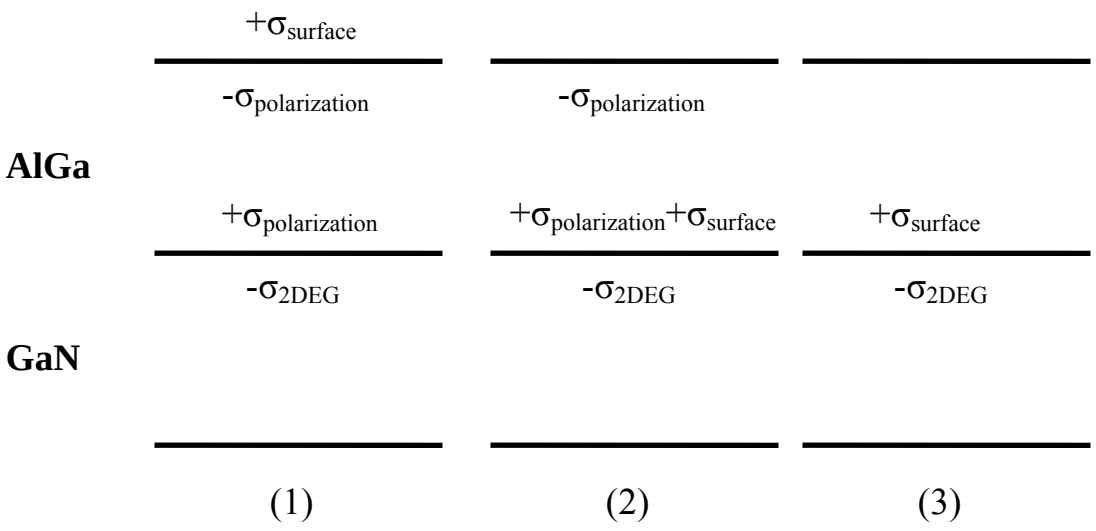

Fig 1.4: Equivalent modeling approach on polarization charge in AlGaN/GaN HFETs

1.3 Models

The intriguing nature of AlGaN/GaN HFETs has attracted tremendous research interest since their inception. Researchers are continually progressing in better understanding this kind of device. Consequently, various types of models are under development for AlGaN/GaN HFETs.

Among all models of AlGaN/GaN HFETs, the most popular kind of model is an empirical model. Most empirical models are already integrated into commercial circuit simulators, such as Agilent EE HEMT1 [9] and AIM Spice [10]. The main advantage of an empirical model is its capability of modeling a device without fully understanding the device's physics. However, all model parameters are required to be extracted from device characterization before the model works. Hence parameters are not predictable before the complete set of measurements is applied. Moreover, a novel design can not be evaluated until a real device is processed and characterized. Meanwhile, the lack of understanding of the device physics may prevent further improvement.

Another modeling approach is TCAD simulation. TCAD simulations can help us to understand device physics and operation mechanisms. An example is ATLAS, a PISCES based two-dimensional numerical device simulator from Silvaco [11], which is also the numerical simulator used in this project. After creation of an appropriate mesh and definition of simulation parameters and models, numerical simulation is ready to be performed. During

the simulation, a set of fundamental semiconductor equations, including Poisson's equation, continuity equations, and transport equations are solved for every grid point. Numerical simulators perform excellently in predicting the device performance. Unlike empirical models, numerical simulations are performed before any real device is processed and fabricated. However, its main shortcoming is the tremendous time and resource consumption required by the simulator. This makes numerical models inappropriate for large-signal modeling which usually requires numerous simulations.

As a consequence, a physics-based analytical model is of great research interest. Researchers have been working toward such a model whose physics-based features give insight into the device physics, and whose analytical features allow it to support a large-signal model. The idea of dividing the HFETs' channel into zones has been a research focus for a long time [2]-[4] [12]-[14]. In this project, we successfully build a physics-based analytical model for large-signal simulation employing this zone-division idea for the first time. This new model is not only physics based but also analytical. The zone-division methodology and the large signal circuit with analytical components are shown in Fig 1.5.

The model results are verified by ATLAS numerical simulations and experimental data. The model structure and verification process are shown in Fig 1.6, which is discussed in details in Chapter 6. The multifold process designed in this project verifies not only the final model result but also the prediction of each zone's model. The verification data include the DC and

RF experimental data, together with simulation data generated by ATLAS 2D numerical simulator, which is pre-calibrated by the experimental DC IV data.

The input parameters of this model include the device's fabrication structure and material properties parameters, which is listed in Table 1.1.

Table 1.1 Input parameters of the model

Fabrication parameters	Gate-Source Spacing
	Gate-Drain Spacing
	Gate length
	Thickness of AlGaN layer
	Thickness of GaN buffer layer
	Doping density of AlGaN layer
	Doping density of GaN buffer layer
	Gate eletrode metal workfunction
	Positive sheet charge density for 2DEG
	Polarization sheet charge density
	Affinity of AlGaN
	Affinity of GaN
Material properties parameters	Low-field mobility
	Electron saturation velocity
	Order of velocity-field curve
	Permittivity of AlGaN
	Permittivity of GaN

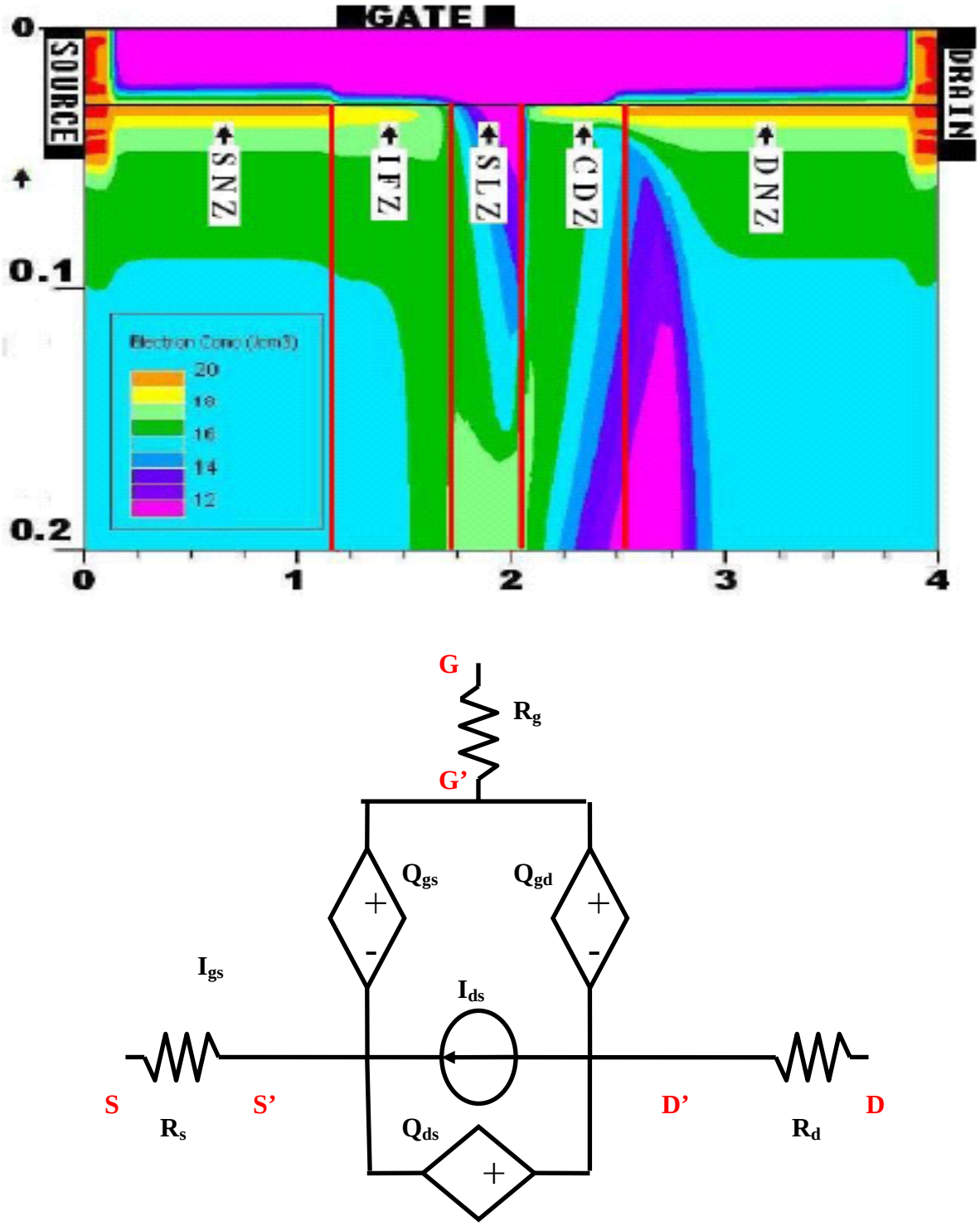

Fig 1.5: Zone-division methodology and large-signal circuit with analytical component

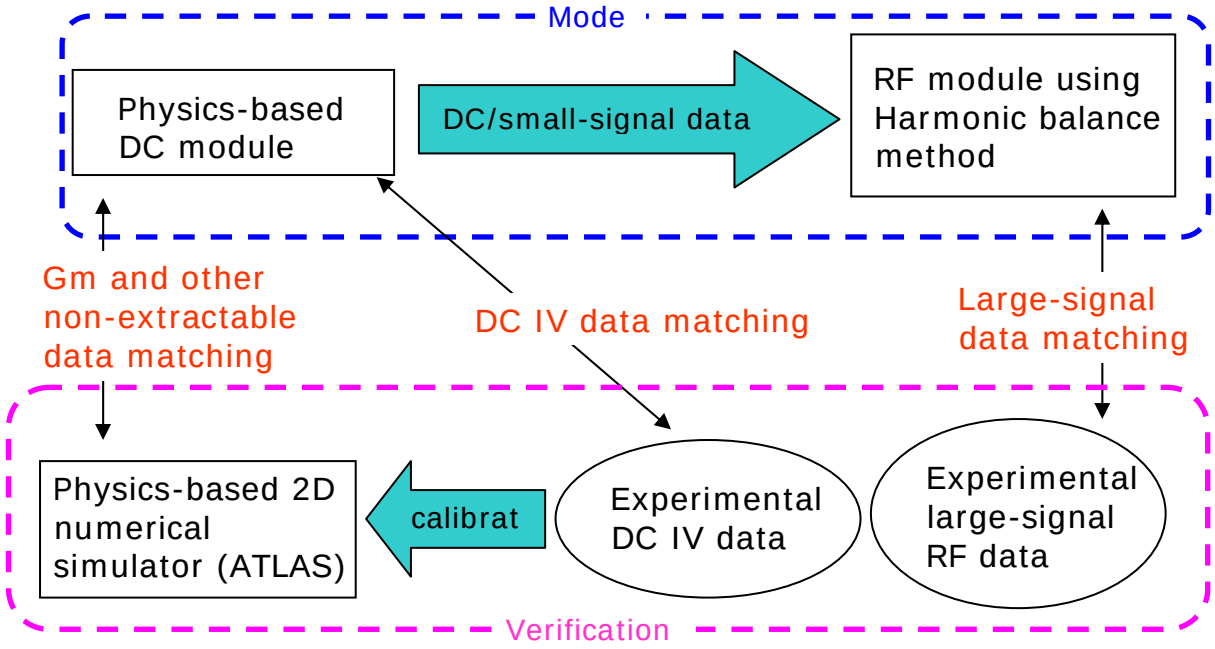

Fig 1.6: Flow chart of the project for the complete model

1.4 Outlines

In order to systematically describe and explain this new physics-based model, the dissertation begins from an introduction to the three types of AlGaN/GaN HFETs' models, including empirical, numerical, and the physics-based zone-division model.

The dissertation is comprised of the following chapters:

Chapter II explains the novel zone-division method employed in this model. This particular method makes the model distinct from any previous model. Moreover, this method makes the model purely physics-based, which has never been reported before. For all zones, particular analysis of the operation modes and the physical picture is introduced in detail.

Chapter III investigates the nonlinear source and drain resistances, together with the corresponding performance degradation in AlGaN/GaN HFETs. The physical origin is discussed in depth as the basis of the model for the corresponding zones. Model verifications are executed

Chapter V explores the additional changes happened in the device after the device saturates. For the first time, additional zones are observed under such circumstances. Physics-based models for the resulting zones are innovatively built.

Chapter VI describes how all zones with their own physics-based models are connected.

Equivalent circuit component determination is discussed as well. A large-signal equivalent circuit is purposed for future integration of this model into circuit simulators.

Chapter VII summarizes the results of this work and proposes the guidelines for future work.

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CHAPTER 2

2.1 Zone division

As introduced in 1.3 previously, there have been a variety of attempts to model a HEMT through the zone-division method. Zone-division allows a better approximation and derivation in each zone where the dominant relationship, either empirical or physics-based, can be distinguished. This method offers a solution for acquiring analytical expressions in each zone. At the same time, voltage and current continuities can be used as boundary conditions to connect all zones. This method can lead to a complete solution to the whole device by identifying the boundary conditions at the source and drain with external bias or current injection. The first step of zone-division is to divide the device into several zones. As will be described in detail later, both the number of zones and the physics in zones are subject to change with the mode under which the device operates.

2.1.1 Three types of Device operations and corresponding zones appearance

AlGaN/GaN HFETs demonstrate promising performance in various kinds of applications. However, in different applications, the device may need to work in different operation regions for desired device behaviors. For example, during the application as a class A or class AB power amplifier, the AlGaN/GaN HFETs usually work in the saturation region. Alternatively, the transistor is usually in pinchoff operation when it works as a switch or as a class B power amplifier.

During our research on AlGaN/GaN HFET modeling, we observed that the device employs related but different physics while working in different operating regions. In this work, three operating regions are distinguished for an AlGaN/GaN HFETs. They are triode operation, saturated operation and pinchoff operation.

The device is in pinchoff operation when the device is "pinched off". This happens when the gate-source voltage (Vg) drops below the pinchoff voltage (Vpo), which is defined in 2.2.2.1. From the DC IV characteristics, only a very small amount of drain current can be observed, mostly due to a variety of current leakage instead of normal current transportation in the channel. In this model, we assume an abrupt approximation where the drain-source transport current is zero when the device is in pinchoff mode since there is no leakage current considered at this time. In pinchoff operation, no zone is analyzed because there is no drain current in channel and the capacitance is also very small. We will discuss pinchoff operation in detail in 2.4

The device works in triode operation when Vg is above Vpo and the drain-source voltage (Vd) is smaller than a threshold value. This threshold value is a function of Vg. In this regime, drain current increases rapidly with increasing Vd and a fixed Vg. In the triode operation mode, the AlGaN/GaN HFET is divided into three zones. They are the Source Neutral Zone (SNZ) which occupies the source access region, the Drain Neutral Zone (DNZ)

which occupies the drain access region, and the Intrinsic FET Zone (IFZ) located beneath the entire area of the gate electrode. Fig 2.1 shows the zone division in an ATLAS simulation of an AlGaN/GaN HFET under triode operation over the electron density contour.. Triode operation is discussed in detail in 2.2.

Saturated operation is in effect when Vg is above Vpo and Vd is larger than the threshold voltage which defines the boundary between triode operation and saturation operation. When the device operates in saturation, drain current keeps increasing with increasing Vd and a fixed Vg. However, the increase of drain current is much slower than that in triode operation. Fig 2.2 shows triode and saturation operation regimes in DC IV characteristics. In saturation operation mode, the AlGaN/GaN HFET is divided into five zones. They are the Source Neutral Zone (SNZ) which occupies source access region, the Intrinsic FET Zone (IFZ) is located beneath part of area beneath the gate electrode at source side, the Space-charge Limited Zone (SLZ) which occupies the rest of the area beneath the gate electrode at drain side, the Charge Deficit Zone (CDZ) which occupies part of drain access region at the drain-side gate edge and the Drain Neutral Zone (DNZ) which occupies the rest of drain access region. Fig 2.3 shows the zone division in an ATLAS simulation of an AlGaN/GaN HFET under saturation operation over the electron density contour. Saturated operation is further discussed in 2.3.

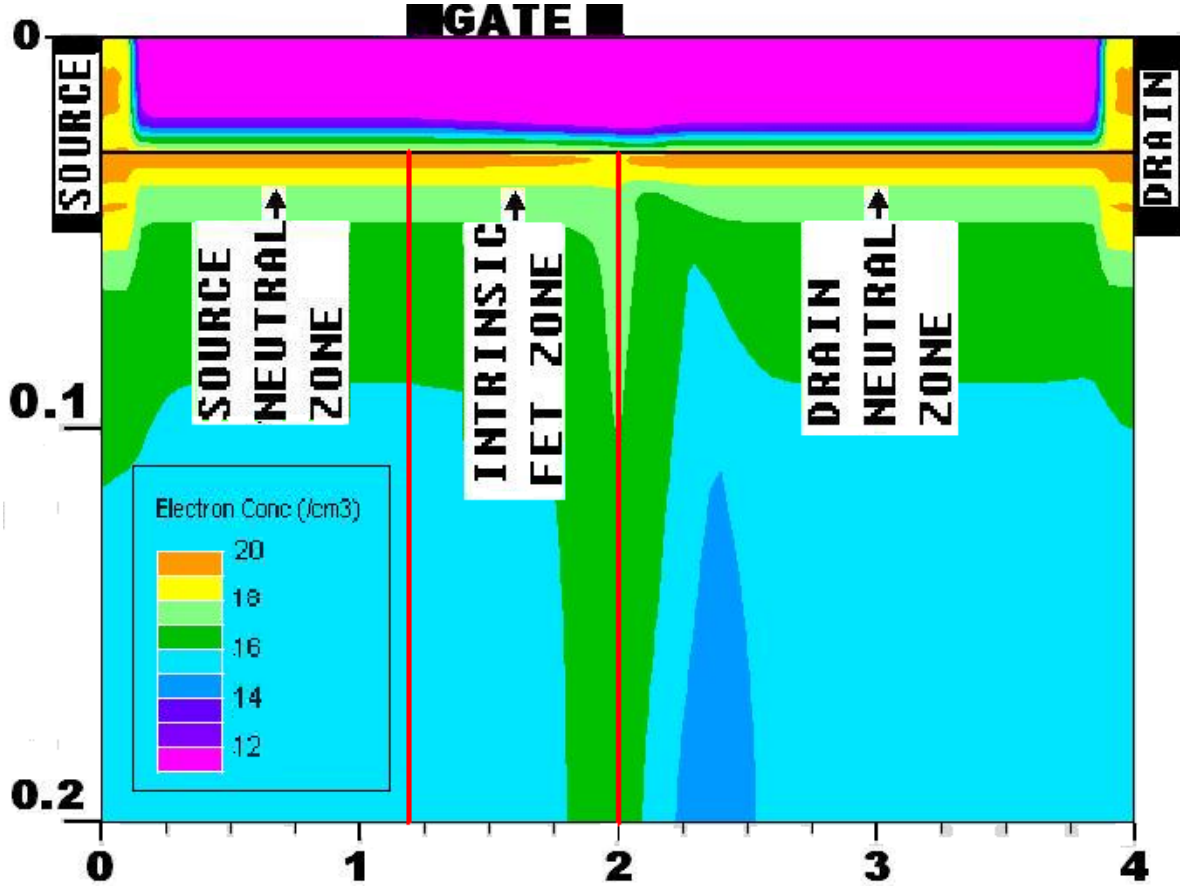

Fig. 2.1. Three zones illustrated over ATLAS simulated electron density contour of an AlGaN/GaN HFET working under triode operation (Both X and Y axes are in units of microns).

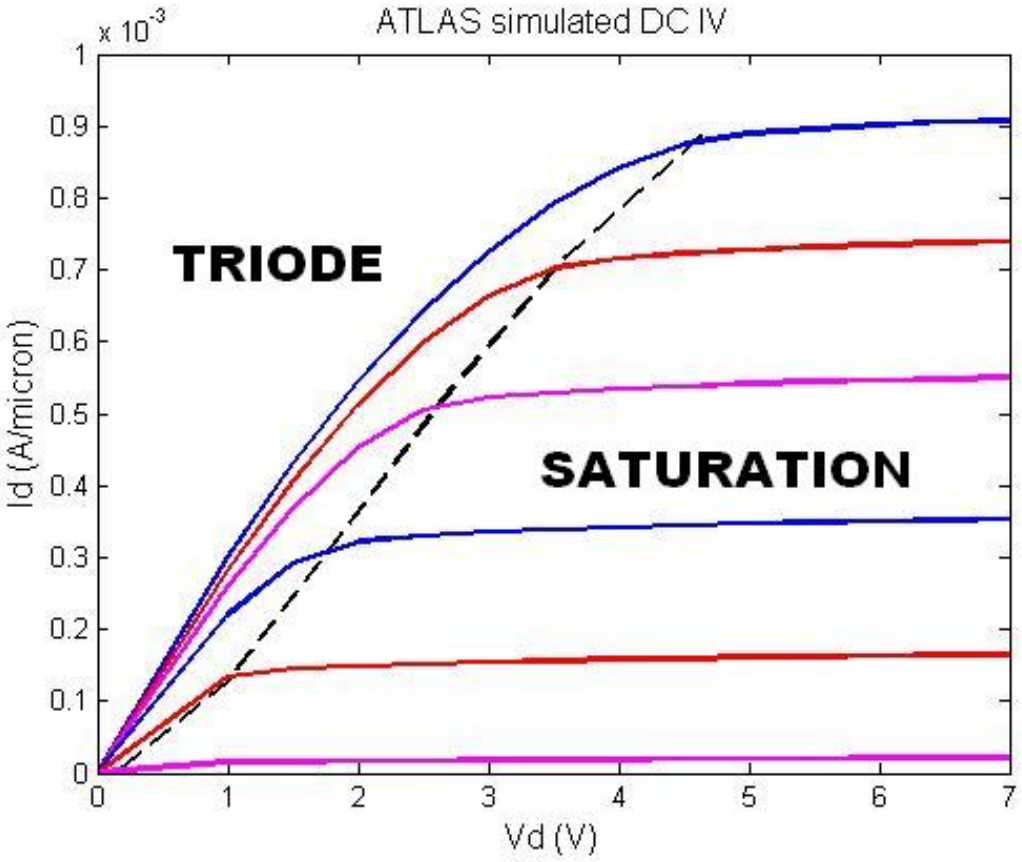

Fig. 2.2 Triode and saturation operation modes over DC IV characteristics of an AlGaN/GaN HFET

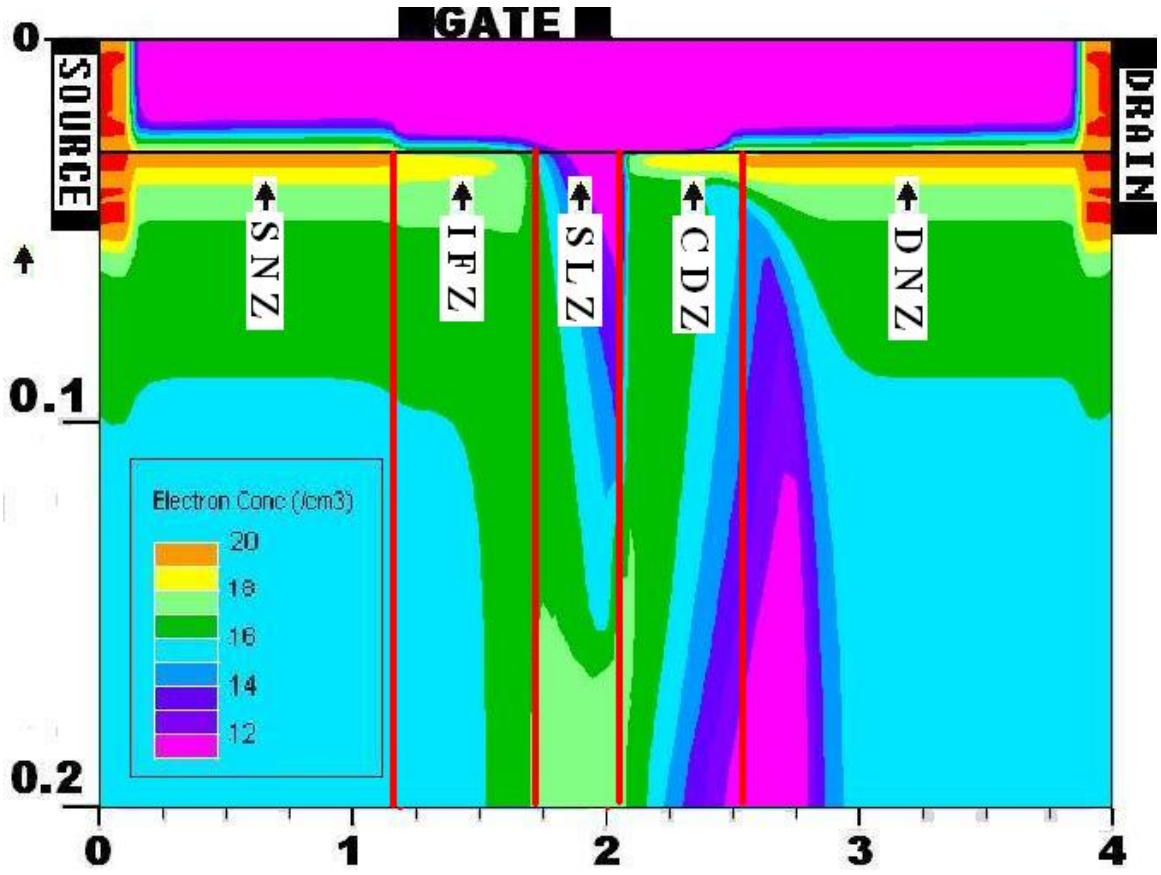

Fig. 2.3 Five zones illustrated over ATLAS simulated electron density contour of an AlGaN/GaN HFET working under saturation operation (Both X and Y axes are in units of microns).

2.2 Device under triode operation

As mentioned in 2.1.1, the device works under triode operation when Vgs is greater than Vpo, which is defined in 2.2.2.1. At the same time, Vds is less than a certain value which depends on Vgs. At this time, three zones: SNZ, IFZ and DNZ are present in the device. The SNZ and DNZ are described in details in 2.2.1, and IFZ is further explained in 2.2.2. During device operation, electrons are traveling at a constant velocity in the SNZ, accelerating while traveling in the IFZ, and traveling again at a constant velocity in the DNZ. However, electron velocity remains well below saturation velocity throughout the channel. The reason is that the lateral electric field (Ex) stays at a relative low level throughout the channel. Fig. 2.4 shows ATLAS simulated n and Ex at a cutline along the middle of the channel 1.5nm beneath the AlGaN/GaN interface in GaN, from source to drain. We can see that Ex is relatively low compared to Fig. 2.5, which shows the same characteristic in saturation operation. In Fig.2.4, we can clearly distinguish all three zones with completely different n and Ex, which implies the different physical nature in these three zones.

2.2.1 Source and drain neutral zones

From Fig 2.1 and Fig 2.3, we observe that in the SNZ and the DNZ, electron density is at its maximum value through the whole channel. Meanwhile, cutlines in Fig 2.4 and Fig 2.5 support this conclusion. Fig 2.6 shows n, Ex and Ey amid the SNZ in the Y direction, which

is perpendicular to the AlGaN/GaN interface. The profiles are from the AlGaN/GaN interface to the bottom of the device. It is obvious that n indicates the electron wavefunction profile with the peak about 1.5nm beneath AlGaN/GaN interface, which is in the middle of the channel. Ey starts from a very high value at the AlGaN/GaN interface because of the positive polarization charge at the AlGaN side of the interface. While moving towards the bottom of the device, Ey decreases sharply due to the screening effect caused by high electron density in the channel. Profiles of n and Ey is in accordance with the fact that a quantum well is at GaN side of AlGaN/GaN interface due to the band discontinuity of the AlGaN/GaN heterojunction. On the other hand, Fig 2.7 and Fig 2.8 show the conduction band diagram at two arbitrary points in source access region, which is SNZ. These two conduction band diagram confirm that the quantum well in SNZ is in its normal state as there is no metal electrode to pin the Fermi level at the upper surface of AlGaN. Moreover, the flat conduction band deep in bulk GaN proves our guess on the existence of a neutral GaN layer beneath the channel. Besides, the band diagram in Fig 2.7 and Fig 2.8 are found to be almost identical except for a potential shift. This confirms our assumption that the band diagram keeps its shape in the vertical cross section perpendicular to the AlGaN/GaN interface. The unchanged band diagram implies the functions of Ex, Ey and n are independence of lateral position x, which is exactly what we assume in model of SNZ. Meanwhile, Fig 2.9 and Fig 2.10 show the conduction band diagram at two arbitrary points in drain access region, which is DNZ when the device is in triode operation. These two band diagram, together with Fig 2.4 and Fig 2.5, implies that DNZ has the same features as SNZ has.

We notice that the integral of the n profile in Fig 2.6 gives a number approximately equal to, the positive sheet charge density, $n_{ss.}$ This reveals that the quantum well is fully filled and charge in this vertical cross section satisfies electrical neutrality. Similar tests are executed at various locations in the SNZ. The electrical neutrality conclusion is found in effect throughout the whole SNZ. Moreover, it is obvious that the profile of n in Fig 2.6 implies that the bulk GaN is almost neutral right beneath the quantum well. The charge contribution from this neutral layer is actually negligible due to the fact that the GaN substrate has a very low doping level of 10^{15} cm^{-3}. In contrast to n_{ss}, which is $7*10^{12}$ cm^{-2}, the contribution from GaN bulk doping is only a quarter percent, which is estimated by

$$\frac{\int_{GaN\ \ thickness} n_{GaN}\,dy}{n_{ss}} = \frac{10^{15}\times(0.2-0.0297)\times10^{-4}}{7\times10^{12}} \approx 0.25\%$$

On the other hand, we can easily estimate the same from Fig 2.6 since the axis for n is in a logarithmic scale.

The current is the product of transportation charge and carrier velocity. Considering the continuity of current throughout the channel, the large amount of electrons in the SNZ quantum well implies a relatively small electron velocity in the SNZ. This statement is proven by ATLAS simulation in which we observe that the velocity in the SNZ is relatively low.

As the boundary of the SNZ near the gate, nearly all electrons are confined in the quantum well at the AlGaN/GaN interface by the positive polarization sheet charge, which forms the 2DEG. Because the large amount of electrons in 2DEG screens the positive sheet charge, the bulk GaN beneath the quantum well is almost neutral and has a trivial contribution to charge transport. As a result, the 2DEG has an amount of electric charge approximately equal to the positive polarization charge; otherwise, no neutral GaN layer would exist.

This analysis applies on DNZ as well since same phenomena are observed in DNZ. As a result, the above conclusions for the SNZ apply also to the DNZ, and hence the model for the DNZ as well, which is introduced in the next chapter.

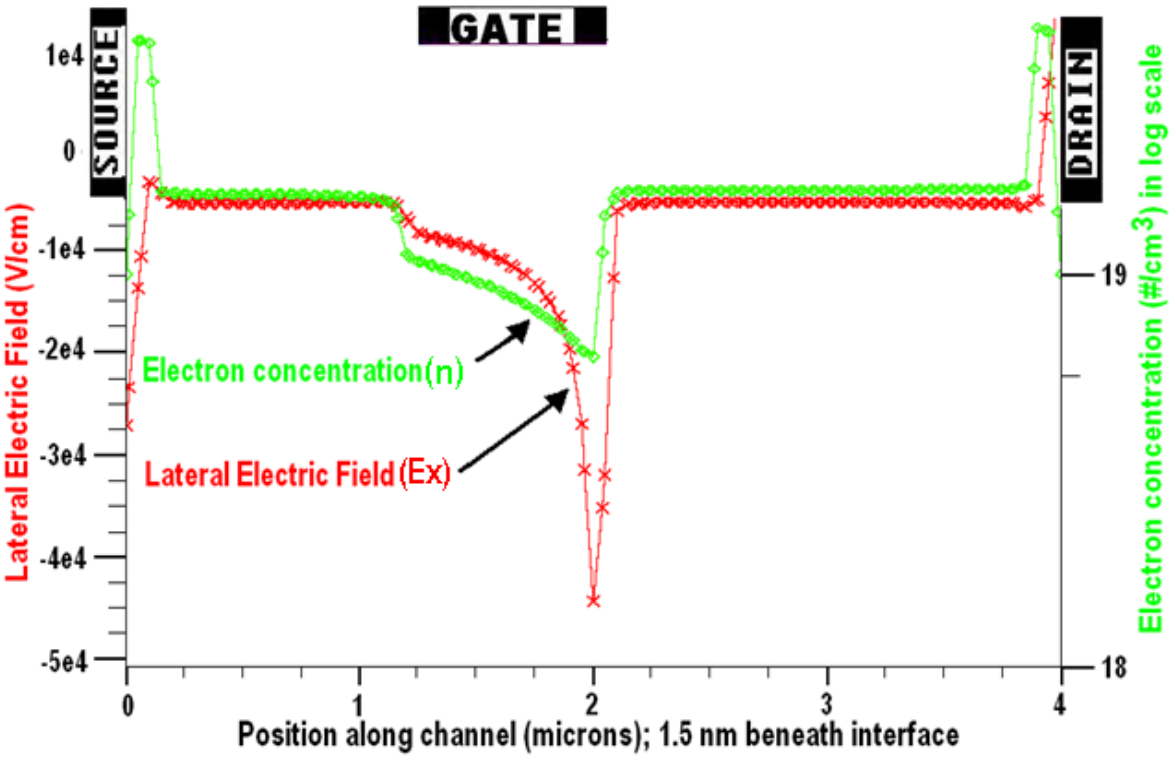

Fig. 2.4 n and Ex along the AlGaN/GaN interface 1.5nm beneath the AlGaN/GaN interface in an AlGaN/GaN HFET under triode operation (X axes in units of microns)

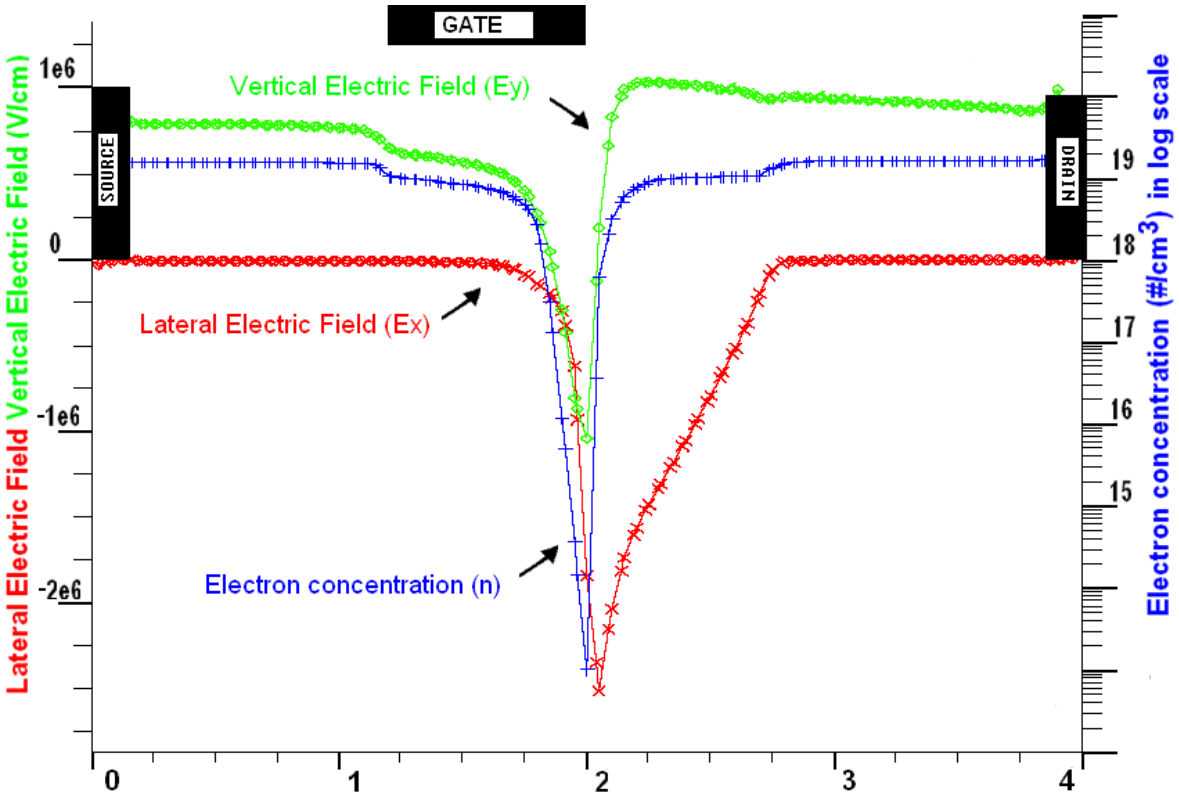

Fig. 2.5 n, Ex and Ey along the AlGaN/GaN interface 1.5nm beneath the AlGaN/GaN interface in an AlGaN/GaN HFET under saturation operation (X axes in units of microns)

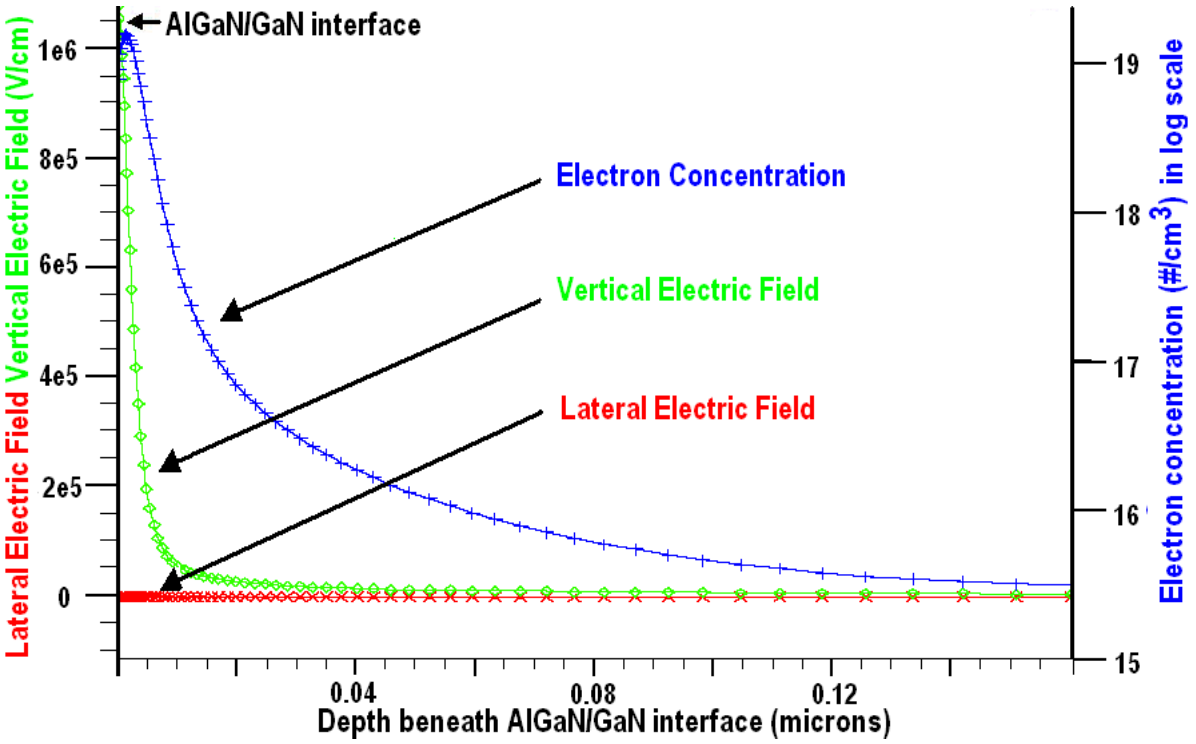

Fig. 2.6 n, Ex and Ey in the vertical cross section in the middle of SNZ (X axes in units of microns)

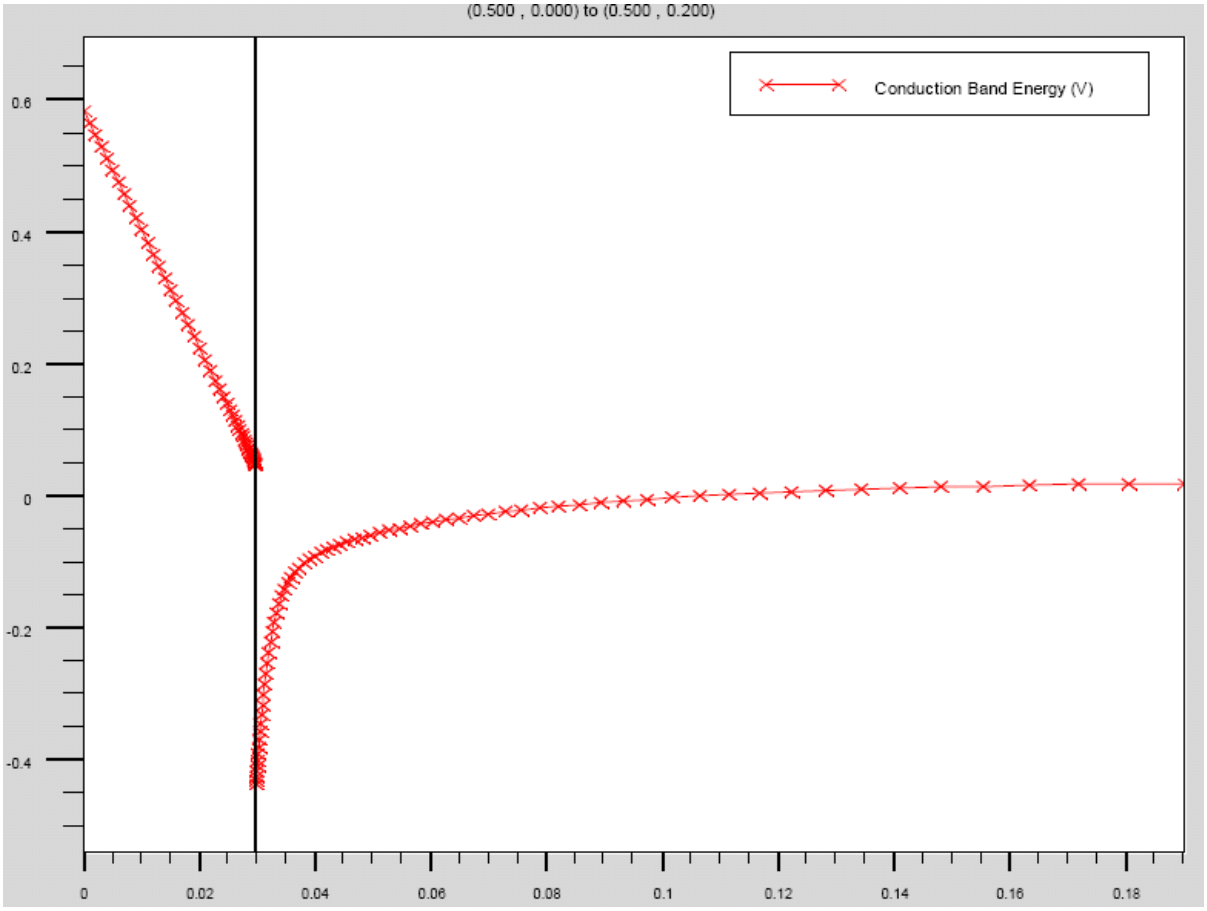

Fig 2.7 ATLAS simulated conduction band diagram. The vertical cutline is made arbitrarily between the source electrode and the middle of source access region, but closer to the source electrode than the cutline of Fig 2.8. The vertical cutline starts from AlGaN's upper surface and ends at the bottom of this device. The bold line is the AlGaN/GaN interface. All units are in microns.

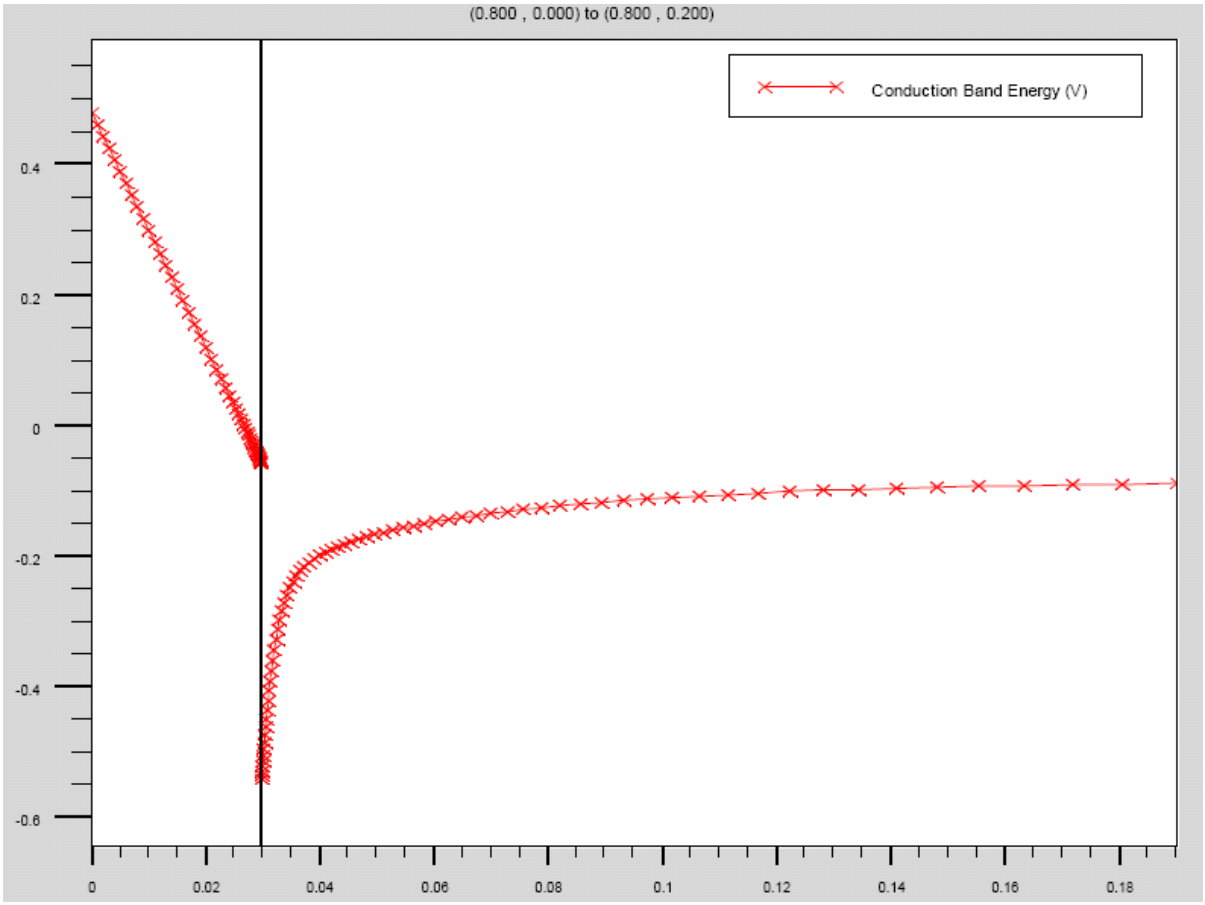

Fig 2.8 ATLAS simulated conduction band diagram. The vertical cutline is made arbitrarily between the middle of source access region and source-side gate edge, but closer to the gate electrode than the cutline of Fig 2.7. This vertical cutline starts from AlGaN's upper surface and ends at the bottom of this device. The bold line is the AlGaN/GaN interface. All units are in microns.

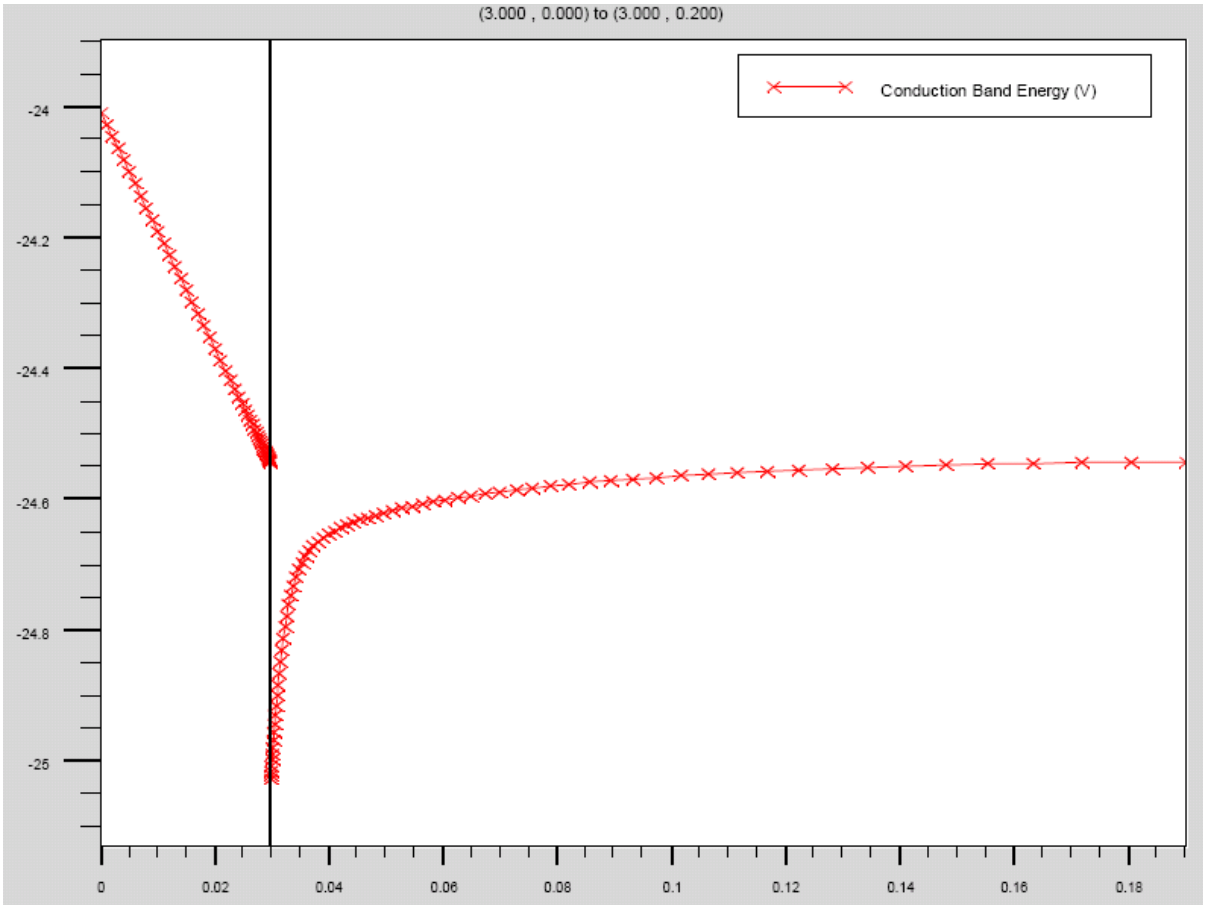

Fig 2.9 ATLAS simulated Conduction band diagram. The vertical cutline is made in the middle of drain access region, but closer to the gate electrode than the cutline of Fig 2.10. The vertical cutline starts from AlGaN's upper surface and ends at the bottom of this device. The bold line is the AlGaN/GaN interface. All units are in microns.

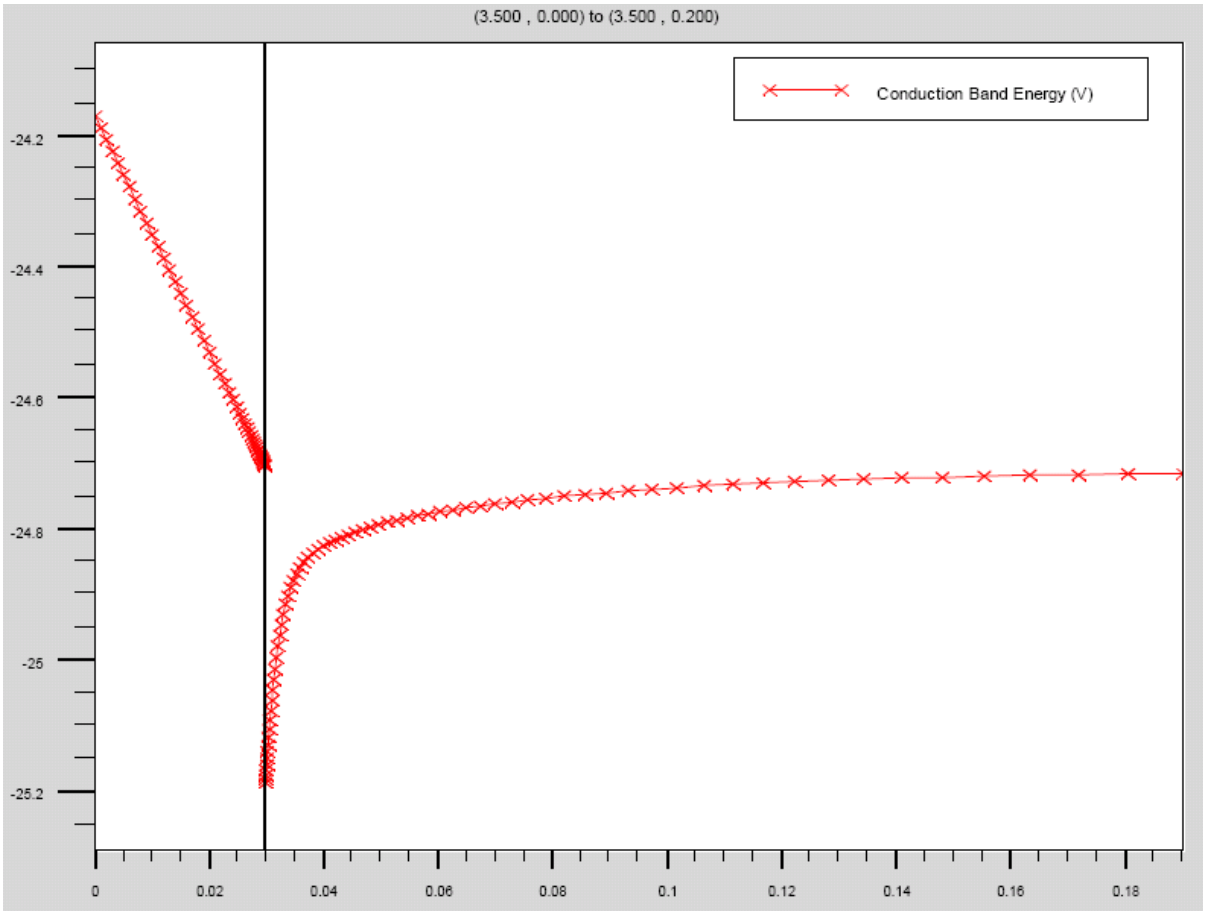

Fig 2.10 ATLAS simulated Conduction band diagram. The vertical cutline is made in the drain access region's length from drain-side gate edge, about three-quarters of the distance to the drain electrode. The vertical cutline starts from AlGaN's upper surface and ends at the bottom of this device. The bold line is the AlGaN/GaN interface. All units are in microns.

2.2.2 Intrinsic FET Zone

As introduced in 2.1, the IFZ is the zone beneath the entire gate electrode of a HFET under triode operation. In this zone, the quantum well is modulated by the gate voltage together with drain voltage. At the source-side gate edge, low voltage leads to more electrons in the quantum well. At the drain-side gate edge, high voltage leads to fewer electrons in the quantum well. We confirm these phenomena in Fig 2.1, which clearly shows the difference in channel electron concentrations beneath the two edges of gate electrode. To maintain current continuity, electron velocity increases as approaching the drain-side gate edge. In this model, the gradual channel approximation is assumed in this zone. Fig 2.11 shows the conduction band diagram of IFZ in vertical direction, which is perpendicular to the AlGaN/GaN interface. In Fig. 2.11, we can see that the bulk GaN beneath the channel is neutral as it is in the access regions shown in Fig 2.7 through 2.10. However, the quantum well, which works as the channel, is reduced due to the Metal-Insulator-Semiconductor structure. The gate electrode pins the potential at Vg and depletes the AlGaN by a higher Ey. This partially compensates the polarization charge at the AlGaN/GaN interface, and hence distorts the conduction band of GaN less, leaving us a more shallow quantum well. In the case that the device enters saturation operation mode, this quantum well finally vanishes and the conduction band diagram reaches a “flat-band” scenario, which is shown in Fig 2.12. This scenario is very important in determining pinchoff voltage, which we will discuss in detail below.

Under triode operation, the low drain voltage does not form a very high electric field. As a result, electrons will not accelerate enough to approach their saturation velocity. This is evident in Fig 2.4, which shows that $|E_x|$ under the gate is an order of magnitude less than the critical electric field $E_c = v_{sat}/\mu$, where v_{sat} is electron saturation velocity and μ is electron mobility. When the lateral electric field does reach E_c, the device enters saturation operation, which is further analyzed in 2.2.2.2.

2.2.2.1 Determination on Pinchoff Voltage

In this model, a pinchoff voltage (Vpo) is predefined from a variety of fabrication and material property parameters. This definition is based on a band diagram when a "flat-band" condition exists. The "flat-band" band diagram happens when the gate voltage equals the pinchoff voltage. In this case, Fermi-level alignment straightens the conduction band in the GaN, from which the word "flat-band" comes. In other words, the quantum well at the AlGaN/GaN interface vanishes at this time. The bulk GaN beneath the gate electrode is neutral and ready to deplete when the gate voltage drops more. Fig 2.12 shows an ATLAS simulated "flat-band" band diagram. This is also used in the definition of pinchoff voltage in a GaAs HFET [4]. The definition of pinchoff voltage can be expressed as

$$V_{po} = \phi_m - \chi_s - \frac{q \times (n_{ss} + n_{po}) \times d_{AlGaN}}{\varepsilon_{AlGaN}} + \frac{kT}{q} \ln\left(\frac{N_c}{n_i}\right) - \frac{q \times N_{AlGaN} \times d_{AlGaN}^2}{2\varepsilon_{AlGaN}} \qquad (2.1)$$

Where Φ_m is the metal workfunction; χ_s is the affinity of AlGaN; n_{ss} is the electron sheet charge density; n_{po} is the polarization charge density; d_{AlGaN} is the thickness of AlGaN layer;

ε_{AlGaN} is the permittivity of AlGaN; N_c is the conduction band state density of AlGaN; n_i is the intrinsic electron concentration of AlGaN; and N_{AlGaN} is the doping level of AlGaN layer. The first term is the difference in gate-metal and GaN work functions. The second term corresponds to the simple capacitor voltage induced by the AlGaN/GaN interface sheet charge and the piezoelectric charge. The last two terms represent the Fermi level offset and the electrostatic voltage resulting from the ionized dopants in the depleted AlGaN layer.

Verification of the terms in Equation 2.1 are obtained from several ATLAS simulations. The curves shown in Fig 2.13 plots our ATLAS simulated drain currents against gate voltages at several fixed drain voltages as indicated. The intercept with the horizontal axis implies a pinch-off voltage that is evidently consistent with the prediction from Equation (2.1). In addition to Fig 2.13, we simulated other device designs to validate particular terms of Equation (2.1). Fig 2.14 compares pinch-offs for the HFET of Fig 2.13 with three other devices obtained by changing one quantity in Equation (2.1) at a time. The drain voltage is fixed at 1V for all four device designs. The blue curve (with diamonds) is for an AlGaN/GaN HFET with the original design shown in Fig 2.1. The magenta curve (with squares) is for a device with a half-volt offset in the work function of gate electrode: it shows that the intercept also moves about half volt as predicted by Equation (2.1). The orange curve (with triangles) is for a device with the AlGaN/GaN interface sheet charge density adjusted to shift the second term in Equation (2.1) by one volt: it shows that the intercept also moves about 1V. The black curve (with crosses) is for a device with the AlGaN layer thickness halved: in

this case, interception point moves to -2.5V, as expected from Equation (2.1). These simulations validate Equation (2.1) and further show that its first two terms dominate the pinch-off voltage, while its last two terms represent corrections that are usually small.

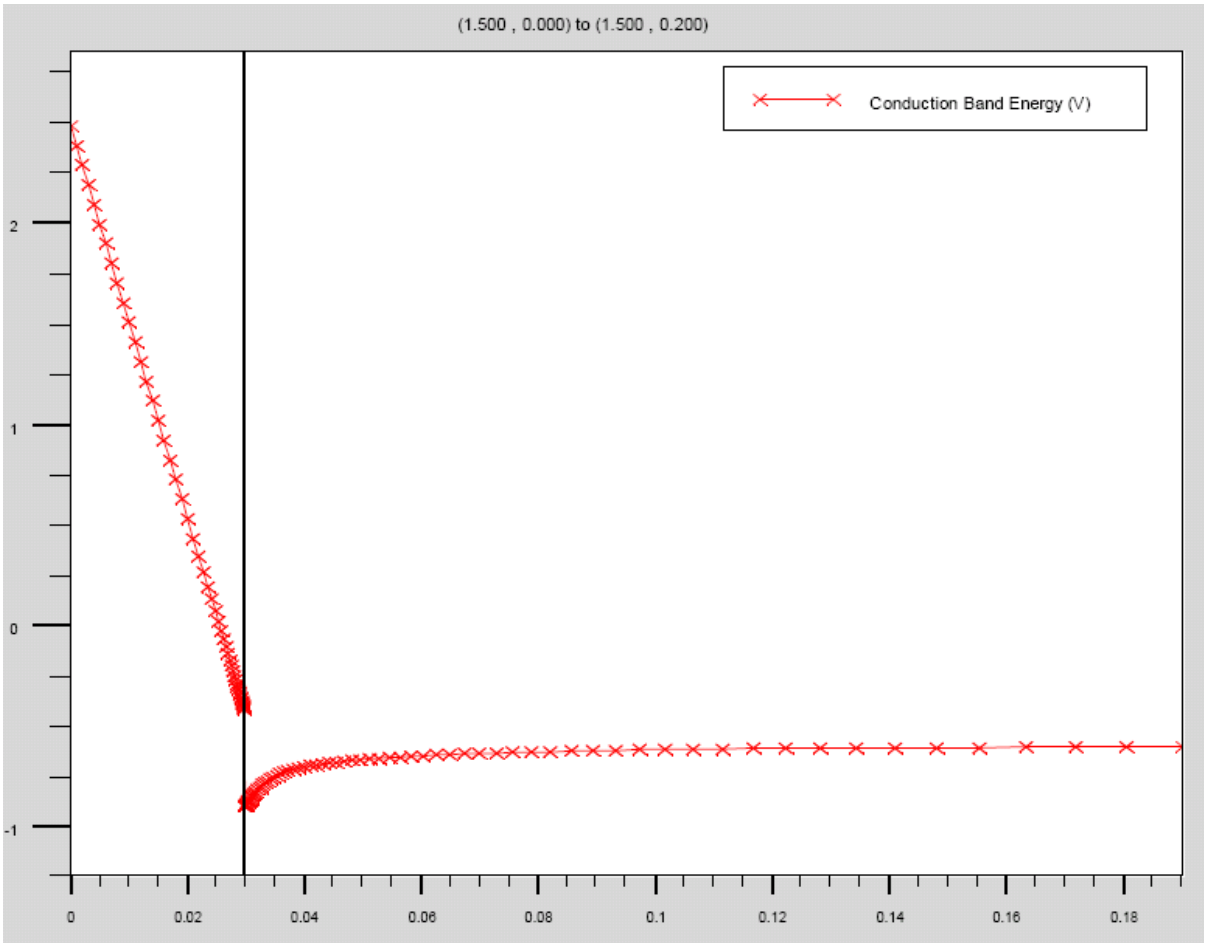

Fig 2.11 ATLAS simulated Conduction band diagram. The cutline is made vertically beneath the gate in IFZ. The vertical cutline starts from the interface between gate electrode and AlGaN, and ends at the bottom of this device. The bold line is the AlGaN/GaN interface. All units are in microns.

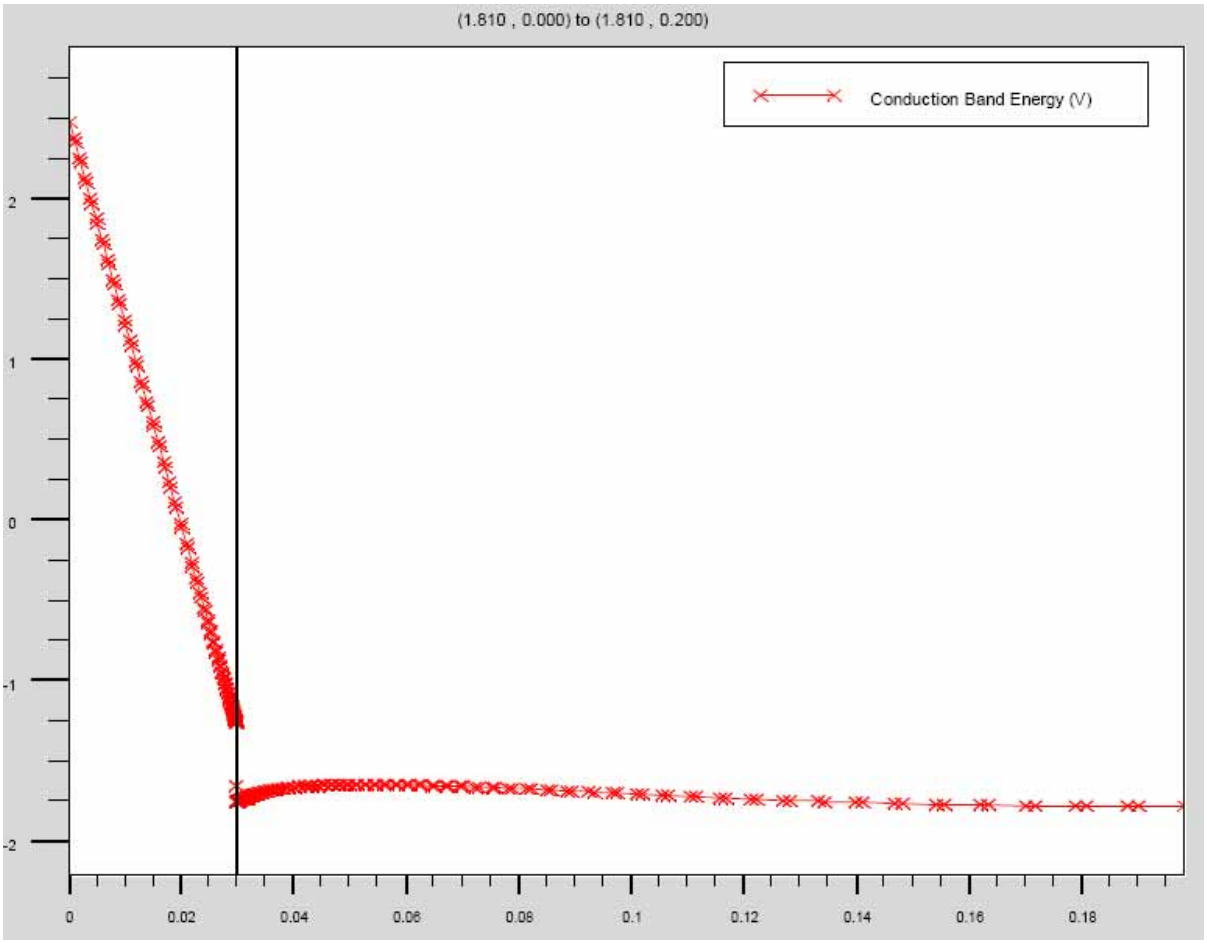

Fig. 2.12 ATLAS simulated “flat-band” band diagram from gate electrode to the bottom of device. The vertical bold line is the AlGaN/GaN interface. All units are in microns.

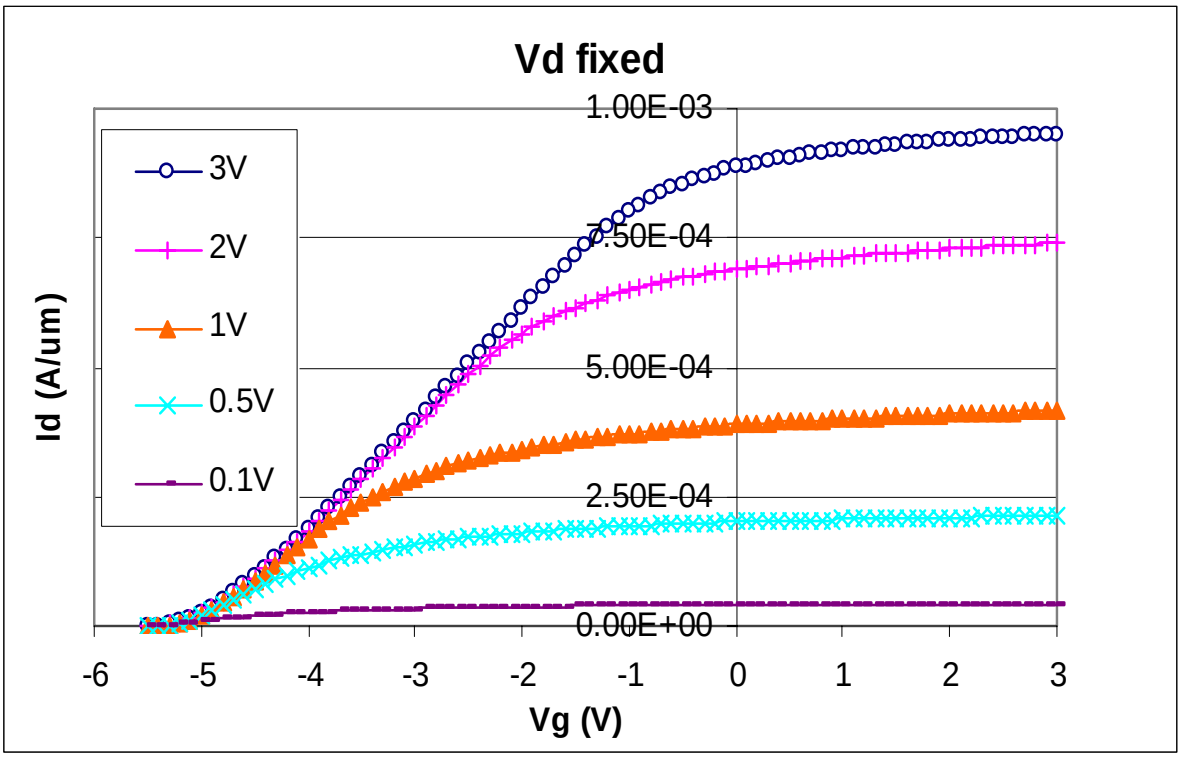

Fig 2.13: Simulated drain current *versus* gate voltage at different fixed drain voltages of an AlGaN/GaN HFET whose structure is shown in Fig 2.1.

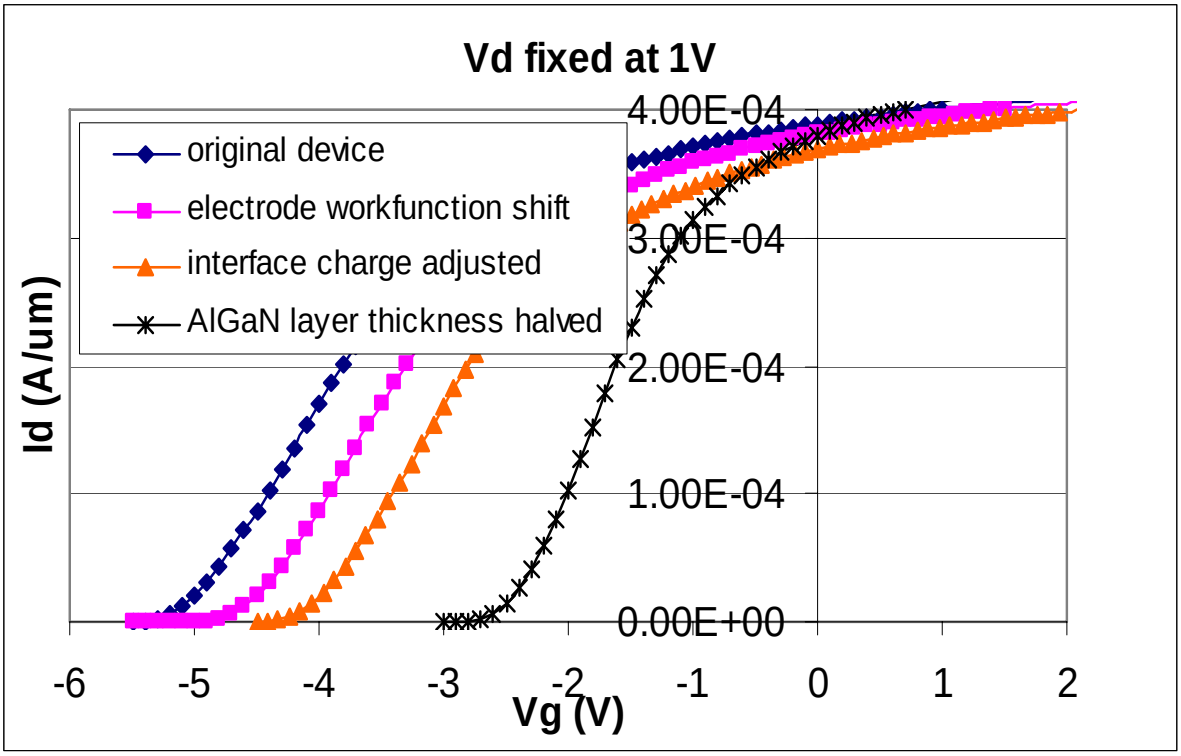

Fig 2.14: Simulated drain current *versus* gate voltage at fixed 1V drain voltage for AlGaN/GaN HFETs with the original design (blue diamonds); with electrodes' work functions shifted by 0.5V (magenta squares); with interface sheet charge density adjusted by $1.937*10^{12}cm^{-2}$ to shift the pinch-off voltage by 1V according to Equation (2.1) (orange triangles); and with AlGaN layer thickness halved to shift the pinch-off voltage to -2.5V (black crosses)

2.3 Device under saturated operation

For a fixed Vg above Vpo, the device starts in triode operation when drain voltage (Vd) starts increasing from zero. However, the device eventually reaches saturation operation when Vd exceeds a certain value. This Vd value increases with increasing Vg. This threshold value is discussed in 2.3.1.

When the device operates in saturation, a depletion region appears surrounding the drain side gate edge. This depletion region can be clearly identified in Fig 2.5. Besides that, Fig 2.15 shows the conduction band diagram of a vertical cross section perpendicular to the AlGaN/GaN interface in CDZ. We found out that the bulk GaN is fully depleted beneath the channel. This is consistent with the existence of a depletion region, which is shown in Fig 2.3. Fig 2.3 and Fig 2.6 also show that there are somewhat fewer electrons in the quantum well in the drain access region near the gate even though the quantum well here is the same size as it is in SNZ and DNZ. This leads to a charge deficit balance by the gradient of Ey, which coincides with the tilted band diagram in Fig 2.15. To emphasize this unique feature, we denote this partially depleted portion of the drain access region as the charge deficit zone or CDZ. In this model, the depletion region is divided into two zones with the gate edge as the boundary. In other words, part of this depletion region is under the gate while the other part is located in the drain access region outside the gate. We name the zone under the gate electrode the space-charge limited zone (SLZ) since space charge limited transport applies in this zone. The details of this zone are discussed in 2.3.2.

The rest of the depletion region is the CDZ and it occupies part of the drain access region. According to our observation, the solution to the 2D Poisson equation in this specific area forms a new zone with unique physics. It is followed by a DNZ that appears the same as it is under triode operation except that its length is reduced. The physical nature of this new Charge Deficit Zone (CDZ) is further analyzed in 2.3.2. The CDZ shares a feature with the SLZ in that they both expand with increasing Vd at a fixed Vg. However, the CDZ expands in the direction toward the drain by squeezing the DNZ in the drain access region. The lengths of IFZ and DNZ are shortened by SLZ and CDZ, but otherwise the physics of SNZ, IFZ and DNZ is the same as it is in a device under triode operation. The Ex, Ey and n profiles in Fig 2.6 keep the same regardless of the mode under which the device is working.

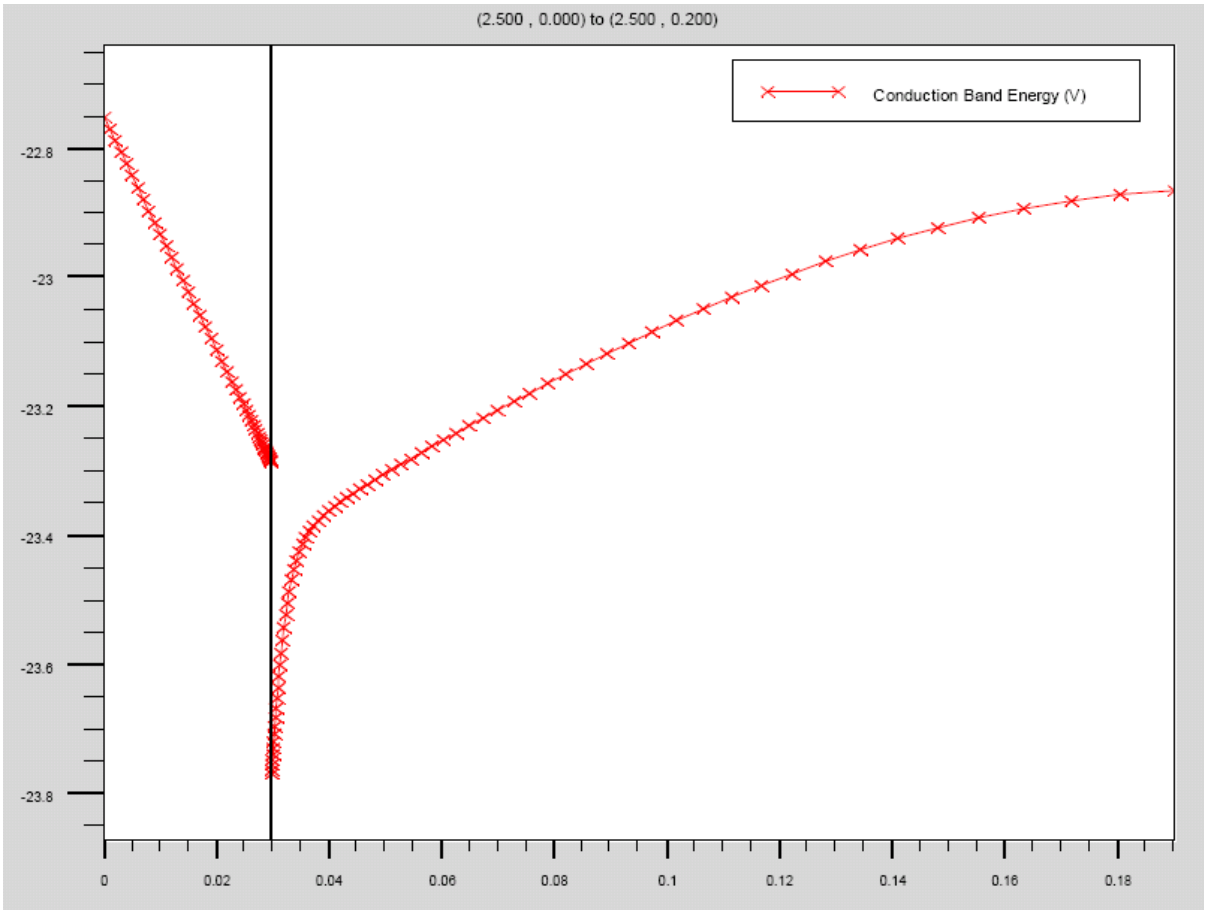

Fig 2.15: ATLAS simulated Conduction band diagram. The cutline is made vertically in CDZ. The vertical cutline starts from the upper surface of AlGaN, and ends at the bottom of this device. The bold line is the AlGaN/GaN interface. The horizontal axis is in microns.

2.3.1 Vd threshold between triode and saturated operations

At a fixed Vg, there is a Vd value when the quantum well first becomes shallower by the flattened conduction band. The initial flattening effect must occur at the drain-side gate edge since this is where the maximum voltage difference between the two sides of AlGaN layer appears, i.e. gate electrode and channel. The reason is that the channel voltage at this point is the highest in the IFZ, and there is no gate electrode pinning the voltage at Vg beyond this point. In fact, this also explains why the depletion region always starts from drain-side gate edge.

If we consider a device still under triode operation, there are only 3 zones and the IFZ occupies the whole area beneath the gate electrode. Assuming a second order velocity-field curve, we have in the IFZ the relationship

$$\frac{I}{\beta} = \int_{V_s'}^{V_d'} \sqrt{\left(V - V_{gt}\right)^2 - \left(\frac{I}{\beta V_l}\right)^2}\, dV$$

Where V_s' and V_d' are channel voltages at the two edges of the IFZ. Expressions for V_s' and V_d' are derived in the next chapter. V_{gt} is the effective gate voltage, which is defined as $V_{gt} = V_g - V_{po}$, and $V_l = E_c \times l_g$. Here l_g is the gate length. Detailed derivation of this expression can be found in chapter 5.

When the threshold drain bias is reached, Vd makes the drain current stop increasing in triode operation, which can be described as $\frac{\partial I}{\partial V_d} = 0$. Therefore, if we take the first order derivative with respect to Vd of the above I-V relationship and apply this condition, we can obtain

$$\left(V_d - V_{gt}\right)^2 - \left(\frac{I}{\beta V_l}\right)^2 = 0$$

We have

$$V_d = V_{gt} - \frac{I}{\beta V_l}$$

The other root

$$V_d = V_{gt} + \frac{I}{\beta V_l}$$

is omitted since this root corresponds to saturated operation instead of triode operation.

The solution $V_d = V_{gt} - \frac{I}{\beta V_l}$ implies that saturation occurs when Ex at the drain-side gate edge equals to Ec. This is the moment when the quantum well starts significantly shrinking. This result is in accord with explanations from other groups [3].

Fig 2.2 shows these threshold Vd values corresponding to a series of Vg's. The value at any fixed Vg is determined by the model program by noting the first decrease in triode drain

current as Vd increases. This condition identifies the change of device operation from triode to saturation, and is de facto equivalent to $\frac{\partial I}{\partial V_d} = 0$ within numeric error tolerance.

2.3.2 Space-Charge Limited Zone

When the device first enters saturation operation, a depletion region starts forming at the drain-side gate edge, where the highest electric field and hence lowest electron concentration occur. As we stated previously in 2.2.2.1, the triode operation ends when Vd makes the peak lateral electric field reach E_c. At this point, electron velocity is in the proximity of its saturation value. Afterwards, the lateral electric field keeps increasing with the increasing Vd. This makes electron velocity even higher. Meanwhile, the rising channel potential flattens the GaN-side conduction band in the AlGaN/GaN heterojunction. As a result, the quantum well becomes shallower which frees electrons from the quantum well's confinement. These electrons "spill out" into the bulk GaN beneath the AlGaN/GaN heterojunction because the AlGaN still works as a barrier in this case. After the band completely straightens out for higher Vd, a barrier, i.e. a depletion region, appears instead of the previous quantum well under triode operation. This barrier can be clearly observed in Fig 2.16, which shows the conduction band diagram of a cross section perpendicular to the AlGaN/GaN interface. At this moment the quantum well completely vanishes and all electrons originally in the quantum well are injected into the bulk GaN, which has a flat conduction band near the bottom of device. Fig 2.16 shows this too. Now, electrons are traveling at a very high speed, very close to the saturation velocity. In this model we assume that electron velocity is equal

to the saturation velocity at this time. Thereafter, the depletion region grows with rising Vd, and electron flow is pushed deeper into the bulk GaN by it. Fig 2.3 shows this detour process of electron flow. Note that when electrons trespass into the bulk GaN, the GaN beneath them remains neutral while not counting these injected charges and its conduction band is flat down to the bottom of the device.

2.3.3 Charge Deficit Zone

Beyond the drain-side gate edge, the bounding effect of gate electrode disappears. Consequently, the band diagram at the AlGaN/GaN interface recovers from the barrier into the normal quantum well. This terminates the detour of the electrons which fall back from the bulk GaN to become confined in the reformed quantum well. Together with the spill-out process in the SLZ, this flow-back process forms a V shaped "detour" in the electrons' path in any device under saturated operation. This phenomenon is confirmed in Fig 2.3, which shows the V shaped detour of electron flow beneath the drain-side gate edge. Meanwhile, n, as well as electron velocity and Ex, need to recover to their values under a normal quantum well state. In Fig 2.5, we can clearly see that Ex is dropping almost linearly in the CDZ and n remains low in CDZ before they both recover in the DNZ, where they resume values resembling the SNZ. These phenomena derive from the solution of the 2D Poisson equation in the CDZ with its own unique boundary condition. Our model on the SLZ and the CDZ are reported in detail in chapter 4.

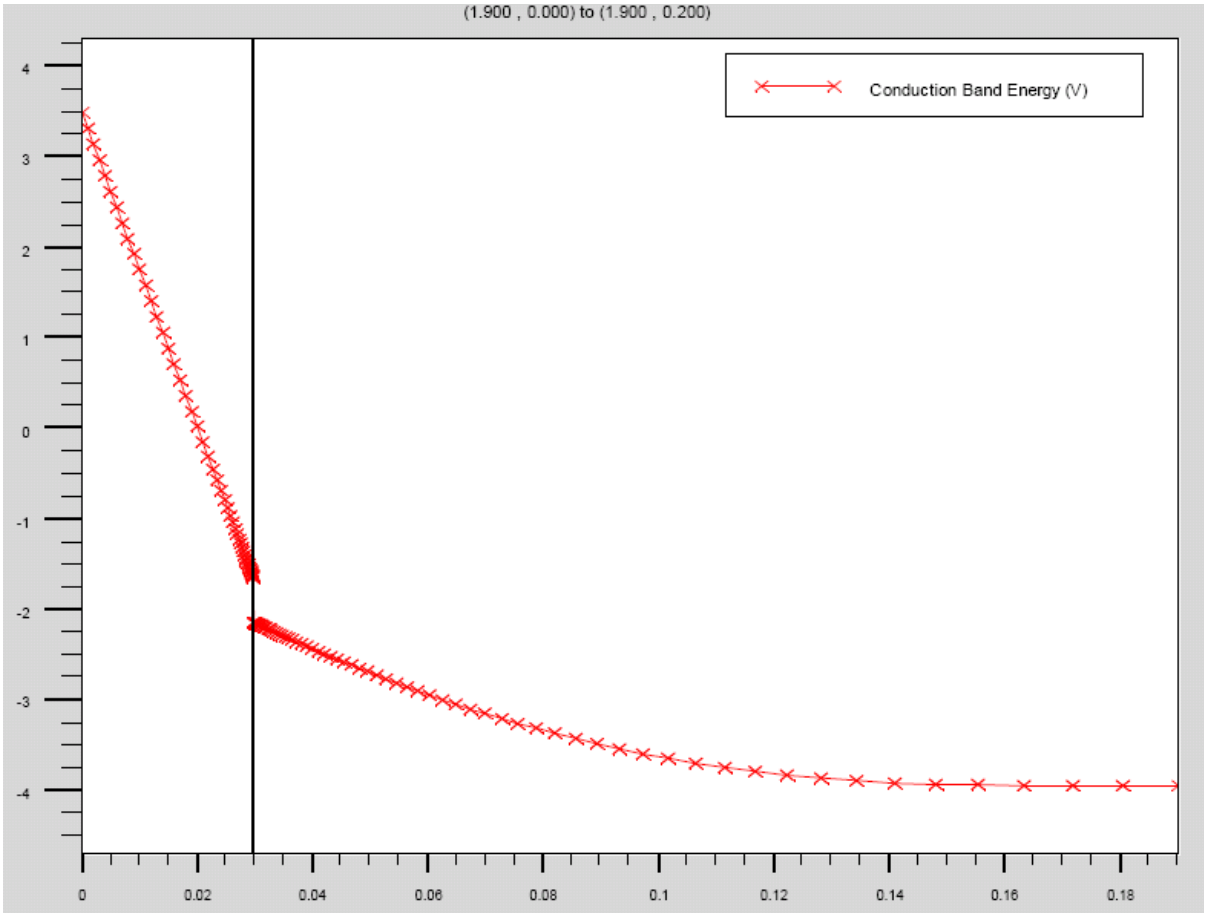

Fig 2.16 ATLAS simulated Conduction band diagram. The cutline is made vertically in SLZ. The vertical cutline starts from the interface between AlGaN and gate electrode, and ends at the bottom of this device. The bold line is the AlGaN/GaN interface. The units of the horizontal axis are microns.

2.4 Device under Pinchoff Operation

When the gate-source voltage equals pinchoff voltage defined in 2.2.2.1, the device reaches pinchoff operation. At this time, the "flat-band" band diagram described in 2.2.2.1,applies for the channel beneath the source-side gate edge. If the drain-source voltage is positive, the voltage increases at a position closer to the drain, while the gate electrode voltage keeps the same everwhere. This depletes the entire channel area beneath the gate electrode. Hence a depletion region instead of a quantum well occupies the whole channel area beneath the gate electrode. If gate-source voltage keeps dropping, then the GaN under the gate depletes more. This expands the depletion region in the intrinsic FET zone. At this time, the device is pinched off more "deeply". Fig.2.3 shows an ATLAS simulated electron density contour of an AlGaN/GaN HFET under pinchoff voltage. Fig. 2.4 shows an ATAS simulated electron density contour of an AlGaN/GaN HFET "deeply" under pinchoff voltage. We can see that the "deeper" pinchoff brings in no new features except an expanded depletion region beneath the gate. This supports our abrupt pinchoff approximation which is mentioned in 2.1.

The abrupt-pinchoff approximation is assumed mainly for sake of simplification. However, we do observe that gate leakage is usually 4 or more magnitudes less than drain current [1] mostly due to the high Schottky barrier between gate electrode metal and AlGaN. The gate leakage may be suppressed more by other improved fabrication techniques too, such as passivation or adding an additional AlN layer as the insulator, which is of great research interest and still under investigation [2] [3]. Meanwhile, the drain leakage through substrate

and below the channel is reduced to a negligible amount because electrons' density in the undoped bulk GaN substrate is much less than that in the 2DEG. The low doping level in the GaN substrate also leads to a low capacitance change when the device is in pinchoff mode. After the device reaches pinchoff mode, the amount of electrons left in GaN substrate is much less than the amount of electrons in the 2DEG sheet charge layer which has already been depleted before pinchoff. Therefore, the contribution from these electrons is trivial in capacitance. In this model, the capacitance is also approximately assumed to be zero for this reason.

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CHAPTER 3

3.1 Nonlinear resistances at Source and Drain

In most circuit models, the source and drain access regions are treated as ideal resistors, which is equivalent to assuming constant mobility for carrier transport, i.e. a linear electron velocity-field relationship. In this model, however, we show that a more realistic treatment of these series resistances automatically predicts the observed bell-shaped dependence of transconductance gm (Vg) on gate-to-source voltage Vg as well as the finite saturation of drain current for large Vg. We argue that this justifies the non-linear series resistor model access regions previously introduced to numerically model large-signal RF data from AlGaN/GaN HFET amplifiers [1].

As explained in the last chapter, space charge in the Source and Drain Neutral Zones is negligible since the quantum wells of the AlGaN/GaN heterojunction are fully filled with electrons and thus channel electrons completely screen the positive sheet charge above the AlGaN/GaN interface. This is shown for the source access region in Fig 2.1, where the electron concentration, lateral and vertical electric fields are plotted along a typical vertical cross section through the source access region. In Fig 2.6, we can see a peak electron concentration as high as $10^{19}cm^{-3}$ in the quantum well at the AlGaN/GaN interface. The lateral electric field Ex is small and varies little with depth. The vertical electric field Ey exceeds 1 MV/cm near the AlGaN positive sheet charge, but drops to zero a few nanometers

below the interface. The electron concentration n also falls to the bulk GaN background doping level, but more slowly. From this, we conclude that the channel completely screens the sheet charge above the interface, that the bulk GaN is nearly neutral, and that the number of electrons in the channel approximately equals the amount of positive sheet charge in AlGaN, which can be proven by simulation data.

In the Drain Neutral zone, similar cross-sectional lines show that the positive sheet charge at the AlGaN/GaN interface is similarly completely screened by the channel electrons, and that the bulk GaN beneath the channel is practically neutral there, too. Above saturation, the drain neutral zone recedes from the gate edge, where a Charge Deficit Zone forms to support most of the drain voltage except near the upper left end point of an amplifier load line [2].

Fig. 2.4 shows the electron concentrations and lateral electric fields in Source and Drain Neutral Zones are almost constant. Therefore, the 2D Poisson equations for the channel in the Source and Drain Neutral Zones can be approximated by 1D Poisson equations in the vertical direction. In other words, in the neutral zones, all the electric field lines sourced by positive charges in the AlGaN layer are vertical and that they all terminate on electrons in the 2DEG. Average electron velocity is uniform, lateral, and lower than the saturation velocity v_{sat}, in accord with the fact the maximum current an HFET can carry is the product of the positive sheet charge density and the electron saturation velocity:

$$I_{sat} = W \times J_{sat} = W \times q \times n_{ss} \times v_{sat} \tag{3.1}$$

Therefore, in both neutral zones, net charge vanishes; lateral electric fields are constant; voltage drops linearly; and the electron velocity

$$v = I/(W \times q \times n_{ss}) \tag{3.2}$$

is proportional to the drain current. A similar relationship was found in AlGaAs/GaAs HFETs [3].

3.2 Model implementation

Based on analysis in the previous section, electron concentration is constant in the neutral zones in the access regions. Therefore, drain current determines electron velocity which, in turn, determines the lateral electric field via the velocity-field curve. In the case of the following "second order" velocity-electric field relation, we have

$$v = \frac{\mu E}{\sqrt{1+(E/E_C)^2}} \tag{3.3}$$

where $E_c = v_{sat}/\mu$, so that

$$E = \frac{E_c}{\sqrt{(I_{sat}/I)^2 - 1}} \tag{3.4}$$

and the resistivity is

$$\rho = \frac{E}{J} = \frac{E_c}{\sqrt{J_{sat}^2 - J^2}} . \tag{3.5}$$

Equation (3.5) implies that the resistivity in each access region is a non-linear function of current. This resistivity changes little when the drain current is less than half of the saturation current, but increases dramatically when the current approaches the saturation current. Near the saturation current, this increasing resistivity eventually determines the maximum drain current that the device allows.

In Fig. 3.1, we compare the resistivity data from the ATLAS simulations with the model result predicted by Equation (3.5). The two curves are very close to each other. This supports the statement we made at the beginning of this chapter that the resistivity in this neutral source access region is effectively determined by the velocity-field curve and the current flowing through this region. The nonlinearity of the resistivity derives directly from the nonlinearity of the velocity-field curve. As for a general form of a p^{th} order velocity-field curve

$$v = \frac{\mu E}{\sqrt[p]{1+\left(E/E_C\right)^p}} \tag{3.6}$$

which now implies

$$E = \frac{E_c}{\sqrt[p]{\left(I_{sat}/I\right)^p - 1}} \tag{3.7}$$

so that the resistivity becomes

$$\rho = \frac{E}{J} = \frac{E_c}{\sqrt[p]{J_{sat}^{\,p} - J^p}} \tag{3.8}$$

For any positive p, the resistivity increases slowly when the drain current is low, but it increases sharply and reaches a high value when the drain current approaches the saturation current, which implies the saturation current is the upper limit set by the FET's design and can not be exceeded.

Similar tests of the model against simulations were conducted for the resistivity of the drain access region with similar results: The drain access region's resistivity is also nonlinear and it obeys the same model. Therefore, both neutral zones in these access regions have non-linear resistivity described by Equation (3.5) or Equation (3.8). The effect of these non-linear resistances on DC IV curves will be discussed at the end of the next section.

In GaAs devices, the resistance in access regions is usually considered as distributed resistance since a parallel conduction exists in the partially undepleted AlGaAs layer [4]. However, in AlGaN/GaN HFETs, the large piezoelectric field in AlGaN sweeps electrons into the 2DEG channel, and hence depletes the AlGaN layer. As the result, almost all electrons are gathering in the 2DEG channel, which is proven by Fig 2.3.

Space-charge limiting [5] and partial channel depletion by charges in the upper surface [6] can also increase the resistivity of the access regions, but the effect of the velocity-field curve on resistivity appears to dominate at low frequency.

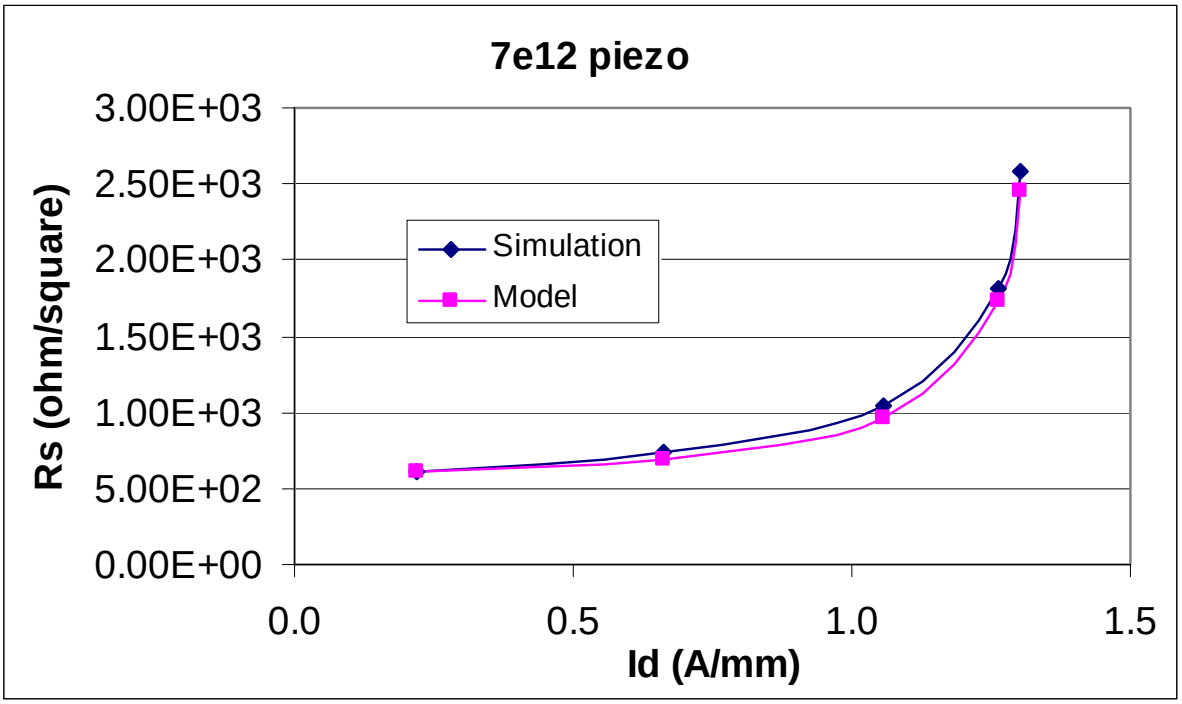

Fig 3.1. Modeled (magenta squares) and simulated (blue diamonds) Resistivity versus drain current density per mm in width of an AlGaN/GaN HFET whose structure is shown in Fig 2.1.

3.3 Model verification

It is interesting that equation (3.5) predicts that the resistivity is independent of drain and gate voltage variations that preserve the drain current. To test this, several practices are designed to extract resistivity in the SNZ and the DNZ with the drain current kept fixed but other parameters changing. The parameters involved in this verification are drain and gate bias, which is discussed in 3.3.1, gate-source spacing, in 3.3.2 and gate-drain spacing in 3.3.3. After these verification efforts, we conclude that resistivity is independent of all three in the SNZ and the DNZ.

3.3.1 Effect of operating points

In Fig 3.2, we compared the simulated resistivity at different operating points based on ATLAS simulation results of another HFET with a similar structure. The blue curve (with squares) spans operating points with the same drain voltage of 10V, but with gate voltages ranging, left to right, from near pinch-off to near open-channel. In other words, the trace of this curve corresponds to a vertical line at a 10V drain bias in the I-V plane of the usual plot of device characteristics. The other three curves (with triangles) consist of operating points with various drain voltages but with gate voltages fixed at -3V, -1V, and 1V. The traces of these three curves (with triangles) are the knee-like IV curves at fixed gate bias in the device's usual IV characteristic plot. The agreement between all four of these curves in Fig 3.2 shows that the non-linear resistivity is accurately modeled as a function of current only.

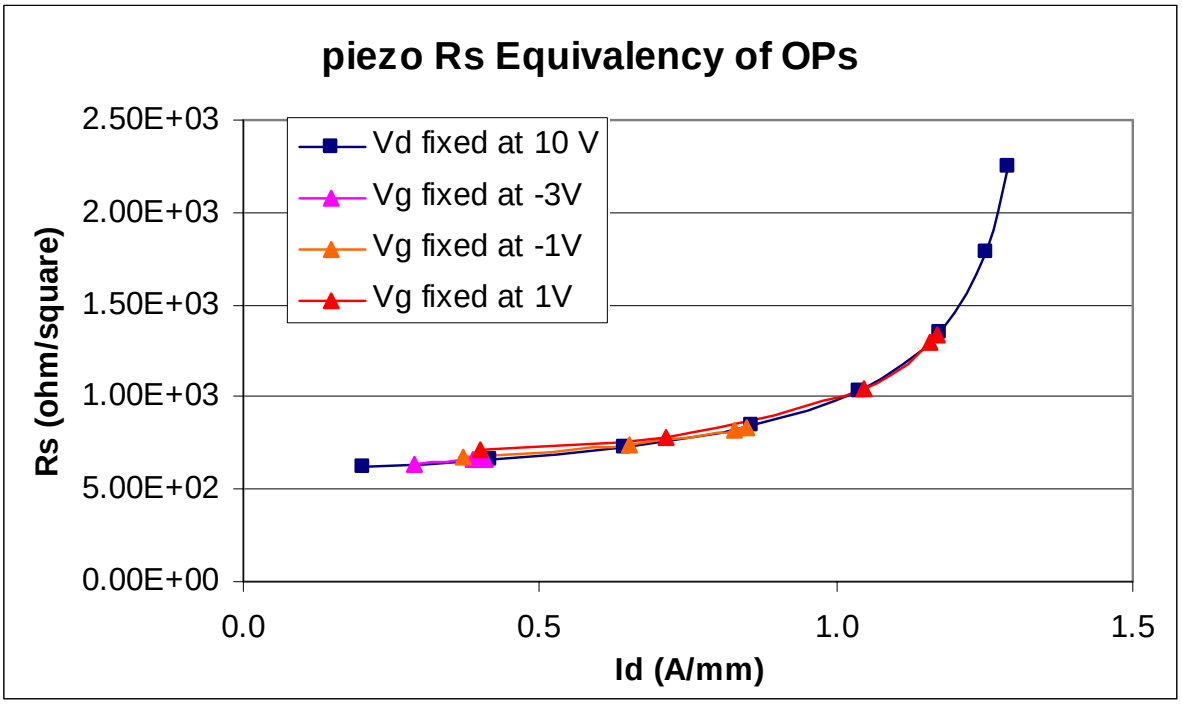

Fig 3.2: Resistivity versus drain current density of various operation points. The blue trace with squares connects the set of operating points with various gate voltages but a drain voltage fixed at 10V. The other three traces with magenta, orange and red triangles are operating points with various drain voltages but with gate voltages fixed at -3V, -1V and 1V, respectively. Data are from ATLAS

3.3.2 Effect of Gate-Source Spacing

Furthermore, other simulations indicate that the resistivity is independent of the length of the access regions, as shown in Fig 3.3. In Fig 3.3, resistivity is simulated for a set of device designs with the same vertical structure but with source access regions of different lengths. The 4-micron-long device shown in Fig 2.1 has a 1.2 micron long source access region. The source access regions of the other two devices are 1 and 2 microns longer, but all other fabrication parameters were kept the same, making the total lengths of those devices 5 and 6 microns respectively. Fig 3.3 shows that the resistivity curves of all three devices coincide regardless of the source access regions' lengths.

Please note that resistivity instead of resistance is the parameter that remains constant. In other words, resistance in the SNZ is proportional to its length. Hence these three devices exhibit different in DC IV characteristics because the voltage dropping across the SNZ is proportional to the SNZ's length.

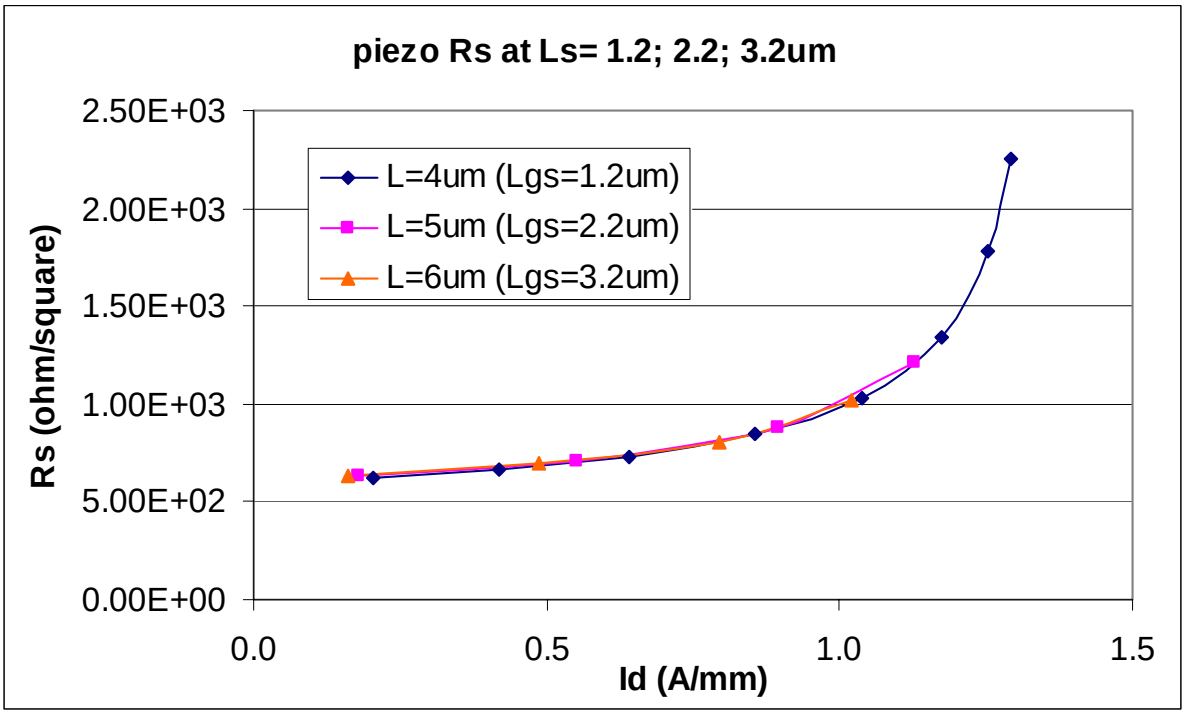

Fig 3.3: Resistivity versus drain current density of a set of AlGaN/GaN HFETs with the same fabrication structure but different lengths of source access region. The curve with blue diamonds is for the 4-micron device whose structure is shown in Fig 2.1. The curve with magenta squares is for a device having one extra micron in the source access region, making the device's total length 5 micron. The curve with orange triangles is for a device with still another micron in the source access region's length, making it 6 microns in total length. Data are from ATLAS simulations.

3.3.3 Effect of Gate-Drain Spacing

The same verification is executed in the DNZ as well, as shown in Fig 3.4. In Fig 3.4, resistivity is simulated for a set of device designs with the same vertical structure but with drain access regions of different lengths. The 4-micron-long device shown in Fig 2.1 has a 2-micron long drain access region. The drain access regions of the other two devices are 1 and 2 microns longer, but all other fabrication parameters were kept the same, making the total lengths of those devices 5 and 6 microns respectively. Fig 3.4 shows that the resistivity curves of all three devices coincide regardless of the source access regions' lengths.

Unlike the SNZ which has a fixed length always equal to the length of source access region, the length of the DNZ varies with the operation mode which the device works under. According to the zone division methodology which was introduced in the last chapter, the length of the DNZ is equal to the length of drain access region when the device works under triode operation. However, when the device works under saturated operation, the length of drain access region is shared by the DNZ and the CDZ. The individual lengths of the DNZ and the CDZ are dependent on gate and drain bias. We will discuss the CDZ's characteristics in another chapter.

In this verification effort, the simulation data shown in Fig 3.4 are acquired in the identified DNZ in each operation case. In all three verifications in 3.3, data are collected from operation points all over the DC IV plane, including those under triode and saturation operation. For

example, the device remains in saturation when Vd is fixed at 10V in Fig 3.2. However, In Fig 3.2's operating points where Vg is fixed, the first several operation points are in triode operation. Electron density contours in Fig 2.1 and Fig 2.3 also show the same electron density in the DNZ and the SNZ. As a conclusion, the operation modes defined in this model do not affect this nonlinear resistance model, although the length of the DNZ should be calculated to determine whether a certain location in the drain access region belongs to the DNZ or not.

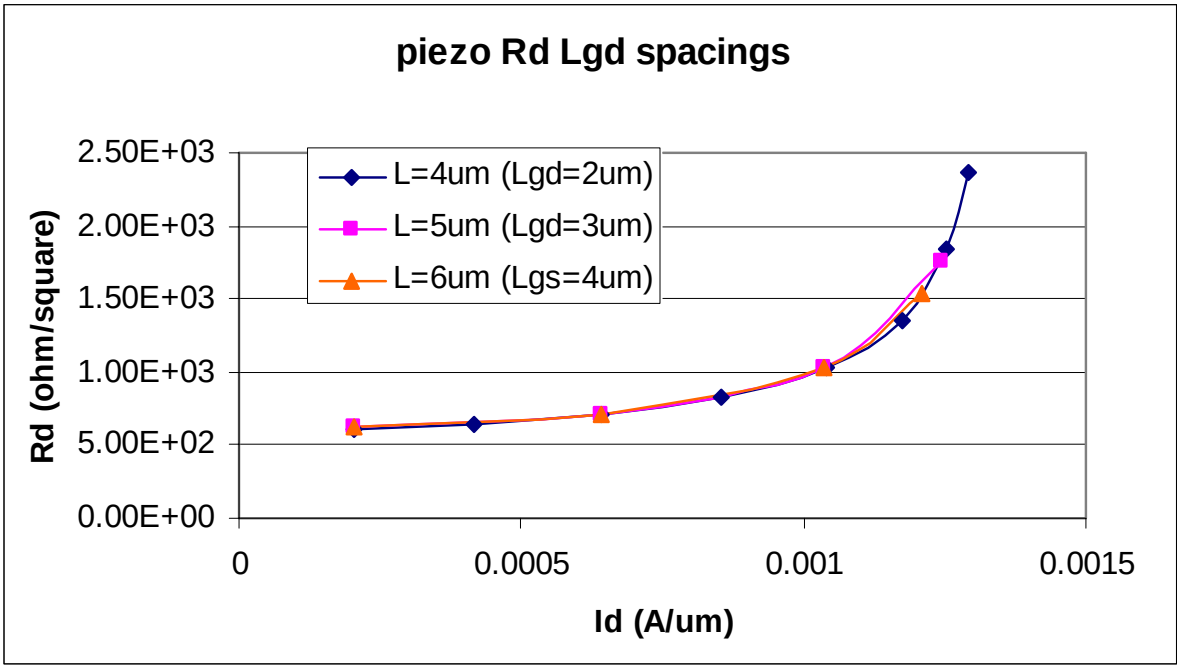

Fig 3.4: Resistivity versus drain current density of a set of AlGaN/GaN HFETs with the same fabrication structure but different lengths of drain access region. The curve with blue diamonds is for the 4-micron device whose structure is shown in Fig 2.1. The curve with magenta squares is for a device having one extra micron in the drain access region, making the device's total length 5 micron. The curve with orange triangles is for a device with still another micron in the drain access region's length, making it 6 microns in total length. Data are from ATLAS simulations.

3.4 Performance degradation due to nonlinear resistance

In this section, we are going to investigate the effect of velocity saturation on device performance degradation. The investigation on DC performance degradation is in two stages based on ATLAS simulation result. We will first use Fig 3.5 to show that velocity saturation in the access regions of the HFET is most important for understanding the bell-shaped transconductance of HFETs. We then use Fig 3.6 to show that additional incorporation of velocity saturation under the gate primarily affects the saturation voltage of HFETs.

Fig 3.5 shows the effect of nonlinear resistance in the access regions on a DC IV curve. In this case, as the device is set to work under triode operation, the SNZ and the DNZ entirely occupy both access regions. The symbols in Fig 3.5 were obtained by replacing the nonlinear second order velocity-field curve with constant-mobility velocity model (i.e., a piecewise linear velocity-field relationship) everywhere in the device; they show that the saturation current for large gate voltage is unrealistically large when the resistance of the access regions is treated as a constant. Moreover, it is obvious in Fig 3.5 that the transconductance monotonically increases when linear resistors are assumed, which would corresponds to a constant-slope velocity-field curve. The solid curves in Fig 3.5 were obtained by using the second order velocity-field in the access regions, but for now, constant mobility under the gate to isolate and demonstrates the effects from the SNZ and the DNZ. Fig 3.5 shows that the rate of drain current increasing with gate voltage has a peak that is determined by the velocity field curve in the access regions of the HFET. This reduced sensitivity to gate

voltage produces a bell-shaped transconductance. In other words, the open-channel-side of the transconductance curve is suppressed by the compression of drain current at the large drain current end, i.e. the large gate voltage end.

It is also interesting that, as shown in Fig 3.5, the IV curves at gate voltages near pinchoff voltage (-4.12V) have a much less error, which are IV curves corresponding to gate voltages of -2V,-3V and -4V. However, those IV curves with higher gate voltages (-1V and 1V), which are the curves at the top of Fig 3.5, show a much more severe error. The explanation may be that the constant-slope velocity-field curve stays close to the second-order velocity-field curve at low electric field range. The piecewise linear velocity-field curve implies a constant resistivity in both access regions, since carrier velocity does not saturate under this assumption, so that the second order velocity-field curve can be regarded as the cause of non-linear resistance. Meanwhile, according to the analysis in the previous section, the low electric field in the access regions corresponds to low drain current in the device, in other words, operations near pinchoff voltage with low Vd. We will discuss the relation between DC IV characteristics and velocity-field curve more specifically in 3.5.

Fig 3.6 shows that the velocity-field relationship in the Intrinsic FET zone is significant even though its effect is smaller. In Fig 3.6, the solid lines now show DC IV curves assuming a second order velocity-field relationship in the access regions but a constant-mobility in the Intrinsic FET Zone. The symbols in Fig 3.6 show DC IV curves obtained using the more

realistic second order velocity-field relationship everywhere. The DC IV curves in symbols are compressed somewhat more than the solid curves, but the most pronounced new effect of velocity saturation in the intrinsic FET zone is the reduction of saturation voltages. Historically, a similar effect was found in AlGaAs/GaAs HEMT's [3] [7].

Moreover, it can be noticed in Fig 3.6 that this velocity-field curve replacement in the Intrinsic FET Zone affects more around the peak of the transconductance curve. As a result, the bell-shape becomes more notable.

Now we can conclude that the nonlinearity of resistance in the SNZ and the DNZ comes from the nonlinear velocity-field curve. Increasing drain current level aggravates this nonlinearity. This explains that why constant resistors models of the source and drain access regions do not incur significant error when the drain current level is relatively low. However, in AlGaN/GaN HFETs, a high drain current level is usual when the device is driven hard. In this case, the error in source and drain resistors is no longer negligible.

The nonlinear resistance works like a negative feedback per se. When the current level approaches the maximum transportation capacity, I_{sat}, the resistance dramatically increases to suppress the current flowing through it, as shown in Fig 3.1. This degrades the

transconductance and make it bell-shaped by decreasing it in the open channel end where the Vg and hence current is high.

This current suppression also gives us an insight on the phenomenon “RF-walkout” when the device is driven to a higher power level [8]. This is illustrated in Fig. 3.7 [9]. The dynamic load line rotates in the region where drain current is high. We explain this distortion on the dynamic load line in the way that the source and drain resistances change nonlinearly when the drain level reaches the neighborhood of I_{sat}. This effect keeps the dynamic load line from achieving its full extent of the potential current swing indicated in DC IV characteristics, and as a result, may greatly harm the device RF performance and linearity if not considered prior to a specific design.

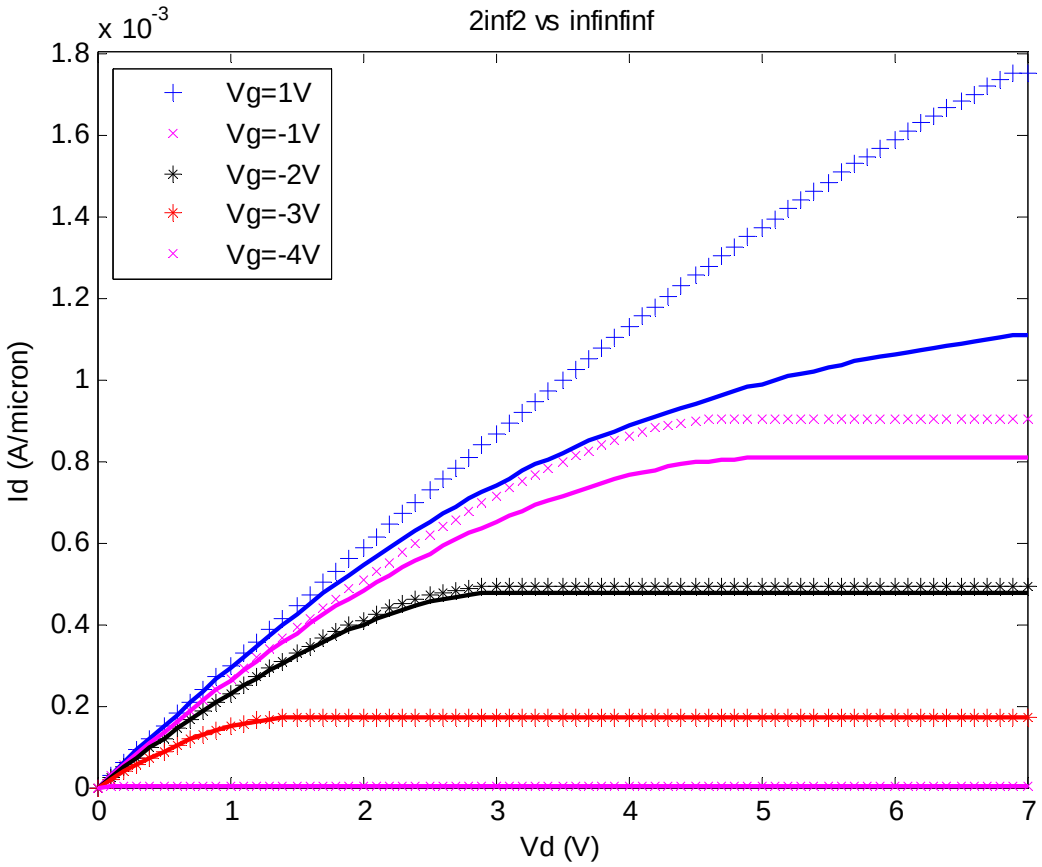

Fig 3.5: Impact of non-linear source and drain access resistances on modeled DC IV curves. Symbols assume constant resistances everywhere. Solid lines assume non-linear resistances in the access regions as discussed in the text.

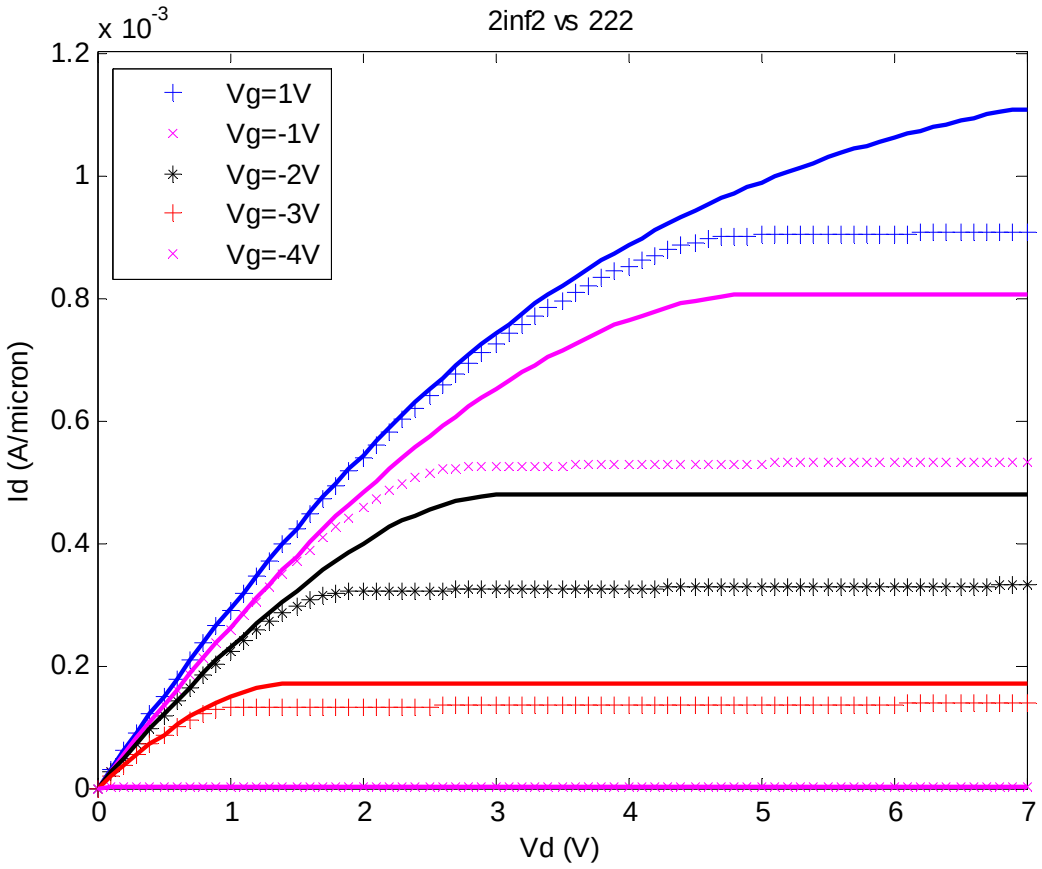

Fig 3.6: Impact of velocity-field curve in the Intrinsic FET Zone on the modeled DC IV curves of an HFET. The solid lines assume a second order velocity-field curve in the access regions but a piecewise velocity-field curve in the Intrinsic FET Zone. The symbols assume a second order velocity-field curve everywhere in the HFET.

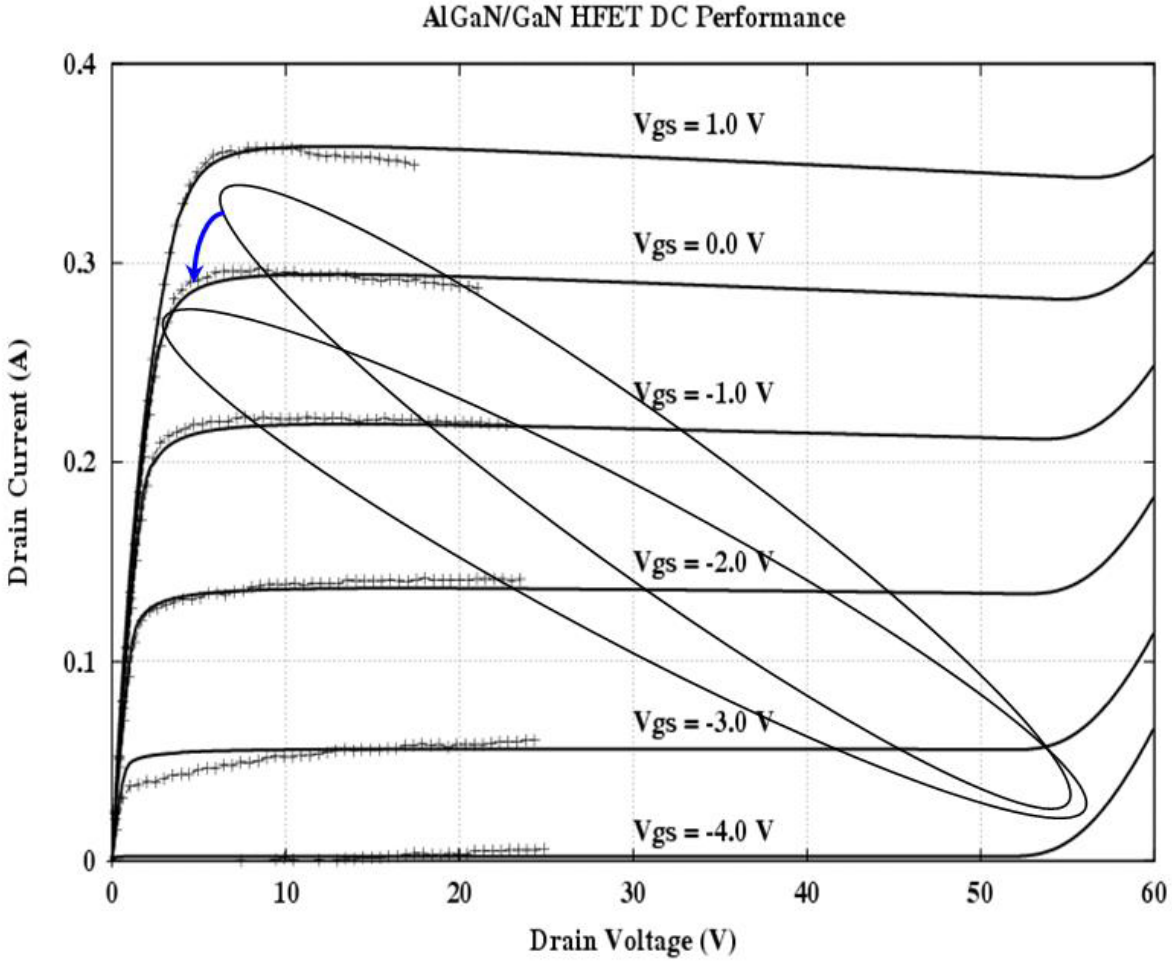

Fig 3.7: Impact of nonlinear resistance in RF performance, known as “RF-walkout”. The dynamic load line rotates counterclockwise during a large signal simulation [9]

3.5 Key role of velocity-field curve

We now reproduced the I-V curves from a two dimensional simulation of a AlGaN/GaN HFET with a compact model, using only geometrical specifications and material parameters, including the same value of p in velocity-field curve. In this section we show the necessity of accurately modeling p by comparing compact models corresponding to different values of p in the velocity-field curve. The ATLAS simulated device in this investigation has a similar structure to the primary device used in this dissertation. The only difference is that the pinchoff voltage is -5.2V instead of -4.12V.

The original fit of an HFET assumed a p=2 velocity-field curve as shown in Equation (3.3). Fig 3.8 shows the DC IV characteristics simulated by ATLAS using a p=2 velocity-field curve, together with the model result using p=2. The model prediction matches simulation result very well. We will then compare it with a fit using p=1

$$v = \frac{\mu E}{1 + \left(E / E_C\right)} \tag{3.9}$$

We will use this pair of p values to show that a set of I-V characteristics corresponding to one value of p can be matched using a different value of p by adjusting the electron mobility and saturation velocity, but that this approach will result in different estimates of important figures of merit, such as the cutoff frequency.

As an example, if we simply change p to 1 in our proposed model we cannot expect the resulting p=1 model curves to fit the I-V simulation data because the simulation data was produced with p=2. This is confirmed in Fig 3.9. However this approach does preserve the simulation values of μ=1500 cm^2/V-s and v_{sat} =1.2*10^7cm/s in the original p=2 velocity-field curve, and therefore it also preserves the cutoff frequency which is proportional to saturation velocity. Fig 3.10 shows that we can apparently improve the erroneous fit shown in Fig 3.9 by increasing mobility by 30% to μ=1950cm^2/V-s and increasing saturation velocity by 35% to v_{sat} =1.62*10^7cm/s in this p=1 model.

This DC IV characteristics matching between two set of completely different parameters is not a coincidence. The first set of parameters is p=1, μ=1950 cm^2/V-s and v_{sat} =1.62*10^7cm/s. The second set is p=2, μ=1500 cm^2/V-s and v_{sat} =1.2*10^7cm/s. This DC IV characteristics matching, instead, is a consequence of velocity-field curve match. Fig. 3.11 compares the various velocity-field curves corresponding to these cases. The original p=2 velocity-field curve (red solid line) corresponds to the ATLAS simulation of I-V data. The p=1 velocity-field curve (cyan triangles) comes from μ=1500 cm^2/V-s and v_{sat} =1.2*10^7cm/s, which is used in the p=1 model resulting in erroneous fit in Fig. 3.9. The p=1 velocity-field curve (indigo crosses) comes from μ=1950cm^2/V-s and v_{sat} =1.62*10^7cm/s, which is used in the p=1 model resulting in Fig 3.10. The piecewise linear curve (black dashed line) with the same μ and v_{sat} as the ATLAS simulation is included for comparison. Comparison of the indigo (with crosses) and red (solid line) curves shows that the adjusted p=1 velocity-field

curve now approximates the p=2 velocity-field curve of the original fit at low fields. This agreement is the underlying reason for the improved I-V fit in Fig 3.10. This adjusted p=1 model is almost as accurate as the p=2 model, but it significantly overestimates the mobility and saturation velocity, which leads to different estimates of figures or merit such as the cutoff frequency. Moreover, the adjusted p=1 velocity-field curve does not stay in the proximity of p=2 velocity-field curve within the whole range. This suggests that this approximation is only valid in a certain low electric field range. In other words, this alternative velocity-field curve may incur significant error in DC IV characteristics if the external bias condition makes the electric field inside the device out of a specific range. We conclude that it is not possible to predict RF performance of a device by fitting its DC IV curves only.

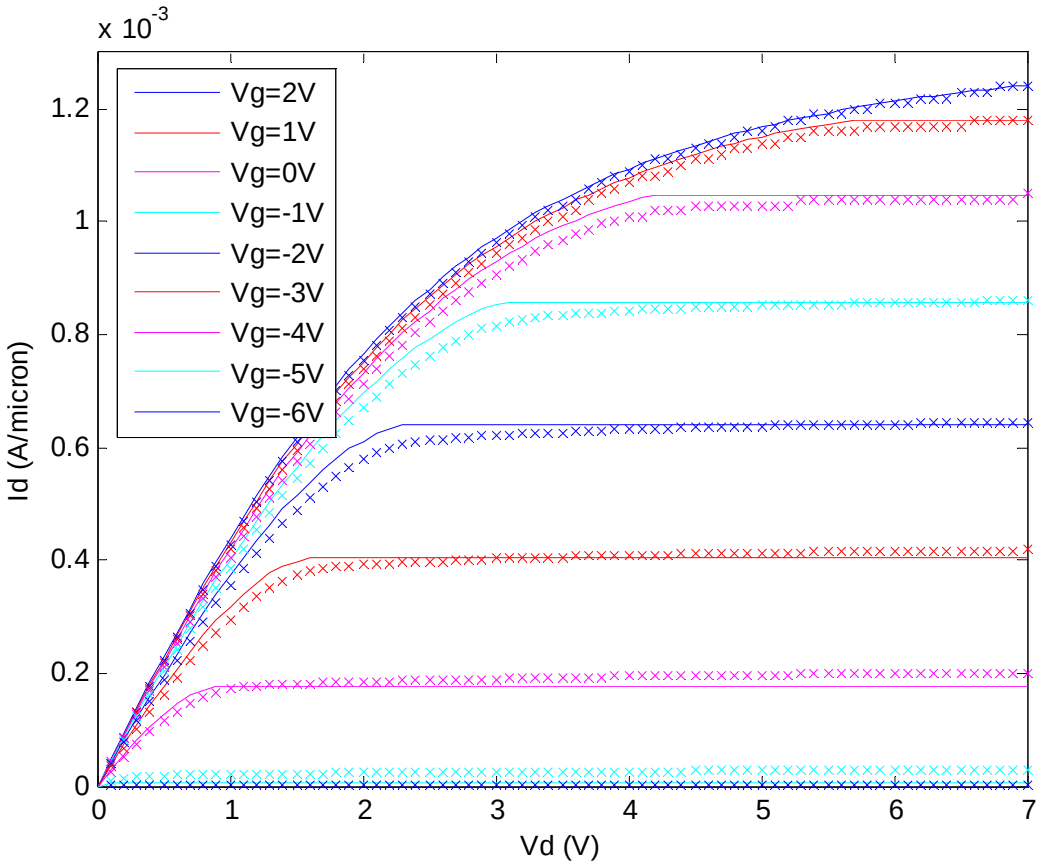

Fig 3.8: I-V characteristic of an AlGaN/GaN HFET. Crosses are ATLAS simulation data. Solid lines are the model result.

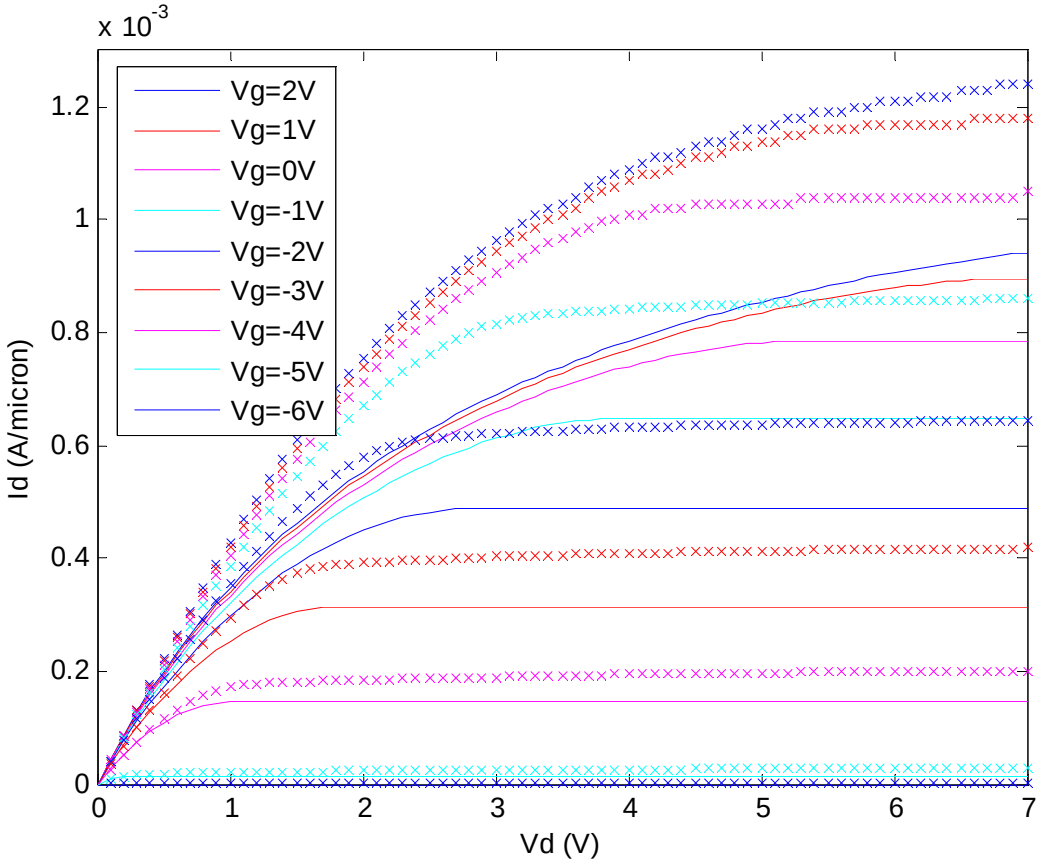

Fig 3.9: I-V curve (shown for comparison with Fig 3.8) of a p=1 model with unadjusted electron mobility and saturation velocity. Crosses are simulation data. Solid lines result from the model.

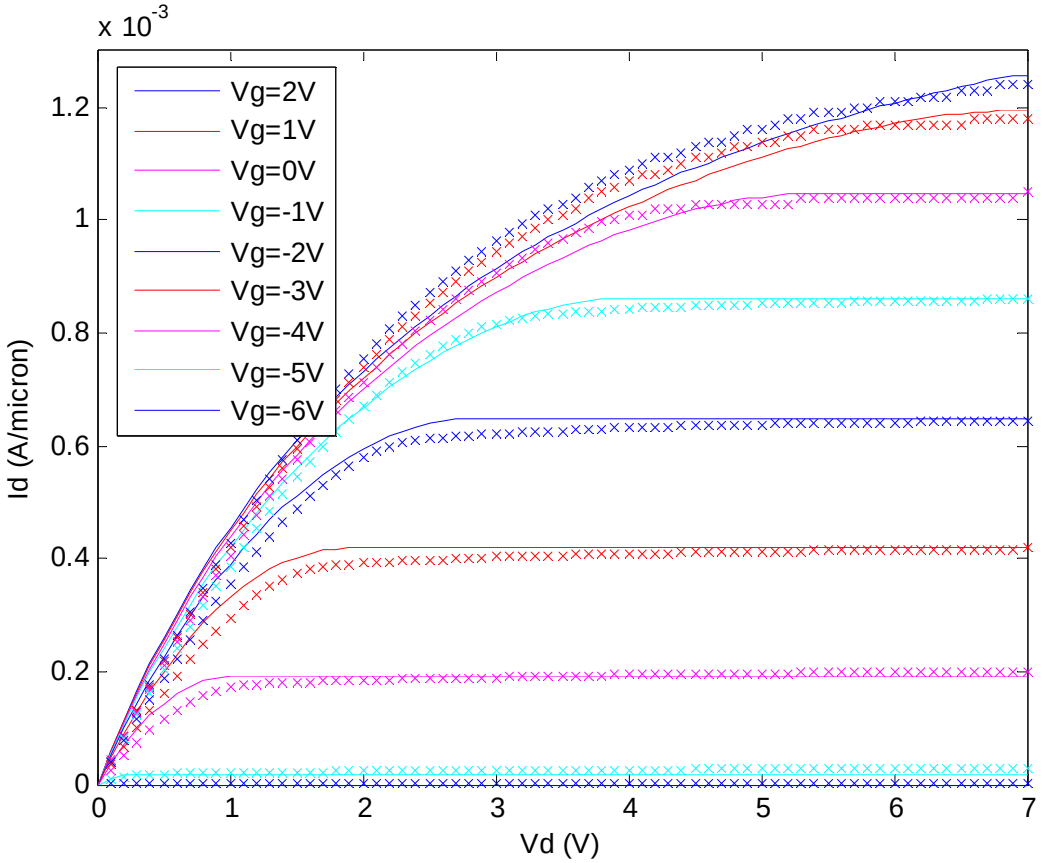

Fig 3.10: I-V curve of a p=1 model with adjusted electron mobility and saturation velocity. Mobility is set as 1.3 times of its original value. Saturation velocity is adjusted 1.35 times larger. Crosses are simulation data. Solid lines are the model result

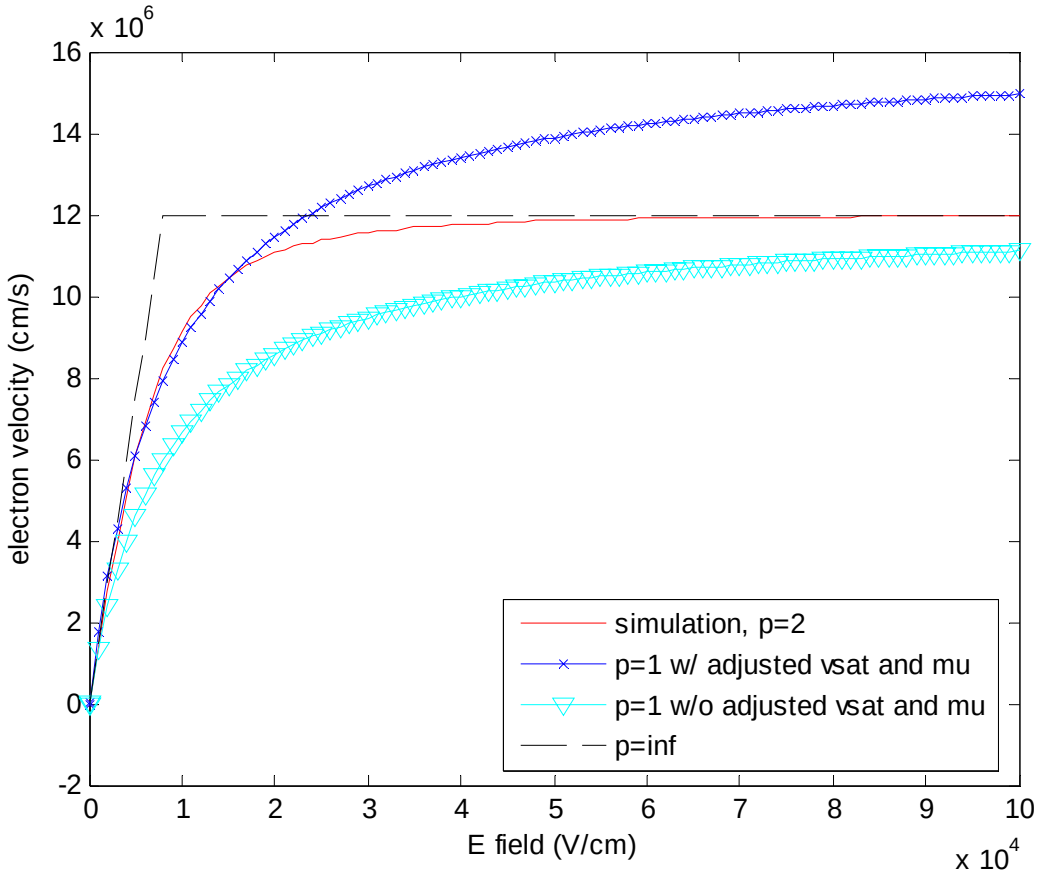

Fig 3.11: Fit of electron velocity-electric field curves. Red solid line is the ATLAS simulation result. Cyan curve with triangles is the unadjusted p=1 curve used in Fig 3.9. Indigo curve with crosses is the adjusted p=1 curve used in Fig 3.10. Black dashed line is the usual piecewise linear velocity field curve.

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CHAPTER 4

4.1 Space Charge Limited Zone

As stated in chapter 2, the space charge limited and charge deficit zones occur when the device operates in saturation. The existence of these two zones is apparent in Fig 2.3 and 2.5. After the drain current saturates, a depletion region forms at the gate edge near the drain. This depletion region expands in both directions, towards the source beneath gate, and towards the drain in the drain access region.

In the depletion region's edge beneath the gate, the quantum well at the AlGaN/GaN interface vanishes. The band structure reaches a flat-band condition, which is shown in Fig 2.12. Beyond this flat-band point, no quantum well exists but is replaced by the depletion region, which is shown in Fig 2.16. Hence the electron flow is pushed away from the channel obliquely towards the bottom of the device. This detour is obvious in Fig 2.3. Therefore, a net space charge is pushed into the neutral GaN beneath the depletion region while working as the drain current. Hence space charge limited transport is in effect in the SLZ. This space charge limited transport is modeled by solving the1D Poisson equation [1], which we will discuss later in this chapter.

4.1.1 Space Charge Limited transportation

When we inject additional charges into a neutral semiconductor, net space charge appears in the semiconductor. At this time, an effect named Space charge limited transportation happens. Before the injection of these excess charges, free electrons in this semiconductor have an amount equal to that of dopants, and hence screen all dopants. As a result, electric field is constant due to Poisson's equation. However, when excess charge exists, the electric field will change due to the charge's effect on Poisson's equation.

Here is an example of space charge limited transport on a uniformly doped semiconductor slab: The slab is uniform in directions of width and depth (y and z directions), so we only need to list expressions in the length direction, x, which is the direction of current flow. For simplification, we assume that ohmic contacts are at both sides. Under equilibrium conditions the lateral electric field in this slab can be expressed according to Poisson's Equation as

$$\frac{dE_x}{dx} = \frac{q}{\varepsilon}\left(N_d - n\right)$$

where Ex is the electric field in x direction, Nd is the donor density, and n is the free electron density under thermal equilibrium. Because the thermal equilibrium electron density essentially equals to the donor density

$$N_d = n$$

Hence Ex is a constant along the slab. However, when there is a high level of current injection making the injected charge in this slab comparable to the thermal equilibrium density of electrons, n, the Poisson's Equation in this slab changes its form to

$$\frac{dE_x}{dx} = \frac{q}{\varepsilon}\left(N_d - n - \delta n\right) = -\frac{q}{\varepsilon}\delta n$$

where δn is the injected charge density. Ex changes exponentially in magnitude as a function of injected charge. At the same time, the voltage dropped across this slab changes in the same manner. We will see in the next section that the same kind of transport occurs in the SLZ due to the similar physical nature between the SLZ and this example semiconductor slab.

4.1.2 Physics in Space Charge Limited Zone

Vertical electric field (Ey) in an ATLAS simulated AlGaN/GaN HFET is shown in Fig 4.1. In the SNZ, IFZ and DNZ, Ey proves our analysis of these three zones in the last two chapters. There is a huge positive Ey in the area close to the AlGaN/GaN interface. According to ATLAS's setting, Ey is positive when electric field lines are pointing downward. This is in accord with our theory in the SNZ, IFZ and the DNZ that there is an electric dipole consisting of a layer of positive sheet charge at the AlGaN/GaN interface and electrons in the quantum well beneath them. Meanwhile, the negative Ey in these three zones' AlGaN layer represents the piezoelectric field in which field lines point upward from positive sheet charge to negative sheet charge at the upper surface of the AlGaN. Moreover, bulk GaN beneath these three zones has Ey close to zero since they are neutral according to our analysis. In conclusion, part of the field lines that emit from positive sheet charge go upward and end on negative sheet charge forming the piezoelectric field. The rest goes downward and is completely screened by the electrons in the quantum well because the density of electrons in the quantum well is always equal to the difference between the

densities of positive and negative sheet charge at the two sides of AlGaN layer. In the IFZ, more field lines end in the gate electrode at the upper surface of AlGaN. This effect is demonstrated in Fig 4.1 by showing a larger Ey in the AlGaN layer above the IFZ. Compared to the SNZ and DNZ, fewer field lines end on electrons in the channel in the IFZ. This agrees with the fact that there are fewer electrons in the IFZ, and results in less Ey in the IFZ's quantum well as well, which can be found in Fig 4.1 too.

However, Fig 4.1 shows that Ey is negative in the SLZ, which is at the source side of bulk GaN beneath the drain-side gate edge. In the SLZ, all field lines emit from the positive sheet charge end at the gate electrode. Besides that, the ionized dopants in the depletion region beneath the positive sheet charge emit field lines ending at the gate electrode as well. In Fig 4.1, we notice that Ey in the GaN beneath the depletion region is around zero. This implies that there are almost no vertical field lines in this area. On the other hand, position closer to the drain has a high voltage. This makes the depletion region expand deeper toward the bottom of device, and hence the area with zero Ey becomes thinner. Eventually, this forms an oblique line, which divides the bulk GaN into two layers. The upper triangle is the depletion region and the lower trapezoid is the zero Ey area in which electrons are flowing. This scenario is depicted in Fig 4.1. Therefore, electron transport in the SLZ is completely driven by the drain since very few electric field lines ending at gate electrode are emitted from this zone, which means no electrons travel across this oblique line. In other words, the electrons in the SLZ are completely free of gate control but are driven by the drain electrode. We may

conclude that electrons in the SLZ are pushed into a trapezoid of neutral GaN by the depletion region. In this zone, space charge limited transportation is in effect. The above analysis is based on the abrupt depletion assumption. In a real device the oblique line is more like an oblique belt and the triangle, together with the trapezoid, does not have a clear boundary. Meanwhile, due to a bounded velocity, electrons should not spread out through the bottom of device as soon as they enter the SLZ. For the sake of simplification, we assume an abrupt depletion approximation and a belt assumption which we will explain further in the following section.

Because of current continuity, the electron concentration and velocity are preserved in the SLZ. According to the analysis carried out in chapter 2, electrons are traveling at a very high velocity close to the saturation value as soon as they leave the IFZ and enter the SLZ. The electrons hardly have any significant margin to move faster. As a result, the amount of electrons in any vertical cross section amid the SLZ has to keep around the same value. Fig 4.2 shows n and Ey in a vertical cross section where the “flat-band” conduction band diagram happens, i.e. the boundary between the IFZ and the SLZ. Fig 4.3 shows n and Ey in a vertical cross section in the middle of the SLZ. We can see in Fig 4.2 that when the quantum well vanishes and hence the SLZ starts, electrons are uniformly distributed in the whole cross section because the conduction band is flat?through the whole bulk GaN layer. Also Fig 4.3 shows that the depletion region squeezes the neutral GaN channel, and electrons evenly spread out through the depth of this channel.

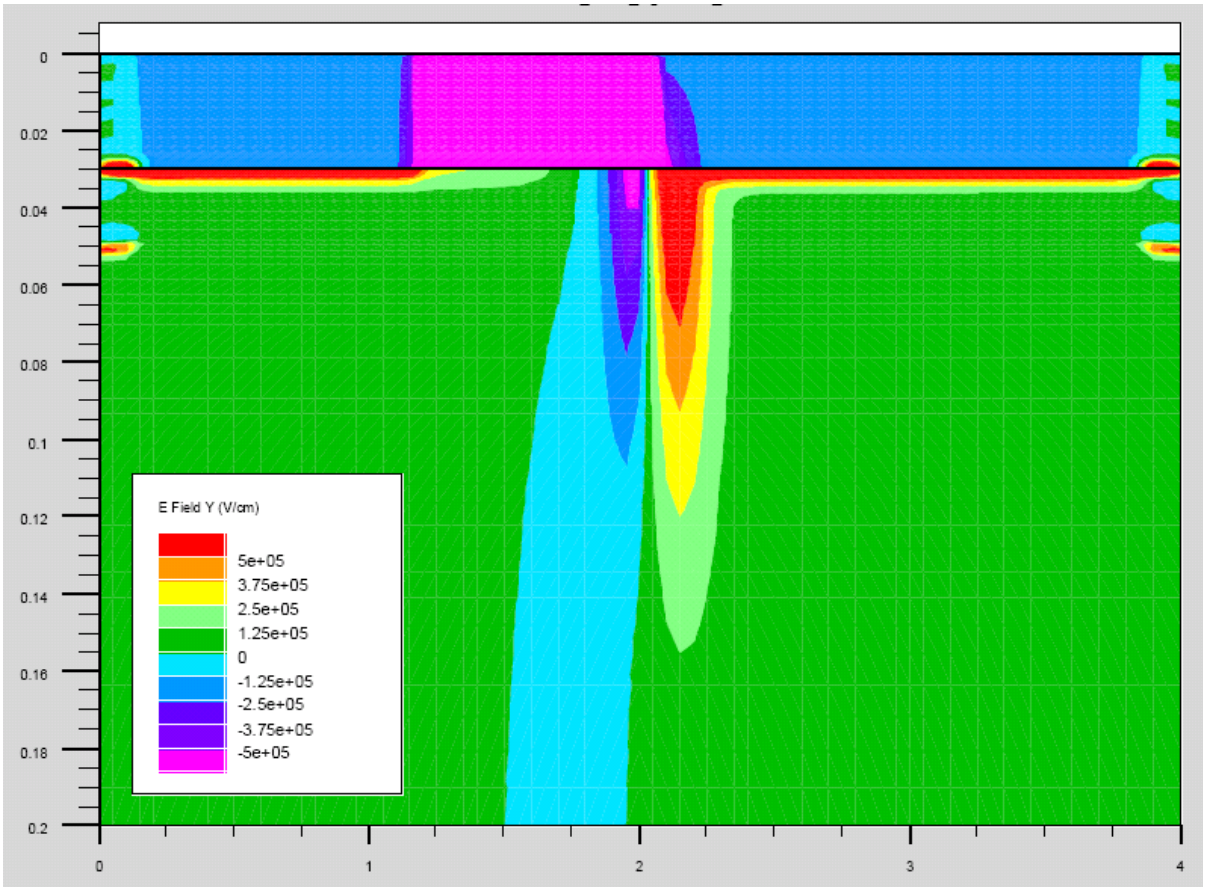

Fig 4.1: ATLAS simulated vertical electric field (Ey) contour. The gate electrode starts from x=1.2; y=0 to x=2; y=0. Source electrode starts from x=0; y=0 to x=0; y=0.05. Drain electrode starts from x=4; y=0 to x=4; y=0.05. All units are in microns.

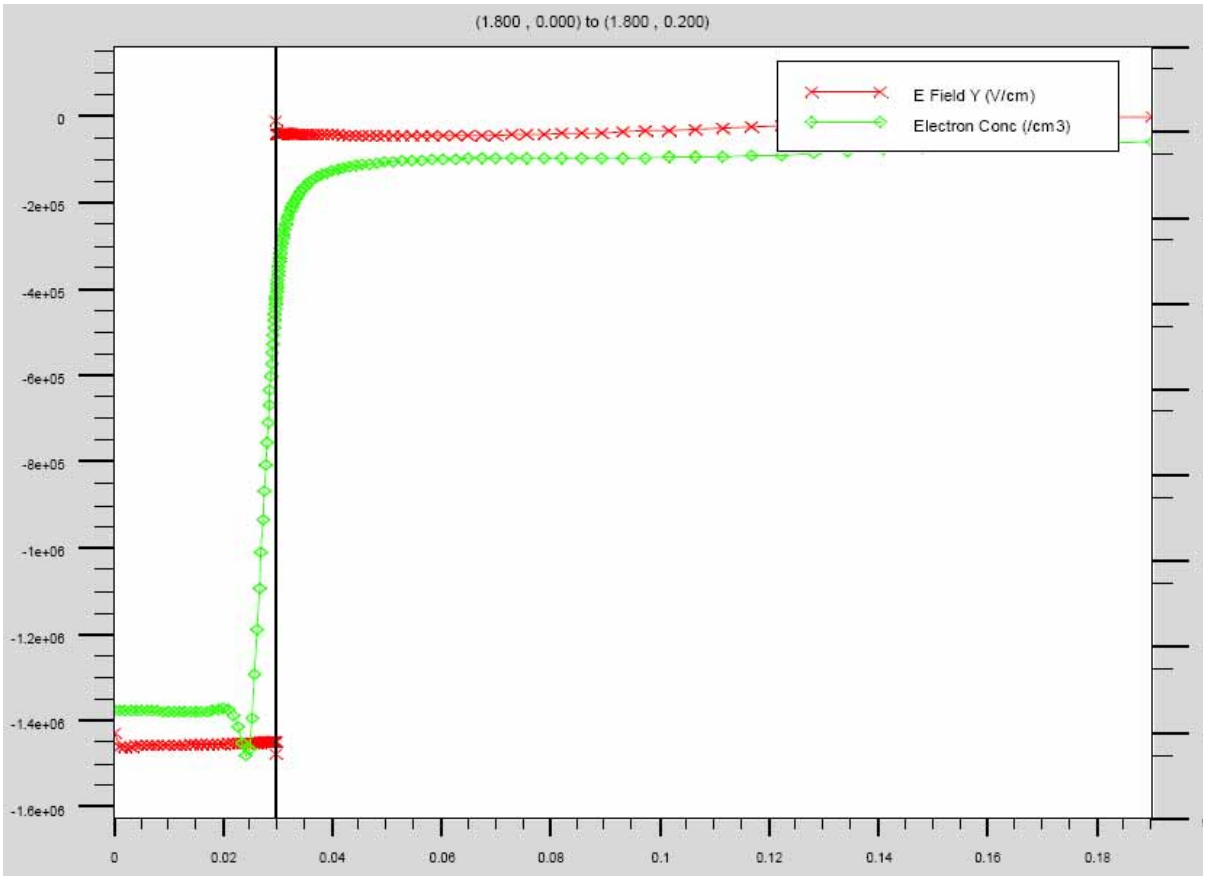

Fig. 4.2 n and Ey in the vertical cross section where "flat-band" conduction band diagram exists (X axes, which stands for Y direction in device, is in units of microns)

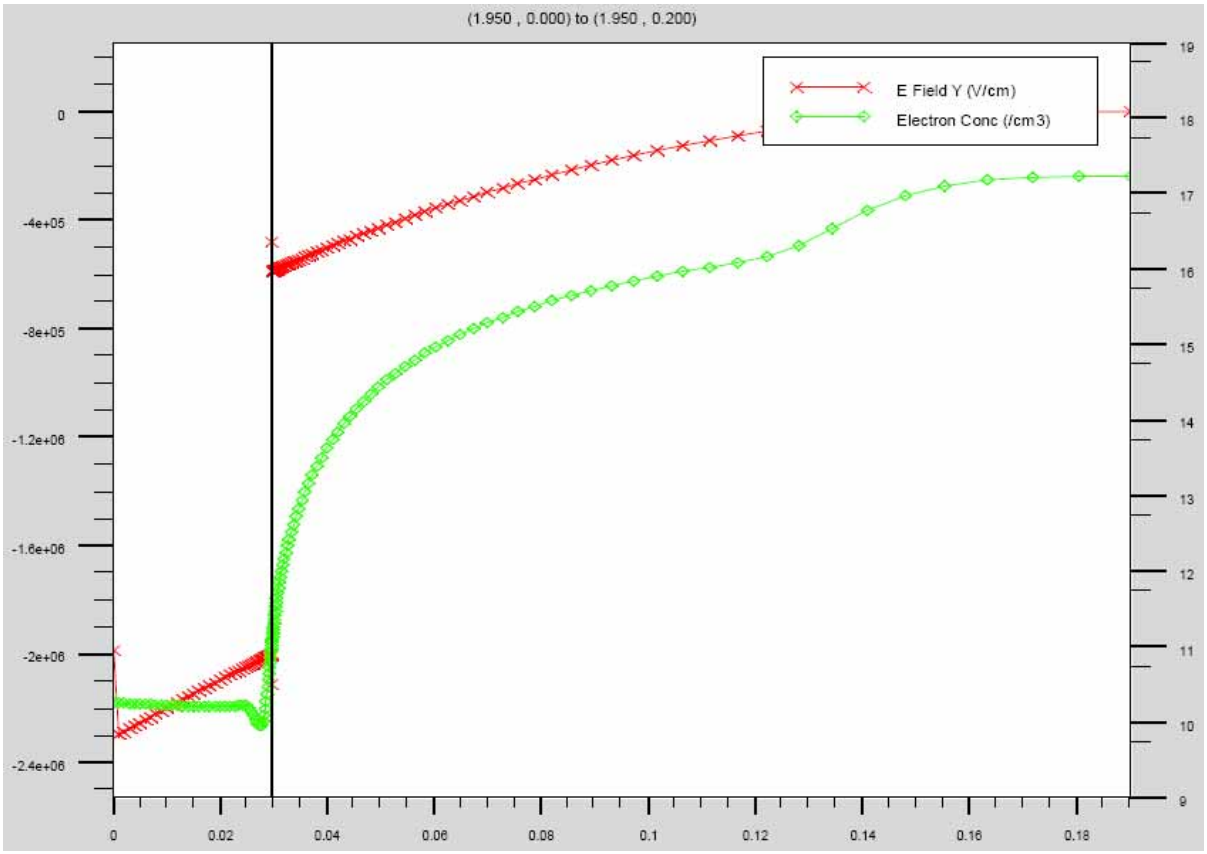

Fig. 4.3 n and Ey in the vertical cross section in the middle of the SLZ (X axes, which stands for Y direction in device, is in units of microns)

4.1.3 Model on Space Charge Limited Zone

As explained previously, we consider space-charge-limited charge transport in the SLZ after the device saturates. The electric field here is very high, and hence, electrons are traveling at a speed close to electron velocity v_{sat}. Therefore, the total amount of electrons in a vertical cross section is

$$N_{SLZ} = \frac{I}{W \times v_{sat}}$$

In fact, this is approximately the total amount of electrons in any vertical cross section in the SLZ as analyzed in the previous section. If we assume an abrupt depletion approximation and define t as the depth of the flat-band GaN beneath the depletion region, which is the channel in the SLZ,

$$N_{SLZ} = \int_{ChannelDepth} n_{SLZ} dz$$

Please note the free electron density is always equal to the ionized dopants before any current injection. Hence the space charge in this zone equals the density of injected electrons n_{SLZ} here, which can be quantified as

$$\frac{dE_x}{dx} = \frac{q}{\varepsilon} \times n_{SLZ} = \frac{I}{\varepsilon \times W \times v_{sat} \times t(x)} \tag{4.1}$$

Here t(x) is the depth of the open channel in the bulk GaN at the device's bottom.

In this model, we also assume that the electron trapezoid is a parallelogram for the sake of simplification. This actually assumes that electron flow does not spread out much in the

vertical direction while flowing in the lateral direction under the influence of the drain electrode. That is, we assume the electron flow in the SLZ is an oblique belt with constant width. At this time, t can be equivalently expressed as a proportional t to the total GaN thickness modulated by the drain current

$$t / t_{GaN} = I / I_{sat} \tag{4.2}$$

where t_{GaN} is the total thickness of the device and I_{sat} is the maximum current that the device can carry. That is, t is a constant instead of a function of position This makes Equation (4.1) to

$$\frac{dE_x}{dx} = \frac{q}{\varepsilon} \times n_{SLZ} = \frac{I_{sat}}{\varepsilon \times W \times v_{sat} \times t_{GaN}} \tag{4.3}$$

Equation (4.3) determines the slope of lateral electric field. We will solve it together with its counterpart in the CDZ for devices working under saturation operation. However, we will show in the following section that the dominant zone in a saturated device is essentially the CDZ which always appears in combination with the SLZ.

Despite the small error, a potential improvement is to solve the 1D Poisson by using t(x) as a linear function. At the boundary of the IFZ and the SLZ, the total thickness of the bulk GaN, $t_{GaN,}$ should be used as t(x). At the boundary of the SLZ and the CDZ, t in Equation (4.2) can be used as t(x) at this end. This will reduce the error from our current “constant-width-belt assumption”, but will bring in a more complex form of voltage drop and electric field in the SLZ.

4.2 Charge Deficit Zone

Under high drain bias, most of drain voltage drops in the drain access region. This leads to a peak of lateral electric field at the gate edge, which is shown in Fig. 4.4. The lateral electric field's peak can be as high as a few MV/cm giving rise to a new but significant zone of interest in the drain access region. Research by other groups suggests a similar picture [2]-[7].

This newly observed zone, usually appearing with a larger voltage drop, is a charge deficit zone where a quantum well exists but contains too few electrons to neutralize the piezoelectric polarization charge. That is, the positive polarization sheet charge at the interface exceeds the charge of electrons in the quantum well. This zone is not conspicuous in the case of a small drain bias application. However, it becomes important when a large drain bias is applied since most of the drain bias drops in this charge deficit region, which is shown in Table 4.1. In a device with a short drain access region, the CDZ may occupy the whole drain access region. In a design with a long enough drain access region, however, the CDZ and the DNZ share the drain access region in the same order away from the drain electrode.

Table 4.1 Percentage of total drain voltage drop in CDZ with regard to drain and gate bias from ATLAS

Vg(V)\Vd(V)	50	100	150	200
2	82%	89%	92%	93%
0	81%	88%	90%	92%
-2	80%	86%	89%	90%
-4	80%	86%	88%	90%

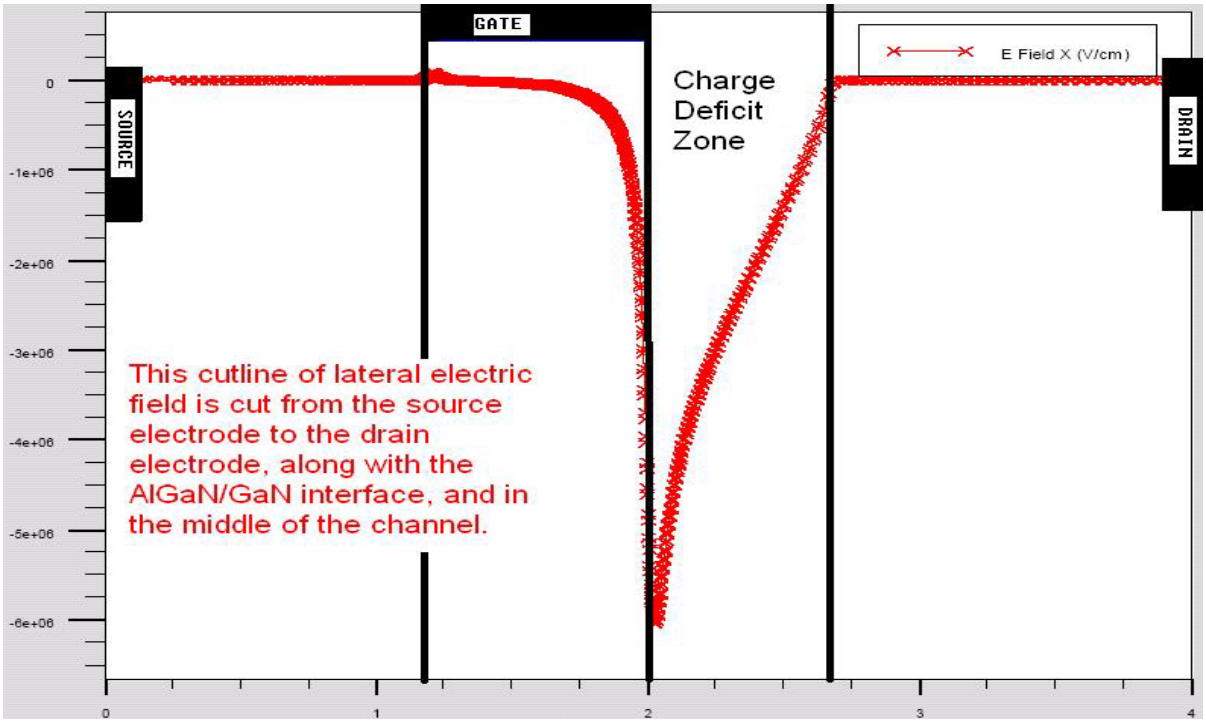

Fig 4.4 ATLAS lateral electric field cutline along the middle line of the channel in an HFET with electrodes marked

4.2.1 Physics in Charge Deficit Zone

After electron flow passes the SLZ, the conduction band in GaN is no longer distorted since there is no gate electrode pinning the Fermi level at the upper surface of AlGaN layer. Consequently, the quantum well at AlGaN/GaN interface resumes. Through the numeric ATLAS simulation, we discovered a new zone next to the SLZ in the drain access region, which is named the CDZ.

The length of the CDZ is dependent on the device structure, and also varies with applied gate and drain bias. The sum of the lengths of the CDZ and the DNZ approximately equals the gate-to-drain length. In fact, there is a transition zone. In this transition zone, electrons, which were previously pushed to the bottom of the device in the SLZ, flow back to the AlGaN/GaN interface before the CDZ starts. This produces a V-shape electron path around the depletion region at the drain-side gate edge, which can be identified in Fig 2.1. However, this transition zone is relatively short. Under a fixed gate bias, the CDZ lengthens with larger drain voltage; as a result the DNZ is shorter at larger Vd.

However, the derivative of Ex in the channel is almost always constant in the CDZ. This is shown in Fig. 4.5a, which plots Ex in this region as a function of the lateral dimension; it shows a family of right-angled triangles with parallel hypotenuses. This pattern of parallel hypotenuses is due to the constant Ex derivative which corresponds to the constant electron concentration here, and the increasing voltage drop caused by the increasing drain bias. In

contrast, Fig. 4.5b compares cases with constant drain bias but different gate bias. In this case, the charge deficit zone's length reaches its minimum when the device is pinched off and approaches its maximum when the drain current approaches the device's capacity value, i.e. the length is largest when the channel is wide open. We notice that in Fig 4.5b, the derivative keeps unchanged after the pinchoff while Vg keeps dropping. The areas of the triangles are almost unchanged by the gate voltage as long as the drain voltage is fixed this time, even though the derivative of Ex increases with decreasing gate bias. This derivative reaches its maximum and stays there after the device begins to pinch off.

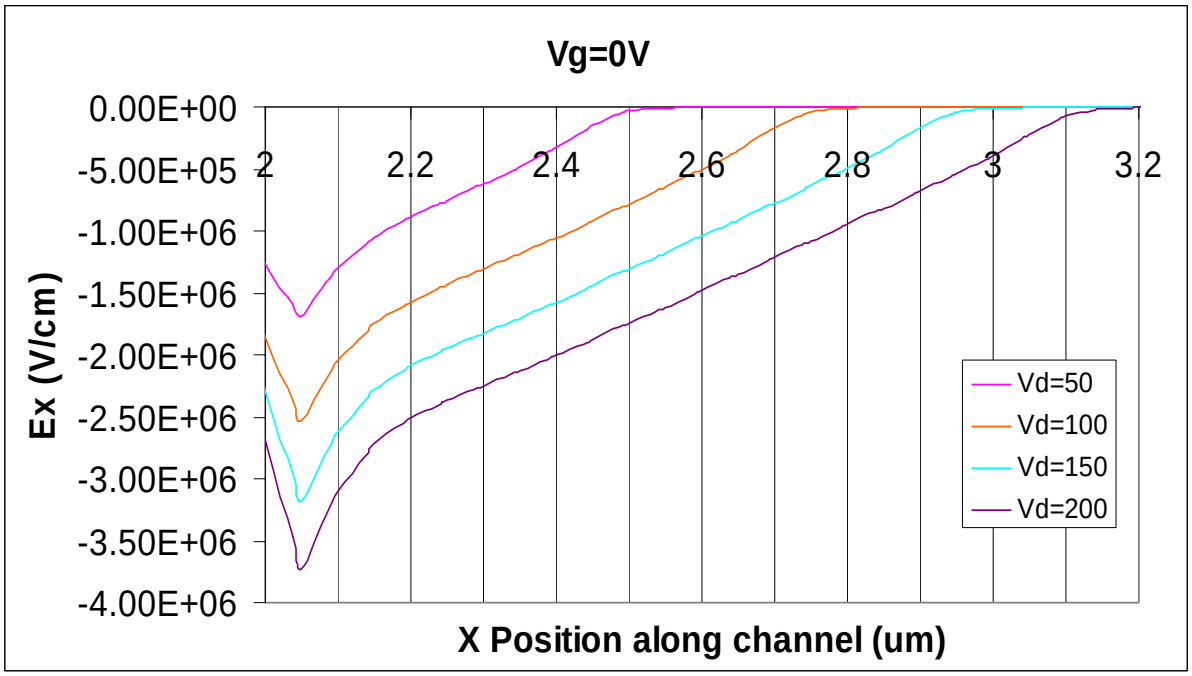

Fig. 4.5a: dEx/dx vs. x in charge deficit zones of HFETs under same Vg but different Vd

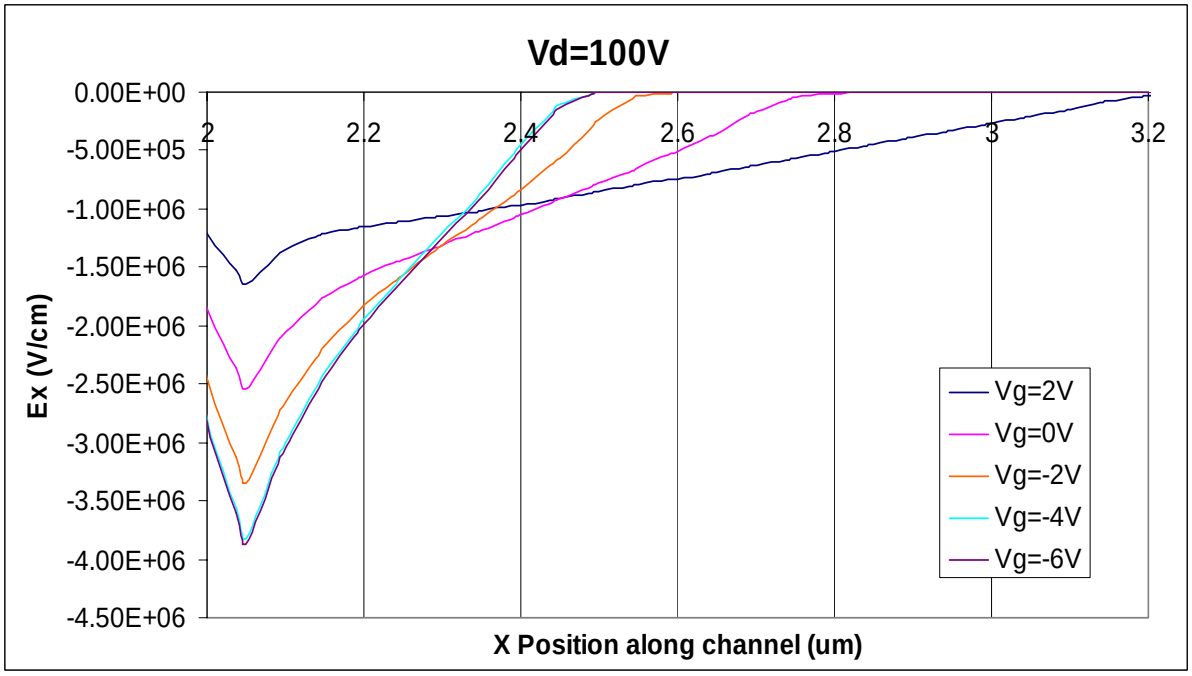

Fig. 4.5b: dEx/dx vs. x in charge deficit zones of HFETs under same Vd but different Vg

4.2.2 Charge Deficit Zone's model and its effect on DC IV

This zone has been previously ignored but is found to have significant effects upon the performance of the device, particularly in high power operation when the device is exposed to high bias and RF terminal voltages. This new model for the charge deficit zone follows classic analytic device modeling procedures, where Poisson's Equation and the electron current density equation are solved analytically in the device.

In the charge deficit region, all electrons travel at their saturation velocity. Because of current continuity, the number of electrons is constant and equals to the quotient of drain current divided by electron saturation velocity as shown in:

$$n = \frac{J_d}{qv_{sat}}$$

This is proved by the comparison with simulation result, which is shown in Fig. 4.6. Therefore, the electron concentration is independent of lateral position. This makes voltage profiles along different vertical cross sections at different lateral positions almost identical. The only difference is a constant voltage shift depending on the distance of the cross section from the drain.

In our analysis, we divide the device into several layers. There are three layers under the abrupt depletion approximation. The layer at the top is a depleted insulating AlGaN layer. A piezoelectric electric field is also there but it does not affect the analysis here. The AlGaN/GaN interface is at the bottom of the AlGaN insulating layer and the positive

polarization sheet charge is confined to this interface. The 2DEG layer lies beneath this interface. This layer is so thin (1-2 nm) that it can be analyzed as a one-dimensional sheet of electrons regardless of the profile of the electron wave function. The peak of vertical electric field and the largest drop rate of the vertical electric field are in this layer caused by the screening of the transportation electrons. At the bottom of the device is the depleted bulk GaN layer. As a result, a cross section of the charge deficit region and its vertical electric field look like Fig 4.7 approximately.

The lateral electric field is continuous everywhere and the vertical electric field has a discontinuity only at the AlGaN/GaN interface because the interface is the only place lying a sheet of charge. By assuming homogeneous (reflecting) Neumann boundary conditions [8] as ATLAS does, we apply the two-dimensional Poisson's Equation in all the three layers. We have:

$$\frac{dEx}{dx} = \frac{qn_{ss}}{\varepsilon T} - \frac{J}{\varepsilon v_{sat} T} + \frac{qN}{\varepsilon} = \frac{q}{\varepsilon T}\left(n_{ss} - \frac{J}{qv_{sat}} + NT \right) \tag{4.4}$$

where n_{ss} is the area density of positive sheet polarization charge at the AlGaN/GaN interface and

We define

$$N = \frac{1}{T}\int_{T} N(y)dy$$

as the effective doping with T as the total thickness of the device.

We verified the resulting model against simulations of industrial AlGaN/GaN HFET shown in Fig 4.8. The device is 4μm long and 0.2μm thick. Its GaN substrate thickness is 0.1703 microns and is N-type at 1e15cm^{-3}. The AlGaN layer thickness is 0.0297 microns and is N-type at 1e16cm^{-3}. The source and drain electrodes are 0.05 micron long. The 0.8 micron gate electrode lies in 1.2μm≤x≤2μm, so that the drain access region is 2μm long. Electron saturation velocity is vsat=1.2e7 cm/s, μ=1500 cm^2/V-s and polarization charge density corresponds to nss=0.7e13 /cm^2. It is convenient to adopt ATLAS's default width of 1 micron.

In the simulation of Fig 4.8, Vg is swept from pinch off to open channel operation and the simulated $\partial E_x/\partial x$ is extracted along a line from source to drain and 1.5nm beneath the AlGaN/GaN interface. The modeled $\partial E_x/\partial x$ predicts an intercept 6.567 MV/cm-μm and a slope 4.854 GΩ/cm. Fig 4.8 shows these values compare well with 2D simulations.

Fig 4.9 and Fig 4.10 show that the DC IV characteristics and the transconductance are both improved by incorporating the SL and CD zone models into the time domain device model. Fig 4.9 shows the impact of the SL and DC zones on the DC IV characteristic. After the device saturates, the expanding SLZ will shorten the IFZ, which makes the effective gate length shorter. This leads to an increase of drain current which is shown as the difference between the dotted lines and solid lines in Fig 4.9. Fig 4.10 shows that a significant offset error is incurred by omitting the SL and CD zones. A similar offset error is not observed in

triode operation [9] because the SL and CD zones are not present before the drain current saturates. However, the offset error appears as the SL and CD zones emerge, and this discrepancy increases with drain voltage when the SL and CD zones are not properly accounted for.

In conclusion, a new and distinct zone (CDZ) in the drain access region of an HFET is analytically characterized. A compact physics-based description of its operation was developed and used to show that the electrical impact of this region increases with drain voltage Vd. The CDZ model was integrated into our previous DC IV model to accurately and compactly reproduce 2D simulation results at all Vd of interest.

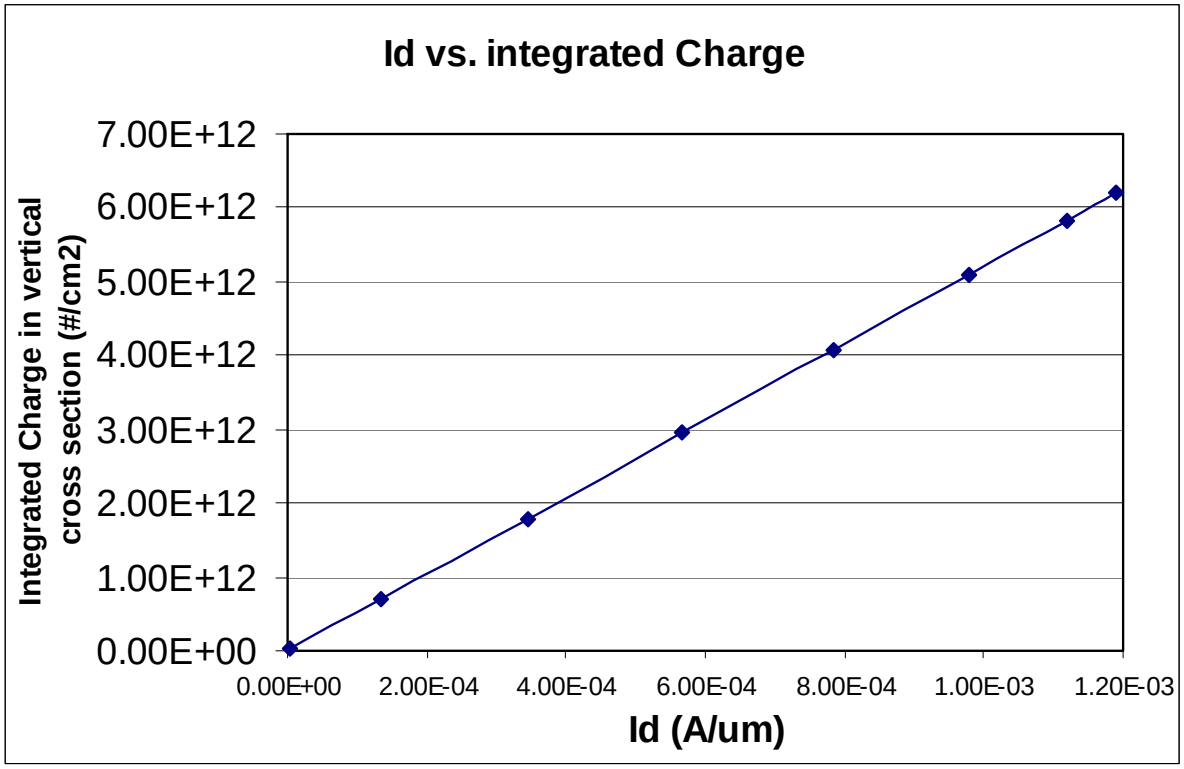

Fig 4.6 ATLAS Election density in charge deficit zone regarding drain current

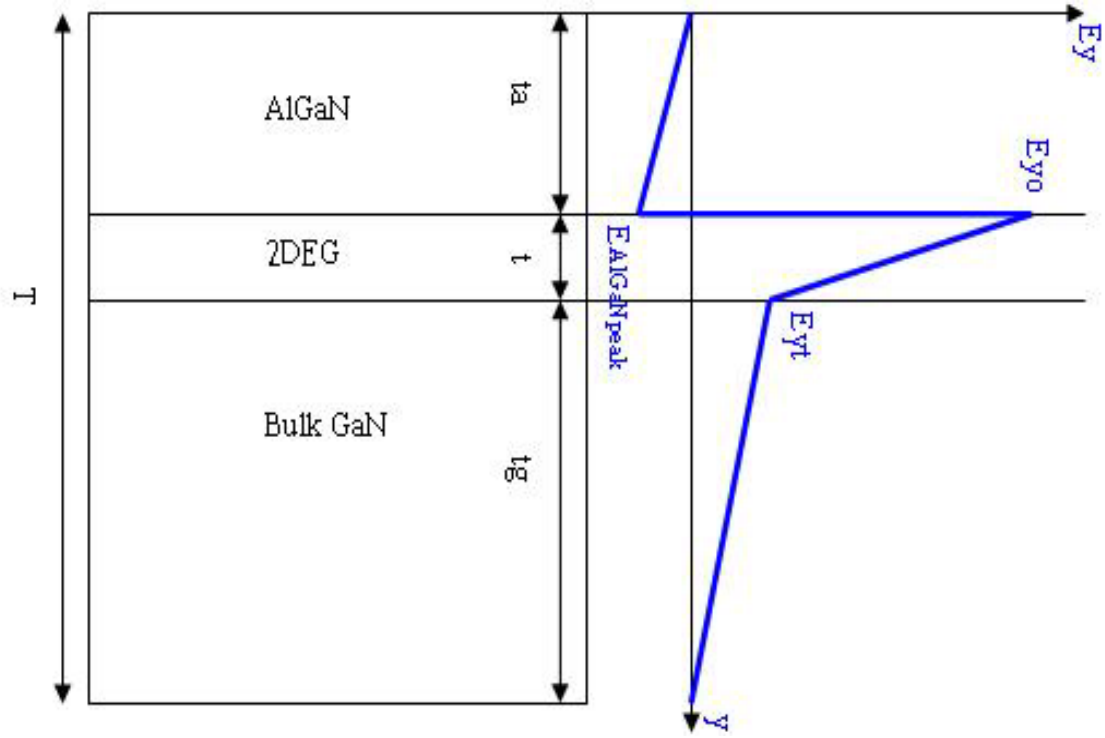

Fig 4.7 Cross section and approximate vertical electric field of charge deficit region

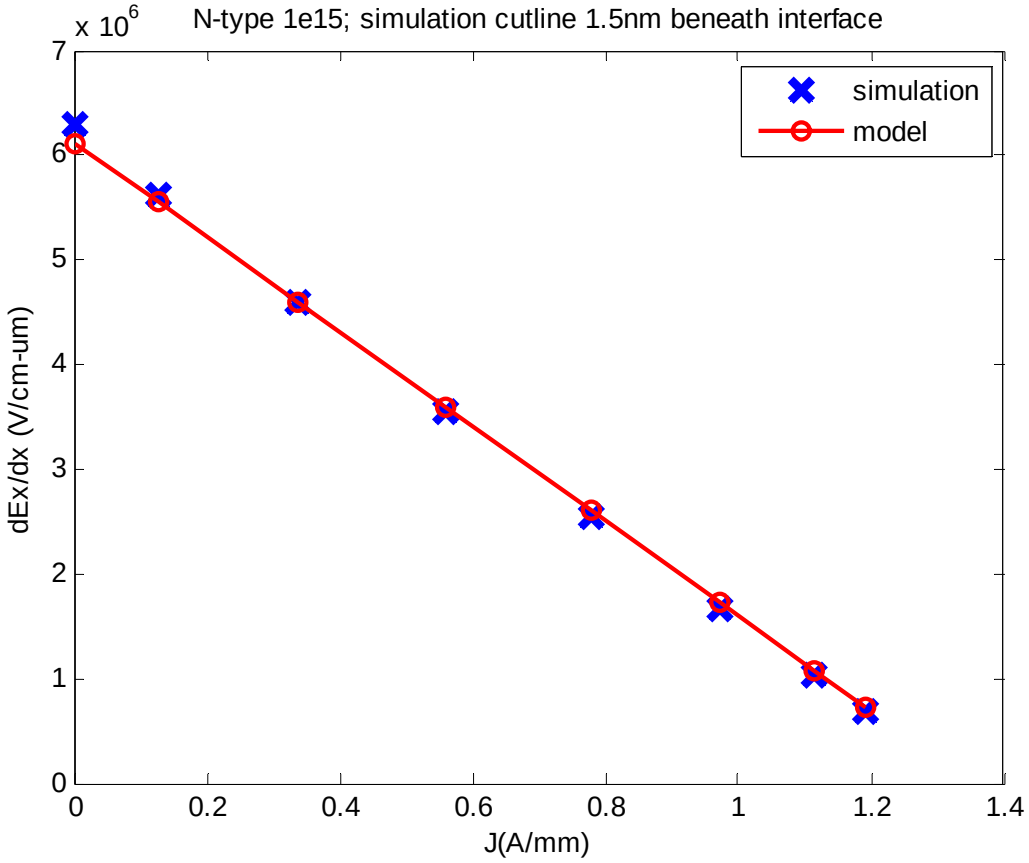

Fig 4.8 Comparison between the simulation data and model result of dEx/dx against J of the 0.2-micron-thick device with 1e15cm-3 GaN substrate background doping

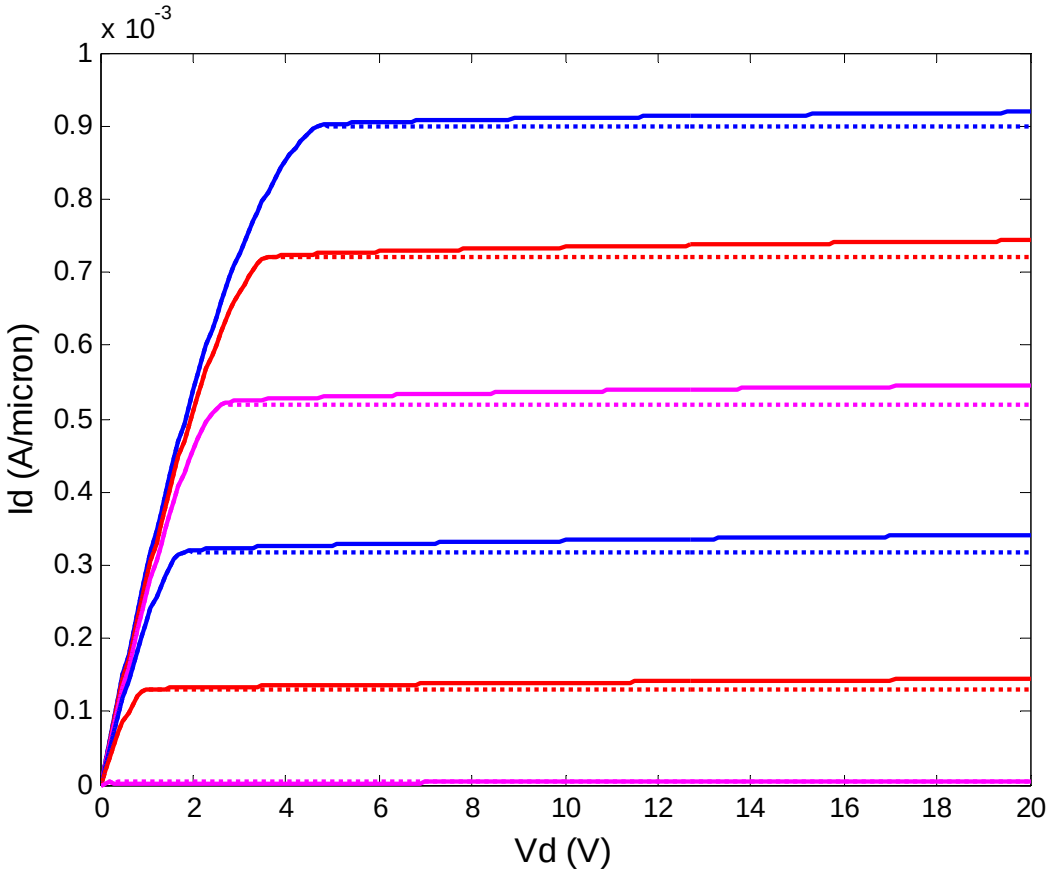

Fig 4.9 Impact of Space-charge Limited and Charge Deficit (SL and CD) zones on the DC IV curves up to 20V of an HFET. The dotted lines are the model without considering these two zones. The solid lines are from the new model which properly accounts for both these zones.

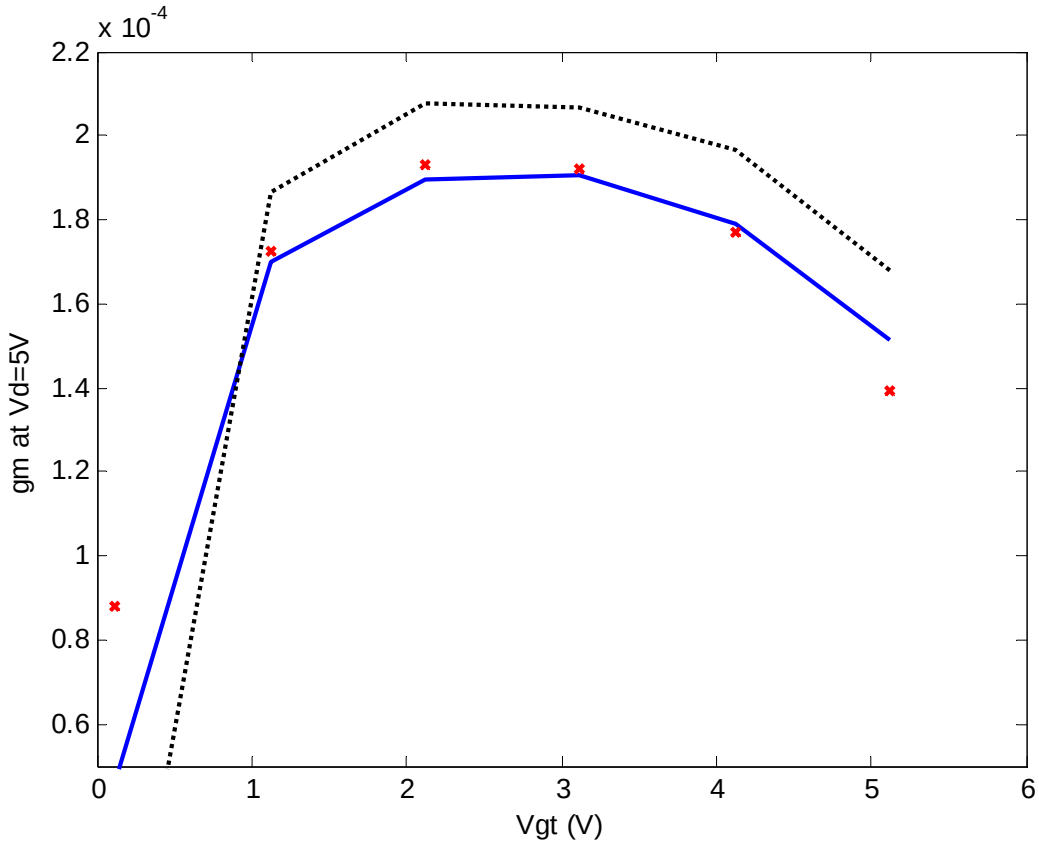

Fig 4.10 Modeled transconductance at Vd=5V is improved by proper inclusion of the new SL and CD zones. DOTTED LINE: Significant errors are observed before inclusion of the Space Charge Limited and Charge Deficit Zones, SOLID LINE: the complete model agrees with ATLAS simulation data which are shown as CROSSES.

4.2.3 Model verification on background doping and device thickness

To further test the model, another set of simulations were run. The GaN substrate doping was kept N-type, but elevated to 1e17cm^{-3} for the second simulation. All other parameters were kept unchanged. The comparison of Ex's derivative between modeled and simulated results is in Fig 4.11.

Moreover, a device with a thicker GaN substrate of 0.3703 microns is simulated under appropriate bias conditions. At this time, the thickness of the AlGaN layer remains unchanged. Hence the thickness of the device is 0.4 microns, twice as before. The GaN substrate doping is kept at 1e15cm^{-3} this time. The comparison of Ex's derivative between modeled and simulated results is in Fig 4.12. Hereinbefore, we have tested both fabrication variables and the model agrees well with all testing simulation results.

During these data comparisons, we also find that the GaN substrate background doping has no practical effect when the doping is as low as 1e15cm^{-3}. However, in devices with heavily doped GaN substrate, the substrate doping plays a much more important role. This implies that high enough GaN substrate background doping affects the device operation in contrast to the simulations with lightly doped GaN substrate. Fig 4.13 and Fig 4.14 show the difference between zero background doping and non-zero background doping which are 1e15cm^{-3} and 1e17cm^{-3}, respectively. They prove that the effect of background doping is negligible in and only in lightly doped substrates, as predicted by our model.

We conclude that the degree of impact from background doping is determined by how much space charge the ionized dopants offer. As analyzed previously, the bulk GaN layer is depleted in the CDZ. The total space charge from depleted bulk GaN is a term added to the positive sheet charge in Equation (4.4). Hence this term is negligible when it is much smaller, 1e15cm^{-3} in this case, than n_{ss}. This further verifies our model expression from another perspective.

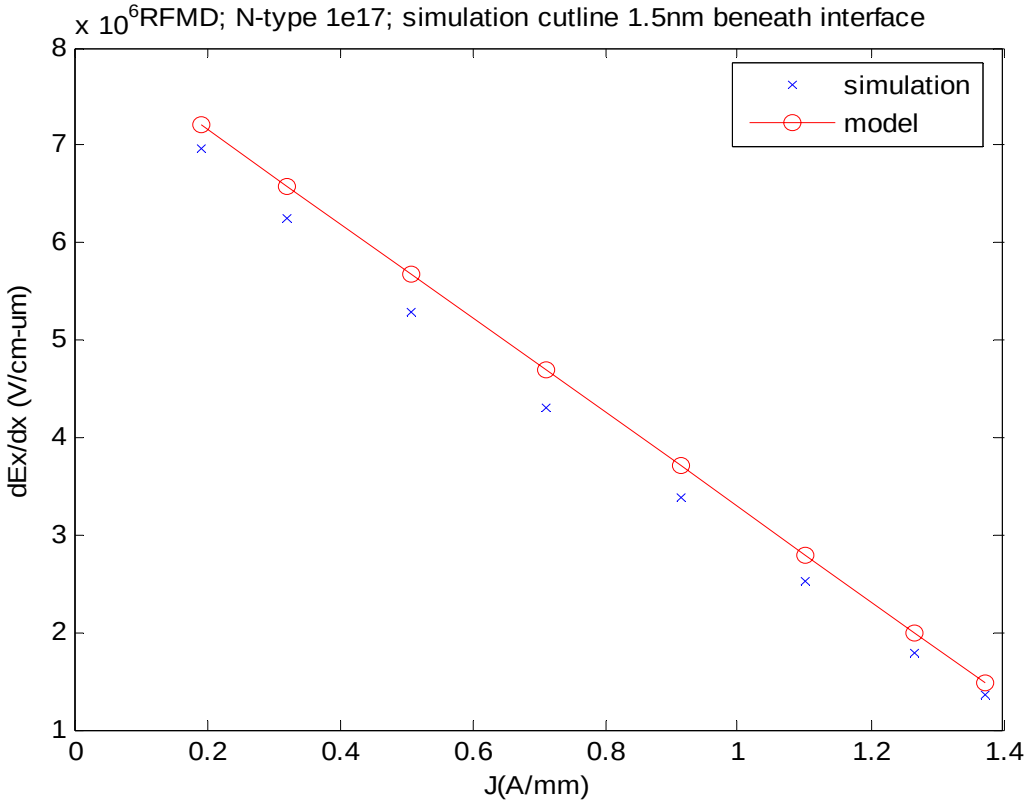

Fig 4.11 Comparison between the simulation data and model result of dEx/dx against J of the 0.2-micron-thick device with 1e17cm^{-3} GaN substrate background doping

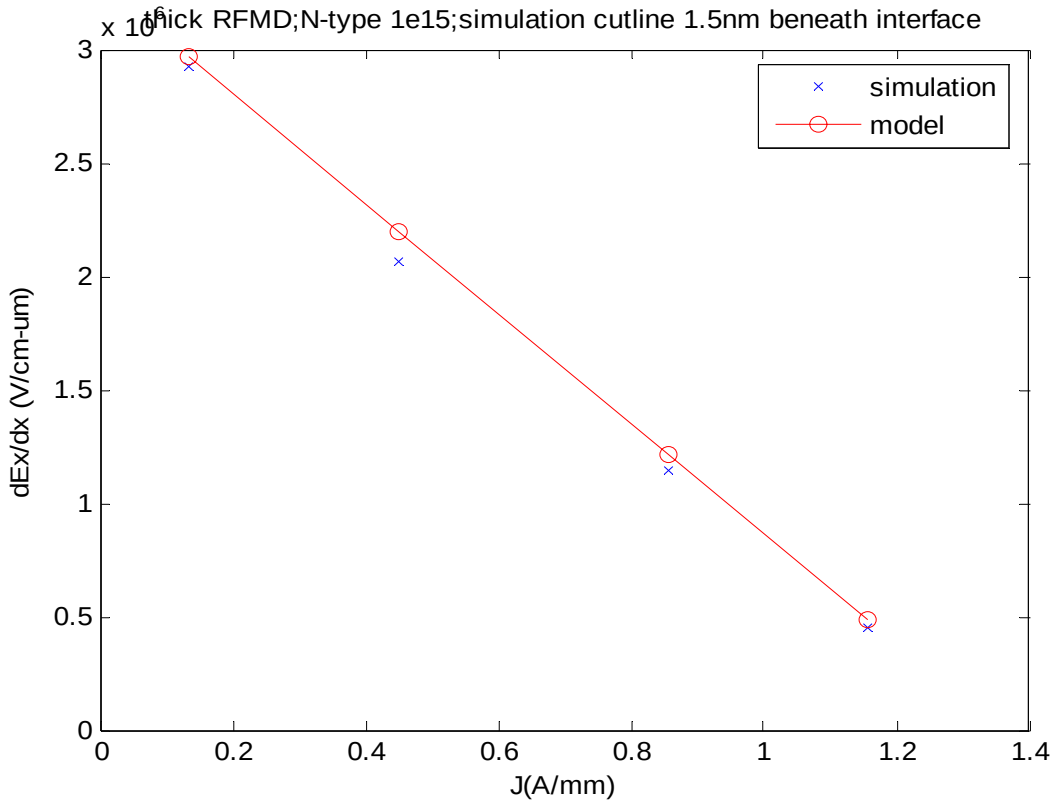

Fig 4.12 Comparison between the simulation data and model result of dEx/dx against J of the 0.4-micron-thick device with 1e15cm^{-3} GaN substrate background doping

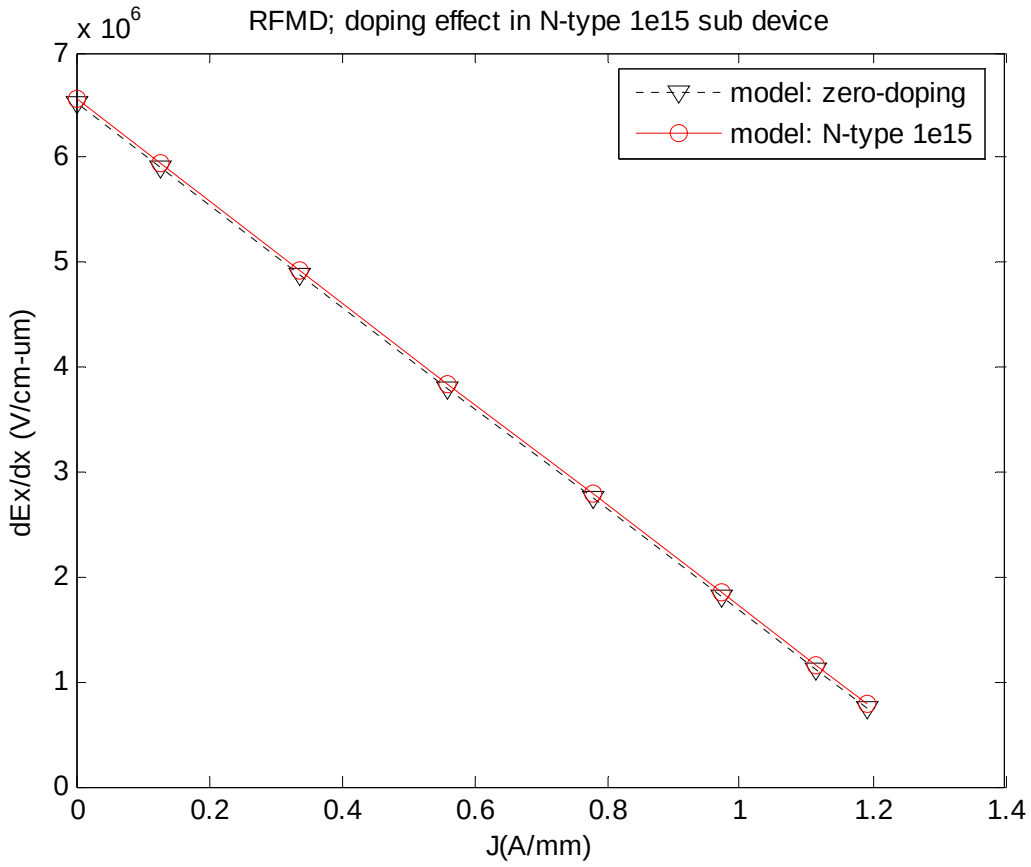

Fig 4.13 Comparison between model results of zero background doping and 1e15cm^{-3} N-type doping with the same device structure and operating environments

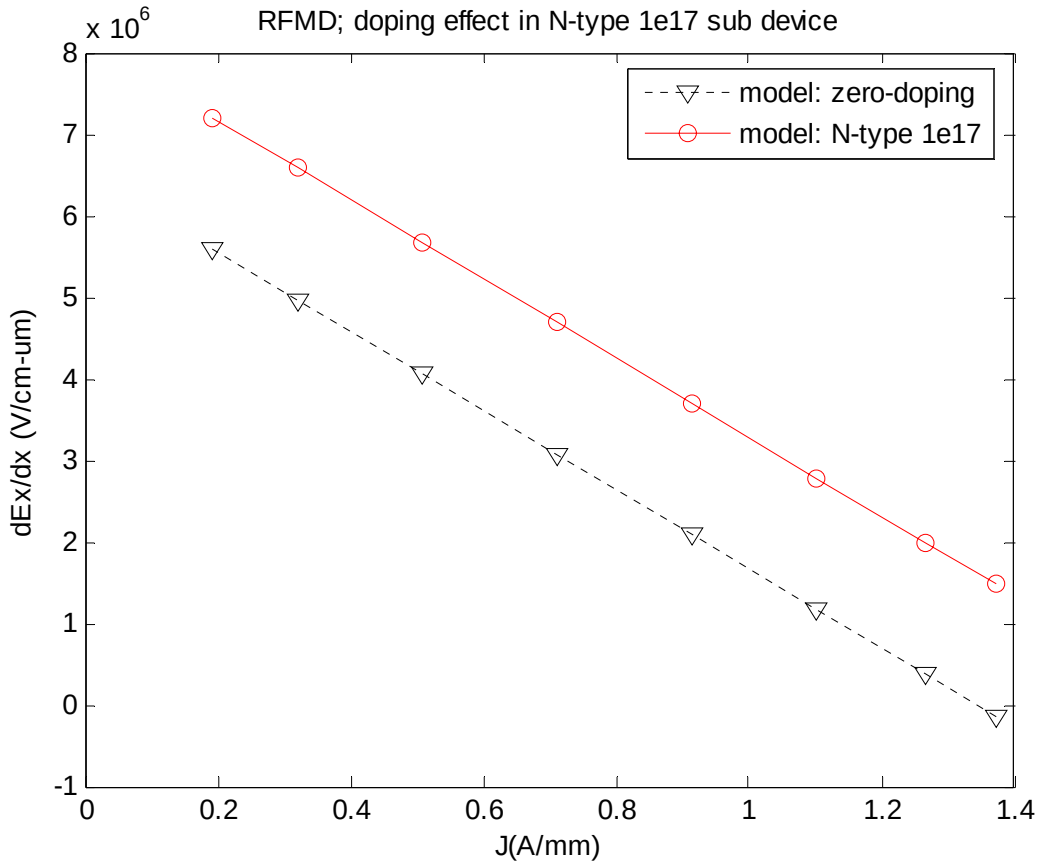

Fig 4.14 Comparison between model results of zero background doping and 1e17cm^{-3} N-type doping with the same device structure and operating environments

4.3 Impact Ionization and control methods

When the device is driven under high drain bias, impact ionization may no longer be negligible and bring degradation to the device's performance. The impact ionization current is usually evaluated by [10]

$$G = \alpha J = aJe^{-b/E} \tag{4.5}$$

Where a and b are empirical constants, E is the electric field where impact ionization happens, and J is the current density at the position. Please note that E should be the projection of the total electric field on the direction of J. The contribution from holes is trivial in an HFET and hence neglected here. ATLAS uses the same expression when evaluating impact ionization as well [8]. Obviously, because b is in the exponential in Equation (4.5), it is more significant in modulating the impact ionization. Additionally, b is large in GaN due to its large bandgap. Fig 4.15 shows an example of how a and b help in controlling the impact ionization rate. In Fig 4.15, ratio on alpha is plot against change in b with electric field fixed, which corresponds to fraction change on b/E ratio.

At the same time, Equation (4.5) also suggests that the CDZ be the zone where the most impact ionizations happen because lateral electric field is the highest in the CDZ. Also current is in the same direction of lateral electric field in this zone. Fig 4.16 shows the simulated impact ionization rate along a parallel line along and 1nm beneath the AlGaN/GaN interface. The impact ionization rate does show the same trend with lateral electric field. On the other hand, Ex is independent of depth z. Fig 4.17 shows that the impact ionization is the

highest in the quantum well. This is in accordance with Equation (4.5) that impact ionization needs both Ex and current density (J). J is the highest at the range of quantum well in the depth direction, which agrees with our analysis that electrons are confined in quantum well in the CDZ.

In overview of the whole device, Fig 4.18 shows simulated impact ionization rates within the entire device along three load lines. In this figure, we notice that impact ionization rate is low at the open channel end because the lateral electric field is relatively low when the channel is open, regardless that the CDZ is longer at this moment. The explanation is that the ratio b/E is dominant in the impact ionization rate based on out previous analysis in Fig 4.15. When the gate voltage approaches the Vpo, however, the increase on lateral electric field dramatically raises the impact ionization rate. Nevertheless, Impact ionization rate drops in the vicinity of pinchoff voltage because J is extremely low at this time.

To minimize impact ionization rate, electric field should be suppressed in priority according to the analysis above. When J, a and b are fixed, the only method in reducing impact ionization is hence suppressing the electric field in the CDZ. Considering that the voltage must be dropped somewhere to meet voltage boundary conditions, an effective method is to distribute voltage drop more evenly across the CDZ. For example, in a device with drain access region shorter than the required length of a fully extended CDZ, the peak electric field will come out higher, which leads to a much more harsh impact ionization. However, when

the drain access region is longer than the CDZ, the extra length does not help in lowering the peak electric field because the DNZ occupies the extra part in the drain access region. Another possible method includes modulating the passivation charge which may change the positive sheet charge, and hence bring in a lower slope of lateral electric field, which makes the CDZ longer and peak electric field lower as a result. There are other fabrication methods such as field plates [4] [11], which actually follows the same idea to lower peak electric field by better utilize the length of drain access region in voltage dropping.

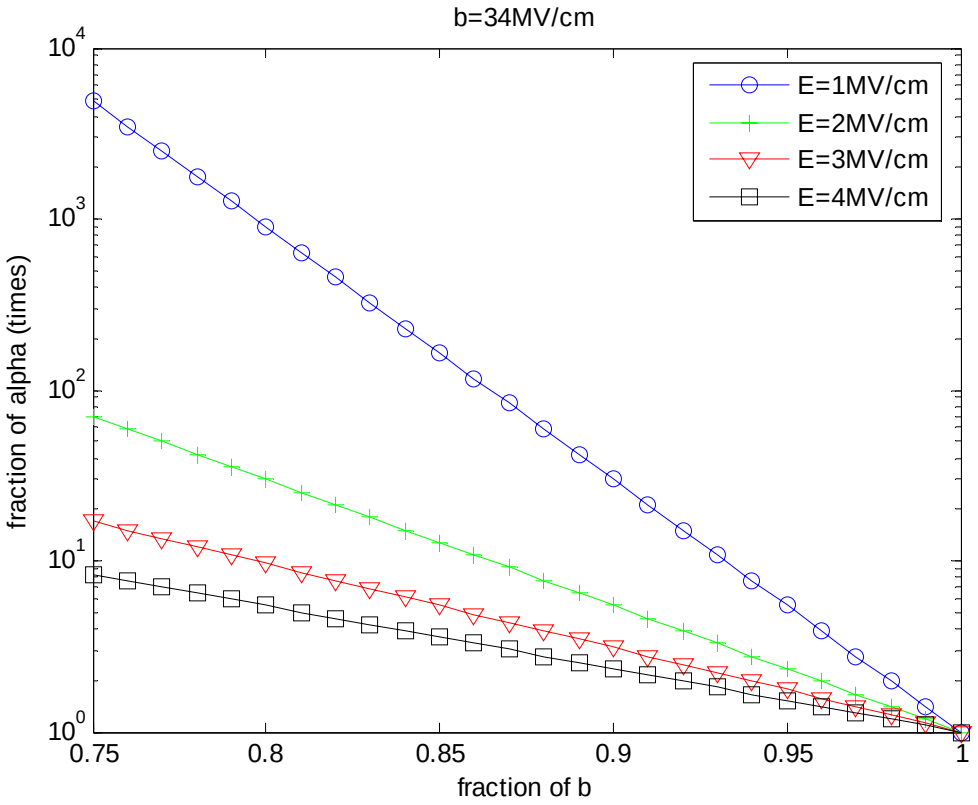

Fig 4.15: Impact of b on impact ionization ratio alpha, which is proportional to impact ionization rate G.

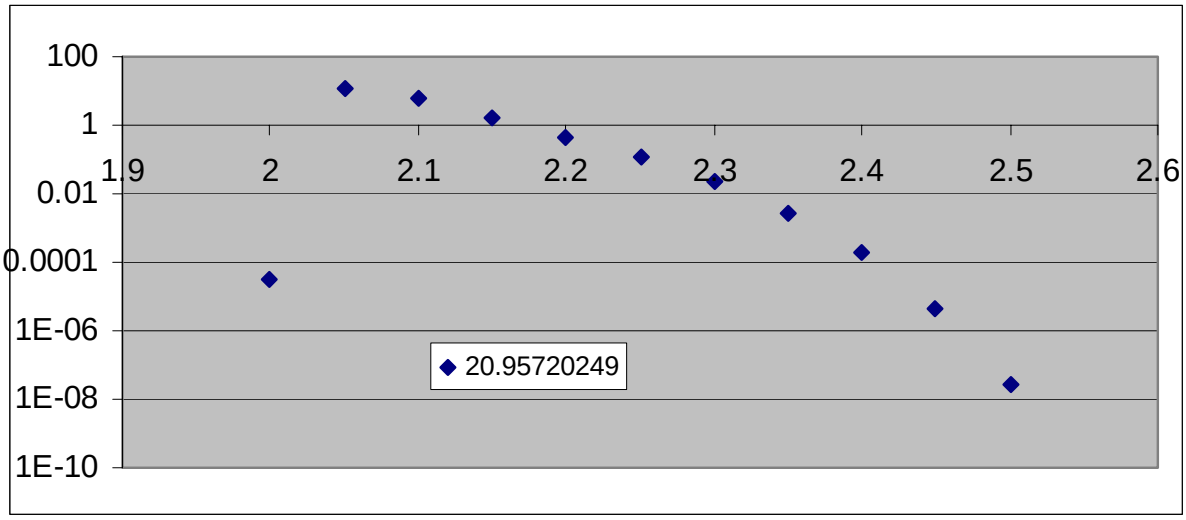

Fig 4.16: Impact Ionization generation rate in a 0.05-micron-long mesh along the channel at 1 nm beneath the AlGaN/GaN interface at operating point Vd=100V, Vg=0V. X axes is the distance from source electrode in microns (drain-side gate edge is at x=2 microns). CDZ starts from the situs x=2um.

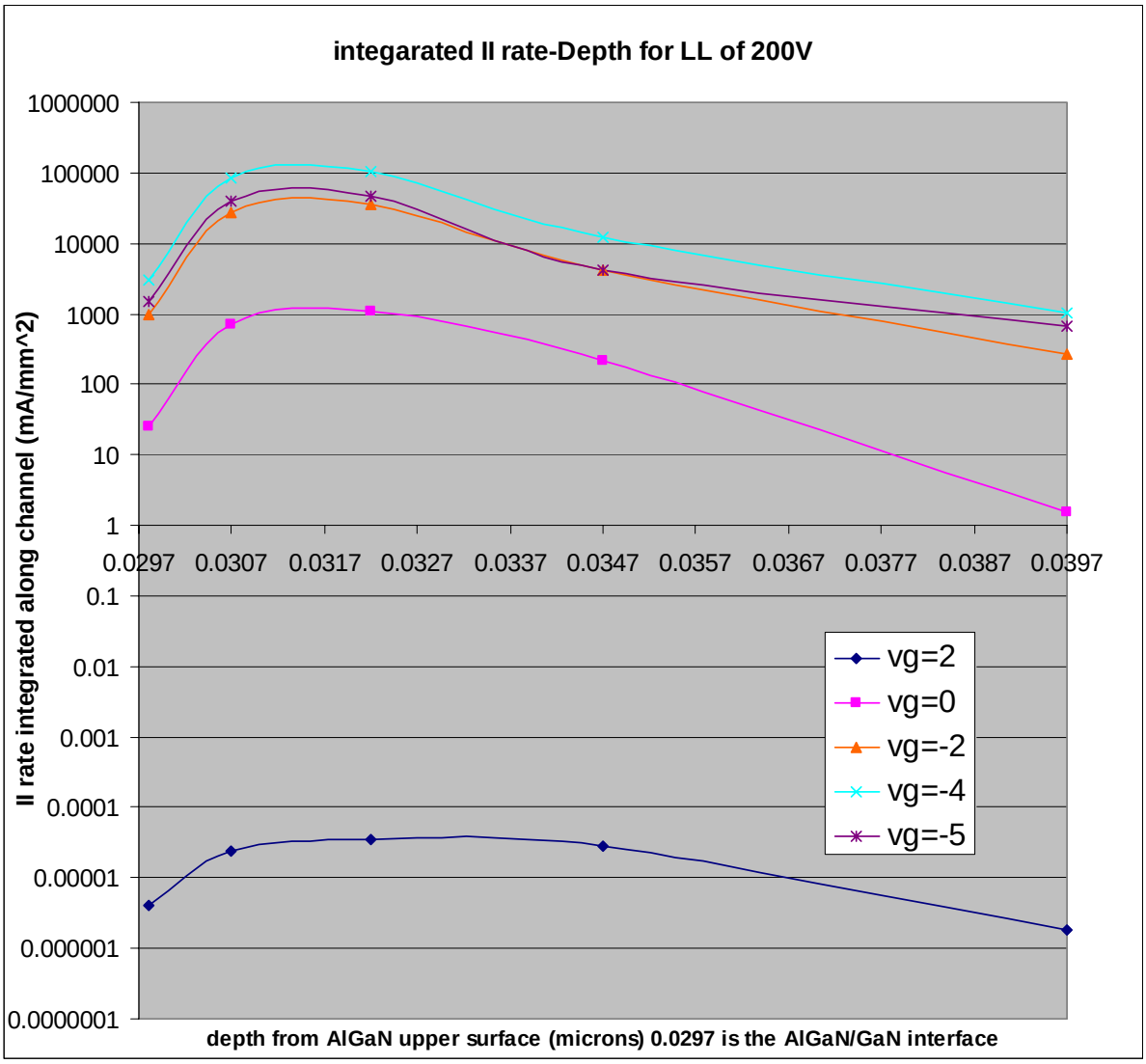

Fig 4.17: Impact ionization gate in meshes on depth direction. X axes is the distance from upper surface of AlGaN layer, which is 0.0297 microns in thickness. Operating points are along a 200V and 1.6A/mm load lines.

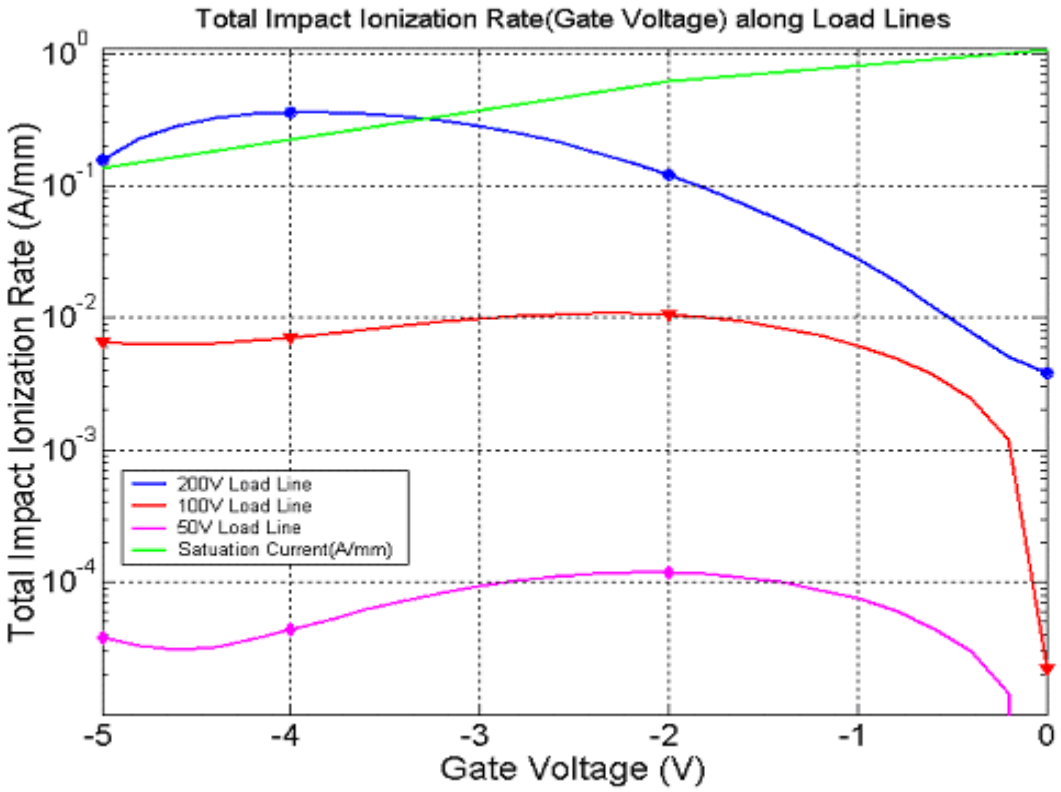

Fig 4.18: Impact ionization rate in an AlGaN/GaN HFET with bulk GaN doping: n-type, 1e17 cm^{-3}. Along Load Lines of 200V and 1.6mA/micron; 100V and 1.6mA/micron; 50V and 1.6mA/micron The applied Impact ionization model parameters are a = 2.9e8 cm-1 and b = 21.3 MV/cm

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CHAPTER 5

5.1 Model implementation and result

The current continuity equation defines that the divergence of the current density is equal to the negative rate of change of the charge density.

$$\nabla \cdot J = -\frac{\partial \rho}{\partial t}$$

In an AlGaN/GaN HFET, the charge density at any position is independent of time. Therefore, current is continuous everywhere in the device.

On the other hand, Gauss's law

$$\nabla \cdot D = \rho$$

determines that lateral electric field is continuous because there is no vertical cross section that has a non-zero area density of electron charge. In the vertical direction, however, the positive polarization charge is a sheet charge with a non-zero area density of electron charge n_{ss} and n_{po}. This results in a discontinuity of the vertical electric field at the AlGaN/GaN interface. This discontinuity is throughout the whole AlGaN/GaN interface in all zones from source to drain. This phenomenon is confirmed by ATLAS simulation. Figs 5.1 to 5.5 show this in the SNZ, IFZ, SLZ, CDZ and DNZ, respectively. Moreover, in these five figures, we notice that the discontinuity in Ey keeps the same value around 1.4e6 V/cm in all five zones. This comes from

$$\Delta E_y = \frac{q}{\varepsilon}(n_{ss} + n_{po})$$

Which gives

$$1.4\times10^{6} V/cm \approx \frac{1.6\times10^{-19} C}{10.4\times8.85\times10^{-14} F/cm}\times 8.04\times10^{12} cm^{-2}$$

In the lateral direction, however, no such sheet charge exists. Hence lateral electric field is continuous everywhere in the device. Voltage which is the integral of electric field on a certain path,

$$V = -\int_{path\ l} E \cdot dl$$

is always continuous because electric field is finite everywhere.

In this model, voltage and current continuities are strictly enforced and work as the boundary conditions connecting neighboring zones. Meanwhile, lateral electric field is set to be continuous in some cases as well, which will be explained in detail in the following section. However, the continuity of electron concentration and velocity along the channel is violated under certain circumstances. The reason is that there are short transition regions between certain pairs of zones, as an example, the SNZ and IFZ. Electron concentration and velocity change gradually between these transition regions [1]. This can be observed in Fig 2.4 and Fig 2.5. Actually, the other must change when one of these two terms changes because the product of these two, the current, is set to be continuous everywhere. The discontinuity of lateral electric field, which happens occasionally, is due to the lack of transition regions as

well. However, these transition regions are neglected in this model because they are short and the error introduced by them is negligible.

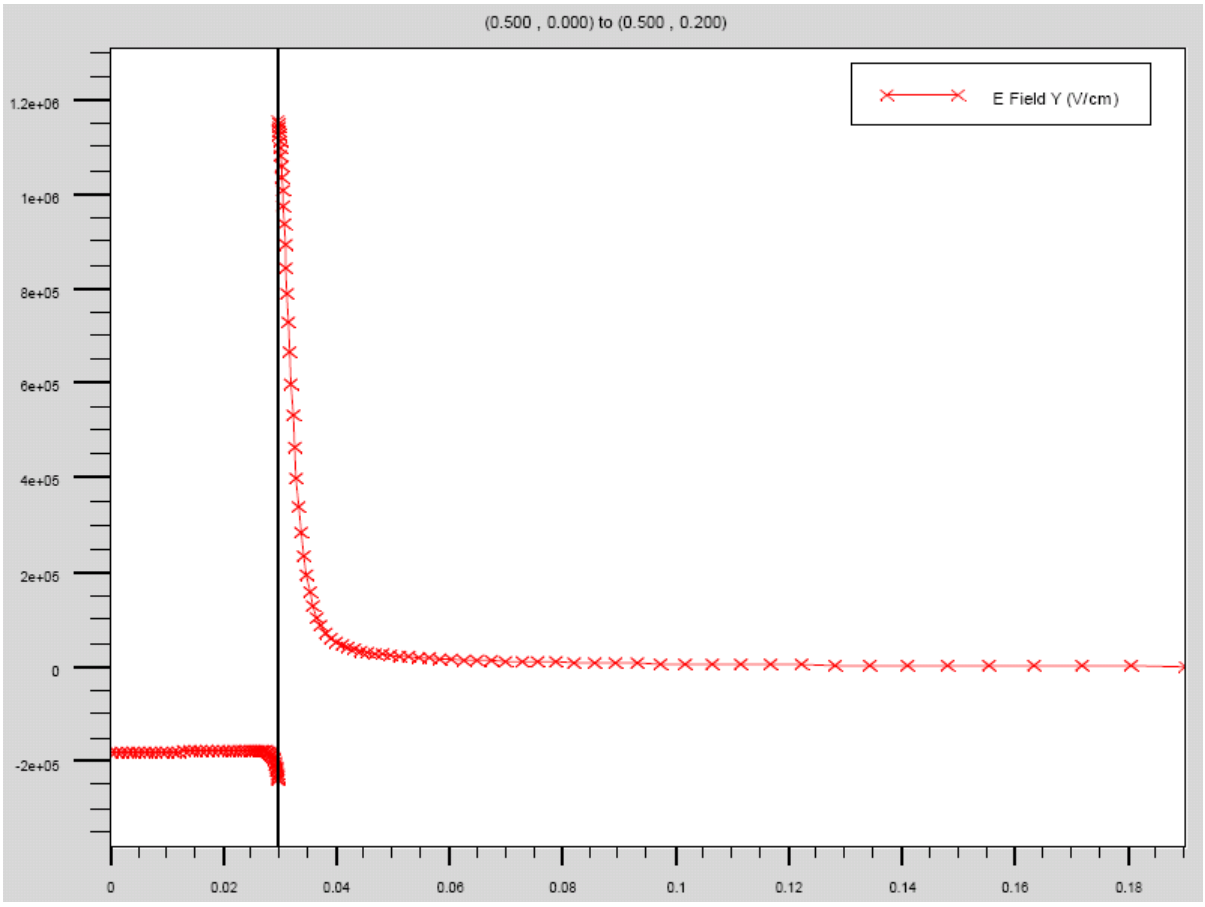

Fig 5.1: Ey in vertical cross section in SNZ from upper surface of AlGaN to the device's bottom. The bold line is the AlGaN/GaN interface.

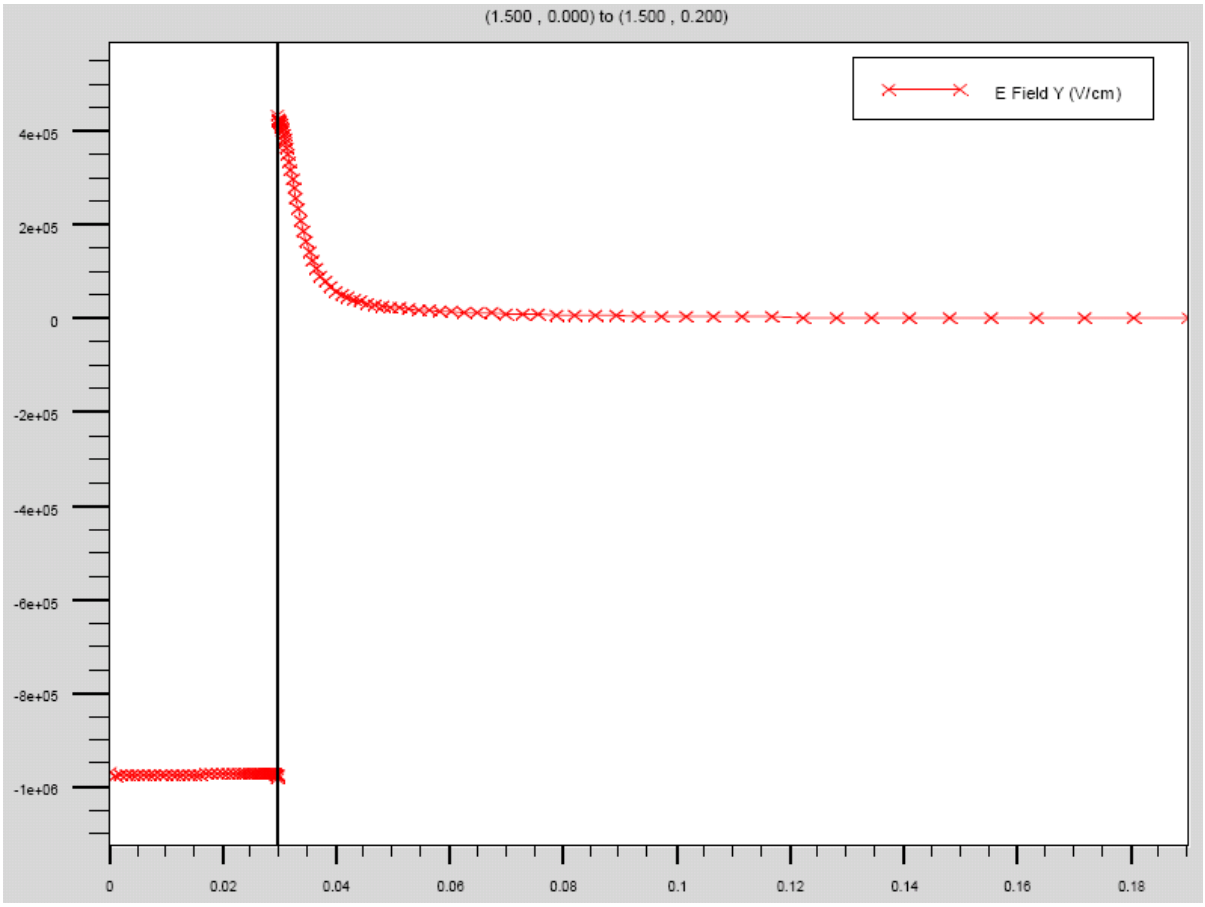

Fig 5.2: Ey in vertical cross section in IFZ from upper surface of AlGaN to the device's bottom. The bold line is the AlGaN/GaN interface.

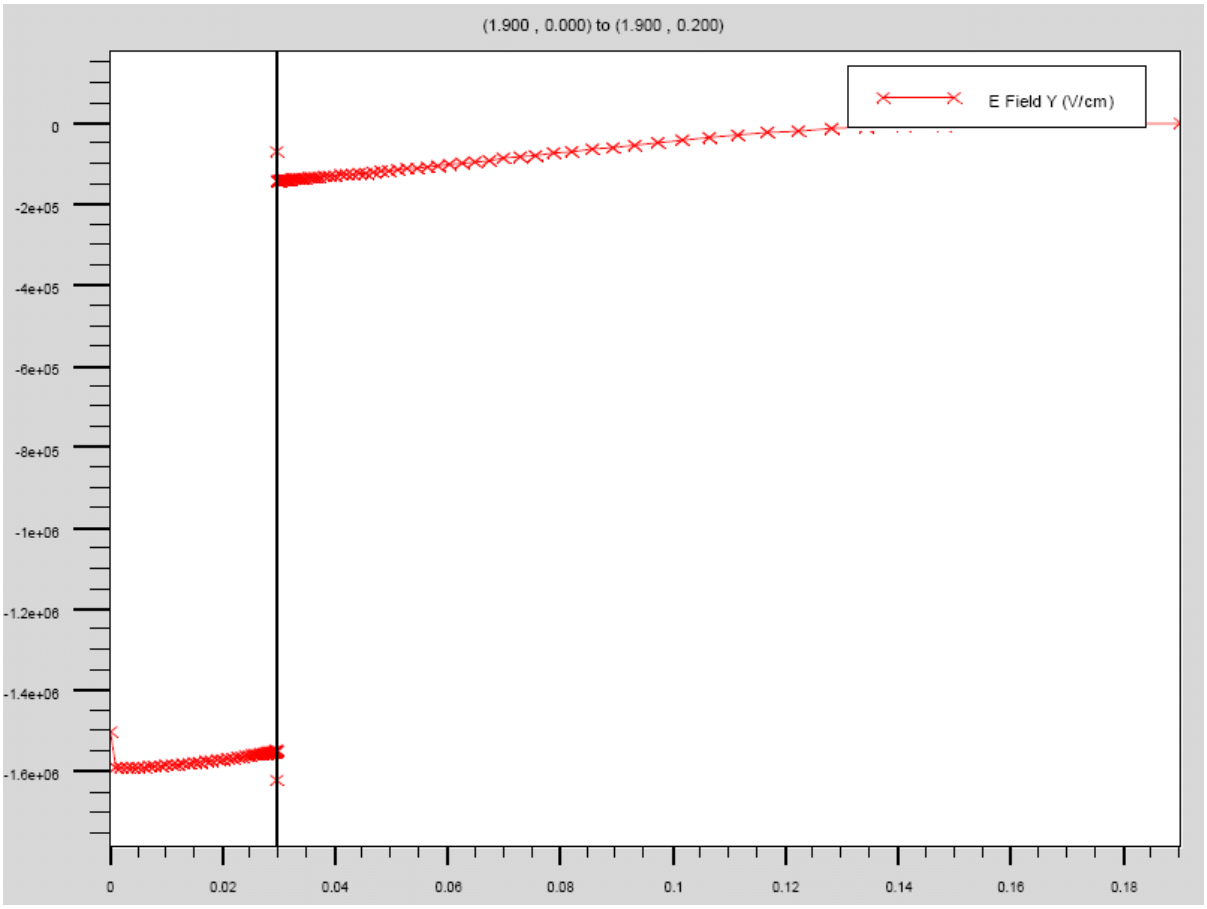

Fig 5.3: Ey in vertical cross section in SLZ from upper surface of AlGaN to the device's bottom. The bold line is the AlGaN/GaN interface.

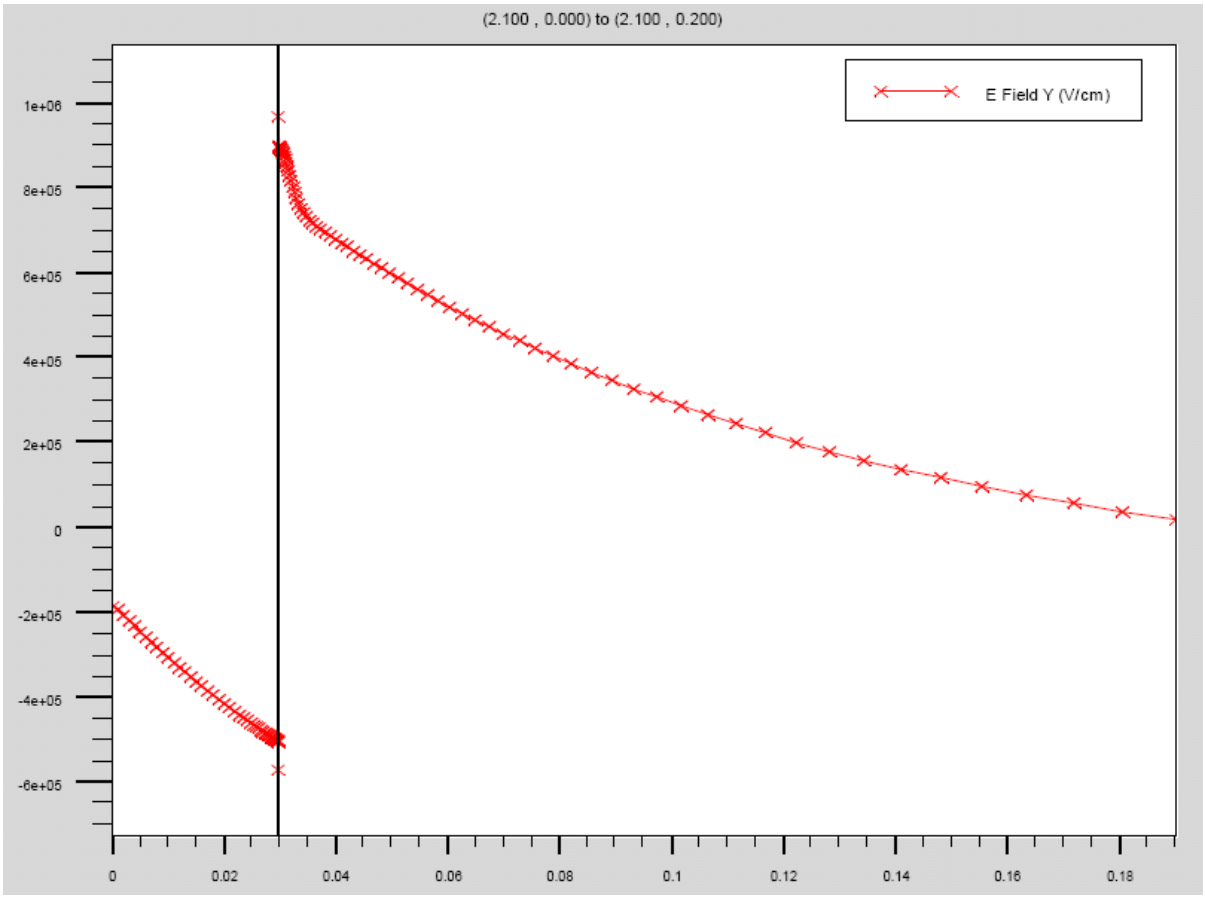

Fig 5.4: Ey in vertical cross section in CDZ from upper surface of AlGaN to the device's bottom. The bold line is the AlGaN/GaN interface.

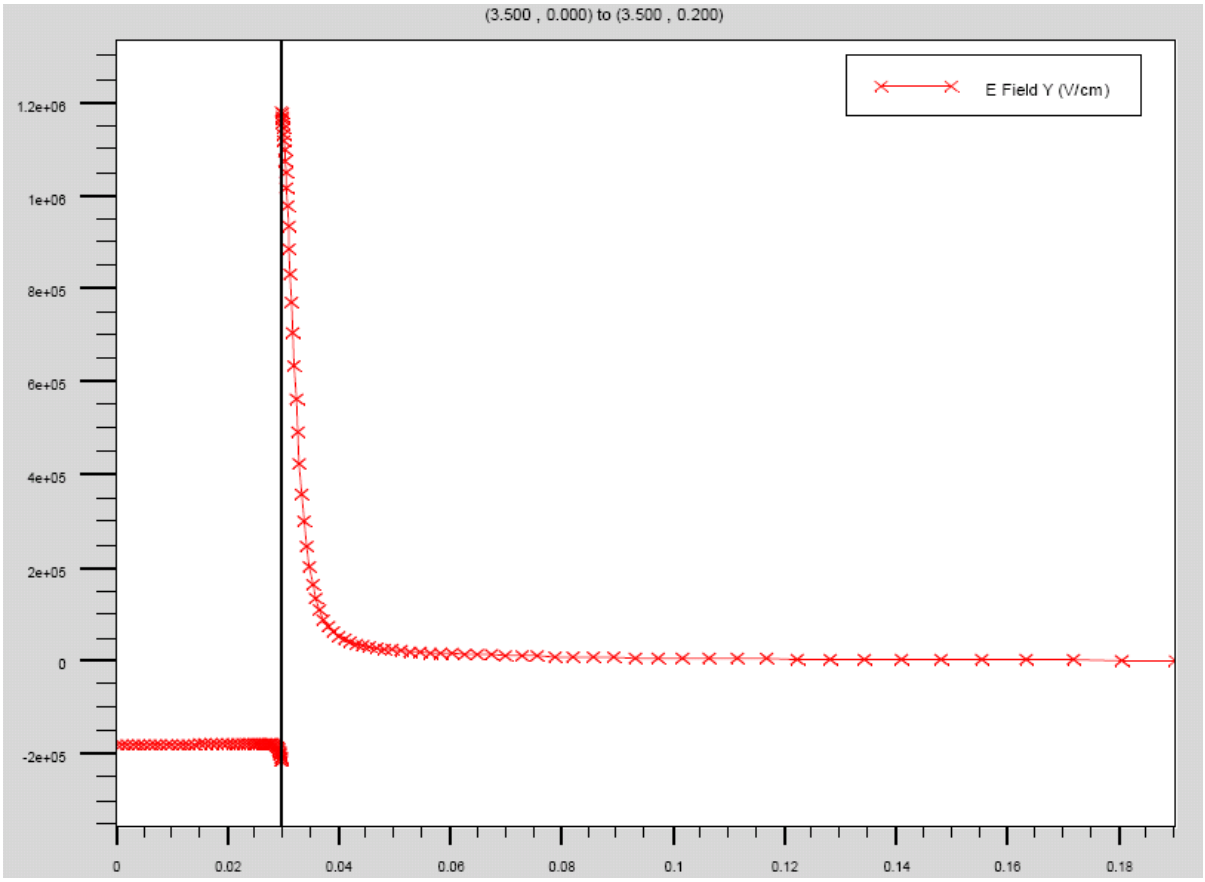

Fig 5.5: Ey in vertical cross section in DNZ from upper surface of AlGaN to the device's bottom. The bold line is the AlGaN/GaN interface.

5.2 DC model implementation

In chapter 3, we built up models for the SNZ and the DNZ. When the device works under triode operation, the GCA is going to be applied in the IFZ. All of the three zones present in triode operation, SNZ, IFZ and DNZ, are connected by voltage and current continuities. Therefore, according to the conclusions we made on non-linear resistances in chapter 3, we can readily determine the voltage dropped across either neutral zone as the product of the lateral electric field with the zone length. So, in the case of the "second order" velocity-electric field relation, the voltage

$$V_s = E_s l_s = \frac{E_c l_s I}{\sqrt{I_{sat}^2 - I^2}} = \frac{V_a I}{\sqrt{I_{sat}^2 - I^2}} \tag{5.1}$$

appears across the Source Neutral Zone. For a grounded source electrode, Vs is thus the voltage at the boundary of the Intrinsic FET Zone and the Source Neutral Zone. Similarly, in the Drain Neutral Zone, we have

$$V_D - V_d = E_d l_d = \frac{E_c l_d I}{\sqrt{I_{sat}^2 - I^2}} = \frac{V_b I}{\sqrt{I_{sat}^2 - I^2}} \tag{5.2}.$$

Here V_D is the voltage at the drain electrode, and Vd is the voltage at the boundary of the Intrinsic FET Zone and the Drain Neutral Zone. Equations (5.1) and (5.2) are the origin of non-linear source and drain resistances in circuit models as stated and proven in chapter 3. In the Intrinsic FET Zone, the gradual channel approximation gives

$$\frac{I}{\beta}-\frac{1}{2}\left[\left(V-V_{gt}\right)\sqrt{\left(V-V_{gt}\right)^2-\left(\frac{I}{\beta V_l}\right)^2}\right]_{V_s}^{V_d}+\frac{1}{2}\left(\frac{I}{\beta V_l}\right)^2\ln\left|\frac{V_d-V_{gt}+\sqrt{\left(V_d-V_{gt}\right)^2-\left(\frac{I}{\beta V_l}\right)^2}}{V_s-V_{gt}+\sqrt{\left(V_s-V_{gt}\right)^2-\left(\frac{I}{\beta V_l}\right)^2}}\right|=0 \qquad (5.3)$$

where $\beta = C\times\mu\times W/L$, C is the gate capacitance; μ is the electron mobility; W and L are usual gate dimensions. Because current is continuous throughout the channel, drain current I is at the same value in all three zones. Meanwhile, the continuity of voltage requires that voltages dropped across all these three zones add up to the drain bias V_D. Therefore, after determining the pinch-off voltage, we simultaneously solve Equations (5.1), (5.2), and (5.3) to get the desired relation between drain terminal voltage V_D and drain current I. This result for another device with a similar structure [2] is shown in Fig 5.6 along with the ATLAS simulation results for comparison. Significantly, Fig 5.6 uses no adjustable parameters, but only the same geometric and material design parameters used in ATLAS. This method is also applicable, for this case of the general pth-order velocity-field curve, the following three equations

$$\int_{V_s}^{V_d}\sqrt[p]{\left(V_{gt}-V\right)^p-\left(I/\beta V_l\right)^p}\,dV = I/\beta \qquad (5.4)$$

$$V_s = E_s l_s = \frac{E_c l_s I}{\sqrt[p]{I_{sat}^p - I^p}} = \frac{V_a I}{\sqrt[p]{I_{sat}^p - I^p}} \qquad (5.5)$$

$$V_D - V_d = E_d l_d = \frac{E_c l_d I}{\sqrt[p]{I_{sat}^p - I^p}} = \frac{V_b I}{\sqrt[p]{I_{sat}^p - I^p}} \qquad (5.6)$$

are solved numerically to get the I-V expression for the HFET. Hence, the current and voltage continuities are sufficient in determination on DC IV characteristics for a device under triode operation.

With increasing drain voltage , the device finally reaches the saturation operation mode. This threshold point is determined by the method which was introduced in chapter 2. Beyond this point, the device has 5 zones. At any drain voltage more than the threshold value, the derivative of lateral electric field can be calculated from corresponding expressions in chapter 4. As explained in chapter 4, the derivative of lateral electric fields in the SLZ and the CDZ are approximated considered constant. Hence the lateral electric fields in the SLZ and CDZ are linear. The boundary condition between the IFZ and the SLZ is that Ex is equal to Ec, as proven in chapter 2. The boundary condition between the SLZ and the CDZ is that Ex is continuous at this point. The boundary condition between the CDZ and the DNZ is that Ex in the CDZ drops to the Ex level in the DNZ, which is also a function of drain current. Meanwhile, lateral electric fields in the SNZ and the DNZ are functions of drain current just as they are in the device under triode mode. After determination of Ex in all zones, the voltage dropped across all zones can be related with drain current I. Afterwards, using a method similar to that in triode operation mode, we acquire the relation between drain bias and drain current, which can be solved numerically. The modeled DC IV characteristic for this 5-zone model is shown in Fig 5.7, together with which experimental and ATLAS

simulation data are shown for comparison. Again there is no adjustable parameters at all. The curves just fit naturally.

Please note that another difference between methods for devices under triode and saturation operation is the lengths of the IFZ and the DNZ. In triode operation, the length of the IFZ is fixed at the length of gate electrode. The length of DNZ is always equal to the length of drain access region. In saturation operation, the length of the IFZ is the difference between the length of the gate electrode and the length of the SLZ. The DNZ occupies the rest of drain access region after accommodating the CDZ. In an extreme case of a short drain access region, there may exist no DNZ at all as the CDZ would occupy the whole drain access region alone. These zones' lengths are proven to be a function of drain current as well. The boundary condition between the SLZ and the CDZ that Ex is continuous works out as the additional relationship from which the length-current relation can be derived. As an example, the length of SLZ with a second-order velocity-field curve is

$$l_3 = l_g - \frac{\beta l_g}{2I}\left[\left(V_{gt}-V_s\right)\sqrt{\left(V_{gt}-V_s\right)^2-\left(\frac{I}{\beta V_l}\right)^2}-\left(\frac{I}{\beta V_l}\right)^2\ln\left(\frac{\frac{I}{\beta V_l}}{V_{gt}-V_s-\sqrt{\left(V_{gt}-V_s\right)^2-\left(\frac{I}{\beta V_l}\right)^2}}\right)\right]$$

However, please note that the variable L_3 in the current code is the ratio of l_3 to l_g, which is a number from 0 to 1 since the length of the SLZ can never be greater than the length of gate electrode.

The boundary between the SLZ and the CDZ is actually where the peak lateral electric field happens. At the same time, the continuity of lateral electric field at the boundary between the IFZ and the SLZ, and at the boundary between the CDZ and DNZ relates current with the lengths of the CDZ and the SLZ as well. In other words, continuity of lateral electric field is an additional continuity besides the voltage and current continuities while in saturation operation. As a conclusion, we developed a method to determine the DC IV characteristic of an AlGaN/GaN HFET under both triode and saturation operation modes.

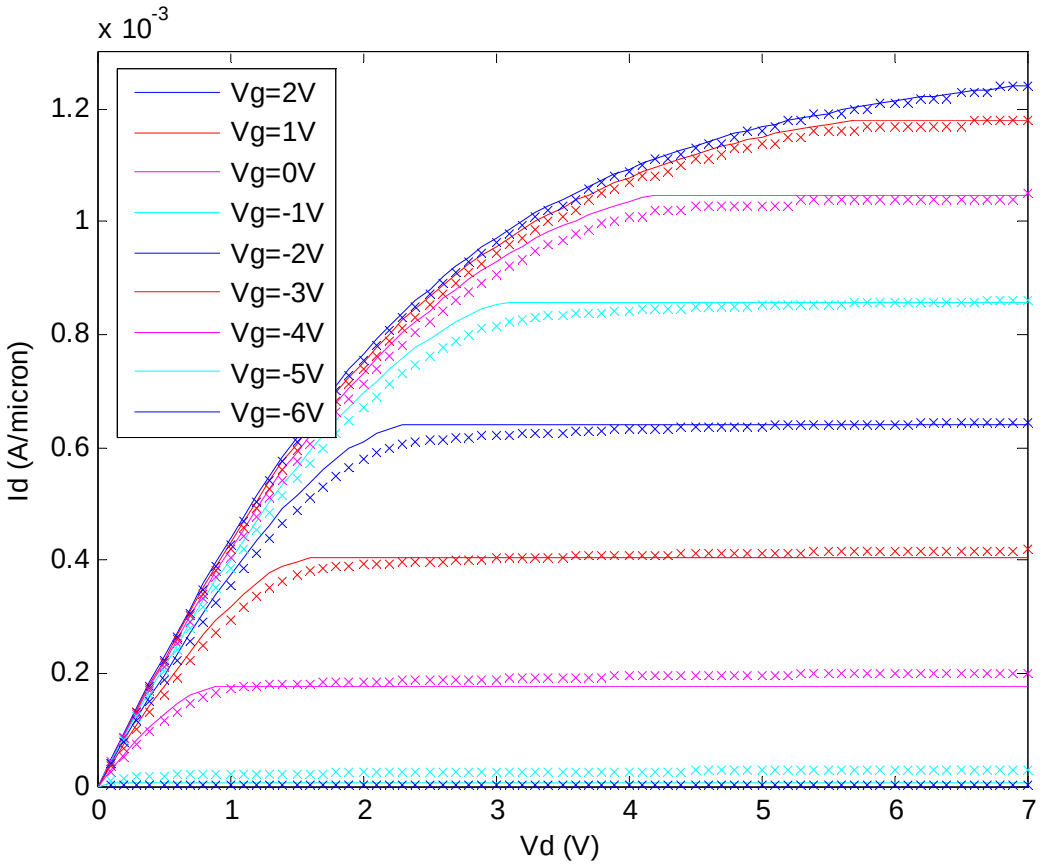

Fig 5.6: I-V characteristic of an AlGaN/GaN HFET with similar structure. The pinchoff voltage in this device is -5.15V, which can be determined by pinchoff expression in chapter 2. Crosses are ATLAS simulation data. Solid lines are the model result.

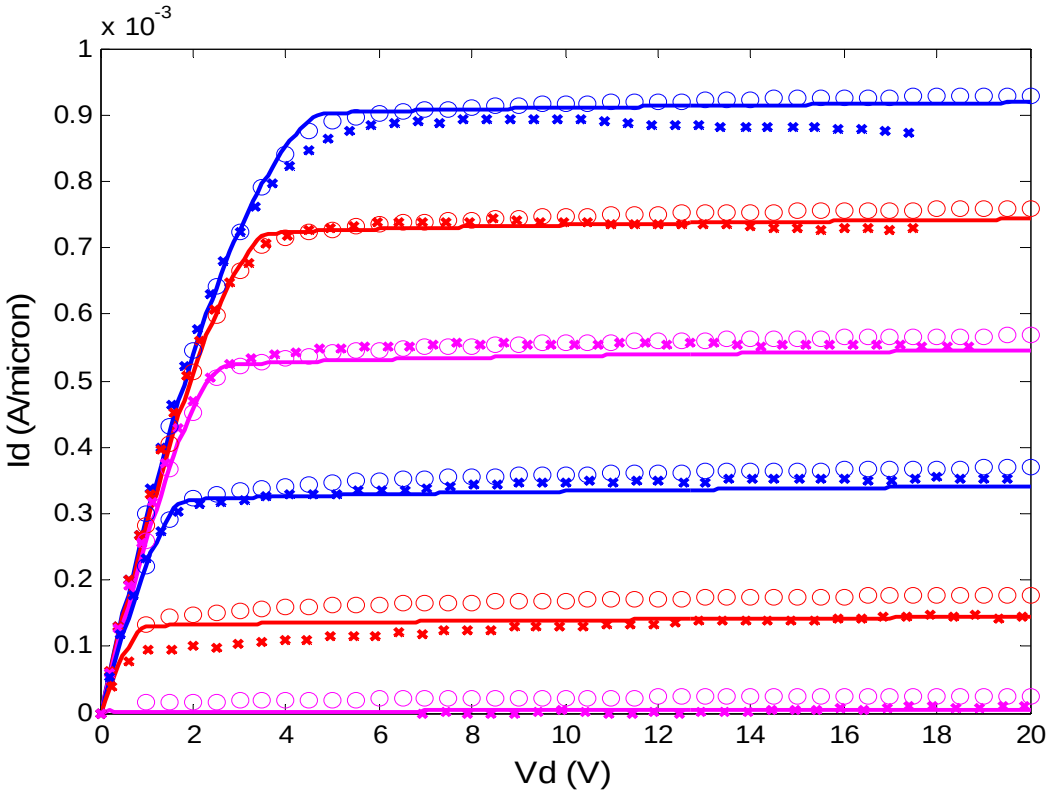

Fig 5.7: DC I-V characteristics for an AlGaN/GaN HFET. CROSSES: Experimental measurements. CIRCLES: ATLAS simulation data. SOLID LINES: the new complete model result.

5.3 Small and large signal components

After acquiring drain current, the transconductance, gm, and conductance, gd, are available through derivatives of drain current on gate and drain bias. Modelled and simulated transconductances are shown in Fig 2.10.

Other than conductance and transconducatance, charges are another important component required in the equivalent electric circuit. Since the DC module provides us a complete physical view of this device we can easily evaluate the charge control model. The charges are determined based on their physical nature in this model. In the SNZ and DNZ, electron density is always equal to the positive polarization charge density at the AlGaN/GaN interface. The amount of these charge densities are always the same since electrons in the SNZ and the DNZ never reach their saturation velocity. Different current injection levels only change the electrons' speed while traveling across these two zones. Therefore, charge densities in the SNZ and the DNZ are constant throughout the whole operational IV plane. However, the length of the DNZ is a variable when the device is in saturation mode. The charge in the DNZ can not be treated as a constant although the charge density in the DNZ is a constant. In the SNZ, the constant zone length fixes the charge in the SNZ at a constant level. The amount of charge in the IFZ is changing due to varying electron velocity in this zone. Under triode operation, different gate and drain bias offers the IFZ different boundary conditions, which modulates the amount of charge collected by the gate. Under saturated operation, the length of the IFZ is added in as another variable. Whichever mode it is, the DC

module provides us all the information needed for an integral across the whole IFZ, which was introduced in the previous section. Hence the total charge under the gate electrode can be easily integrated. The charge in the SLZ is driven by the drain electrode only because no electric field lines emitting from these charges are collected by the drain electrode. Vertical electric field is zero at the virtual oblique line in the GaN dividing the upper depletion region and the lower neutral region where electrons are traveling. In the CDZ, some electric field lines emitted from positive polarization field sheet charge are screened by the electrons traveling in the channel. However, there must be some excess electric field lines because electron density is less than the positive sheet charge density in the CDZ. These excess field lines end at the drain electrode. Besides, the ionized dopants in the depletion region emit field lines too since they also have positive charge. However, this portion of field lines' source is negligible since the bulk GaN has a very low doping level. Due to the high electron velocity in the SLZ and the CDZ, charges in these two zones can be evaluated easily as well from the drain current and lengths of these zones. All these charges can be calculated at all combinations of gate and drain bias.

Because the charge in the SNZ keeps constant as demonstrated previously, the charges in the IFZ, SLZ, CDZ and DNZ are considered to be all of the charge components in this device. The charge in the IFZ is regarded as part of gate charge Qg. The charge in the SLZ is considered as part of drain charge Qd. The charge in the CDZ and DNZ is defined as a portion shared by Qg and Qd. In other words, Qg consists of charges in the IFZ, CDZ and

DNZ, and Qd comprises charges in the SLZ, CDZ and DNZ. A fact of these charge components is that the charge in the SLZ is usually less than the charge in the CDZ. Also the charge in the CDZ and DNZ is normally less than the charge in the IFZ. That is, the charge in the IFZ usually dominates in Qg and the charge in the CDZ and DNZ usually dominate in Qd.

In the current stage, capacitances needed in the capacitance matrix are then determined by partial derivatives of these charges. After determination of all charges and capacitances, they are provided to the RF module, together with other values previously derived from DC IV, by means of building up lookup tables which feed the large-signal simulator, in this project, TEFLON. An example is that C_{dd} is the derivative of Qd on Vd, whose comparison between modeled and simulated results is shown in Fig 5.8 and Fig 5.9 for different bulk GaN doping levels. The expression of Cdd is

$$C_{dd} = \frac{\partial Q_d}{\partial V_d} = \frac{\partial}{\partial V_d}\left(Q_{CDZ} + Q_{DNZ}\right)$$

Where Q_{CDZ} is the charge in the CDZ and Q_{DNZ} is the charge in the DNZ. Q_{CDZ} is modulated by the electron density in the CDZ, which is a function of drain current. Meanwhile, Q_{CDZ} is also dependent on the length of the CDZ, which is a function of drain current and drain bias. The details of this expression can be found in chapter 2, which focuses on the CDZ's model. Q_{DNZ} is only a function of the DNZ's length, which is the leftover of the length of drain access region from the length of the CDZ. Hence the capacitance comes out as

$$C_{dd} = \frac{\partial}{\partial V_d}\left\{\left[q \times \left(n_{ss} + N_{AlGaN} \times t_a + N_{GaN} \times t_g\right) - \frac{J_d}{v_{sat}}\right] \times l_{CDZ} - q \times n_{ss} \times L_d\right\}$$

Where L_d is the length of drain access region and l_{CDZ} is the length of CDZ.

Fig 5.10 shows a large-signal equivalent circuit proposed for commercial circuit simulators, such as ADS and Microwave Office. This equivalent circuit is ready for coding in C or Verilog-A. All major components in this circuit are descirbed in this dessertation. Other compoents such as gate leakage are described in the chapter on future work.

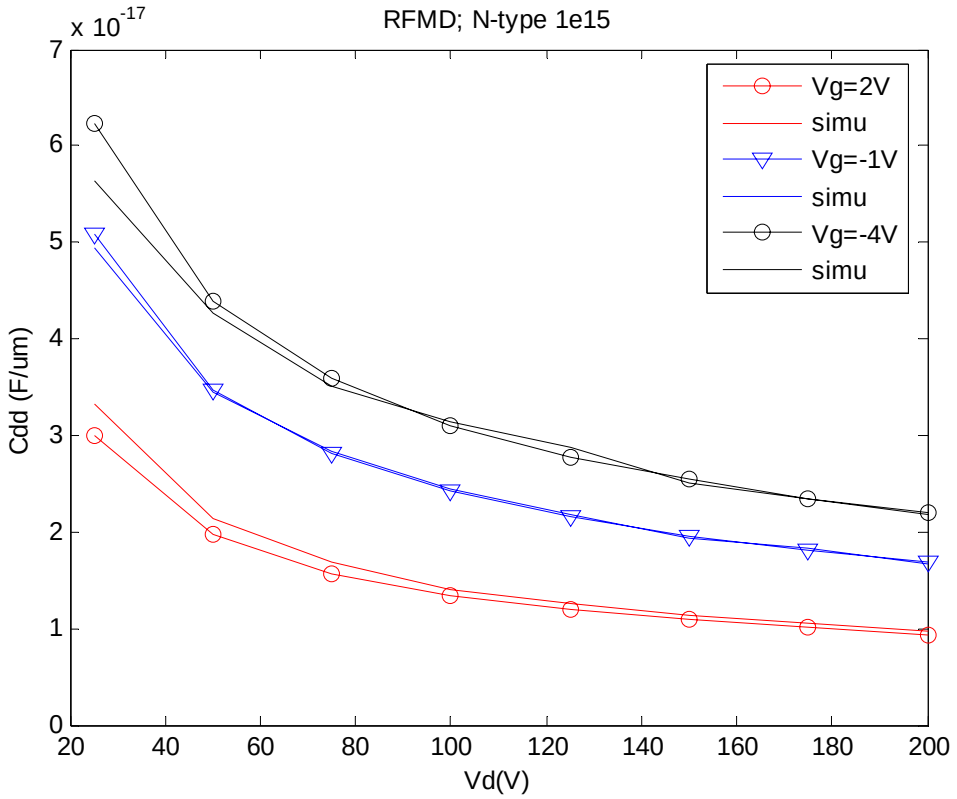

Fig. 5.8. Modeled and simulated C_{dd} of an AlGaN/GaN HFET with a background doping of 1e15^cm^{-3}

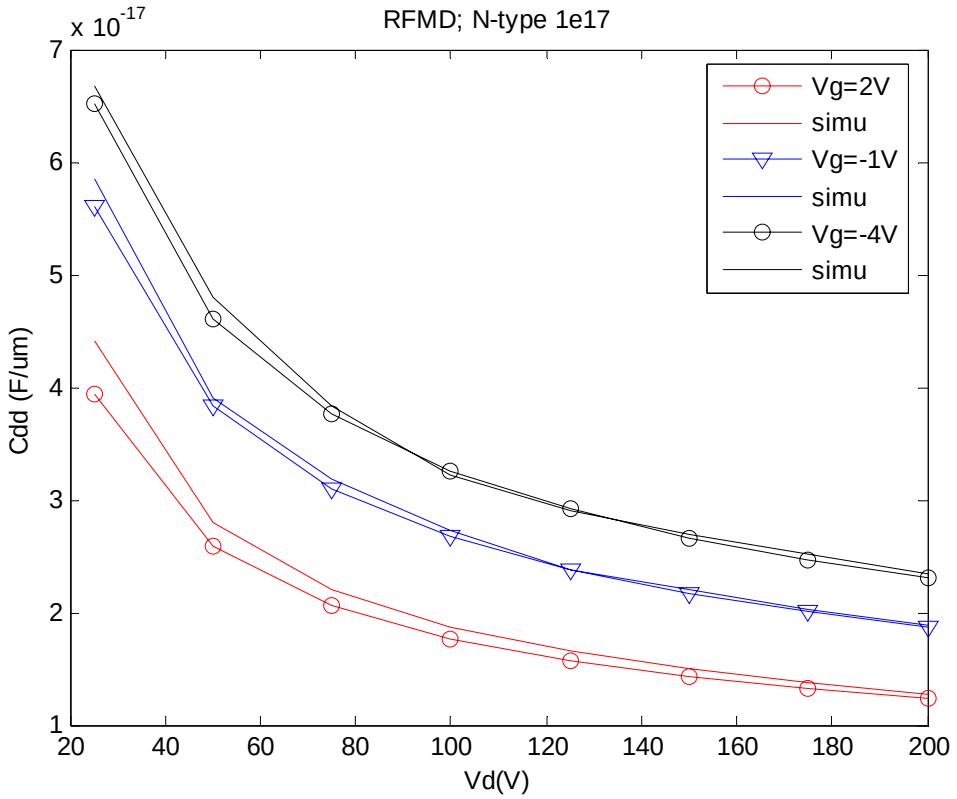

Fig. 5.9 Modeled and simulated C_{dd} of an AlGaN/GaN HFET with a background doping of 1e17^cm^{-3}

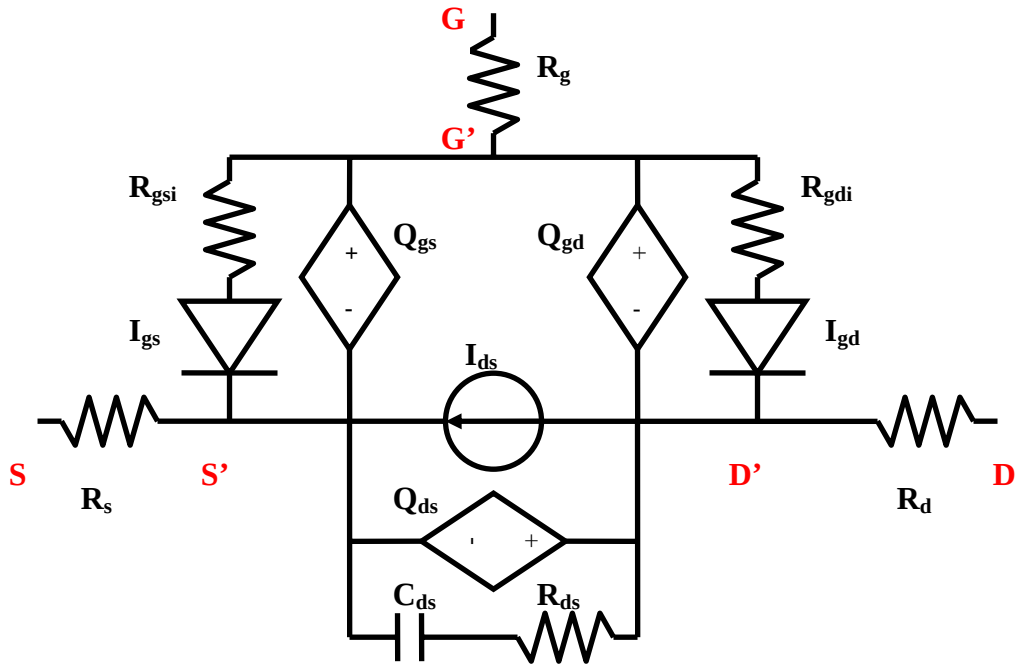

Fig 5.10 Proposed large-signal equivalent electric circuit of this model, ready for C and/or Verilog-A, and integratable in commercial simulators, such as ADS/Microwave office

5.4 Large signal simulation and result

The current RF module of this large-signal model is based on TELFON, our harmonic-balance circuit simulator. The small and large signal equivalent circuits employed by TELFON are shown in Fig 5.11 and Fig 5.12 [3]. Components in these figures can be evaluated from our DC module independently and physically. The new model is also ready to be integrated into any commercially available harmonic balance simulator that permits user defined device models. Teflon was originally designed to produce a lookup table during an initial DC simulation, and later use it for the large signal RF simulation. In the present effort, the lookup table is generated from the HFET DC module described in the previous section. Drain current, transconductance, conductance, charges controlled by gate and drain electrodes, and large signal capacitance matrices are calculated and tabulated as functions of gate and drain voltages. These tables are used in a harmonic balance circuit simulation to predict large signal RF operation.

Simulated and measured RF performance at 2.14 GHz of the industrial HFET with a gate width of 0.4-mm is shown in Fig. 5.13. The device was biased for class A-B operation at drain voltage of 28 V. Seven harmonics are used in the harmonic-balance routine. The simulated RF performance, including gain, output power and power-added efficiency (PAE) coincide with the experiment data. The DC drain current in the large signal equivalent circuit follows the measured data closely as well, which is shown in Fig 5.14. Dynamic load lines' shift toward high voltage values with increasing input power also indicates the nonlinear

increase in resistance at varying input power levels [4], which is shown in Fig 5.15. Distortion is notable at the right bottom corner with increasing RF power level while the AlGaN/GaN HFET is driven under class AB operation. (nodes are in red, components are in black)

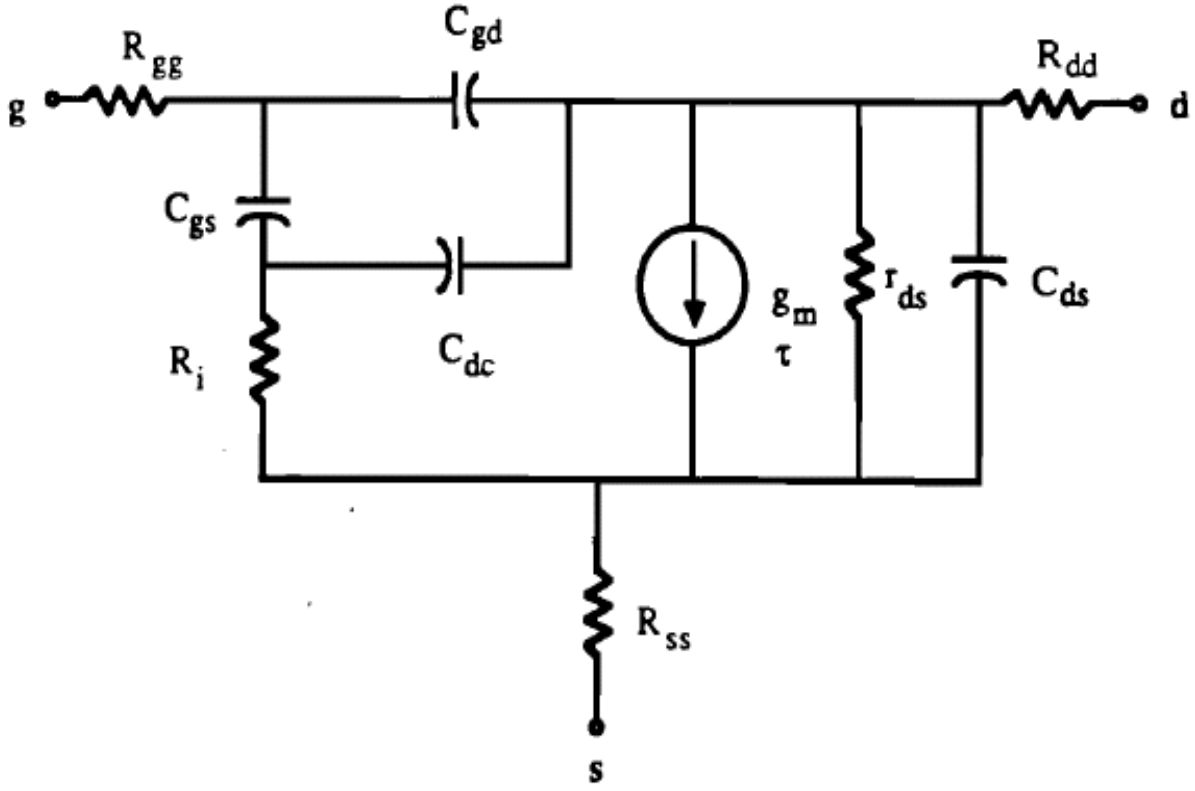

Fig 5.11: Small signal equivalent circuit in TEFLON

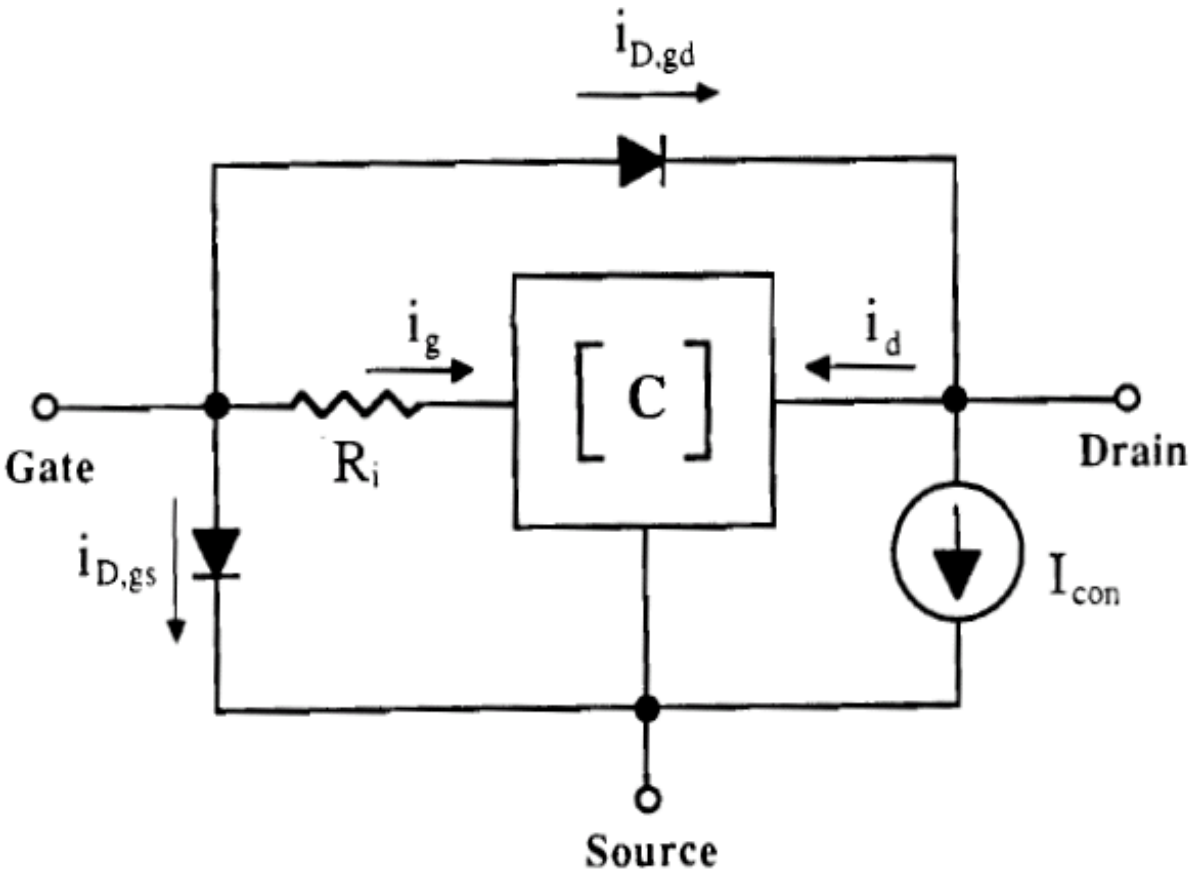

Fig 5.12: Large signal equivalent circuit in TEFLON

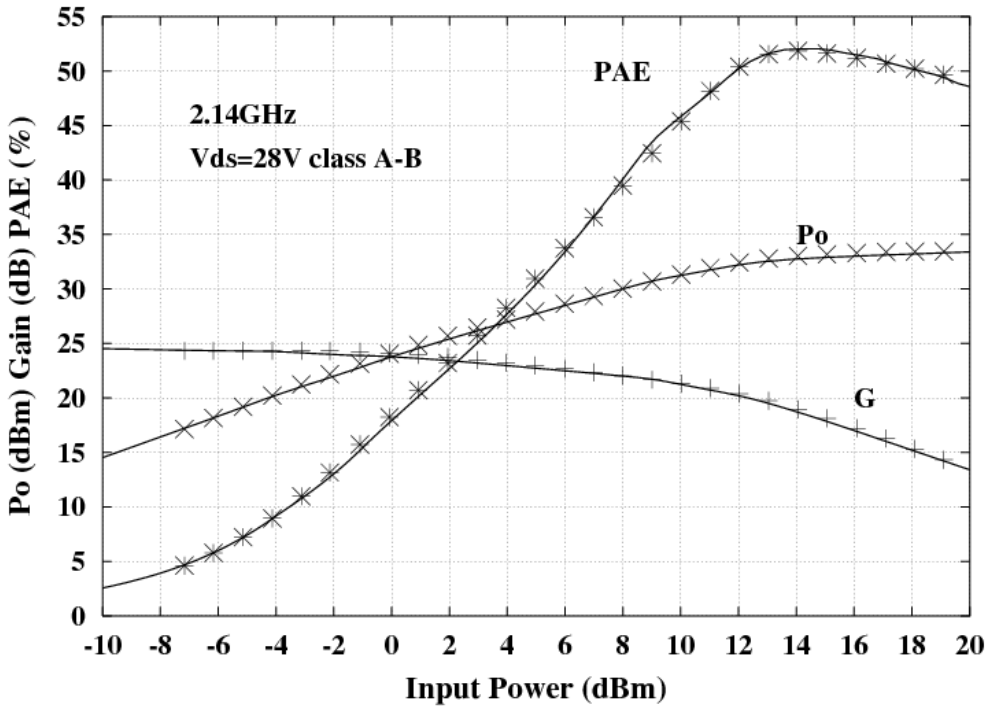

Fig 5.13 Simulated and measured RF performance versus input power for the AlGaN/GaN HFET amplifier at 2.14GHz(points: measured data, solid lines: simulated data; Vds= 28V Class AB).

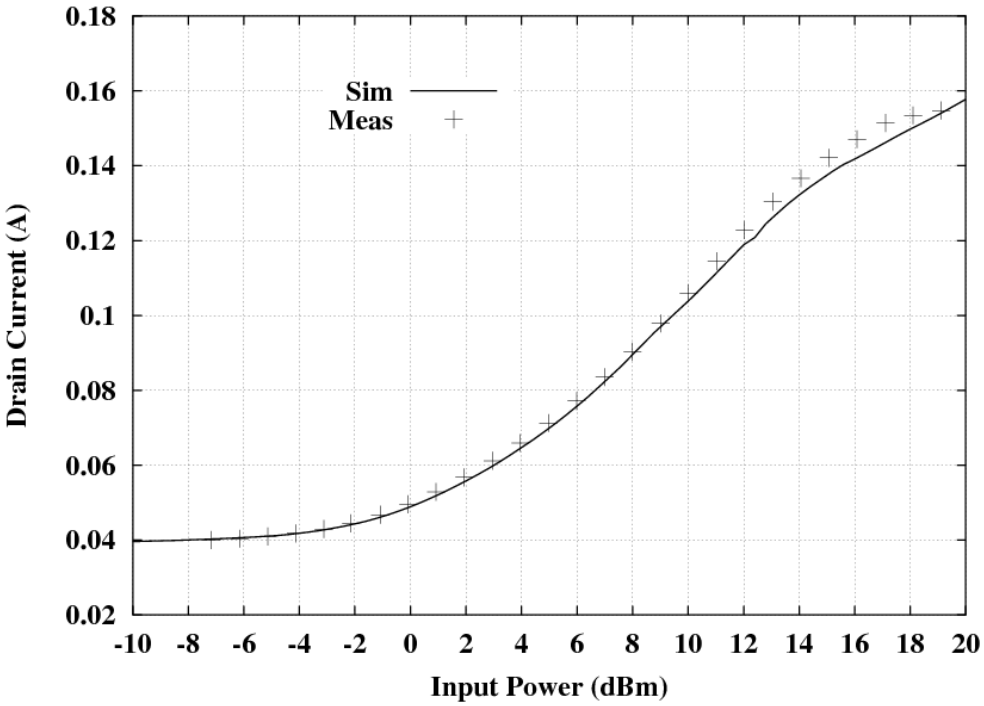

Fig. 5.14. Simulated and measured DC drain current versus input power for the AlGaN/GaN HFET amplifier at 2.14 GHz (Vds=28V, Class AB)

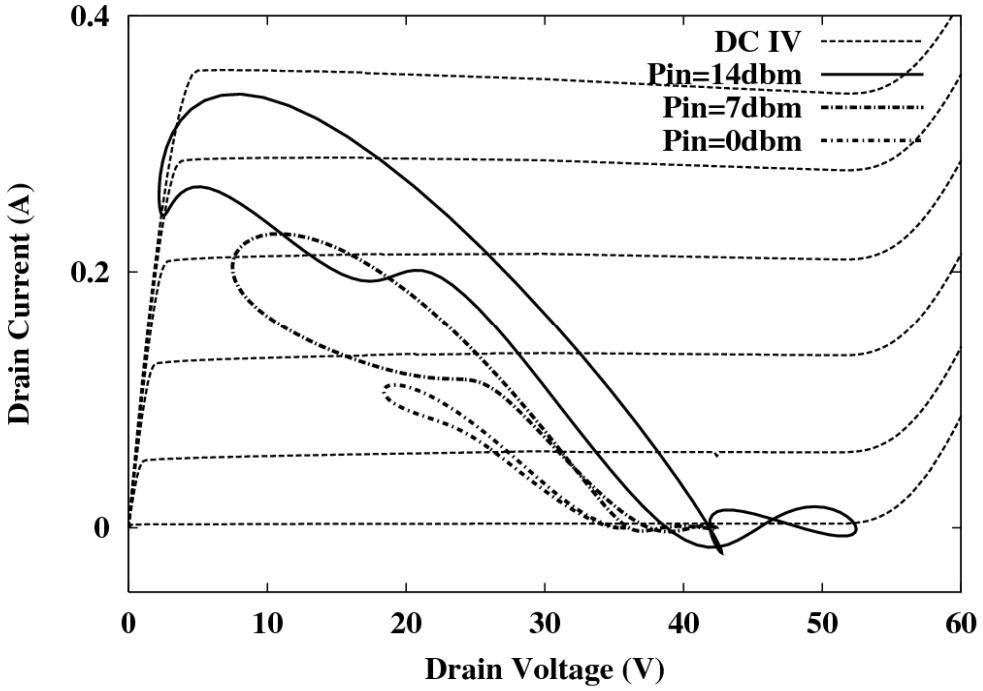

Fig. 5.15 Dynamic Load Line at Pin=0,7 and 14 dbm superimposed upon DC at 2.14 GHz (Vds=28V, Class AB)

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CHAPTER 6

6.1 Conclusions

In this project, our complete physics-based DC and large-signal RF simulator for AlGaN/GaN HFETs is described in detail. The model includes a DC device module and an RF module of a large-signal circuit simulator. The flowchart of this project is shown in Fig.1.6. The DC module is physics-based and correctly accounts for several different kinds of carrier transport appropriate to the physics of the corresponding zones. These zones are discussed, modeled, solved, and verified separately, and then combined with appropriate boundary conditions. Models of nonlinear resistances, space-charge transportation and charge-deficit transport are presented qualitatively and quantitatively. The resulting analytic DC IV curves are shown to agree well with experimental data from an industrial AlGaN/GaN HFET. These modeled DC IV curves and transconductance curves are also shown to compactly predict ATLAS two-dimensional simulation results accurately without the need for any adjustable fitting parameters. The new model depends only on basic device structural dimensions, material properties, and impurity doping information.

Besides drain current, transconductance and conductance; charges and capacitances are evaluated by the DC module in terms of their physical nature as well. The RF module then uses these quasi-static values generated by the DC module to produce large-signal RF simulations. The RF large-signal simulation results are also shown to agree well with

experimental data. Moreover, this compact AlGaN/GaN HFET model is computationally efficient enough to be integrated into any harmonic-balance simulator that allows user defined device models. Since the HFET model does not require a priori calibration to experimental data, the new model can be used for device design optimization investigations as well as circuit design applications.

Specifically, nonlinear resistances in the source and drain access regions are investigated by dividing an AlGaN/GaN HFET under triode operation into three zones. Under triode operation, the zone division is illustrated in Fig 2.1. A model is built considering the velocity-field curve as the key factor of the nonlinearity. This nonlinear resistance model is tested at different operating points and with various fabrication structures. Based on this nonlinear resistance model, a physics-based compact model for AlGaN/GaN HFETs was reported and shown to reproduce experimental data. Meanwhile, two dimensional simulation data are matched without any adjustable parameters. Also, it is argued by three sets of IV curves that the non-linear resistances are the key factors in producing a bell-shaped transconductance curve. Since the fact that the positive sheet charge is fully neutralized brings electric neutrality around the AlGaN/GaN interface, the zones associated with nonlinear resistances are named the “Source Neutral Zone (SNZ)” and “Drain Neutral Zone (DNZ)”. The local physics-based models for the three zones in the device at low drain bias were presented in detail. Additionally, the proposed model was used to show that conventional parameter fitting approaches to HFET modeling can result in good fits to dc I-V

data that nevertheless introduce significant errors in estimates of important RF figures of merit.

For the first time, a new and distinguishable zone in the drain access region of an HFET is discovered and analyzed. The charge deficit due to the unscreened positive charge is considered to be playing the key role in this zone. As the result, the zone is named the "Charge Deficit Zone (CDZ)". This zone's length and the lateral electric field within it are found to be dependent on the fabrication structure of the device, the current injected into it (which is determined by the applied gate bias), and the voltage drop across it (which is decided by drain bias applied). The impact of this zone on the device increases with increasing drain bias. This zone's impact on overall device performance is proven including DC IV characteristics and transconductance. An analytical model is successfully constructed based on the physics of this zone. The resulting model predictions compare favorably with numerical simulation from ATLAS in a variety of operating conditions. A verification process was executed based on a variety of parameters, including device background doping and thickness. Together with the CDZ, another zone appears during saturation operation in tandem. This zone is analyzed and modeled for the first time for HFETs. It is shown that this zone, derived from the depletion region at the drain said gate edge, transforms the quantum well, which works as the device's channel, into a barrier. The barrier detours the electron flow and consequently obliges the majority of electrons to travel in the neutral bulk GaN near the bottom of the device. This interesting operation brings space-charge limited transport in

this unique zone. Hence this zone is named the “Space charge Limited Zone (SLZ)”. A model of the SLZ is built and connected with the CDZ’s model since the SLZ and CDZ are neighboring zones and share the drain side gate edge as the boundary. These two zones expand rapidly with increasing drain bias. Because of their physical nature, as analyzed in this dissertation, the SLZ grows faster when the drain current is small and the CDZ extends faster when the drain current is high. However, regardless how large the drain current is, these two zones dominate after the device saturates, especially at a high drain bias. By adding models of the SLZ and CDZ into the model of a device under triode operation, a complete physics-based model for all five zones in the device which apply in saturation operation is presented in detail. This five-zone division for saturation operation is shown in Fig 2.3. The two additional zones are proven to bring significant improvement in DC IV curves when a high drain voltage is applied.

6.2 Future work

As introduced in the previous chapters, several assumptions are made for the sake of simplification. For example, between the SLZ and the CDZ, we neglect the short transition region where electrons flow back from the device's bottom toward the channel. Another example is that the contact resistances are neglected while they should be considered in series at the three terminals. These assumptions are responsible for a certain error which is proven to be tolerable at this stage. However, better modeling of these errors definitely improves the model.

Besides this, since this model is the first pure physics-based model reported for AlGaN/GaN HFETs, only dominant principles are considered. In a real device, there are other effects at second or even higher orders. For example, the thermal effect associated with self-heating is becoming more and more serious with the increasing power level in applications. Other than the thermal effect, the disturbing problems of gate leakage and gate lag in GaAs MESFETs occur in AlGaN/GaN HFETs as well.

6.2.1 Thermal effect

Some compound device models currently use a thermal circuit in simulating the thermal effect. Such a thermal circuit is shown in Fig 6.1 [1]. The origins of the thermal circuit can be found by examining a simplified thermal problem. Following the approach of Schaefer and Dunn [2] and considering the simplified thermal problem of a distributed heat conductor, a

link between the heat flow equations and the thermal circuit is demonstrated by an analogy between heat flow equations and transmission line equations [1]. This thermal circuit can be set isolated from the electric circuit. The dissipated power supplies this thermal circuit as the current source. The device temperature is the voltage at the ungrounded node. By setting parameters in the electric circuit as temperature dependent, the dissipated power appears to be a function of the temperature in the electric circuit. At the same time, the thermal circuit provides the feedback because the dissipated power works as a source. The solution to both the electric and thermal circuits is the steady state at which the device works. This thermal circuit can be easily implemented by C or Verilog-A.

After integration of the thermal circuit into the device's electric circuit described in Fig 5.10, the DC IV characteristic free of thermal effect can be verified through comparison with ATLAS simulation results. However, experimental DC IV characteristic should be compared against the result adjusted by this thermal circuit.

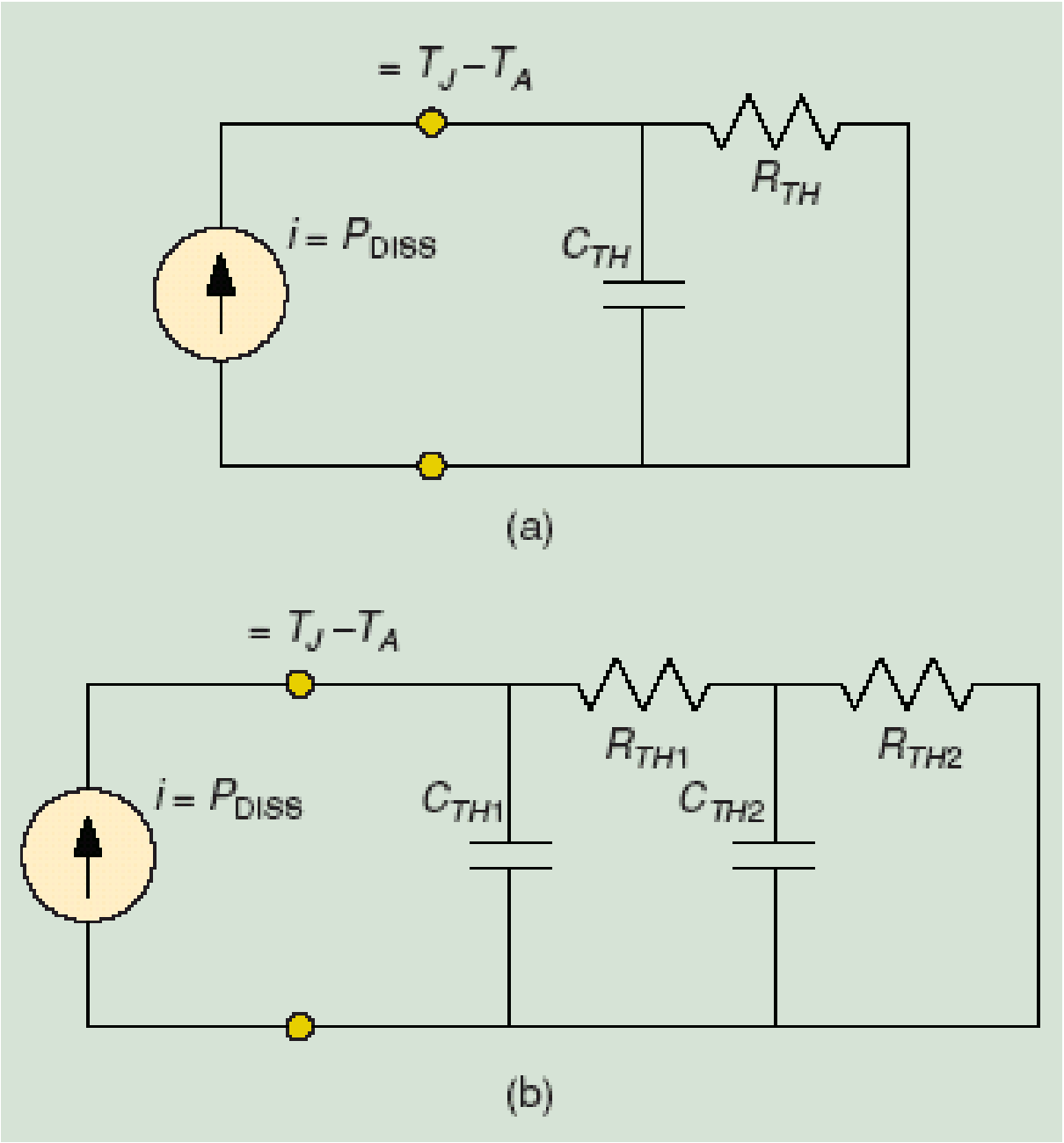

Fig 6.1: Lumped-element thermal circuit with (a) one RC section and (b) two RC sections [1]

6.2.2 Gate leakage and delay

Although the gate leakage in AlGaN/GaN HFETs is greatly improved from GaAs devices, the gate leakage remains as a problem due to the increasing bias in applications. The gate leakage can be treated in similar way to that in TEFLON [3] since the high electric field at the drain-side gate edge is responsible for the gate leakage in both HFETs and MESFETs. This model is illustrated in Fig 6.2.

The delay in frequency response is considered an effect of the depletion region at the drain-side gate edge [4]. With models of the SLZ and the CDZ, we can now estimate the length of this depletion region and quantitatively determine the delay as a consequence. This delay brings a phase shift in the component of drain current source in the electric circuit shown in Fig 5.10

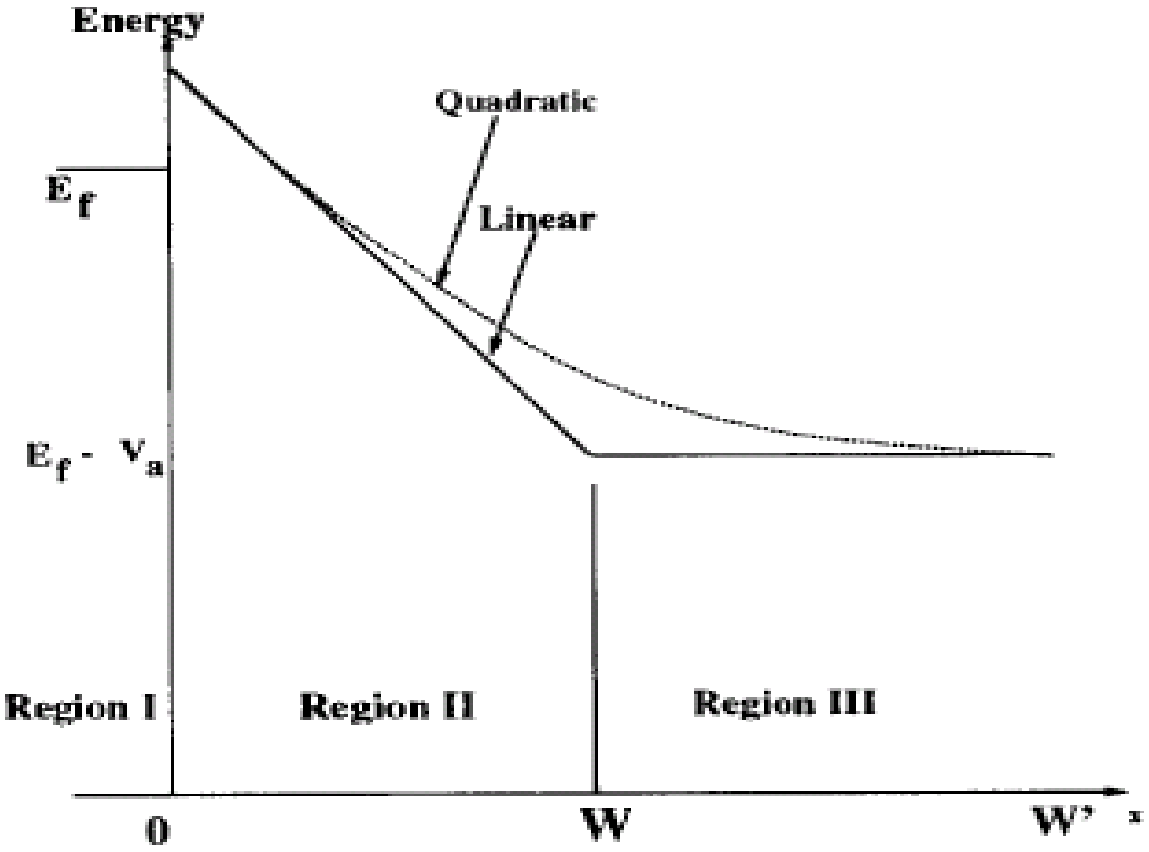

Fig 6.2: Illustration of the gate leakage model in TEFLON

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