# ABSTRACT

TERRY, DAVID B. A holistic investigation of alternative gate stack materials for future CMOS applications. (Under the direction of Dr. Gregory N. Parsons.)

High dielectric constant (high-k) insulators and metal gate electrodes are important for advanced MOS devices to limit gate leakage by increasing gate capacitance with ultimately thicker films and eliminate poly-depletion & dopant diffusion, respectively. Reactions between dielectric/substrate and gate electrode/dielectric during deposition or post-deposition processing lead to an increase in interfacial layer formation, and the mechanisms that control the changes need to be well understood. We investigate yttrium-based and hafnium-based high-k dielectrics and ruthenium-based gate electrodes formed by various processing methods such as physical vapor deposition (PVD), chemical vapor deposition (CVD), and atomic layer deposition (ALD) on Si(100). Characterization techniques include IR, XPS, TEM, EELS, AES, and IV and CV electrical analysis. During deposition and post-deposition treatments the interfaces have some extent of interfacial layer formation. The extent of the intermixing depends on substrate surface preparation, process conditions, and annealing conditions. The transition metal alluminate dielectrics show evidence on flatband voltage tuning via charge compensation. Also, the ruthenium gate electrodes show that process condition can have a direct effect the electronic and chemical properties of MOS structures such as *in-situ* versus *ex-situ* capacitor fabrication and the role of subsurface adsorbed oxygen in ruthenium.

# A holistic investigation of alternative gate stack materials for future CMOS applications

by

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**APPROVED BY:**

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This thesis is dedicated to:

my Daughter, Elaina Santana Skipper,

my parents, James E. Terry and Kathleen L. Terry,

and my brothers (& their families), James, Chris, and Greg,

for all of their love and support.

## Biography

David B. Terry was born June 16, 1970 in Lancaster, Pennsylvania. He grew up in Wilmington, North Carolina and graduated from New Hanover High School. He join the United States Air Force from 1990-1993 with a job in communication were he relayed, received, and transmitted TOP SECRET messages. He majored in Chemistry, and received a Bachelor of Science degree with honors in 1999. He enrolled in the Chemical Engineering graduate program at North Carolina State University in August 1999. Upon completion of his Masters degree (2004), he continued to pursue his Ph.D. in the Chemical Engineering Department at North Carolina State University under the guidance of Dr. Gregory Parsons.

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# Chapter 1 Introduction

***Historical Perspective***

In 1947, the invention of the metal-oxide-semiconductor field-effect transistor (MOSFET) by Bardeen, Brattain, and Shockley [1] and the subsequent development of monolithic silicon based integrated circuit fabrication techniques has led to unprecedented levels of growth in the semiconductor industry through the latter half of the 20$^{th}$ century. The scaling of silicon based microelectronic devices and integrated circuits were originally predicted by Gordon Moore [2] in 1965 to last at least a decade. Through the years, complementary metal-oxide-semiconductor field-effect transistor (CMOSFET) device scaling to ever smaller physical dimensions has led to continuous improvement in microelectronic device performance and to its widespread proliferation which now constitute about 90% of the semiconductor device market. Phenomenal advances in photolithography techniques, tools and pattern transfer processes and equipment have however, ensured the validity of *Moore's Law* well into the 21$^{st}$ century. In an evolution driven primarily by photolithography, minimum feature sizes on devices have been scaled down from several microns in the 1970's to less than 100nm today. This has enabled consistent improvement in device packing densities on chips, enhancement in circuit speeds and vastly improved performance-to-cost ratios for microelectronics based products. As a result of aggressively scaled devices, scientist and engineers will have to address the rapidly approaching physical limits for many conventional transistor materials. Therefore, trends for future device scaling are greatly dependent on significant changes in basic transistor materials and device structures. The turn of the century is beyond any doubt an exciting time for device and

process integration engineers and materials scientists alike and the need for enhanced cross-disciplinary research has seldom been more promising.

***Complementary metal oxide semiconductor***

Complementary metal oxide semiconductor (CMOS) transistor technology has traditionally relied on Si (element or as part of a compound) in several morphological forms (bulk single crystalline, thin film polycrystalline, thin film epitaxial) to serve the varied functions that are needed for the satisfactory operation of a field-effect transistor. Silicon and Si based materials have thus been used in several functional forms as semiconductor (channel, body), insulator (gate dielectric, inter-metal dielectric) and conductor (gate electrode, silicide contacts) in a conventional field-effect transistor, shown in figure 1.1. While thermodynamically stable, ease of formation and acceptable dielectric properties have been some of the motivations behind the use of $SiO_2$ as a gate dielectric; ease of process integration and device performance issues like threshold voltage control have been the important considerations in the use of poly-silicon gate electrodes. Research over the last few years indicates an increasing use of metal-based stack materials for future CMOS devices [3].

In order to be acceptable for use as gate electrodes in future CMOS devices, candidate materials must posses several general physical properties and must lend themselves easily to conventional Si processing techniques (lithography, deposition (physical/chemical vapor), etching (dry/wet), etc.). Candidate metals must have high (> 1000 ºC) melting points and must be thermodynamically stable on the MOSFET gate dielectric ($SiO_2$ or other alternative gate dielectrics). These metals must be very conductive and must have thermal expansion coefficients close to Si (to minimize the possibility of thermally induced stresses

after rapid thermal processing). In addition to these requirements, the selection of materials for this application is also constrained by the need to obtain low and symmetric threshold voltages on the N- and PMOSFET devices. The gate electrode of a MOSFET influences the threshold voltage of the transistor through its work function. In order to obtain low and symmetric threshold voltages on the two types of devices, while maintaining acceptable short channel performance, it is essential that the two gate electrodes have different work functions. The ideal gate work function for bulk-Si NMOSFETs (PMOSFETs) is ± 0.2V of the $E_C$ ($E_V$) of Si respectively [4] (shown in figure 1.2). It is thus evident that the integration of multiple metals on a single substrate or the development of a single metal tunable work function schemes will become necessary in future CMOS gate stacks. From a process perspective, the latter is highly desirable. Engineering the work function of a metal thin film at dielectric interfaces is however not trivial. This dissertation will briefly discuss different approaches developed to fabricating dual-metal gate CMOS devices and focus on a novel single-metal tunable work function approach that might assist in the integration of metal gates into CMOSFET devices.

***Objective of this work***

Our primary objective is to investigate alternative candidate materials for the replacement of Si-based gate stack materials specifically replacing current $SiO_2$ dielectrics and poly-Si gates. Since it will be crucial to replace these materials simultaneously, our goal throughout this dissertation is to holistically research candidate materials in tandem. The primary goal was to develop optimal deposition processes for both dielectrics and gate materials. The second goal was to investigate the interface properties as well as bulk

properties leading candidate materials and the effects they have at the interface. The third goal was to understand the chemical reactions that take place during the deposition processes.

***Overview of Dissertation***

This dissertation has been focused on understanding process reaction mechanisms during processing of candidate alternative gate stack materials for CMOSFET applications. The impact these materials will have for future CMOS devices were evaluated. For dielectrics, the flatband voltage was tunable with alloying $Al_2O_3$ with $Y_2O_3$ or $HfO_2$ with yttrium aluminates being most sensitive to small changes in atomic percentages of Al incorporation. Also, the film composition for ruthenium films grown by atomic layer deposition varies between reactant pulse with an adsorbed oxygen layer after the oxygen pulse which later reacts with the precursor ligands.

Chapter 2 illustrates the guidelines necessary for selecting alternative gate stacks materials and highlights some of the challenges for their succession to current Si-based materials. Interfaces stabilities when in contact with other materials (specifically thermal stabilities of dielectrics in contact with the silicon substrate and gate electrodes in contact with the dielectric) are also highlighted.

Chapter 3 discussed the possible techniques used to fabricate alternative gate stack materials. The choice of processing technique used to fabricate the materials must allow for easy implementation into current CMOS processing technologies. Also, the methods for analysis the materials are discussed which include techniques for physical, chemical, and electrical characterization.

Chapter 4 presents results of charge compensation and thermal stabilities of yttrium alluminates and hafnium alluminates formed by oxidation of Hf:Al and Y:Al mixtures on

silicon. Successful flatband voltage tuning is present and the yttrium alluminate films were most sensitive to small changed in Al composition. Capacitance versus voltage analysis indicates that the addition of Al to Hf and Y oxides results in a positive shift in flatband voltage with increasing Al concentration for both set of mixtures. Also, the suppression of interfacial layer formation was significantly reduce with small amounts (<5 atomic percent) of Al which is indicated by reduction of equivalent oxide thickness (eot) values. X-ray photoelectron spectroscopy (XPS) investigation of Y(or Hf) and Al chemical states of the alloy films indicate the films are a homogenous mixture of $HfO_2$ (or $Y_2O_3$) and $Al_2O_3$.

Chapter 5 we evaluate ruthenium-based metals as potential candidates for gate electrodes in advanced gate stack applications. We deposited $RuO_2$ metal from tris-tetramethyl-heptadianato Ru (Ru TMHD) introduced downstream from a remote $N_2O$ plasma at 365 and 500°C, and examined the deposited film and interface structure using Auger and X-ray photoelectron spectroscopies. The films show some evidence for N and C incorporation, consistent with the 250°C decomposition temperature of the Ru TMHD. Based on AES results, the O/Ru ratio is larger for the films deposited at higher temperature. Because of the difference between the oxidizing and reducing environments in CVD processing, we expect that metallic oxides such as $RuO_2$ will result in different metal/dielectric interface structure than for elemental metal/dielectric interfaces. To examine the role of deposition chemistry on interface structure, several thicknesses of $RuO_2$ have been deposited by plasma CVD on $HfO_2$ formed in our lab by atomic layer deposition. The effect of $HfO_2$ surface structure, and the trends in $RuO_2$ composition with film thickness determined using AES and XPS will be presented and discussed

Chapter 6 describes how the oxidation of Hf metal films on Si appears to follow different charge generation rules than the traditional oxidation of Si described in detail by Deal et al. Oxidation of thin Hf metal films on silicon in oxygen rich environments to form Hf-silicate results in rapid growth of silicon oxide interfacial layers and generation of significant charge concentration in the films. Oxidation of Hf in oxygen-deficient environment leads to improved control of the interface with much thinner interfacial layers and substantial reduction in the charge present in the films. Results from capacitance vs. voltage and x-ray photoelectron spectroscopy measurements are compared to correlate charge with chemical structure evolution during oxidation and dielectric layer formation. It is demonstrated that processing conditions may influence the quality of the Hf dielectric film significantly by generating positive charge that is not intrinsic to the material.

Chapter 7 evaluates the role of atomic layer deposition (ALD) ruthenium films from bis(cyclopentadienyl) ruthenium $(RuCp)_2$ using online Auger Electron Spectroscopy (AES) to identify surface composition of the films during the ALD process. The AES results show significant changes in film composition when comparing the surface after the precursor pulse and the reactant pulse. The compositions show evidence that the ruthenium films form an adsorbed oxygen layer during the reactant pulse which facilitates the oxidation of unreacted precursor ligands leftover from the precursor pulse step.

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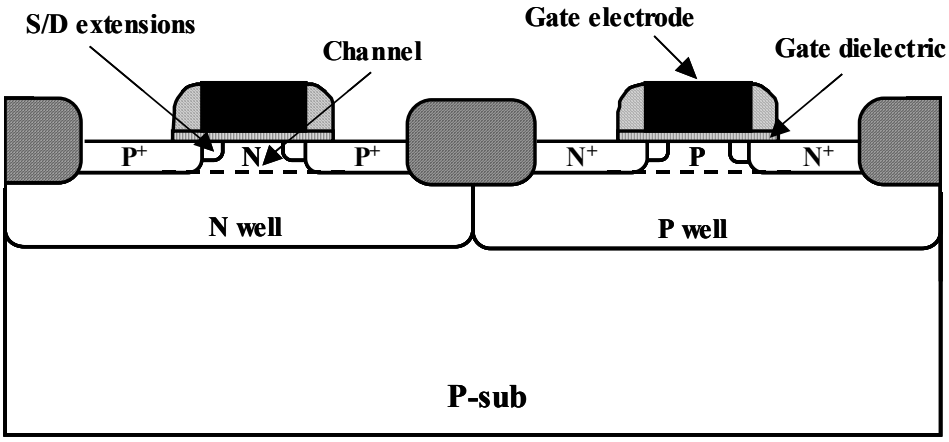


Figure 1.1: Illustration of a complete CMOS structure

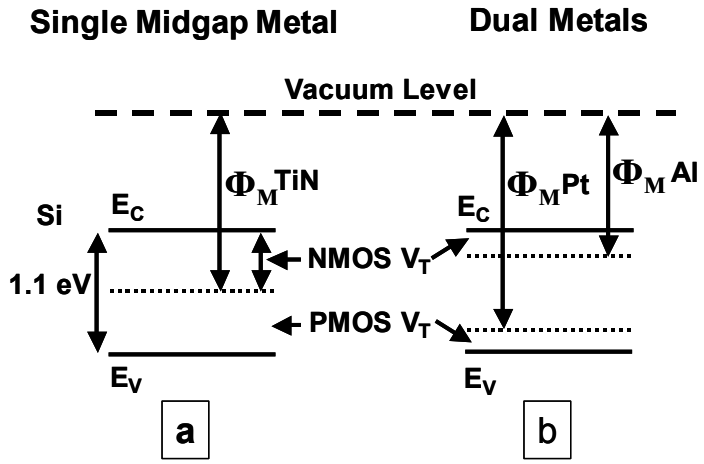


Figure 1.2: Comparison of metal workfunctions for midgap metal and dual metals.

# Chapter 2 Metal Gate CMOS Technology

### *Advanced Gate Electrode Materials*

Polycrystalline silicon (poly-Si) has been used as a MOSFET gate material for several decades. One of the primary reasons for this is its high compatibility with CMOS processing. Poly-Si can be very easily deposited by low-pressure chemical vapor deposition (LPCVD) techniques and it displays excellent thermal stability on $SiO_2$, which has been the gate dielectric of choice for MOSFETs. From a device performance perspective, the most important property of the gate electrode is its work function at the dielectric interface. In a MOS system, it is the work function of the gate that controls the threshold voltage of the device, by controlling how much applied voltage is necessary to bring about inversion in the transistor substrate. For a CMOS technology, it is generally desirable to have low and symmetric threshold voltages on the N- and PMOS devices. As device channel lengths have been scaled down over successive technology generations, dopant concentrations in the channel have been increased in order to maintain good short channel performance (i.e., in order to prevent the channel depletion region from becoming too large and the drain depletion charge from significantly penetrating into the channel region). This in turn requires the gate work function to be close to $E_C$ and $E_V$ for bulk-Si N- and PMOS devices respectively (so that reasonably low threshold voltages can be maintained). Adjusting the dopant concentrations in the transistor channel can also control the device threshold voltage. In principle, a single gate material with Fermi level near the middle of the Si bandgap could be used for both N and PMOS operation, it would not allow the threshold voltages to be kept low. Possibly more importantly, it would also deteriorate device short channel performance. Thus, dual-doped poly-Si has been a preferred CMOS gate material. The primary process

integration benefit comes from the ease with which an undoped poly-Si can be converted to a low work function ($n+$) or a high work function ($p+$) film using ion implantation of appropriate dopants (donors or acceptors) followed by thermal annealing.

Perhaps the most pressing reason to look at alterative gate materials for deep-submicron CMOS devices arises from the fact that a heavily doped poly-Si gate will become depleted at the gate/dielectric interface when the channel is in inversion[1]. A schematic band diagram across the MOS stack is shown in Fig. 2.1 to illustrate this phenomenon.

A depletion layer in the gate can be harmful in several ways. It adds a capacitance in series to the gate dielectric capacitance and thus adds to the effective dielectric thickness between the gate and the channel. This implies a reduction in the capacitive coupling between the gate and the channel in inversion. For comparable channel currents, the reduction in the inversion capacitance in the case of a poly-Si gate device lowers the drive current significantly [2]. The gate depletion effect is of particular concern for deep-submicron CMOS technology. As the dielectric thickness is scaled to 1nm and below in sub-50nm devices [3, 4], even the addition of a few tenths of a nanometer in the form of a depletion layer can significantly increase the effective dielectric thickness of the device. This would also be a serious setback to all efforts to scale down the gate dielectric thickness using high-permittivity gate dielectrics. Because of this, many researchers have investigated alternative gate electrode materials, which can either reduce or eliminate the gate depletion effect. The use of metal gate materials is most beneficial for devices with very thin EOT (< 1nm) where high performance (high drive currents) is most important. While refractory metals and their metallic derivatives are attractive candidates, there are numerous process

integration challenges that must be overcome before a viable metal-gate CMOS technology can be developed.

In addition to the gate depletion effect, thermodynamic incompatibility with high-k gate dielectric is also an issue for poly-Si gate technology. There have been successful demonstrations of MOS capacitors and transistors with ultra-thin EOT using high-k gate dielectrics viz. oxides of Hf, Zr, Al, Y, and La [5-9]. Many of these materials are not thermally stable in contact with poly-Si above certain temperatures, and therefore cannot be used in a conventional dual poly-Si gate CMOS process, in which the highest activation annealing temperature can exceed 1000ºC. Therefore, alternative gate materials that are thermally stable with various advances gate dielectric materials will be needed. It must be mentioned however, that the high-k dielectric is typically separated from the Si substrate by a thin interfacial layer ($SiO_2$, $Si_3N_4$, or an oxy-nitride) and hence the bottom interface can withstand elevated temperatures.

When ultra-thin gate dielectrics are used in conjunction with poly-Si gate electrodes, dopant penetration from the gate into the channel can be a significant problem. It has been especially severe for *p*+ gate electrodes given the small mass and high diffusivity of B in Si. Boron penetration has also been observed to occur through high-k dielectrics [10] and is a potentially significant concern for future gate stacks since it leads to instabilities in device operations.

An additional concern with poly-Si gate electrodes is the active dopant concentration limited conductivity. For CMOS applications, the poly-Si gate electrode is deposited undoped and subsequently converted to *n*- or *p*-type using appropriate ion implantation and annealing. The electrically active dopant concentration is thus inherently limited by the

physical dose of dopant ions implanted into the gate, the thermal budget allowed to activate the dopants (ie. move them to substitutional sites in the Si lattice) and the solid solubility of the dopant atoms in Si. This might lead to unreasonably high resistivities on the gate lines. For example, when dopants are implanted in the poly-Si gate, they need to be "activated" by a high-temperature anneal (up to 1100°C) to diffuse the dopant atoms to lattice sites and make them electrically active (thereby making the gate conductive). However, current CMOS processes use lower temperature anneals (~950°C) to limit unwanted dopant diffusion in other regions of the device. Therefore, the poly-Si is not completely activated and has some finite capacitance, because it is not completely conductive. In operation, this poly-depletion effect adds a series capacitance with an EOT of 3-7Å to the gate stack, which becomes a significant problem as industry attempts to scale the gate stack to EOT values below 10nm. A further difficulty arises with the continued scaling of the physical dimensions of the gate electrode. According to the International Technology Roadmap for Semiconductors (ITRS) [11], the aspect ratio for the gate electrode is expected to remain constant (height/length) as the gate length is scaled down. Concomitantly, the gate sheet resistance is to be maintained at 5 Ω/□. This implies the need for a steady increase in gate active dopant concentrations as the gate length is scaled down. If the use of high-k gate dielectrics precludes the use of high thermal budgets for dopant activation, it is unclear how the specified values of active dopant concentration and gate sheet resistance would be achieved in a poly-Si gate technology. The solid solubility of the commonly used dopants in Si poses physical limitations on the gate sheet resistance. In order to achieve required gate sheet resistance of 5 Ω/□, the active dopant concentration in the gate would have to be ~$1.8 \times 10^{20} cm^{-3}$ for the 65 nm technology node. The solid solubility of B, As, and P at 1000ºC

are ~$1x10^{20}$ $cm^{-3}$, $2x10^{20}$ $cm^{-3}$, and $3x10^{20}$ $cm^{-3}$ respectively [12]. It should be noted that the required active dopant levels would imply super-saturated solutions of B in Si and near 100% activation of P and As.

Metal gate materials thus appear to be very attractive candidates for future CMOS devices. However, there are significant process integration challenges that must be overcome before a metal gate technology can be considered to be viable for integrated circuit manufacturing.

***Selection of Materials***

Candidate gate materials must satisfy several criteria in order to be viable for use in a Si-based CMOS fabrication process. As mentioned earlier, for sub-65nm technology nodes, the ITRS specifies a gate sheet resistance of $\leq 5$ Ω/□. Thus these materials must be highly conductive and must have very high melting points, and be stable in contact with the high-k dielectric in order to withstand thermal budgets commonly used in CMOS processing. It is also important that these materials lend themselves easily to conventional thin-film deposition (physical or chemical vapor) and reactive ion etching (RIE) techniques. These requirements will ensure that advanced gate CMOS devices can still be fabricated using conventional tools. The new gate materials also need to have thermal expansion coefficients that closely match those of the single crystalline Si substrate in order to ensure that no significant thermal stresses are introduced in the film during rapid temperature changes (as used for dopant activation), and they must have good adhesion with the underlying dielectric. The general requirements described above already limit the candidate materials to some of the high melting point refractory metals, e.g. W, Ti, Ta, Mo, Nb, Re, Ru and their binary or ternary metallic derivatives, e.g. WN, TiN, TaN, MoN, $MoO_2$, TaSiN.

The most significant constraint in the choice of gate material, however, relates to the need to precisely engineer the transistor threshold voltage. As mentioned earlier, in order to obtain low and symmetric N- and PMOSFET threshold voltages ($V_T$) while suppressing short-channel effects, it is essential to have the gate work function between ± 0.2eV of $E_C$ and $E_V$ for bulk-Si N- and PMOSFETs respectively [3]. There is thus a need to identify metallic materials that have work functions close to the above value and to develop process integration schemes that will provide multiple gate work functions for NMOS and PMOS devices integrated on a single Si substrate. A further challenge is imposed by the dependence of the metal work function on the properties of the underlying dielectric film. In general, metal work functions at dielectric interfaces differ from their values in vacuum [13]. This observation and its theoretical origins indicate that the search for metal gate materials must be conducted in tandem with the search for alternative gate dielectrics. It should also be noted that metals with complementary work functions also display inherent differences in physical properties like reactivity. Low work function metals are typically easily oxidized while high work function metals are inherently inert. This imposes additional constraints on the choice of metal gate material and process integration schemes.

***Candidate Materials***

The choice of materials are governed by two sets of requirements alluded to earlier in this chapter. One set encompasses general physical and chemical properties that are required by the constraints imposed by the device fabrication methods. The other set includes specific properties needed for optimum performance of the device.

*Physical Properties*

Candidate gate metals need to be thermodynamically stable on the gate dielectric and must be able to withstand thermal budgets commonly used in CMOS fabrication. The highest temperatures used in device fabrication are for the activation of dopant atoms in the source, drain, and gate regions of the transistor. Typical activation thermal budgets include rapid thermal annealing at temperatures just above 1000ºC (either a spike anneal with no soak time or for a few seconds soak at the highest temperature). This implies minimum melting temperature of well above 1000ºC for assured thermal stability. While nitrided $SiO_2$ is the currently used dielectric, it would be very likely that a change from $SiO_2$ to higher permittivity dielectrics will occur simultaneously with that from poly-Si to alternative gate electrode materials. Hence, the new gate electrode material must be chosen in tandem with potential high-k materials being explored. The choice of high-k gate dielectrics is governed by similar thermal stability concerns with the Si substrate and specific physical and electronic properties such as the permittivity, band gap, electron and hole effective masses and band offsets with respect to the Si substrate. A modest permittivity (k~20-30) is expected to be an optimum value given the inverse relationship between permittivity and band gap (a smaller band gap is undesirable as it would lower the barrier height for electron or hole tunneling between the gate and the channel). Over the last several years, many research groups have actively pursued the search for new gate dielectrics starting from purely theoretical thermodynamic considerations [14] to experimental demonstrations of high-k MOS capacitors and transistors [15-17]. While a lot of work remains to be done in this field, it appears that metal-based dielectrics (binary or ternary oxides and silicates of refractory or rare earth metals) are most likely candidates to replace $SiO_2$ or $SiO_2$ based ($Si_3N_4$ or SiON)

gate dielectrics. It is essential that the thermal stability of alternative gate materials on at least a subset of candidate dielectrics be experimentally verified. Typically, low work function metals are fairly reactive (prone to oxidation) (eg. Al, Ti, Ta) while high work function metals tend to be inert (eg. Ni, Pt, Pd, etc.) and naturally immune to oxidation.

The techniques used to deposit the gate electrode affects a number of important properties of the gate electrode. The morphology of the gate electrode is important for several reasons. An amorphous gate electrode is likely to have a work function significantly different from that of a crystalline one. In addition, different crystalline facets of a single crystal typically display a wide range of work functions. Thus, it is critical to identify deposition conditions that will lead to appropriate film morphologies and orientations. Furthermore, the deposition technique will also affect the quality of the interface between the gate electrode and the dielectric. In general, a deposition technique that permits sharp interfaces to be obtained is desirable. Most metal thin films are deposited using physical vapor deposition (PVD) techniques viz. sputtering (using DC, magnetron, or RF sources) or evaporation (using electron beam or thermal evaporation). Unfortunately, most of these techniques involve the use of energetic particles (ions, electrons) and are mostly likely to impart physical damage to the gate dielectric (rough interfaces, metal ions penetrating into the dielectric, etc.) and result in degraded gate dielectric reliability [18, 19]. Chemical vapor deposition techniques would lead to minimal damage to the underlying dielectric and are desirable for this application. Chemical vapor deposition will also provide a number of variables, viz. temperature, pressure, gas flow to control the film microstructure. However, apart from a few exceptions (W and Ta) precursors for refractory metal CVD have not been

very well identified or characterized. This is a challenging area that can be expected to become even more important as CMOS technology continues to be scaled down.

Yet another important consideration in the choice of a gate material is its patternability. Gate films will need to be etched with high selectivity to the underlying dielectric. In addition, the gate etch should ideally result in vertical sidewalls without any protrusions or notches at the dielectric interface. This implies optimizations of reactive ion etch chemistries and process conditions that ensure high etch selectivity and ideal sidewall profiles. While wet etch chemistries might also be used to remove metal films with high selectivity to the gate dielectric, the use of wet etchants for sub-50 nm line patterning is unlikely given the isotropic nature of wet etching processes. The choice of gate material will have to account for the inherent reactivity or inertness of the metal under consideration.

State of the art CMOS fabrication processes involve the use of rapid thermal annealing (RTA) to activate dopant atoms in the source, drain, and gate with minimal diffusion. Typical RTA temperatures are between 900-1000ºC and typical annealing times range from a few seconds to a minute. In some cases, spike annealing (no soak at peak temperature) is also used. Temperature ramp-up is typically between 200-250ºC/s and cool-down of the wafer is also very rapid. This rapid thermal cycling can become a source of thermally induced stresses in the MOS stack and might lead to cracking or peeling of gate films depending on the magnitude of the stress induced. In light of this, it is necessary to choose a gate material that has a coefficient of thermal expansion that is close to that of bulk Si.

*Work Function*

The most direct impact of the gate electrode on the operation of a MOSFET is through its control of the device threshold voltage ($V_T$). The voltage required for the onset of inversion in the MOSFET channel is determined by the work function of the gate electrode. The threshold voltage of a MOSFET is typically given by the following expression:

$$V_T = V_{FB} + \frac{\sqrt{2\varepsilon_{Si} q N_a 2\phi_B}}{C_{OX}}$$

where ε is the permittivity of Si, $q$ is the electronic charge, $N_a$ is the dopant concentration in the channel, $\phi_B$ is the band bending in the Si substrate and $C_{ox}$ is the oxide capacitance. $V_{FB}$ is the flat band voltage across the MOS stack and denotes the voltage applied on the gate electrode that eliminates any band bending across the stack. $V_{FB}$ is given by the following expression:

$$V_{FB} = \Phi_{MS} + 2\phi_B \pm \frac{Q_f}{C_{OX}}$$

where $\Phi_{MS}$ indicates the work function difference between the metal gate and the Si substrate and $Q_f$ denotes the magnitude of fixed charge in the oxide film.

The gate electrode through the work function difference between the gate and the channel thus directly controls the threshold voltage of the MOSFET. The band bending in the channel is given by the following expression:

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right)$$

where $n_i$ is the intrinsic Si carrier concentration. For typical channel doping levels used ($1x10^{16}$-$1x10^{18}cm^{-3}$), $\phi_B$ is approximately 0.3-0.4 eV. To minimize $V_T$ the flat band voltage should thus be ~ -0.8 V for an NMOS device and ~ +0.8V for a PMOS device. This in turn

implies gate work function values of ~ 4.1V for NMOS and ~ 5.1V for PMOS devices. More precise calculations performed using 2D device simulations [3] indicate that for an optimum combination of short channel performance and device drive current, gate work functions for sub-50 nm bulk CMOS transistors should be between ± 0.2eV of $E_C$ ($E_V$) for NMOS (PMOS). Sub-100 nm gate length bulk-Si MOSFETs typically need fairly high dopant concentrations in the channel regions to prevent the drain depletion region from penetrating excessively into the channel leading to poor short-channel performance. However, high levels of channel doping typically degrade carrier mobility in the transistor channel.

***Metal Gate/High-k Dielectric Integration***

An important consideration in the selection of metal gate electrodes is the work function dependence in contact with high-k dielectric. In general, the work function of a metal at a dielectric interface is different from its value in vacuum. This variation needs to be taken into account when designing transistor gate stacks with alternative gate dielectrics.

The dependence of the metal work function on the permittivity of the gate dielectric has been explained by Lu et al [20] using experimental data in conjunction with interface dipole theory [21]. In order to accurately predict metal work functions at dielectric interfaces, one needs to take into account charge transfer across such interfaces. In general, there are always intrinsic interface states at metal-dielectric interfaces [22] which can be predominantly donor like (closer to $E_V$) or acceptor like (closer to $E_C$). When an interface is formed between a metal and a dielectric, these interface states can get charged up resulting in a dipole that will drive the bands to align in a way that minimizes the charge transfer. The energy level at which the dominant character of the interface states changes between donor- and acceptor-like is called the charge neutrality level, $E_{CNL}$. For example, in the case where

the metal Fermi level ($E_{F,M}$) is above the dielectric charge neutrality level ($E_{CNL,D}$), the dipole layer created at the interface will be charged negatively on the dielectric side. This dipole will tend to drive the metal Fermi level towards $E_{CNL,D}$ and hence the effective metal work function ($\Phi_{M,eff}$) will be different from the vacuum metal work function ($\Phi_{M,vac}$). This work function change is proportional to the difference between $E_{CNL,D}$ and $E_{F,M}$, or equivalently, the difference between $\Phi_{M,vac}$ and $\Phi_{CNL,D}$. Taking into account the effects of charge screening in the dielectric, the effective metal work function $\Phi_{M,eff}$ is given by

$$\Phi_{M,eff} = \Phi_{CNL,D} + S\left(\Phi_{M,vac} - \Phi_{CNL,D}\right)$$

where *S* is a slope parameter that accounts for dielectric screening and depends on the electronic component of the dielectric constant, $\varepsilon_\infty$, [23] according to

$$S = \left[1 + 0.1\left(\varepsilon_\infty - 1\right)^2\right]^{-1}$$

A larger dielectric screening lowers the slope parameter *S* and increases the degree of pinning of the metal work function to $E_{CNL,D}$. Values for $\varepsilon_\infty$ for various dielectrics of interest ($SiO_2$, $Si_3N_4$, $HfO_2$, and $ZrO_2$) have been used to calculate the slope parameters for these dielectrics. Comparison of theoretical and measured interfacial work functions for several metals of interest (Al, Ti, W, Mo, and Pt) led to reasonable agreement indicating the validity of the theory. An important conclusion of this work was highlighted in [20], where it was shown that in order to obtain $\Phi_{M,eff}$ of 4.05V (5.17V) for NMOS (PMOS) gate electrodes, metals with even smaller (larger) $\Phi_{M,vac}$ have to be used as the permittivity of the gate dielectric is increased. The consequence of this theory on the selection of gate metals is that PMOS compatible metals will most likely be very inert (high work function), while NMOS compatible metals will be very reactive (low work function). These complementary properties are likely to have a significant impact on future CMOS gate stack process

integration since very inert metals are by definition difficult to etch (a general lack of volatile compounds) while reactive metals are likely to react with the underlying gate dielectric (typically an oxidation reaction where oxygen from the dielectric can preferentially bond with the gate metal).

***Process Integration***

In general, one may use a combination of two or more metals on a single Si substrate to achieve the work function requirements discussed above. While the processes described herein have been successfully implemented, it must be noted that the integration of multiple metals on a single wafer poses significant process integration challenges and it would be highly desirable to develop a single metal tunable work function gate CMOS process. Such a process would allow for minimal process complexity and would be relatively easy to integrate on a single Si substrate.

*Dual Metal Gate CMOS Technology*

Probably the most intuitive approach to developing a metal gate CMOS process involves the use of two metal, on serving as the NMOS gate and the other as the PMOS gate. Process integration is however not very straightforward since two film deposition steps and at least two etch steps would be involved.

The general process involves the deposition of one metal over the entire substrate after active area definition and gate dielectric deposition. Following the first deposition, a well lithography is performed to expose either n- or p-well regions and the exposed metal is removed using a wet etch chemistry. For example, if the first metal is appropriate for NMOS gates, then it is retained over the p-well and removed from the n-wells and vice-versa for the PMOS gate metal. The choice of which metal to deposit first depends on the relative ease of

removal of the two metals and the selectivity of the etch chemistries on the gate dielectric. Following the removal of the first metal, the photoresist is stripped and after rinsing the wafer, a second metal is deposited over the substance. In doing so, a bilayer metal stack is formed on one half of the substrate, while a single layer gate is formed over the other half and each well has a different metal in direct contact with the gate dielectric. In order to prevent interdiffusion between the two metals on the side where a bilayer is formed, a thin diffusion barrier metal (< 5nm) can be deposited over the first metal before patterning. Figure. 2.2 shows a schematic cross-section through the gate stacks after the two deposition steps. Following the second deposition, photolithography is used to define the gate lines on the N- and PMOS sides.

One concern arises from the fact that the first gate metal is chemically removed over the gate dielectric on one of the wells. In doing so, it is likely that the chemicals used for the metal etch can also attack the thin gate dielectric film. This was also observed in the case of the Mo and Ti gate process where the Ti etchant also attacked the $Si_3N_4$ gate dielectric on the n-well. This discrepancy is generally intolerable, as it would lead to substantial mismatch in the performance of the two types of devices. If a different combination of gate metals and dielectric is used, it might be possible to avoid this drawback, however, any exposure of the dielectric to metal etchants is likely to affect the long term reliability of the gate dielectric film and should be avoided as much as possible. Hence, it is unlikely that the process mentioned herein can be ported to manufacturing as described. One solution is to intentionally remove the gate dielectric entirely over the n-well (or p-well) after removing the first metal layer. This way the n-well (or p-well) active region is exposed and after appropriate cleaning procedures, a new gate stack can be deposited over that well. While this

solution can provide for a more reliable gate dielectric film, it introduces substantial process complexity (removal of dielectric film over first metal film on one well).

Gate lithography of the asymmetrical gate stack presents another concern since the optimal focus depths for the two wells can be substantially different. Another concern lies with developing a high selectivity reactive ion etch process for the asymmetrical gate stacks on the n- and p-wells. Since one well will have a bilayer metal stack and the other well will have only a single metal layer, a high etch selectivity is needed between the second gate metal and the gate dielectric.

*Metal Interdiffuion Gate CMOS Technology*

A technique that alleviates some of the above mentioned concerns was developed [23] and referred to as metal-interdiffusion-gate (MIG) CMOS process since it relies on interdiffusion between two (or more) metal films. This approach can be implemented as follows.

Following gate dielectric deposition, a first metal layer is deposited and immediately capped with a second metal layer. The first metal film is intentionally kept thin ($\leq$ 10nm) while the second metal film can be much thicker. In the next step, resist lithography is used to expose and remove the top metal film over one of the two wells. For example, if the first metal has a work function corresponding to that for NMOS devices, then the second metal is removed over the those areas (p-wells) and vice-versa. Following selective removal of the second metal, gate lithography can be preformed to define gate lines on both the wells. After gate definition, an interdiffusion anneal is performed to interdiffuse the two metals in the bilayer. Depending on the choice of the metals in the pair, this anneal can lead to one of several outcomes.

If the metals do not thermodynamically prefer to alloy over the temperature range used and simple prefer to intermix, the resulting bilayer gate will have a work function that corresponds to that of the mixture. The exact value is however difficult to predict and will depend on the extent of the intermixing (which in turn depends on the relative thicknesses of the two metals films, the interdiffusion coefficients, etc.)

Another outcome can lead to the diffusion of the top metal through the bottom layer and its segregation at the dielectric interface. This will lead to the threshold voltage of the resulting transistor being determined entirely by the segregated metal layer. In effect, the bottom layer can act as a sieve to allow the top metal to pass through. This approach was demonstrated with the use of Ni and Ti bilayer gate stacks [23] and was shown to lead to low and symmetrical threshold voltage n- and p-channel transistors. Ni and Ti were chosen for this demonstration since they have complementary work functions (~ 5V and ~ 4V respectively). Ni was used at the top metal. Ni is a fast diffuser in Ti [24, 25] and is also known to segregate at the $SiO_2$ interface. Even at the relatively low temperature used for interdiffusion (400ºC), x-ray photoelectron spectroscopy (XPS) results indicated that interdiffusion was complete and elemental Ni was observed at the $SiO_2$ interface. This indicates that Ni is stable on $SiO_2$ up to 400ºC and does not preferentially form metal silicides or oxides.

Another possible outcome is the preferential alloying of the two metals to form a binary alloy with a work function determined be the exact composition of the alloy. This approach was recently demonstrated using Ru-Ta system [26]. Co-sputtering of several alloy compositions have also shown desirable work function values and the MIG approach can

potentially be applied to that system as well [27-29]. It is thus important to note that the general MIG concept can also be extended to ternary systems.

The primary advantage of a MIG approach over the dual-metal gate approach described earlier lies in the protection of the gate dielectric at all times since the bottom metal layer is always present to protect the dielectric. Hence, reliability problems associated with the earlier approach can be prevented.

***Work Function Engineering***

The work function of a metal depends on several physical and chemical properties. The conventional definition of the work function of a metal quantifies it in terms of the energy required to remove an electron from the metal surface [30]. Implicit in this definition is the idea that the energy required to remove an electron from a metal is primarily a property of the surface and specifically a property of the interface between the metal and its surrounding medium. From a purely thermodynamic perspective, the work function of a metal can also be defined in terms of the chemical potential within the metal (the Fermi level is in fact one manifestation of the Gibbs free energy of a metal). From a thermodynamic perspective then, structural and/or chemical changes at a metal surface are likely to change the free energy at that surface and hence affect the work function. The notion that structural or chemical changes in a thin metal film are likely to affect its work function is one of the primary hypotheses of this work. This section will discuss various approaches developed to modulate thin film work functions and the feasibility of some of these approaches.

*Structural Modification*

Changes to the structural morphology of thin metal films can be further classified into modification to film texture or preferred orientation, modification to crystalline phase and

modification (disruption) in the long-range order within the crystal lattice. In general, metals display anisotropy in their work function [13]. The origin of this anisotropy is believed to be the difference in atomic packing density along the various crystallographic planes. Densely packed crystallographic surfaces display high work functions since these surfaces are smooth and relatively inert with fewer broken atomic bonds (most bonds are within the plane). Open crystallographic surfaces display lower work functions owing to a greater number of broken bonds (larger fraction of bonds outside the plane). Smoluchowski [31] has developed a formal semi-quantitative theory to explain this anisotropy based on a similar crystallographic analysis. Amorphous metal films are expected to have lower work functions than their crystalline counterparts.

*Chemical Modification*

There are several ways to selectively change the chemistry of thin metal films deposited on high-k substrates. It should be noted however, that the final chemistry of the film should be such that the film retains near metallic conductivity. As such, conducting metal nitrides, metal silicides and conducting metal oxides are potential candidates. This section describes a few techniques developed to implement this approach.

A very powerful yet straightforward way to introduce foreign elements into a film is ion implantation. Ion implantation is an attractive approach for a number of reasons. If the work function can indeed be modulated over the desired range, ion implantation can provide for a highly integrable and CMOS compatible process since photoresist masking can be used to selectively implant the desired ions. In addition, ion implantation is a technique that has been used in CMOS processing for decades and has achieved a high level of sophistication (very precise control of implantation parameters like beam currents, voltages and tilts is

possible). In addition, fairly sophisticated simulators are available to model implanted depth profiles in a variety of substrates with fairly high precision.

An alternative way to introduce nitrogen into metal films is to use a sacrificial layer as a solid diffusion source. In this approach, thin metal films (<50nm) such as low workfunction metals are deposited and subsequently capped with over-stoichiometric metal nitride layers (ie, $TiN_{1+x}$). The motivation behind such an approach is that the excess N in the capping layers will most likely diffuse out into the underlying metal films upon thermal annealing. The metal nitride capping films can thus be use as solid diffusion sources to introduce N into the metal films. Inversely, before metal deposition of a capping layer, a pretreatment of a sacrificial layer to the underlying metal film (ie, ion implantation of nitrogen or $-NH_2$ surface termination) could act as a solid diffusion layer upon subsequent metal deposition with thermal treatment. The shortcoming of the later approach is the high probability of N diffusing into the underlying film. For instance, diffusion of nitrogen into an underlying high-k dielectric film would lower its permittivity and lead to deleterious insulating properties.

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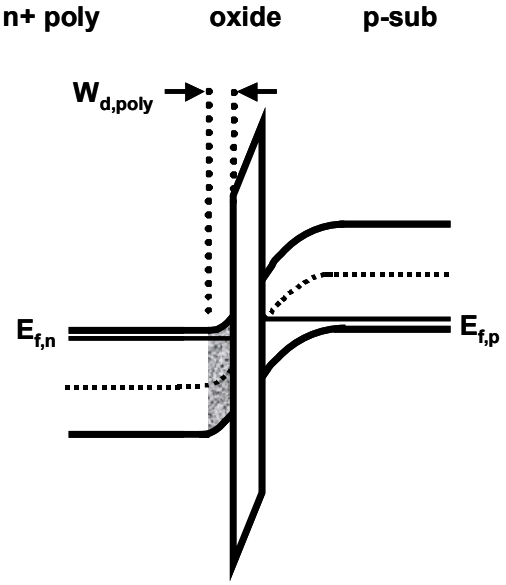


Figure 2.1: The poly-silicon gate depletion effect typically adds several angstroms to the dielectric EOT ($W_{d,poly}$) when the channel is in inversion

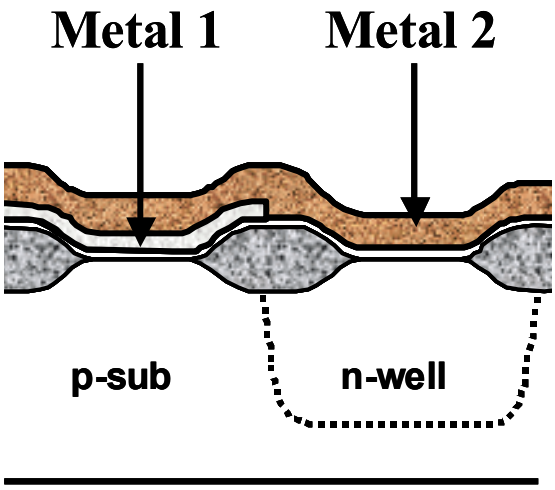


Figure 2.2: cross section of through the gate stack after two metal depositions.

# Chapter 3 Deposition and Characterization Techniques

## *Atomic Layer Deposition (ALD)*

### *Introduction*

Atomic layer deposition (ALD) is a self-limiting film growth process characterized by the alternate exposure of chemical species for deposition and surface preparation. However, ALD (originally based on atomic layer epitaxy, or ALE) had already been developed in the 1970's by Dr. Suntola and its first successful application was for the deposition of material for thin-film electroluminescent (TFEL) flat-panel displays [1]. Until the 1990's, ALD had been considered only for very limited semiconductor process applications because its biggest limitation has been its low growth rate, leading to a potential problem in mass production. ALD could not compete with other widely used thin film deposition techniques such as physical vapor deposition (PVD) and chemical vapor deposition (CVD). However, with the continued dimensional scaling of semiconductor devices, now clearly entering the nanoscale domain, the need for a deposition technique to produce very uniform, conformal thin films at lower temperatures is increasingly demanded to meet further CMOSFET scaling requirements.

### *ALD process*

In a "standard" CVD process a wafer or a group of wafers are placed in a vacuum chamber where the chemical percursors are thermally reacted at low pressure to deposit a film on the wafer. The deposition process is continuous – the vapors flow continuously into the chamber during the deposition process. The deposited film thickness depends on the temperature, pressure, gas flow volumes and uniformity, chemical depletion effects, and

time. Controlling all of these parameters to the level required for good thickness control of thin films is very difficult and exhaustive.

ALD deposits films using pulses of gas producing one atomic layer at a time. Within fairly wide process windows the deposited film thickness is only dependent on the number of deposition cycles providing extremely high uniformity and thickness control. In figure 3.1, the basic deposition process is illustrated for zirconium dioxide.

1. $ZrCl_4$ vapor is introduced into the process chamber.
2. the $ZrCl_4$ vapor forms an adsorbed monolayer on the surface of the wafer. Although not shown, following monolayer formation the chamber would be purged of $ZrCl_4$ vapor by an inert gas prior to the next step.
3. $H_2O$ vapor is introduced into the chamber.
4. The $H_2O$ vapor reacts with the $ZrCl_4$ surface monolayer to produce one monolayer of $ZrO_2$. Because only a monolayer of $ZrCl_4$ exists on the wafer surface, only one monolayer of $ZrO_2$ is produced making the process self-limited. Following $ZrO_2$ formation the chamber would be purged again and additional cycles would be performed as necessary to produce the desired film thickness.

ALD reactions are typically carried out in the 200°C to 400°C temperature range. If the deposition temperature is too high, film growth can be retarded by desorption of desired products or reactant (because chemical bonding cannot be sustained or the density of chemically reactive sites is reduced) or film growth can be enhanced by thermal decomposition of reactants (yielding a CVD like process). If the deposition temperature is too low, film growth can be retarded by insufficiently low thermal activated chemisorption leading to decreases in film forming reaction rates or the rate can be enhanced by reactant

condensation. The temperature window for maximum deposition rate is relatively wide compared to CVD processes that are much more temperature sensitive [1, 2]. Figure 3.2 schematically illustrates the allowable temperature window for ALD. Depending on the specific chemistry involved, ALD growth rates may also be reduced by desorption of adsorbed reactants during the purge steps [3].

Precursor must be volatile and thermally stable to ensure efficient transportation so that reactions will not be precursor transportation controlled (ie, critically controlled heating of gas feed lines to minimize condensation or unwanted precursor reactions). The vapor pressure of precursors must be high enough to completely fill the deposition chamber so that monolayer deposition takes place within a reasonable length of time (approximate vapor pressures of 0.1 Torr). Precursors must chemisorb onto the surface or rapidly react with surface groups, such as hydroxyl group on oxide surfaces, and react aggressively with the second vapor (whether a reducing or oxidizing vapor) to keep the deposition times short. Also, the self-limiting property of ALD will be lost if the precursor self-decomposes, etches the underlying film, or dissolve into the film.

The major limitation of ALD is its slowness: usually only a fraction of a monolayer is deposited in one cycle. This observation is generally attributed to steric hindrance of molecular precursors adsorbing on the surface, leading to saturation at less than one full monolayer of surface coverage [4]. Typical deposition rate are 100-300 nm $h^{-1}$. Therefore, it is not very practical to grow micrometer thick films. Fortunately, due to aggressive scaling of CMOSFET devices, the films require for future generation IC devices are very thin therefore negating the issue of ALD's slowness.

*Intrinsic Advantages of ALD*

This surface-controlled mechanism of film growth by the sequential deposition of monolayers (as discussed in the previous section) gives ALD some characteristic advantages over more traditional CVD and PVD techniques [1, 5]. In theory, since the final film thickness depends only on the number of ALD cycles used, atomic-scale thickness control is easily achieved (in practice, this prediction is not necessarily true for very thin films or polycrystalline materials). Because individual reactants are isolated from each other by purge or evacuation steps, highly reactive chemistries can be used, which allows for a wider selection of precursors than that traditionally available for CVD and lower deposition temperatures [6]. Self-limiting surface reactions in ALD allow for much better uniformity than CVD for films deposited on large-area wafers, because parts of the wafer exposed to a higher flux of reactants will not have thicker films, since the deposition during any individual pulse stops when a given area reaches saturation. Similarly, ALD deposition of sequential monolayers leads to much better conformality than PVD for films deposited on high aspect-ratio structures, meaning that the film thickness is constant over all parts of three-dimensional structures such as deep trenches, in which shadowing effects usually hinder PVD methods. Because of these advantages, ALD is beginning to replace CVD and PVD in the semiconductor industry for applications that require high conformality and uniformity, such as DRAM (Dynamic Random Access Memory) cells and back-end interconnect barriers and metallization [7]. Because of its excellent thickness control and uniformity, ALD could also the best deposition method for new high dielectric constant (or high-k) gate materials and alternative gate metals and geometries [8, 9].

***PALD Reactor***

My research will utilize a Plasma Atomic Layer Deposition (PALD) reactor, shown in figure 3.3, which was reconfigured from a previous triode PECVD system built to form high-k gate dielectric materials ($Ta_2O_5$ and $Al_2O_3$). The reactor has a load lock chamber in addition to the main reaction chamber so that a low base pressure of the order of $10^{-7}$ torr could be maintained. By applying a radio frequency (rf) power at 13.56 MHz to a copper coil with an inner diameter > 32 mm wrapped around a 32-mm quartz tube, a capacitive plasma can be generated. The substrates are placed on a 3" diameter stainless steel platen that can be mounted onto a specially designed stainless steel heating block. The platen is ~2 cm below a 0.25" stainless steel precursor feed line. The heater was made from six - 200 Watt, 120 Volt cartridge heaters electrically connected in parallel and inserted into the heating block which conductively heat directly on the back of the substrate platen and was easily heated to 500°C. The temperature was measured with a thermocouple wire inside a grounded stainless steel tube, which contacted inside the heater block within proximity of its center core. A PID controller that sends a 4-20 mA current to a silicon-controlled rectifier, SCR, varies the power to the cartridge heaters from a 110 Volt 30 Amp outlet. This new substrate-heating configuration is to replace an older inadequate lamp-heating configuration because the older heater kept shorting during deposition of conductive films. Recent ALD Ru deposition experiments with the previous heater led to *conductive* films being deposited on the ceramic spacers (used to prevent the lamps form shorting with the mounting assembly attached to the reactor wall), which shorted the electrical load from the lamps to the reactor. Consequently, burning the electrical components in the operating control panel and melting the copper electrodes (located inside the chamber).

The PALD reactor operates at the following parameters ranges. Pressure can be varies from 0.2-2 torr, and rf power from 1-1000 W (although typical operating power is limited to <400 W to avoid melting the o-rings in ultra Torr fitting on the quartz tube due to extensive heating from higher wattages). The total flow rate of gaseous reactants is usually between 100-2000 sccm resulting in residence times ~3-15 seconds since the volume the reactor is approximately 16 liters. Process gases, including $H_2$, $N_2$, $O_2$, Ar, and solid metallorganic precursors (contained in a sublimation cell and using Ar as a carrier gas), are delivered through heated lines (90°C - 200°C) to avoid condensation, and valve switching is controlled by four Omega timers to allow gas pulse cycling for ALD processes. The substrate temperatures are in the range between room temperature to 500°C.

Additionally, a Physical Electronics' (PHI's) Model 3017 Auger Electron Spectroscopy Subsystem with a 5keV, 10μA electron beam and a high sensitivity Cylindrical Mirror Analyzer (CMA) was attached to the loadlock to accommodate online chemical analysis of gate metal ALD films. This addition facilitated the necessity for an in vacuum sample transfer system utilizing a MDC Cab-Fast® platen fork and 3" diameter sample platen design.

***Film Characterization***

On-line *Auger Electron Spectroscopy (AES)*

Auger electron spectroscopy (AES) uses a focused electron beam of 3-5 keV to excite Auger electrons out of outer shells of the atoms in the film. The energy of Auger electrons is measured to determine the elements present in the sample. Since Auger electrons are readily absorbed in all solids, the Auger technique samples a depth of typically 5 to 50 Å. The most frequent use for AES is a depth information method by obtaining a spectrum from the

surface, then deposit a fixed number of atomic layers by ALD and to repeat the analysis until the desired depth has been reached [10]. In this way, the variation in composition with depth can be determined. Typical AES depth profile analysis are obtain by depositing a thick ALD film followed by cycling between obtaining AES spectra (typically 5-50 Å) and sputtering a few atomic layers until the desired film depth had been reached. The advantage to our new analysis configuration is a non-destructive method in which the samples can be used for further analysis with complimentary analytical instruments and the sample can be further developed through addition processing.

*Fourier Transform Infrared Spectroscopy (FT-IR)*

Chemical bonds having a dipole moment absorb light on the infrared range of the spectrum. Fourier transform infrared spectroscopy (FTIR) measures the vibrational modes of various bonds. Hence IR absorption analysis is an excellent tool to observe the water adsorption (OH groups) on high-k dielectric films. The instrument is a Nicolet Model 750 and has a wavenumber range of 400-4000 $cm^{-1}$. Chemically bonded groups in the dielectric films have vibrational frequencies in this range and each group will absorb light at a specific range of wavenumber values.

*X-ray Photoelectron Spectroscopy (XPS)*

X-ray photoelectron spectroscopy (XPS) is another surface analysis technique where an incident X-ray beam results in the emission of photoelectrons from the surface (and near surface region) of the material and the binding energy of these photoelectrons is used to identify different elements near the surface region. Collecting the electrons that emerge at small angles to the surface plane increases the surface sensitivity of photoelectron spectroscopy. These electrons must travel a longer distance in the solid, and therefore they

are more likely to be absorbed unless they are generated at the surface or near the surface region. The electron kinetic energy is related to the incident X-ray energy as:

$$E_{kin} \approx h\nu - E_B$$

where $E_B$ is the binding energy of the electron and is characteristic of the atom from which it was emitted. These values are well tabulated in literature [11]. The shift in the binding energy corresponds to different oxidation states of the atom. Hence XPS can be used to establish what elements are present and the bonding environment on the surface.

*Rutherford Backscattering Spectroscopy (RBS)*

Rutherford backscattering spectroscopy (RBS), also known as high-energy ion (back)-scattering spectrometry (HEIS), is based on bombarding a sample with energetic ions (typically He ions of 1 to 3 MeV energy) and measuring the energy of the backscattered He ions [12]. It is quantitative without recourse to calibrated standards. It can determine the masses of the elements in the film, their depth profile over distances from 100Å to several microns from the surface, and the crystalline structure in a nondestructive way. The depth resolution is on the order of 100 Å. RBS is particularly suitable for heavy elements on light substrates. Its major weakness is the difficulty of measuring light elements on a heavy substrate

*Transmission Electron Microscopy (TEM)*

Transmission electron microscopy (TEM) provides extremely high resolution, approaching 1.5 Å. Since the incident electron beam must pass entirely through the section, which needs to be prepared only ten to hundreds of nanometers thick, the sample preparation is a real challenge [13]. The three primary imaging modes are bright-field, dark-field and high-resolution microscopy. In particular, high resolution TEM (HRTEM) gives structural

information on the atomic size level and has become very important for interface analysis. Physical thickness, presence of interface layers or smoothness of an interface and crystallinity of a film can be obtained from TEM. However, small crystallites may amorphize from ion beam bombardment in sample preparation.

Electron energy loss spectroscopy (EELS) is the analysis of the distribution of electron energies for electrons transmitted through the film [12]. EELS is very sensitive to low-Z (Z=atomic number) elements ($Z \leq 10$). It is mainly used to microanalytical and structural information approaching the very high resolution of the electron beam.

*Surface Profilometry*

A Tencor Alpha-Step 500 surface profilometer will be used to physically measure film thickness. An apparatus with a diamond needle stylus mechanically moves across the sample and traces the topography of the film so that the profilometer can measure surface roughness or the height of a step (> 80 Å). The step is made by placing a cover slide on the silicon sample before deposition that serves as a shadow mask. For deposition conditions that involve the precursors with low sticking coefficient or high surface mobility, a step created by the cover slide can be difficult to achieve because the precursors or reactants may diffuse underneath the slide. In this situation, the photoresist is applied to the film, and the film dipped into a buffered HF oxide etch (BOE) solution until the solution droplets bead up on the uncovered silicon surface since a bare silicon surface is hydrophobic and the oxide is hydrophilic. In fact, the etch rate is also a parameter of interest. Then the photoresist is removed by trichloroethylene or acetone, and the dielectric step remaining is used to determine the thickness.

*Ellipsometry*

Ellipsometry can also be used to determine the thickness of films as well as optical constants. Spectroscopic ellipsometry (SE), like single wave ellipsometry but using multiple wavelengths, is a true contact-less, noninvasive technique measuring the change in polarization state of light reflected from the surface of a sample. A VASE SE system (J. A. Woollam Co., Inc.) with combination of variable angle of incidence is used to measure the aluminate films. However some difficulties may be encountered when measuring thin films (<100Å). This may be due to the limitations of ellipsometry on accuracy and uncertainty of the calculated film parameters which stem from 1) the choice of starting assumptions during data analysis, i.e., there are different dispersion relations or dielectric functions for the dielectric film, none of which is taken to be the standard; and 2) the inevitable correlation of variables when extracting multiple variables in the very thin film regime [14]. This may also be from the uncertain composition of the gate metal films, and the presence of an interface layer at the metal/high-k interface. Since very thin films (20-50 Å) of high-k dielectrics are important to the CMOS industry, the ellipsometry must be combined with other methods for thickness measurement, such as transmission electron microscopy (TEM).

*Electrical measurement on MOS Capacitors*

High- and low frequency capacitance-voltage (C-V) measurements can be performed on MOS capacitors (MOSCAPs). The parameters that can be extracted include flat band voltage ($V_{fb}$), threshold voltage ($V_{th}$), doping concentration of the substrate, fixed charge ($Q_f$), interface traps density ($D_{it}$), and oxide thickness ($t_{ox}$). The dielectric constant is obtained by the equation $\varepsilon = Ct_{ox}/\varepsilon_0 A$, where C is the capacitance, A is the electrode area, $\varepsilon_0$ is the vacuum permittivity. The fixed oxide charge is deduced by the shift in the measured

$V_{fb}$ from the ideal case where $V_{fb} = \Phi_{ms}$, the work function difference of the semiconductor and metal. As the gate dielectric thickness is less than 2.5 nm, a universal model by Hauser for high-frequency C-V data can be used to extract parameters of interest [15].

MOSCAPs with field oxide isolation and contact pad are better than those made from shadow masks and the use of mercury probe. The devices made from shadow masks suffer various problems including large corner electrical field, humidity effect, charging from the environment and processing damage. The area of the devices cannot be fabricated very small ($<2.5\times10^{-5}$ $cm^2$) due to the difficulties in probing small dots.

Current-voltage (I-V) measurements can also be performed on MOSCAPs. Leakage current and mechanism (Fowler-Nordheim tunneling or direct tunneling) may be extracted.

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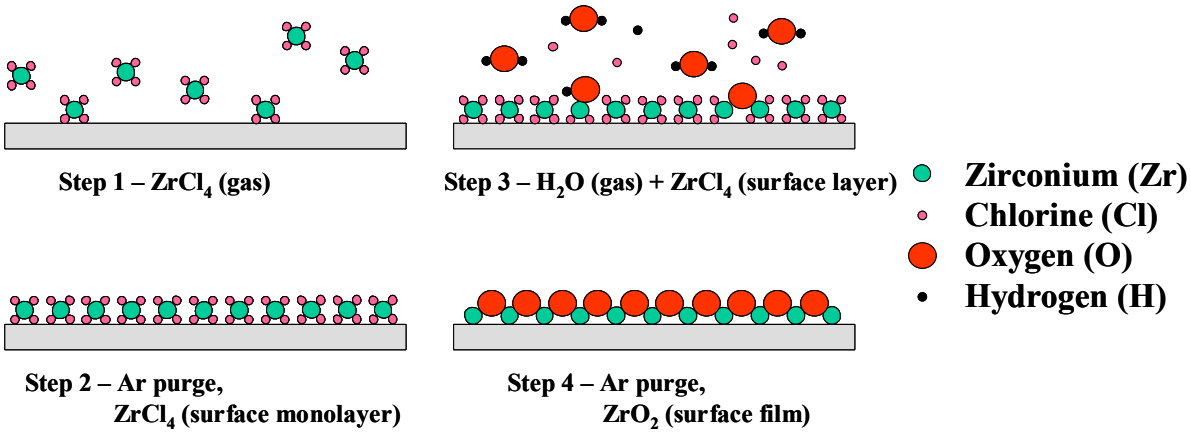


Figure 3.1: Atomic Layer Deposition of $ZrO_2$

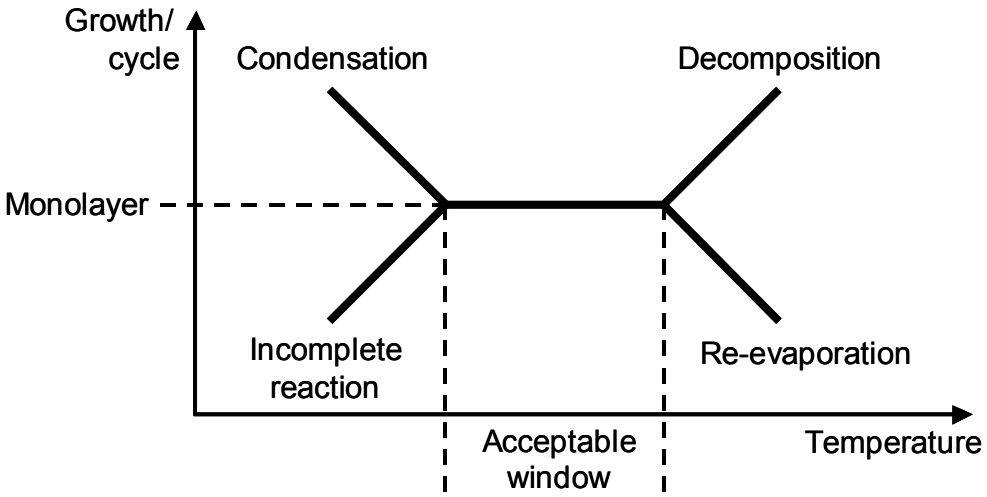


Figure 3.2: Typical process window for atomic layer deposition.

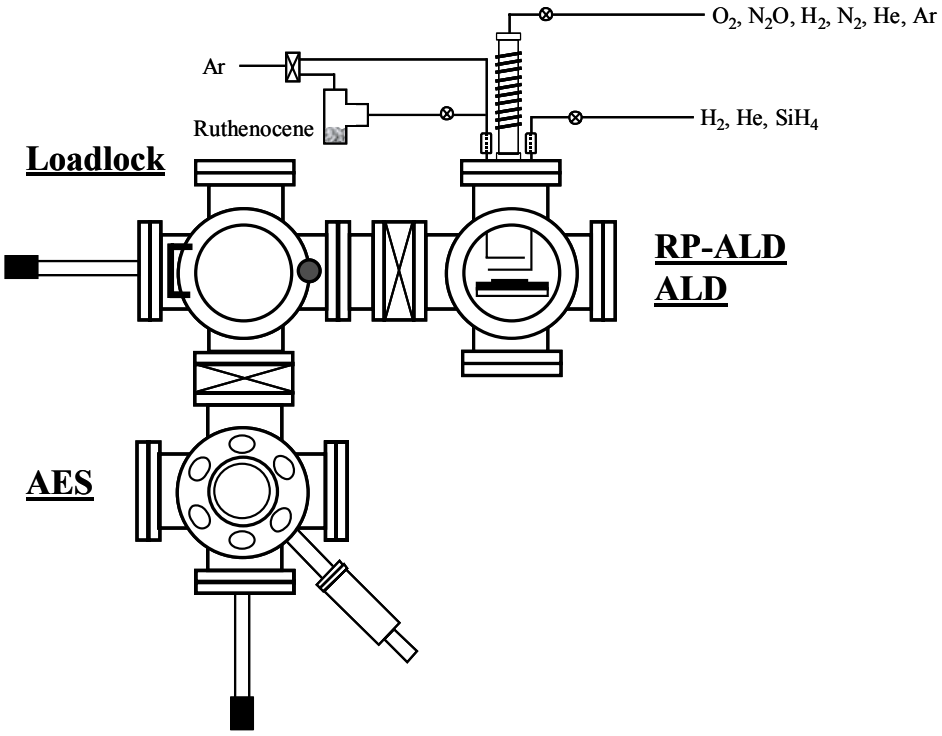


Figure 3.3: Cluster tool including remote plasma atomic layer deposition (RP-ALD) and thermal atomic layer deposition (ALD) capabilities. Including the capability for *online* Auger Electron Spectroscopy (AES).

# Chapter 4

## Charge Compensation and Thermal Stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ and $(Y_2O_3)_x(Al_2O_3)_{1-x}$ formed by oxidation of $Hf_x:Al_{1-x}$ and $Y_x:Al_{1-x}$ mixtures on Si

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## Abstract

The dielectric properties of Yttrium:Aluminum & Hafnium:Aluminum oxide mixtures were investigated. Capacitance versus voltage (C-V) analysis indicates that the addition of Al to Hf and Y oxides results in a positive shift in flatband voltage with increasing Al concentration for both sets of mixtures. Also, C-V measurements show the ability to tune the flatband voltage of high-k oxides by means of aluminum alloying. Yttrium aluminates (when compared to hafnium aluminates) were more sensitive to flatband voltage tuning where the flatband voltage varied from –1.2V to –0.7V (as compared to –0.8 to –0.6V for hafnium aluminates). Additionally, the rate of silicon oxidation varied, EOT tuning, by aluminum alloying. XPS investigation of Y(or Hf) and Al chemical states of the alloy films indicate the films are a homogenous mixture of $HfO_2$ (or $Y_2O_3$) and $Al_2O_3$.

***Introduction***

The International Technology Roadmap for Semiconductors (ITRS) suggests a gate dielectric thickness below 1.0nm for the 65nm generation by 2007 if industry continues to use silicon oxynitride [1]. Because of the aggressive scaling of complementary metal oxide semiconductor (CMOS) devices, $SiO_2$ gate dielectrics are approaching their physical limits due to direct charge tunneling as dielectric thickness decreases. In order to achieve the desired device performance by reducing leakage currents, a physically thicker film is allowed with an alternative high-k material. Therefore, the study of alternative high-k gate dielectrics with reduced gate leakage currents appears critical.

Initially there was intense effort in the search for a high-k dielectric replacement for $SiO_2$, with $Y_2O_3$, $Al_2O_3$, $HfO_2$, $ZrO_2$, and their silicate and aluminate forms as the leading candidates for an alternative high-k dielectric [2-4]. The assumption for the replacement is materials with a higher dielectric constant than $SiO_2$ will reduce tunneling. Theoretically, these oxides are stable on Si surface at equilibrium however since metal deposition processes are under non-equilibrium conditions all high-k dielectrics (with the important exception of Al) have a significant tendency to form large interfacial layers upon high temperature post deposition anneals. Thus meeting appreciable equivalent oxide thickness have proven to be very difficult since any lower-k interfacial layer will ultimately decrease the overall capacitance of the dielectric. Additionally, most high-k materials will become crystalline or poly-crystalline during post deposition anneals in which grain boundaries provide current pathways and degrades the gate oxide ability to electrically separate the gate electrode from the channel.

Currently, several chip manufacturers have decided to replace $SiO_2$ with hafnium-based dielectrics. As with $SiO_2$, these first replacements will eventually reach their physical limits facilitating the need for another replacement. Recently, transition metal aluminates such as $(HfO_2)_x(Al_2O_3)_{1-X}$ [5-10], $(ZrO_2)_x(Al_2O_3)_{1-X}$ [11, 12] , and $(La_2O_3)_x(Al_2O_3)_{1-X}$ [13-19] have received much attention. The theory of pseudobinary alloys is to mix a high-k crystalline material such as $HfO_2$, $ZrO_2$, or $La_2O_3$, with a lower-k amorphous material to create a more thermodynamically stable dielectric on silicon. Additionally, $Al_2O_3$ [20] and recently $LaAlO_3$ [15] have demonstrated an abrupt interface with silicon. Therefore, alloying aluminum with high-k transition metal oxides may provide a more abrupt interface than the end member oxides. However, the permittivity for the pseudobinary alloy is lower than the transition metal oxide (high-k material) but this tradeoff may be worth the thermodynamic stability for improved device performance. Previous studies have shown that intrinsic negative fixed charge is present in $Al_2O_3$/Si interfaces[21] and intrinsic positive fixed charge in $Y_2O_3$(or $HfO_2$)/Si interfaces[3]. Therefore alloying transition metal oxides with aluminum oxide is a possible way to achieve charge neutrality at the high-k/Si interface. Such charge compensation may promote electrical tuning such as flatband voltage, $V_{FB}$.

Charge compensation (chemical modification) of transition metal oxide films by means of aluminum alloying to form transition metal aluminates, specifically $YAlO_x$ ($LaAlO_x$) and $HfAlO_x$, may improve the stability and electronic performance of the dielectric/silicon interface in electronic devices. Charge compensation is based on the idea of combining a dielectric with positive fixed charge, $+Q_f$, (oxides of yttrium, lanthanum, and hafnium) and a dielectric with negative fixed charge, $-Q_f$, (aluminum oxide) to create a charge balanced dielectric. For an ideal metal-insulator-semiconductor (MIS) structure, at

V=0 applied voltage on the metal gate, the work function difference between the metal and the substrate, $\Phi_{MS}$, is zero.

$$\Phi_{MS} = \Phi_M - \left( \chi + \frac{E_g}{2q} - \Psi_B \right) = 0 \text{ ; for } n\text{-type} \tag{7}$$

$$\Phi_{MS} = \Phi_M - \left( \chi + \frac{E_g}{2q} + \Psi_B \right) = 0 \text{ ; for } p\text{-type} \tag{8}$$

where $\Phi_M$ is the metal work function, $\chi$ is the semiconductor electron affinity, $E_g$ is the semiconductor band gap, $\Phi_B$ is the potential barrier between the metal and dielectric, and $\Psi_B$ is the potential difference between the Fermi level and the intrinsic Fermi level. Under these conditions, the energy bands are flat and the $V=V_{FB}=0$. However, due to fixed charge in dielectric (especially high-k materials), the measured $V_{FB}$ can be expressed as:

$$V_{FB} = \Phi_{MS} \pm \left( \frac{Q_f}{C_{acc}} \right) \tag{9}$$

where $C_{acc}$ is the measured capacitance in accumulation. Therefore alternative high-k dielectrics require some voltage bias to offset the band bending due to fixed charge to achieve flatband conditions. One method to achieve flatband conditions in high-k dielectrics without the necessary voltage biasing is to mix a dielectric with negative fixed charge (ie $Al_2O_3$) with a dielectric having positive fixed charge (ie $HfO_2$ or $Y_2O_3$). Alloying two dielectrics with the appropriate compositional ratio (since the magnitude of negative fixed charge for $Al_2O_3$ will be different than the magnitude of positive fixed charge for $HfO_2$ or $Y_2O_3$) should net a zero fixed charge. Also, for instances where the $\Phi_{MS}$ may not be equal to zero the dielectric alloy should have the appropriate composition so that the net fixed charge will offset the $\Phi_{MS}$ value which will allow us to operate at $V_{FB}=0$.

The primary focus in this work is to achieve a better understanding of the fundamental issues concerning the constitutive and electrical behavior of transition metal aluminate dielectrics. Therefore, we will concentrate on obtaining fundamental chemical and electrical data pertaining to the bond formation and bond arrangement at the interfaces of a metal gate/M:Al/Si substrate structure with M=Y, La, or Hf using remote PECVD and PVD with post deposition anneals as possible routes to optimal interface formation.

***Experimental Approach***

Thin films of transition metal oxides ($Y_2O_3$ and $HfO_2$) , and films with varying concentration of Y(or HF):Al metal mixtures were formed by oxidation of metal mixtures. Metal mixtures were deposited using ultra high vacuum physical vapor deposition, and oxidation was performed by *ex-situ* furnace oxidation in dry air. The Si(100) substrates were prepared by J.T. Baker clean for 5 min, deionized water (DI) rinse for 5min, and buffer oxide etch (BOE) for 1 min. They were blown dry with nitrogen and placed in the PVD loadlock.

The Y, Hf, and Al targets were purchased from Target Materials with a 99.99%, 99.5%, and 99.999% purity, respectively. Variations in homogeneous mixtures of the deposited metal films were accomplished by varying the r.f. power and sputtering for a fixed amount of time based on measured single metal deposition rates. Metal oxide semiconductor capacitors were formed with 2000Å Al electrodes by shadow mask Al metal evaporation.

Film characterization was preformed using X-ray Photoelectron Spectroscopy (XPS) and capacitance-voltage (C-V) analysis. XPS was conducted on a Riber LAS3000 instrument equipped with a single-pass, cylindrical mirror (MAC2) analyzer. An Mg Kα (hν=1253.6 eV), non-monochromatic X-ray source at a 90° take-off angle was used for all measurements. Step sizes of 1.0eV and 0.1eV were used to obtain survey and detailed XPS spectra, respectively. C-V measurements were conducted on an HP4284 LCR with a 1 MHz sweeping frequency from –3 to 1 Volt. Capacitor areas were measured using a Nikon Eclipse Optical Microscope equipped with a digital camera. Small electrode areas, ~$1x10^{-5}cm^2$, were measured to avoid instrumental errors associated with large areas. Equivalent oxide thickness (EOT) and flatband voltage were extracted from C-V data using the NCSU CV program [22].

***Results and Discussion***

Y:Al & Hf:Al films with thickness ~25Å were deposited on H terminated Si(100) substrates and oxidized *ex-situ* at 400 to 700°C in dry air at atmospheric pressure for 2 minutes. XPS was then used to analyze the surface composition of the films and spectral regions are displayed in Figures 4.1 and 4.2 for Y:Al and Hf:Al mixtures, respectively. The films were sufficiently thin enough to detect the 99.3eV Si substrate peak in the Si 2p spectra (except for the 100% Hf film). Consider first the Y:Al films in Figure 4.1. For the Si 2p spectra in Figure 4.1a the feature at 99.3eV is from the Si substrate. The intensity of the substrate peak decreases with decreasing Y content [increasing Al fraction] consistent with increasing film thickness with increasing Al content. The feature near 103eV is due to oxidized silicon either at the dielectric/silicon interface and/or oxidized Si in the dielectric film bulk. The relative size of the Si-O feature increases with increasing Al content. The position of the Si-O peak near 103eV shifts to lower binding energy as Y content increases from 0 to 78%, then it shifts to higher binding energy as Y content increases further. The shift to lower binding energy is likely due to a relatively large amount of silicon in the film bulk (ie, formation on Y-silicate) for low Al content[4]. The shift to higher binding energy is consistent with a relatively thick interfacial oxide layer for high Al content. This interpretation is also consistent with the position of the O1s peak for these films, shown in Figure 4.1b.

For the Hf case, shown in Figure 4.2a-b, the Si-O peak intensity decreases with increasing Hf content and peak position stays nearly fixed at 103.0eV. The O1s peak shifts smoothly from 533.0eV to 531.5eV with increasing Hf content. This data is consistent with

silicate at the dielectric/silicon interface, but with lower silicon content as compared to the Y samples.

The electrical properties of Y:Al and Hf:Al mixtures were evaluated by C-V measurements with Al electrodes without a forming gas anneal. The effects of temperature on flatband voltage for $Y_2O_3$ and $HfO_2$ films are shown in Figure 4.3. The measurements were made with voltage sweeps from depletion to accumulation at 1 MHz. With increasing anneal temperature, the flatband voltage increases positively for $Y_2O_3$ and negatively for $HfO_2$ films. The flatband voltage for $HfO_2$ films were more sensitive to anneal temperature than the $Y_2O_3$ films. This can be seen in Fig. 4.3 where $V_{FB}$ is plotted versus anneal temperature. The magnitude of negative shift for $HfO_2$ is greater than the positive shift for $Y_2O_3$. The flatband voltage shifted from –0.18V to –0.78V for the hafnium films and –1.22V to –1.18V for the yttrium films over the temperature range studied. However, both series show a negative flatband shift indicating positive fixed charge. No attempt was made to distinguish between bulk and interface trapped charge.

The effects of anneal temperature for the 42% Y:Al and 70% Hf:Al mixtures can be seen in Figure 4.4. Similar effects were observed for the mixtures as for the elemental oxides. Hafnium based mixtures were more sensitive to temperature than yttrium based mixtures. The flatband voltage shifted from –0.55V to –0.61V for the hafnium based films and –0.78V to –0.76V for the yttrium based films over the temperature range. All films show negative flatband voltage indicating positive fixed charge. Figures 4.5 & 4.6 illustrate the hysteresis of 7mV for 42% Y and 21mV for 70% Hf films, respectively, which is significantly less than the shifts observed by annealing.

The ability to tune flatband voltage with Al alloying was also investigated. Figure 4.7 shows the effects of Al alloying on Yttrium and Hafnium oxide films. All films were annealed at 700°C in air for 2 min (except 500°C for 100% Al) and $V_{FB}$ was characterized as a function of alloy composition. A positive shift in flatband voltage was observed for both series with increasing Al composition, with yttrium films showing a larger sensitivity to Al alloying. A zero flatband voltage was never achieved in any of the films possibly due to dangling bonds at the silicon interface. Dangling bonds are usually associated with lattice mismatch between high-k dielectric films in contact with Si substrate, which is consistent with the negative voltages shown in Figures 4.3c. It may be possible to recover the flatband condition via $H_2$ forming gas anneal to passivate the observed dangling bonds.

The effects of Al alloying on equivalent oxide thickness (EOT) was also investigated. There was an increase in EOT with increasing temperature, in most cases, for $YAlO_x$ and $HfAlO_x$ films seen in figures 4.8 and 4.9, respectively. This is likely because at higher temperatures, oxygen can diffuse with relative ease through both deposited metal mixture series and react with the silicon surface forming an interfacial silicate layer. This is consistent with the binding energy peak shifts in the XPS data. Also for several films, we observed a systematic increase in EOT with decreasing aluminum composition possibly due to the higher reactivity of Y (or Hf) metals to OH groups than the Al metals.

***Conclusions***

Yttrium:Aliminum & Hafnium:Aluminum mixtures were grown on H-passivated Si(100) substrates by PVD and *ex-situ* furnace oxidation in dry air. XPS analysis revealed that silicon consumption was evident regardless of Al composition. C-V measurements show the ability to tune the flatband voltage of high-k oxides by means of aluminum alloying. Yttrium aluminates (when compared to hafnium aluminates) were more sensitive to flatband voltage tuning where the flatband voltage varied from –1.2V to –0.7V (as compared to –0.8 to –0.6V for hafnium aluminates). Also, the rate of silicon oxidation varied, EOT tuning, by aluminum alloying. The negative shift in flatband voltages were attributed to lattice mismatch between the high-k/silicon interface resulting in dangling bond formation.

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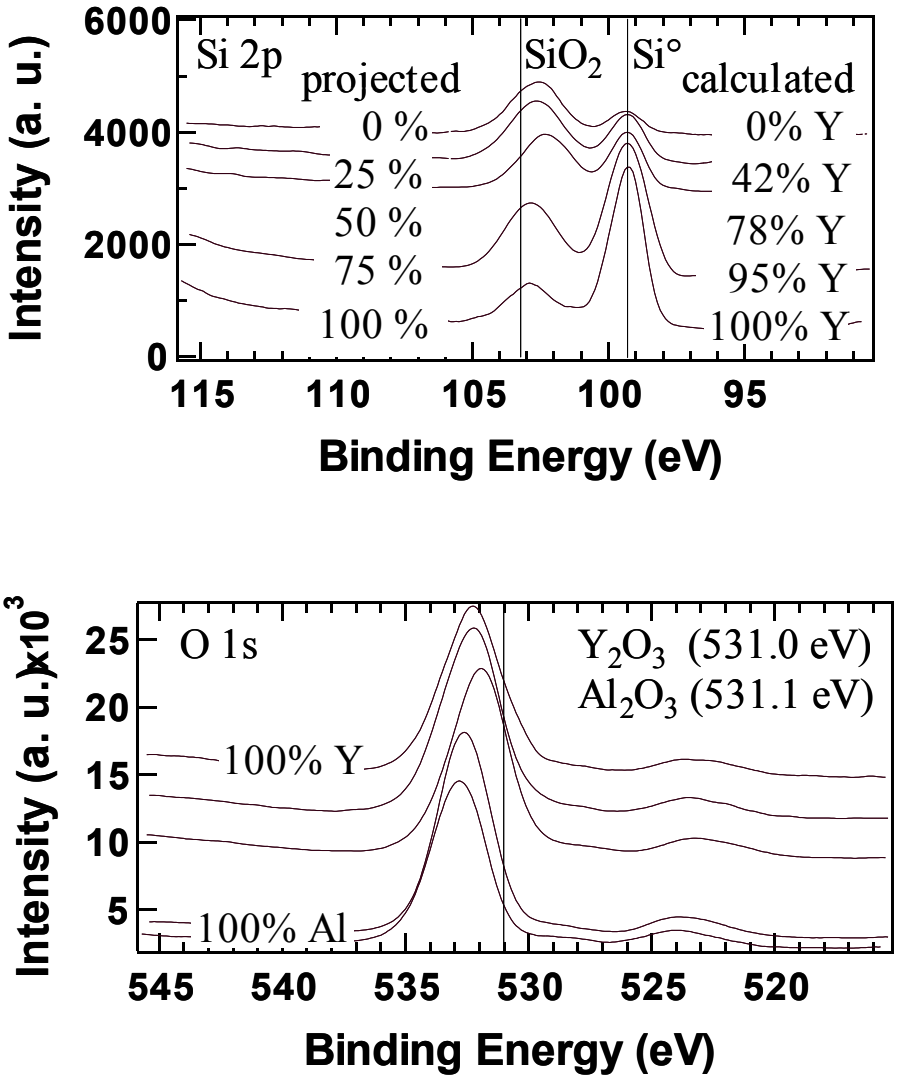


Figure 4.1: XPS of PVD Y and Al metals.

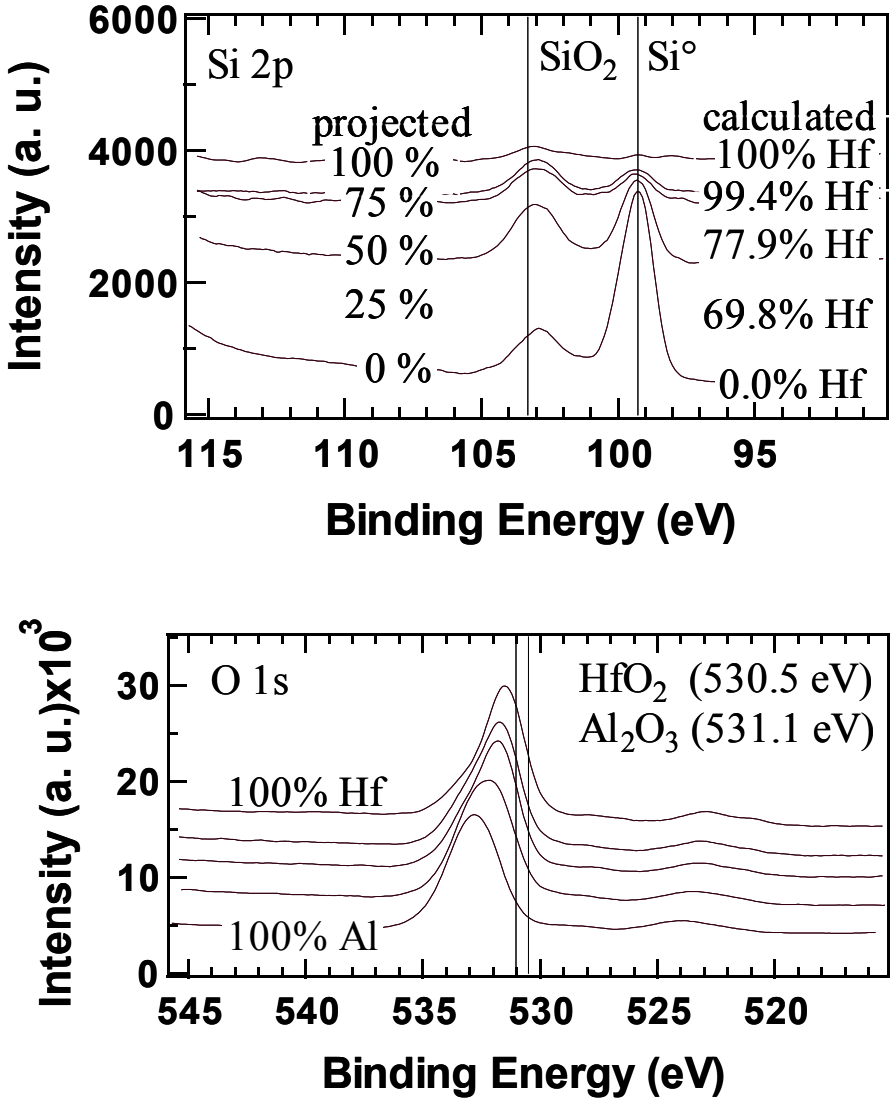


Figure 4.2: XPS of PVD Hf and Al metals.

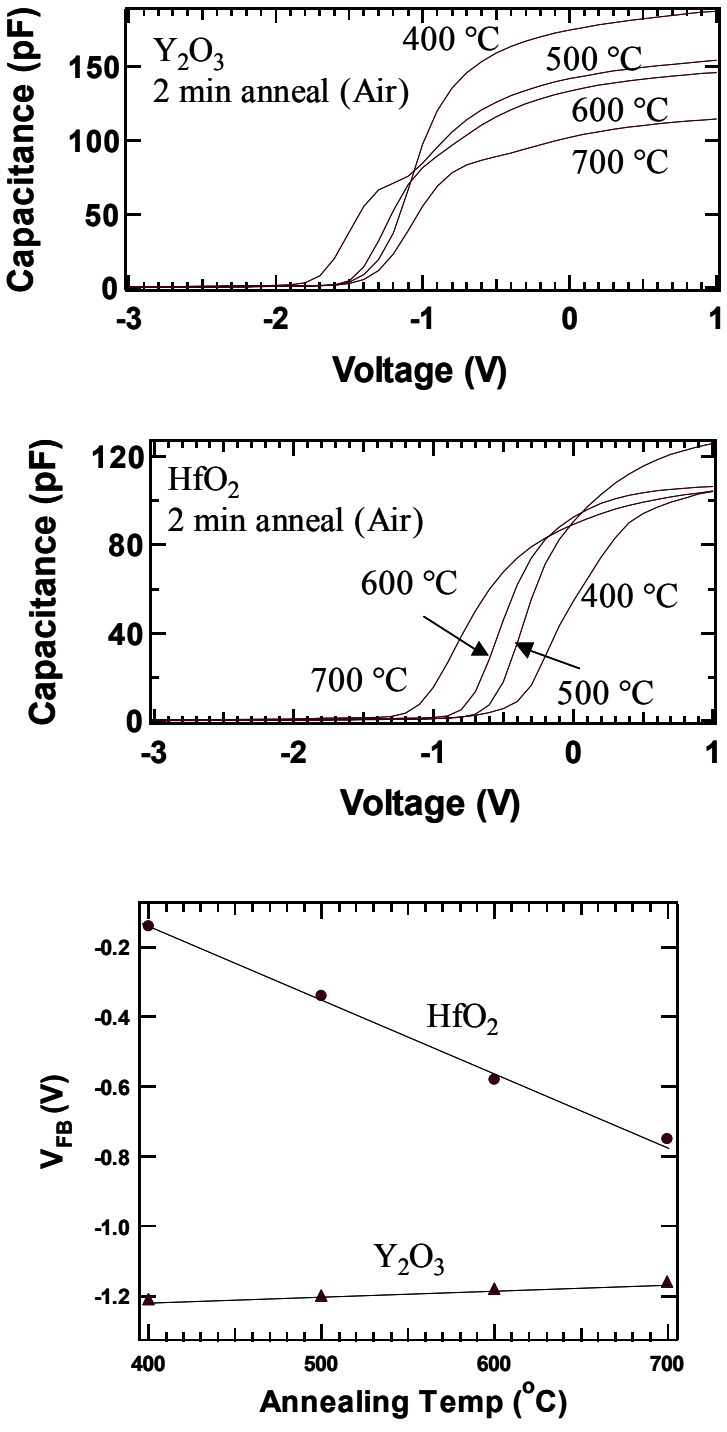


Figure 4.3: Effects of temperature on flatband voltage for end member $Y_2O_3$ and $HfO_2$ films

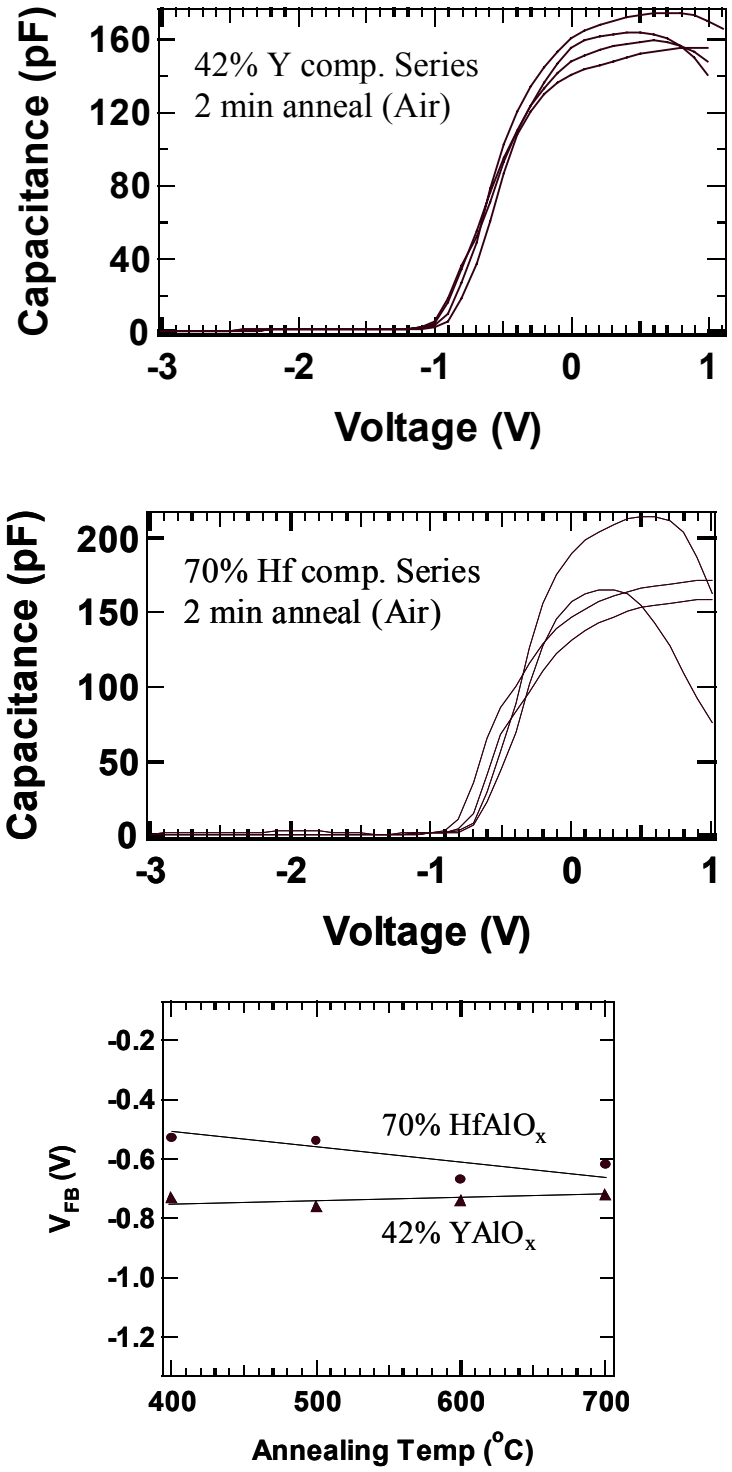


Figure 4.4: Effects of temperature on flatband voltage for 42% $Y_2O_3$ and 70% $HfO_2$ films

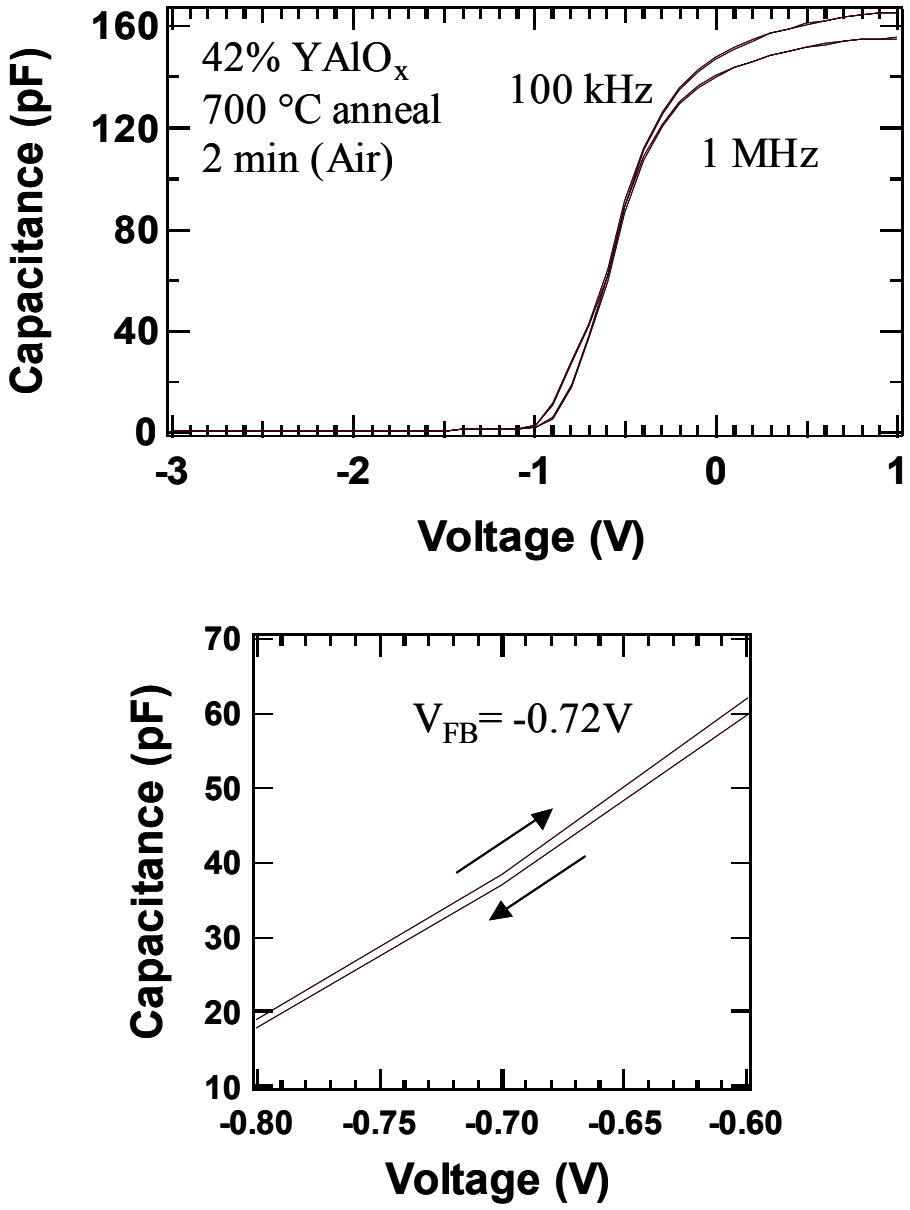


Figure 4.5: Hysteresis for 42% $YAlO_x$ film with flatband voltage, $V_{FB}$.

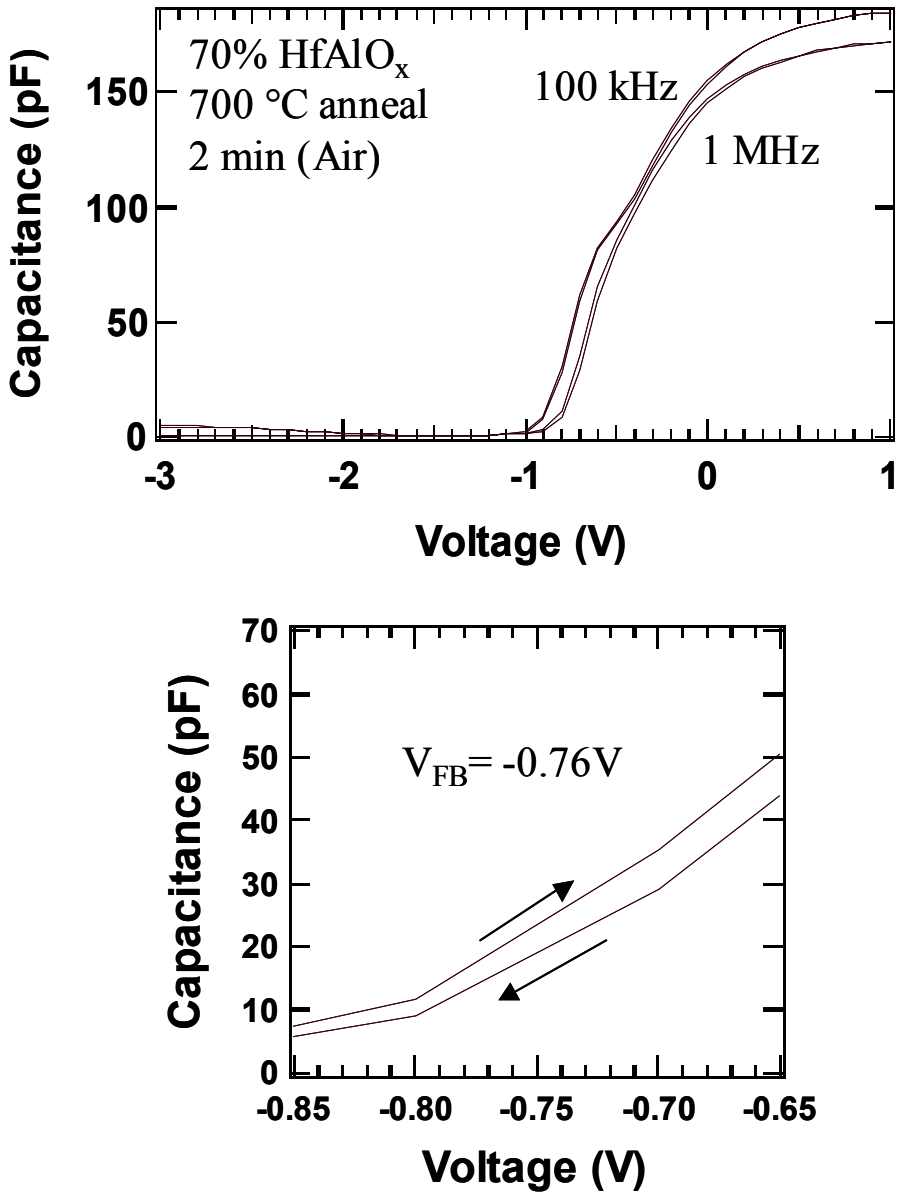


Figure 4.6: Hysteresis for 70% $HfAlO_x$ film with flatband voltage, $V_{FB}$.

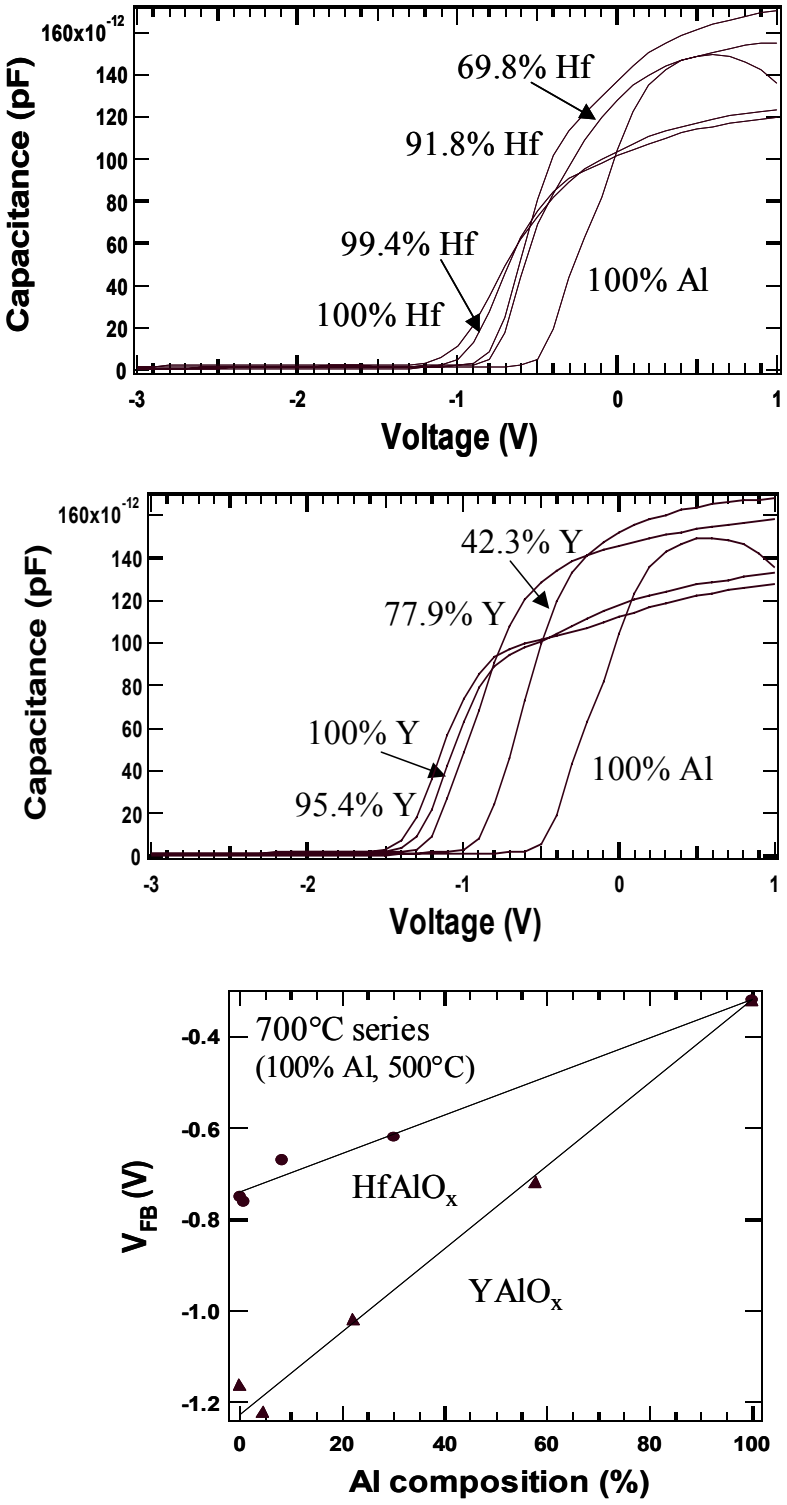


Figure 4.7: Effects of Al alloying on Yttrium and Hafnium films.

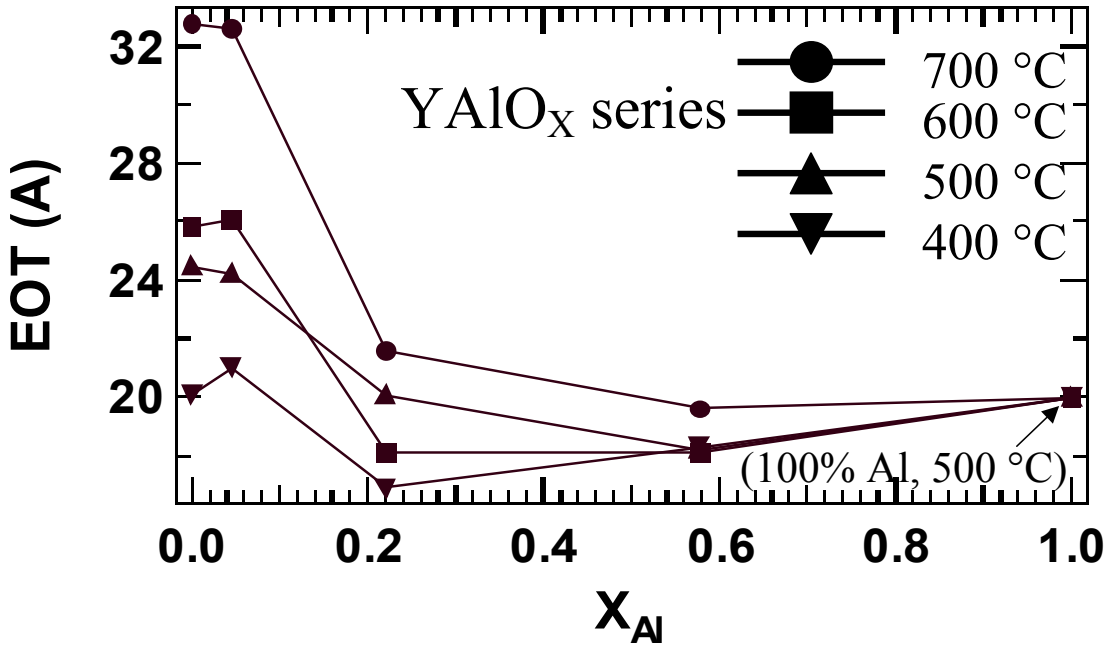


Figure 4.8: The effect of aluminum alloying on equivalent oxide thickness (EOT) for $YAlO_x$ films.

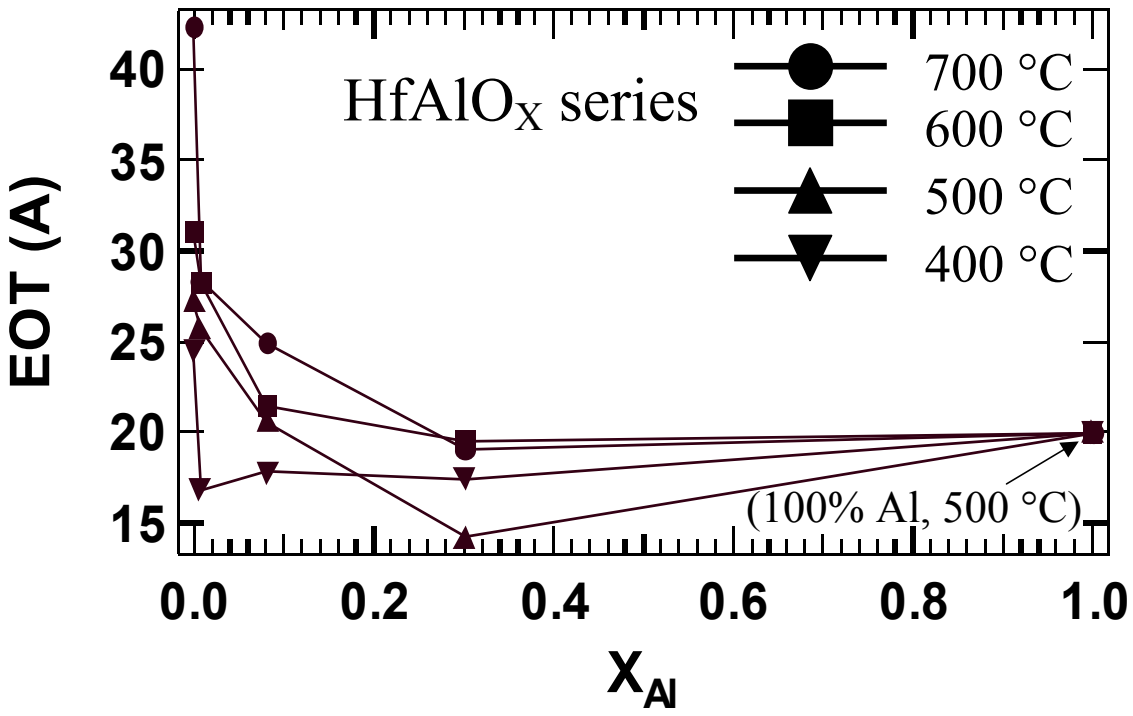


Figure 4.9: The effect of aluminum alloying on equivalent oxide thickness (EOT) for $HfAlO_x$ films.

# Chapter 5

## Chemical Vapor Deposition of $RuO_2$ for Gate Electrode Applications

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## Abstract

Ruthenium-based metals are potential candidates for gate electrodes in advanced gate stack applications. The detailed structure of the interface between high-k dielectrics and the gate metal will be important to maintain low equivalent oxide thickness, but the effect of metal deposition on the high-k/metal interface structure is not known. We have deposited $RuO_2$ metal from Tris-tetramethyl-heptadianato Ru (Ru TMHD) introduced downstream from a remote $N_2O$ plasma at 365 and 500°C, and examined the deposited film and interface structure using Auger and X-ray photoelectron spectroscopies. The films show some evidence for N and C incorporation, consistent with the 250°C decomposition temperature of the Ru TMHD. Based on AES results, the O/Ru ratio is larger for the films deposited at higher temperature. Because of the difference between the oxidizing and reducing environments in CVD processing, we expect that metallic oxides such as $RuO_2$ will result in different metal/dielectric interface structure than for elemental metal/dielectric interfaces. To examine the role of deposition chemistry on interface structure, several thicknesses of $RuO_2$ have been deposited by plasma CVD on $HfO_2$ formed in our lab by atomic layer deposition.

The effect of $HfO_2$ surface structure, and the trends in $RuO_2$ composition with film thickness determined using AES and XPS will be presented and discussed.

## Introduction

Currently, conventional complimentary metal oxide semiconductor (CMOS) technology uses heavily doped polycrystalline silicon (poly-Si) as a conductive gate material on top of the dielectric. A major problem with this approach is the poly-Si is not completely activated and has some finite capacitance because it is not completely metallic. This polysilicon gate depletion effect, or "poly-depletion", adds a series capacitance with an EOT of 3-7Å to the gate stack, which becomes a significant problem as the gate stacks scales below EOT values of 15Å. Other challenges with the continuous use of poly-Si gates with further scaling, in addition to poly-depletion and boron penetration, are reactions with high-k materials, and high poly-Si sheet resistance [1, 2].

One suggestion to alleviate these problems would be to substitute the poly-Si gates with metal gates, one with a work function close to the Si valence band edge for PMOS and one with a work function close the Si conduction band edge for NMOS. Simulation results have shown that a single "mid-gap" metal having a Fermi level near the middle of the Si band gap would not be viable for MOSFET technology nodes past 50nm because of poor drive currents due to high threshold voltages and short-channel effects [3]. A major drawback with the dual-metal gate approach is the possible requirement of extra patterning and etching steps to deposit different metals on the NMOS and PMOS areas of a CMOS device. Other challenges include the intrinsic properties and reactivities of metals with low and high work functions. Categorically, low work function (NMOS compatible) metals are reactive species (including La, Hf, Ta) that react with the dielectric to form detrimental

interface states, while high work function (PMOS compatible) metals are intrinsically inert elements (such as Pt and Ir) with poor adhesion and are difficult to etch.

Several candidate materials have been initially investigated for PMOS and NMOS-compatible gate metals. For PMOS metals, promising results have been observed for Ru [4], and Mo [5] while other studies have included Ni [6-8], Ir [7, 9], and Pt [10]. However, these metals were mostly studied in the form of silicides due to the poor abhesion. $RuO_2$ (a conductive oxide) has also been studied, but the interface stability must be examined carefully because of potential for oxygen diffusion through the dielectric to the silicon substrate to form interfacial $SiO_2$ [11]. For NMOS metals, promising results have been observed for Ti [12], and Ta (generally in alloys such as $TiSi_xN_y$ or $TaSi_xN_y$) [13, 14], while other studies have included metallic Hf and Zr [15]. To date, no set of NMOS and PMOS metals have been identified that provide Fermi level position and stability required for high performance devices.

**Experimental Approach**

Thin ruthenium oxide films were deposited by plasma-enhanced chemical vapor deposition (PECVD) or Chemical Vapor Deposition (CVD) (see Figure 5.1) on atomic layer deposition (ALD) hafnium dioxide dielectric (see Figure 5.2) or thermal silicon dioxide dielectric. Before electrode and dielectric deposition, Si(100) substrates were prepared by J.T. Baker clean for 5 min, deionized water (DI) rinse for 5min, and buffer oxide etch (BOE) for 4 min, deionized water (DI) rinse for 1 mn, and dried in $N_2$ flow. The process of furnace annealing in air for 10 minutes was used to form the silicon dioxide dielectrics. The hafnium oxide dielectric was formed in our laboratory by ALD using tetrakis(diethylamino) hafnium precursor, 98% purity (purchased from Strem Chemicals, Inc.) at 325°C and 0.5 Torr. The dielectric substrates were then loaded into the PECVD/CVD reactor for Ruthenium Oxide films. The ruthenium precursor used was Tris(2,2,6,6-tetramethyl-3,5-heptanedionato) ruthenium [$Ru(TMHD)_3$], 99% purity for $RuO_2$ films (purchased from Strem Chemicals, Inc.).

Metal Oxide Semiconductor (MOS) capacitors were fabricated with varying thickness of $RuO_2$ films deposited at 325°C & 500°C and *ex-situ* capped with PVD Aluminum films (see Figure 5.3) through a shadow mask. Varying $RuO_2$ film thickness before Al capping ranged from 0 to ~185Å on $HfO_2$ dielectrics and 600-1700Å on $SiO_2$ dielectrics as determined from step height measurements using a Tencor Alpha Step 500 surface profilometer. To electrically separate the Al contacts, the exposed $RuO_2$ film (between the Al contacts) was Reactive Ion Etched (RIE) using $O_2/CHF_3$ (20sccm/0.5sccm) at 40mTorr and 150 Watts.

Film characterization was preformed using Auger Electron Spectroscopy (AES), X-ray Photoelectron Spectroscopy (XPS), Medium Energy Ion Spectroscopy (MEIS), and capacitance-voltage (C-V) characterization. AES was conducted using a Physical Electronics' (PHI's) Model 3017 Auger Electron Spectroscopy Subsystem with a 5keV, 10μA electron beam and a high sensitivity Cylindrical Mirror Analyzer (CMA). XPS was conducted using a Riber LAS3000 instrument equipped with a single-pass, cylindrical mirror (MAC2) analyzer. An Mg Kα ($h\nu$=1253.6 eV), non-monochromatic X-ray source at a 90° take-off angle was used for all XPS measurements. Step sizes of 1.0eV and 0.1eV were used to obtain survey and detailed XPS spectra, respectively. C-V measurements were performed on an HP4284 LCR with voltage sweeps from depletion to accumulation (–3 to 1 Volt) at 1 MHz. The MOS capacitors areas (with ~$1x10^{-5}cm^2$ Al gate contacts formed using a shadow mask) were measured using a Nikon Eclipse Optical Microscope equipped with a digital camera to avoid instrumental errors associated with large areas. Equivalent oxide thickness (EOT) and flatband voltage were extracted from C-V data using the NCSU CV program which includes quantum mechanical effects [16].

## Results and Discussion

### A. Chemical characterization of $RuO_2$ on $HfO_2$

Auger measurements were performed to analyze the relative atomic composition of bulk $RuO_2$ and bulk $HfO_2$ films for varying substrate temperature during $RuO_2$ depositions (shown in Figure 5.4). $HfO_2$ films were deposited using an ALD process with thickness ~500Å (sufficiently thick to avoid seeing any possible interactions with underlying substrate) on H-terminated Si(100) substrates. Then the samples were cleaved into two samples with subsequent $RuO_2$ deposition using CVD process with thickness >500Å (sufficiently thick to avoid seeing any possible interactions with the underlying $HfO_2$ films). Figure 5.4 shows that relative atomic compositions change by varying the substrate temperature (365ºC & 500ºC) during $RuO_2$ deposition. Films deposited at 500ºC have increased oxygen incorporation by comparing the Ru:O and Hf:O peak ratios to the films deposited at 365ºC.

Initial XPS measurements were performed to analyze the chemical bonding of thin $RuO_2$ films deposited on ALD $HfO_2$ dielectrics using two different process conditions (an oxidizing $N_2O$ plasma or a reducing $H_2$ plasma) during $RuO_2$ deposition, which are shown in Figure 5.5. The figure shows the Hf 4f spectra with a higher binding energy for films deposited with $N_2O$ plasma and a lower binding energy for films deposited with $H_2$ plasma compared to the binding energy for the underlying $HfO_2$ dielectric. The result of Hf 4f peak shifting to higher binding energy (Figure 5.5b) is attributed to excess oxidation from using oxidizing $N_2O$ plasma, which is consistent with oxygen incorporation results from Auger (Figure 5.4). Figure 5.5c suggests that some reduction of the $HfO_2$ occurs during CVD process with reducing $H_2$ plasma, which results in deficient dielectric strength.

**B. CV characterization of $RuO_2$ on $SiO_2$**

Electrical effects of advanced gate electrodes on conventional $SiO_2$ dielectrics have also been investigated. Figure 5.6 shows the C-V curves of the capacitors with varying $RuO_2$ gate electrodes thicknesses on ~100Å $SiO_2$ before and after 400°C forming gas anneal in $N_2$(5% $H_2$) at 500Torr for 30 mins. The capacitance was measured at a frequency of 1MHz on an area of ~$1x10^{-5}cm^2$. The flat-band voltage ($V_{FB}$) and equivalent oxide thickness for $SiO_2$ (EOT) for the capacitors were obtained by using NCSU CV program [16]. For the as-deposited samples with 0Å $RuO_2$ (Figure 5.6a), the flat-band voltage was –4.7V and was attributed to the damage in the dielectric by the plasma during the sputtering process. This damage can be significantly corrected after a low temperature forming gas anneal and the results of the recovery of the flat-band voltage is –0.5V, which is also shown in Figure 5.6a. The sample with 600Å $RuO_2$ (Figure 5.6b) has a flat-band voltage of –0.1V, which adequately illustrates its ability to protect the $SiO_2$ dielectric from plasma damage during Al deposition. The negligible shift in flat-band voltage after forming gas anneal (also shown in Figure 5.6b) further suggests that minimal plasma damage to the dielectric has occurred. However, the equivalent oxide thickness significantly increases from 259Å to 443Å because of additional interface layer formation. This is consistent with the excess oxygen in the $RuO_2$ films (established previously from chemical analysis) diffusing through the $SiO_2$ and reacting with the Si substrate to form additional $SiO_2$.

**C. CV characterization of $RuO_2$ on $HfO_2$**

In addition to studying the electrical effects of advanced gate electrodes on group IV dielectrics, the extent of $RuO_2$ film thickness against plasma damage to the dielectric by varying the $RuO_2$ film thickness was also studied. To begin, a sample with ~50Å $HfO_2$ film

was cleaved into four separate samples and subsequent $RuO_2$ films were deposited with varying thickness. Figures 5.7a-d show CV curves for capacitors with 0Å, 90 Å**,** 120 Å, and 180 Å $RuO_2$ films respectively on ~50Å $HfO_2$ dielectric films and Figures 5.7e-h show the respective CV curves after 400°C forming gas anneal in $N_2$(5% $H_2$) at 500Torr for 30 mins. The capacitance was measured at a frequency of 1MHz on an area of ~$1x10^{-5}cm^2$. The flat-band voltage ($V_{FB}$) and equivalent oxide thickness for $SiO_2$ (EOT) for the capacitors were obtained by using NCSU CV program [16]. Similarly to the $SiO_2$, the as-deposited $HfO_2$ film with 0Å $RuO_2$ (Figure 5.7a) has a flat-band voltage of –4.4V, which further suggests excessive charge was introduced into the dielectric via plasma damage during Al deposition. In general, Figure 5.7a-d shows a general trend as $RuO_2$ thickness increases the flat-band voltage shifts more positive indicating a higher degree of "shielding" from plasma damage to the dielectric as the $RuO_2$ thickness increases. At 180 Å $RuO_2$ (Figure 5.7d) shows a flat-band voltage of –1.4V indicating some plasma damage has occurred to the dielectric. Therefore, minimal $RuO_2$ thickness to adequately protect the dielectric from plasma damage is >180Å. Also, for each film stack, their respective CV curve (Figures 5.7e-h) shows an increase in EOT after the forming gas anneal. For Figure 5.7e with 0Å $RuO_2$ the increase in EOT is attributed to water adsorption during ambient exposure diffusing through the $HfO_2$ dielectric and reacting with the underlying substrate to form an interfacial layer. Increases in EOT values for Figures 5.7f-h with 90Å**,** 120Å, and 180Å $RuO_2$, respectively, suggests a combination of water adsorption during ambient exposure and excess oxygen in $RuO_2$ diffusing through the $HfO_2$ dielectric and forming additional interfacial layer formation.

**D. CV characterization of *ex-situ* versus *in-situ* $RuO_2$ on $HfO_2$ film stacks**

To determine the extent of water adsorption during ambient exposure for $HfO_2$ dielectric films, the electrical performance of *in-situ* $RuO_2$ capping layers versus *ex-situ* $RuO_2$ films were studied. Both *in-situ* and *ex-situ* film stacks with $RuO_2$ on $HfO_2$ were fabricated using the PECVD reactor (Figure 5.1) using the processing conditions illustrated in Figure 5.8. The CV curve in Figure 5.8b shows an EOT=15Å when the $RuO_2$ film is deposited *is*-situ with the $HfO_2$ dielectric layer. However when the $RuO_2$ film is deposited *ex-situ* after the $HfO_2$ dielectric has been deposited (with roughly the same $HfO_2$ and $RuO_2$ processing conditions and the *in-situ* film stack) and exposed to ambient conditions for 4 hours then the EOT value increases to 27Å. This increase is attributed to water adsorption during ambient exposure diffusing through the dielectric and promoting interfacial layer formation.

**Conclusions:**

$RuO_2$ films were evaluated as a potential candidate for gate electrodes in advanced gate stack applications. $RuO_2$ films with excessive oxygen were produced when using an oxidizing $N_2O$ plasma source. Increases in EOT values when using an oxidizing plasma source indicates the necessity to determine the detailed structure of the interface between high-k dielectrics and the gate metal will be important to maintain low equivalent oxide thickness, but the effect of metal deposition on the high-k/metal interface structure is not known. We have deposited $RuO_2$ metal from Tris-tetramethyl-heptadianato Ru (Ru TMHD) introduced downstream from a remote $N_2O$ or $H_2$ plasma at 365 and 500°C, and examined the deposited film and interface structure using Auger and X-ray photoelectron spectroscopies. The films show some evidence for N and C incorporation, consistent with the 250°C decomposition temperature of the Ru TMHD. Based on AES results, the O/Ru ratio is larger for the films deposited at higher temperature. Because of the difference between the oxidizing and reducing environments in CVD processing, we expect that metallic oxides such as $RuO_2$ will result in different metal/dielectric interface structure than for elemental metal/dielectric interfaces. Finally, changes in flat-band voltages due to plasma damage to the dielectric indicate a detailed evaluation on the effect of electrical performance is important for alloying gate metals via PVD processes.

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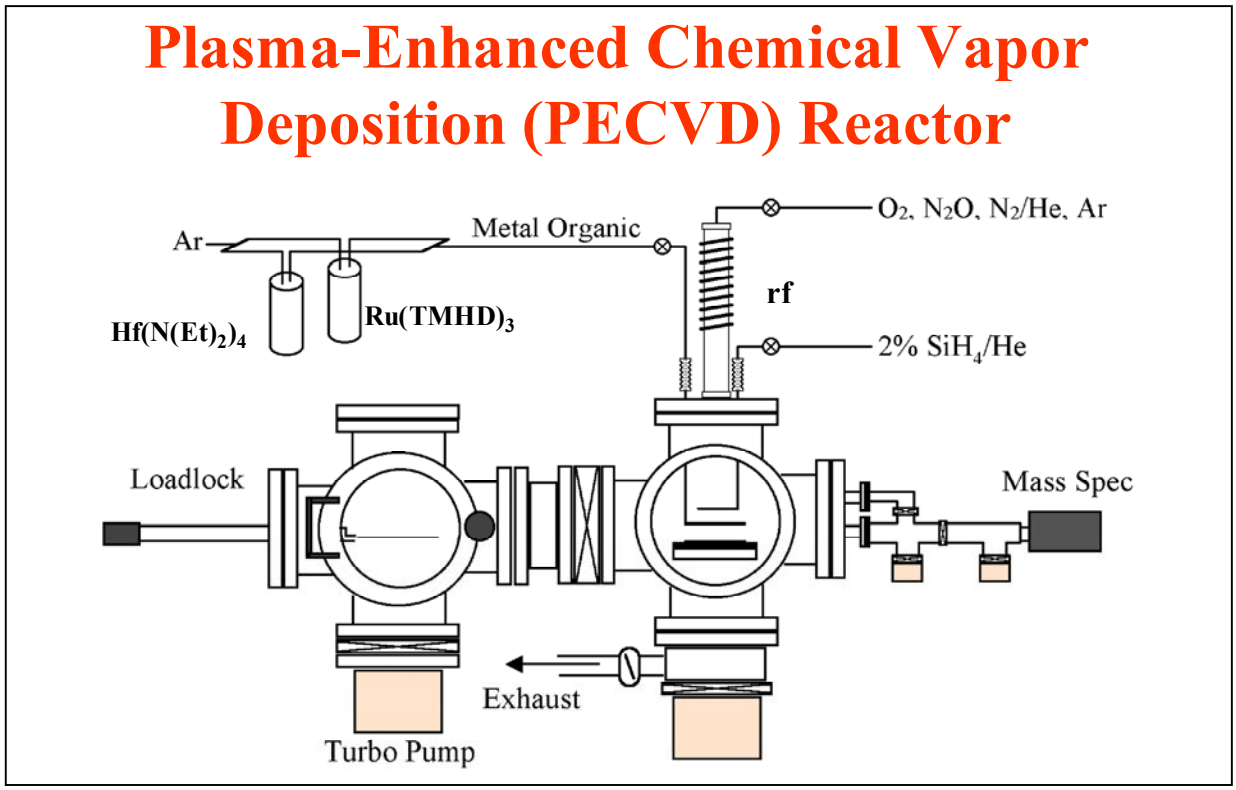


Figure 5.1: Schematic drawing of PECVD Reactor

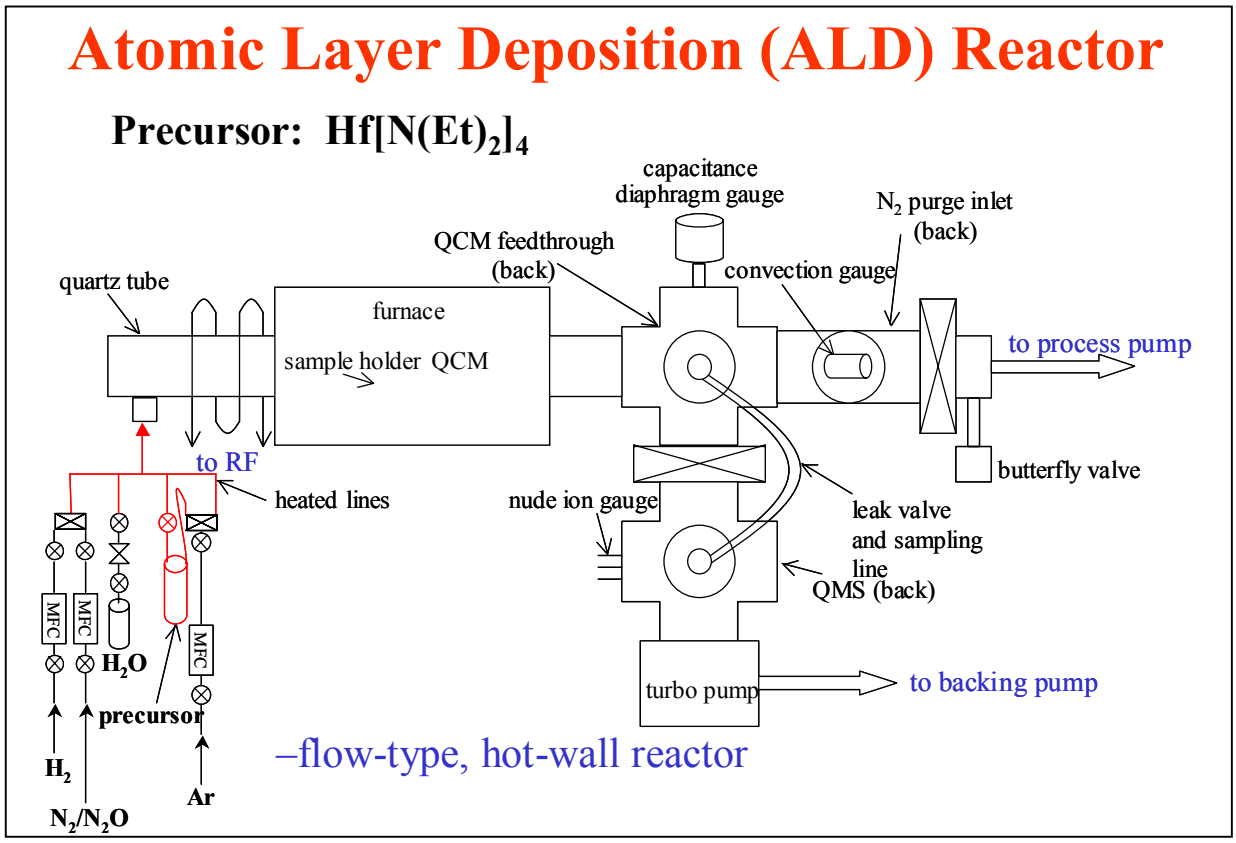


Figure 5.2: Schematic drawing of ALD Reactor

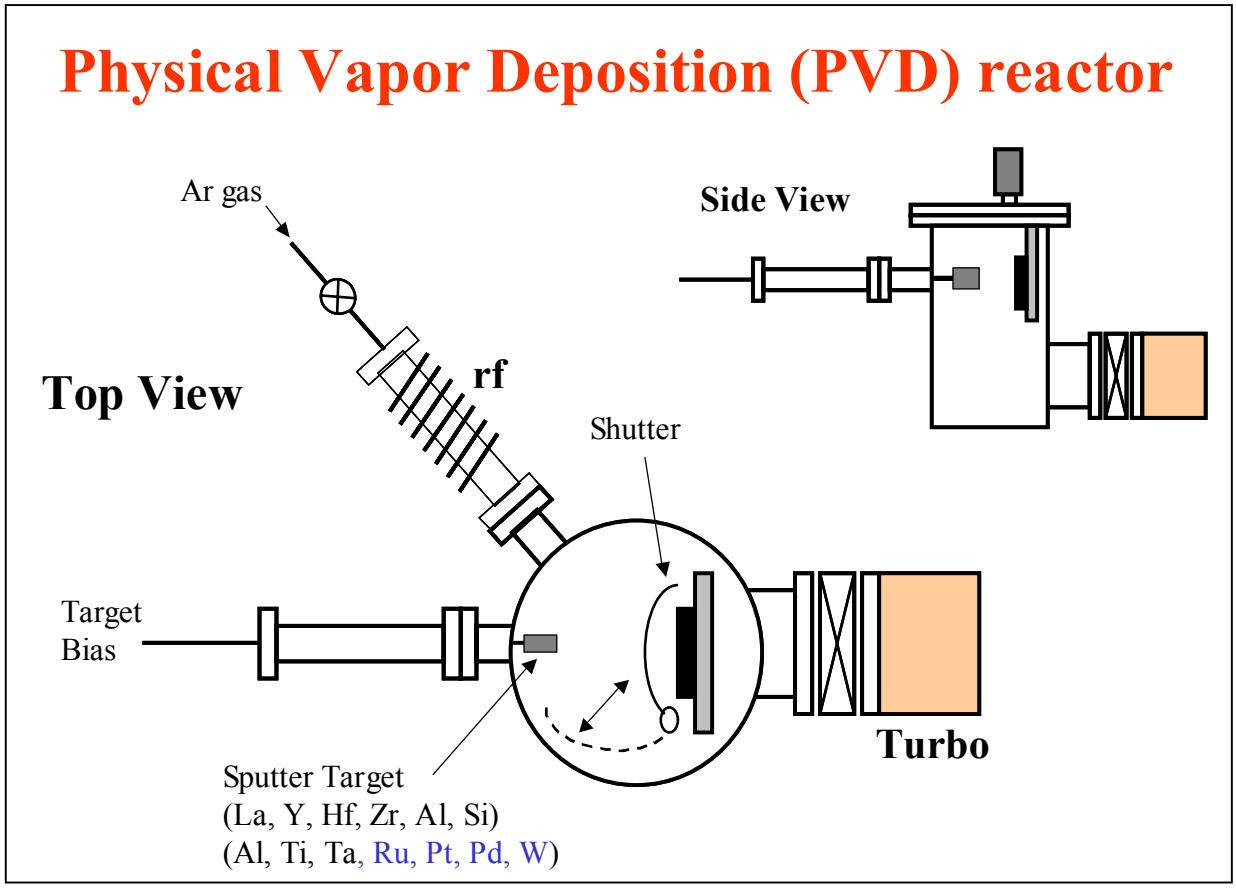


Figure 5.3: Schematic drawing of PVD Reactor

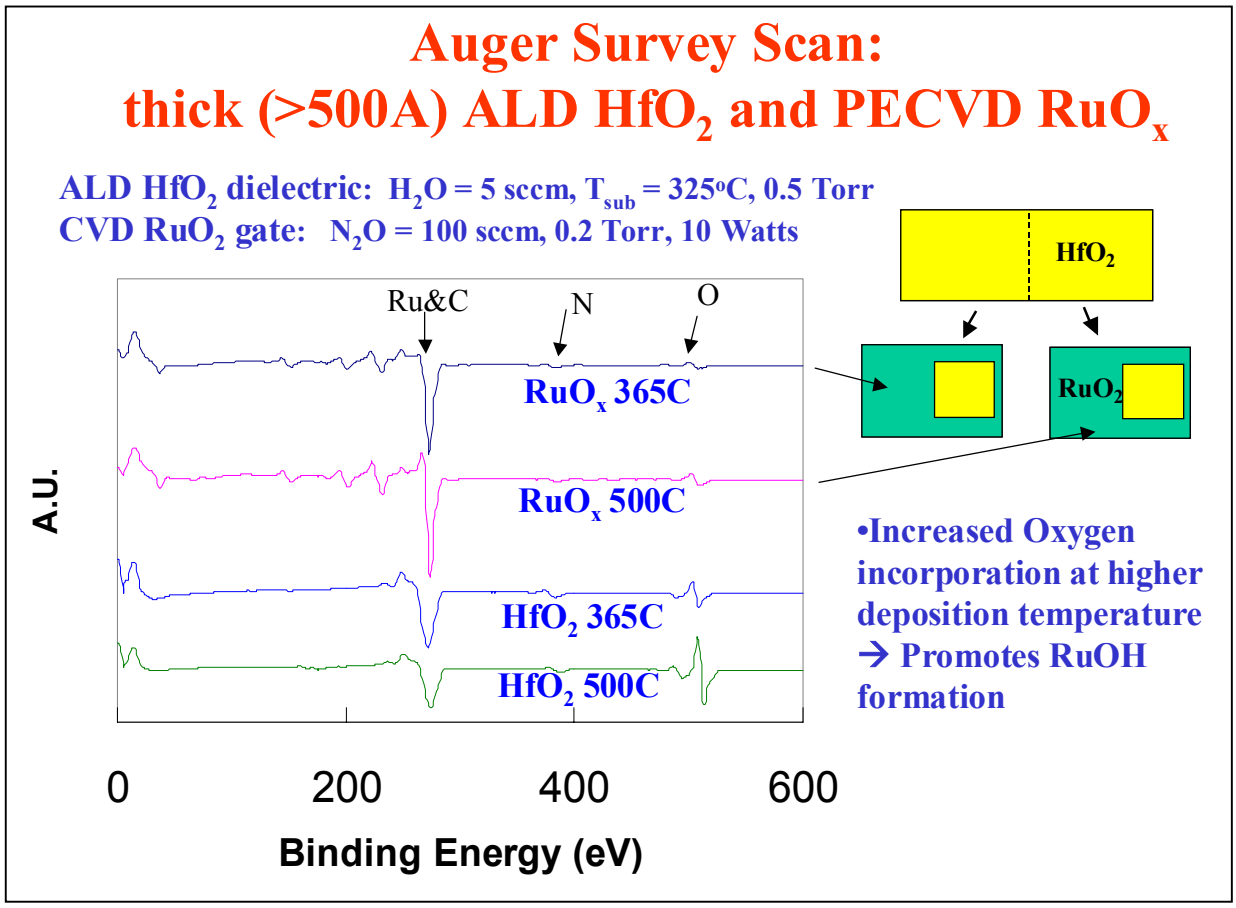


Figure 5.4: Auger analysis of $RuO_2$ on $HfO_2$

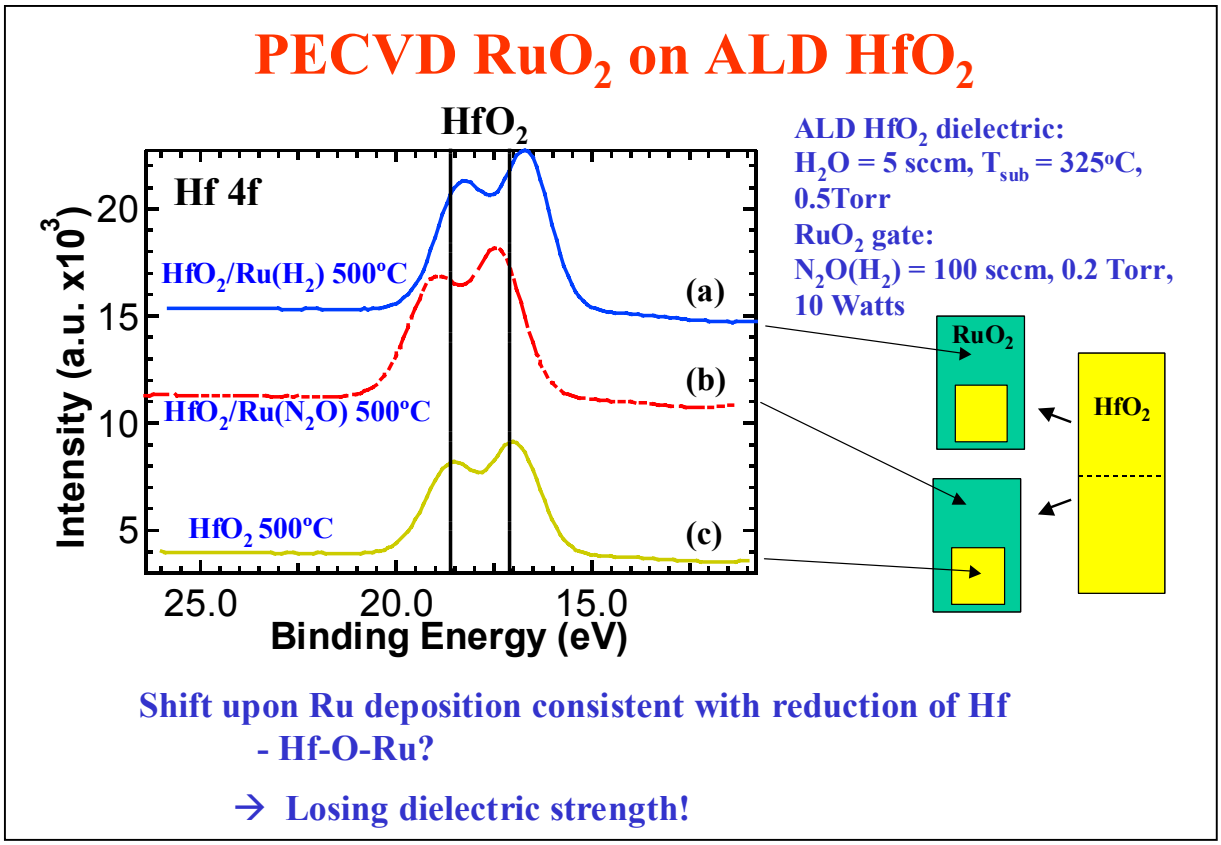


Figure 5.5: XPS analysis of Hf 4f peak for $RuO_2$ on $HfO_2$

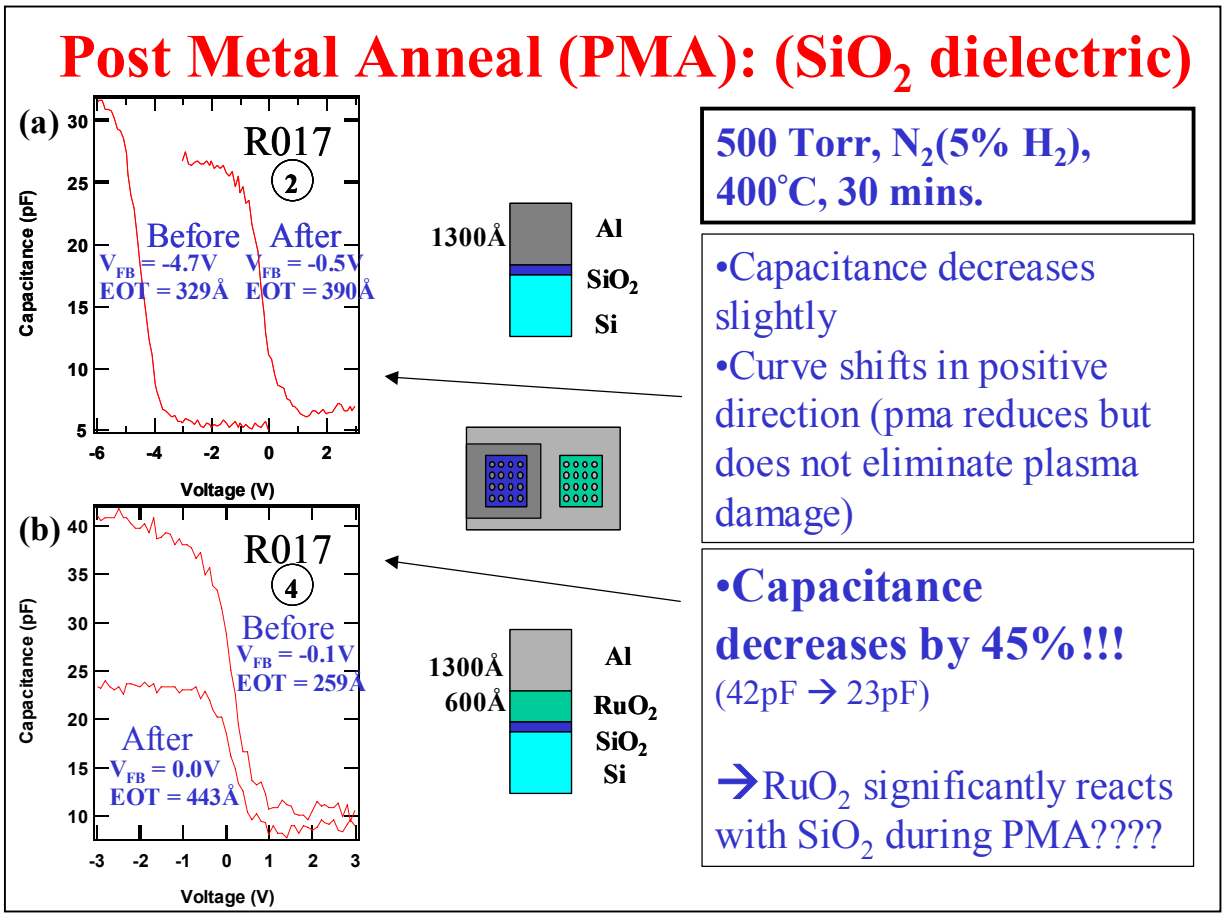


Figure 5.6: CV characterization of $RuO_2$ on $SiO_2$

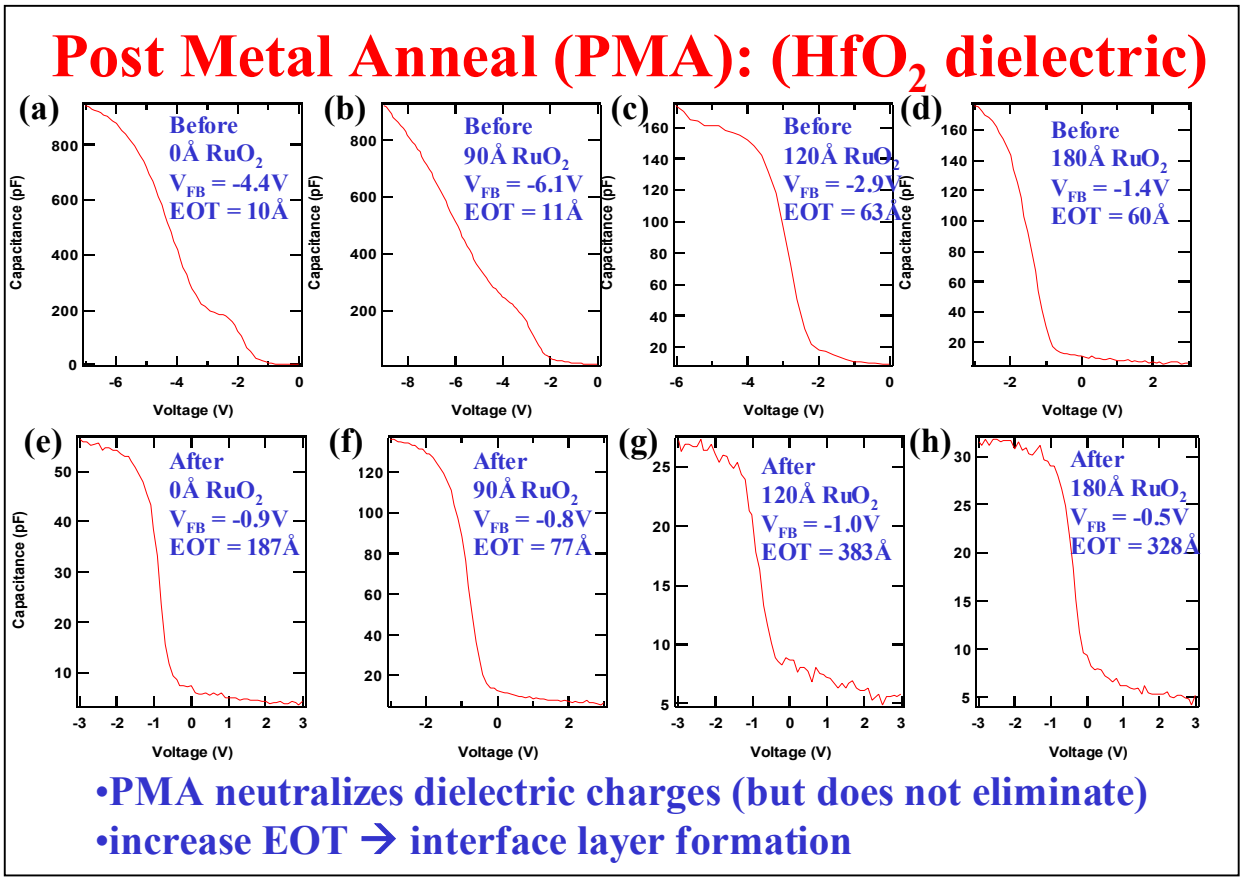


Figure 5.7: CV characterization of $RuO_2$ on $HfO_2$.

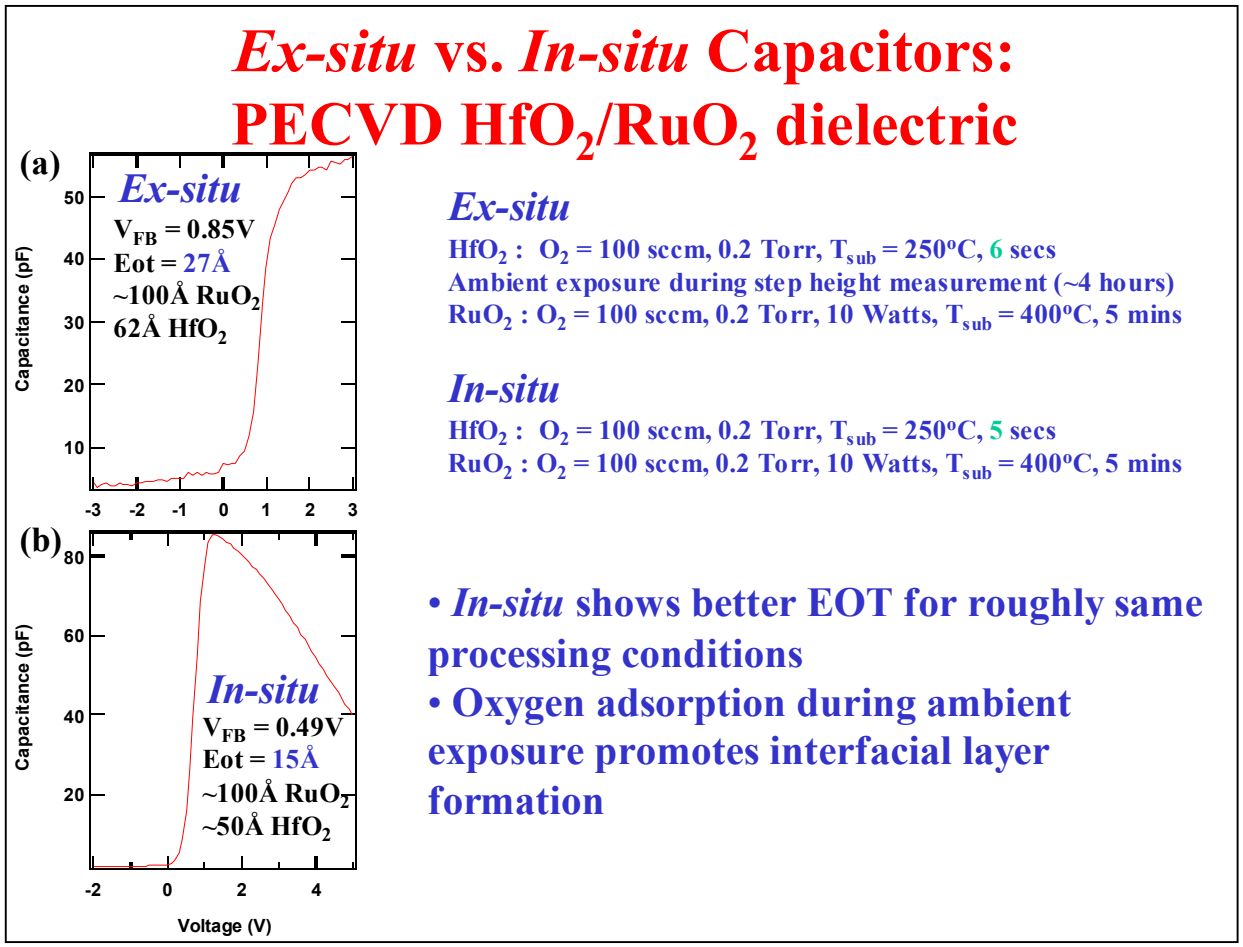


Figure 5.8: CV comparison of *ex-situ* versus *in-situ* $RuO_2$ on $HfO_2$ process.

# Chapter 6

## Charge generation during oxidation of thin Hf metal films on silicon

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## Abstract

Oxidation of Hf metal films on Si appears to follow different charge generation rules than the traditional oxidation of Si described in detail by Deal et al. Oxidation of thin Hf metal films on silicon in oxygen rich environments to form Hf-silicate results in rapid growth of silicon oxide interfacial layers and generation of significant charge concentration in the films. Oxidation of Hf in oxygen-deficient environment leads to improved control of the interface with much thinner interfacial layers and substantial reduction in the charge present in the films. Results from capacitance vs. voltage and x-ray photoelectron spectroscopy measurements are compared to correlate charge with chemical structure evolution during oxidation and dielectric layer formation. It is demonstrated that processing conditions may influence the quality of the Hf dielectric film significantly by generating positive charge that is not intrinsic to the material.

PACS codes: 73.61.Ng; **77.55.+f**
Keywords: oxidation; dielectrics; interfaces; charge defects; $HfO_2$

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***Introduction***

The search for a replacement material for the $SiO_2$ gate dielectric in CMOS devices[1] has led to the evaluation of the properties of several high dielectric constant materials, mainly oxides and silicates of group III and IV metals.[2, 3] One of the major shortcomings of most candidate materials is the large amount of charge in the film that degrades the carrier mobility in devices.[2] For some of these materials the charge is mainly inherent and as such difficult to neutralize.[4]

Extensive research of the Si oxidation process by Deal et al.[5] established the guidelines for the formation of high quality $SiO_2$ films. The main conclusion of this work was that oxidation or post deposition inert anneals at high temperatures lead to significantly reduced concentrations of fixed charge in the $SiO_2$ film. This conclusion was somewhat arbitrarily extended to the oxidation of other metal films on Si and there is the widespread belief that formation of a $SiO_2$ interfacial layer although it may reduce the overall gate stack capacitance offers a better quality interface in return. In this article we demonstrate that oxidation of Hf metal on Si can be different from oxidation of Si in terms of charge generation in the film. More specifically, it is shown that fast growth of the $SiO_2$ interfacial layer directly correlates with increased amounts of charge in the produced Hf-silicate film. This is achieved by comparing the electrical properties of $HfSiO_x$ films prepared by oxidation of thin Hf-metal films in O-rich and O-deficient environments and correlating it to film composition measurements obtained by XPS.

***Experimental***

Thin Hf metal films were deposited on H-terminated Si(100) substrates via dc or rf sputtering following the techniques described in earlier work.[6] After deposition of the metal, the films were oxidized ex-situ in a tube furnace or in a Rapid Thermal Anneal (RTA) instrument. The furnace oxidations were performed at 600°C either in the presence of $N_2O$, or using the impurity $O_2$ present in dry $N_2$ at atmospheric pressure, following the procedure initially described by B. H. Lee et al..[7] The RTA oxidations were performed in dry air at temperatures ranging from 400 to 700°C. The RTA chamber was purged with Ar at high air flow rates for several minutes before the anneal and the samples were removed only when the chamber temperature was below 200 C to prevent undesirable reactions of the film with atmospheric components such as $H_2O$ or $CO_2$. The initial Hf-metal film thickness was determined by extrapolating linear time vs. step height measurements made using thicker films.

After oxidation, samples from the same run were used for compositional analysis via X-ray Photoelectron Spectroscopy (XPS), and for electrical characterization. XPS measurements were performed with a Riber LAS3000 (MAC2 analyzer, Mg Kα hv=1253.6 eV, non-monochromatic X-ray source) at 75º take-off-angle with 0.1eV step size. The energy scale was calibrated by setting the adventitious C 1s peak to a binding energy of 285.0 eV. Al top and back-contacts were formed by resistive-heating evaporation using shadow masks. Capacitances vs. voltage measurements were performed with an HP 4284A impedance meter at 1MHz. Typical capacitor area, as determined by digital photography, was $4x10^{-4}cm^2$. Flatband voltage ($V_{FB}$) and equivalent oxide thickness (EOT) were obtained by processing the C-V characteristics with the NCSU C-V program that includes corrections for the

quantum mechanical effects.[8] Some samples were annealed in forming gas (FG) (10% $H_2$ in $N_2$) for 30 min at 400°C using a standard Tylan furnace available in the NCSU cleanroom.

***Results***

Initially, we compare the results for $N_2O$ vs. $N_2$ oxidation in the tube furnace. Figure 6.1(a) shows the C-V curves for 0.8nm Hf-metal films oxidized in the tube furnace in $N_2O$ at 600°C for 30 to 300s. In general, an increase in the oxidation times leads to smaller capacitances (i.e. thicker interface layers) but the shape and position of the curve remains practically unchanged for oxidations up to 120s. For the sample oxidized for 300s a reduction in the capacitance and a significant shift of the curve to more negative voltage is observed. Figure 6.1 (b) plots the C-V curves for 0.8nm Hf films oxidized in a $N_2$ ambient for 45, 90 and 300s. Even in this environment there is enough impurity O, probably in the form of $O_2$ and $H_2O$, to form metal oxide as evidenced by the capacitance measurements. The capacitance of the gate stack decreases somewhat with longer oxidation, but the decline percentage is significantly smaller than for $N_2O$ oxidation, and the position of the curve is not significantly affected.

Figure 6.2(a) presents the equivalent oxide thickness (EOT) as a function of the oxidation time and Figure 6.2(b) presents the flatband voltage ($V_{FB}$) vs. oxidation time for films obtained by the two processes. The expected position of $V_{FB}$, calculated from the work function of the Al gate and the doping of the Si substrate is ~0V. The data points represent the average of measurements on several capacitors of the same sample and the error bars represent one standard deviation. If no error bar is shown, the size of the error bar is equal to (or less than) the size of the data point symbol.

For the $N_2O$ (circles) process the key observations are: i) the EOT is proportional to the oxidation time and increases by almost a factor of two, from ~1.4nm for 30s oxidation to

2.6nm for 300s oxidation, in the conditions examined. ii) The $V_{FB}$ remains almost constant at –0.35V for oxidations up to 120s. At this point it appears that a turning point in the oxidation process is reached and longer oxidations (300s) result in a substantially more negative $V_{FB}$. This particular data point is the average over several capacitors on two different samples processed in the span of several weeks.

For the $N_2$ process (squares) the key findings are: i) Oxidations in $N_2$ in excess of 90s result in EOT significantly smaller than for oxidations in $N_2O$. ii) The marginal increase in the EOT from 1.5nm to ~1.6nm for oxidation between 15 and 300s, is accompanied by a marginal reduction in the $V_{FB}$ from ~ -0.375 to -0.3V iii) To obtain an increase in the EOT comparable to the $N_2O$ process, a 3600s oxidation in this O deficient environment is required. This film, unlike the films oxidized in $N_2O$, exhibits the highest EOT but the lowest shift in the $V_{FB}$.

Clearly a substantial difference in the electrical quality of the films prepared in O rich and O deficient environments in the tube furnace is observed. To investigate further the charge generation during fast oxidation another set of Hf-metal films was oxidized in dry air in the much cleaner environment of an RTA for 2 min at temperatures ranging from 400 C to 700 C. Figures 6.3 (a) and (b) shows the EOT and flatband voltage vs. oxidation temperature for the RTA oxidized films respectively. As the oxidation temperature increases, the flatband voltage becomes more negative, indicative of positive charge generation in the films. [9] At the same time the EOT of the gate stack increases due to the formation of a low-k interfacial layer. The electrical characteristics of the air-RTA annealed films mirror that of the $N_2O$-furnace films indicating a similar charge generation mechanism.

To investigate whether a similar charge generation mechanism is responsible for the observations for the two fast oxidizing processes ($N_2O$-furnace vs air-RTA) we plot (Fig. 6.4) the shift in the $V_{FB}$ ($\Delta V_{FB}$) vs. the increase in the interfacial layer thickness ($\Delta$EOT). We assume that the increase in the EOT is exclusively due to the growth of the $SiO_2$ interfacial layer. For the samples oxidized in air the $V_{FB}$ and EOT obtained for the 400  C oxidation is treated as the baseline measurement. The situation is more complex for the samples oxidized in $N_2O$. Oxidation from 15 to 75s does not affect the EOT substantially and the corresponding shift in the $V_{FB}$ exhibits a marginal reduction. At 90s oxidation time there is a sizable increase in the EOT and longer oxidation times reinforce this trend. At the same time the shift in the $V_{FB}$ becomes substantially more negative. So for the samples oxidized in $N_2O$, the measurements for the 90s sample are used as a baseline. Fig. 6.4 shows that the trend exhibited by the two sets of data is very similar suggesting a common mechanism for the generation of the charge in the films during the growth of the interfacial layer, despite the difference in the oxidation medium and method.

Hf 4f, Si 2p and O 1s XP spectra for some of the samples are shown in Fig. 6.5. From the spectra it is obvious that the composition of the films is compatible with Hf-silicate[10, 11] with some $SiO_2$ at the interface. From the Si 2p spectra, it is seen that the substrate peak $Si^0$ can be detected for all samples. The peak at ~102.5eV is a mixture of $SiO_2$ and $HfSiO_x$ bonding. For the samples (i) and (ii) oxidized in $N_2O$ for 30 and 90s respectively, the ratio of the $HfSiO_x/SiO_2$ to the $Si^0$ peak areas is approximately the same and less than 1. However, for sample (iii) oxidized in $N_2O$ for 300s a substantial increase in the $HfSiO_x/SiO_2$ peak area is observed, which is now larger than the $Si^0$ peak. This increase in the $HfSiO_x/SiO_2$ peak area can be interpreted in terms of growth of a thick interfacial $SiO_2$ layer.  The spectrum for

the sample (iv) oxidized for 300s in $N_2$ is comparable to spectrum (i) oxidized for 30 seconds in $N_2O$, confirming the observations based on the electrical data that oxidation in $N_2$ results in much less interfacial $SiO_2$.

***Discussion***

It is well established that for thermal oxidation of Si, higher thermal budget during oxidation either in the form of elevated temperature or longer oxidation or post deposition inert anneals causes significant reduction in the concentration of fixed charge in the film.[5] There is increasing evidence that the $HfO_x$/Si interface behaves substantially differently[12-14] than the well studied $SiO_2$/Si interface. The results described in this article show that there is a distinct difference in the electrical quality of the films produced in fast and slow oxidation. In the case of fast oxidation ($N_2O$ and dry air) rapid oxidation of the interface is accompanied by generation of charge in the film.

The rapid oxidation of the interface during the $N_2O$ and dry air processes is evidenced by the increase in the EOT (decreased capacitance per unit area) and corroborated by the XP spectra. The electrical and the XPS data indicate that the increase in the EOT stems from an increase in the thickness of the $SiO_2$ interfacial layer. In general, it is believed that a Si/$SiO_2$ interface is superior to a metal oxide/Si interface. The key finding of this work is that for the case of Hf-metal on Si there is a correlation between the growth rate of the interfacial layer and the amount of charge generated in the film. More specifically, fast growth of the interfacial layer such as when using $N_2O$ or air as oxidizers, results in the generation of a substantial concentration of fixed charge. Oxidation of the Hf/Si interface in an oxygen deficient environment leads to thinner interfacial layers and less charge detection in the films. The specific results that support this conclusion are: growth of ~1.6 of interfacial $SiO_2$ at 600°C in $N_2O$ in 300s results in -0.65eV shift in the flatband voltage. For dry air oxidation increasing the oxidation temperature from 400°C to 700° results in the growth of ~2.0nm of

additional interfacial $SiO_2$ in 120s that is accompanied by a ~-0.6V shift of the flatband voltage (from ~–0.2V to ~–0.8V). The fact that this trend is reproducible both in the case of the furnace and the strictly controlled RTA oxidation demonstrates that the observed correlation is linked to some fundamental change in the quality of the interface and is not a side effect of poor film formation. Fig. 6.4 demonstrates that the charge generation mechanism is similar for the furnace ($N_2O$) and RTA (air) oxidations, and does not depend on the initial Hf metal film thickness. Contrary, very slow growth of 0.7nm of interfacial $SiO_2$ at 600°C in $N_2$ in 3600s results in marginal reduction in the amount of charge in the film.

Recent studies have demonstrated trapping of Hf atoms in $SiO_2$ interlayers during rapid thermal annealing of $HfO_2$ films on Si and suggest that these defects affect the charge transport through the film.[13] Rashkeev at al.[13] suggest the introduction of ionic bonding due to the metal atom disrupts the integrity of the covalent $SiO_2$, and defects are generated. In our study, fast oxidation of Hf/Si interface likely results in the entrapment of Hf atoms in the $SiO_2$ interfacial layer. The presence of the Hf impurity also likely produces energy levels inside the Si energy gap and the C-V curves obtained in the course of this work corroborate that conclusion; the rising part of the curves is stretched over 2 V, indicative of interface traps distributed evenly over the bandgap.

Gavartin et al.[12] have suggested that ALD $HfO_2$ films may be rich in oxygen vacancies and interstitial atoms. These vacancies can drift towards the interface resulting in the formation of Si-Hf bonds that can act as hole traps and a source of fixed charge. This explanation can partially explain the charge generation during fast oxidation but it does not account for the absence of this effect during the slow oxidation

Generation of positive fixed charge has also been observed during postdeposition reoxidation of $ZrO_2/SiO_2$ gate stacks formed by atomic layer deposition, and the fixed charge has been attributed to formation of overcoordinated O center induced by a large density of H atoms originating from the $H_2O$ precursor.[15] Our process is $H_2O$ free, and IR measurements on thick samples do not show any appreciable absorption of $H_2O$ even after long ambient exposures.[16] Cleary more detailed experiments are required to trace the origin of this type of charge.

The correlation between growth of interfacial $SiO_2$ and presence of charge in the film is corroborated by the XPS data. The substrate $Si^0$ peaks appear at a lower binding energy than expected. Opila et al. have reported and explained the relationship between fixed charge and the position of the $Si^0$ peak in XP spectra for Hf and Zr silicate films.[17] The shift in $Si^0$ peak in our films can be explained by the existence of charge in the layers that the substrate photoelectrons have to transverse. For samples (i) (ii) and (iv) that exhibit comparable amounts of charge ($V_{FB}$ shifted by ~-0.35V) the substrate peak appears at ~98.9eV (Fig. 6.4) shifted by ~-0.4V from the nominal value of 99.3eV. For sample (iii), which exhibits an additional ~–0.6V shift in the $V_{FB}$, the $Si^0$ peak is shifted by ~-0.5eV more than for the other samples.

Forming-gas-anneal (10%$H_2$ in $N_2$ for 30min at 400°C, data not shown) results in partial neutralization of the charges when performed before Al gate deposition and almost complete removal after Al deposition for the films oxidized in $N_2O$. In both cases, however, neutralization of the charge is accompanied by significant increase in the gate capacitance, indicative of reaction at the dielectric-gate metal interface. For the case of $N_2$ oxidation, FGA does not have an effect on either the flatband voltage or the EOT. This may suggest that the

~-0.4V shift in the $V_{FB}$ may be due to fixed or oxide charge, as FGA is known to passivate interface charge.[18] While, forming gas anneal may remove part of these defects, processes that avoid charge generation are generally preferred as further thermal treatment and stress on the device may lead to desorption of the H-atoms and regeneration of the defects, which will deteriorate carrier mobility in devices significantly.

***Conclusions***

There increasingly mounting evidence that oxidation of thin Hf-metal films on Si is a very complex process and very different from oxidation of Si. Fast oxidation leads to growth of thick interfacial layers and the generation of significant concentration of charge in the film. Slow oxidation allows better control of the interface and results in significantly reduced charge in the film. FGA on capacitors with Al gates yields inconclusive results due to reaction in the gate metal/dielectric interface.

*Acknowledgements*

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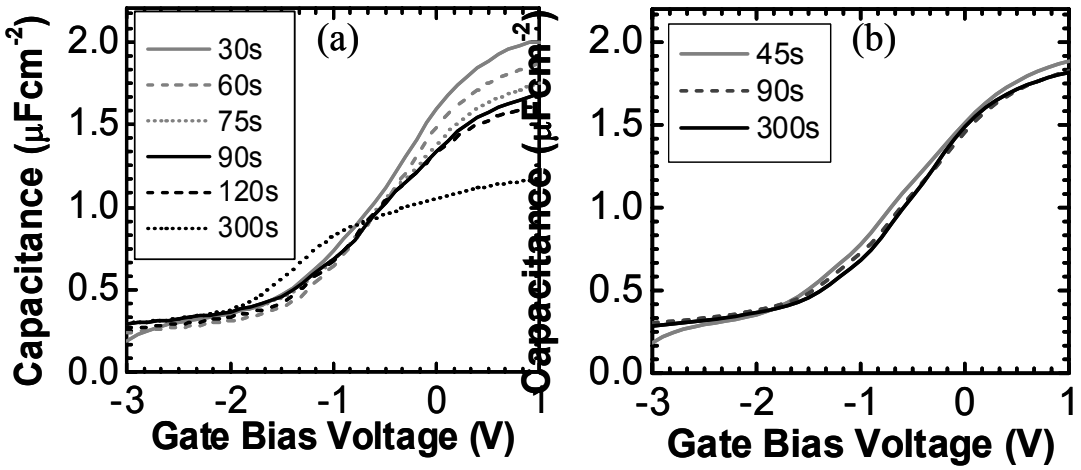


Figure 6.1: Capacitance vs. Voltage measurements for 0.8nm Hf-metal films oxidized in $N_2O$ (Fig. 6.1a) and $N_2$ (Fig. 6.1b) with Al gates as a function of oxidation time (legend). Oxidation in $N_2O$ for 300s results in substantial reduction of the capacitance and generation of positive fixed charge in the films. Oxidation up to 300s in $N_2$ does not have a significant effect in the electrical properties of the films.

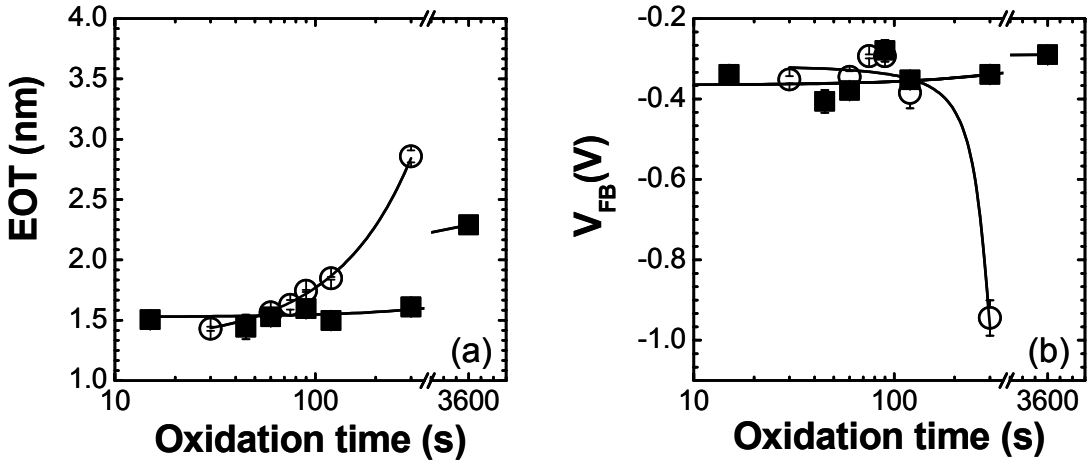


Figure 6.2: Equivalent Oxide Thickness (EOT) and flatband voltage $V_{FB}$ vs. oxidation time for 0.8nm Hf-metal films oxidized in $N_2$ (squares) and $N_2O$ (circles). Oxidation of Hf-metal on Si in $N_2O$ leads to growth of thick interfacial layers that is accompanied by the generation of large amounts of charge in the case of 300s oxidation time. Oxidation of Hf-metal on Si in $N_2$ and Si in $N_2O$ leads to significantly reduced charge generation.

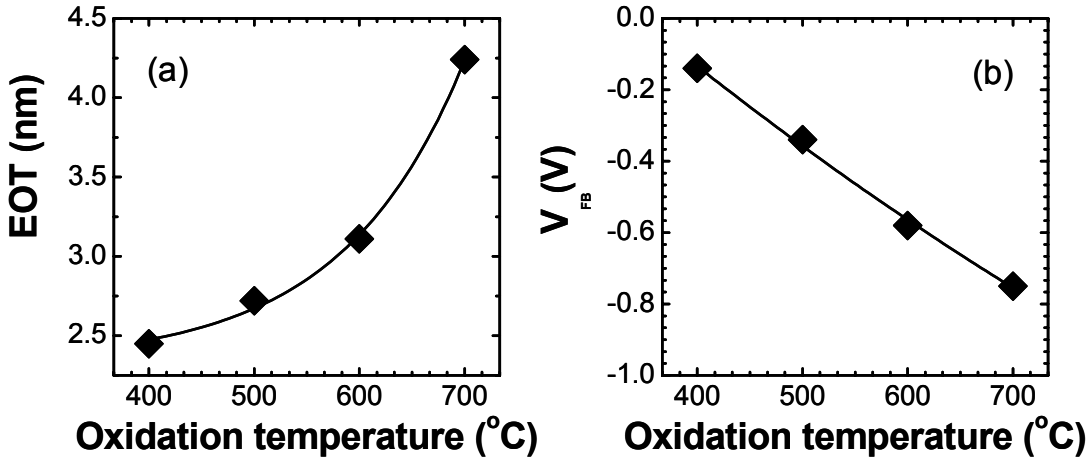


Figure 6.3: Equivalent Oxide Thickness (EOT) and flatband voltage $V_{FB}$ vs. oxidation temperature for 2.5nm Hf-metal films oxidized in dry air from 2 min in an RTA. Oxidation of Hf-metal on Si at higher temperatures leads to growth of thick interfacial layers that is accompanied by the generation of large amounts of charge as evidenced by the shift in $V_{FB}$.

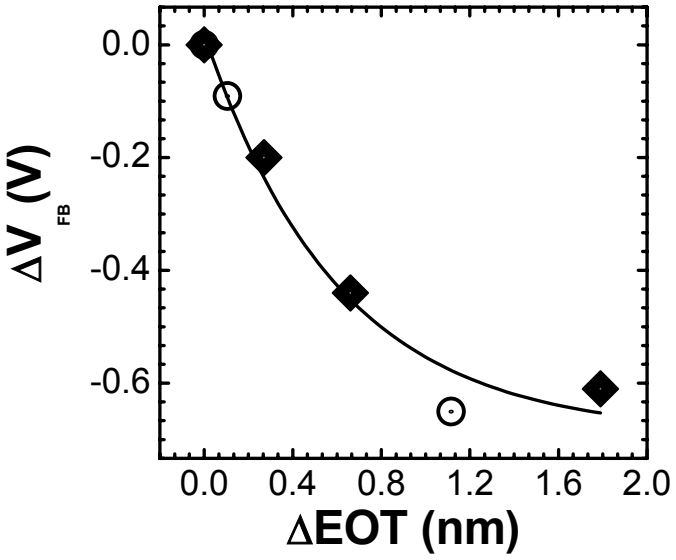


Figure 6.4: Shift in the $V_{FB}$ as a function of the interfacial layer thickness increase. For the samples oxidized in the RTA (diamonds) the $V_{FB}$ and EOT obtained for the 400 C oxidation is treated as the baseline measurement. For the samples oxidized in the tube furnace in $N_2O$ at 600 C (circles) the $V_{FB}$ and EOT obtained for the 90s oxidation is treated as the baseline measurement.

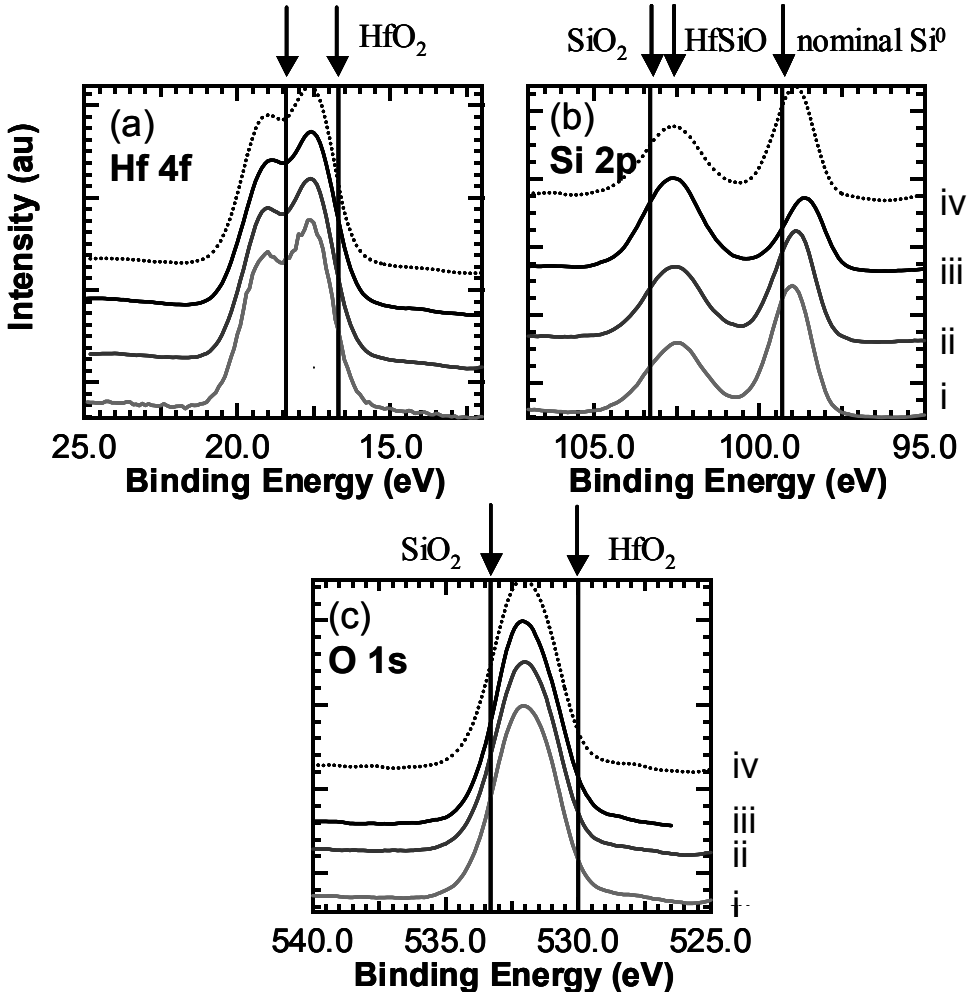


Figure 6.5: Hf 4f, Si 2p and O 1s spectra for 0.8nm-metal films oxidized in (i) $N_2O$ for 30s (ii) $N_2O$ for 90s (iii) $N_2O$ for 300s and (iv) $N_2$ for 300s. Spectra (i), (ii) and (iv) are practically identical and correspond to samples with comparable electrical properties. We can observe the growth of the $SiO_2$ peak in the Si 2p spectrum for sample (iii), result of the fast interface oxidation achieved in $N_2O$.

# Chapter 7

# Surface Sensitivity of Atomic Layer Deposition of Ruthenium using Ruthenium Cylcopentadienyl precursor

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## Abstract

Atomic layer deposition (ALD) ruthenium films from bis(cyclopentadienyl) ruthenium $(RuCp)_2$ were studied using online Auger Electron Spectroscopy (AES) to identify surface composition of the films during the ALD process. The AES results show significant changes in film composition when comparing the surface after the precursor pulse and the reactant pulse. The compositions show evidence that the ruthenium films form an adsorbed oxygen layer during the reactant pulse which facilitates the oxidation of unreacted precursor ligands leftover from the precursor pulse step.

## Introduction

As silicon complementary metal oxide semiconductor (CMOS) devices are scaled below 100 nm, current materials will eventually reach their physical or electrical limits to satisfy the ever growing stringent market demands. One such concern is with the continued use of poly-Si gate electrodes. For CMOS device fabrication processes, the poly-Si gate electrode is deposited undoped and subsequently converted to *n*- or *p*-type using appropriate ion implantation and annealing. For example, when dopants are implanted in the poly-Si gate, they need to be "activated" by a high-temperature anneal (up to 1100°C) to diffuse the dopant atoms to lattice sites and make them electrically active (thereby making the gate conductive). However, current CMOS processes use lower temperature anneals (~950°C) to limit unwanted dopant diffusion in other regions of the device. Therefore, the poly-Si is not completely activated and has some finite capacitance, because it is not completely metallic. In operation, this poly-depletion effect adds a series capacitance with an EOT of 3-7Å to the gate stack, which becomes a significant problem as industry attempts to scale the gate stack to EOT values below 10nm[1-4]. When poly-Si gate electrodes are used in conjunction with ultra-thin gate dielectrics dopant penetration from the gate into the channel can be a significant problem[5]. Particularly this problem is severe for *p*+ gate electrodes, which use boron as its dopant. Boron penetration has been observed to occur through high-k dielectrics[2] given the small mass and high diffusivity of B and is a concern for future gate stacks since it leads to instabilities in device operations. Thus, the search for alternative gate materials faces many challenges since they must have compatible work functions, process compatibility with dielectric deposition and annealing, and have thermal (up to 1000°C) &

chemical interface stability with dielectrics. To replace $n^+$ and $p^+$ polysilicon and maintain scaled performance, it is necessary to identify tandem metals with workfunctions within ~0.2eV of the conduction and valence band edges, ie workfunctions of ~5.0eV and ~4.0eV for NMOS and PMOS gates, respectively[3]. Many midgap workfunction materials such as tungsten are inadequate for future CMOS technologies since they exhibit 1) threshold voltages that are too large for low-voltages operations and 2) severely degraded short channel characteristics[3].

Atomic layer deposition (ALD) is a processing technique for metal gate deposition. ALD is a surface controlled cyclic layer-by-layer process each atomic layer results from a saturated surface controlled chemical reaction. Chemisorption, that is the chemical reaction between the volatile precursor and the surface, is assured by carefully selecting the reaction temperature so that the precursors are not allowed to condense or decompose on the surface. This absorption mechanism, which saturatively binds at least one alternating precursor firmly to the surface so that the precursor used, can meet with each other and react leading to film growth. The precursor doses are kept high enough to achieve surface saturation. Commonly, in the growth of binary compounds such as metal oxides, a reaction cycle consists of two reaction steps. In one step the metal compound precursor in the vapor phase is transported to the surface of a wafer where chemical transformation occurs leaving the desired solid-state composition as a thin film and releasing volatile coproducts that exit the reactor, and in the other step it reacts with the reactant precursor. Between the steps a purge is applied to remove the excess of precursor and the reaction by-products, which makes the process self-limiting. However, the precursors used in an ALD process should have complementary

surface reactions, which means that each vapor precursors must prepare the surface for its reaction with the other precursor.

The self-controlled growth mode of ALD contributes several advantages. Controlling the number of reaction cycles enable precise growth and thickness of ultra thin films in a straightforward manner. The precursors are saturatively chemisorbed, thus bringing stoichiometric films with large area uniformity and conformality even on complex surfaces with deformities. Layer-by-layer growth allows one to change the material abruptly after each step.

Alternative gate metal candidate include elemental metals or metal alloys (ie, metal nitrides, metal silicides, or other metal alloys). However, many of these metal candidate suffer from thermal instabilities leading to a degraded interface with the underlying high-k dielectrics [6]. Recently, Ru and $RuO_2$ thin films have been investigated as gate electrodes to overcome the challenges associated with the introduction of gate metals due to its relatively high work function (4.7 eV) [7]. Ruthenium thin films have been deposited by several processes such as physical vapor deposition (PVD) [8, 9], chemical vapor deposition (CVD) [10, 11], and atomic layer deposition (ALD) [12, 13]. Several precursors have been studied for Ru-based films including solid precursor such as $RuCp_2$ [12, 13], (Cp=cyclopentadienyl) $Ru(acac)_3$ [14], (acac= acetylacetone), $Ru(tmhd)_3$ [15], (tmhd = 2,2,6,6-tetramethyl-3,5-heptanedionate), and liquid precursors such as $Ru(EtCp)_2$ [16-18], and $Ru(OD)_3$ [19], (OD=2,4-octanedionate). In the process of $Ru(Cp)_2$ [12, 13] the films were grown at temperatures of 275-400°C and oxygen was used to oxidatively decompose the ligands of the metal precursor. Unlike other inert metals (ie platinum) ruthenium is susceptible to oxidation but $RuO_x$ formation was not reported. Because precursors are feed simultaneously during

CVD process, it is likely that the chemical reaction are different from the surface reactions that take place during ALD processes.

To better understand the chemical reaction that take place during ALD process we report ALD ruthenium films deposited from $Ru(Cp)_2$ and molecular oxygen using online Auger Electron Spectroscopy (AES). AES identifies elemental compositions of the top few layers of a surface by measuring the energies of Auger electrons. Electrons of energy 3-20keV are incident upon a conducting sample. These electrons eject core electrons from atoms contained in the sample resulting in a photoelectron and an atom with a core hole. The atom then relaxes via electrons with a lower binding energy dropping into the core hole. Therefore, AES cannot detect hydrogen or helium, but is sensitive to all other elements, being most sensitive to the low atomic number elements. The energy thus released can be converted into an Xray or emit an electron. This emitted electron is called an Auger electron after Pierre Auger who discovered this relaxation process [20]. Since the Auger process emits two electrons, the atom is left in a doubly ionized state. The energy of the Auger electron is characteristic of the element that emitted it, and can thus be used to identify the element. The short inelastic mean free path (IMFP) of Auger electrons in solids ensures the surface sensitivity of AES. Utilizing online Auger analysis minimizes the inaccuracy of composition calculation due to adsorbed impurities on the surface from ambient exposure.

**Experimental Approach**

Thin elemental ruthenium films were deposited by atomic layer deposition (ALD) (see Figure 7.1) on hafnium dioxide dielectric substrates. The hafnium oxide dielectric substrates were provided by Texas Instruments Inc. with thickness ~ 35Å. The ALD ruthenium films were formed with Bis(cyclopentadienyl)ruthenium precursor (purchased from Strem Chemicals, Inc. with 99% purity) and molecular oxygen (purchased from National Welders, Inc. with 99.99% purity). Argon gas (purchased from National Welders, Inc. with 99.99% purity) was used as a carrier gas for ruthenium precursor and as the purge gas between reactant pulses. The $HfO_2$ dielectric substrates were loaded as received from Texas Instruments into the ALD reactor for ALD ruthenium films.

Ru thin films with varying thicknesses were deposited at 325°C & 380°C. The films were transferred from the process chamber to the analysis chamber at pressures $<1x10^{-5}$ Torr. Film characterization was preformed using Auger Electron Spectroscopy (AES). AES was conducted using a Physical Electronics' (PHI's) Model 3017 Auger Electron Spectroscopy Subsystem with a 5keV, 10μA electron beam and a high sensitivity Cylindrical Mirror Analyzer (CMA). Auger spectra were obtained at pressure $< 2x10^{-8}$ Torr.

## Results and Discussion

### A. Thermal Pretreatment

The extent of water adsorption during ambient exposure for $HfO_2$ dielectric films is determined by monitoring the oxygen KLL (~510eV) and carbon KLL (~275eV) AES peaks before and after thermal annealing. Figure 7.2 shows these AES peaks with initial conditions (of the films as received from Texas Instruments, Inc.) and after a 325°C thermal treatment for 40 minutes. The oxygen peak shows a decrease in peak-to-peak height, which is indicative of water evolving from the $HfO_2$ surface and consistence with reported literature of high-k dielectric adsorbing water when exposed to ambient conditions [21]. However, the carbon shows an increase in peak-to-peak height after thermal treatment. The presence of a carbon peak after thermal treatment is associated with carbon incorporation into the film during deposition process used to grow the $HfO_2$ film. The increase in peak intensity is a result of electron beam penetrating deeper into the dielectric film since the previous adsorbed water layer has been removed from the thermal treatment.

### B. ALD Ru Film Growth

Figure 7.3 shows AES spectra of ALD ruthenium film growth from 100 to 350 cycles. These films were deposited at 325°C and 1.0 Torr. The first three spectra are from the ALD cycle after the $O_2$ pulse, which completes the ALD cycle. These spectra show an increasing peak intensity at ~277eV (Ru MNN and C KLL) and a decreasing peak intensity at ~510 eV (O KLL). These peak changes thus represent ruthenium film growth. Sufficiently thick Ru films are necessary so that the underlying $HfO_2$ film does not contribute to the oxygen peak intensity. As can been seen in Figure 7.3, the Ru film was sufficiently

thick after 250 cycles to avoid peak interferences. The slow film growth illustrates the ALD process of Ru films is sensitive to film coalescence. After the Ru films were sufficient thick enough, an additional 100 cycles were deposited and stopped after the $RuCp_2$ pulse, which is only half the ALD, cycle. This fourth spectrum (seen in Figure 7.4) shows a dramatic increase in peak intensity at ~277eV and a decrease in peak intensity at ~510eV indicating that different chemistries are involved during the precursor and oxygen pulses. Another series of ALD Ru film were grown at 380°C, shown in Figure 7.5. Similarly, the Ru films were sufficiently thick enough after 200 cycles to avoid spectra interference from the underlying $HfO_2$ film. After sufficient film thickness was established an additional 9 ½ cycles were deposited. The last cycle was terminated after the metal precursor pulse, which is half the cycle and label $210^*$ with the * indicating a half cycle. The increase in C KLL peak intensity and the decrease in O KLL peak intensity follow the same trend as films grown at 325°C. Then, the remaining half cycle was completed (eg., completing the $210^{th}$ cycle) in which the Ru film was allowed to be exposed to the final oxygen pulse. Noticeably, the spectra of 200 and 210 cycles for practical purposes are identical.

Because of the large carbon/ruthenium peak intensity during the metal precursor pulse and the abundance of oxygen during the molecular oxygen pulse, the following chemistries are used to describe the chemical process of steady-state ALD ruthenium film growth. During the reactant pulse, the oxygen plays two roles. First, the unreacted metal precursor ligands adsorbed on the surface react with the oxygen releasing volatile byproduct yielding further Ru film growth. Secondly, a layer of adsorded oxygen must have been formed on the ruthenium surface during the oxygen pulse. During the metal precursor pulse, the adsorbed oxygen reacts with part of the ligands, which become volatile byproducts. The

extent of reacted ligands is determined by the amount of available adsorbed oxygen. Therefore the oxidation reaction is completed during the oxygen pulse step.

The amount of available adsorbed oxygen on the ruthenium film at 325 and 380°C can been seen in Figure 7.6. This figure shows the surface composition of the ruthenium films with atomic percent of Ru (▲), O (●), C (■), with solid connecting lines for 325°C films and dashed connecting lines for 380°C films. The atomic percent of oxygen increases from 43% at 325°C to 64% at 380°C. This increase in oxygen content at the ruthenium surface is consistent with previous studies, which show that at room temperature the maximum surface coverage of oxygen is 0.5 ML and at temperatures above 280°C the oxygen begins to penetrate into the subsurface region after surface saturation [22]. This penetrating oxygen into the subsurface can react with metal precursor ligands since previous studies have shown this oxygen to be mobile [23]. However, in addition to film temperature, the amount of available adsorbed oxygen in ruthenium may depend on reactor design and process conditions such as oxygen dose and reactor pressure.

## Conclusions

Film compositions of ALD ruthenium films from $RuCp_2$ and molecular oxygen were studied with online Auger electron spectroscopy. Based on the AES results, the $RuCp_2$ were partially oxidized into volatile byproducts and the oxidation reaction was completed during the oxygen pulse. Also, an adsorbed oxygen layer formation in the ruthenium film was formed during the oxygen pulse. No ruthenium oxide films were formed since the AES spectra shows that all the adsorbed oxygen in consumed in the complete oxidation reaction. The extent of adsorbed oxygen into the ruthenium film increases with film temperature.

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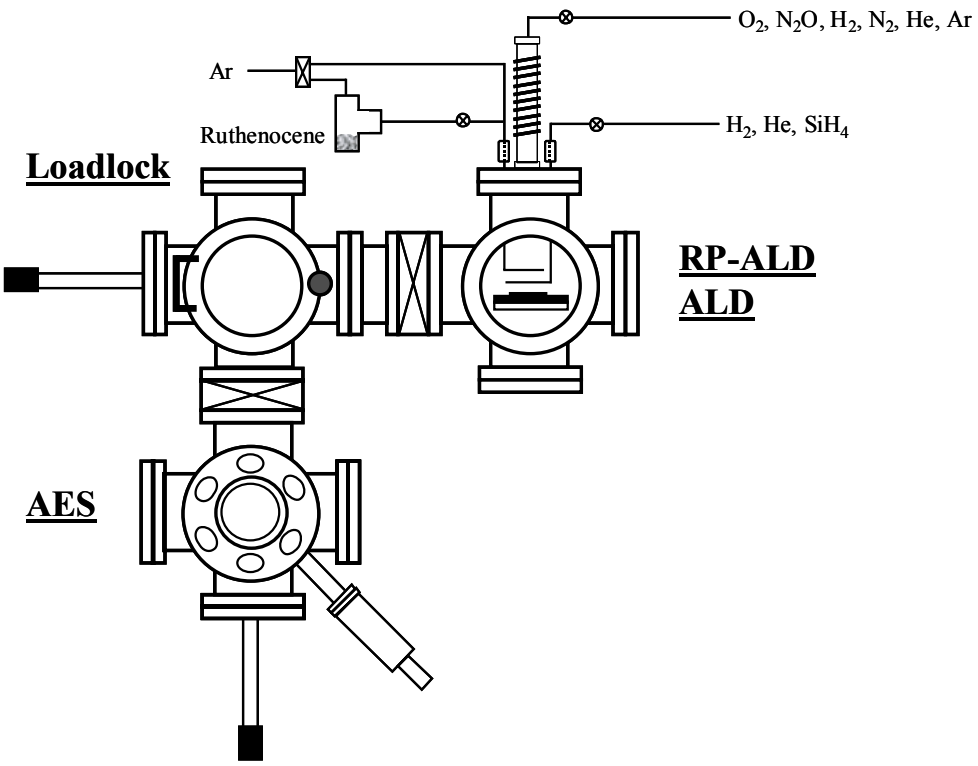
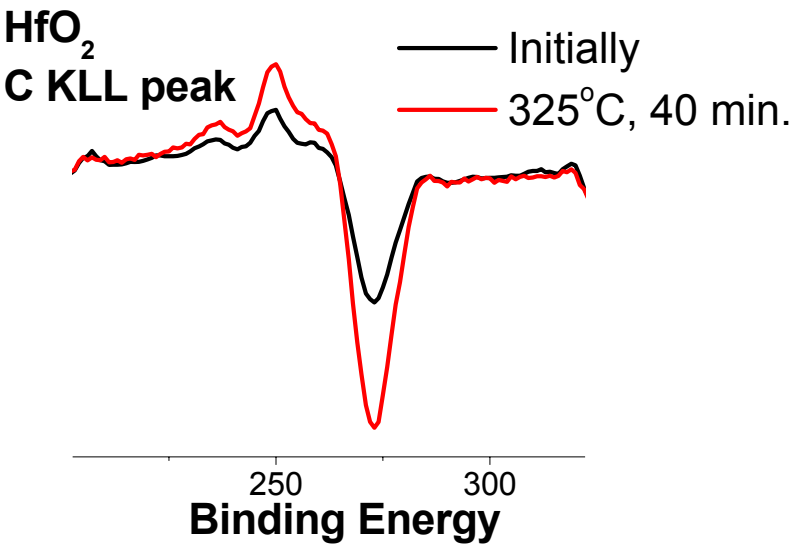



Figure 7.1: Schematic drawing of ALD Reactor



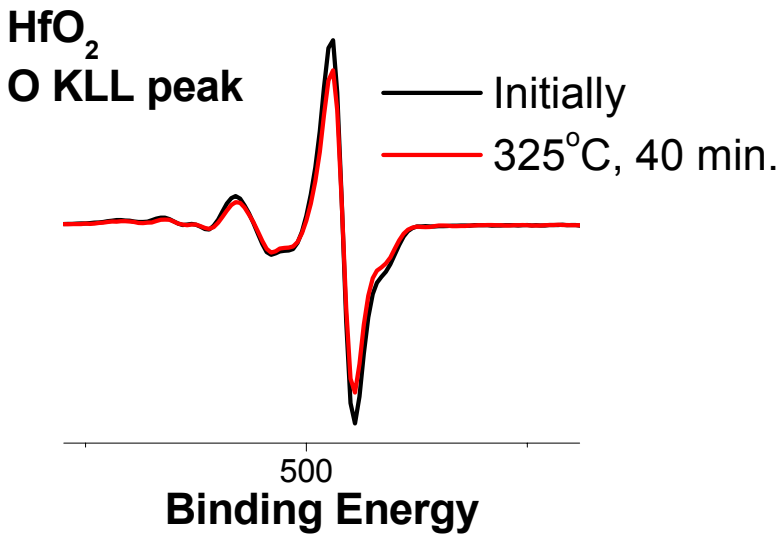




Figure 7.2. AES of C KLL peak and O KLL peak of $HfO_2$ at initial condition and after a 325°C thermal treatment for 40 minutes.

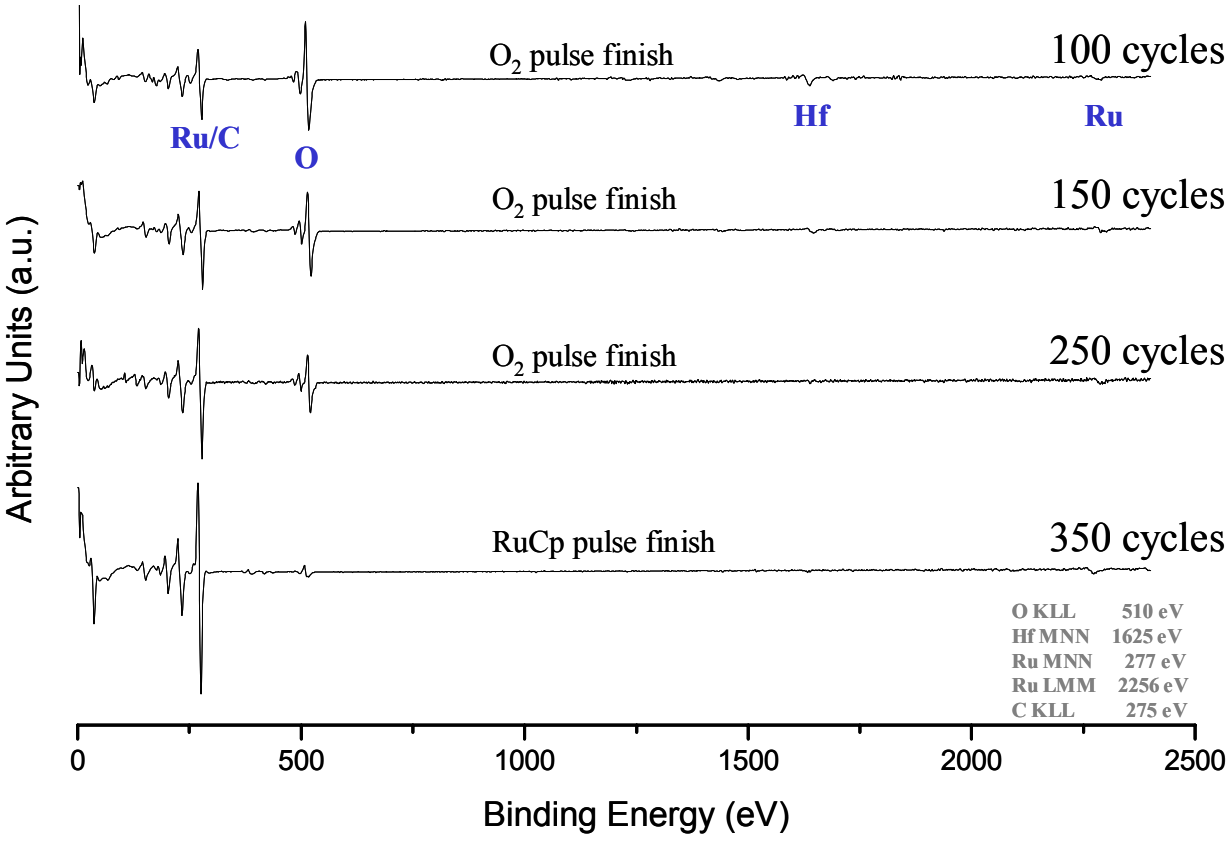



Figure 7.3. AES Survey Spectra of ALD Ru growth series

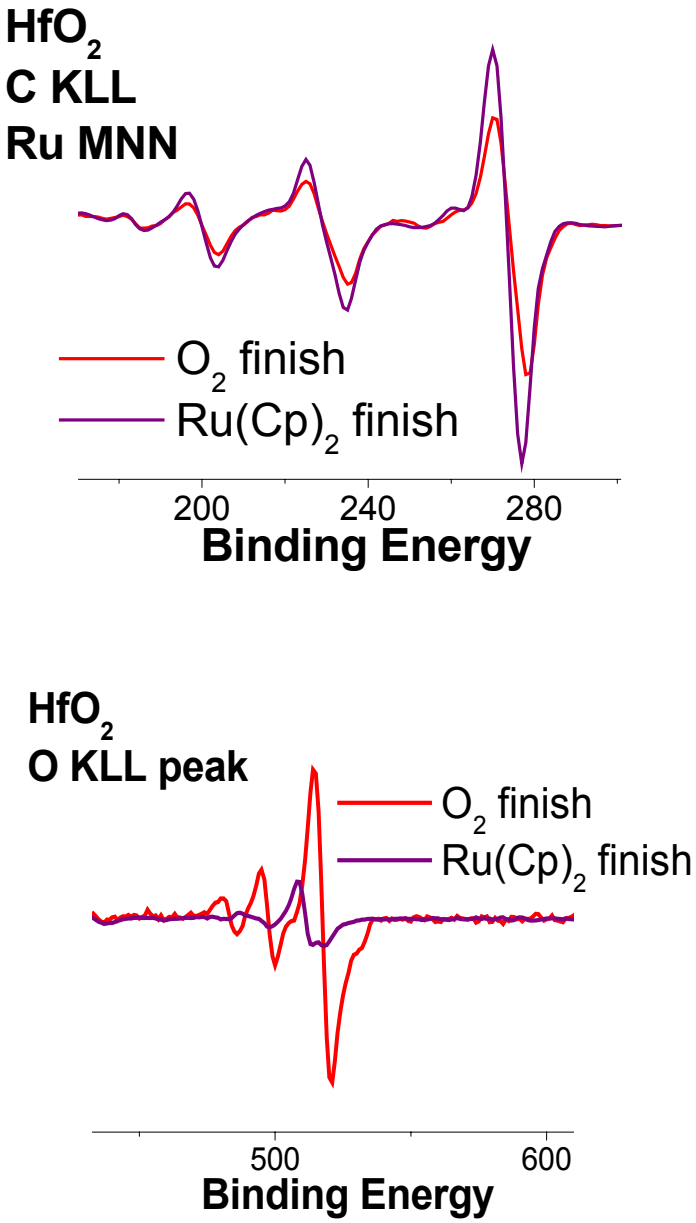



Figure 7.4. The C KLL peak and O KLL peak of ALD Ru films at after $O_2$ pulse and $Ru(Cp)_2$ pulse during the ALD process.

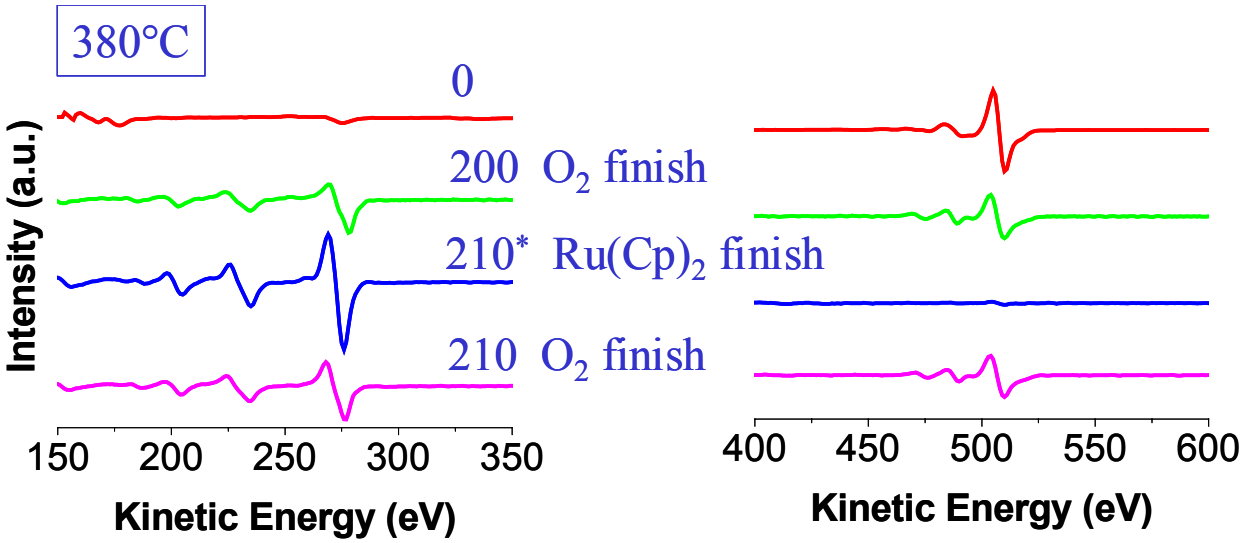



Figure 7.5. AES spectra of ALD Ru films at 380°C

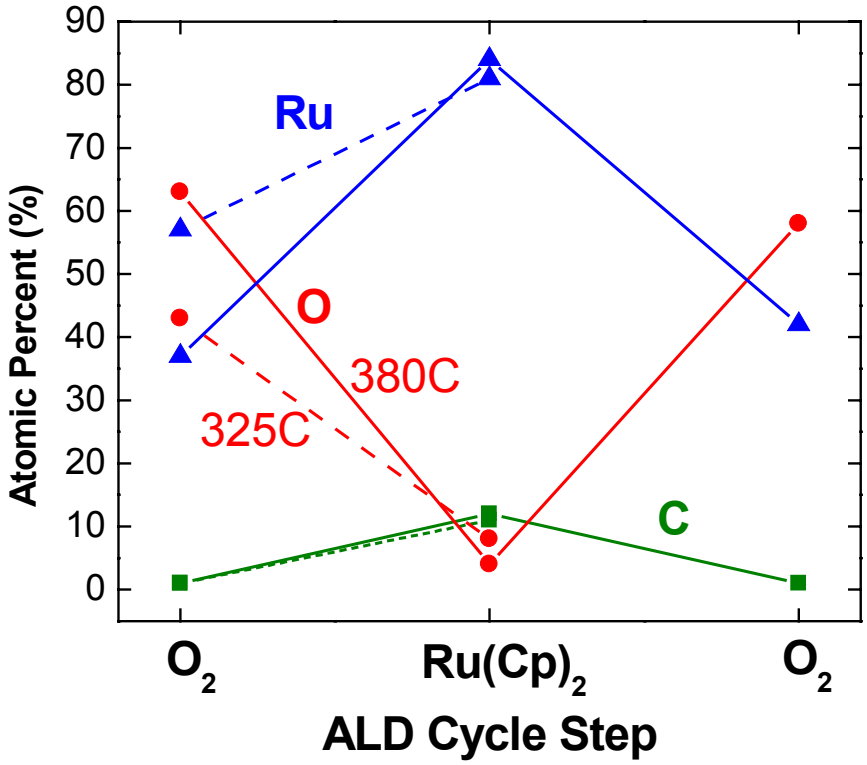



Figure 7.6. Atomic percent composition of Ru film surface during each step of the ALD process.