Abstract

HAN, CHONG. Power System Dynamic Voltage Management with Advanced STATCOM and Energy Storage System. (Under the direction of Dr. Alex Q. Huang).

STATCOM (static synchronous compensator) and ESS (energy storage system), as a shunt-link flexible AC transmission system (FACTS) controller, has shown extensive feasibility in terms of cost-effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. Recently, advances in power electronics technologies, such as the emerging kilohertz high power semiconductor switches, cascaded multilevel converter (CMC) topology comprising modular H-bridge voltage source converter (VSC), and digital control technology, have the potential to achieve the modularity and scalability design, lower the overall cost, and improve the reliability and functionality of power electronics-based controllers, hence, resulting in increasing applications of STATCOM/ESS. However, how to control a CMC-based STATCOM/ESS to realize excellent performance, high reliability and low cost poses the challenges to researchers.

On the other side, renewable large wind farms, as a fast growing power generation method, undergoes its inherent power quality and stability issues. How to develop the effective and accurate model of a wind power system and how to control STATCOM for wind power support are not in a classical textbook and posing challenges. Meanwhile, as an industrial customer of utilities, electrical arc furnace (EAF) is the major flicker source that degrades the grid power quality. How to economically and efficiently mitigate EAF flicker is a tough issue bothering utility professionals. As a promising solution, a high bandwidth STATCOM/ESS can be used.

This dissertation is dedicated to a comprehensive study of CMC-based STATCOM and its ultracapacitor energy storage system (UESS), and its applications in power system dynamic voltage management, specifically, wind farm voltage fluctuations suppressions and EAF flicker mitigation. The goal of this dissertation is to achieve high-performance, reliable, flexible, cost-effective controllers of the CMC-based STATCOM/UESS for the specific challenging utility applications. Major contributions proposed in this dissertation include:

1) STATCOM model analysis and compensator design guideline;

2) STATCOM AC-side energization and de-energization;

3) STATCOM per-phase DC voltage balancing;

4) wind farm voltage fluctuation suppression;

5) EAF flicker mitigation;

6) modeling, integration and control of UESS.

Power System Dynamic Voltage Management with Advanced STATCOM and Energy Storage System

by

Chong Han

A dissertation submitted to the Graduate Faculty of
North Carolina State University
in partial fulfillment of the
requirements for the Degree of
Doctor of Philosophy

Electrical Engineering

Raleigh, North Carolina

2006

Approved by

Dr. Alex Q. Huang Chair of Advisory Committee	Dr. Mesut E. Baran
Dr. Mo-Yuen Chow	Dr. Subhashish Bhattacharya
Dr. Tomislav Vukina	

To My Wife Shiping & Daughter Shelly

and

My Parents Zizhang & Meijiao

Biography

Chong Han was born in Jiangxi, China. He received his Bachelor degree with Advanced Class honor in Electrical Engineering from Huazhong University of Science and Technology (HUST), Wuhan, China, in 1999. Since 1998, he has been with the power system automation real-time TNA lab and superconducting power research center, HUST, Wuhan, China.

In 2001, he earned a scholarship and joined the Center for Power Electronics System (CPES) in the Bradley Department of Electrical and Computer Engineering at Virginia Tech (VT), Blacksburg, VA. In 2004, he received his Master degree in Electrical Engineering at Virginia Tech and joined the Semiconductor Power Electronics Center (SPEC) in the Department of Electrical and Computer Engineering at North Carolina State University (NCSU) to continue his Ph.D. study.

His current research interests include modeling and control of AC/DC and DC/DC power converter, power electronics applications in power systems, real-time TNA, energy storage system, and power system simulation.

He is a member of the Eta Kappa Nu Honor Society and the IEEE power electronics society, power system society, industry applications society, and industry electronics society. He also served as a student council committee member of CPES and the president of 1st student council committee of SPEC.

Acknowledgements

First of all, I would like to express my greatest appreciation to my advisor, Dr. Alex Q. Huang, for his guidance, encouragement and continuous support. His extensive knowledge, broad vision and creative thinking supported me throughout my research and study. His guidance made me never stick in the mud but encouraged me to bravely move forward and inspire myself. Maybe the personality, research methodology and attitude I learned from him are much more important than the knowledge of electrical engineering. I will cherish this valuable experience I spent in North Carolina State University (NCSU) and Virginia Tech (VT) under his great guidance and continuous support forever.

My gratefulness also goes to my committee members: Dr. Mesut E. Baran, Dr. Mo-Yuen Chow, Dr. Subhashish Bhattacharya, Dr. Tomislav Vukina, and Dr. John J. Grainger, who taught me courses, passed me knowledge, and served my advisory committee. I appreciate Dr. Mesut E. Baran and Dr. Subhashish Bhattacharya for their valuable discussions, encouragement and comments on my research. I would like to thank Dr. Dushan Boroyevich, Dr. Fred Wang, and Dr. Yilu Liu at Virginia Tech for their guidance and suggestions.

I am also indebted to all faculty, staff, and students at the Semiconductor Power Electronics Center (SPEC) and Center for Power Electronics Systems (CPES) for their support and friendship, which made my stay at SPEC and CPES pleasant and enjoyable.

I am especially indebted to my colleagues in the high power group. Thanks to Dr. Yunfeng Liu, Dr. Zhenxue Xu, Dr. Bin Zhang, Dr. Siriroj Sirisukprasert, Dr. Xigen Zhou, Mr. Hongfang

Wang, Mr. Joshua Hawley, Mr. Bin Chen, Mr. Wei Liu, Mr. Zhaoning Yang, Mr. Andrew Schmit, Dr. Zhong Du, Mr. Wenchao Song, Mr. Karan Tewari, Mr. Yu Liu, Mr. Tiefu Zhao, Mr. Shoubik Doss, Mr. Jun Li, Mr. Xiaohu Zhou. It was my pleasure to work with such talented and creative fellows. I also greatly appreciate their help and friendship among us.

Besides, it has been a great pleasure to work with so many talented colleagues at NCSU and VT, especially SPEC and CPES. The time while working was helped along by so many friends, and my life at Raleigh and Blacksburg became so colorful with the presence of them. I am grateful for Dr. Yong Li, Mr. Dengming Peng, Dr. Wei Dong, Dr. Qun Zhao, Dr. Bo Yang, Dr. Peter Barbosa, Dr. Francisco Canales, Dr. Kaiwei Yao, Dr. Jinjun Liu, Dr. Zhou Chen, Dr. Changrong Liu, Dr. Sihua Wen, Dr. Lingyin Zhao, Dr. Rengang Chen, Dr. Jia Wei, Dr. Jinghong Guo, Dr. Ming Xu, Dr. Gang Chen, Dr. Rolando Burgos, Dr. Zhenxian Liang, Mr. Nick Sun, Mr. Yu Meng, Dr. Xin Zhang, Ms. Ji Pan, Dr. Haifei Deng, Ms. Yan Ma, Dr. Shuo Wang, Dr. Yang Qiu, Ms. Juanjuan Sun, Dr. Yuancheng Ren, Dr. Jinghai Zhou, Ms. Li Ma, Dr. Bing Lu, Dr. Huiyu Zhu, Mr. Mao Ye, Dr. Yingfeng Pang, Mr. Carl T. Tinsley, Mr. Jerry Francis, Dr. Chucheng Xiao, Mr. Liyu Yang, Ms. Tingting Sang, Dr. Zhiye Zhang, Dr. Xiaoming Duan, Ms. Manjing Xie, Dr. Wenduo Liu, Dr. Qian Liu, Dr. Wei Shen, Ms. Shen Wang, Dr. Jian Yin, Mr. Sebastian Rosado, Dr. Li Zhang, Dr. Steven Tsai, Mr. Xiangfei Ma, Dr. Ning Zhu, Mr. Dianbo Fu, Mr. Chuanyun Wang, Ms. Chunchun Xu, Ms. Yan Jiang, Ms. Xi Xiong, Mr. Daniel Ghizoni, Mr. Tim Thacker, Mr. Ding Li, Mr. Julu Sun, Mr. Jinseok Park, Ms. Yan Gao, Mr. Hongtao Mu, Mr. Yang Gao, Mr. Ali Hajjiah, Ms. Yan Liang, Ms. Jing Xu, Ms. Michele Lim, Mr. Yan Dong, Mr. Jinsang Kim, Mr. Mohamed Haj-Maharsi, Mr. Ning Zhu, Ms. Xiaojun Xu, Mr. Yi Du, Mr. Jun Wang, Mr. Jiwei Fan, Mr. Xin Zhou, Mr. Jeesung Jung, Mr. Sungkeun Lim, Mr. Xiangzhong

Xue, Ms. Zhengping Xi, Mr. Rahul Godbole, Mr. Gunjan Patel, Mr. Xiaopeng Wang, Ms. Rong Guo, Mr. Jinfeng Qin.

I would like to thank Mr. Michael R. Ingram at Tennessee Valley Authority (TVA), Mr. Stanley Atcitty at Sandia National Laboratories, Mr. Wayne Litzenberger, Mr. Loren Anderson, and Mr. Anders Johnson at Bonneville Power Administration (BPA), Dr. Abdel-Aty Edris at Electric Power Research Institute (EPRI), and Mr. Haresh Kamath at EPRI Solutions for their suggestions and comments on my research projects, and, more importantly, bringing me a golden opportunity to join these state-of-the-art projects. I would also like to thank US Department of Energy (DOE), Sandia Lab, TVA, BPA and EPRI for their support of my research projects.

I would like to acknowledge the administrative and lab management staff at NCSU and VT, Mr. Jerry Kirk, Mr. Brian P. Carty, Mr. Dan Green, Ms. Fay Bostic, Ms. Tara Britt, Ms. Dawn Hartley, Ms. Elaine Hardin, Ms. Pascale Toussaint, Ms. Teresa Shaw, Ms. Elizabeth Tranter, Ms. Marianne Hawthorne, Ms. Ann Craig, Ms. Trish Rose, Ms. Linda Gallagher, Mr. Robert Martin, Mr. Steve Chen for the countless ways they have helped in my work. Thanks are also given to Ms. Nancy House and Ms. Alice Osborn, who polished my publications and dissertation.

As a part of my graduate study, the 2005 summer internship at the Semtech Corporation and the 2006 summer internship at the corporate research center (CRC) of ABB was a very good time and introduced me to a number of great people, who gave me real world experiences and broadened my career vision. Thanks to Mr. Tom Karpus, Mr. Bill Radar, Mr. Tom Ivins, Dr. Warren Schroeder, Ms. Maya Yarbrough, Mr. Brian McLean, Mr. Anousone Sibounheuang, Ms. Xiao Xu, Mr. Steven Granger, Mr. Bob Borden, Mr. Athar Zaidi, Mr. Pankaj Kashikar, Mr. Paul Hirtle, Dr. Zhenyuan Wang, Dr. Le Tang, Dr. David Lubkeman.

I would like to express my sincere and deep appreciation to all my dear friends and tutors in China, USA and anywhere else who encouraged me in the past, are promoting me achieve this success and will inspire me in the future. Without them, a beautiful and enjoyable life is a mission impossible!

To my dear Dad and Mom, Zizhang Han and Meijiao Lv, I know you must be so cheerful to know that I am going to accomplish a Ph.D. degree. And I would like to tell you that I am so proud to be your son. Together with my brother, you are supporting me all the time through my life. I would like to thank my beloved parents who are always with me in my heart. I would like to dedicate all of goodness from this dissertation to them. I also greatly appreciate my uncle, Wanmin Han, and his family for their consistent support and encouragement during my study to pursue advanced degrees.

Finally, and most importantly, I highly appreciate my wife, Shiping Chen, for her love, understanding, encouragement and sacrifice. If it were not for her, my dreams would never come true. Thanks to my lovely daughter, Shelly, who bring me the pride and happiness of being a father. They are my eternal source of inspiration in every aspect and every moment of my life.

TABLE OF CONTENTS

LIST OF FIGURES ..... **x**

LIST OF TABLES ..... **xvi**

Chapter 1 Introduction **1**

1.1 Background 1

I. STATCOM *2*

II. Energy Storage System *7*

III. Arc Furnace Flicker Mitigation *8*

IV. Renewable Wind Power Support *9*

V. Semiconductor Devices *11*

VI. Converter Topology *16*

VII. Control Technology *19*

1.2 Motivation 22

1.3 Dissertation Outline 23

Chapter 2 Improved Modeling and Control of Cascaded Multilevel Converter-based STATCOM **27**

2.1 Review on Modeling and Control of CMC-based STATCOM 27

2.2 Transfer Functions Analysis of CMC-based STATCOM 37

2.3 Energization and De-energization of CMC-based STATCOM 45

2.4 Per-phase DC Voltage Balancing of CMC-based STATCOM 50

2.5 Design and Demonstration of a 4.5MVA CMC-based STATCOM 56

I. System Integration *56*

II. Passive Components Selection *59*

III. Digitial Controller *63*

IV. Transformless Grid-Connected Demonstration *67*

2.6 Conclusion 71

Chapter 3 Wind Farm Voltage Fluctuation Suppression **73**

3.1 System Description 74

3.2 Modeling and Control 77
I. 12-Bus System Model *77*
II. Wind Farm Model *78*
III. Model Validation *79*
IV. STATCOM Model and Control *82*
3.3 System Study and Analysis 84
3.4 Conclusion 91

Chapter 4 Electric Arc Furnace Flicker Mitigation 93

4.1 Case Description and Steady-state Analysis 94
4.2 Field Data-based Study 99
I. Problem Description *99*
II. Soluion Comparison *103*
III. Modeling and Control for Field Data-based Study *107*
IV. Case Study *110*
4.3 Modeling and Control of STATCOM for EAF Flicker Migitation 112
4.4 TNA System and Experiement Results 118
4.5 Conclusion 125

Chapter 5 Modeling, Integration, and Control of Ultracapacitor Energy Storage System 127

5.1 Modeling of Ultracapacitor Energy Storage 127
5.2 Integration of Ultracapacitor with Modular Voltage Source Converter 132
5.3 Control of CMC-based Ultracapacitor Energy Storage System 135
5.4 TNA System and Experimental Results of CMC-based UESS 140
5.5 Conclusion 145

Chapter 6 Conclusions and Future Research 146

6.1 Conclusions 146
6.2 Future Research 152

References 154

LIST OF FIGURES

Figure 1-1. Single-line diagram of the voltage-source converter-based STATCOM. 3

Figure 1-2. An ETO Prototype. 14

Figure 1-3. Snubberless turn-off of ETO.....14

Figure 1-4. A general three-phase wye-configuration CMC. 18

Figure 2-1. Schematic of a cascaded-multilevel converter-based STATCOM system. 28

Figure 2-2. Average model of the cascaded-multilevel converter-based STATCOM in the ABC frame.....29

Figure 2-3. Average model of the cascaded-multilevel converter-based STATCOM in the ABC frame.....29

Figure 2-4. A simplified average model for the cascaded-multilevel converter-based STATCOM in the ABC frame. 31

Figure 2-5. Simplified average model for the cascaded-multilevel converter-based STATCOM in DQ0 coordinates. 32

Figure 2-6. Small-signal model for the cascaded-multilevel converter-based STATCOM in DQ0 coordinates. 33

Figure 2-7. Open-loop transfer functions. 36

Figure 2-8. Completed control block diagram of the CMC-based STATCOM. 37

Figure 2-9. Bode plot of full-order control-to-current transfer function 40

Figure 2-10. Bode plot comparison of full-order and 2^{nd} reduced-order control-to-current transfer functions.....42

Figure 2-11. 1^{st} and 2^{nd} reduced-order control-to-current bode plot: (a) without delay (b) with delay.....44

Figure 2-12. A group of designed loop gains during charge and discharge of DC capacitors. 47

Figure 2-13. (a) Simulation results of STATCOM whole operating process, (b) experimental results of STATCOM energization, (c) experimental results of STATCOM de-energization.....49

Figure 2-14. Per-phase DC voltage balancing control block diagram. 51

Figure 2-15. Bode plot of a per-phase Vdc balancing loop. 53

Figure 2-16. Simulation results of per-phase Vdc balancing control: (a) standy mode, (b) capactive mode, (c) inductive mode, and (d) Vdc balancing during Iq step change. 54

Figure 2-17. Experimental results of per-phase Vdc balancing control: (a) standby mode, (b) capactive mode, (c) inductive mode, and (d) capacitive mode step to standby mode, (e) inductive mode step to standby mode, (f) standby mode step to capacitive mode, and (g) standby mode step to inductive mode. 55

Figure 2-18. 1.5MVA ETO-based modular VSC and its full-rating test results: (a) prototype picture, and (b) full-rating open-loop test results. 56

Figure 2-19. Simulation result of a 4.5 MVA ETO and CMC-based STATCOM. 57

Figure 2-20. Schematic diagram of a 4.5MVA STATCOM: (a) one-line diagram, and (b) 480V/500A demonstration diagram. 58

Figure 2-21. System integration diagram of the STATCOM 59

Figure 2-22. DC capacitance formula derivation schematic in half cycle: (a) Vdc and Vo, (b) capacitive Io, and (c) equivalent Io integral. 61

Figure 2-23. Relationship among Vripple, Cdc and M 61

Figure 2-24. STATCOM 480 V/500 A setup 63

Figure 2-25. Simulation results.....64

Figure 2-26. Central controller setup 65

Figure 2-27. STATCOM operation modes.....66

Figure 2-28. STATCOM experiment waveforms: (a) energization, (b) de-energization, (c) capacitive 500A, (d) Iq step response, (e) + Q → -Q, and (f) - Q → +Q.....68

Figure 3-1. One-line diagram of the studied system.....75

Figure 3-2. Field SCADA data of wind farm typical operation. 77

Figure 3-3. Comparison of simulation result and field data at an operating point.....80

Figure 3-4. Comparison of simulation result and data for a 6 hour operation: (a) bus 2 voltage and power flow from bus 2 to bus 3, (b) bus 3 voltage and power flow from WF2, (c) bus 4 voltage and power flow from bus 4 to bus 5, and (d) bus 5 and 6 voltage and WF1 power output at bus 5 and 6.....81

Figure 3-5. Simulation results of the CMC-based STATCOM model.....83

Figure 3-6. Steady-state simulation results: (a) PV curve, and (b) VQ curve.....84

Figure 3-7. STATCOM voltage control capability vs. location: (a) (a) capacitive VAR vs bus 5 voltage, and (b) inductive VAR vs bus 5 voltage. 87

Figure 3-8. STATCOM external controller for voltage fluctuation suppresion.....88

Figure 3-9. comparison voltage fluctuation with or without STATCOM: (a) bus 2 voltage, (b) bus 3 Vvoltage, (c) bus 4 voltage, (d) bus 5 and 6 voltage, (e) bus 8 voltage, and (f) bus 11 voltage.....90

Figure 4-1. One-line diagram of a CMC-based STATCOM and EAF system 94

Figure 4-2. Hoeganaes arc furnace 94

Figure 4-3. Maximum permissible flicker in IEEE standard.....95

Figure 4-4. Reactive power compensation 96

Figure 4-5. Normalized $\Delta V_{PCC}/V_{PCC}$ (Q_C/S_{EAF}, X_S/R_S) 97

Figure 4-6. PSCAD/EMTDC simulation results 98

Figure 4-7. Calculation and simulation results 99

Figure 4-8. 45 MVA electric arc furnace: (a) one-line diagram, and (b) furnace photo..... 100

Figure 4-9. EAF field data: (a) 2hrs current and bus voltage, and (b) 9mins extracted bus voltage. 102

Figure 4-10. Worst-case EAF instantaneous real and reactive power..... 103

Figure 4-11. EAF compensation block diagram: (a) EAF without compensator, and (b) EAF with compensator. 104

Figure 4-12. Passive filter impedance for EAF flicker mitigation: (a) 2nd order low pass filter, and (b) 2nd order band pass filter. 106

Figure 4-13. Field data based EAF model. 107

Figure 4-14. Simulation results VS. field recorded data. 108

Figure 4-15. 30MVA STATCOM average model simulation results..... 109

Figure 4-16. Iq reference feedback methods. 110

Figure 4-17. Case study: (a) case 1: 4.5 MVA STATCOM, (b) case 2: 4.5 MVA STATCOM with 14 MVAr cap bank, (c) case 3: 30 MVA STATCOM, and (d) case 4: 30 MVA STATCOM with 14 MVAr cap bank. 111

Figure 4-18. EAF flicker worst-case model 113

Figure 4-19. One-line diagram of a CMC-based STATCOM 114

Figure 4-20. Simplified system model of a STATCOM and EAF system 115

Figure 4-21. STATCOM and EAF system model in dq0 frame 115

Figure 4-22. Small-signal model in dq0 frame of a STATCOM and EAF system 116

Figure 4-23. Flicker control block diagram 118

Figure 4-24. Real-time TNA of a STATCOM and EAF system.....119

Figure 4-25. Iq_ref command response of the STATCOM TNA.....120

Figure 4-26. High-speed solid-state AC-switch.....121

Figure 4-27. TNA experiment results of the EAF flicker.....122

Figure 4-28. Real-time TNA of a STATCOM and EAF system.....123

Figure 4-29. Comparison between TNA experiment results and PSCAD simulation results 124

Figure 5-1. Structure of a 2kV UCAP string.....128

Figure 5-2. UCAP measurement: (a) measurement setup, (b) capacitance measurement, and (c) ESR measurement. 129

Figure 5-3. Testing setup of a 2kV UCAP string. 130

Figure 5-4. 2kV UCAP string model development: (a) DC discharge testing results, and (b) simulation results with the extracted model.....131

Figure 5-5. Proposed interface to connect UCAP and VSC. 132

Figure 5-6. UCAP ESR-related Issues at high current operation condition: (a) UCAP voltage window utilization, and (b) UCAP efficiency Vs. UCAP current. 134

Figure 5-7. UESS control block diagram.....136

Figure 5-8. Typical operation range of a UESS. 137

Figure 5-9. UESS simulation results: (a) real power control, and (b) reactive power control. 139

Figure 5-10. Scaled-down UESS TNA system: (a) TNA setup, and (b) TNA schematic.....141

Figure 5-11. Experimental results of UESS four typical operating modes: (a) full discharge mode, (b) full charge mode, (c) full capacitive mode, and (d) full inductive mode. 143

Figure 5-12. Experimental results of UESS step response: (a) step change from +Q to –P, and (b) step change from -Q to +P. 144

LIST OF TABLES

Table 1-1. Comprison among STATCOM, SVC and MSC. 6

Table 1-2. Comprison among ETO, IGCT and IGBT. 15

Table 2-1. Demonstrated STATCOM Specification 62

Table 2-2. DC Bus Voltages and Ripples 69

Table 2-3. Voltages and THD at PCC 69

Table 2-4. Cooling Performance Measurement 70

Table 4-1. Specification of a CMC-based STATCOM and EAF TNA System 120

Table 5-1. UESS Prototype System Specification 138

Table 5-2. UESS TNA System Parameters 141

Chapter 1 INTRODUCTION

This chapter presents the background of this dissertation including a brief introduction on STATCOM and energy storage system (ESS), their utility applications, and the key technologies, which comprise a STATCOM/ESS system, including semiconductor devices, voltage source converter topologies and control technologies. The dissertation motivation is also discussed. An outline of the dissertation is given at the end of this chapter.

1.1 Background

Power electronics is one of the fastest changing and "enabling infrastructure technologies" in the field of electrical engineering today. Power electronics-based transmission controllers, also known as FACTS (flexible alternating current transmission systems) controllers [A1], are the key elements for transforming transmission and distribution (T&D) systems from being "passive" to "active" systems (that is, flexible, controllable, and securely utilized up to their thermal capacity).

Power electronics–based controllers can increase the capacity of existing transmission networks by allowing energy companies to direct power along specific corridors, aligning the physical flow of power with commercial transactions. In many instances, power electronics–based controllers can increase power transfer capability by up to 50% while maintaining transmission system security and stability.

On the other hand, the increasing frequency of blackouts, brownouts and small-scale outages is due primarily to the lack of quick voltage support, leading to voltage collapse and poor quality of power (low voltage, voltage flicker, harmonics, etc.) in many regions of the country.

Without a large amount of investment in transmission infrastructure, the use of power electronics systems to provide dynamic voltage support is critical to the security of electric power grids. Advances in power electronics technologies, such as the emerging emitter turn-off (ETO) thyristor, modular voltage source converter (VSC) technology, and digital control technology, have the potential of lowering the overall cost, improving the reliability, functionality and performance of power electronics-based controllers, hence resulting in increasing applications of these controllers. The development and demonstration of such an advanced power electronics-based transmission controller to solve the typical, emerging and challenging system issues, such as electric arc furnace (EAF) flicker mitigation and wind farm voltage fluctuation suppression, would give the utilities and industry customers the confidence to widely adopt these controllers.

I. STATCOM

The concept of the static synchronous compensator (STATCOM) was proposed by Gyugyi in 1976. In general, a STATCOM system consists of three main parts: a voltage source converter, a coupling reactor or a step-up transformer, and a controller, as shown in Figure 1-1. The magnitude and phase of VSC output voltage V_O can be regulated through the turn-on/turn-off of VSC switches, so that the VSC output current I_O can be controlled. Here, I_O is equal to the sum of the VSC output voltage V_O minus the voltage at an AC point of common coupling (PCC) V_{PCC} divided by the impedance of the coupling reactor Xs. In other words, the capacitive or

inductive output currents of a STATCOM can be achieved through regulating the magnitude of V_O to be larger or smaller than the magnitude of V_{PCC}. Meanwhile, the phase of V_O is almost in phase with V_{PCC} but has a small phase shift angle for compensating the converter internal loss and thereby keeping the system stable. Therefore, I_O can be controlled inherently and independently of V_{PCC}.

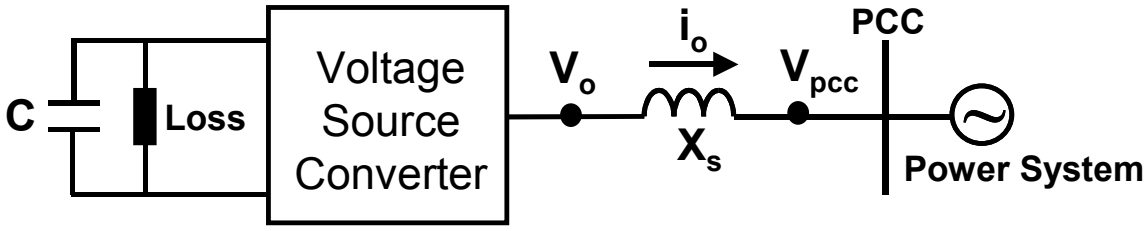


Figure 1-1. Single-line diagram of the voltage-source converter-based STATCOM.

Compared to its conventional FACTS counterparts like static var compensator (SVC), STATCOM has many advantages with its natures [A1]-[A3]:

- Voltage support capability: When STATCOM is VSC-based FACTS technology, its I_O is independent of AC line voltage. On the other hand, SVC, as impedance-based FACTS technology, its I_O is linearly proportional to the decrease of AC line voltage. Therefore, during contingencies, STATCOM provides more reactive power and stronger voltage support than SVC does.

- Transmittable power and transient stability: With the VSC-based nature of STATCOM and the impedance-based nature of SVC, STATCOM has a larger deaccelaration area than SVC with the same rating for a midpoint installation on a transmission line. Therefore, for the same transient stability margin, STATCOM can transmit more power than the SVC with the same rating, or STATCOM with smaller rating than SVC can transmit the same power on a line as SVC. In other words, when transmitting the same power, STATCOM has a larger transient stability margin than SVC.

- Response speed: Traditionally, a mechnical switch capacitor (MSC) has to complete a switching transience with a time span of several or even teen cycles. As a FACTS device, SVC includes TCR (thyristor controlled reactor) and TSC (thyristor switched capacitor). Limited by having no turn-off capability, TCR per-phase can be controlled per half cycle through changing the firing angle, and TSC needs a full cycle to update for a transient-free switching. However, with the semiconductor device having turn-off capability and VSC technology, STATCOM can update its control at least within a half-cycle with a line switching frequency (or so-called fundamental switching frequency). With the emerging fast semiconductor devices [D6][D7][D8], STATCOM can even have much faster control bandwidth and response time.

- Capability to exchange real power: Because of the VSC nature, STATCOM has the unique capability to interface with an energy storage system, exchange real power with the power network in bi-directions, and independently control both reactive power and real power, which is untouchable over the SVC.

- Harmonics: Compared to a MSC, whose switching angle cannot be accurately controlled, TSC can switch in a transient-free condition to accurately match voltages of capacitor bank and AC instantaneous voltages and, hence, have very low harmonics emission. However, a capacitor bank tends to incur resonance in an inductive bulky power system, though a small series reactor has been carefully tuned to avoid resonance. The output current of a basic TSR per-phase performs like an interception of ideal sinusoidal waveforms, and its harmonics is not relatively small. With parallel operation or multipulse arrangement, the TCR harmonics can be reduced, but a filter is typically required. With the innovation of VSC topologies and fast switching semiconductor devices and modulation methods, the harmonics emission of STATCOM is very low and does not require a filter.

- Loss VS VAR output characeritics: Both STATCOM and SVC have a loss about 0.1~0.2% around zero var output and about 1% for the full var output. But for semiconductor related loss, STATCOM is higher than SVC for conduction loss or switching loss. With the fast development of semiconductor devices, such as ETO/IGCT/IGBT and further SiC-based devices, the semiconductor related loss is expected to be reduced while the losses of convertional power components, such as reactors and capacitors, are not likely to be changed significantly.

- Physical size and installation: With high power density of semiconductor devices and VSC capability to circulate reactive power without large capacitor and reactor banks with their affiliated apparatus, such as switchfear, fuse and relay, the physical size of STATCOM can be significantly reduced (about 30~40%), as well as the installation

labor and cost, when compared to SVC. Moreover, a smaller physical size offers STATCOM potential mobility and convenience for relocation.

- Lifetime: Compared to a typical life of thousands operation times for mechanical breakers or switches, a semiconductor device has almost infinite switching cycles and 100 FIT (failures in trilion seconds). With less passive components, such as capacitor and reactor banks, STATCOM has an even longer lifetime than SVC. With fast development and improvement of semiconductor devices, the lifetime of STATCOM is expected to be improved further.

A characteristics comparison among STATCOM, SVC and MSC is shown in Table 1-1.

TABLE 1-1. COMPRISON AMONG STATCOM, SVC AND MSC.

Characteristic	STATCOM	SVC	MSC
Voltage support capability	Best	Better	Good
Speed of response	Fastest	Fast	Slow
Footprint	Smallest	Small	Small
Harmonics (without filter)	Small	Large	Large
Loss	Low	Lower	Lowest
Initial investment	High	Low	Low
Maintenance cost	High	High	Low
Technology lifecycle stage	Innovative	Maturity	Saturation

II. Energy Storage System

Energy storage system (ESS), as an "enabling infrastructure technology", not only can provide the "ride-through" over outages and improve profitability in high-energy applications, but it also can increase system reliability and dynamic stability, improve power quality, and enhance transmission capacity of the transmission grid in a high power application [A1][B1]. For a high power application, the use of short-term (cycles to seconds) energy storage integrated with a power electronics-based controller, well known as a FACTS controller, could offer the following three distinct advantages:

- Provide system damping, while maintaining constant voltage following a disturbance.

- Provide additional damping in situations where the dynamic reactive power provided by traditional FACTS controllers with similar ratings is inadequate. Alternatively, it could provide the same amount of damping at less cost. Damping of oscillation, by repeatedly interchanging small amounts of real power with the system, would be an excellent ESS application.

- Provide energy to maintain the speed of locally connected induction motors during a power system disturbance. This may prevent a voltage collapse in areas where there is a large concentration of induction motors that would otherwise stall.

While the superconductive magnetic energy storage (SMES) technology overcomes many barriers from a technology perspective and has been commercially available at some specific sizes, the cost and relative complexity of the overall SMES system still makes it an expensive choice for short-term ESS [B2]-[B5].

Recent advances in ultracapacitor (UCAP) technology with an asymmetric design have brought much excitement to the industry with the hope of a new and better short-term energy storage solution [B6][B7]. UCAP, as one type of electrochemical capacitor, stores electrical energy in the electric double layer using relatively inexpensive materials, provides energy density thousands of times larger than conventional electrolytic capacitors, and has miscellaneous advantages over other high-power energy storage devices: high power density, low cost, reliable and long cycle life, fast and deep charge/discharge capability, wide operation temperature, maintenance-free operation and storage, and is environmentally safe. These characteristics make UCAP a desirable energy storage element for short-term high-power ESS application at much lower cost.

III. Arc Furnace Flicker Mitigation

Recently, with the growth of manufacturing and population, power quality becomes more and more important. Flicker, as one of the most common power quality issues, is caused by feeder voltage fluctuation, which influences domestic lighting and the sensitive apparatus of nearby transmission and distribution systems. Electrical arc furnace (EAF), as a major industrial customer of a utility, consumes considerable real power and reactive power with the time-varying, stochastic and even chaotic characteristics during its melting and refining process and, therefore, returns severe flicker back to utility power grids [C1].

How to economically and efficiently mitigate EAF flicker is consistently a tough issue. The basic methodology for flicker mitigation can be categorized into three types: (1) Regulating the EAF passive components, such as source impedance [C2]. Although the added series reactance can to some extent mitigate the flicker, it reduces power supply capability and therefore

decreases EAF productivity. Moreover, it is also expensive and laborious to control upstream transformer reactance or series reactor in the deregulated power system. (2) Compensation through the combination of thyristor and passive components, such as the well-known SVC. Not only can SVC improve the power quality of a nearby system, but it also increases EAF productivity and brings additional economic benefits. However, its relatively low bandwidth cannot catch up with the time-varying flicker very well with the inherent limit of relatively low bandwidth and, hence, its dynamic performance for flicker mitigation is limited. (3) The state-of-the-art solution is the STATCOM based on the voltage-source-converter (VSC) [C3]. With fast response and flexible control, it performs better than SVC [C4]. At present, STATCOM is considered as a suitable FACTS unit for flicker mitigation [C12].

IV. Renewable Wind Power Support

Recently, due mainly to technology innovation and cost reduction, renewable wind energy is enjoying a rapid growth globally to become an important green electricity source to replace polluting and exhausting fossil fuels. The wind turbines with 2~3 MW capability have already been commercially available and a 5MW wind turbine will also be available in a few years. Moreover, the cost of wind energy has been reduced to 4.5 Cents/kWh and is very competitive against conventional fuels, and will be further reduced to 3 Cents/kWh for utility-scale wind energy onshore and 5 Cents/kWh offshore by 2012 [H1][H2]. Additionally, public policy is fostering further integration of wind energy into the power system.

However, with wind being a geographically and climatically uncontrollable resource and the nature of distributed wind induction generators, the stability and power quality issues of

integrating large wind farms in a grid may become pronounced, particularly in a weak power system.

Conventionally, the low cost mechanical switched cap banks (MSCs) and transformer tap changers (TCs) are used to address these issues which are related to stability and power quality. However, although these devices help improve the power factor of WF and steady-state voltage regulation, the power quality issues, such as power fluctuations, voltage fluctuations, and harmonics, cannot be solved satisfactorily by them because these devices are not fast enough [H3]. Moreover, the frequent switching of MSC and TC to deal with power quality issues may even cause resonance and transient over-voltage, adding additional stress on wind turbine gearboxes and shafts, making themselves and the turbines wear out quickly and, hence, increasing their maintenance and replacement cost [H4]. Therefore, a fast dynamic VAR compensator is needed to address these issues more effectively, as has been pointed out in many literature papers [H2][H4][H5][H6][H7].

The STATCOM is considered for this application, because it provides many advantages, in particular the fast response time (1~2 cycles) and superior voltage support capability with its nature of voltage source [A1]. With the recent innovations in high-power semiconductor switch, converter topology and digital control technology, faster STATCOM (quarter cycle) with low cost is emerging [E5][E10][E11], which is promising to facilitate integrating wind energy into the grid to achieve a more cost-effective and reliable renewable wind energy.`

V. Semiconductor Devices

About four decades ago, it was the invention of thyristors, also known as silicon-controlled rectifiers (SCR) that led to the emergence of power electronics applications and markets. SCR is still the dominant component used in HVDC systems due to its high power ratings. However, SCR has a limited application in FACTS controllers because it lacks the ability of controlled turnoff capability. Therefore, developing a power semiconductor switch with controlled turn-off capability has been a major focus for many semiconductor companies and researchers. Today, most FACTS controllers in service utilize the gate turn-off (GTO) Thyristor as the main power semiconductor switch due to its advantages over other available devices in power handling capacity, reliability, and cost. Its main disadvantage, however, is the need for a bulky snubber capacitor to protect the GTO during the turn-off process. The discharge of this snubber requires the significant power dissipation on a resistor, thereby increasing cost and size, or the use of complex energy recovery circuits, which again increase cost and size.

Turning the GTO off requires a gate current equal to 1/5 to 1/3 of the anode current that must be supplied for a long time by the gate driver resulting in an expensive and complicated gate driver design. Since the turn-off gain (anode current divided by gate current) is typically 3 to 5, the typical turn-off storage time is very long in the range of 20-45 microseconds. Additionally, the GTO requires a turn-on snubber to limit current rise rate until the entire GTO device has come into the conduction state, and to limit the reverse recovery of the diode being turned off. Therefore, due to the slow speed determined by the turn-on and turn-off processes, the switching frequency of GTO devices is low, typically below 500 Hz, and in many cases at a line frequency 60Hz. The low switching frequency increases the power converter's output harmonics that will have to be reduced by a large passive filter, which again increases the total cost.

The insulated gate bipolar transistor (IGBT) device, developed in the 1990s and based on the integration of fine-pattern metal oxide semiconductor field effective transistor (MOSFET) and vertical bipolar transistor, has improved dramatically, in power ratings and reliability. However, it has been quite clear for sometime that the IGBT technology needs further improvements to allow its use in high power applications. The weak conductivity modulation in the IGBT results in significantly higher conduction loss, thereby limiting the upper voltage rating that the IGBT can feasibly penetrate. Furthermore, the reliability of a high-current IGBT module is a major concern. Although an accurate number is hard to obtain, it is generally believed that the thermal cycling reliability of today's high power IGBT module is still 100 times worse than a traditional press pack device such as the GTO. Finally, because the internal electric field inside a high voltage IGBT is typically higher than a GTO, there is strong concern about the long-term stability of an IGBT-based power electronics converter.

Recent innovations in GTO based technology, such as GTO devices made using wafer level fabrication, make a large capacity GTO device relatively easy to achieve. Today, the GTO ratings have already reached 6kA and 6kV. The blocking capability of the GTO technology can be further extended to >10kV without a major cost increase. This is possible because the mesa junction termination technology used in GTO generally allows easier extension of the voltage capability compared with the planar junction termination technology used in the IGBT. More importantly, the double-sided injection allows stronger conductivity modulation, hence even at 10kV the forward drop of the GTO is still acceptable. The same cannot be said for the IGBT because of its weaker conductivity modulation.

Several innovations have been proposed to improve the GTO's switching speed so that it can be used as a high-frequency power switch. The two most notable ones are the integrated gate commutated thyristor (IGCT) developed by ABB and the emitter turn-off thyristor (ETO) developed by semiconductor power electronics center (SPEC), North Carolina State University. Fundamentally, both of these innovations concentrate on reducing the GTO's gate drive power consumption and eliminate the need for a dV/dt snubber. The IGCT and ETO differ in their approach, performance, and cost. The IGCT relies on a proprietary, expensive, special GTO wafer design plus a specially designed low inductance press pack housing. Due to a reduced gate inductance, the IGCT turn-off is performed in transistor mode instead of thyristor mode, hence the dV/dt snubber is reduced or eliminated. The speed of the device is also increased to allow higher frequency operation.

Generally, the cost of the power semiconductor switches and diodes used in a converter-based controller is about 50% of the overall cost of the controller. The emerging ETO thyristor combines the advantages of thyristor's high voltage/current capability and MOSFET's (Metal-Oxide Semiconductor Field Effect Transistor) easy gate control. Due to very high silicon utilization and a greatly simplified drive circuit, its cost is much lower than other high power competing technologies, such as GTO, IGCT, and IGBT. Figure 1-2 shows a 4.5 kV/4 kA ETO device which is used for the STATCOM in this dissertation [D2][D3].

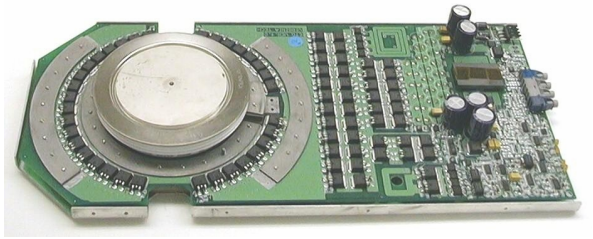


Figure 1-2. An ETO Prototype.

The turn-off operation of the ETO is similar to the IGCT in that it also turns off in the transistor mode instead of in the thyristor mode, allowing both high frequency operation and elimination of the dv/dt snubber. Figure 1-3 shows the ETO turn-off waveform at 5 kA, DC 2.2 kV and $T_j = 25^{O}C$ without dv/dt snubber. Furthermore, the gating power of the ETO is much lower than the IGCT because ETO is a voltage turn-off device while the IGCT is a current turn-off device.

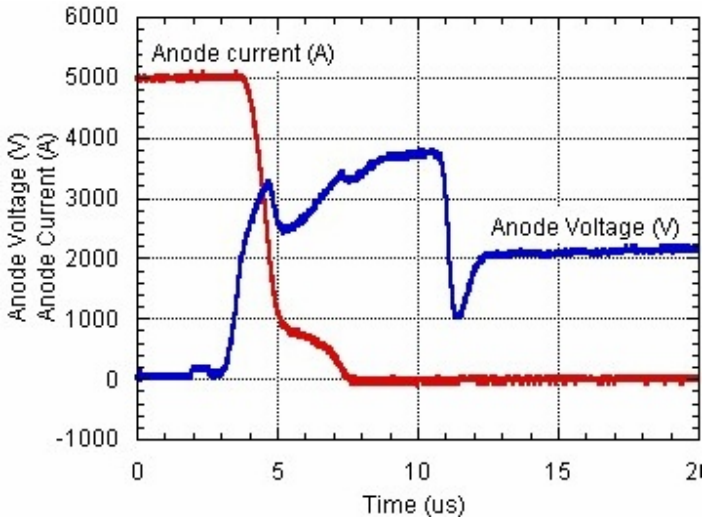


Figure 1-3. Snubberless turn-off of ETO.

The ETO shown in Fig. 1 is capable of switching at 1 kHz or above, hence enabling the use of pulse width modulation (PWM) in high-power voltage source converter applications. Table 1-2 is a qualitative comparison with other competing technologies.

TABLE 1-2. COMPRISON AMONG ETO, IGCT AND IGBT.

Characteristic	**ETO**	**IGCT**	**IGBT**
Conduction Losses	Good	Good	Poor
Positive Temperature Coefficient	Best	Poor	Good
Identical Switching Times	Best	Best	Good
Turn-Off Capability	Best	Good	Good
Built-In Current Sensing Capability	Yes	No	No
Control Power Needed	Low	Very High	Low
Cost per kW	Lowest	Low	Higher
Current Scalability	Easy	Difficult	Moderate
Technology Lifecycle Stage	Introduction	Maturity	Saturation

In summary, the characteristics that make the ETO a viable choice for today's high power applications include:

- Proven press pack packaging technology for high reliability

- Hybrid integration of two mature technologies resulting in lower cost
- Voltage and current ratings determined by the GTO and can be easily scaled to 6 kA, 6 kV (rating can be raised without major cost increase)
- Extremely easy for parallel and series connections deployment
- Voltage controlled turn-off resulting in significantly reduced gate driver power requirement
- Faster switching speed to allow high frequency pulse width modulation (PWM) control in a high power electronics system
- Snubberless turn-off capability resulting in low loss and component count
- Optical-driven switching making it flexible for control
- Built-in current sensing capability

VI. Converter Topology

Based on the number of their synthesized output voltage levels, VSCs can generally be categorized into two major groups: conventional two-level converters and more-than-two-level converters or multilevel converters. With recent power semiconductor technologies, a traditional two-level VSC is not competent for FACTS controller applications because of` the needing for bulky zigzag transformers and series/parrallel switches to match harmonics, voltage and power specfications [E1][E3].

An attractive alternative to the two-level converter is the multilevel VSC. Without semiconductor devices connected in series, the multilevel converters show the feasibility of clamping the voltages across individual devices below their limitations. This allows the recent semiconductor devices to be utilized in higher-voltage applications without incurring voltage-sharing problems. Another significant advantage of the multilevel configuration is the harmonic reduction in the output waveform even with a very low switching frequency.

In the past two decades, several state-of-the-art multilevel VSCs have been introduced by both universities and industries. Some of these have become quite popular, but some have not. Different topologies show their advantages in particular applications. In the literature, multilevel VSCs are categorized into two groups: topology-level multilevel converters and hybrid multilevel converters, which are either the transformer magnetic coupling multipulse converters or the hybrid combinations of topology-level multilevel converters. A detailed discussion about the types of multilevel VSCs can be found in [E1][E3][F1].

In the first category, there are four major capacitor-voltage synthesis-based multilevel converters [E1]-[E5], listed as follows:

A) diode-clamped multilevel converter

B) flying-capacitor multilevel converter

C) P2 multilevel converter

D) cascaded multilevel converters (CMC) with separated DC sources

Among these topologies, the CMC toplogy has recently become very popular in high-power AC supplies and adjustable-speed drive applications due to its modularity and flexibility. A single-phase, *m*-level configuration of the CMC is shown in Figure 1-4.

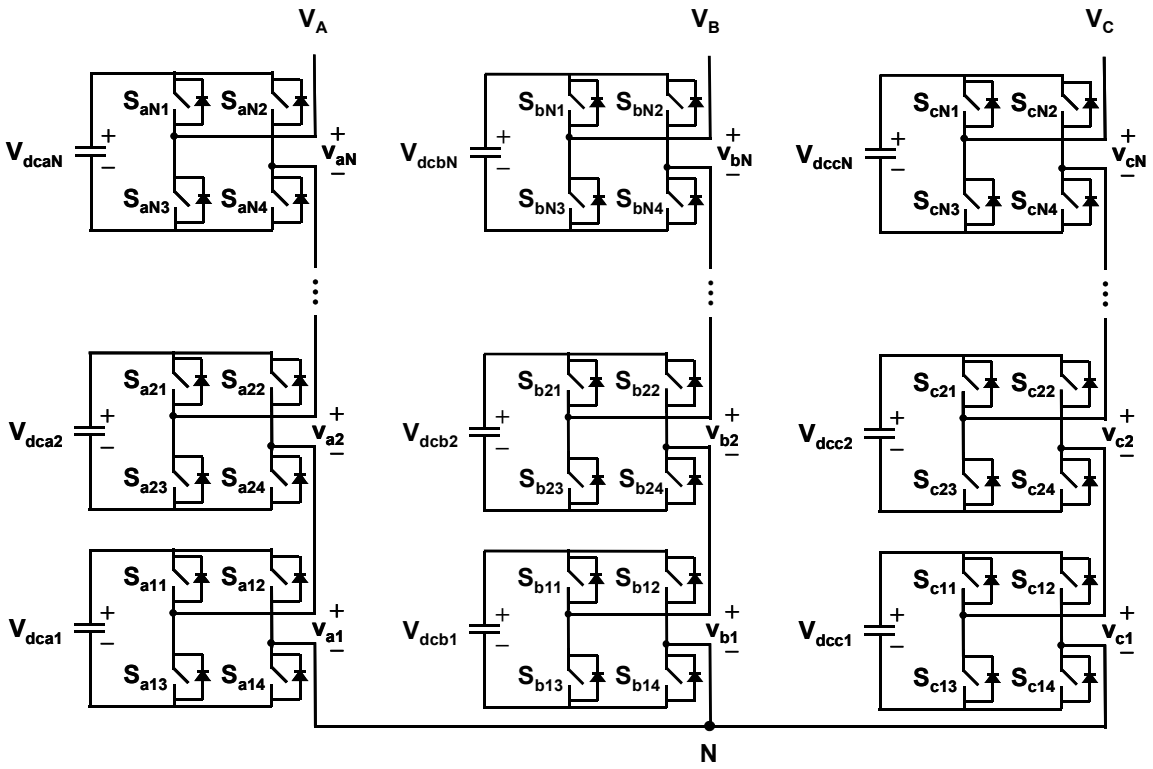


Figure 1-4. A general three-phase wye-configuration CMC.

From a system point of view, a modular multilevel converter is preferable in high-power FACTS applications since the modularity not only simplifies the manufacturing and packaging of hardware, thereby reducing the system costs and improving the system reliability, but also makes the entire system scalable in terms of power capability and common coupling voltage levels. Therefore, a CMC system at a suitable voltage level can be directly connected to a AC grid without transoformer coupling.

Particularly, compared to its major counterparts, such as the diode-clamped multilevel converter and flying capacitor multilevel converter, the CMC, which is composed of many

identical full-bridge VSCs, not only has a unique modular feature, but also has no clamping diodes or flying capacitors and, hence, needs fewer main power components to achieve the same power capability [E1][E3].

For the harmonics, the CMC synthesizes its output near sinusoidal voltage waveforms by combining the output voltages of the modular H-bridge VSC at each phase. With a sufficiently high number of voltage levels, a premium-quality output waveform with fast system response can be achieved by switching the main power semiconductor devices only at the line frequency. This naturally minimizes the entire system losses and the output filter requirement. In addition, by adding more H-bridge VSCs, not only the amount of VAR can simply increase without redesigning the power stage, but also the built-in redundancy and improved reliability against individual H-bridge converter failure can be more easily realized compared to other topologies.

Moreover, a three-phase CMC topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offer the potential for AC system phase-balancing. And the separate DC buses allow the viable energy storage units without ultra high voltage rating to be integrated with VSC for high power ESS application. These two features are impossible in other VSC topologies utilizing a common DC link.

VII. Control Technology

As a matter of fact, how to design a reliable and stable STATCOM/ESS system and effectively control STATCOM/ESS to achieve the system application objective is very complicated. The conventional STATCOM control design was intricate without a good

understanding of controlled plant and well-defined system transfer functions. The control compensators were therefore randomly selected. The stability of the system was achieved by trial and error processes, which were time-consuming and ineffective.

In the literature, there are two typical STATCOM control schemes: 1) Indirect control method is to control the reactive output current indirectly by controlling the DC capacitor voltage via controlling the angle of converter output voltage; 2) Direct control method is to keep the DC voltages constant and control the reactive output current directly by controlling the converter output voltage through PWM. With emerging fast switching semiconductor devices, multilevel converter topologies and variant PWM technologies, the direct control method has been widely applied and it is also the focused control method in this dissertation.

Recently, a 1st order transfer function of a CMC-based STATCOM including decoupling control items and neglecting the DC-side dynamics is proposed by Dr. F.Z. Peng, etc., and utilized for the STATCOM interal current control design [E2][E8][E9]. And furthermore, a generalized 2nd order transfer function of a CMC-based STATCOM including the cross-coupling effects but neglecting DC-side dynamics is derived for the internal current loop control design by Dr. Siriroj, etc., and a current-to-DC-voltages transfer function is also derived for the STATCOM DC voltage loop control design [E3][E4]. Whether the assumption to neglect the DC-side dynamics has any limitation or causes any problem has not yet been studied in a literature.

Regarding the external control of STATCOM to deal with the specific system applications, since the conventional STATCOMs mainly deal with steady-state voltage regulation like the functions of cap bank, their external control is based on the steady-state voltage regulation,

where its control parameters are tuned through trial-and-error and its structure has been designed and demonstrated [A1]. With the recent innovation in power semiconductor devices and converter technology, the state-of-the-art STATCOMs have a wide system application range and can deal with the emerging and challenging system issues, such as renewable wind power support and arc furnace flicker mitigation, which need numerous research to develop the model and control for such system applications.

A renewable large wind farm, as a fast growing power generation method, has its inherent power quality and stability issues. There is also a growing literature addressing the problem analysis and solution study [H2][H3][H4][H5][H6][H7][H8]. At present, how to develop the effective and accurate model of a wind power system and how to design the control of STATCOM for wind power support are posing challenges to researchers.

On the other side, hitherto, there is no straightforward method mentioned in the literature to model EAF and utilze the model to develop the compensator to assure that the EAF and STATCOM combined system operates in a stable and effective operating range.

Conventionally, an open-loop sensing-then-compensation method (current direct feedback control) is used for flicker mitigation, which means that the load current (or its fluctuation/harmonics components) is sensed and directly feedbacked as the command/reference of the compensator, as the compensator device follows the command for compensation [C3]. The compensator device with its internal control tries to maintain its own stability and generate the response following the command. But for an overall EAF-Compensator-grid system, there is no external control to ensure the stability of a whole system and adaptively compensate the flicker

following the predefined flicker command. Therefore, the system stability and performance verification need numerous time-domain simulation case studies.

1.2 Motivation

The successful development and demonstration of a STATCOM/ESS for typical, emerging and chanlleging system applications with integrating advanced semiconductor device technology, VSC technology and control technology will result in the significant cost reduction, reliability improvement, flexibility and modularity, and an increased application of power electronics–based controllers.

A STATCOM and ultracapacitor energy storage system (UESS), based on ETO technology at the device level, modular VSC-based CMC and its control technology as a converter system, and UCAP as the energy storage, is a state-of-the-art FACTS/ESS for utility high power applications from power quality enhancement, voltage and frequency stabilization, and power transfer limit improvements, to renewable energy and distributed generation support. It is expected that integrating the STATCOM/UESS technology in flexible AC transmission systems (FACTS) will result in an FACTS/ESS that is capable of extremely fast response and that is less costly per kW/kVA than any other FACTS/ESS based on traditional storage/power electronics technologies.

With the above as motivation, this dissertation focuses on cost-effectively integrating these emerging technologies as an STATCOM/UESS system for typical, emerging and challenging system applications, and developing a reliable, stable and effective model and controller to utilize such an STATCOM/UESS concept for the specific system enhancement objectives.

1.3 Dissertation Outline

The goal of this dissertation is to achieve high-performance, reliable, flexible, cost-effective controllers of the CMC-based STATCOM/UESS for specific challenging utility applications. Major contributions proposed in this dissertation include:

1) CMC-based STATCOM model analysis and compensator design guideline;

2) an untunable close-loop AC side energization and de-energization method of CMC-based STATCOM;

3) an effective per-phase DC-bus voltage balancing scheme based on derived voltage-loop transfer functions and so-called imaginary ABC-DQ0 Park Transformation;

4) analysis, modeling and control of STATCOM for voltage fluctuation suppression in a large wind power system;

5) field data-based STATCOM study for flicker mitigation and model-based STATCOM compensator design for EAF flicker mitigation;

6) modeling, integration and control of UESS comprising UCAPs and modular VSCs.

All developed models and control strategies above are validated with the experimental results based on a scaled-down transient network analyzer (TNA) system or a full-scale high power prototype or field-recorded data. Based on the sequence of the contributions above, this dissertation is divided into five chapters.

Chapter 2 presents a comphensive CMC-based STATCOM control methodology. The modeling and control works that were done by previous researchers are reviewed. Based on the generalized models of CMC-based STATCOM in DQ0 coordinates, the full-order frequency domain transfer function of CMC-based STATCOM is derived. The derived full-order transfer functions are compared with the simplfied transfer functions in the literature, and the relationship among them is analyzed, and the generalized and straightforward guideline for STATCOM control and compensator design is given.

Based on the analysis of the derived control-to-current transfer functions, a DQ frame-based control method of AC-side close-loop direct energization and de-energization of a CMC-based STATCOM, which is conducted by loop-gain shaping method without tuning compensator parameters and can flexibly control the speed of energization and de-energization, is presented.

To deal with unbalanced DC voltages at each phase, a pre-phase balancing scheme is proposed. The DC voltage-loop transfer funcation is derived. Based on the derived transfer functions, the balancing control loops are designed with desired bandwidth, phase margin and gain margin. Through an imaginary DQ0/ABC transformation method, the individual DQ coordinate-based balancing control loops are allowed to be converted to each phase for per-phase balancing control. At the end of chapter 2, the design and experimental demonstration of a 4.5 MVA ETO and CMC-based STATCOM with the proposed control method is presented.

Chapter 3 presents the study of a STATCOM in facilitating the integration of a large WF into a weak power system. First, an actual weak power system with two nearby large WFs is introduced. Based on the field SCADA data analysis, the issues are highlighted and steady-state and dynamic voltage controls are needed to solve these issues. A STATCOM is proposed for

dynamic voltage control, particularly to suppress the short-term (seconds to minutes) voltage fluctuations. Secondly, a model of the system, WF and STATCOM for steady-state and dynamic impact study is developed in the PSCAD/ETMDC simulation environment. The developed model is validated by using the field data. Moreover, based on the PV and VQ curves obtained from the simulation, the system voltage control and stability issues are analyzed, and the size and location of STATCOM are assessed. Finally, a STATCOM control strategy for voltage fluctuation suppression is presented, and the dynamic simulations are used to verify the performance of the proposed STATCOM and its control strategy.

Chapter 4 presents the study of a CMC-based STATCOM for flicker mitigation. First, as the specific case, a CMC-based STATCOM is proposed to evaluate the performance of the EAF flicker mitigation for a practical 40 MVA arc furnace in Tennessee. A steady-state analysis is conducted to assess the size of STATCOM. Based on the field data recorded at the electric system surrounding EAF, the flicker issue and reactive power compensation requirements are quantitatively analyzed. All possible compensation solutions, including passive filter, SVC, STATCOM are discussed. The extensive simulations based on the field data are conducted to study the system performance and cost-effectiveness for flicker mitigation, which verifies the steady-state study and gives the guideline for STATCOM sizing and performance estimation.

Furthermore, other than the EAF model for the purpose of a harmonics analysis, an EAF worst-case model is proposed so that the deterministic impedance of EAF at specific operating points can be evaluated. Combining the average model of EAF and STATCOM, the small-signal transfer function of voltage loop for PCC (point of common coupling) is derived. By utilizing the

control bandwidth of the STATCOM internal control loop, the external voltage loop of STATCOM for flicker mitigation is designed.

Chapter 5 begins with an electrical model of UCAP through the measurement of single UCAP cells and a full-scale UCAP string. Considering the features of UCAPs, the potential issues related to UCAP ESR (equivalent series resistor) is pointed out, and an effective and simple interface to integrate the UCAP and modular VSC is proposed, so that the high frequency effect on UCAP is bypassed and the transformation between STATCOM and UESS is easy. Finally, with the proposed interface and toplogy, the UESS real power and reactive power independent control scheme is proposed, designed and validated.

Chapter 6 draws the conclusion for this dissertation and proposes future work.

Chapter 2 IMPROVED MODELING AND CONTROL OF CASCADED MULTILEVEL CONVERTER-BASED STATCOM

This chapter presents the modeling and control of a CMC-based STATCOM. Full-order transfer functions of a CMC-based STATCOM is derived and compared to previous reduced-order transfer functions, and a general transfer functions-based control design guideline is obtained. Through the further analysis of transfer functions, an AC-side engization and de-energization control method is presented. Using the derived control-to-DC voltages transfer function and imaginary Park Transformation concept, a per-phase DC volatage scheme is presented. Finally, based on the developed method, a 4.5MVA CMC-based STATCOM is experimentally demonstrated.

2.1 Review on Modeling and Control of CMC-based STATCOM

A generalized wye-connection CMC-based STATCOM with N modular H-bridge VSCs at each phase is shown in Figure 2-1. A multilevel-cascaded converter consists of a number of identical H-bridge converters, whose output terminals are connected in series. The output voltage is thus the summation of those H-bridge converters, i.e.,

$$V_{kn} = V_{k1} + V_{k2} + \cdots + V_{kN},$$

Equation 2-1

where k is the phase notation, i.e., a, b or c, and

N is the number of H-bridge converters per phase.

Since three output voltage levels can be synthesized by an H-bridge converter, the total number of output-phase voltage levels equals 2*N*+1. The maximum number of line-to-line voltage levels is 4*N*+1.

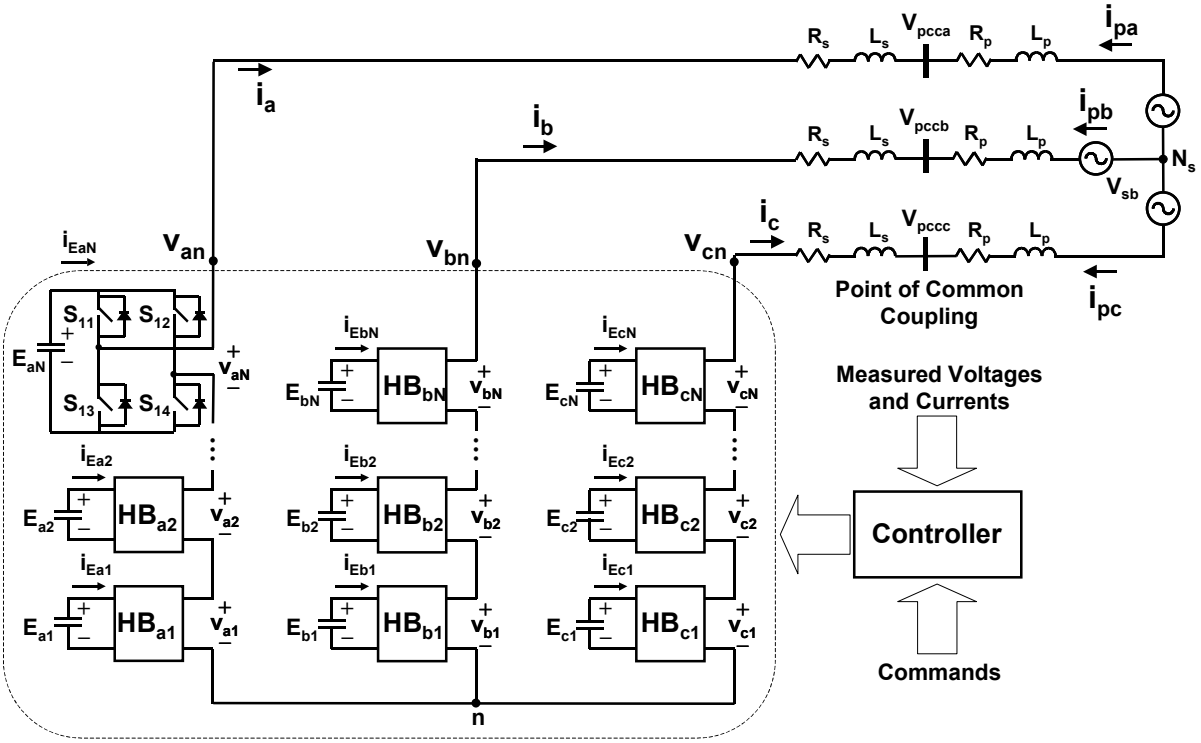


Figure 2-1. Schematic of a cascaded-multilevel converter-based STATCOM system.

Through the modeling development procedures from a switching model to an average model for a CMC-based STATCOM [E3][G1], shown in Figure 2-2, a time-invariant average model in dq0 frame with its open-loop transfer functions may be obtained. First, a general average model in ABC coordinates for the CMC-based STATCOM, shown in Figure 2-1, can be realized, as shown in Figure 2-3.

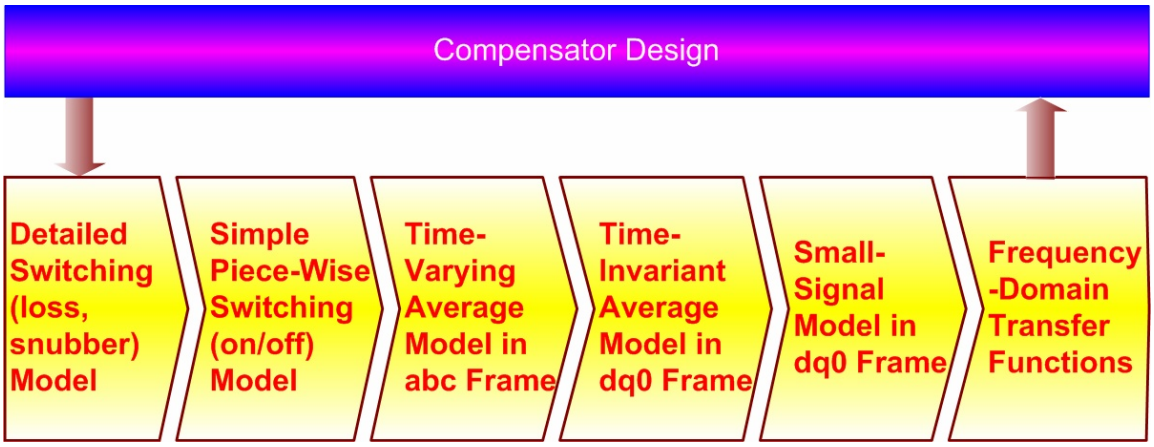


Figure 2-2. Average model of the cascaded-multilevel converter-based STATCOM in the ABC frame.

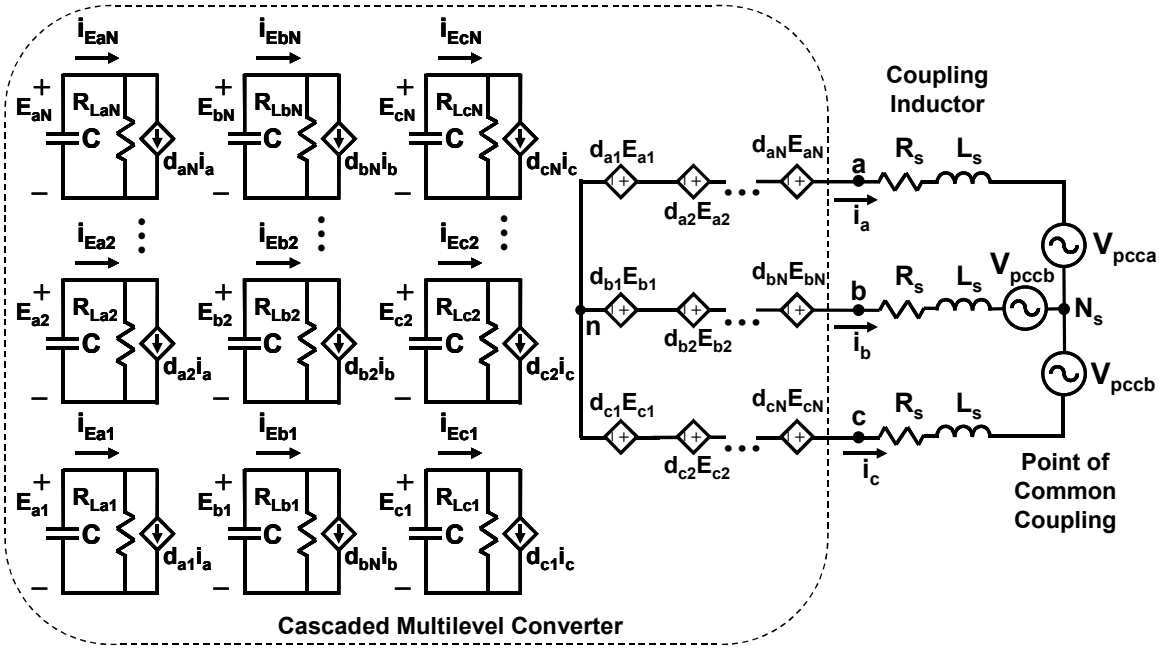


Figure 2-3. Average model of the cascaded-multilevel converter-based STATCOM in the ABC frame.

To simplify the model, the following three assumptions are made:

1) Based on a meaningful AC output control, all DC voltage sources are assumed to be equally regulated, i.e.,

$$E_j = E_{aj} = E_{bj} = E_{cj} \text{ , for } j = 1 \ldots N \text{ , and}$$

$$E = E_1 = E_2 = \cdots = E_N \text{ .}$$

2) The losses for each H-bridge converter in the same level are assumed to be identical, as follows:

$$R_{Lj} = R_{Laj} = R_{Lbj} = R_{Lcj} \text{ , for } j = 1 \ldots N \text{ .}$$

3) Due to equal synthesized output voltages, all duty cycles in the same phase are assumed to be identical, i.e.,

$$d_k = d_{k1} = d_{k2} = \cdots = d_{kN} \text{ , for } k = a, b, c \text{ .}$$

Based on these three assumptions, the average model in ABC coordinates shown in Figure 2-3 can be simplified as shown in Figure 2-4.

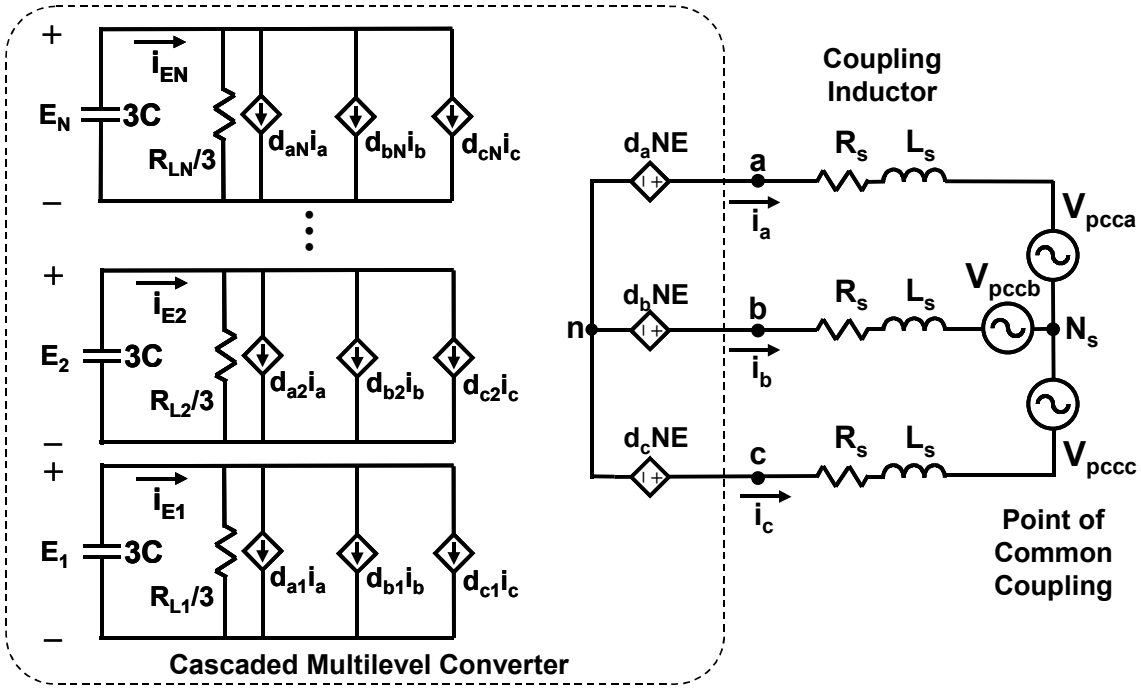


Figure 2-4. A simplified average model for the cascaded-multilevel converter-based STATCOM in the ABC frame.

By applying the Park's Transformation for the differential equations based on the average model in the ABC frame, the average model in the DQ0 frame can be derived. In this dissertation, the preferred Park's Transformation matrix is

$$\vec{T}_{dq0/abc} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\theta) & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta-\frac{2\pi}{3}) & -\sin(\theta+\frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix},$$

Equation 2-2

where ..... $\theta = \int_0^t \omega(\tau)d\tau + \theta(0)$, and $\omega(\tau)$ is the angular velocity.

Thus, a simplified average model for the CMC-based STATCOM in DQ0 coordinates can be obtained, as shown in Figure 2-5. Erasing the DC steady-state value of operating point and higher order small-signal items, the average model can be transferred into its small-signal model, as depicted in Figure 2-6.

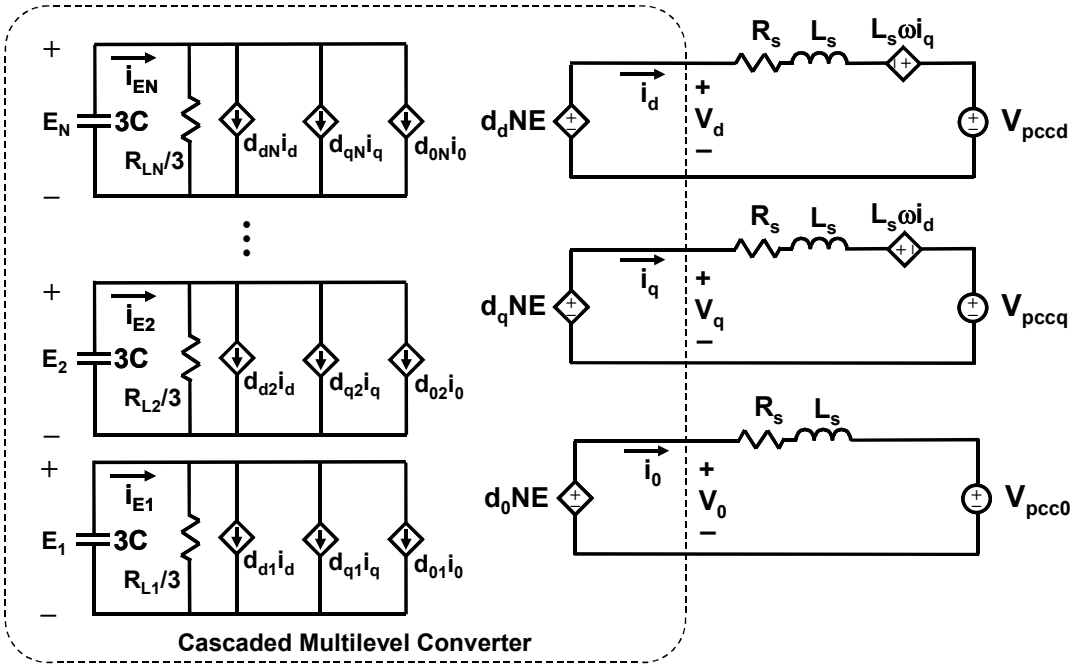


Figure 2-5. Simplified average model for the cascaded-multilevel converter-based STATCOM in DQ0 coordinates.

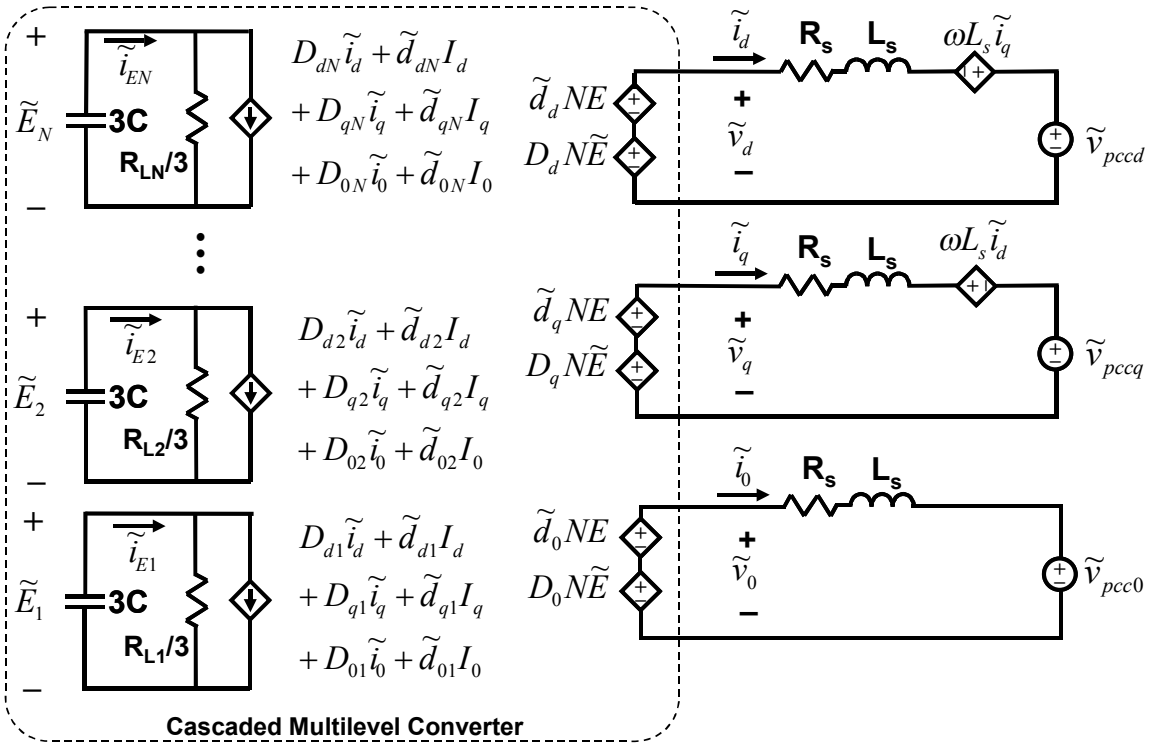


Figure 2-6. Small-signal model for the cascaded-multilevel converter-based STATCOM in DQ0 coordinates.

Based on the derived small-signal model, the following key open-loop transfer functions of the STATCOM system are derived and listed as follows.

1. Control-to-Output-Current Transfer Function:

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d}, \text{ and } G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_q}.$$

Equation 2-3

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d} = \frac{NE(R_s + L_s S)}{L_s{}^2 S^2 + 2L_s R_s S + (R_s{}^2 + \omega^2 L_s{}^2)}.$$

Equation 2-4

Equation 2-4 can also be expressed as a standard second-order transfer function, as follows:

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d} = \frac{K_{idd}(\frac{S}{\omega_Z} + 1)}{\left(\frac{S}{\omega_P}\right)^2 + \frac{S}{Q\omega_P} + 1},$$

Equation 2-5

where

$$K_{idd} = \frac{NER_s}{R_s{}^2 + (\omega L_s)^2}, \qquad Q = \frac{\sqrt{R_s{}^2 + (\omega L_s)^2}}{2R_s},$$

$$\omega_P = \frac{\sqrt{R_s{}^2 + (\omega L_s)^2}}{L_s}, \qquad \textbf{and } \omega_z = \frac{R_s}{L_s}.$$

And G_{iqq} is the exactly same as G_{idd}.

2. Control-to-Cross-Coupling-Output-Current Transfer Function:

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d}, \textbf{ and } G_{idq} = \frac{\tilde{i}_d}{\tilde{d}_q}.$$

Equation 2-6

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d} = \frac{-NE\omega L_s}{L_s{}^2 S^2 + 2L_s R_s S + (R_s{}^2 + \omega^2 L_s{}^2)}, \text{ or}$$

Equation 2-7

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d} = \frac{K_{iqd}}{\left(\frac{S}{\omega_P}\right)^2 + \frac{S}{Q\omega_P} + 1},$$

Equation 2-8

where

$$K_{iqd} = \frac{-\omega LNE}{R_s{}^2 + (\omega L_s)^2}, \qquad Q = \frac{\sqrt{R_s{}^2 + (\omega L_s)^2}}{2R_s},$$

$$\omega_P = \frac{\sqrt{R_s{}^2 + (\omega L_s)^2}}{L_s}, \qquad \text{and } \omega_z = \frac{R_s}{L_s}.$$

Likewise, the transfer function G_{idq} is the same as G_{iqd}.

3. Output-Current-to-DC-Bus-Voltage Transfer Function:

$$G_{Eid} = \frac{\tilde{E}_j}{\tilde{i}_d},\ j = 1 \ldots N,$$

Equation 2-9

where N is the number of H-bridge converters per phase.

$$G_{E\,idj} = \frac{\tilde{E}_j}{\tilde{i}_d} = -\left[\frac{D_{dj}L_sS + (D_{qj}\omega L_s + D_{dj}R_s)}{3CL_sS^2 + 3CR_sS + D_{dj}D_{qj}N}\right], \text{ or}$$

Equation 2-10

$$G_{Eidj} = \frac{\tilde{E}_j}{\tilde{i}_d} = \frac{K_{Eid}(\frac{S}{\omega_Z}+1)}{\left(\frac{S}{\omega_P}\right)^2 + \frac{S}{Q\omega_P}+1},$$

Equation 2-11

where

$$K_{Eidj} = \frac{D_{qj}\omega L_s + D_{dj}R_s}{D_{dj}D_{qj}N},$$

$$Q = \sqrt{\frac{D_{dj}D_{qj}NL_s}{3CR_s{}^2}},$$

$$\omega_P = \sqrt{\frac{D_{dj}D_{qj}N}{3CL_s}},$$

$$\text{and } \omega_z = \frac{D_{qj}\omega}{D_{dj}} + \frac{R_s}{L_s}.$$

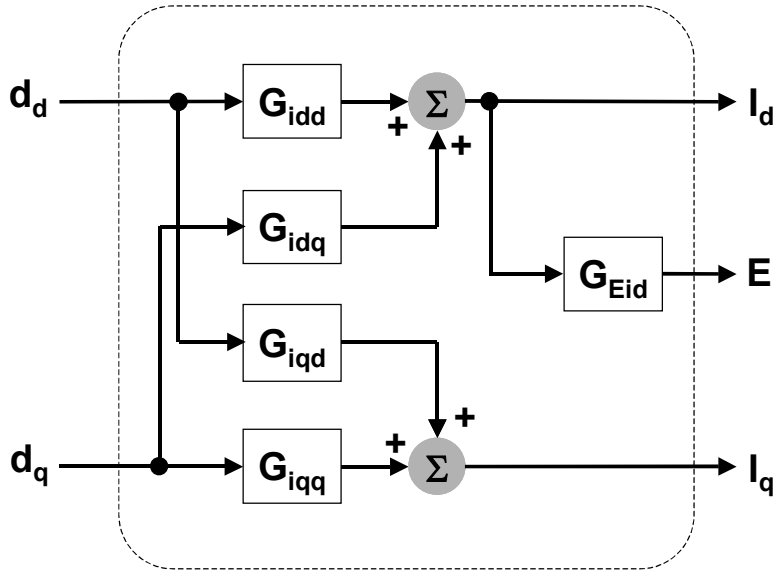


Figure 2-7. Open-loop transfer functions.

Figure 2-7 illustrates the block diagram of the open-loop transfer functions of the CMC-based STATCOM. Based on these transfer functions, the loop-gain shape-based control technique is applied and the main control block diagram is designed, as shown in Figure 2-8.

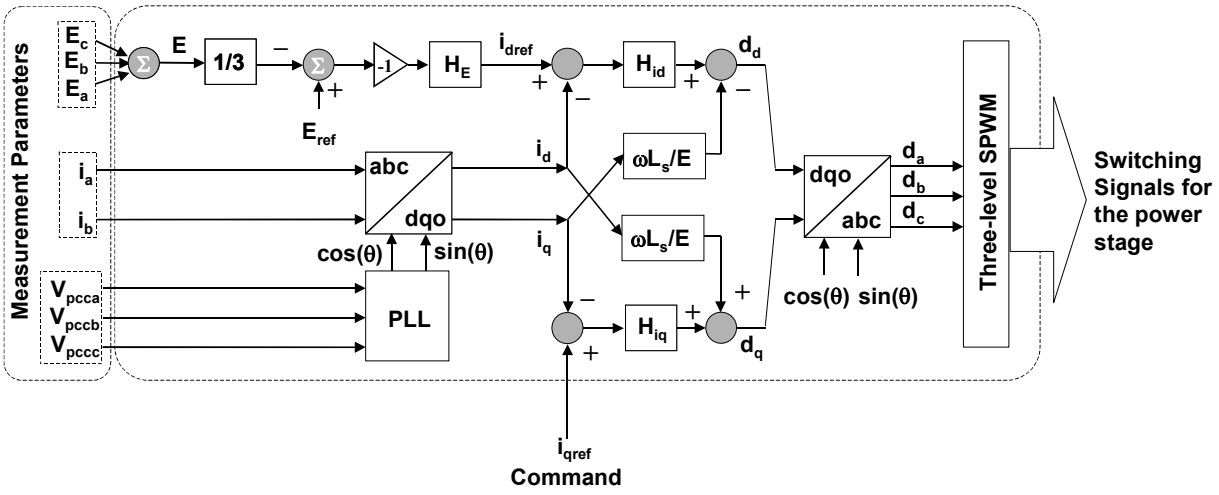


Figure 2-8. Completed control block diagram of the CMC-based STATCOM.

For the more detailed derivation of the model and transfer functions, they can be referred to [E3][G1][G2][G3].

2.2 Transfer Functions Analysis of CMC-based STATCOM

Actually, as you can see, the transfer functions in 2.1 are based on the assumption that the DC-side dynamics or Vdc perturbation does not affect the DQ current dynamics at the AC-side, and hence, these transfer functions are in a reduced-order format with two orders derived from AC-side inductors, but without the 3rd order from the DC-side capacitor. Whether the assumption has any limitation or causes any problem has not yet been studied in the literature and will be presented in this section.

Based on the average model in Figure 2-5, when including the Edc perturbnation and the ESR of DC capacitor and shunt equivalent Rloss, the DC-side admittance and AC-side impedance can be represented as:

$$Ydc = \frac{3\cdot\left[1 + \left(R_C + Rloss\right)\cdot C\cdot S\right]}{Rloss\cdot\left(1 + R_C\cdot C\cdot S\right)}$$

$$Zac = (R + S\cdot L)$$

Equation 2-12

Therefore, the full-order TFs (Transfer Functions) of CMC-based STATCOM are derived as:

Given

$$ddd\cdot N\cdot E + D_d\cdot N\cdot dE + L\cdot\omega\cdot diq - (Zac)\cdot did = 0$$

$$D_q\cdot N\cdot dE - L\cdot\omega\cdot did - (Zac)\cdot diq = 0$$

$$Ydc\cdot dE + ddd\cdot Id + D_d\cdot did + D_q\cdot diq = 0$$

$$Find(did, diq, dE) \rightarrow \begin{bmatrix} N\cdot ddd\cdot\dfrac{-L\cdot\omega\cdot D_q\cdot Id - D_d\cdot Id\cdot Zac + N\cdot E\cdot D_q^{\,2} + E\cdot Ydc\cdot Zac}{L^2\cdot\omega^2\cdot Ydc + D_d^{\,2}\cdot N\cdot Zac + Zac\cdot D_q^{\,2}\cdot N + Zac^2\cdot Ydc} \\ -\left(L\cdot\omega\cdot E\cdot Ydc + D_q\cdot Id\cdot Zac + D_q\cdot D_d\cdot E\cdot N - D_d\cdot L\cdot\omega\cdot Id\right)\cdot N\cdot\dfrac{ddd}{L^2\cdot\omega^2\cdot Ydc + D_d^{\,2}\cdot N\cdot Zac + Zac\cdot D_q^{\,2}\cdot N + Zac^2\cdot Ydc} \\ ddd\cdot\dfrac{-Id\cdot L^2\cdot\omega^2 - Id\cdot Zac^2 - D_d\cdot N\cdot E\cdot Zac + L\cdot\omega\cdot D_q\cdot N\cdot E}{L^2\cdot\omega^2\cdot Ydc + D_d^{\,2}\cdot N\cdot Zac + Zac\cdot D_q^{\,2}\cdot N + Zac^2\cdot Ydc} \end{bmatrix}$$

Equation 2-13

Replacing the Ydc and Zac, the current-loop transfer function can be represented as:

$$G_{idd}(S, Rloss) := N \cdot \frac{-L \cdot \omega \cdot D_q \cdot Id - D_d \cdot Id \cdot (R + S \cdot L) + N \cdot E \cdot D_q^{\,2} + E \cdot \frac{3 \cdot \left[1 + \left(R_C + Rloss\right) \cdot C \cdot S\right]}{Rloss \cdot \left(1 + R_C \cdot C \cdot S\right)} \cdot (R + S \cdot L)}{L^2 \cdot \omega^2 \cdot \frac{3 \cdot \left[1 + \left(R_C + Rloss\right) \cdot C \cdot S\right]}{Rloss \cdot \left(1 + R_C \cdot C \cdot S\right)} + D_d^{\,2} \cdot N \cdot (R + S \cdot L) + (R + S \cdot L) \cdot D_q^{\,2} \cdot N + (R + S \cdot L)^2 \cdot \frac{3 \cdot \left[1 + \left(R_C + Rloss\right) \cdot C \cdot S\right]}{Rloss \cdot \left(1 + R_C \cdot C \cdot S\right)}} \cdot \tau(S)$$

Equation 2-14

Seen from the equation, the control-to-current full-order TF with considering Edc perturbnation is in a sophisticated 3rd-order format including square items of Dd^2 and Dq^2 and having two zeroes and three poles, where two of them derive from AC-side inductors and the 3rd one derives from DC-side capacitor. Figure 2-9 show a typical bode plot of full-order control-to-current transfer functions.

What is the relationship between full-order TFs and reduced-order TF in 2.1? Simply saying, the reduced-order TF is based on neglegible DC perturbation, which means the DC-link is an ideal source or the DC capacitor is infinite large. With this assumption, the following equations can be derived as:

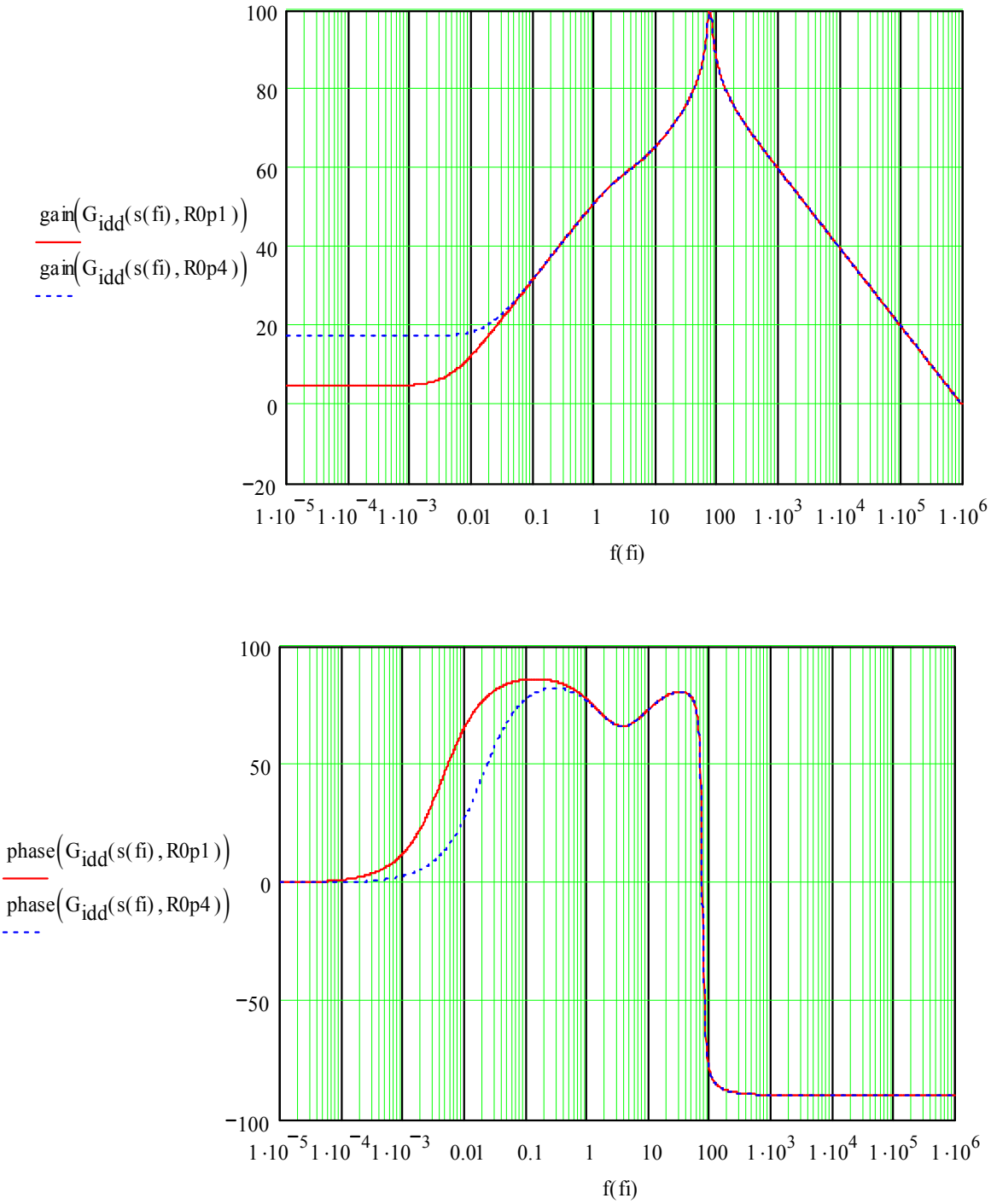


Figure 2-9. Bode plot of full-order control-to-current transfer function

when neglecting the DC and AC side's coupling and assume constant for current-loop TF, e.t. C=inf and Ydc=inf, and then TF becomes

$$\Rightarrow \quad \frac{did}{ddd} = N \cdot \frac{-L \cdot \omega \cdot D_q \cdot Id - D_d \cdot Id \cdot Zac + N \cdot E \cdot D_q^{\,2} + E \cdot Ydc \cdot Zac}{L^2 \cdot \omega^2 \cdot Ydc + D_d^{\,2} \cdot N \cdot Zac + Zac \cdot D_q^{\,2} \cdot N + Zac^2 \cdot Ydc}$$

$$\Rightarrow \quad \frac{did}{ddd} = N \cdot \frac{\left(-L \cdot \omega \cdot D_q \cdot Id - D_d \cdot Id \cdot Zac + N \cdot E \cdot D_q^{\,2}\right) + (E \cdot Zac) \cdot Ydc}{\left(D_d^{\,2} \cdot N \cdot Zac + Zac \cdot D_q^{\,2} \cdot N\right) + \left(L^2 \cdot \omega^2 + Zac^2\right) \cdot Ydc}$$

$$\Rightarrow \quad \frac{did}{ddd} = N \cdot \frac{0 + (E \cdot Zac) \cdot Ydc}{(0) + \left(L^2 \cdot \omega^2 + Zac^2\right) \cdot Ydc}$$

$$\Rightarrow \quad \frac{did}{ddd} = N \cdot \frac{E \cdot Zac}{L^2 \cdot \omega^2 + Zac^2} \quad \Rightarrow \quad \frac{did}{ddd} = \frac{N \cdot E \cdot (L \cdot S + R) \cdot \tau(S)}{L^2 \cdot S^2 + 2 \cdot L \cdot R \cdot S + R^2 + \omega^2 \cdot L^2}$$

which means giving this assumption to the full-order TF, the full-order TFs are exactly transferred into the reduced-order TF format. In the Figure 2-10, the bode plot of full-order and reduced-TF and loop-gain with the same design controller are drawn together for comparison. Seen from the plot, the reduced-order TF has a good match on full-order TF beyond the double-pole frequency for both the gain and phase, and has a large mismatch on full-order TF for a frequency much smaller than the double-pole frequency. Therefore, as long as the designed crossover frequency is higher than the double-pole frequency, the reduced-order TF can be used for close-loop control design and have the almost same bandwidth, phase margin and gain margin as using the full-order TF for a close-loop control design; otherwise, a full-order TF has to be used for design.

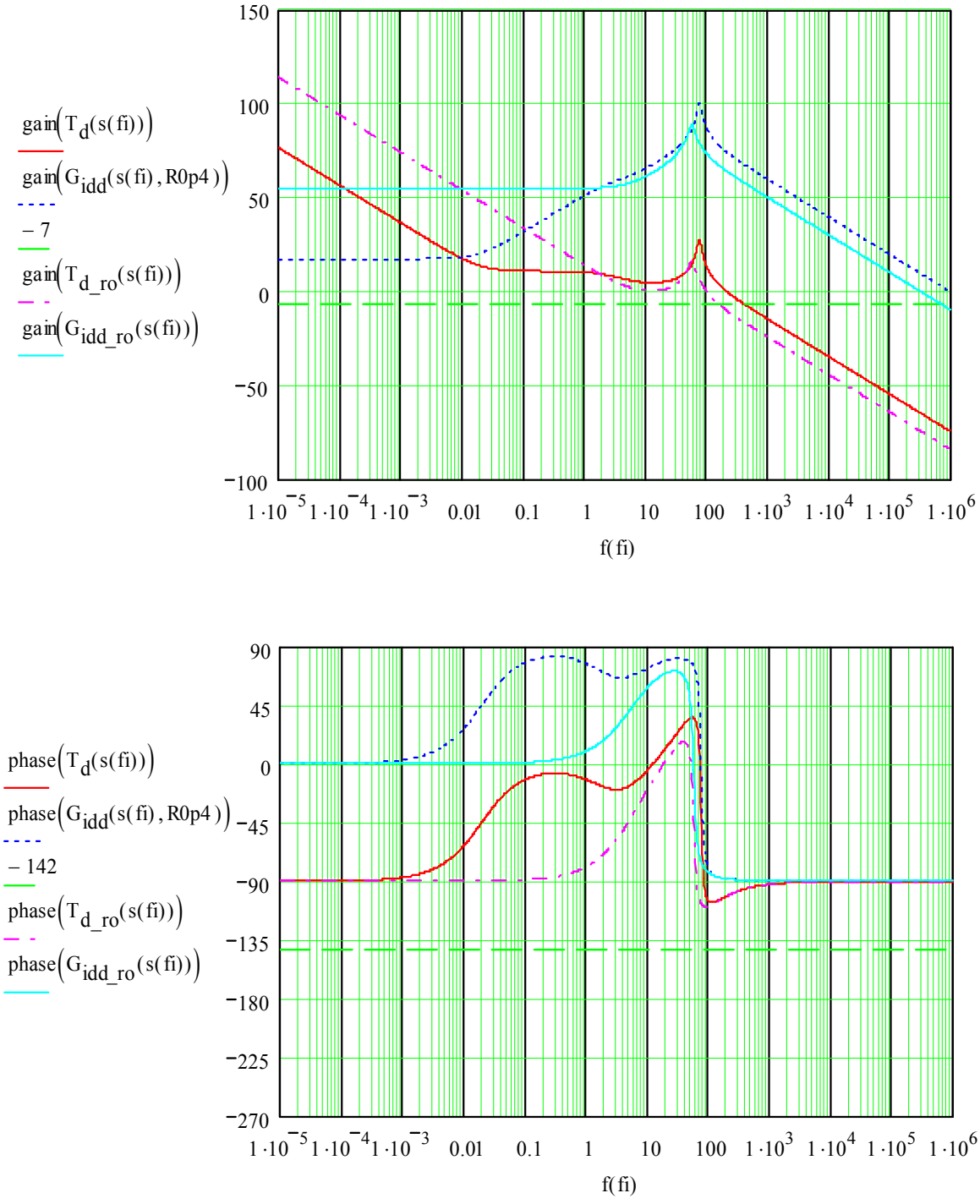


Figure 2-10. Bode plot comparison of full-order and 2nd reduced-order control-to-current transfer functions.

Actually, the 2nd-order TF can be further simplified to a 1st-order TF below, as long as the decoupling duty cycle control items $\pm\omega L_s/E$ shown in Figure 2-8 are included to cancel the coupling items $\pm\omega L_s I_{dq}$ in the STATCOM model shown in Figure 2-5.

$$G_{idd}(S) = \frac{NE(R_s + L_s S)}{L_s{}^2 S^2 + 2L_s R_s S + (R_s{}^2 + \omega^2 L_s{}^2)} \Rightarrow G_{idd}(S) = \frac{NE(R_s + L_s S)}{L_s{}^2 S^2 + 2L_s R_s S + R_s{}^2} \Rightarrow G_{idd}(S) = \frac{NE}{R_s + L_s S}$$

Equation 2-15

Because the cross-coupling effect is eliminated with the applied de-coupled items, the 1st-order TF, plotted in Figure 2-11, matches the 2nd-order TF very well beyond the double pole frequency, and has a large mismatch on the 2nd-order TF for the frequency lower than the double pole frequency, which means the 1st reduced-order TF can be used for the close-loop control design as long as the designed bandwidth is higher than the double pole frequency and the decoupled items are included in the controller.

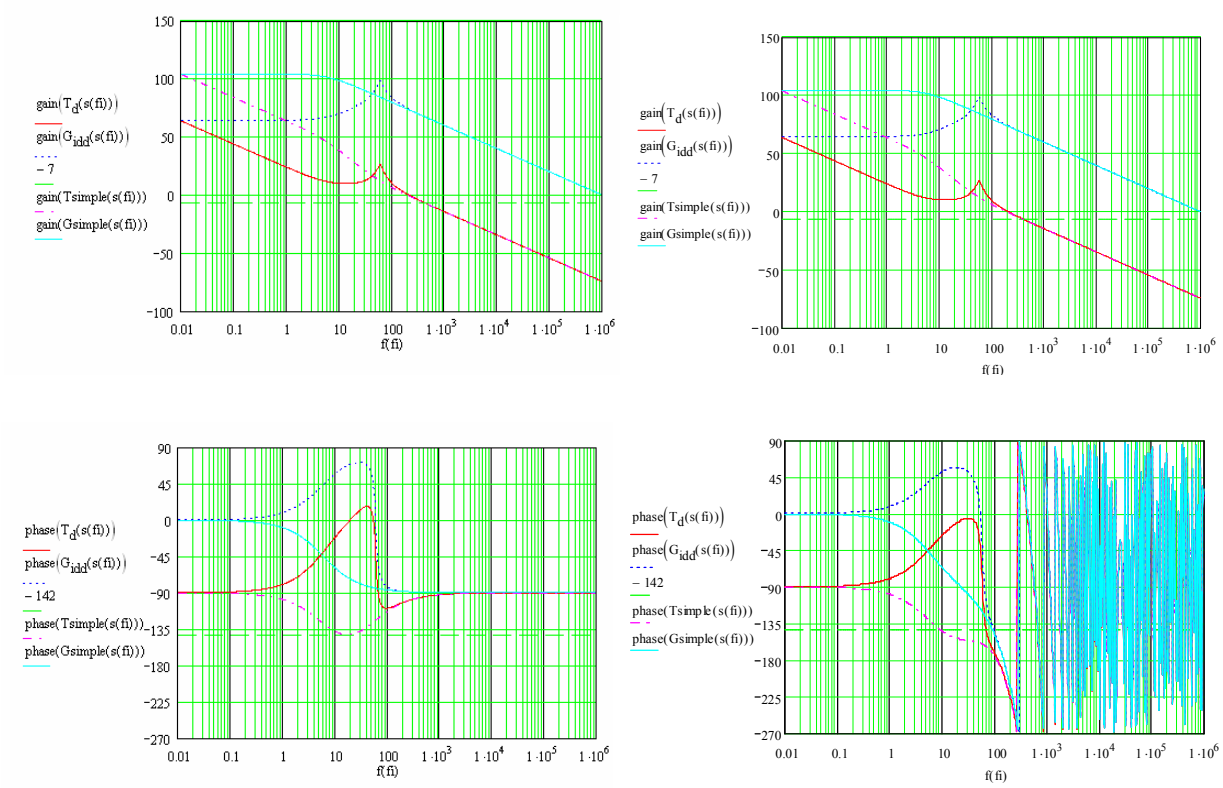


Figure 2-11. 1st and 2nd reduced-order control-to-current bode plot: (a) without delay (b) with delay

Moreover, there are two more interesting things about zero and pole value of the STATCOM TFs. As we can see, the zero of 2nd reduced-order TF is only determined by the AC-side X/R ratio of the STATCOM. For example, when X/R=10, $f_{zero} = R/(2\pi L) = 6$ Hz. And the double pole frequency of 2nd reduced-order TF can be considered to be only dependent to the constant fundamental frequency: $f_{double_pole} = \text{sqrt}((R/(2\cdot\pi\cdot L))^2+(f_0)^2) \approx 60\text{Hz}$.

Therefore, based on the derivation, comparison and analysis, a clear and simple design guideline can be summarized as below:

1. The 1st reduced-order TF can be used for close-loop control design as long as the expected bandwidth of the designed stable close-loop system is larger than 60Hz, which is the normal case

2. Otherwise, the 3rd full-order TF has to be used for the close-loop control design to obtain accurate values of designed bandwidth, phase margin and gain margin, which is a rare case, since the bandwidth of STATCOM faster than 60Hz is designed in a typical case.

2.3 Energization and De-energization of CMC-based STATCOM

The DC capacitor energization and deenergization of CMC-based STATCOM are seldom mentioned in the literature. Conventionally, an additional DC-side charge circuit, which is bulky and induces additional cost, is required to charge and discharge the capacitors [E7]. For AC-side charge/discharge, an AC-side open-loop duty cycle control method can be simply used [E3], however, the speed and current of charge/discharge is not convenient to be controlled with this method. In [E6], a direct phase angle control method of VSC Vo is presented but how to design the compensator is not addressed. Here, based on the derived DQ frame-based transfer functions of the STATCOM, a constant power charge/discharge method based on the DQ frame-based controller is proposed so that the compensators' parameters need not be tuned and the speed of enengization and de-enengization can be flexibly controlled.

As we know, with the PLL (phase locked loop) synchronizing to the PCC (point of common coupling) voltage and V_{PCCq}=0, the STATCOM instantaneous real and reactive power can be expressed by dq variables as below:

$$\mathbf{P = V_{PCC}d^{*}I_{d} \text{ and } Q = V_{PCC}d^{*}I_{q}}$$

Equation 2-16

Therefore, for a given Id reference, STATCOM absorbs or withdraws a constant real power whatever the DC bus voltage is. Therefore, as long as a compensator is designed to make sure the current loop maintains enough phase margin and gain margin for whole DC bus voltage charge/discharge range, a constant power energization and deenergization can be realized. However, since Vdc is a component inside the control-to-current transfer functions, the challenging or unknown factor for such a design is whether a different Vdc could cause the system instability and even affect other performance of the STATCOM during charge/discharge.

To clarify the effect of the Vdc change, Figure 2-12 gives a group of designed loop gains with different DC bus voltages, which shows that the designed control bandwidth increases with increasing Vdc from tens Hz to Hundreds Hz, the phase margin keeps higher than 50 degree, and the gain margin is always higher than 7 dB for the whole energization and deenergization. Therefore, with such a design, the system is ensured stable in the whole Vdc variation range.

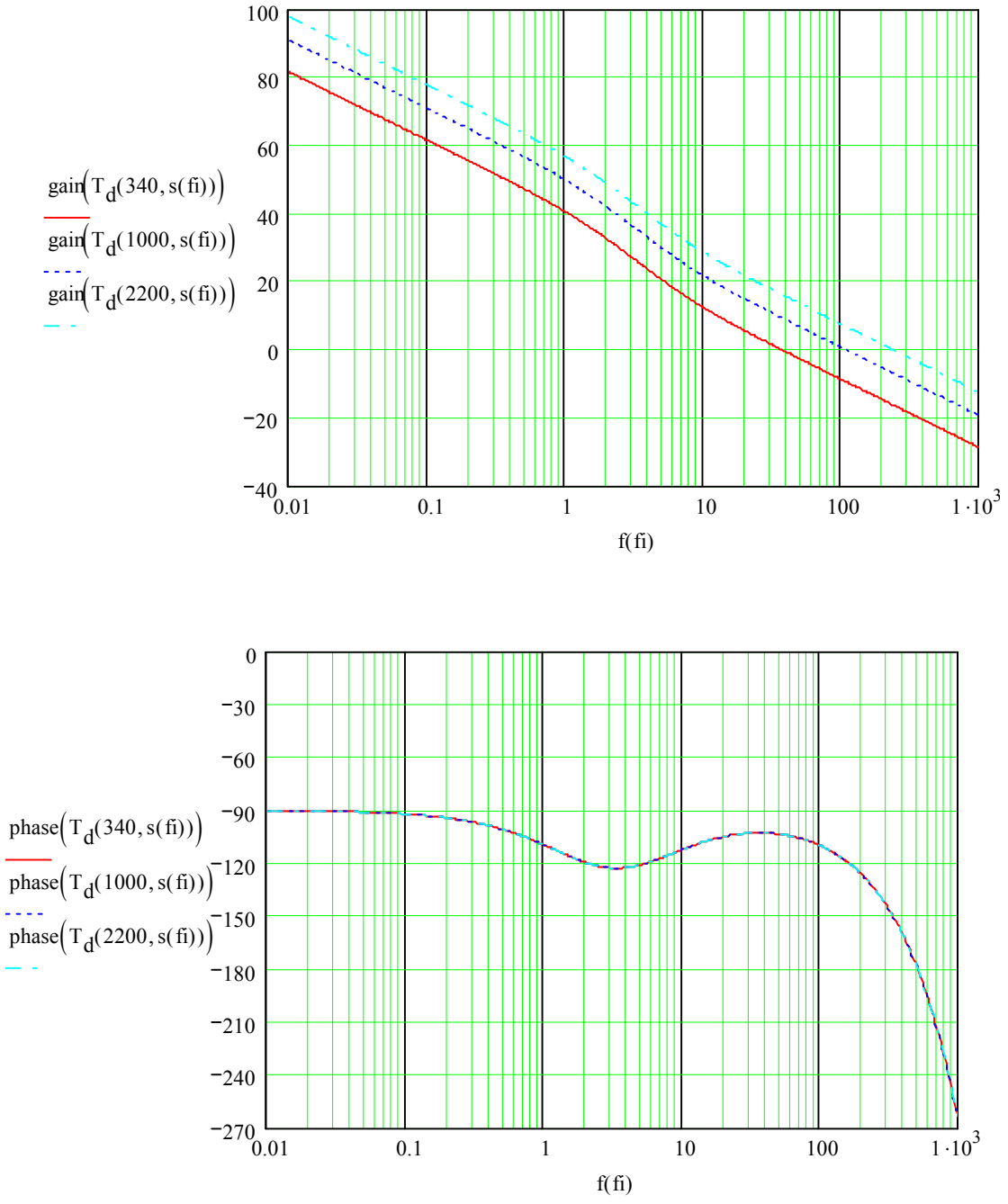
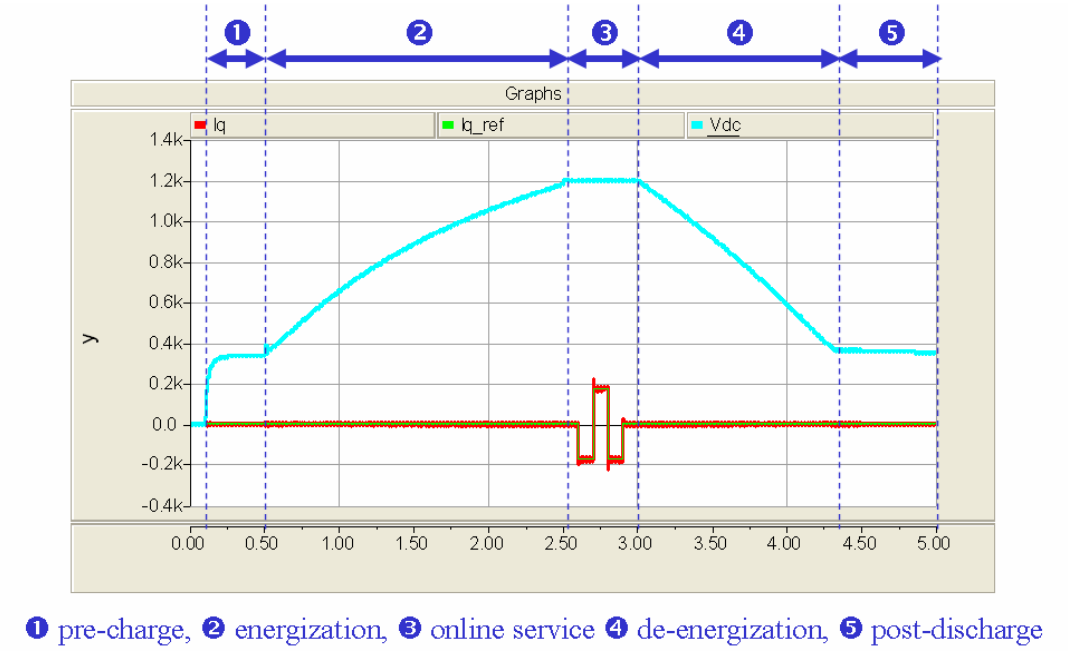
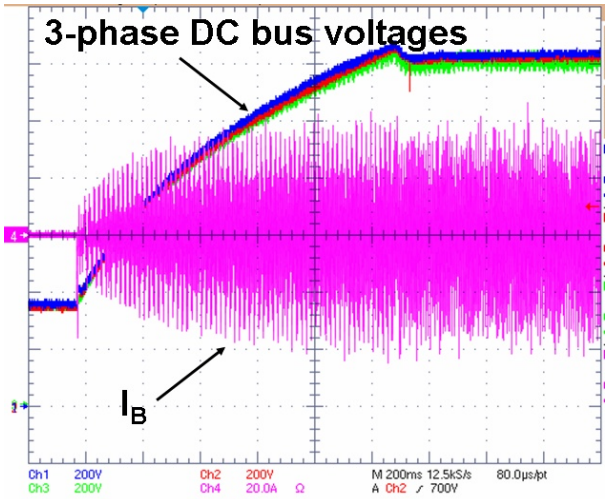


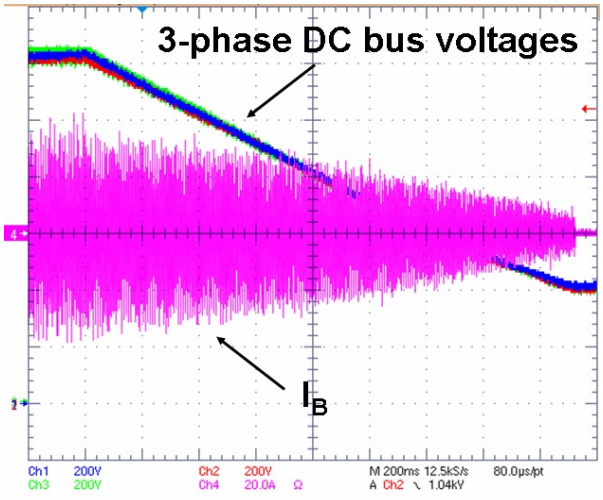
Figure 2-12. A group of designed loop gains during charge and discharge of DC capacitors.

With the designed power stage and controller, the switching model based simulation results and experiemental results of energization and de-energization for the 4.5MVA ETO-based STATCOM at 480V/100A are given below [E5]. In Figure 2-13(a), the STATCOM operation modes include (1) pre-charge mode, in which the STATCOM operates like a diode rectifier and inrush current is limited by the AC series precharging resistor; (2) energization, in which the DC bus voltage is charged to the designed value through the constant power charge method. The charge speed can be controlled by the value of Id reference. The charging slope is lower at higher Vdc is due to more power loss consumed by the converter at higher Vdc; and (3) online service, in which the STATCOM is ready for reactive power compensation, which further includes standby mode, capacitive mode and inductive mode. In the (4) de-energization mode, the DC bus voltage is discharged, just like the reverse process of energization. Finally, the STATCOM is disconnected from the AC side in the (5) post-discharge mode. In the Figure 2-13(b)(c), the energization and de-energization of STATCOM between 340V and 1200V is experimentally verified. Therefore, the proposed energization and de-energization method is proved.



(a)





(b) (c)

Figure 2-13. (a) Simulation results of STATCOM whole operating process, (b) experimental results of STATCOM energization, (c) experimental results of STATCOM de-energization.

2.4 Per-phase DC Voltage Balancing of CMC-based STATCOM

As we all know, there is no perfect identical VSC existing in the real world. Because of the slight loss difference among modular VSCs, the per-phase VSCs cannot have the same DC-capacitor voltages by the main-loop control strategy shown in Figure 2-8 and, hence, the generated reactive current at each phase can be slightly unbalanced, which is undesired and even causes the system instability in a severe case. Therefore, a per-phase DC voltage balancing of a CMC-based STATCOM is required to eliminate this unbalancing effect, whose importance is well known by researchers, but an effective method has not been offered till now due to the difficulty understanding the control plant and the absence of modeling and control theory that applies to single-phase AC variables.

Here, the proposed per-phase DC voltage balancing scheme is based on the derived transfer function in 2.2 and so-called "imaginary" DQ/ABC Park Transformation [E12]. The features of the proposed scheme are listed below:

- small-signal model-based design without any tuning
- control bandwidth is flexible through the design
- stability margin is guaranteed through the design
- simple code and easy to be implemented into DSP (no need of sin, cos, sqrt root calculation)
- generalized control design

Furthermore, with such a per-phase DC voltage balancing scheme, it is also possible to generate the balanced reactive current output at unbalanced Vpcc condition to mitigate and even compensate for the effect of the background unbalanced Vpcc.

The basic structure of the proposed method is shown in Figure 2-14. For each-phase, there is an indentical voltage loop added on the d-axis duty cycle. The compensator design of the loop is based on the control-to-Vdc transfer functions in the section 2.2. To realize the per-phase control, the dq-to-abc Park Transformation needs to be executed for each phase. By using the original q-axis duty cycle and three individual d-axis duty cycle, there are three individual "imaginary" dq-to-abc Park Transformations computed for each phase. For example, for phase A DC capacitor balancing control, the updated duty d from the phase A Vdc loop and the original duty q is transferred into abc and only duty A is used for control. The computed duty B and C just like the visual or imaginary phase B duty and phase C duty which work with the actual phase A to balance phase A's DC capacitor voltage. The actual duty for phase B and C are computed by its own voltage loops in a similar manner.

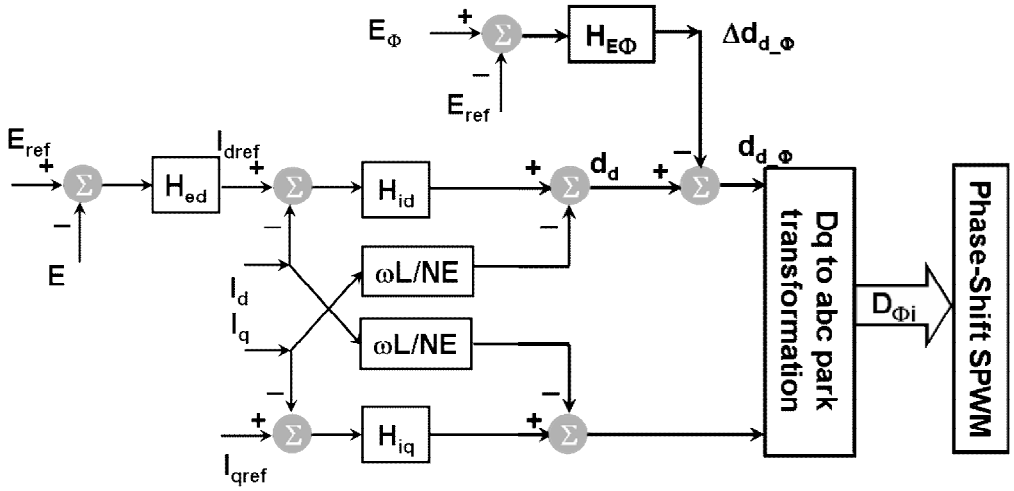


Figure 2-14. Per-phase DC voltage balancing control block diagram.

In the actual implementation of Park Transformation, only one DQ-to-ABC computation is necessary rather than three, which is very easy for digital coding and does not even increase the DSP computation, because, for the balanced phase, the Park Transformations at the other two phases are not needed to be in the feedback loop. And the implemented DQ-to-ABC Park Transformation can be expressed as:

Da = sqrt(2/3)*(cos(theta)*Dd_A-sin(theta)*Dq)

Db = sqrt(2/3)*(cos(theta-120^0)*Dd_B-sin(theta-120^0)*Dq)

Dc = sqrt(2/3)*(cos(theta+120^0)*Dd_C-sin(theta+120^0)*Dq)

Equation 2-17

With this method, a case design for scale-down TNA system is conducted below. By using the open-loop control-to-Vdc transfer function, the compensator $H_{E\Phi}$ is designed so that the control bandwidth is around 1Hz with enough stability margins, shown in Figure 2-15. The simulation results, shown in Figure 2-16, verify the proposed control scheme at different STATCOM operation modes. Excellent voltage balancing is achieved using the proposed scheme.

Figure 2-17 illustrates the experimental performance of the proposed per-phase DC voltage balancing scheme. The three curves in the middle of each graph are the DC bus voltage at each phase and the curve at the bottom is the Iq_ref command, which shows the STATCOM status of reactive power generation. Each graph at the left side gives the performance without applying the per-phase Vdc controller, and each graph at the right side gives the performance by applying the per-phase Vdc controller.

Seen from these experimental results, DC voltages at all three phases with applying the Vdc controller are balanced to Vdc_ref at steady-state. Dynamic performance is also excellent when Iq has a step change. The settling time is as expected. Compared to the simulation results, the larger initial DC voltage difference was observed before balance is reached mainly because the power loss difference in the TNA system is higher than those estimated in the simulation setup. The glitches shown in all step change graphs in Figure 2-17 are due to the sensing noises. In a summary, the experimental results verify the per-phase Vdc control scheme and the simulation results.

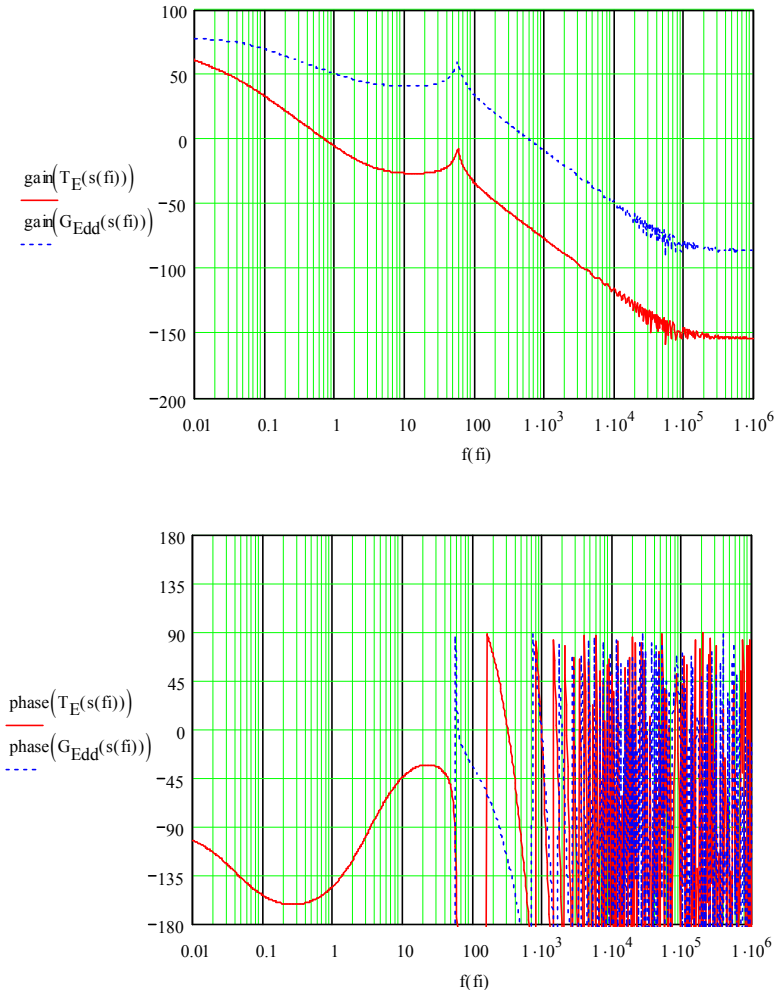
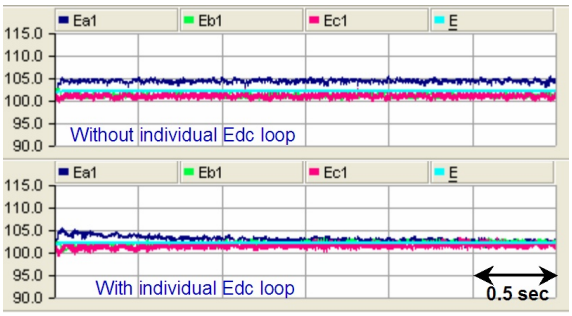
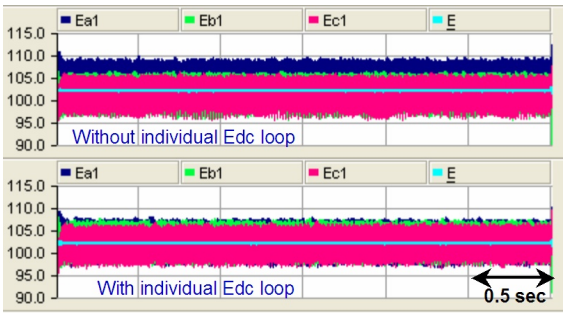


Figure 2-15. Bode plot of a per-phase Vdc balancing loop.



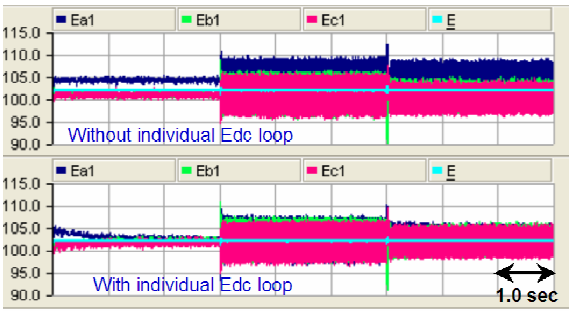
(a)



(b)



(c)



(d)

Figure 2-16. Simulation results of per-phase Vdc balancing control: (a) standy mode, (b) capactive mode, (c) inductive mode, and (d) Vdc balancing during Iq step change.

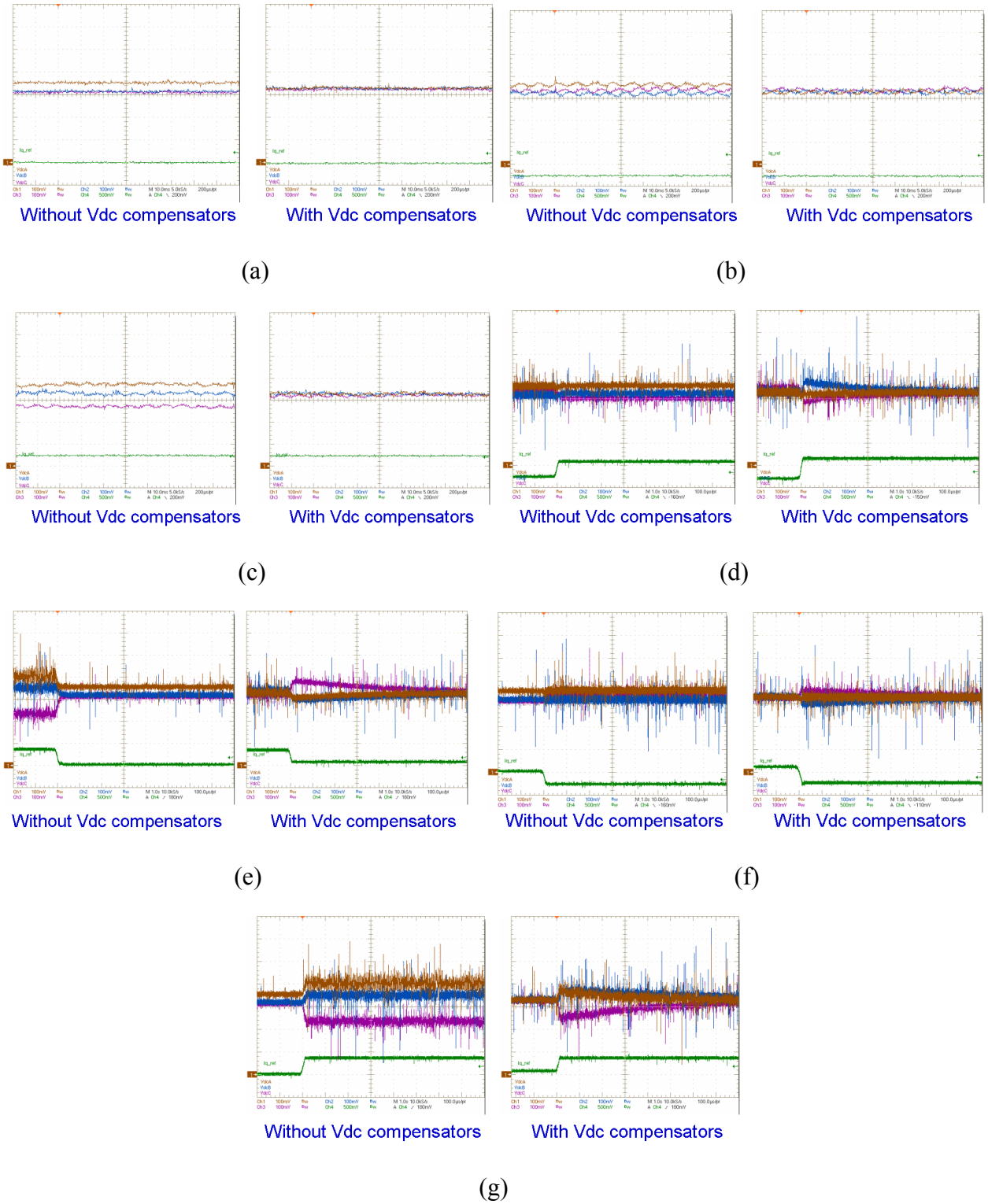
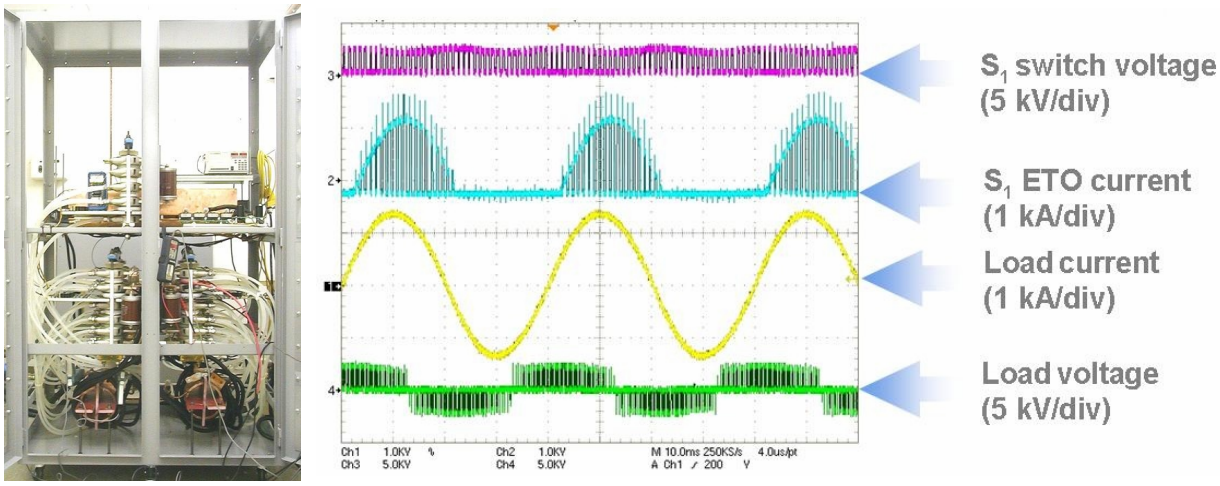


Figure 2-17. Experimental results of per-phase Vdc balancing control: (a) standby mode, (b) capactive mode, (c) inductive mode, and (d) capacitive mode step to standby mode, (e) inductive mode step to standby mode, (f) standby mode step to capacitive mode, and (g) standby mode step to inductive mode.

2.5 Design and Demonstration of a 4.5MVA CMC-based STATCOM

I. System Integration

Based on the gen-3 ETO characteristics and thermal capability, a 1.5 MVA ETO-based, full-bridge VSC building block was designed [D2][F2]. Three ETO-based VSC prototypes were built and verified at their full rating with I_o = 1 kA, V_{dc} = 2 kV, f_{sw} = 1 kHz in an open loop testing. The VSC prototype and the test results are shown in Figure 2-18.



(a) (b)

Figure 2-18. 1.5MVA ETO-based modular VSC and its full-rating test results: (a) prototype picture, and (b) full-rating open-loop test results.

Three VSC prototypes are integrated as a three-level CMC based STATCOM [E5]. One simulation result of the full-rating 4.5MVA STATCOM is shown in Figure 2-19.

At NCSU, the grid tie demonstration is limited by the grid power handling capability at the lab facility. Therefore, the present grid tie demonstration was conducted at the 480 V and 500 A level. The demonstrated power is much less than the rated power.

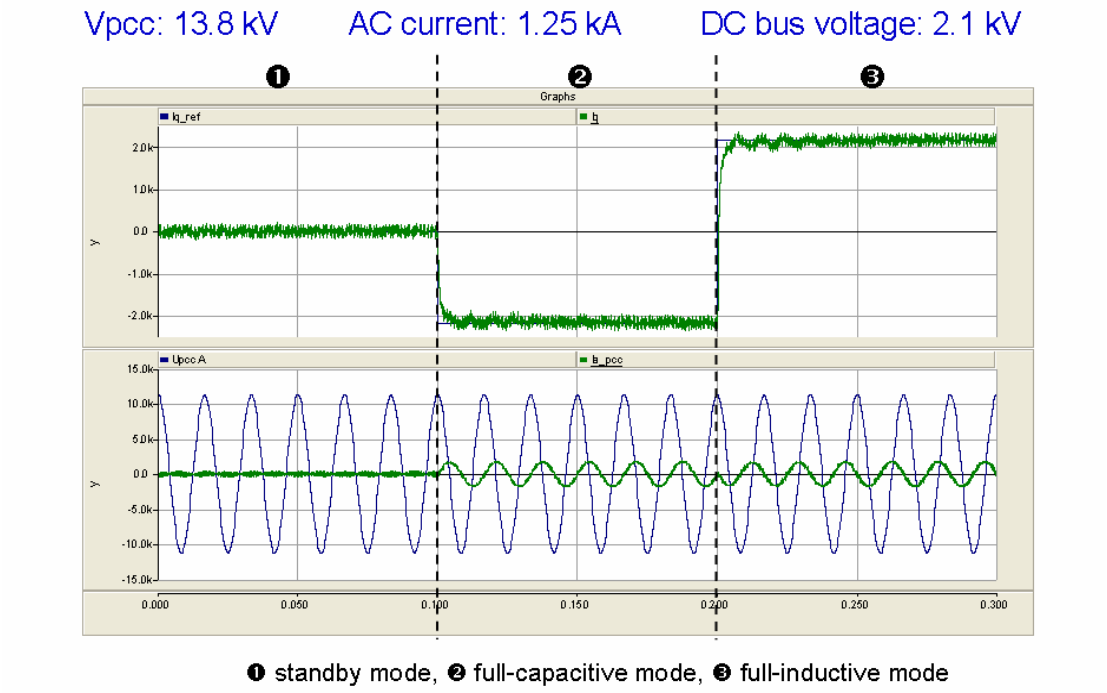
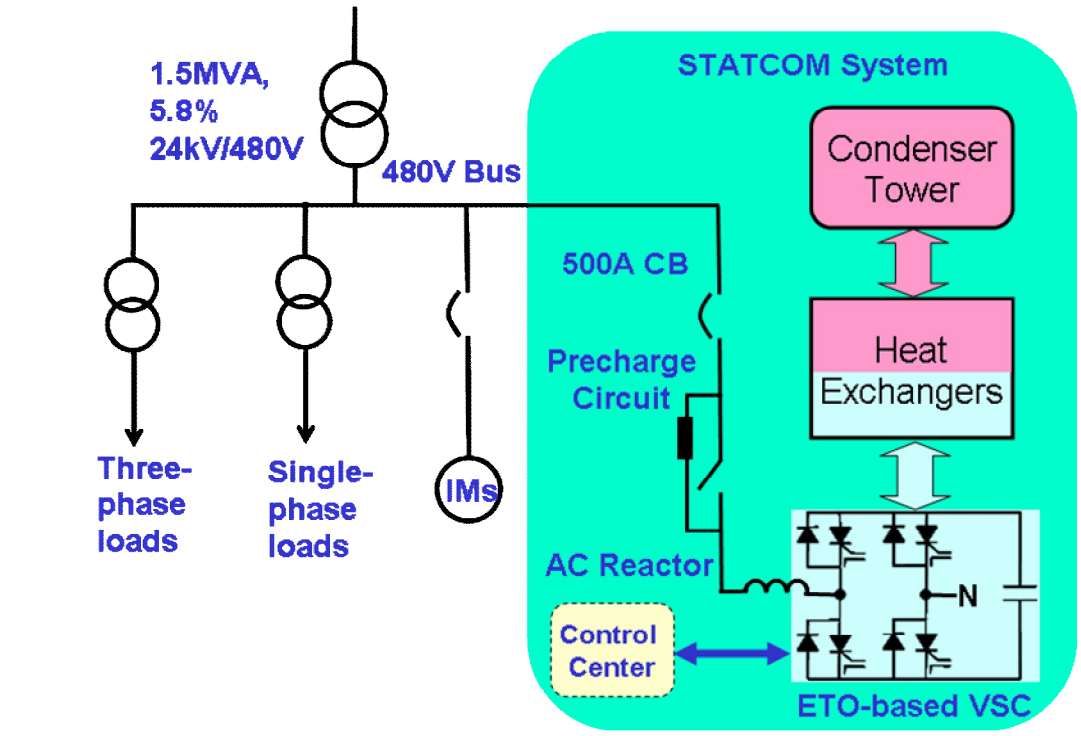
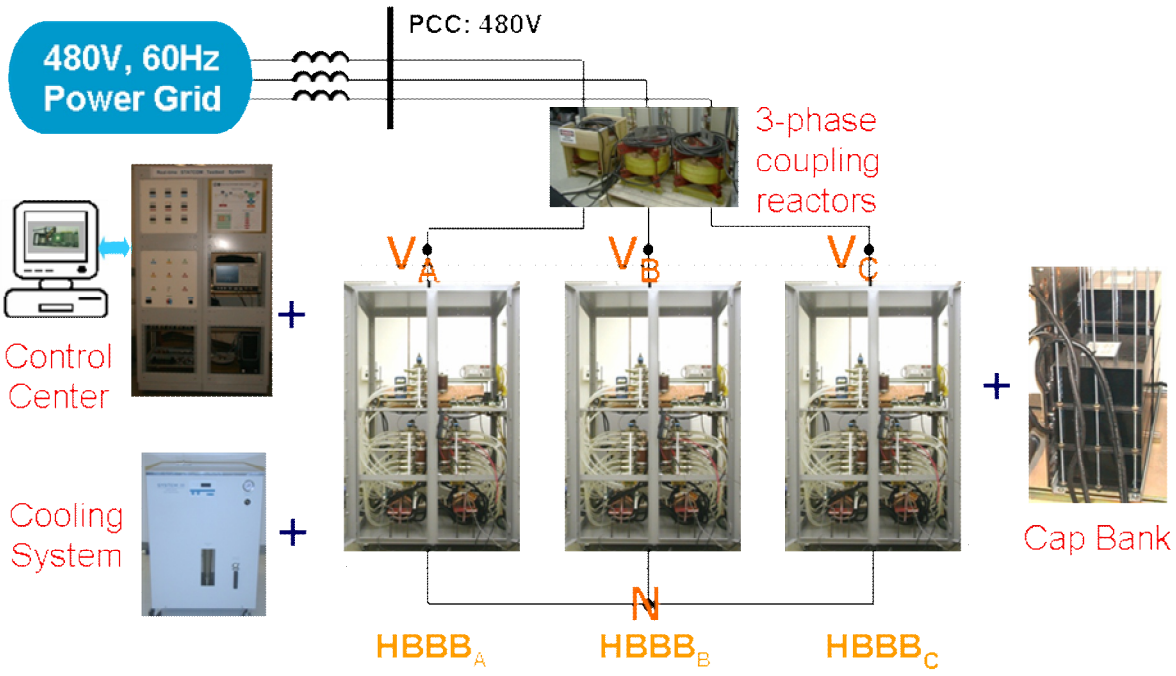


Figure 2-19. Simulation result of a 4.5 MVA ETO and CMC-based STATCOM.

Figure 2-20 shows the block diagram of the STATCOM demonstration system connected to the grid at a 480V feeder without transformer connection. Three 1.5MVA VSCs are integrated to form a three-phase, three-level CMC. The CMC is tied to the grid through a three-phase AC reactor, a three-phase AC breaker and a three-phase AC contactor. A pre-charging network that limits the inrush current when the system is connected to the grid is used. On the DC side, the film capacitors are connected as the DC capacitance per phase through an series ETO-based DC circuit breaker [D3], which is utilized for DC over-current protection and shoot-through protection. The converter system is cooled by a water-cooling system that consists of three water-to-water heat exchangers connected to a condenser tower. A detailed system integration diagram including the control center is shown in Figure 2-21. The control center will be presented in Section III below.



(a)



(b)

Figure 2-20. Schematic diagram of a 4.5MVA STATCOM: (a) one-line diagram, and (b) 480V/500A demonstration diagram.

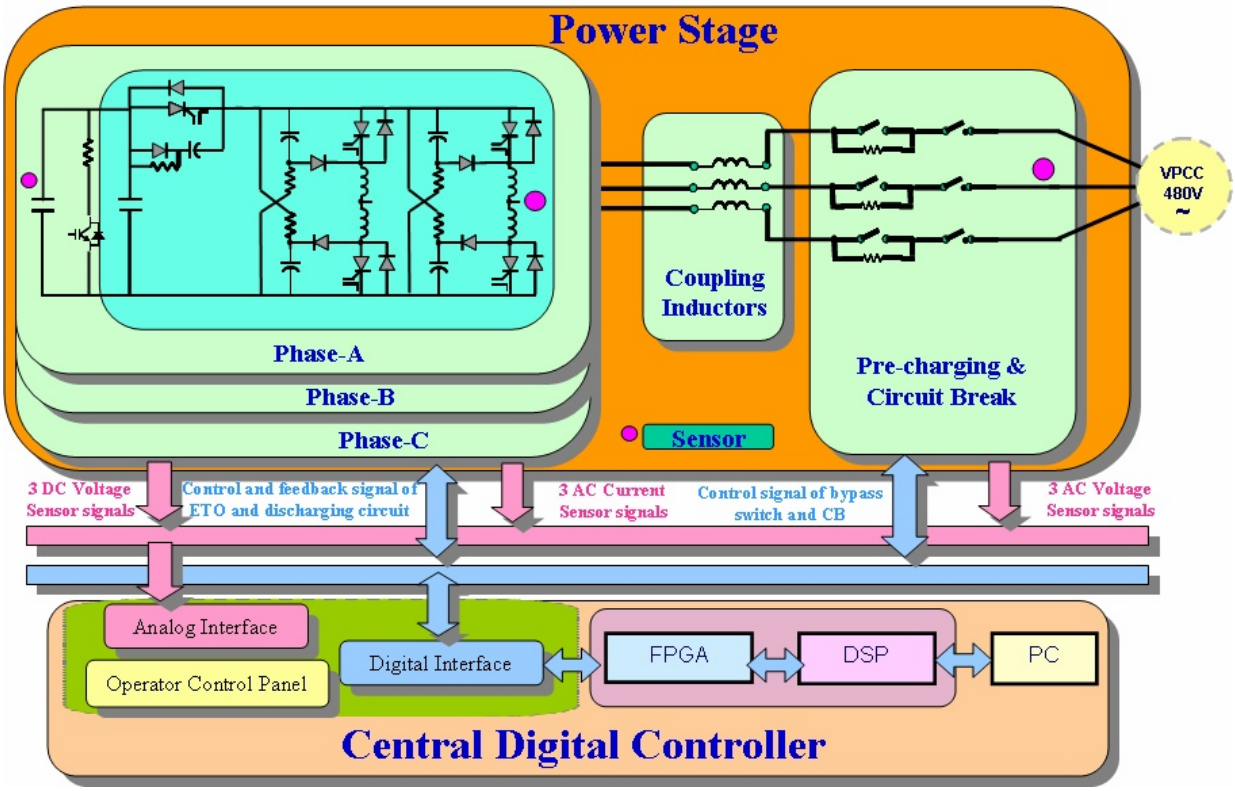


Figure 2-21. System integration diagram of the STATCOM

II. Passive Components Selection

Basically, the DC capacitance and AC coupling inductance are two key passive components for a STATCOM system.

DC capacitance selection is an optimization of DC bus voltage ripples reduction and cost. DC bus voltage ripples should be small enough so that the DC voltage can be kept almost constant to generate clear converter output voltage waveforms and also maintain stable voltage balancing. In CMC-based STATCOM, with H-bridge VSC per phase, the circulating current at the DC bus has a frequency doubling the AC fundamental frequency, e.t. 120Hz, and, hence, causes a 120Hz voltage ripples adding on the average DC bus voltage.

For the 480V/500A demonstration, the converter DC bus voltage is set to the full-rating value, 2kV, so that the same voltage stress as full rating can be tested in this experiment. Therefore, the converter has to run at a low modulation range.

Moreover, the adopted modulation method is unipolar SPWM (sinusoidal pulse width modulation) with a switching frequency at fsw = 1020 Hz, which is 17 times of the fundamental frequency, so that the converter output voltages have a harmonics sideband around k*2*1020Hz.

In the literature hitherto, we do not find an accurate formula to estimate the DC capacitance while considering the whole modulation range from low to high for unipolar SPWM. In the following equation, such a formula is derived for DC capacitance selection and is experimentally verified.

The proposed DC capacitance formula derivation schematic is shown in Figure 2-22. Vdc is charged and discharged due to SPWM current pulse. Through the equivalent approach in Figure 2-22(c), a sinusoidal waveform can be utilized to get the integral of Io for a quarter cycle, and, therefore, the DC bus voltage ripple, DC capacitance and Modulation index (M) can be derived and is shown below:

$$\Delta V_{pp} = \frac{\sqrt{2} \cdot I_{rms}}{C_{dc} \cdot \omega_f} \sqrt{1 - \sin(a\cos(\frac{M_{\max} \cdot \pi}{4}))}$$

Equation 2-18

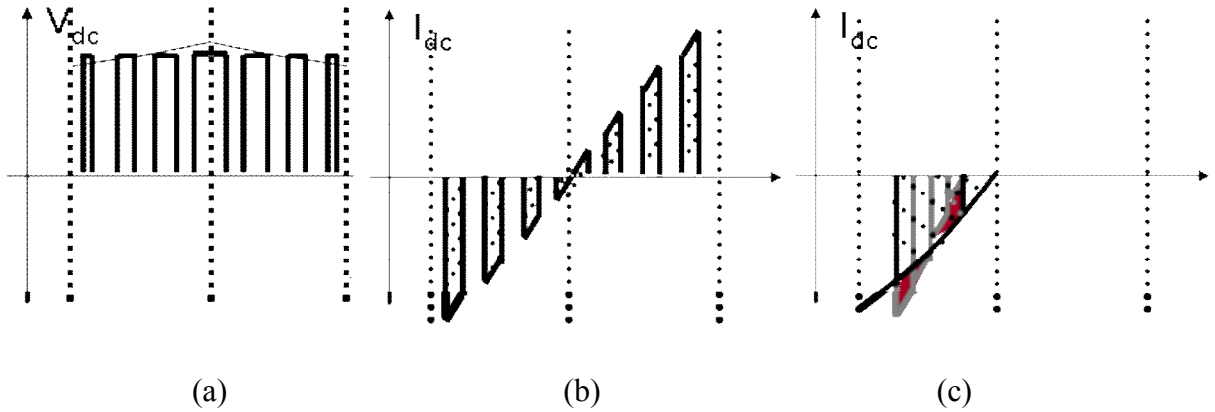


Figure 2-22. DC capacitance formula derivation schematic in half cycle: (a) Vdc and Vo, (b) capacitive Io, and (c) equivalent Io integral.

Obviously, the DC bus voltage ripple is a function of Io, Cdc and M. And the ripple requirement is determined for the worst case, which is the maximum capacitive mode. For 500A maximal Io, the ripple as the function of Cdc and M is plotted in Figure 2-23.

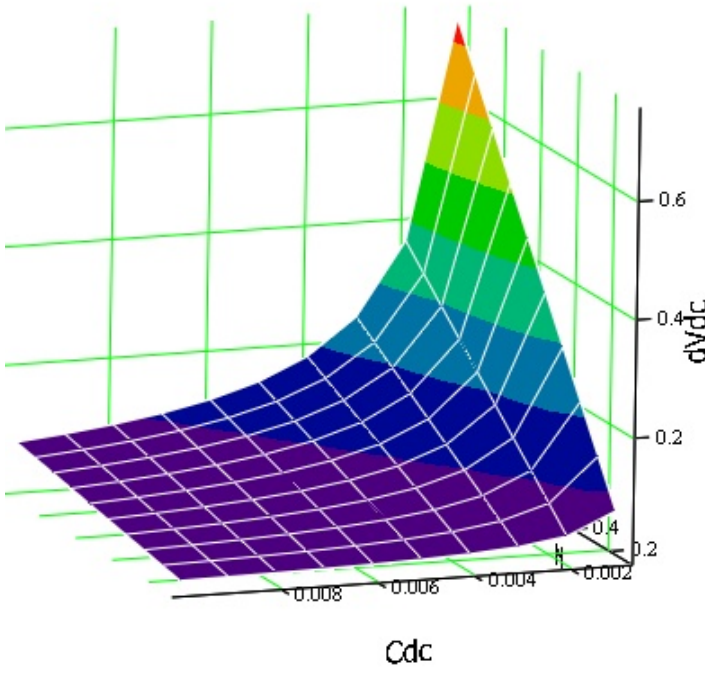


Figure 2-23. Relationship among Vripple, Cdc and M

On the other side, the AC coupling inductance is a matter of modulation index operation range and current harmonics. Normally, the AC coupling inductance is around 0.1pu~0.2pu and the modulation index operates at the high end to minimize harmonics. In this specific case, with given M at standby mode, a per-unit AC reactance can be calculated by:

$$X_{ac_pu} := \frac{M_{max} - M_{standby}}{M_{standby}}$$

Equation 2-19

To meet the IEEE standard 519 harmonics requirement [9], a Mmax has to be large enough so that the AC reactance is relatively large to reduce the current Total Demand Distortion (TDD) to a acceptable level.

After considering the tradeoffs among the design requirements (harmonics and DC bus voltage ripple), the STATCOM specifications are designed and shown in Table 2-1.

TABLE 2-1. DEMONSTRATED STATCOM SPECIFICATION

Three-Level ETO CMC STATCOM	**3-Phase, 3-Wire Wye-Connection**
Individual DC Bus Voltage	**2000±18% V/Phase**
Rated RMS Reactive Current	**500 A/Phase**
Capacitor Impedance	**(0.5m-j/(ω ×1.7mF)) Ω/Phase**
Individual Switching Frequency	**1 kHz**
Coupling Reactor Impedance	**(31m+jω ×2.75 m H) Ω/Phase**
PCC Line-to-line Voltage	**480 V/Phase**

The experimentation setup of the STATCOM with designed passive components is shown in Figure 2-24.

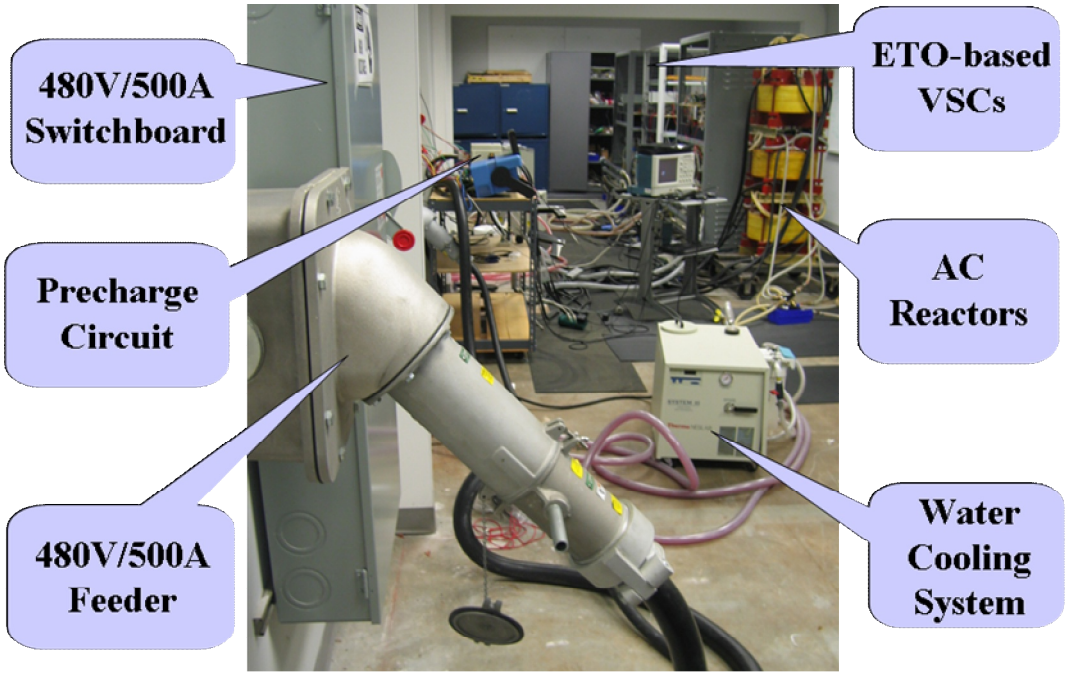


Figure 2-24. STATCOM 480 V/500 A setup

III. Digitial Controller

Based on the derived models and small-signal transfer functions, the closed-loop decoupled controller has been developed and is shown in Figure 2-8. For the control design, the current loop is designed to achieve a high-bandwidth control so that the STATCOM can respond to the command in a subcycle. The Id channel is utilized to balance the DC bus voltage with a slow voltage loop regulator, and the Iq channel is directly utilized to respond to the Var compensation command. These three compensators (H_{id}, H_{iq}, H_E) are designed based on the CMC-based STATCOM model in dq0 frame to achieve the satisfactory bandwidth, gain margin and phase margin for the STATCOM's whole operation range. For the DC capacitor energization and deenergization, the method proposed in 2.3 is adopted.

With the designed power stage and controller, the switching model-based simulation results for the 480V/500A STATCOM are given below. In Figure 2-25, the STATCOM operation modes include (1) pre-charge mode, in which the STATCOM operates like a diode rectifier and inrush current is limited by the AC series precharging resistor; (2) energization, in which the DC bus voltage is charged to the designed value through the constant power charge method. The charge speed can be controlled by the value of Id reference. The charging slope is lower at a higher Vdc due to more power loss consumed by the converter at a higher Vdc; and (3) online service, in which the STATCOM is ready for reactive power compensation, which includes standby mode, capacitive mode and inductive mode. In the (4) de-energization mode, the DC bus voltage is discharged, just like the reverse process of energization. Finally, the STATCOM is disconnected from the AC side in the (5) post-discharge mode.

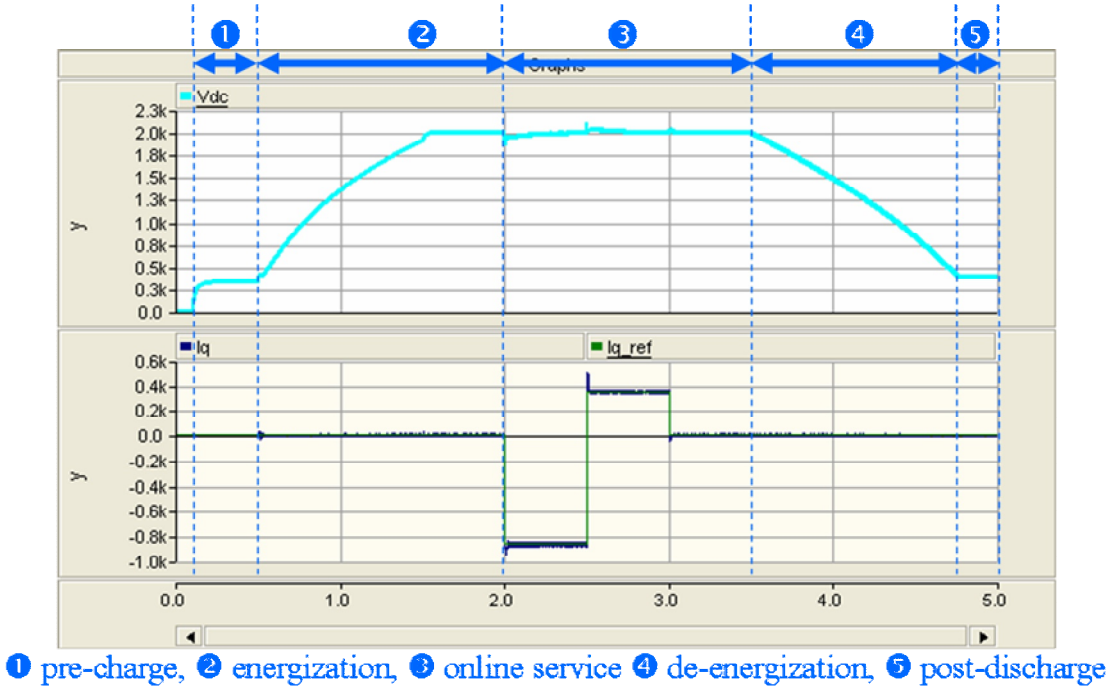


Figure 2-25. Simulation results

Figure 2-26 shows the control system setup. The controller consists of a 64-bit DSP (TMS320C6701), 50 k-gate FPGA (Xilink XCV50), interface circuits and operator control panel. As the central process unit of the whole controller, DSP computes the main feedback control algorithm, monitors system operations and executes the protection command if necessary. FPGA, performing as the DSP buffer, communicates bi-directionally with DSP to transfer in the sampling signals and transfer out the switch duty command, and also calculates the SPWM algorithm to translate the duty signal into practical valve switching signals. Interface circuits, besides transferring the signals, also perform the hardware protection scheme in the case of the FPGA/DSP failure.

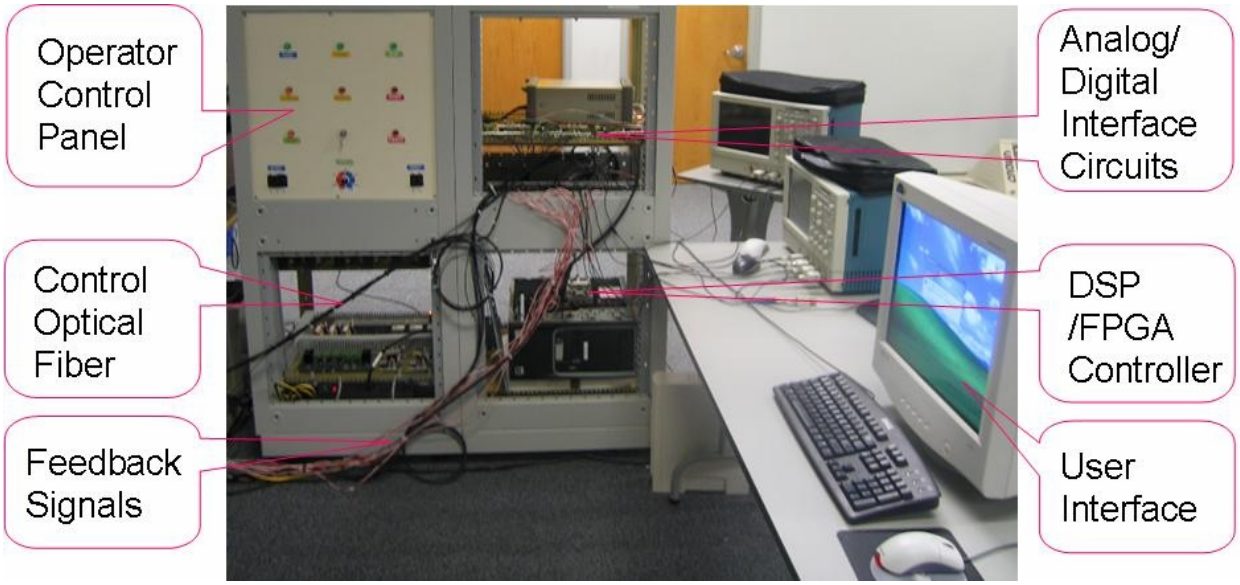


Figure 2-26. Central controller setup

The STATCOM system is protected by protection schemes at both software and hardware levels. Three DC-side solid-state circuit breakers [D3] are used to protect the converter under

shoot-through conditions. Converter testing under shoot-through conditions was first conducted to verify that the protection scheme can indeed protect the system under shoot-through conditions. In the STATCOM system, other protection schemes include: the software trip protection of DC-side over-voltage, DC-side abnormal voltage, AC-side over-voltage, AC-side over-current, switching signal interlock and valve failure protection, and the hardware-trip protection of DC-side over-voltage, DC-side over-current, and AC-side over-current. All of these proection schemes protect both the STATCOM side and utility side from contingencies.

Figure 2-27 shows the control flow block diagram of STATCOM operation modes, which can be controlled through the operator control panel.

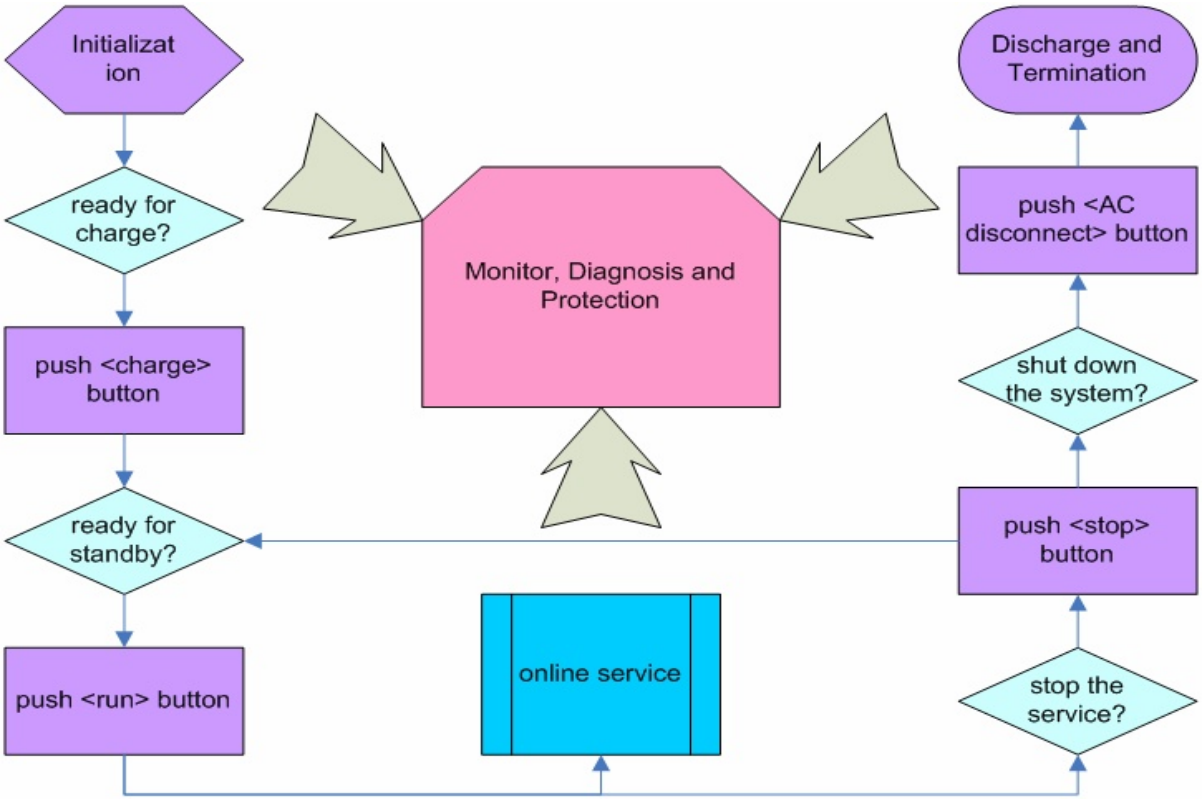


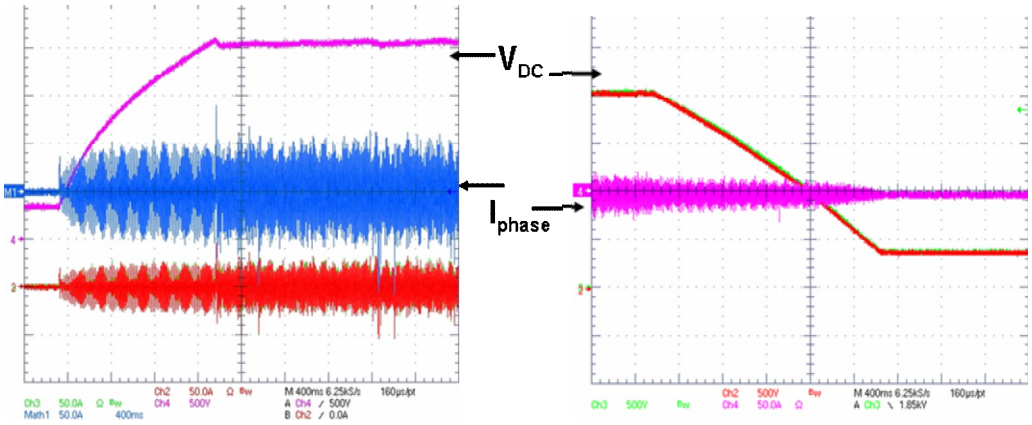
Figure 2-27. STATCOM operation modes

IV. Transformless Grid-Connected Demonstration

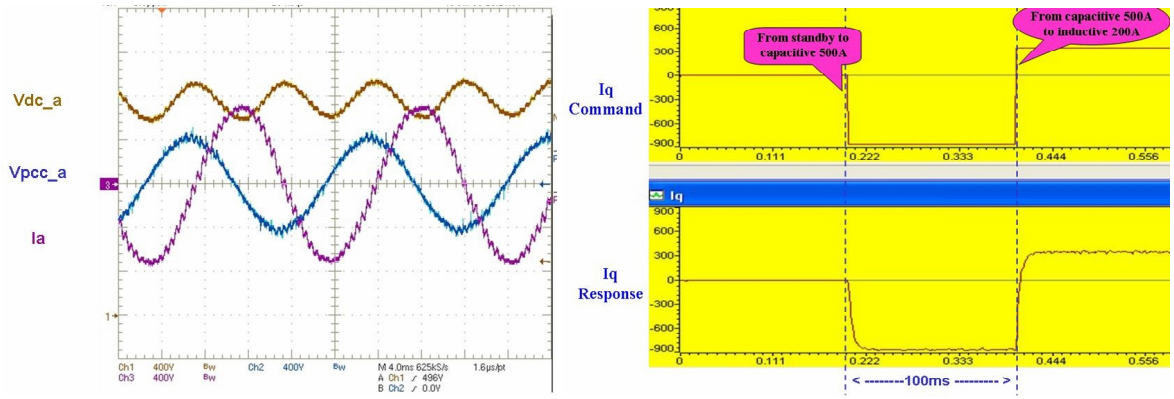
Figure 2-28 gives the experimental demonstration results. First, the DC-cap voltages are pre-charged to a desired voltage level and ready for energization. By closing the current loop, three separate DC-capacitors at each phase are energized through a small Id charge until 2 kV , and de-energization becomes the reverse process of the energization process, both of which are shown in Figure 2-28(a)~(b) and verifies the design and simulation results in the previous section. Such a charge/discharge scheme eliminates the bulky DC-side charge/discharge circuit and achieves a fast, flexible startup/shutdown of STATCOM.

The typical experimental results during the steady-state 500A capacitive current are shown in Figure 2-28(c). Here, the current direction is defined to flow from the converter out to the grid. Clearly demonstrated is that the DC voltage peak-to-peak ripple is just 18% of the 2kV DC bus voltage, which exactly matches the design and verifies the derived formula in the previous section.

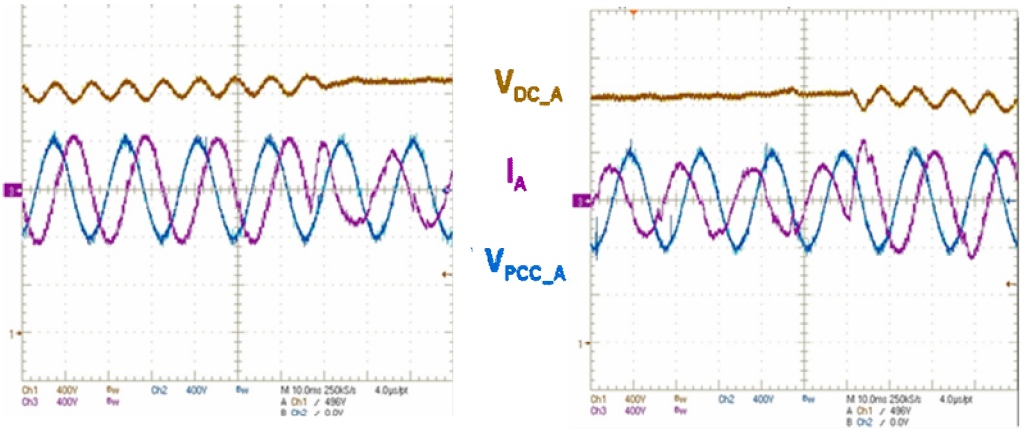
The STATCOM dynamic response for Iq command step change is shown in Figure 2-28(d)~(f). Clearly demonstrated is the fast dynamic response speed (subcycle) of the system and the smooth reactive current with small harmonics that results from the 1 kHz PWM switching frequency and the hundreds Hz current loop bandwidth.



(a) (b)



(c) (d)



From Capacitive 300A to Inductive 200A **From Inductive 200A to Capacitive 300A**

(e) (f)

Figure 2-28. STATCOM experiment waveforms: (a) energization, (b) de-energization, (c) capacitive 500A, (d) Iq step response, (e) + Q → -Q, and (f) - Q → +Q.

Besides the recorded waveforms, various data are also recorded. Table 2-2, gives the measured DC bus voltages and voltage ripples when STATCOM operates at different VAR levels, which demonstrates good DC bus voltage balancing as the DC voltage ripples consistently verify the design. Table 2-3 gives the measured PCC voltages and THD for different conditions, which demonstrate how the grid bus voltage is regulated by the injected STATCOM VARs.

TABLE 2-2. DC BUS VOLTAGES AND RIPPLES

	Standby	Cap 200A	Cap 300A	Cap 400A	Cap 500A
Vdc_A (kV)	2.06	2.01	2.04	1.98	1.90
Vdc_B (kV)	2.04	2.05	2.08	2.06	2.00
Vdc_C (kV)	2.01	2.01	2.02	1.99	1.93
Ripple of Vdc (V)	12.0	92.0	162.0	238.0	364.0

TABLE 2-3. VOLTAGES AND THD AT PCC

	Vpcc_phase	Vpcc_THD
Shutdown	281	1.9
Standby	281	2.1
Inductive 200A	276	2.8
Capacitive 500A	290	2.2

For the cooling system, the heat exchangers run at a flow rate of 52.5 LPM (liter per minute) through the pre-phase converter. The circulating water through the three phases maintains a nearly constant value of 32°C, with a rise of less than 3°C over the water temperature during STATCOM shutdown. The measured ETO temperature is shown in Table 2-4, which demonstrates that ETO thyristors exhibit a steady and controllable rise with the rising current. At maximum capacitive current, the anode temperature of the ETO switch goes up to 60°C, and thereby the junction temperature is around 73°C/kW, which means that the ETO is well cooled.

TABLE 2-4. COOLING PERFORMANCE MEASUREMENT

	Facility Water (°C)	Phase A ETO (°C)	Phase B ETO (°C)	Phase C ETO (°C)
Capacitive mode 200A	31	34.8	34.6	34.8
Capacitive mode 300A	31	47.4	48.4	48
Capacitive mode 400A	31	54	55.2	54
Capacitive mode 500A	31	63.8	61.4	59.5

In this section 2.4, the transformerless grid-connected experimentation of a state-of-the-art ETO and Modular H-bridge PWM converter-based 4.5MVA STATCOM system is presented. The system design with emphasis on system integration, the passive component selection and digital controller design is described. The steady and dynamic performance, DC bus voltage regulation, and cooling performance of the STATCOM system are all clearly demonstrated. Through such experimentation, not only are three defined key technologies for next-generation

power electronics-based transmission controllers, which are advanced power switch technology, modular converter technology and its control technology, but also a state-of-the-art STATCOM system with high performance and low cost is illustrated and ready for a full-rating field test.

2.6 Conclusion

In this chapter, the literature of CMC-based STATCOM modeling and control by previous researchers are first reviewed. To further understand and analyze the controlled CMC-based STATCOM plant, the full-order transfer functions of a generalized CMC-based STATCOM are derived and compared to the reduced-order transfer functions derived from previous researchers. The relationships between full-order and reduced-order transfer functions are illustrated, and the conditions where the reduced-order transfer functions can be used for closed-loop control design are pointed out. As a result, a clear and simple control design guideline is given.

Based on the analysis of the derived control-to-current transfer functions, a DQ frame-based control method of AC-side close-loop direct energization and de-energization of a CMC-based STATCOM, which eliminates the costly and bulky additional DC charge/discharge ciruit and flexibly controls the speed of energization and de-energization, is presented. With such a method, the control design is conducted by loop-gain shaping method without tuning compensators' parameters. The proposed method is verified by the simulation and experimental results.

To deal with unbalanced DC voltages at each phase in a CMC-based STATCOM, a per-phase DC bus voltage balancing control strategy, based on the derived control-to-Vdc transfer function and imaginary DQ0-to-ABC Park Transformation, is presented. Based on the derived

transfer functions, the balancing control loops are designed with a desired bandwidth, phase margin and gain margin. Through the imaginary DQ0-to-ABC transformation method, the DQ frame-based balancing control loop is allowed to be applied at each individual phase for per-phase balancing control. The proposed method is not only a generalized design with ensuring bandwidth and stability margin, but also efficient for DSP/FPGA implementation and computation. The simulation and experimental results well proves the steady-state and dynamic performance of the proposed per-phase DC voltage balancing control strategy.

Finally, a transformerless grid-connected demonstration of a 4.5 MVA ETO, CMC-based STATCOM prototype is presented. The system integration, passive components selection and digital controller of the demonstrated system are illustrated. The experimental results show not only the stable and fast reponse of the STATCOM, but also its low harmonics, excellent DC voltage balance and cooling performance.

In summary, through such a demonstration, not only are three key technologies for next-generation power electronics-based transmission controllers, which are advanced power switch technology, modular converter technology and its control technology, but also a next generation STATCOM system with high performance and low cost is illustrated and ready for a full-rating field test. It is expected that the successful demonstration of this emerging STATCOM technology will result in a FACTS that is capable of extremely fast response and that is less costly per kVA than FACTS based on conventional power electronics technologies.

Chapter 3 WIND FARM VOLTAGE FLUCTUATION SUPPRESSION

Recently, renewable wind energy is enjoying a rapid global growth to become an important green electricity source to replace polluting and exhausting fossil fuels. However, with wind being an uncontrollable resource and the nature of distributed wind induction generators, integrating a large-scale wind-farm (WF) into a power system poses challenges, particularly in a weak power system.

In this chapter, the study of a STATCOM in facilitating the integration of a large WF into a weak power system is presented. First, an actual weak power system with two nearby large WFs is introduced. Based on the field SCADA data analysis, the issues are highlighted, and steady-state and dynamic voltage controls are needed to solve these issues. A STATCOM is proposed for dynamic voltage control, particularly to suppress the short-term (seconds to minutes) voltage fluctuations. Secondly, a model of the system, WF and STATCOM for steady-state and dynamic impact study is developed in the PSCAD/ETMDC simulation environment. The developed model is validated by using the field data. Moreover, based on the PV and VQ curves obtained from the simulation, the system voltage control and stability issues are analyzed, and the size and location of STATCOM are assessed. Finally, a STATCOM control strategy for voltage fluctuation suppression is presented, and the dynamic simulations are used to verify the performance of the proposed STATCOM and its control strategy.

3.1 System Description

Figure 3-1 shows the system investigated in this study. The two WFs, WF1 and WF2, are connected to the existing 69kV loop system at bus 3 and bus 5. The system is supplied by the two main substations, which are represented by three remote boundary equivalent sources at bus 1, 2 and 12. Among them, bus 1 is the strong bus with a short circuit capacity of about 4000 MVA. The WF2 at bus 3 is a large wind farm with a total rating 100 MVA. It is a type C WF [H2] with variable-speed DFIGs (double fed induction generators) and partial back-to-back converters. The WF1 at bus 5 is located at the middle of the weak 69 kV subtransmission system and the short circuit capacity at the bus 5 is about 152 MVA. And the WF1, with a total rating of 50MVA, is type A WF [H2] using fix-speed SCIGs (squirrel cage induction generators). The 6 loads tapped on the 69 kV weak loop system are mostly rural radial loads. The loop network is normally kept closed to improve the reliability of the power supply.

The integration of WF2 into the grid is facilitated by the power converter based interface as it provides VAR compensation capability and, hence, voltage control capability. On the other hand, the WF1 poses a challenge, as the SCIGs sink more VARs when they generate more real power, and the generated wind power rapidly fluctuates with an uncontrollable wind speed, and the large surge current occurs during frequent startups of wind turbines. Thus, when WF1 is located at the weakest part of the loop system, these characteristics of WF1 not only increase the transmission and distribution losses, reduce the system voltage stability margin and limit power generation, but also cause severe voltage fluctuations and irritate the customers in the system, particularly in the weak 69kV loop, where a significant portion of the loads are induction motors, which are sensitive to voltage fluctuations.

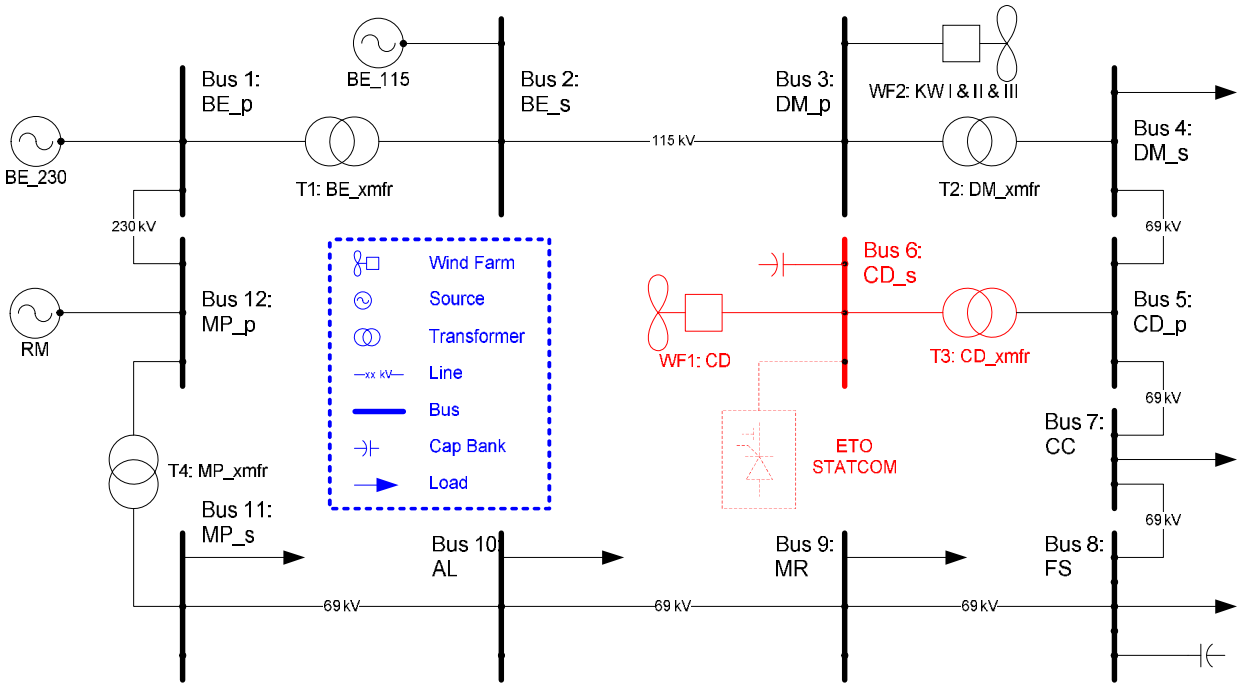


Figure 3-1. One-line diagram of the studied system.

To reduce the voltage fluctuations and improve the power factor, small size MSCs (hundreds kVar) are installed at each individual SCIG terminal and large size MSCs (1~2 MVAr) are installed at bus 6, the 35 kV secondary side of the WF1 main transformer T3. Moreover, to provide voltage support, all the main transformers T1~T4 and many customer transformers have several taps, and two additional MSCs (2.75MVAr each) are installed at bus 8. However, because of slow response time, these devices do not satisfactorily address the dynamic issues of WF1, and even exacerbate them.

Figure 3-2 shows the selected power injection and voltage profile data at WF1 monitored during a typical 3-day operation. The sampling rate of the data is 5 minutes. In Figure 3-2(a), this

profile covers a WF1's whole operating process, from idle (no wind generation) to full rated power output of 50 MW and back to idle. As Figure 3-2(b) indicates, the power factor of WF1 is usually very high, about 0.99 lagging, which is fulfilled by controlling the MSCs at individual SCIGs and bus 6, as long as the generated wind power is larger than about 1 MW. The figure also shows that, when the system is idle, WF1 produces 1~2 capacitive MVAr because of the shunt capacitance of the underground cables connecting individual wind turbines to the common bus 6. Figure 3-2(c) indicates that the voltage fluctuation at bus 5 is about ±1.4% during this period. The year-round monitored data indicates that this is the case most of the time, although ±5% voltage fluctuation sporadically happens from time to time. And there is also voltage fluctuation even without any WF1 generation, which means that the voltage fluctuations of local system are not only caused by generated power fluctuations of WF1, but they are also contributed by WF2 and voltage fluctuations at the remote boundary buses. Therefore, a single STATCOM using emitter turn-off (ETO) thyristor and cascaded-multilevel converter (CMC) is proposed to suppress the voltage fluctuations of the weak loop system.

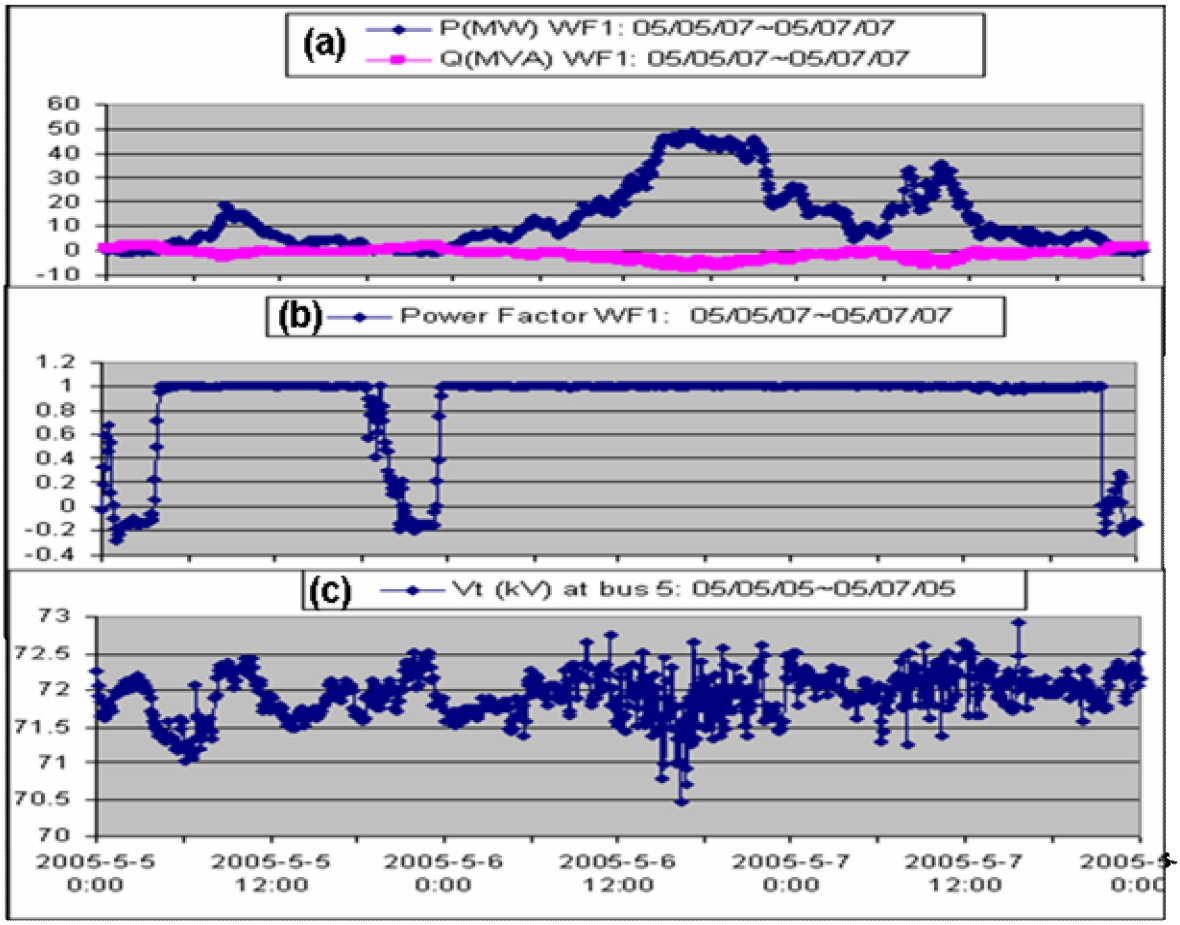


Figure 3-2. Field SCADA data of wind farm typical operation.

3.2 Modeling and Control

In this section, the modeling, PSCAD implementation and validation of the studied 12-bus power system, wind farm and STATCOM are presented.

I. 12-Bus System Model

The system shown in Figure 3-1 is modeled using PSCAD/EMTDC. Since only a balanced operation is considered for this study, the positive-sequence dynamic model is developed. Some of the details include:

- Boundary equivalent source is modeled as ideal voltage sources with series equivalent impedances;

- Transmission lines are represented by their equivalent π model;

- Transformers are implemented using the PSCAD classical transformer modeling approach with including the leakage inductance and resistive loss;

- Loads are considered as constant power. Only one load profile is considered. Data for the monitored loads are obtained from the SCADA, and for the non-monitored loads, they are assumed to be 30% of their supply transformer rating.

II. Wind Farm Model

Since the focus in this study is the system impact study of electrical power flow and voltage, the implemented model of the WFs does not include mechanic dynamics and the detailed electrical model of induction machine [H6][H8], so it is an ideal voltage source with equivalent series and shunt impedance. For such a WF model, the following assumptions have to be made:

- All wind turbines are identical;

- Wind speed is uniform, so that all wind turbines share the same power generation;

- Each turbine runs at the same operating modes at all times, the voltages, current and power factor of each turbine are the same;

- The series equivalent impedances of underground cables that connect the SCIGs to the common bus 6 are negligible;

- All transformers connecting individual SCIGs are identical.

With these assumptions, both WF1 and WF2 are modeled as a quasi-dynamic model so that all the real power, reactive power and voltage of WFs are dynamically controlled to recur the system operation from the field SCADA data for an operating point for steady-state study and a continuous period for dynamic study, where the real power of WF is controlled by the source phase angle, the reactive power of WF is controlled by a shunt cap bank at 35kV bus of WFs, and the bus voltage of WF is controlled by the source voltage.

From the 3-day data in Figure 3-2, a 6 hour period data of the WF1 typical low power generation, which represents a smaller amount of turbine online and the weakest grid connection of WF1, is selected for study. This case corresponds to the operation of 8 turbines out of the total 83 turbines in WF1. To account for the Var contribution of the underground cables, a 2.06MVAr shunt capacitor is added at the 34 kV interface bus 6.

III. Model Validation

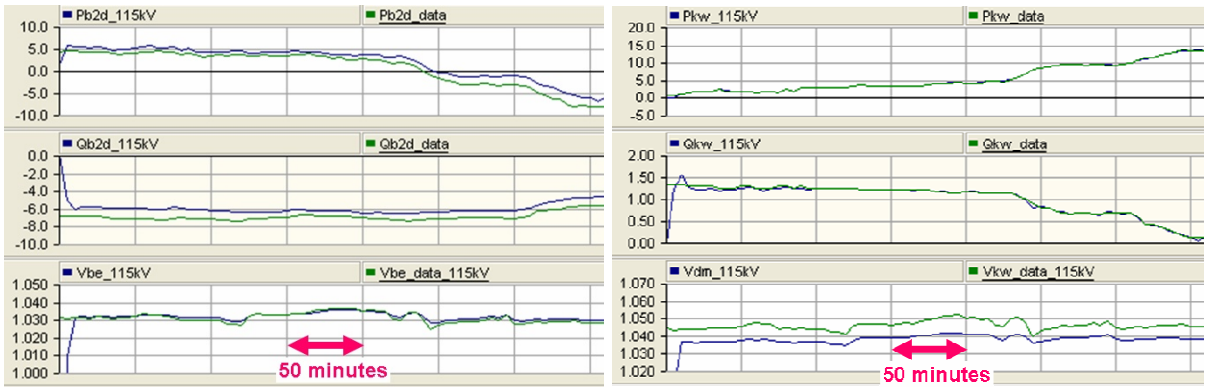
First, a specific operating point in a 6 hour period is selected. By tuning the boundary sources, WFs and the non-monitored loads, this operating point is simulated on PSCAD/EMTDC. The results, given in Figure 3-3, match the field data quite well. Therefore, the 12-bus system model with WFs at the specific operating point is validated.

2005-5-5 20:50:00	Bus 2 to Bus 3	Bus 3 to WF2	Bus 4 to Bus 5	WF1 to Bus 5
Psimu (MW)	4.1 ok	-3.1 ok	4.26 ok	0 ok
Pdata (MW)	3.72	-3.16	4.176	0.0
Qsimu (MVA)	-6.4 ok	-1.6 ok	-3.25 ok	1.08 ok
Qdata (MVA)	-6.78	-1.2	-3.384	1.09
Vsimu (p.u.)	1.034 ok	1.04 ok	1.036 ok	1.04 ok
Vdata (p.u.)	1.034	1.0466	1.026	1.043

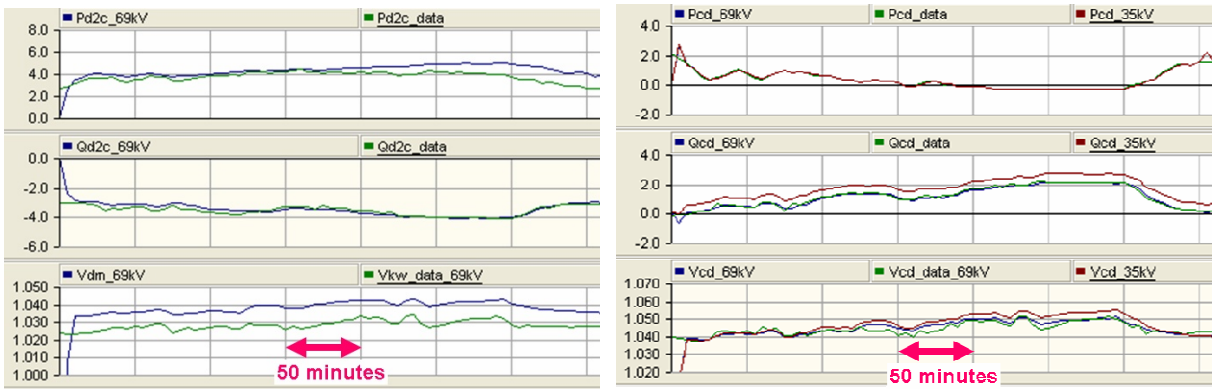
Figure 3-3. Comparison of simulation result and field data at an operating point.

To simulate the operation of the system during 6 hour period, the model is closed-loop controlled by PI controllers in order to match with the monitored data. Therefore, a whole contineous period operation of the studied system can be fully recurred in the off-line PSCAD simulation.

The time-domain simulation results for this 6 hour period are given in Figure 3-4 together with the actual data, where the units of real power, reactive power and voltage are respectively MW, MVAr and p.u., which is the same for the units in the later system simulation results. In general, compared to the field data, the simulated real power, reactive power and voltage follow almost the same fluctuation trend and magnitude, and also have good match in terms of the steady-state values. Therefore, the system models in a continuous operation period are validated and can therefore be used for dynamic STATCOM impact study in the next section.



(a) (b)



(c) (d)

Figure 3-4. Comparison of simulation result and data for a 6 hour operation: (a) bus 2 voltage and power flow from bus 2 to bus 3, (b) bus 3 voltage and power flow from WF2, (c) bus 4 voltage and power flow from bus 4 to bus 5, and (d) bus 5 and 6 voltage and WF1 power output at bus 5 and 6.

Moreover, there are some insights that can also be pointed out from Figure 3-4:

- The mismatch at the beginning of each waveform is because of the simulation initialization transient, which is the same for the later time domain simulation results and will not mentioned again;

- For the real power in Figure 3-4(a)(c), there is a slightly increasing mismatch between the simulation results and the field data, which is because this period is close to midnight and the actual loads gradually decrease while the simulated loads are all modeled as fixed loads;

- For the voltages in Figure 3-4(b)(c), there is a small steady-state offset between the simulation results and field data, though the simulation results follow almost the same fluctuation trend and magnitude while compared to the data. This could be because the tap changer settings of some transformers are unknown and not included into the model;

- In Figure 3-4(d), because of the T3's reactance, there is a constant offset between reactive power at 35 kV bus 5 and 69kV bus 6, and a slightly higher voltage profile at bus 5 than bus 6.

IV. STATCOM Model and Control

The proposed STATCOM uses a CMC-based toplogy, as shown in Figure 2-1. For this study, a harmonics-free dynamic model of the CMC-based STATCOM with its internal control as shown in Figure 2-8, is implemented on PSCAD/EMTDC.

The simulated results, shown in Figure 3-5, illustrate how the CMC-based STATCOM responds to step change commands for increasing and decreasing its reactive power output, where the units of DC voltage, reactive current, AC voltage, AC output current and reactive power output are respectively kV, kA, p.u., p.u., and MVAr. As the figure illustrates, the reactive current step change response has a bandwidth as fast as a quarter-cycle, and ±10MVAr is generated by the STATCOM, and the average DC capacitor voltage of about 1.5 kV is dynamically controlled and does not change due to the Var command change. Therefore, the STATCOM model is validated.

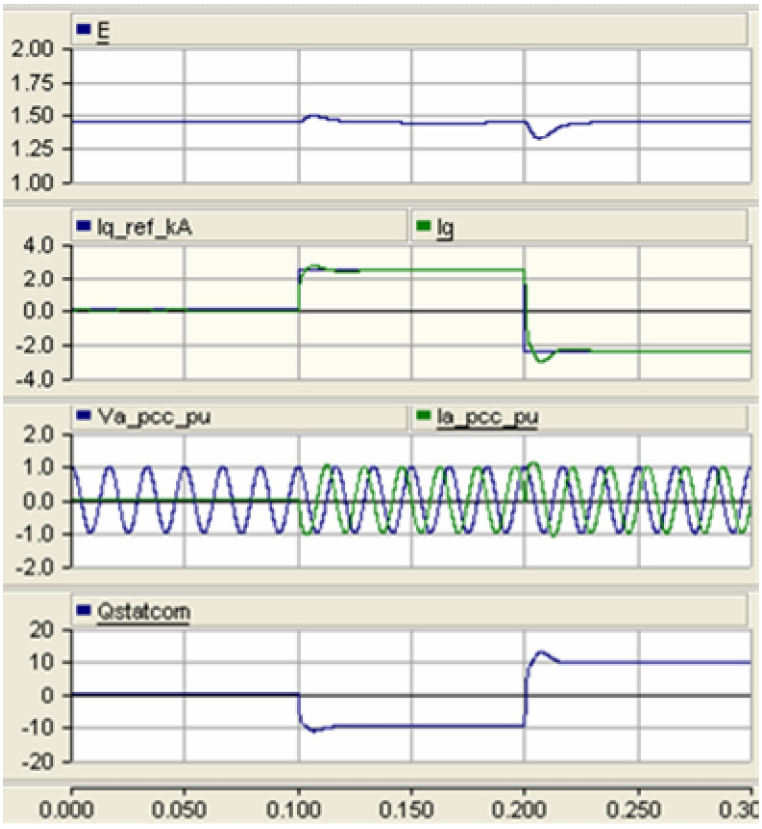
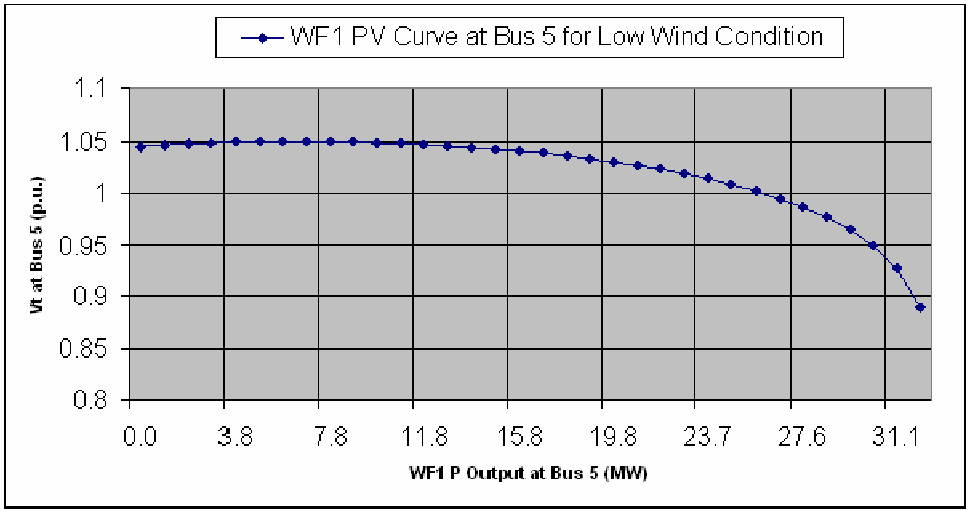


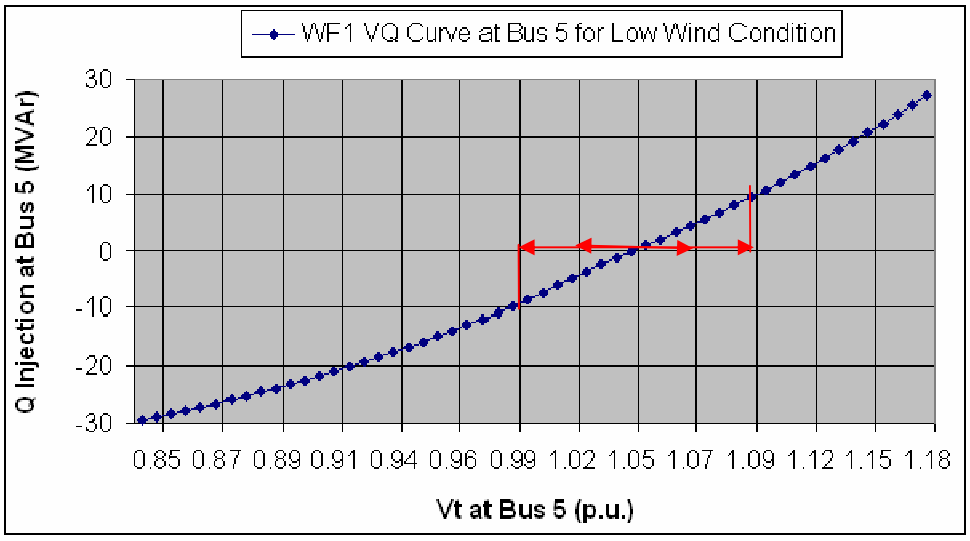
Figure 3-5. Simulation results of the CMC-based STATCOM model.

3.3 System Study and Analysis

With validated system model at the specific operating point, the PV and VQ curve [14][15][16] of WF1 at bus 5 is obtained through the steady-state simulations and is shown in Figure 3-6.



(a)



(b)

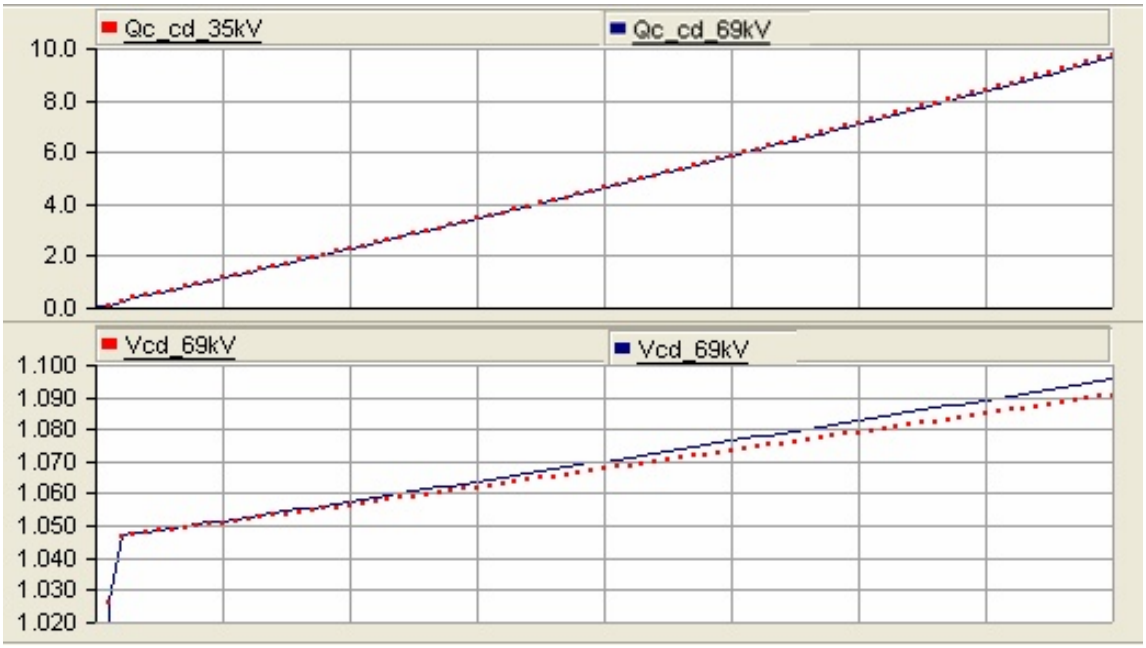
Figure 3-6. Steady-state simulation results: (a) PV curve, and (b) VQ curve.

First, the PV curve at bus 5, where WF1 is connected to the system, is obtained by regulating the WF1 source angle to increase the real power injection at this bus while keeping the rest of the system constant. Figure 3-6(a) shows the PV curve obtained with the nose point of the PV curve located around (32MW, 0.88p.u.). It means that, provided that the WF1 injects the power with a unity power factor at the simulated operating conditions, there is about 30 MW real power injection margin at this bus for voltage stability, which is already far beyond the total rating of 8 online turbines, 4.8 MW, at the specific operating point. Moreover, MSCs at WF1 work as power factor compensators and can further improve the PV curve and extend the WF1 power injection margin from a voltage stability point of view [H7]. Therefore, the voltage stability is not a serious issue for the studied loop system and STATCOM, utilizing its fast response for a cost-effective application, can focus on solving the dynamic voltage fluctuation issue rather than to regulate the steady-state voltage profile.

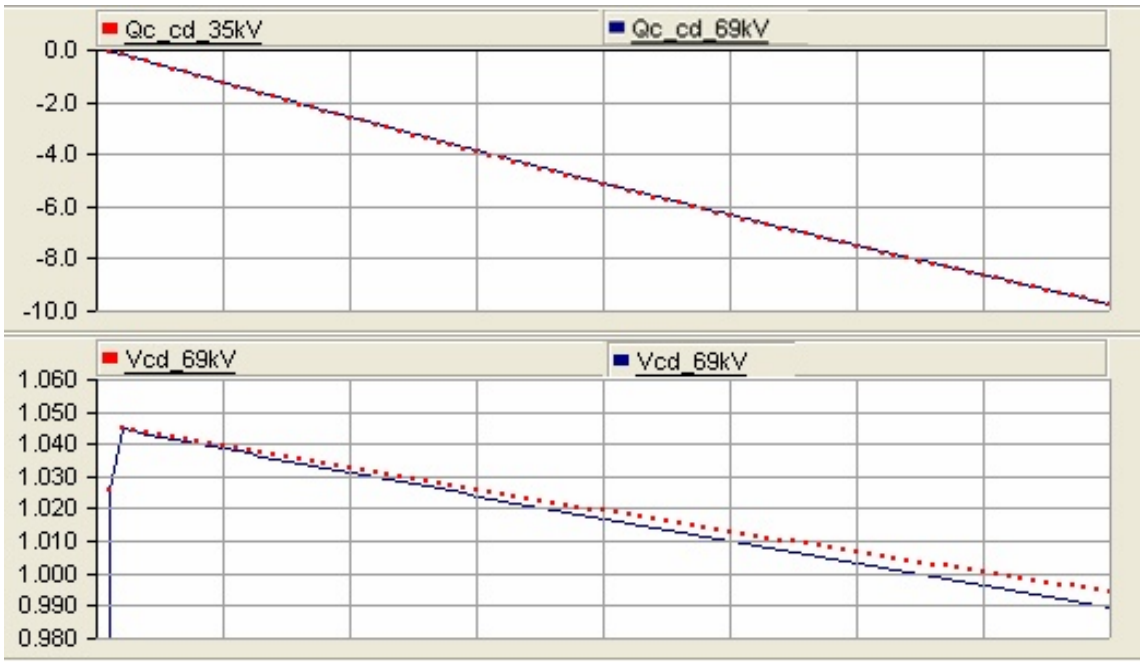
Actually, from a technology point of view, the most effective location to install STATCOM to suppress the voltage fluctuation related to WF1 is just directly at the WF1's point of common point (PCC), which is at 69kV bus 5. In Figure 3-6(b), VQ curve is obtained by injecting Var at bus 5 to evaluate the size of STATCOM. This curve indicates that there is no voltage stability problem at the operating point again, but the sensitivity of the bus voltage to VAR injection is quite high; ±10 MVar injections can cause about ±5% voltage change at the bus. From the year-round data, the most severe voltage fluctuations, which happens rarely, are about ±5%, and most of voltage fluctuations are less than ±1.5%. STATCOM voltage control capability should cover not only typical ±1.5% cases but also the most severe ±5% case. Therefore, a 10MVA STATCOM is a reasonable size to suppress voltage fluctuations at bus 5 covering the most

severe ±5% case, and a STATCOM with the size of 5 MVA is enough to suppress voltage fluctuation for typical ±1.5% cases.

Although bus 5 seems an effective location for STATCOM, if STATCOM can install inside the substation at bus 6, as shown in Figure 3-1, from the practical cost-effectiveness point of view, the additional space for STATCOM need not be planned and the civil works can be significantly reduced so that the cost can be significantly lowered. To compare the STATCOM voltage control capability at different locations, the simulation results with STATCOM respectively installed at bus 5 and bus 6 are shown in Figure 3-7, where the solid line is with STATCOM at 69 kV bus 5, and the dotted line is with STATCOM at 35kV bus 6. Seen from the waveforms, whatever capacitive VAR boosting voltage or inductive VAR bucking voltage off, STATCOM at 35 kV bus 6 has almost the same voltage control capability as STATCOM at 69kV bus5 and the voltage difference between the two locations increases with increasing $|\Delta Q|$. And this voltage difference is just 0.005 p.u. even at the maximum/minimum STATCOM output ±10MVAr. Therefore, a 10MVA STATCOM installed at 35kV bus 6 is still able to suppress voltage fluctuations at bus 5 covering the most severe ±5% case, while a STATCOM with the size of 5 MVA is still enough to suppress voltage fluctuation for typical ±1.5% case. Therefore, considering cost-effectiveness, bus 6 can also be the choice for STATCOM location.



(a)



(b)

Figure 3-7. STATCOM voltage control capability vs. location: (a) (a) capacitive VAR vs bus 5 voltage, and (b) inductive VAR vs bus 5 voltage.

Another simulation has been performed to make a preliminary assessment of the impact of the STATCOM on the system. This simulation involved the dynamic operation of the STATCOM at bus 6 during the 6-hour monitoring period. The proposed STATCOM external control for voltage fluctuation suppression is shown in Figure 3-8. The DC value of bus RMS voltage is substracted from measured RMS voltage, equivalent to feed through a washout filter, so that only the voltage fluctuation part is used as the input to the voltage loop controller. Therefore, STATCOM can adaptively deal with voltage fluctuation independent from the system steady-state voltage regulation by the operations of MSCs and TCs. An additional benefit of this external scheme is that, with a well-designed fast voltage bandwidth utilizing the fast switching capability of ETO switches and the synthesization characteristics of the CMC toplogy, even the relatively faster voltage fluctuations and flickers [C11][H12][H13], due to the switchings of MSCs, blades passing towers [H5], SCIG startups and so on, could be suppressed automatically together with the short-term (seconds to minutes) voltage fluctuations.

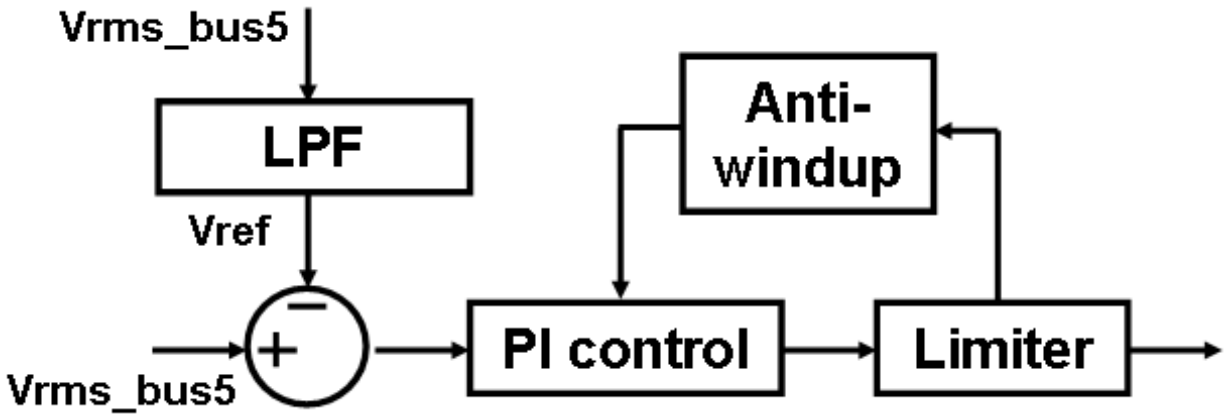


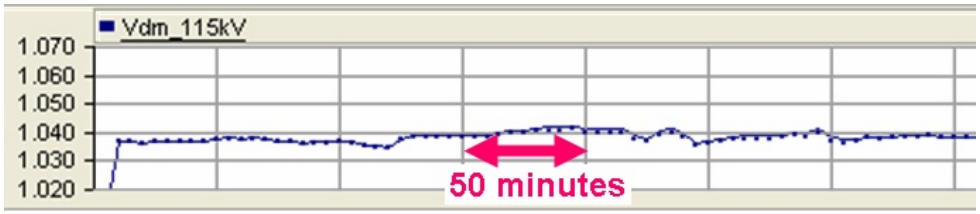
Figure 3-8. STATCOM external controller for voltage fluctuation suppresion.

Figure 3-9 gives the simulation results using STATCOM with its control strategy for voltage fluctuation suppression, where the solid line is without STATCOM and the dotted line is with STATCOM. The STATCOM is located at 35 kV bus 6. Clearly seen from Figure 3-9(a)(b), bus 2 and 3 is almost unchanged even with STATCOM, which is obvious because they are closely connected to a very strong bus 1 with the low impedance of T1 and the short 115kV transmission line. In the Figure 3-9(d), bus 5 voltage fluctuation is almost fully solved, so is bus 6. The reason why voltage fluctuations at bus 6 are slightly larger than bus 5, as is the case with STATCOM, is that the STATCOM control reference is not bus 6 voltage, but bus 5 voltage, though STATCOM is installed not on bus 5 but on bus 6. Shown in the Figure 3-9(c)(e)(f), the voltage fluctuation at other 69kV buses are all suppressed considerably as well, and the extents of suppression are dependent on how these buses are close to bus 5 as the suppression is more at the close bus 4 and 8, and less at the far bus 11. Therefore, these dynamic simulation results verify the previous analysis and assessment based on steady-state PV and VQ curves, and the effectiveness of STATCOM and its control strategy for voltage fluctuation suppression.

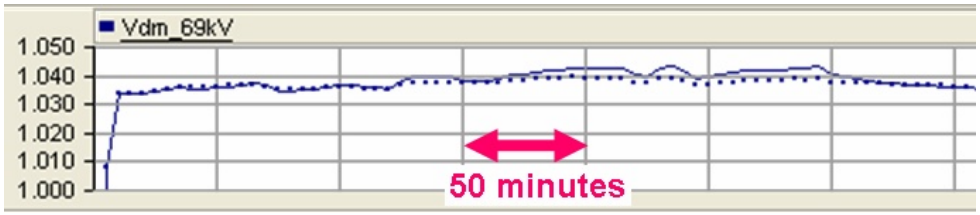
In addition, since the STATCOM suppresses the voltage fluctuation, it is apparent that, compared to the case without STATCOM, the switching times of MSCs and TCs of both main transformers and load transformers to address the voltage fluctuation issue in the system shall be significantly reduced. Therefore, the maintenance and replacement cost of MSC, TC and wind turbines can be lowered, and the power quality issues related to the switching of MSCs and TCs can also be lessened.



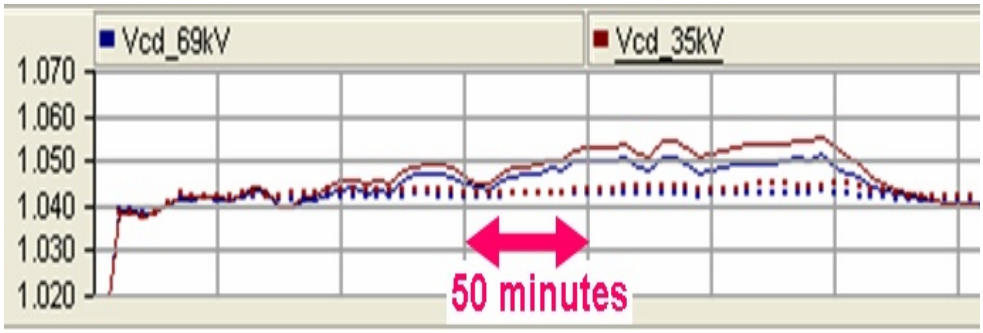
(a)



(b)



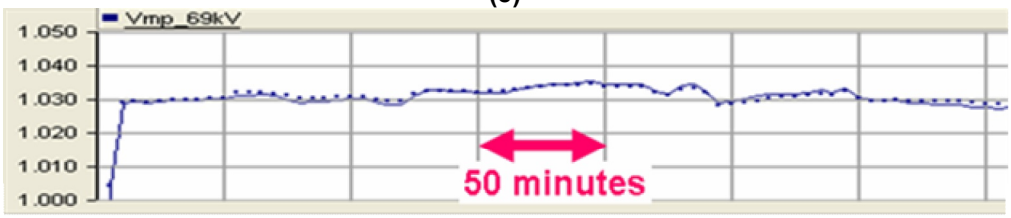
(c)



(d)



(e)



(f)

Figure 3-9. comparison voltage fluctuation with or without STATCOM: (a) bus 2 voltage, (b) bus 3 Vvoltage, (c) bus 4 voltage, (d) bus 5 and 6 voltage, (e) bus 8 voltage, and (f) bus 11 voltage.

3.4 Conclusion

This paper describes the methodology to conduct an impact study of a STATCOM on the integration of a large wind farm into a weak loop power system. The specific issues and solutions of the studied wind farm system are illustrated. For the system study, the models for the system, wind farm and STATCOM are developed, and the system model has also been validated with field data.

From obtained PV and VQ curves from the simulation, the size and location of STATCOM and the system stability are assessed. It indicates that while low-cost MSCs and TCs boost the steady-state voltage locally but are ineffective to suppress the voltage fluctuations (seconds to minutes) due to their nature of a slow dynamic response, a 10MVAr STATCOM, which is a small percentage of wind farm rating, can not only effectively suppress the voltage fluctuations of the wind farm and the whole 69kV loop system, but also inherently reduce the operation times of MSCs and TCs in the system so that the maintenance and replacement cost of MSCs, TCs and wind turbines can be reduced, and the power quality issues related to the switching of MSCs and TCs can also be lessened. The results also show the location of STATCOM selected at 35kV bus 5, the secondary side of the wind farm main transformer, can be a good tradeoff from a cost-effectiveness point of view.

For this specific application of suppressing the voltage fluctuations, the dynamic simulation results for a continuous operation period also verify the effectiveness of the proposed STATCOM and its control strategy, which can adaptively deal with voltage fluctuation independent from system steady-state voltage regulation by the operations of MSCs and TCs, and can even possibly mitigate the faster voltage fluctuations and flicker emissions from wind

farms with a well-designed fast control bandwidth. Therefore, the effectiveness of the installation of a 10MVAr STATCOM system for integrating the specific 50MVA wind farm into the weak loop power system is verified.

Chapter 4 ELECTRIC ARC FURNACE FLICKER MITIGATION

As been introduced in section 1.1, the CMC-based STATCOM is considered a suitable FACTS unit for EAF flicker mitigation, which is one of the most common power quality issues irritating nearby customers. However, how to economically and efficiently mitigate EAF flicker utilizing STATCOM is not straightforward and conclusive yet. In the chapter, the study of a CMC-based STATCOM for flicker mitigation, whose single-line diagram is shown in Figure 4-1, will be presented. Firstly, as the specific case, a CMC-based STATCOM is proposed to evaluate the performance of its EAF flicker mitigation for a practical 40 MVA arc furnace in Tennessee. A steady-state analysis is conducted to assess the size of STATCOM. Based on the field data recorded at the electric system surrounding the EAF, the flicker issue and reactive power compensation requirement are further quantitatively analyzed. The extensive simulations based on the field data are conducted to study the system performance and cost-effectiveness for flicker mitigation, which verifies the steady-state study and gives the guideline for STATCOM sizing and performance estimation.

Furthermore, the models of a CMC-based STATCOM and an EAF flicker are introduced. And based on the DQ-axis model of a CMC-based STATCOM and an EAF flicker, the model-based control strategy is proposed to mitigate the voltage fluctuation at PCC. The satisfactory stability margins and transient performance are earned through the s-domain control design. The simulation and experiment results in a scaled-down TNA system are used to verify the model and controller.

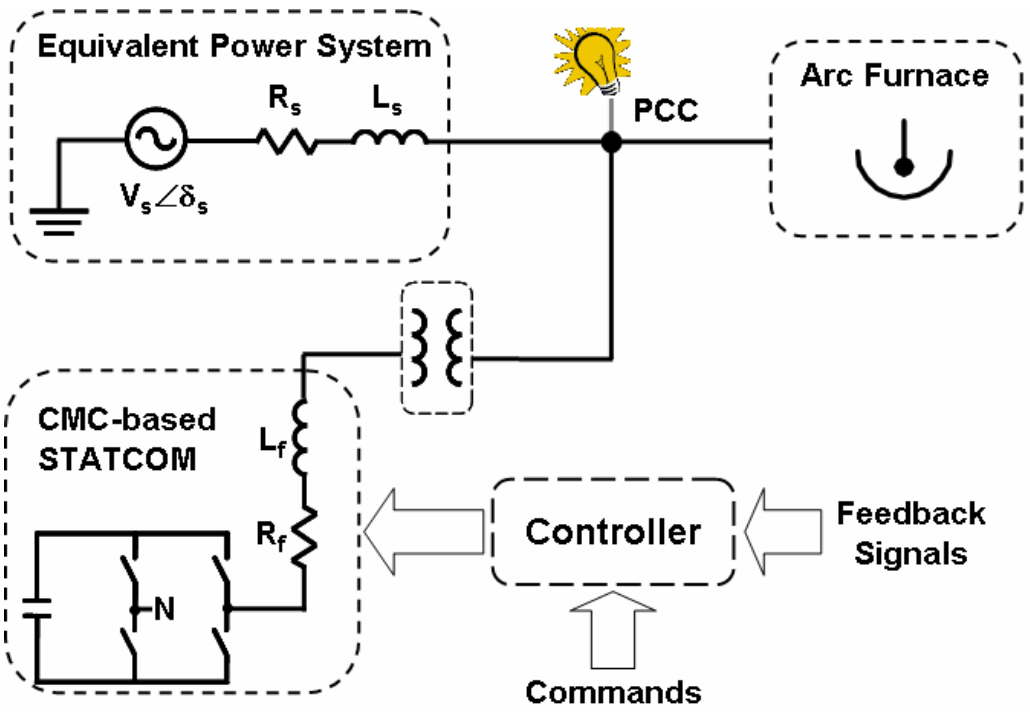


Figure 4-1. One-line diagram of a CMC-based STATCOM and EAF system

4.1 Case Description and Steady-state Analysis

For a 40 MVA arc furnace in Tennessee, shown in Figure 4-2, the flicker can be summarized below from the field recorded PQ data at the 161kV bus: (1) flicker frequency: around 5Hz; (2) flicker magnitude (ΔV/V): around 1%; and (3) source Xs/Rs: around 3 [C8][C13].

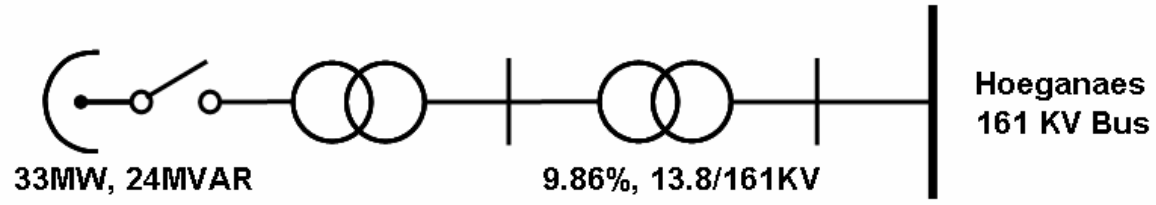


Figure 4-2. Hoeganaes arc furnace

Since the 1% flicker is beyond the IEEE irritability threshold curve of IEEE standard shown in

Figure 4-3 [C9], a mitigation device has to be applied to decrease flicker into an acceptable range.

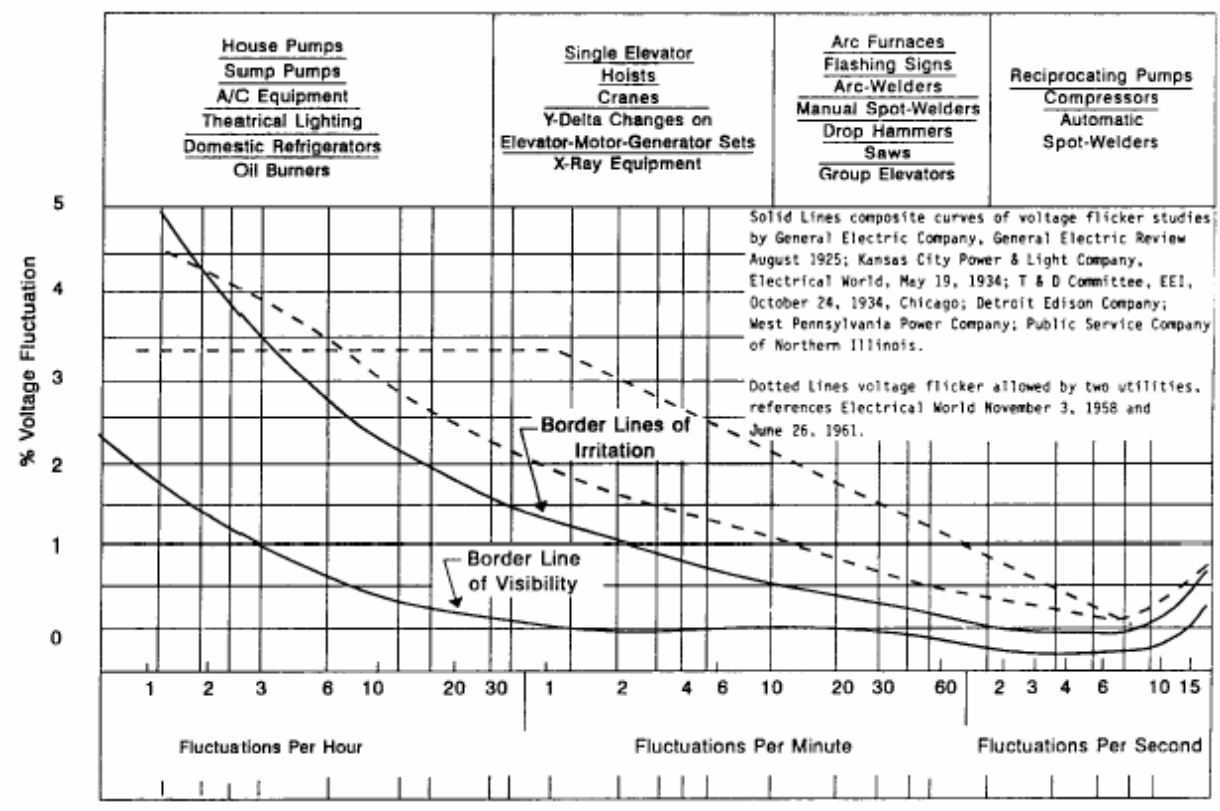


Figure 4-3. Maximum permissible flicker in IEEE standard

For the reactive power compensation, the system steady-state diagram is shown in Figure 4-4. The system voltage and impedance are V_S and X_S. When arc furnace consumes power P_L and Q_L, the voltage of PCC is decreased from the original value to V_{PCC}. To compensate the

voltage of PCC back to V'_{PCC}, the injected reactive power at PCC has to be Q_C. Based on the assumption that the angle between V_S and V_{PCC} is small, the relationship among Q_C, X_S, V_{PCC} and V'_{PCC} can be derived as below:

$$Q_c \approx \frac{V'_{pcc}\left(V'_{pcc} - V_{pcc}\right)}{X_s}$$

Equation 4-1

where X_S is the system impedance, V_{PCC} is the original voltage with EAF, V'_{PCC} is the voltage after reactive power compensation, and Q_C is the injected reactive power at PCC.

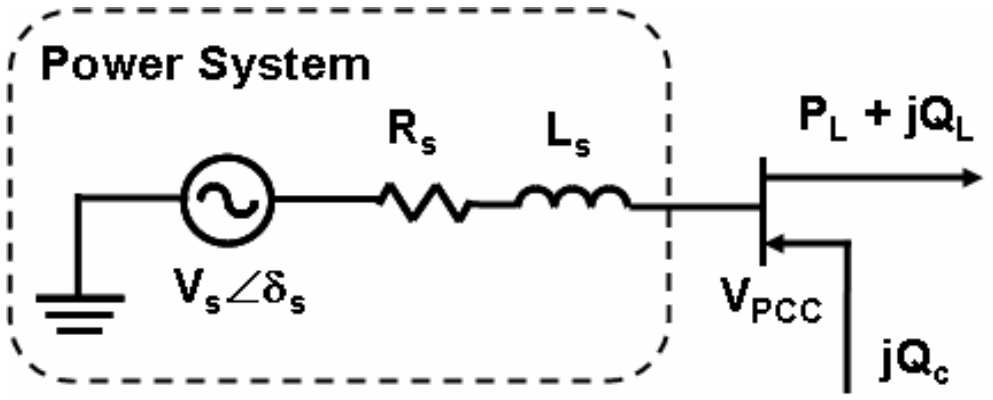


Figure 4-4. Reactive power compensation

Based on Equation 4-1, the normalized relationship among flicker magnitude ($\Delta V_{PCC}/V_{PCC}$), STATCOM capability (Q_C/S_{EAF}), and system X/R ratio (X_S/R_S) is plotted into Figure 4-5. As shown in Figure 4-5, a 4.5MVA and 30MVA STATCOM can mitigate flicker by 20% and 80% respectively, which means the flicker can be fully mitigated into the acceptable range if a 30 MVA is utilized.

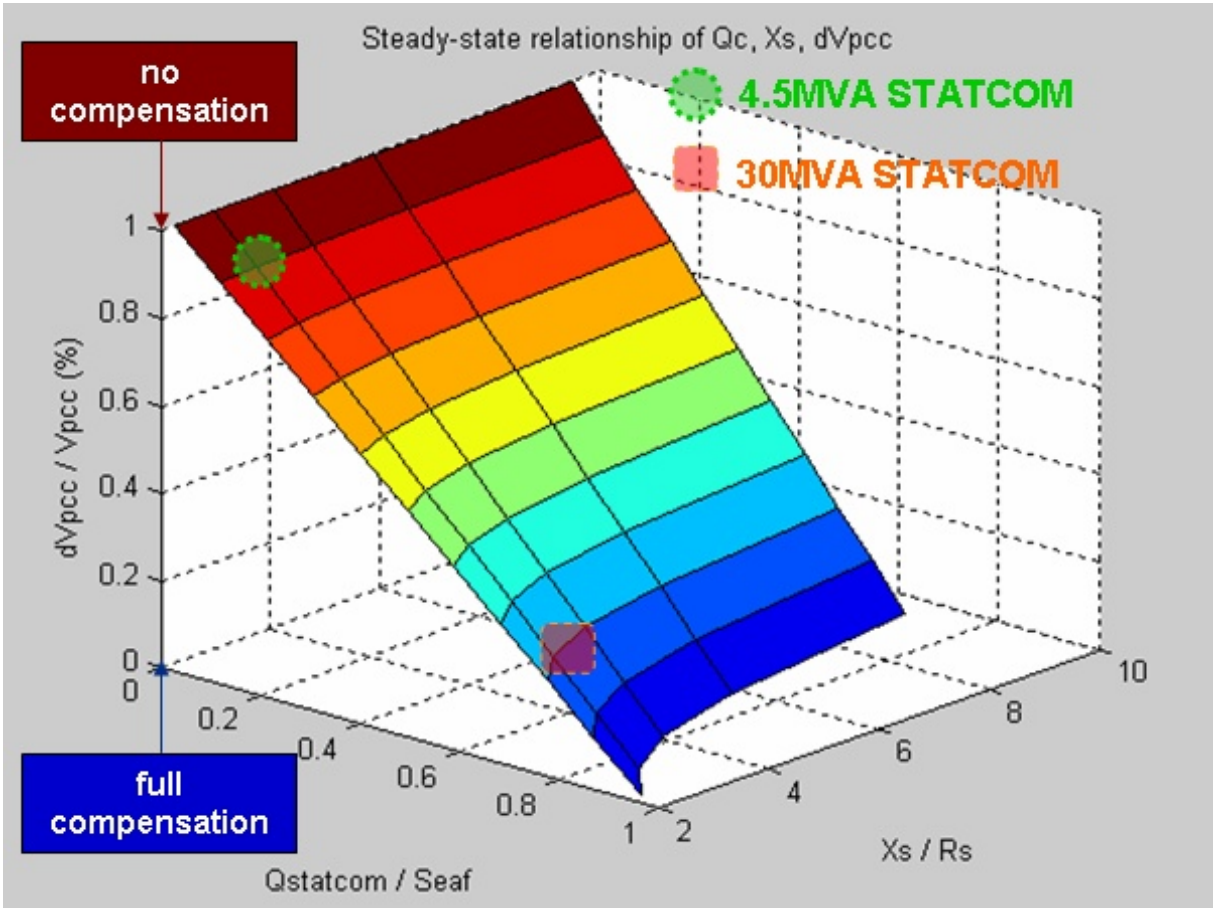


Figure 4-5. Normalized $\Delta V_{PCC}/V_{PCC}$ (Q_C/S_{EAF}, X_S/R_S)

Moreover, offline simulation in PSCAD/EMTDC environment demonstrates the compensation performance for different STATCOM ratings, and results are shown in Figure 4-6. Moreover, the simulation results for different Xs/Rs are also summarized in Figure 4-7. Seen from Figure 4-5 and Figure 4-7, the analysis results and simulation results match each other very well.

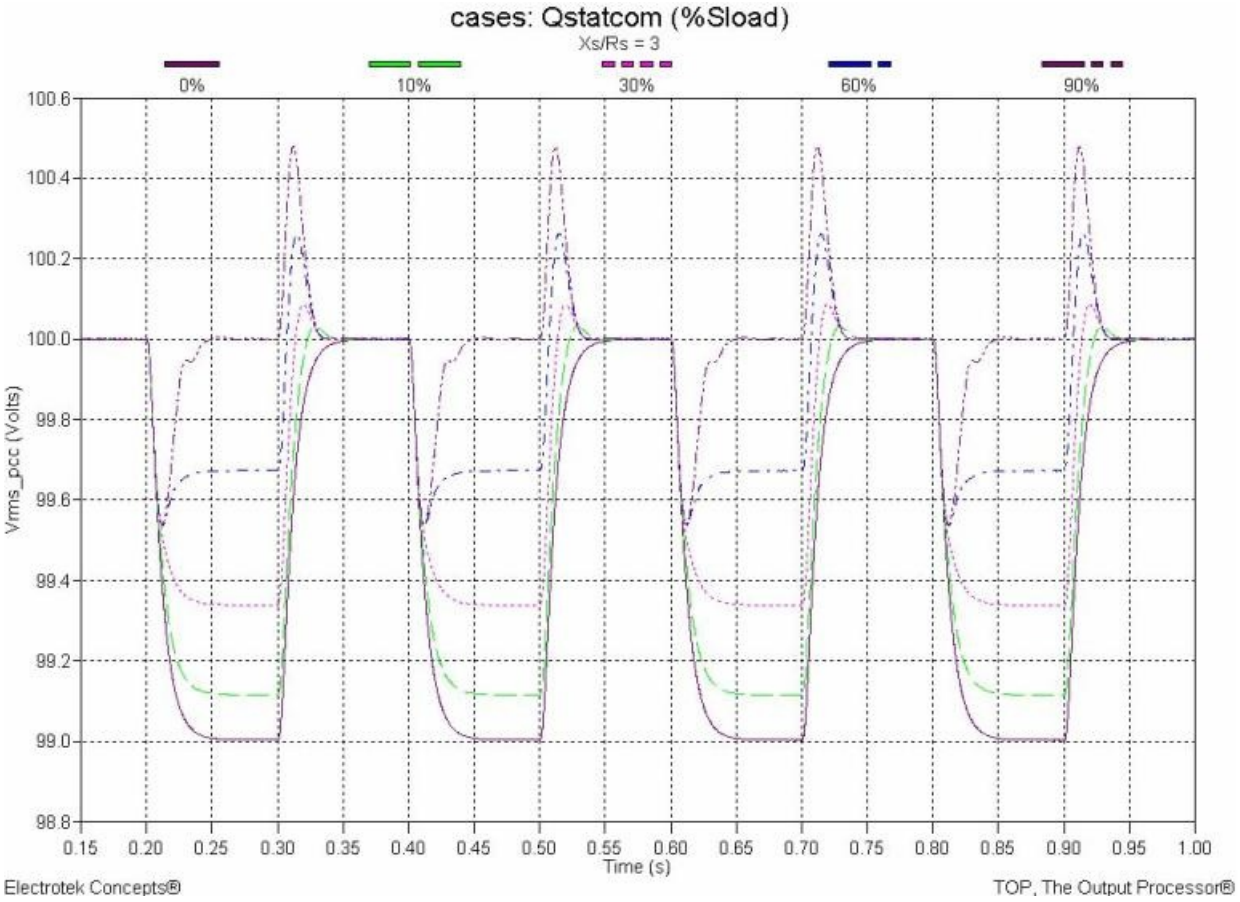


Figure 4-6. PSCAD/EMTDC simulation results

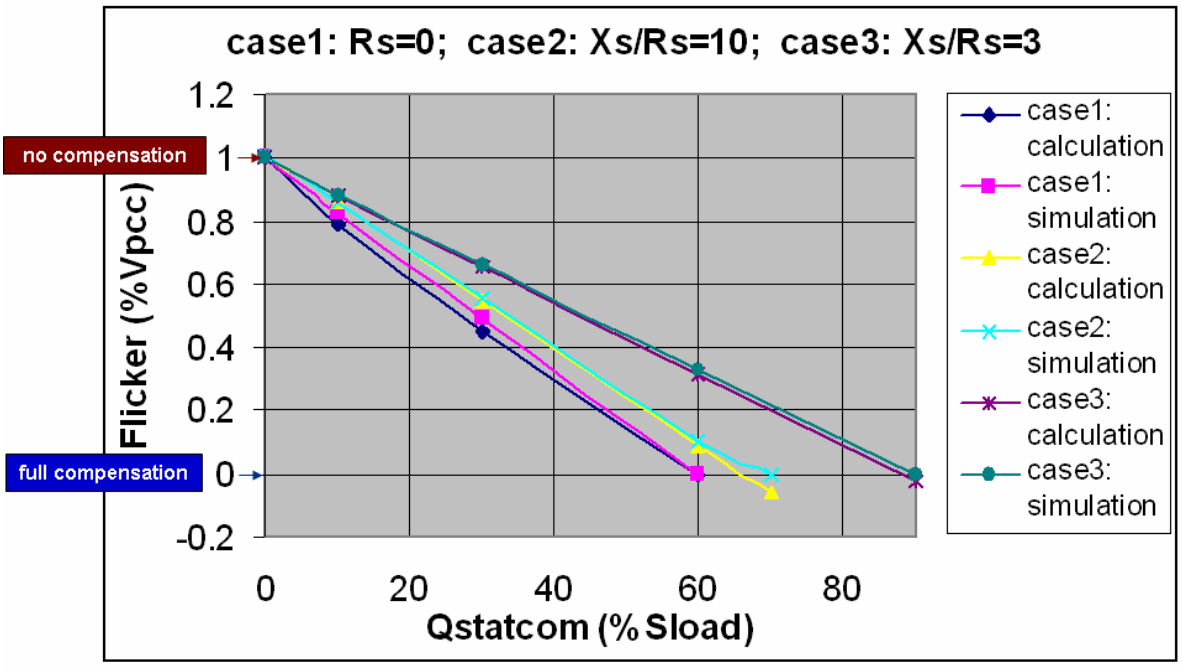
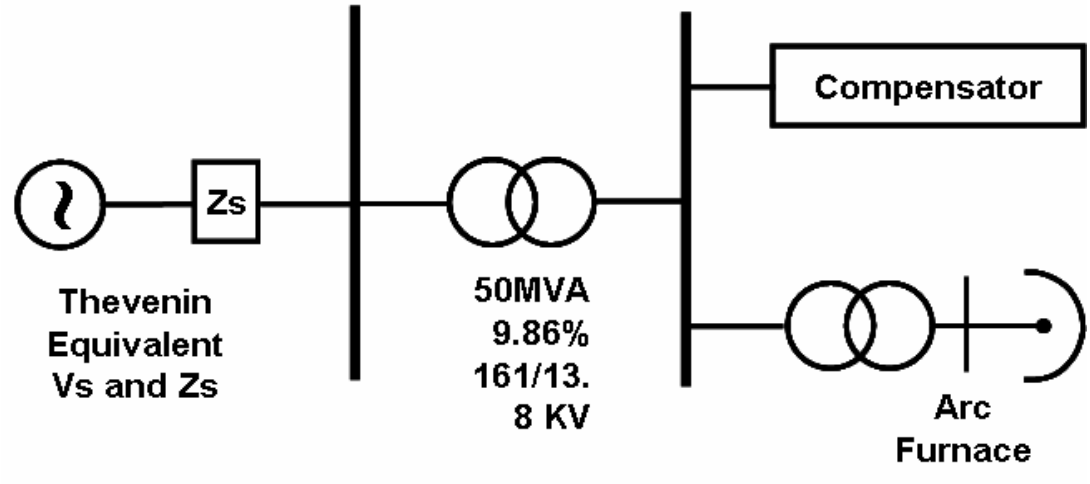


Figure 4-7. Calculation and simulation results

4.2 Field Data-based Study

I. Problem Description

The one-line diagram of the studied system is shown in Figure 4-8(a). The 45 MVA arc furnace is connected from local feeder to a 13.8 kV bus and then to 161 kV transmission line through a 50 MVA 161/13.8 kV transformer. The compensator is planned to be installed on the EAF 13.8kV bus for flicker mitigation and an operating furnace picture is shown in Figure 4-8(b) [C14].



(a)



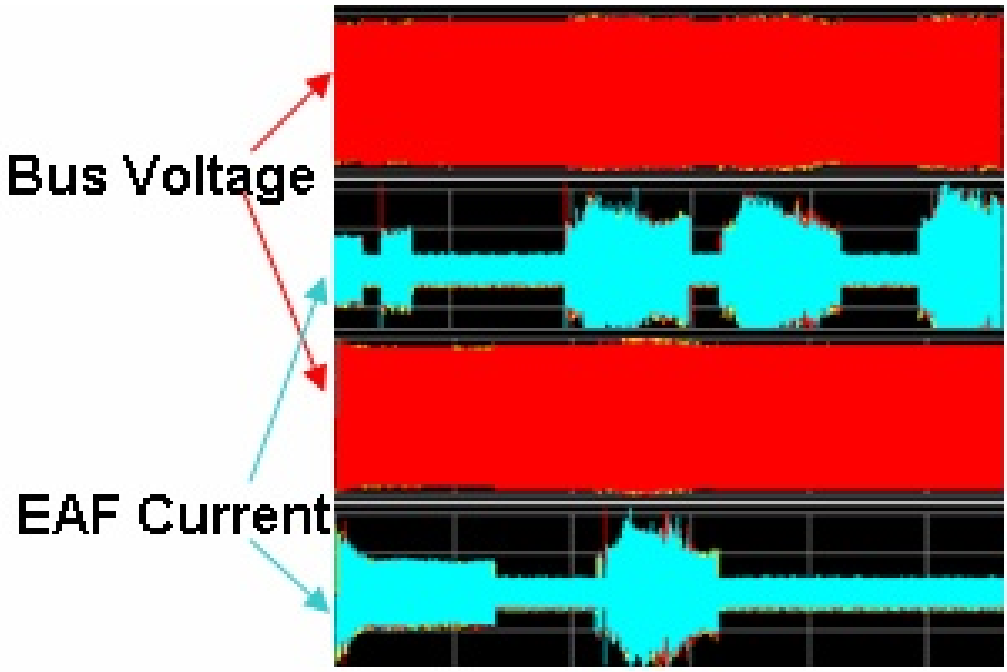
(b)

Figure 4-8. 45 MVA electric arc furnace: (a) one-line diagram, and (b) furnace photo.

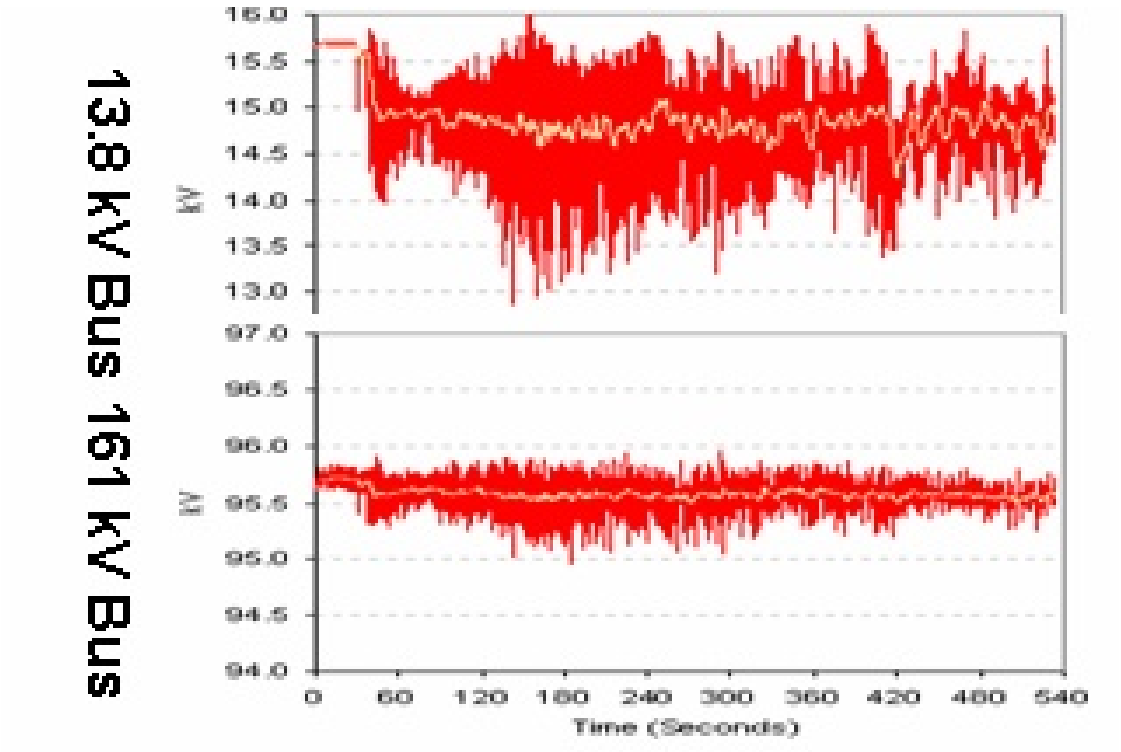
Typically, the two EAF major processes are melting and refining [1]. During these two processes, the EAF's electrode is short-circuited to scrap metal and consumes the time-varying power, which is mainly dependent on arc length. Normally, each of these two processes operates 20~40 minutes with stops and starts. Figure 4-9 (a) shows a two-hour selected instantaneous voltage and current measurement from the operating EAF. Seen from the waveforms, the time-varying EAF currents cause the EAF voltage magnitude fluctuations, especially in the melting and refining processes with large currents.

Actually, very small voltage fluctuations are enough to induce flicker for human eyes. For a standard 60W incandescence lamp, the flicker can be perceptible for a voltage fluctuation around 10Hz and 0.3%. Unfortunately, the EAF operation generates the voltage fluctuation just at this flicker-sensitive frequency range. There is the flicker threshold of irritability curve in IEEE and UIE standard [3]. For the most sensitive flicker frequency 1Hz~20Hz, the voltage fluctuations have to be less than 3% to be acceptable for residential lighting.

For a zoom-in view, a 9 minutes data of voltage at 13.8kV and 161 kV are extracted from the data shown in Fig. 2(a) and their RMS values are calculated and plotted in the Fig 2(b). Obviously, the voltage fluctuation is as large as 13% at 13.8 kV, and because of transformer impedance, the voltage fluctuation is suppressed at 161 kV but still around 1%, both of which are above the threshold allowed by IEEE/UIE standard and need be mitigated to an acceptable level.



(a)



(b)

Figure 4-9. EAF field data: (a) 2hrs current and bus voltage, and (b) 9mins extracted bus voltage.

For the detailed view, 1sec worst-case data during melting process with the maximum peak current is extracted. And from the line-to-line voltages and phase current recorded at EAF 13.8 kV bus, the instantaneous real power and reactive power at EAF 13.8 kV bus is calculated and plotted in the Figure 4-10. Seen from Figure 4-10, one can see that the power consumed by EAF include a constant real power P_0 = 35 MW with fluctuating real power ΔP_{max} = ± 20 MW, a constant reactive power Q_0 = 14 MVAr with fluctuating reactive power ΔQ_{max} = ± 35 MVAr.

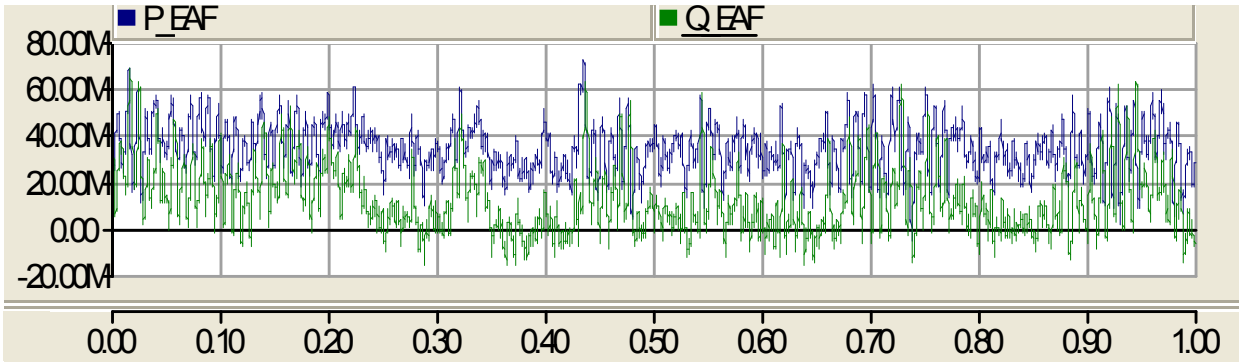


Figure 4-10. Worst-case EAF instantaneous real and reactive power.

II. Soluion Comparison

From power flow point of view, the basic principle of flicker mitigation solution can be simply explained as shown in the Figure 4-11. The power consumed by EAF can be regarded as a constant power (P_0, Q_0) plus a fluctuating power (ΔP, ΔQ). Generally, P_0 affects the angle stability, Q_0 affects the bus voltage profile, voltage stability, and load power factor; ΔP is mainly

related to the fluctuations of bus voltage angle; ΔQ is mainly related to the fluctuations of bus voltage magnitude. To solve the EAF power quality issues, ideally, it is obvious to compensate Q_0, ΔP and ΔQ so that the supply only provides the constant P_0 with a unity power factor, and, thereby, the bus voltage magnitude and angle is kept invariable. However, because of cost-effectiveness and other factors, Q_0, ΔP and ΔQ cannot be fully compensated, but only mitigated to an acceptable level in the real world. Particularly, ΔP mainly affects the voltage angle other than flicker and requires expensive source or energy storage for compensation, which is not within the scope of this chapter.

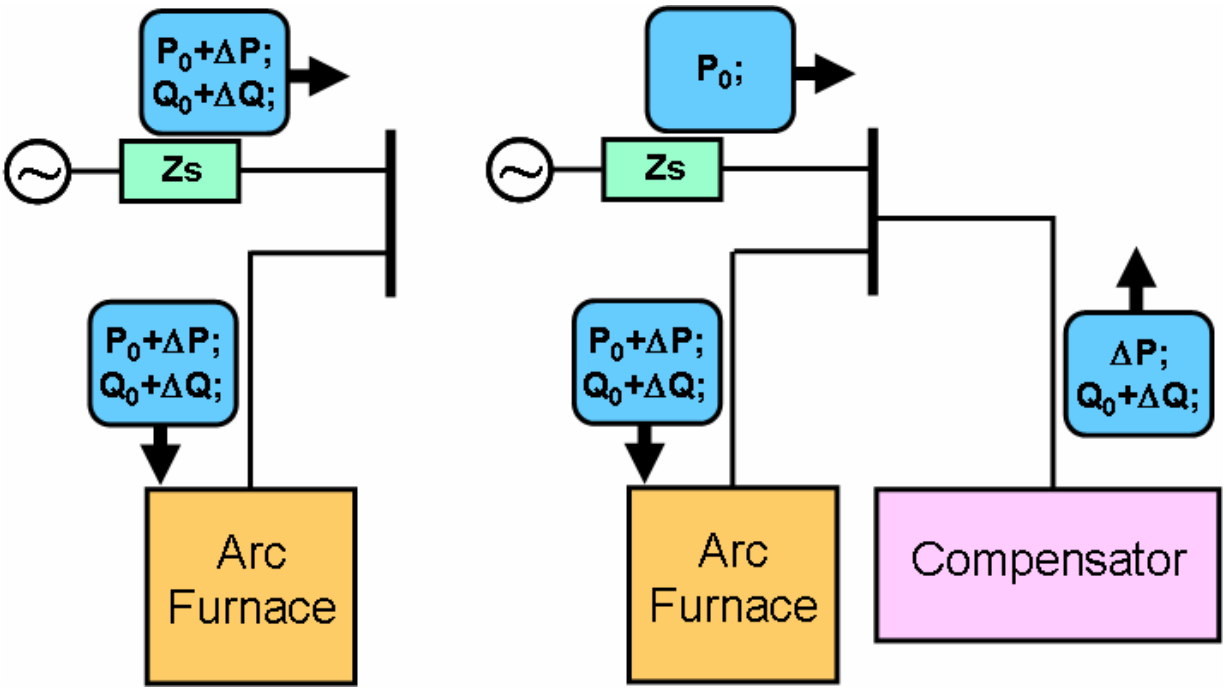
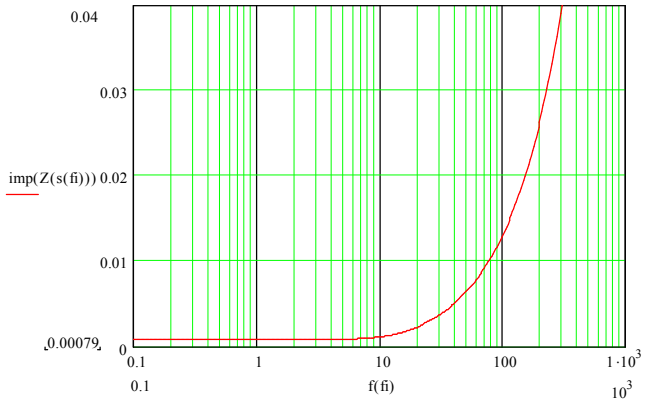


Figure 4-11. EAF compensation block diagram: (a) EAF without compensator, and (b) EAF with compensator.

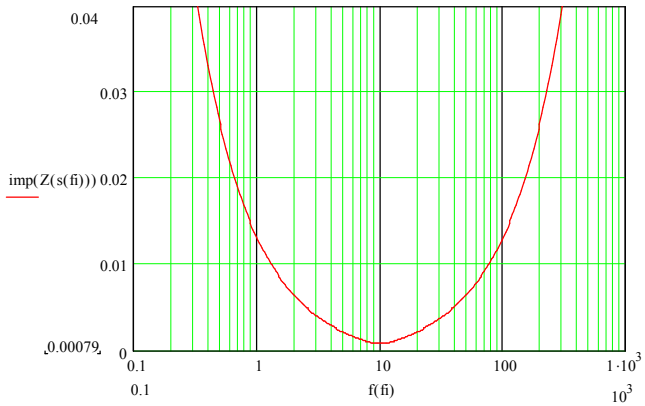
How to economically and efficiently mitigate EAF flicker is consistently a tough issue for utility and industry professionals. The basic methodology for flicker mitigation can be categorized into three types: (1) Passive filters, which can be either series or shunt [G4]. Though passive filters are simple, reliable, low-cost and highly efficient, it is difficult to design for a stiff system, time-consuming for tuning, easy to induce resonance, and susceptible to system impedance variations. Particularly, in this case, two 2^{nd} order passive filters are designed for flicker mitigation, shown in Figure 4-12. The filter impedance at 1Hz~20Hz has to be small enough to force flicker current to flow through the filter path. However, since flicker frequency is very close to fundamental frequency, a 2^{nd} order filter cannot be sharp enough to behave as a high impedance for 60Hz, and hence has to be replaced by a high-order passive filter. Contradictorily, high-order passive filter is complex, non-economical and seldom used. (2) Series active compensator, such as the series impedance regulation [C2]. Although, to some extent, the increasing series reactance can mitigate the flicker, it results in the voltage reduction and therefore decreases EAF productivity. Moreover, it is also expensive and laborious to control upstream transformer reactance or series reactor in the firmer deregulation power system. (3) Shunt active compensator, such as SVC and STATCOM. SVC can improve system power quality, and also increase EAF productivity and provide additional economic benefits. However, it cannot react to the fast-varying flicker (1Hz~20Hz) very well with the inherent limit of relatively low bandwidth and hence its dynamic performance for flicker mitigation is limited. The state-of-the-art solution is the STATCOM based on high frequency switching voltage-source-converter (VSC). While SVC performs as a controlled reactive admittance, STATCOM functions as a synchronous voltage source. With the currently available high-power semiconductor devices, such as IGBT, IGCT, ETO, the STATCOM can switch at 1~3 kHz and

achieve a close-loop bandwidth of 100~300 Hz. Therefore, the STATCOM response time is less than one cycle and follows the fast-changing flicker well. Moreover, STATCOM can also provide real power compensation if interfaced with an energy storage unit. All of these features are unattainable for SVC, and with these benefits, STATCOM performs significantly better than SVC [C4].

At present, STATCOM is considered as the most suitable FACTS device for flicker mitigation [8]. Therefore, in the following, the study will focus on STATCOM as compensator.



(a)



(b)

Figure 4-12. Passive filter impedance for EAF flicker mitigation: (a) 2nd order low pass filter, and (b) 2nd order band pass filter.

III. Modeling and Control for Field Data-based Study

For the field-data based study, an EAF model, shown in Figure 4-13, is proposed for a continuous and practical case study.

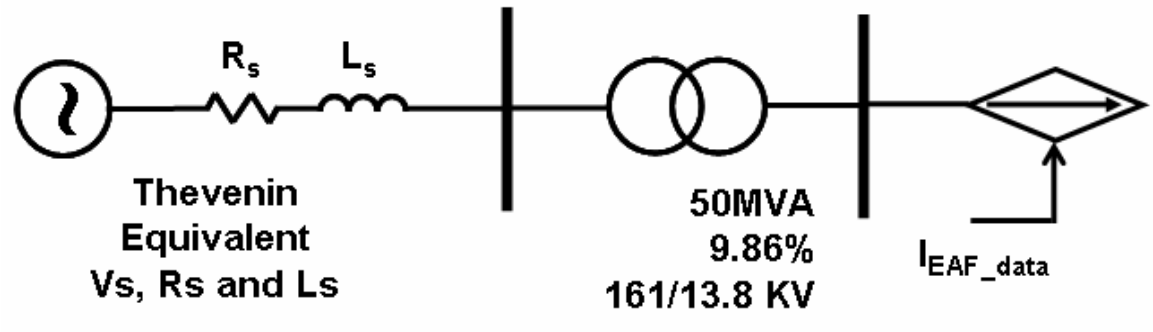


Figure 4-13. Field data based EAF model.

From the extracted EAF instantaneous currents and bus voltages with 10 kHz sampling frequency and derived instantaneous power shown in Figure 4-10, the thevenin equivalent source Rs and Ls can be obtained. Through modeling EAF as an EAF current data controlled current source, a model is implemented into PSCAD/EMTDC simulation software. Figure 4-14 shows the Vpcc waveform in the simulation and the field data. When compared with each other, they match very well except for the high-frequency harmonics, which are filtered out in the field data Vpcc. Therefore, the field data-based EAF model is validated.

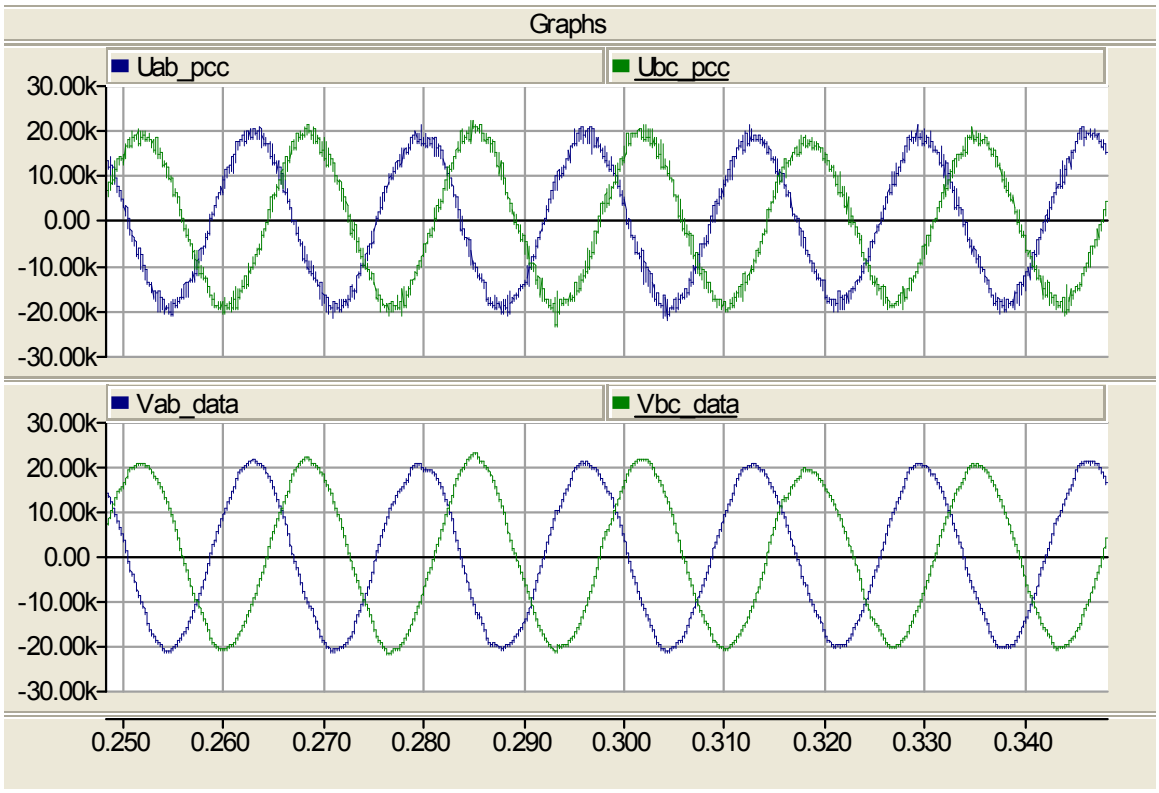


Figure 4-14. Simulation results VS. field recorded data.

For the modeling and control of STATCOM, the CMC-based STATCOM and its internal control are introduced in Chapter 2 and respectively shown in Figure 2-1 and Figure 2-8. With the developed model and controller, a 4.5MVA 3-level and 30 MVA 13-level CMC-based STATCOM, which individually comprises one and six cascaded 1.5 MVA H-bridge VSC per phase, is designed following the control design guideline in the section 2.2. Their simulation results are respectively shown in Figure 2-19 and Figure 4-15, which illustrate that, during the reactive current I_q channel step response, I_q responds in a subcycle, I_d and I_q channels are decoupled controlled, and the DC bus voltages maintain stable.

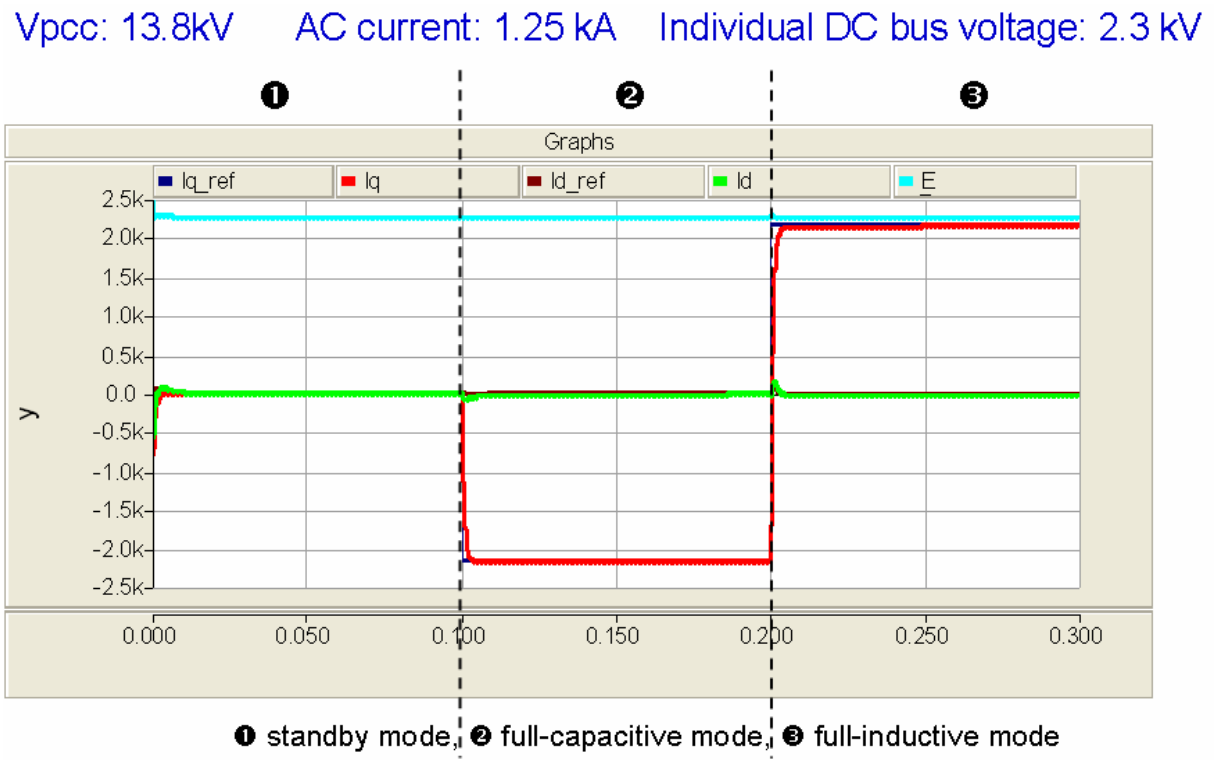


Figure 4-15. 30MVA STATCOM average model simulation results.

Since the purpose here is to study the STATCOM performance under the practical EAF condition, the conventional direct EAF load current feedback methods other than the close-loop control method in the next section is adopted. For the reactive current reference, three methods are compared, which are EAF I_q direct feedback method, EAF fluctuating I_q feedback method, and EAF scaled fluctuating I_q feedback method with $Q_{STATCOM}/Q_{EAF}$ ratio. Seen from Figure 4-16, the EAF fluctuating Iq feedback method can most mitigate the fluctuating reactive power of EAF, and have the best effect on flicker mitigation, therefore, we adopt this design.

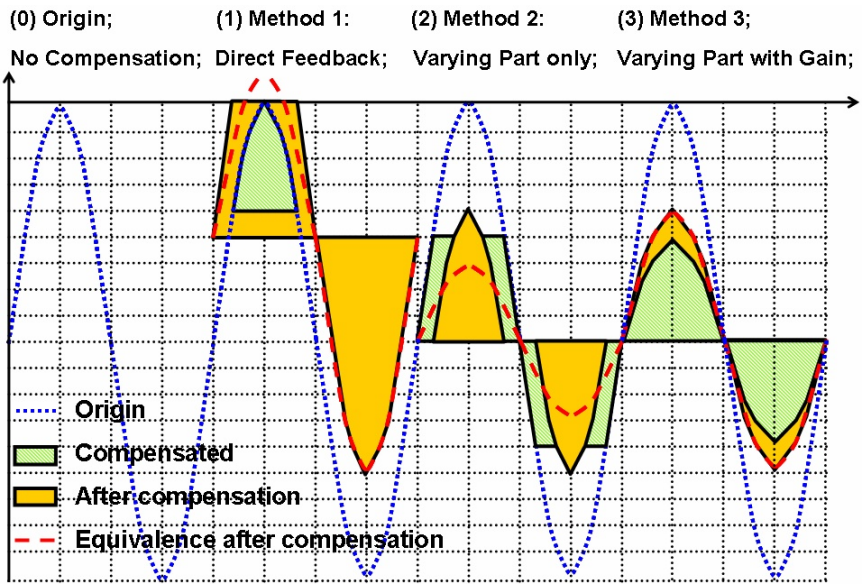


Figure 4-16. Iq reference feedback methods.

IV. Case Study

The simulation results for several cases are presented for the integrated EAF and STATCOM model as shown in Figure 4-17(a)~(d). Case 1: 4.5 MVA STATCOM case. Since the STATCOM is rated 10% of S_{EAF} (45MVA), V_{pcc} voltage fluctuation is not distinctly mitigated as shown in Figure 4-17(a); Case 2: 4.5 MVA STATCOM with 14 MVAr capacitor bank. Capacitor bank compensates the constant Q_0 of EAF load and improves the load power factor. Therefore, STATCOM compensates for the dynamic fluctuating ΔQ only. As shown in Figure 4-17(b), with capacitor bank, the source steady-state reactive current is almost zero and the flicker is slightly further reduced compare to case 1. Case 3: With a 30 MVA rated STATCOM, the fluctuating part of supply reactive current is smaller and the flicker is significantly reduced and is below the flicker threshold of 3%, as shown in Figure 4-17(c). Case 4: With a 30 MVA STATCOM and a 14 MVAr capacitor bank, the flicker is well below 3%, which is shown in Figure 4-17(d). Furthermore, the steady-state load power factor is unity and the bus voltage regulation is improved.

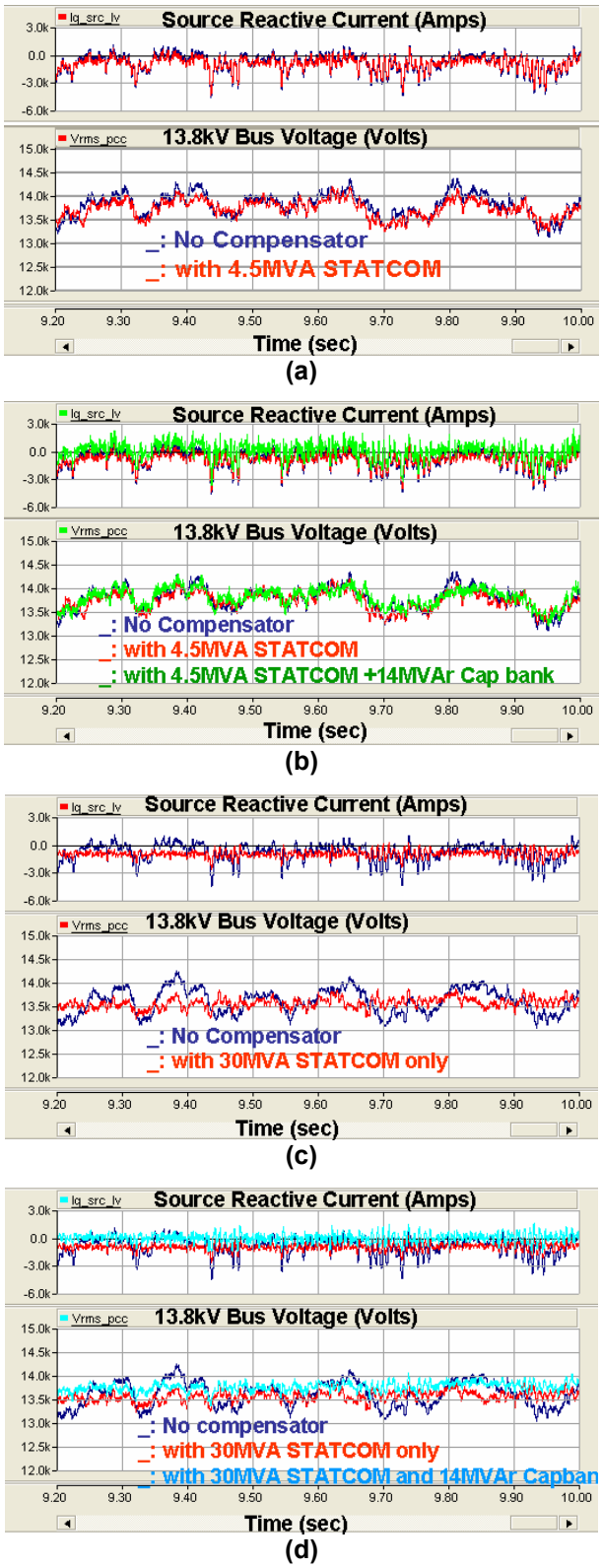


Figure 4-17. Case study: (a) case 1: 4.5 MVA STATCOM, (b) case 2: 4.5 MVA STATCOM with 14 MVAr cap bank, (c) case 3: 30 MVA STATCOM, and (d) case 4: 30 MVA STATCOM with 14 MVAr cap bank.

In this section, based on the field data from 45 MVA EAF installed at TVA, the flicker mitigation and reactive power compensation requirements are quantitatively analyzed. The various compensation solutions are qualitatively compared, such as the passive filter, SVC, and STATCOM. In addition, a field data-based EAF model is proposed and validated by simulation results. The simulation results based on field data show that a 4.5MVA rated STATCOM can, to some extent, mitigate voltage flicker caused by an 45 MVA EAF, whereas a 30 MVA rated STATCOM can completely mitigate the voltage flicker. The additional 14MVAr capacitor bank with the STATCOM improves the load power factor and bus voltage profile. These simulation results verify the steady-state analysis results in the section 4.1. The effectiveness of STATCOM-based flicker compensator is also validated by the simulation.

4.3 Modeling and Control of STATCOM for EAF Flicker Migitation

The model and internal control strategy of STATCOM has been dedicately presented in the previous chapter. For the EAF, historically, there are various methods to model an arc furnace, such as an arcing resistance model, a harmonics accumulation model and a frequency domain method [C5][C6][C7]. These methods can meet the non-linear v-i curve, stochastic and even chaotic characteristics of EAF; therefore, they are satisfactory for the purpose of flicker harmonics analysis. However, for the control design and stability study, a deterministic model needs to be developed.

In our work, a worst-case behavior model composite by switching passive loads, shown in Figure 4-18, is proposed to model EAF flicker [C10][C11]. For any specific case, this model can perform similar impedance as a real-world arc furnace and, therefore, produce similar flicker at PCC. And because of its definite impedance, it is suitable for stability analysis and s-domain

control design. With the model, the flicker characteristics can be approached from four aspects: (1) flicker frequency; (2) flicker magnitude (ΔV/V); (3) source Xs/Rs; and (4) arc furnace power factor.

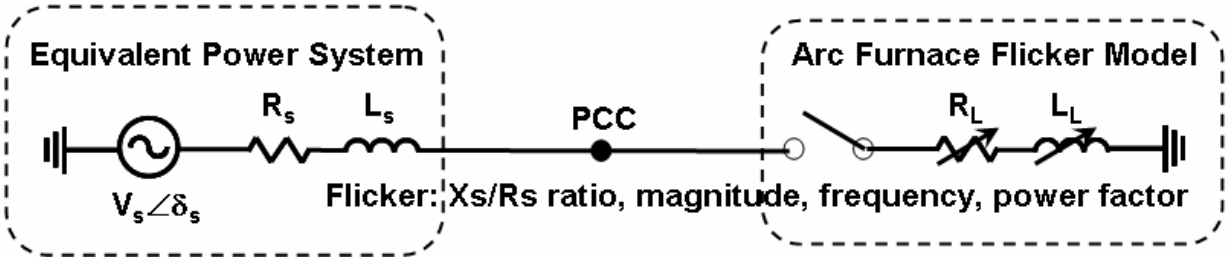


Figure 4-18. EAF flicker worst-case model

As shown in Figure 4-19, the one-line system diagram illustrates how the system and control functions work. The STATCOM control objective is to mitigate voltage fluctuation at PCC caused by an arc furnace load by compensating for the reactive power at the local coupling point. CMC-based STATCOM is controlled through two-loop structure. Two current internal loops, Id-loop and Iq-loop are decoupling controlled and designed with hundreds Hz bandwidth and adequate stability margins. Id reference is responsible for charging/discharging the DC capacitor and therefore is regulated by a voltage loop to maintain the DC-bus voltages. Iq reference is the reactive current command, which is connected with external controller for flicker mitigation. The external control employs the reactive current command to achieve fast and stable EAF flicker mitigation by supporting the voltage Vpcc. Through measuring the voltages at PCC and

generating error signals, the external control gives the Iq reference to internal control so that STATCOM provides reactive power compensation and mitigates the voltage fluctuation at PCC.

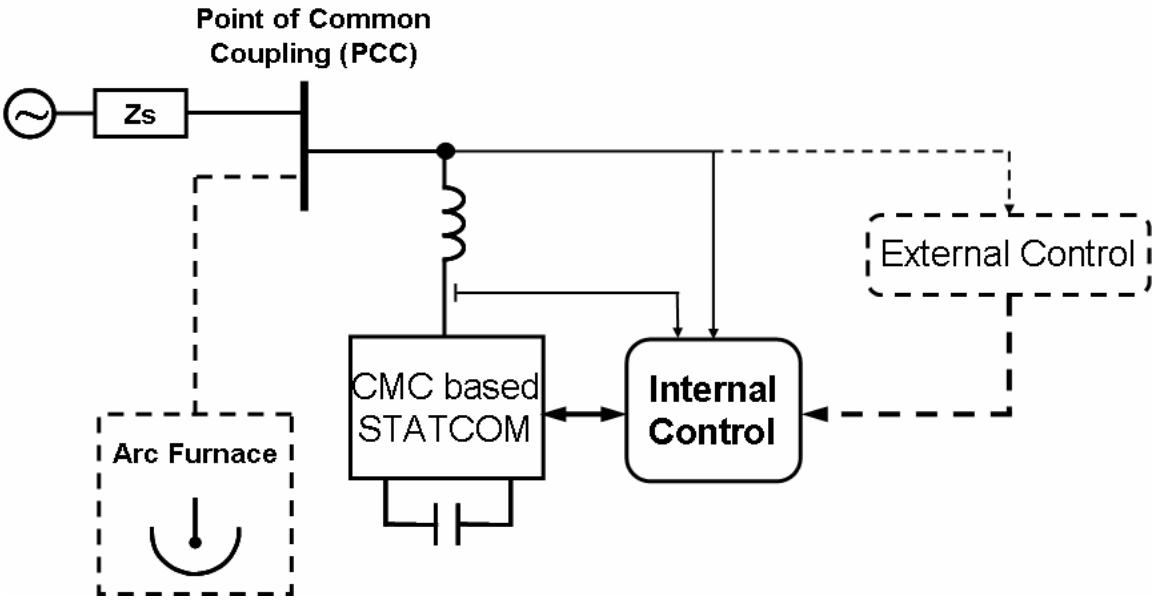


Figure 4-19. One-line diagram of a CMC-based STATCOM

With a designed internal controller, STATCOM can be represented as a 3-phase current-source with typical dynamic response characteristics. Therefore, for a specific case, the whole STATCOM-EAF system can be simplified into an average model in abc frame and shown in Figure 4-20. And it can be transformed into dq0 frame to get a time-invariant model, which is shown in Figure 4-21. Since each variable can be represented as steady-state constant at an operating-point and its small-signal varying disturbance, a small-signal model can be derived by expunging the steady-state value from the large-signal model and is shown in Figure 4-22.

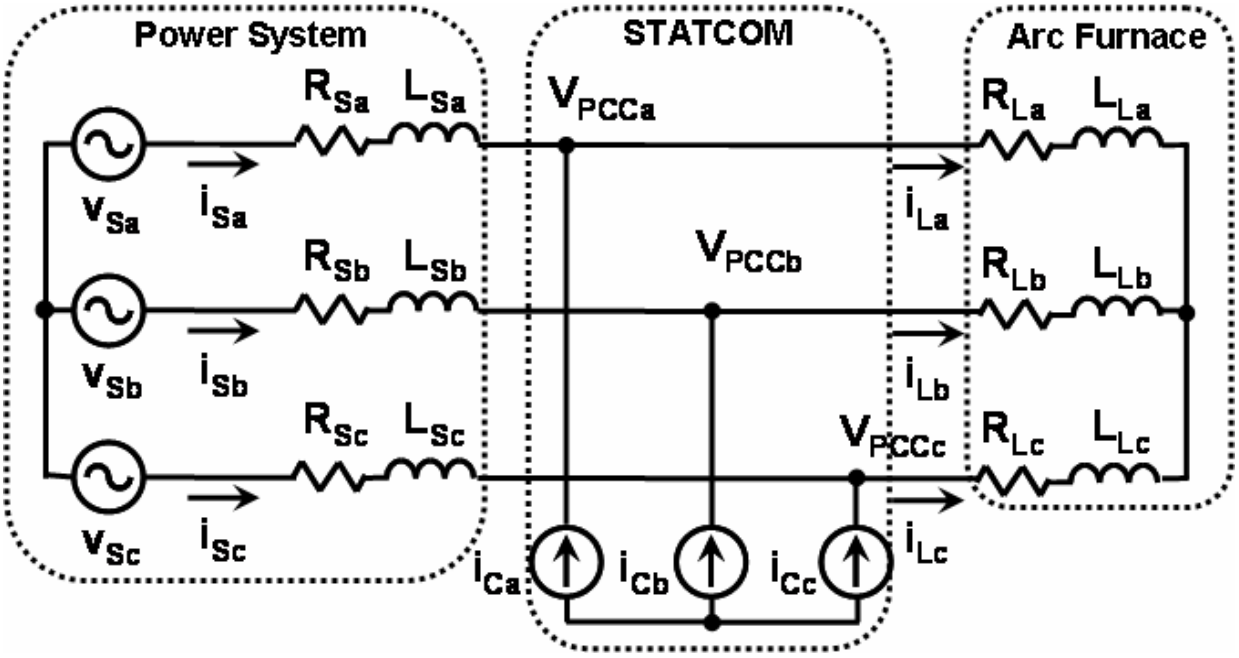


Figure 4-20. Simplified system model of a STATCOM and EAF system

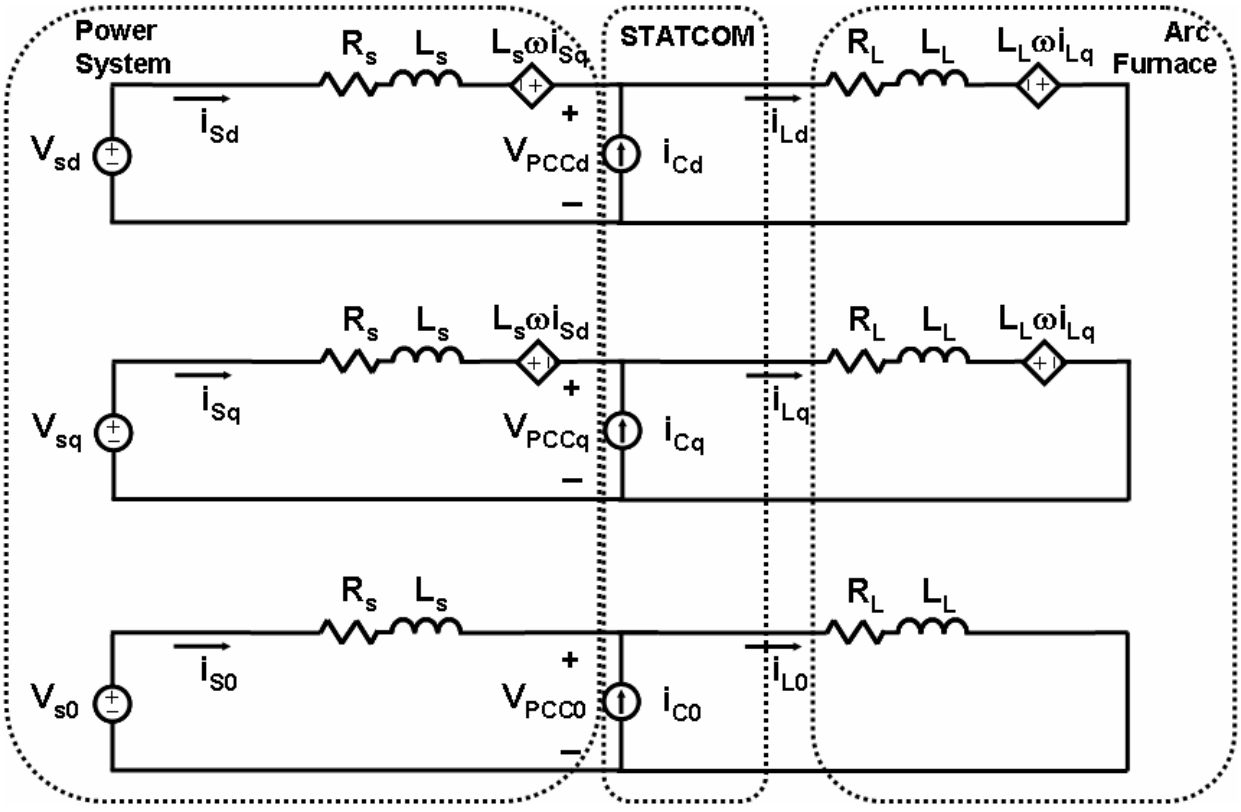


Figure 4-21. STATCOM and EAF system model in dq0 frame

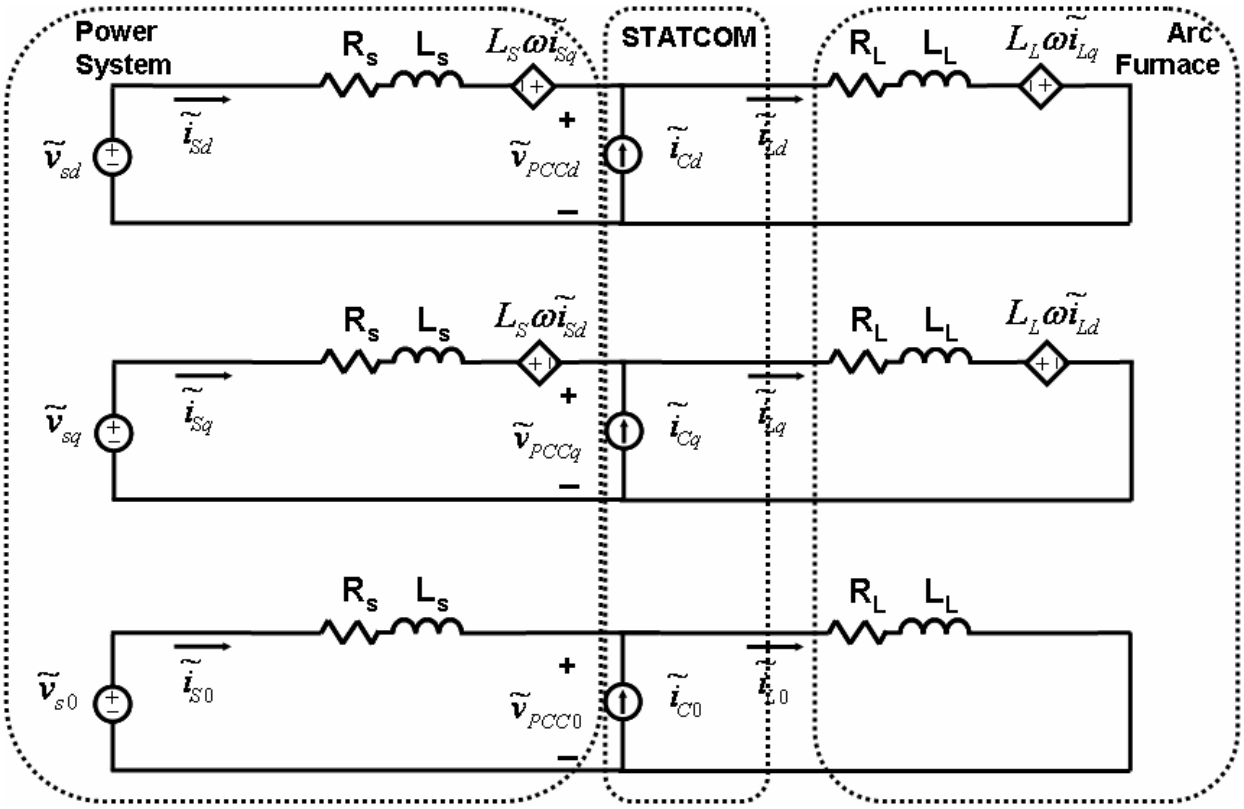


Figure 4-22. Small-signal model in dq0 frame of a STATCOM and EAF system

With derived small-signal model of this Multi-Input Multi-Output (MIMO) system, the open-loop transfer function can be obtained by looking at one loop at a time. The transfer function Gvdq(s) from STATCOM output reactive current Icq to PCC d-axis voltage V_{PCC_d} is given below:

$$Gvdq_std(s) := Kvdq \cdot \frac{\frac{s^2}{\omega z^2} + \frac{s}{Qz \cdot \omega z} + 1}{\frac{s^2}{\omega p^2} + \frac{s}{Qp \cdot \omega p} + 1}$$

Equation 4-2

where

$$Kvdq := \frac{-\omega \cdot \left[\left(Rl^2 \cdot Ls + Rs^2 \cdot Ll\right) + \omega^2 \cdot Ls \cdot Ll \cdot (Ls + Ll)\right]}{(Rs + Rl)^2 + \omega^2 \cdot (Ls + Ll)^2}$$

$$\omega z := \sqrt{\frac{\left(Rl^2 \cdot Ls + Rs^2 \cdot Ll\right) + \omega^2 \cdot Ls \cdot Ll \cdot (Ls + Ll)}{Ls \cdot Ll \cdot (Ls + Ll)}}$$

$$Qz := \frac{\sqrt{\left[\left(Rl^2 \cdot Ls + Rs^2 \cdot Ll\right) + \omega^2 \cdot Ls \cdot Ll \cdot (Ls + Ll)\right] \cdot (Ls + Ll)}}{2 \cdot (Rs + Rl) \cdot \sqrt{Ls \cdot Ll}}$$

$$\omega p := \frac{\sqrt{(Rs + Rl)^2 + \omega^2 \cdot (Ls + Ll)^2}}{Ls + Ll}$$

$$Qp := \frac{\sqrt{(Rs + Rl)^2 + \omega^2 \cdot (Ls + Ll)^2}}{2 \cdot (Rs + Rl)}$$

Since the synchronous angle of Park Transformation is selected to tie with the angle of V_{PCC_a}, V_{PCC_q} can be negligible, and the instantaneous V_{PCC} is only represented by V_{PCC_d}. Therefore, with Gvdq(s) above and close-loop transfer function from Iq_ref to Icq, which is designed in the internal control strategy, we can get the external control compensation Hvq to

achieve the necessary frequency domain and time-domain control specification. The control function block diagram of the whole STATCOM and EAF flicker mitigation system is shown in Figure 4-23.

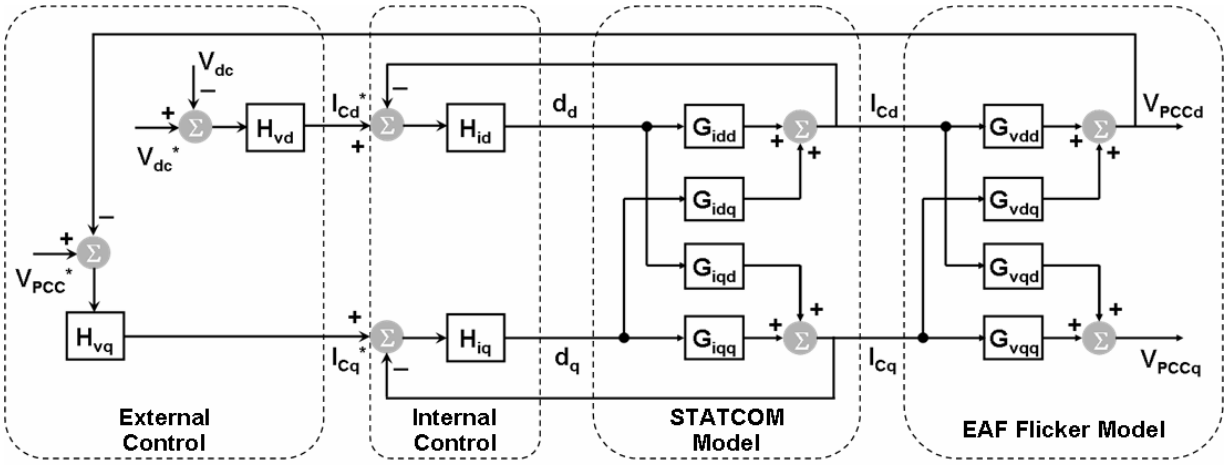


Figure 4-23. Flicker control block diagram

With this proposed control method, the stability of the whole system integrating the power system, EAF and STATCOM is ensured, and the performance of STATCOM for EAF flicker mitigation can be quantitatively designed to achieve a cost-effective flicker mitigation.

4.4 TNA System and Experiement Results

To evaluate the CMC-based STATCOM control strategy and flicker mitigation performance, a real-time TNA system of STATCOM and EAF, shown in Figure 4-24, is developed [C10]. The left cabinet houses the EAF flicker TNA composed of solid-state AC-switches, passive loads, and coupling transformer; the STATCOM power stage with three-level IGBT-based CMC

converters, DC capacitors, AC reactors and pre-charge circuits are housed in the center cabinet; the DSP/FPGA-based central controller are mounted into the cabinet on the right. The parameters of TNA system are listed in Table 4-1.

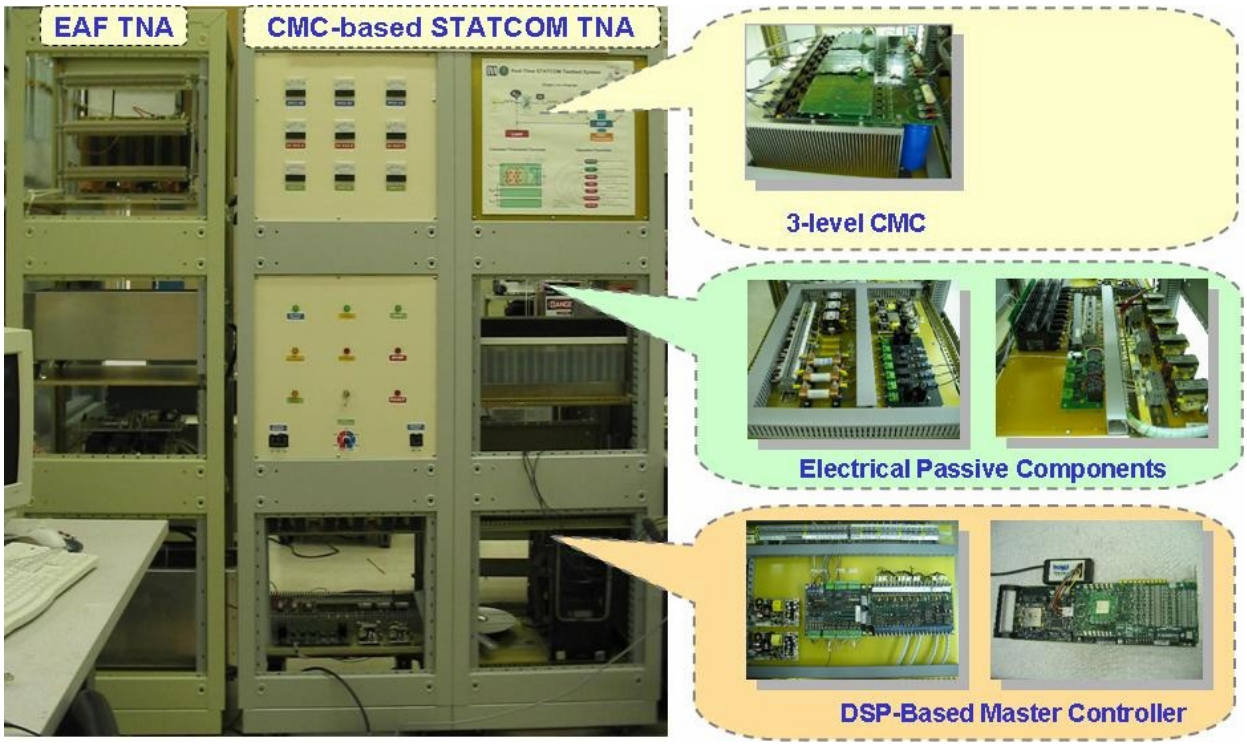


Figure 4-24. Real-time TNA of a STATCOM and EAF system

TABLE 4-1. SPECIFICATION OF A CMC-BASED STATCOM AND EAF TNA SYSTEM

Power Supply	Fundamental frequency	f = 60 Hz
	Source voltage	Vs = 208 V
Arc furnace	Flicker frequency	f=1~10Hz
	Reactor	L_L = 20 mH
	Resistor	R_L= 10.8 Ω
STATCOM	AC side voltage	Vac=100 V
	Coupling inductance	Lc = 3 mH
	Coupling resistance	Rc = 60 m Ω
	DC capacitance	Cdc = 2 mF
	DC side voltage	Vdc = 102 V

The experiment results of STATCOM TNA system following an Iq_ref command step change are shown in Figure 4-25, which provide a subcycle response from full-capacitive mode to full-inductive mode and vice versa.

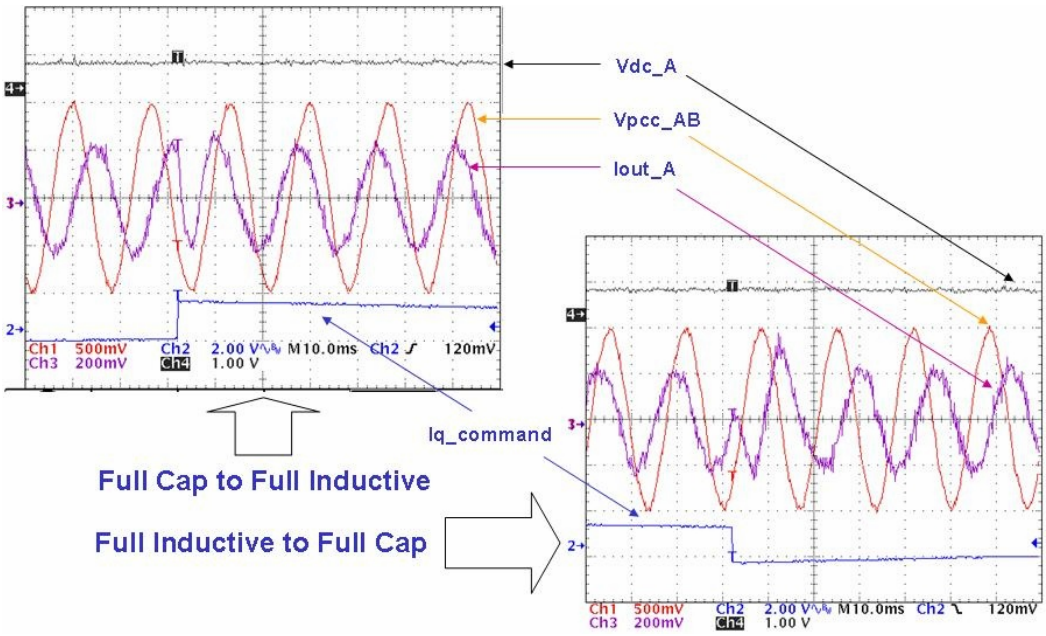


Figure 4-25. Iq_ref command response of the STATCOM TNA

For the EAF flicker TNA, a three-phase AC-switch is designed using a back-to-back IGBT (SKM300GB 1240) phase-leg with RCD snubber to achieve the variable flicker frequency. Its principle diagrams and physical pictures are shown in Figure 4-26.

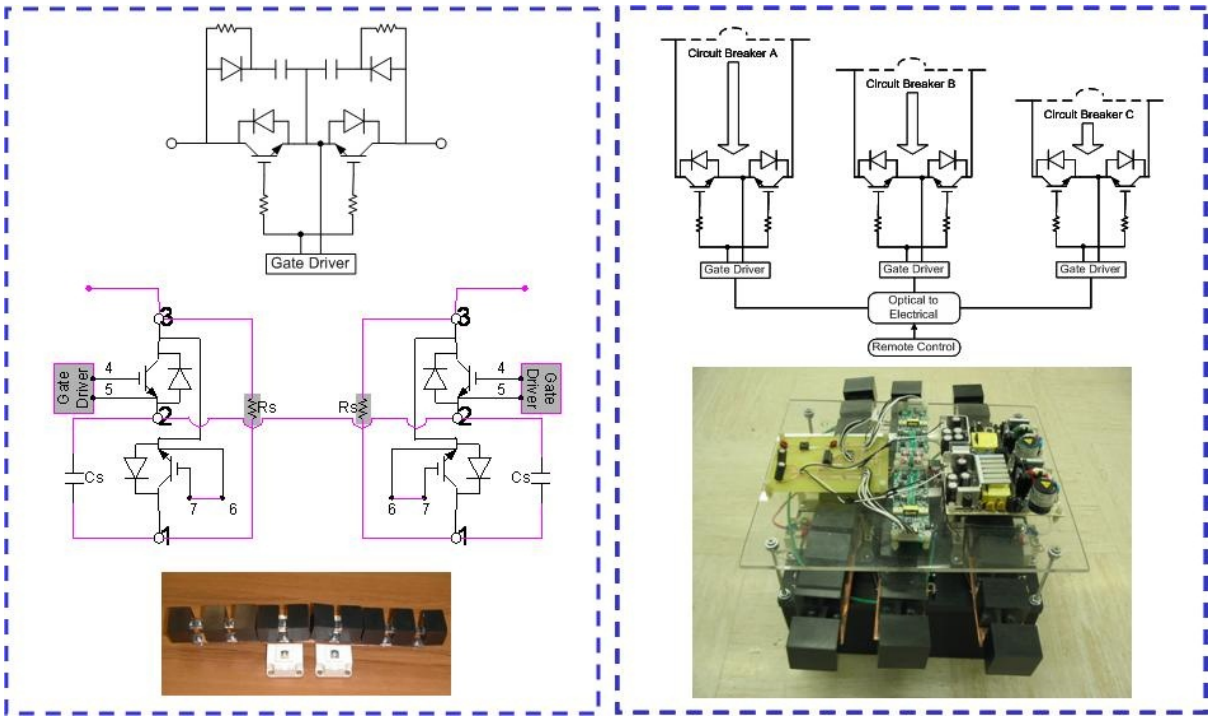


Figure 4-26. High-speed solid-state AC-switch

EAF flicker TNA can generate a flicker at PCC with specific frequency, magnitude, source Xs/Rs ratio and load power factor through regulating the switching frequency of solid-state switch, source impedance and load impedance. A typical 5 Hz 1% flicker at Hoeganaes is scaled down and regenerated by the TNA and shown in Figure 4-27.

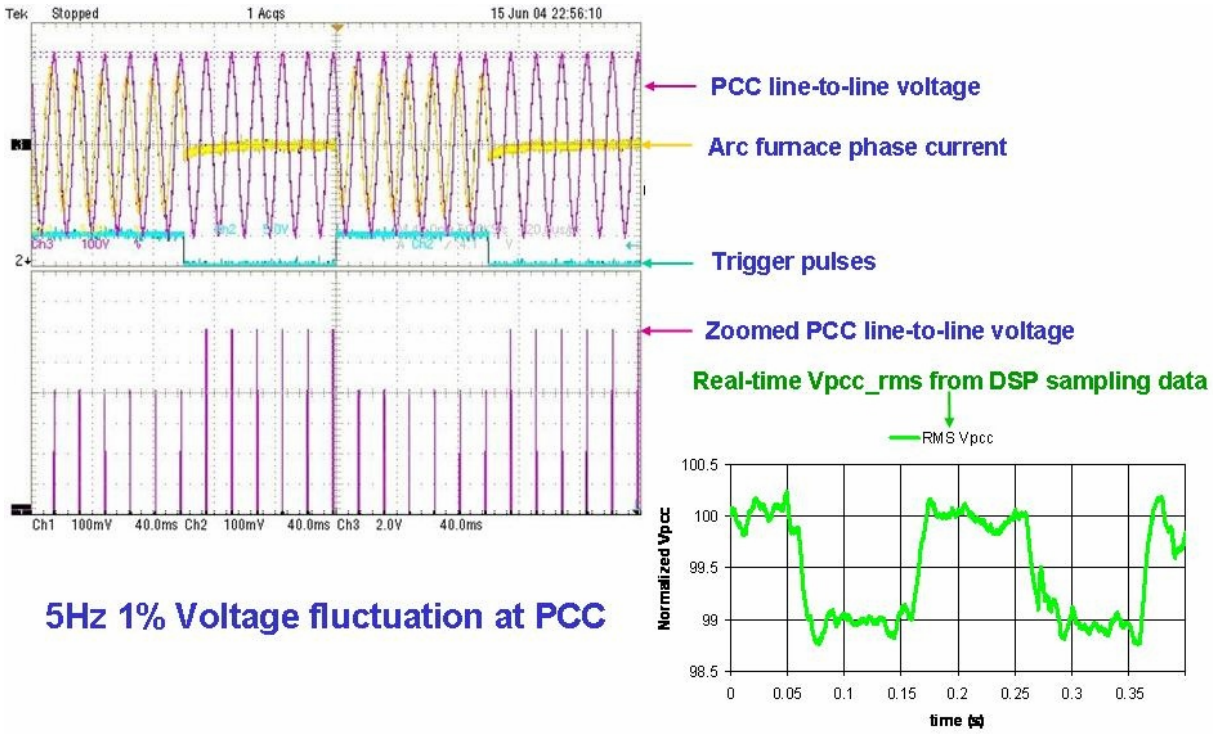


Figure 4-27. TNA experiment results of the EAF flicker

With verified STATCOM TNA and EAF flicker TNA, the whole TNA system is connected at the point of common coupling. External control strategy is also implemented into DSP control to work with internal control strategy simultaneously.

Scaling down the practical arc furnace at Tennessee, the source Xs/Rs ratio and flicker frequency of flicker TNA is adjusted to 3.7 and 5Hz by regulating series impedances and AC-switch switching frequency. And STATCOM TNA rating is set to 30% of EAF TNA rating.

The experimental results recorded by oscilloscope are shown in Figure 4-28. Compared with the results before compensation, the flicker is obviously mitigated after compensation. The

waveform at right side shows that the STATCOM provides dynamic reactive currents to compensate the power consumption by the arc furnace during the on-load and off-load state and hereby successfully mitigates the voltage fluctuation on the system side. The phase shift between voltage and current is not exactly 90^{O} because the Id-channel needs small current to compensate for the STATCOM internal loss and to maintain the VSC DC-bus voltages. The waveform also verifies that the CMC-based STATCOM has a control bandwidth of hundreds Hz and hence is fast enough to compensate flickers (1Hz~20Hz).

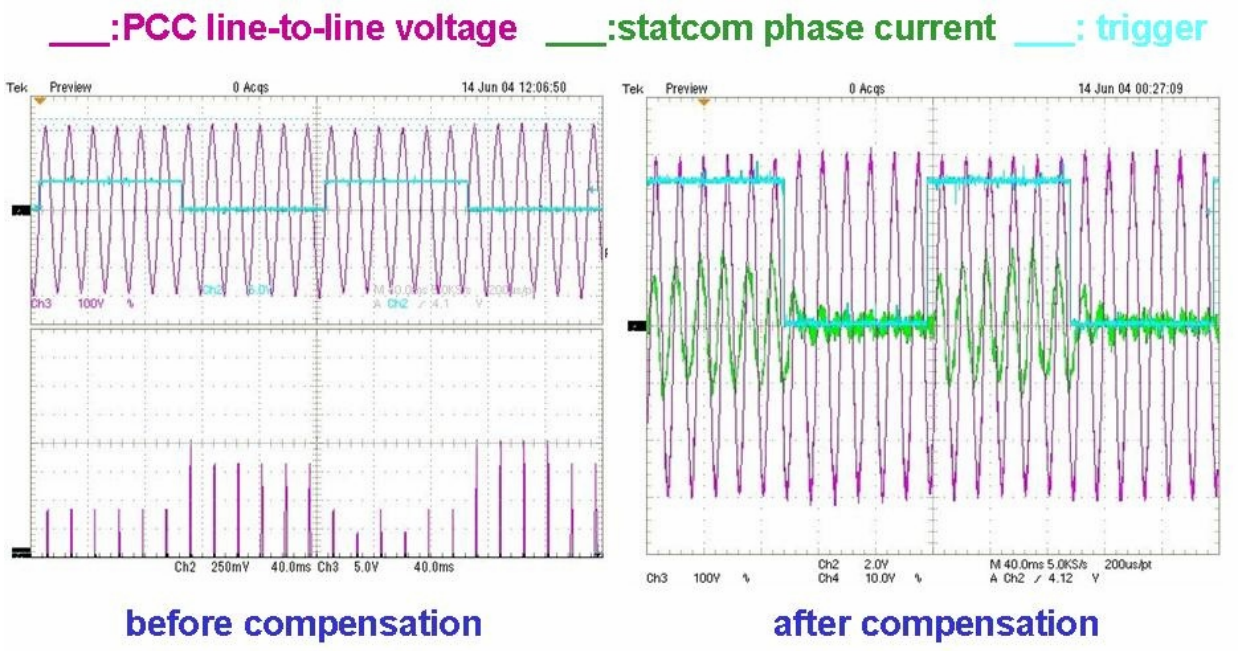


Figure 4-28. Real-time TNA of a STATCOM and EAF system

In Figure 4-29, the experiment waveforms are plotted to compare with the switching model-based simulation results. The experiment results match simulation results very well. From both

the simulation and the experiment, the models of CMC-based STATCOM and EAF flicker are validated, and control strategy of CMC-based STATCOM for flicker mitigation is also verified.

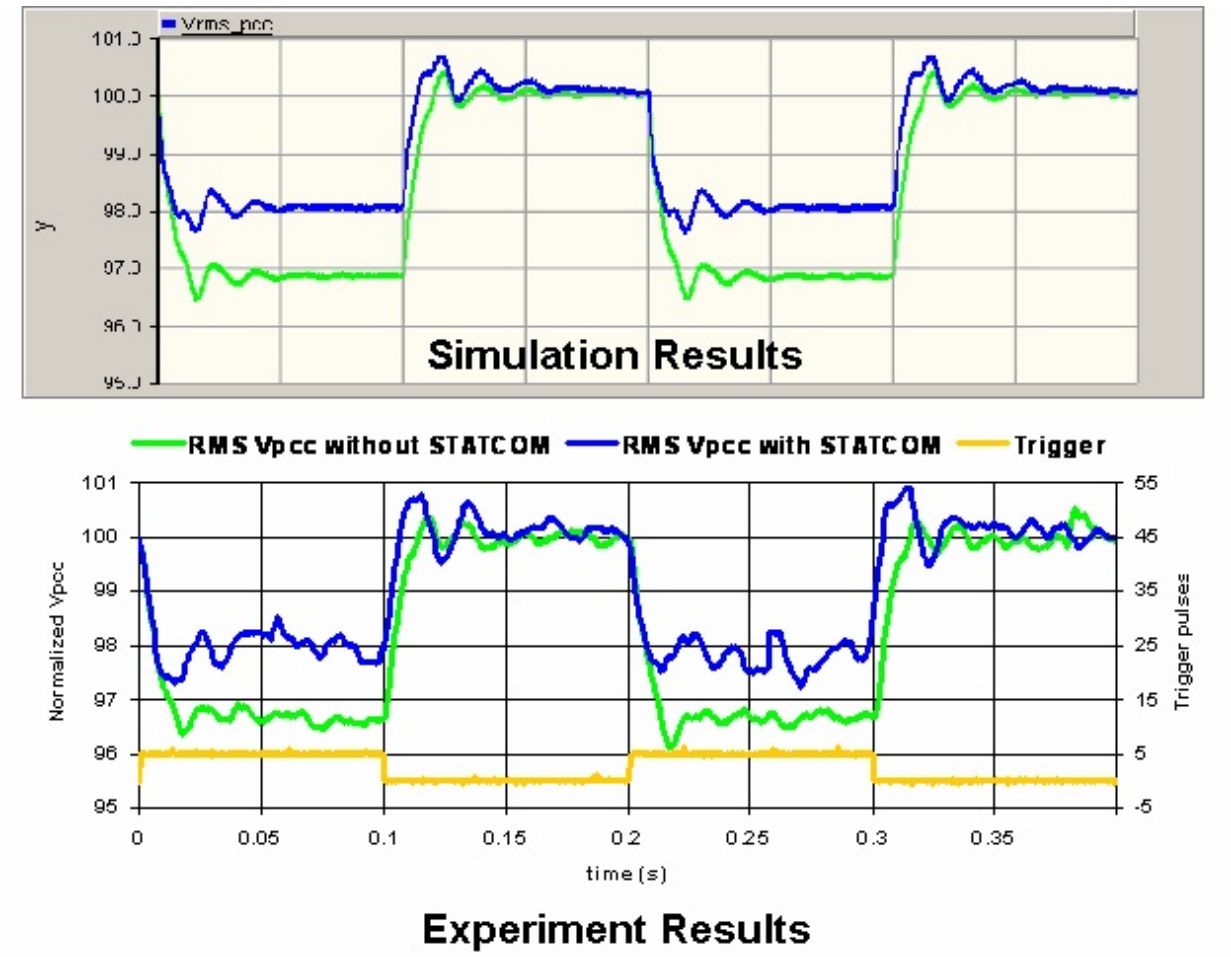


Figure 4-29. Comparison between TNA experiment results and PSCAD simulation results

4.5 Conclusion

In the chapter, for a specific studied EAF case, the steady-state analysis gives a generalized relationship of $\Delta V_{PCC}/V_{PCC}$, Q_C/S_{EAF}, and X_S/R_S and provides the steady-state evaluation of STATCOM's size for flicker mitigation, which is verified by the steady-state simulation results.

Based on the field data from 45 MVA EAF installed at TVA, the flicker mitigation and reactive power compensation requirements are quantitatively analyzed. The various compensation solutions are qualitatively compared, such as passive filter, SVC, and STATCOM. In addition, a field data-based EAF model is proposed and validated by simulation results. The simulation results based on field data show that a 4.5MVA rated STATCOM can, to some extent, mitigate voltage flicker caused by an 45 MVA EAF, whereas a 30 MVA rated STATCOM can completely mitigate the voltage flicker. The additional 14MVAr capacitor bank with the STATCOM improves the load power factor and bus voltage profile. These simulation results verify the steady-state analysis results. The effectiveness of STATCOM-based flicker compensator is also validated by the simulation.

For the modeling and control of the EAF flicker mitigation using a CMC-based STATCOM, an EAF worst-case model is proposed first so that the deterministic impedance of EAF at specific operating points can be evaluated, which can not be accomplished by previous EAF models mainly for harmonics analysis. Combining the developed small-signal models of a worst-case EAF flicker and a CMC-based STATCOM, a generalized hybrid model in dq0 frame of a system-EAF-STATCOM is obtained and STATCOM control-to-Vpcc is derived. With the derived transfer function, the model-based control strategy of CMC-based STATCOM for EAF flicker mitigation is proposed and, other than trial-and-error tuning in previous design, the TF-

based compensator design of the STATCOM external voltage loop gives the system desired control bandwidth and stability margin.

To verify the modeling and control of CMC-based STATCOM for EAF flicker mitigation, a scaled-down real-time TNA integrating CMC-based STATCOM with its digital controller and EAF flicker model is demonstrated. Compared to the simulation results, the TNA experiment results are matched very well with each other, and show that the CMC-based STATCOM system efficiently and rapidly mitigates the EAF flickers, and consistently verify the model and controller design, which provides the confidence for a future field demonstration of the CMC-based STATCOM for EAF flicker mitigation.

Chapter 5 MODELING, INTEGRATION, AND CONTROL OF ULTRACAPACITOR ENERGY STORAGE SYSTEM

An ultracapacitor energy storage system (UESS) is a new class of FACTS/ESS device based on modular VSC and ultracapacitor (UCAP). It targets utility high-power applications ranging from power quality enhancement, voltage and frequency stabilization, power transfer limit improvement to renewable energy and distributed generation support.

In this chapter, the modeling, control and integration of the first generation 4.5MW/4.5MJ UESS prototype, utilizing 1.5 MVA modular VSCs and 2 kV UCAP strings, is presented. First, the testing results of a 45V UCAP module are introduced. A UCAP model is then extracted from the experimental results. Secondly, the interface to combine CMC and UCAP are described, and the potential issues of UCAP for high power operation are discussed. As the UESS's PCS, the CMC's independent real power and reactive power control strategy is presented, and the simulation results are given for verification. Finally, a UESS transient network analyzer (TNA) system utilizing scaled-own CMC and UCAP module is introduced. The TNA experimental results are given to verify the modeling and design of the proposed UESS system.

5.1 Modeling of Ultracapacitor Energy Storage

For the proposed UESS system, a high voltage UCAP string is being developed as shown in Figure 5-1. It comprises 45 series connected 45V UCAP modules and has a rated DC bus voltage of 2kV. The DC bus voltage is selected to match the DC bus voltage requirement for a medium voltage ETO converter [F2]. Each 45V UCAP module comprises 30 series-connected 1.5V UCAP cells. Of asymmetric design, the adopted UCAP technology uses a negative electrode of

activated carbon material and a positive electrode of nickel oxyhydroxide. A low cost aqueous KOH solution, as in alkaline batteries, is used for its electrolyte.

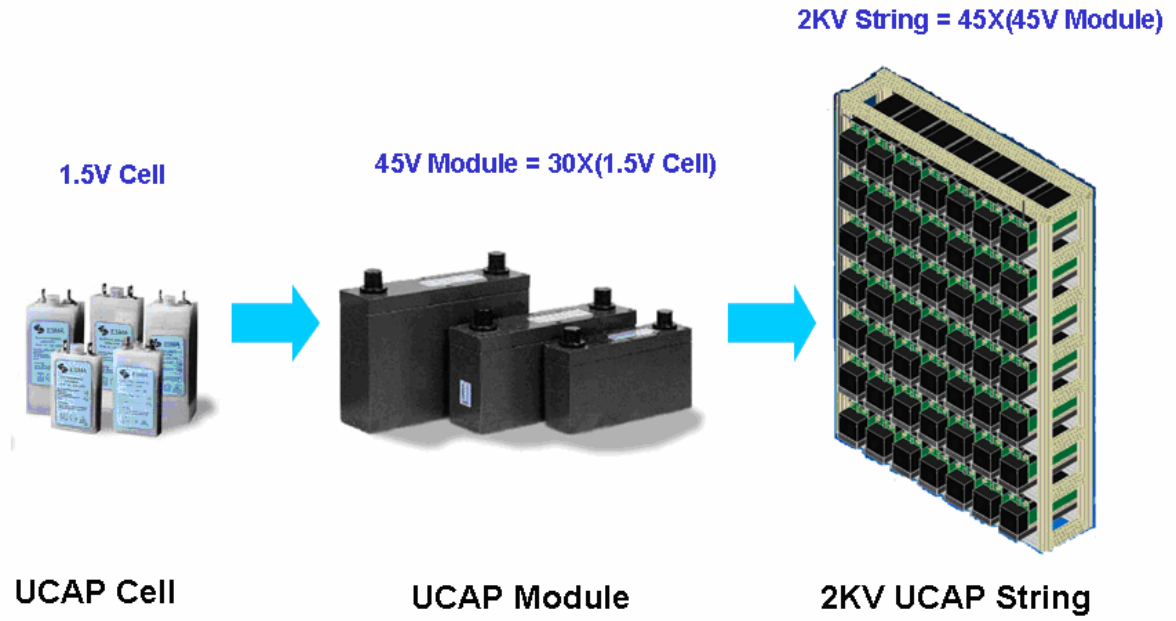
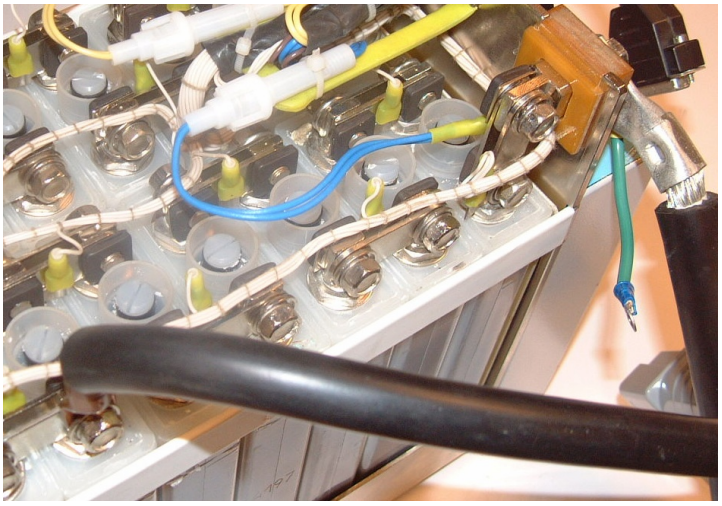


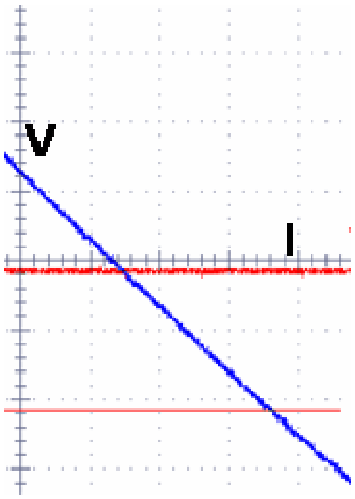
Figure 5-1. Structure of a 2kV UCAP string.

To obtain an accurate UCAP model, cell-based testing is conducted to determine the UCAP's capacitance and equivalent series resistance (ESR). The UCAP measurement setup is shown in Figure 5-2(a). Six series 1.5V cells are connected to a constant current sink for the test. The UCAP's capacitance is determined by applying a constant-current discharge with C=I*dt/dv. As shown in Figure 5-2(b), dv/dt is almost constant. Consequently, UCAP capacitance can be modeled as a constant. For the ESMA Model 30EC402 cell, the test result is 10kF, which is consistent with the model's specifications as listed on its datasheet [B8]. The cell's ESR is calculated by measuring the output voltage drop from no load to steady-state load and then dividing by the load current. As shown in Figure 5-2(c), the cell's open-circuit voltage, related to

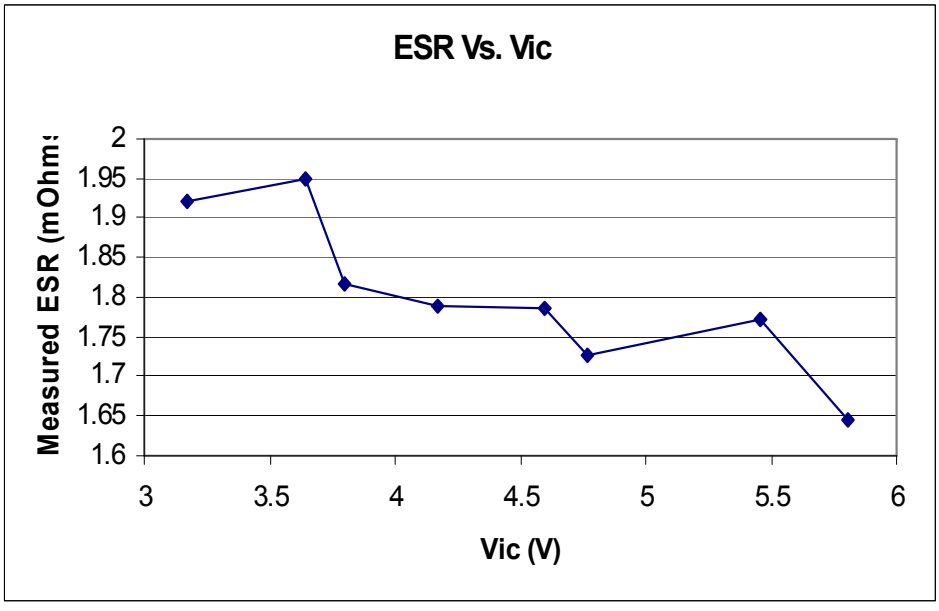
UCAP energy storage, has no significant effect on the UCAP's ESR. Consequently, the ESR can also be modeled as a constant. The measured ESR of the 1.5V cell is 0.3mΩ, which also matches the datasheet. Thus, the UCAP is modeled with constant capacitance and ESR.



(a)



(b)



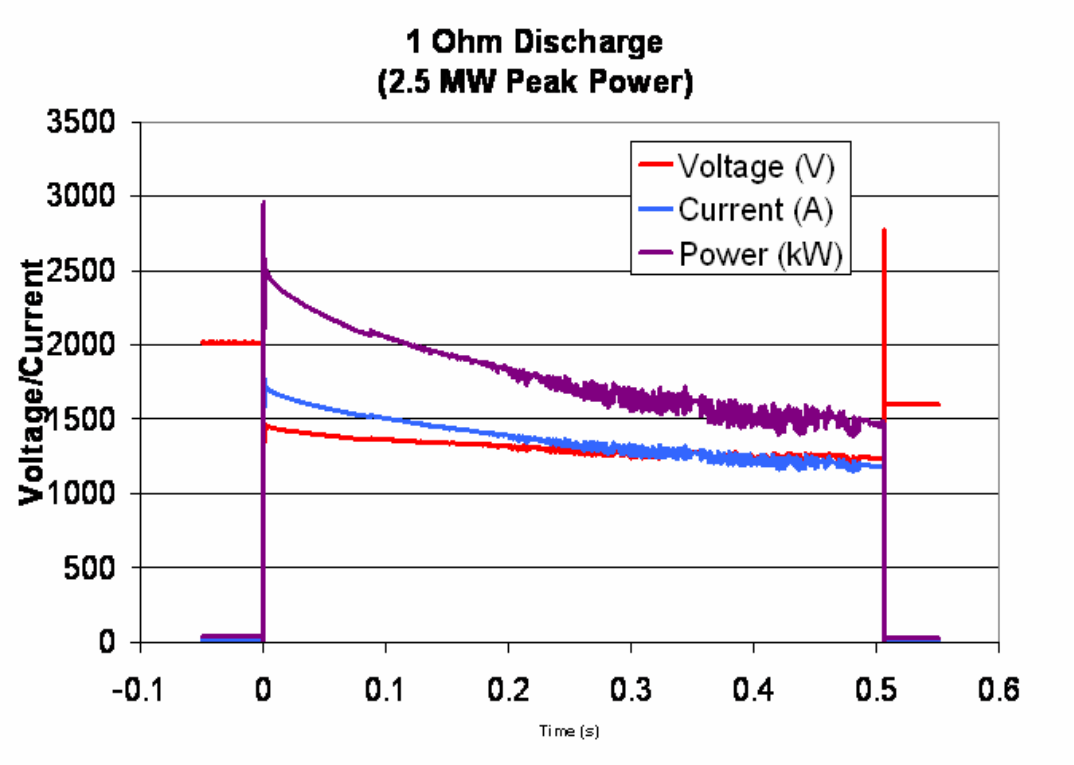
(c)

Figure 5-2. UCAP measurement: (a) measurement setup, (b) capacitance measurement, and (c) ESR measurement.

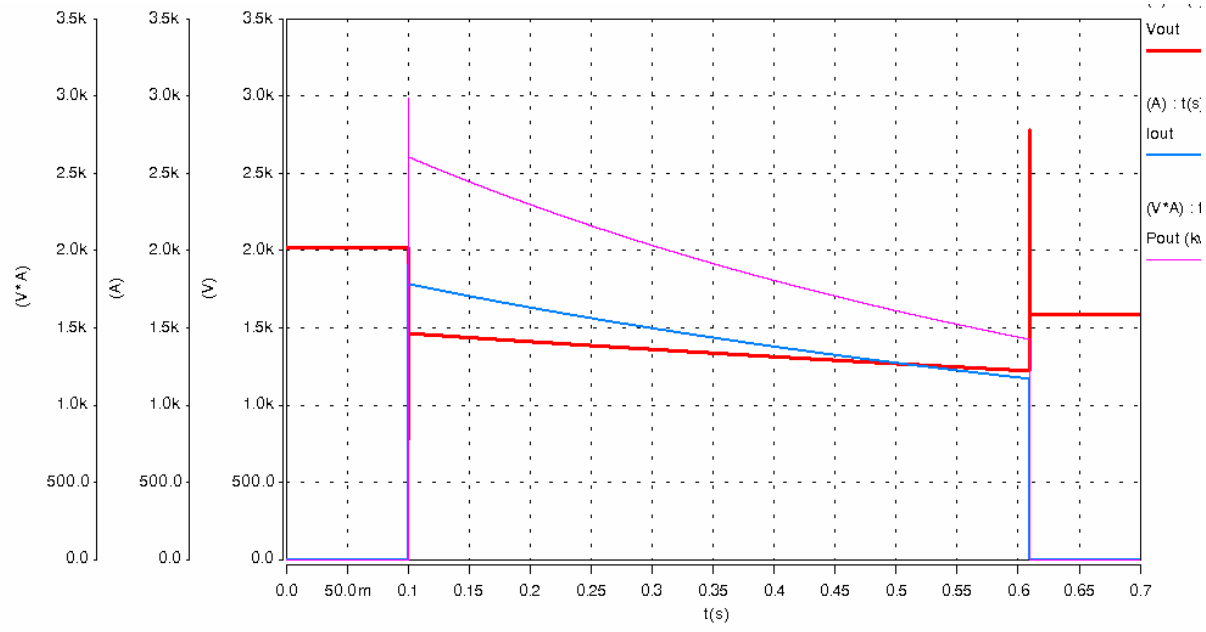
At EPRI Solutions, Tennessee, the developed full-size 2kV UCAP module was built and tested, using a discharge setup shown in Figure 5-3. The 2kV UCAP string on the left backside is connected to a 1Ω resistive bank through an ETO switch [D3]. With such a setup, the string's discharge testing results are shown in Figure 5-4(a). In this test, about 1 MJ of energy was delivered with 2.5MW peak power within 0.5 second. From the testing results, the model parameters of the 2kV string UCAP are extracted using a similar method as the cell-based measurement discussed above. Using the extracted model parameters, the discharge simulation results are shown in Figure 5-4(b). Comparing to the test results, it verifies the accuracy of the UCAP model.



Figure 5-3. Testing setup of a 2kV UCAP string.



(a)



(b)

Figure 5-4. 2kV UCAP string model development: (a) DC discharge testing results, and (b) simulation results with the extracted model.

5.2 Integration of Ultracapacitor with Modular Voltage Source Converter

Also seen in Figure 5-4 are voltage and current spikes during the UCAP's turn-on and turn-off transients. The spikes are the result of equivalent series inductance (ESL) and stray inductance, which can degrade the UCAP and significantly reduce its lifetime. The proposed interface for connecting the UCAP and the modular VSC, shown in Figure 5-5, will mitigate such an effect. A DC-link capacitor is used as a 'filter' to carry the high-frequency current component so that the UCAP only handles DC current with low-frequency ripple; in this case, ESL will not generate a spike on the output voltage. An inherent benefit of this topology is that the UESS can easily be converted into a STATCOM for reactive power compensation when the UCAP is disconnected. With the UCAP energy storage, the UESS automatically achieves black-start capability. Moreover, since H-bridge modular VSC has the capability of charging/discharging DC capacitors from the AC grid [E5], the DC switch can be directly closed without any damping impedance to limit the inrush current when the DC-link capacitors are charged equally to the open-circuit voltage of the UCAP string.

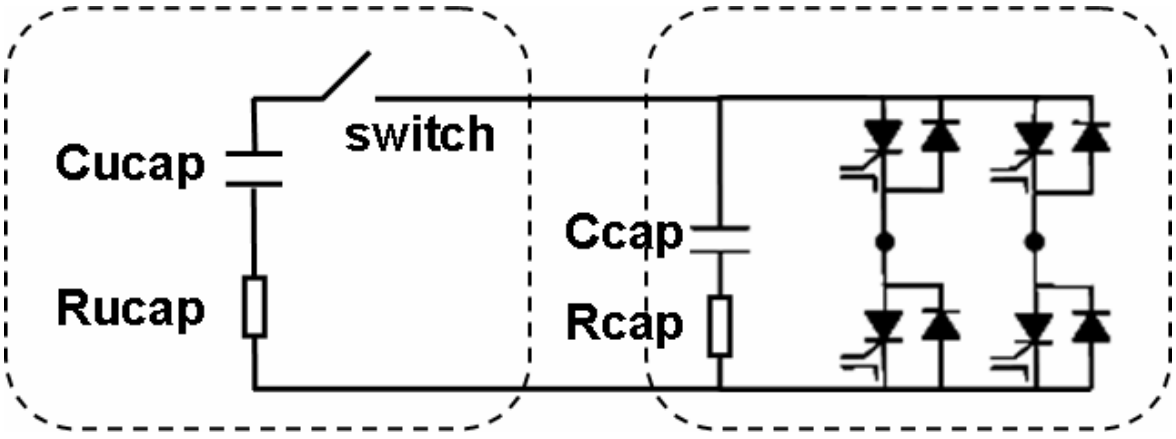
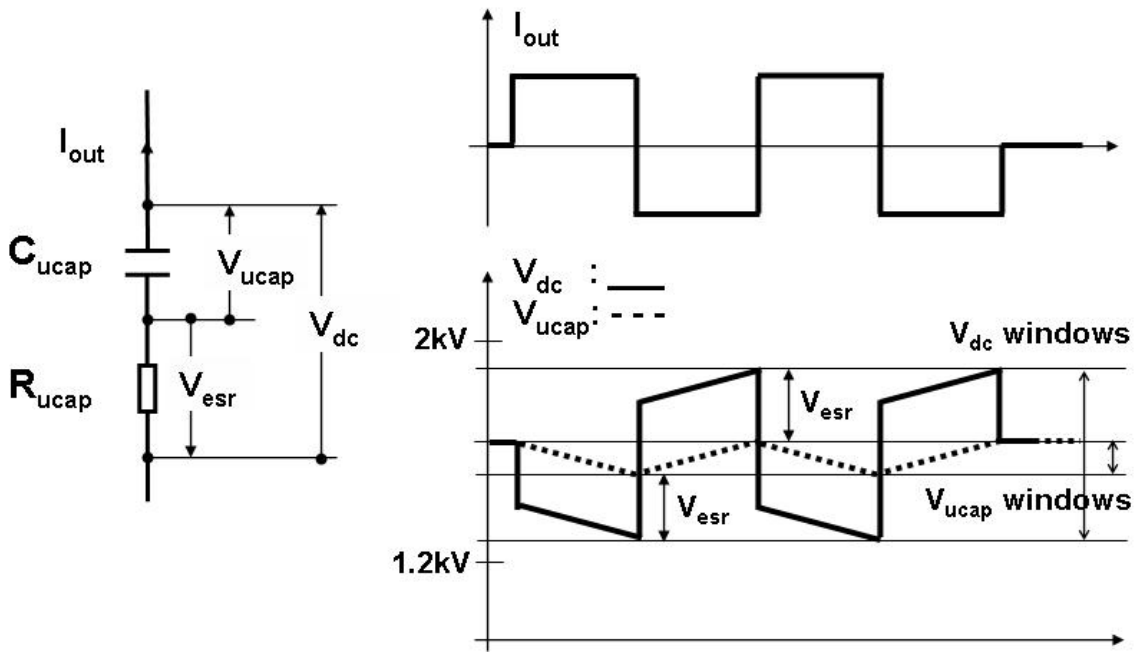


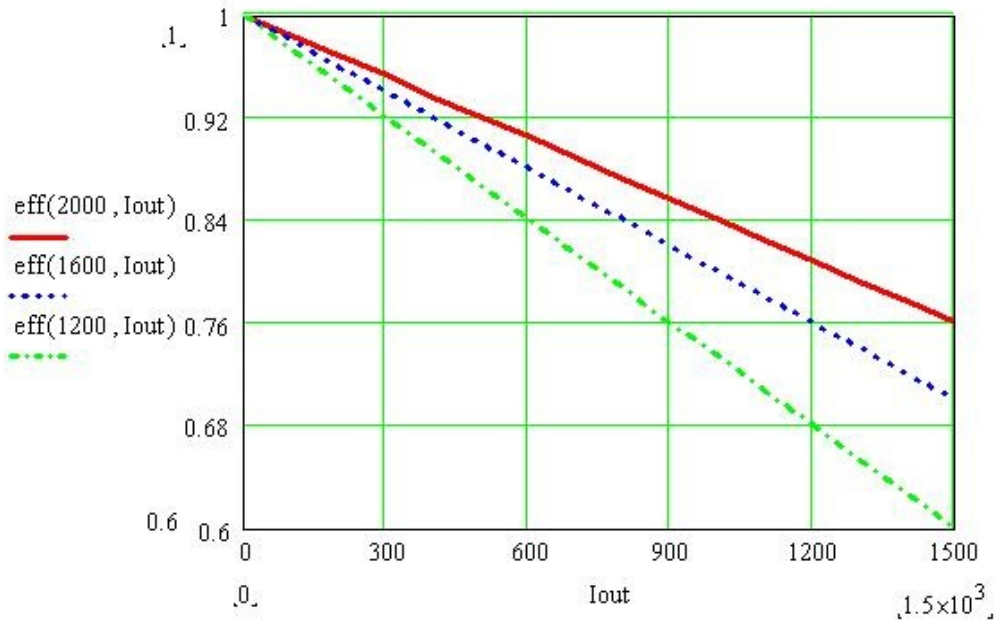
Figure 5-5. Proposed interface to connect UCAP and VSC.

Since the UCAP is tied directly to the converter at a 2kV DC bus, this eliminates the need for a DC-DC circuit, which is necessary for a current-source type ESS, such as SMES. Therefore, the complexity, cost and losses related to the DC-DC circuit can be avoided, and the reliability and efficiency of the overall system is improved though the utilization of energy storage may not be maximized without a DC-DC circuit. This "direct-tie" interface structure is unique for CMC topology and unachievable for traditional multipulse converter and other multilevel converters which share a common higher voltage DC bus because of the limitation of allowable maximum open circuit voltage for ESS. In other words, the CMC topology can offer a flexible and scalable FACTS/ESS with simple interface structure.

For the 2kV UCAP, which consists of 1,350 series-connected, 1.5V cells, the ESR of the string is at least equal to the sum of the individual resistances of the series-connected cells, and, hereby, not small at all for a 2-kV string operating at high-current. The high ESR can manifest itself in one of two ways—a large, internal voltage drop and a decrease in efficiency, as shown in Figure 5-6.



(a)



$$\eta = \frac{P_{total} - P_{ESR}}{P_{total}} = 1 - \frac{R_{UCAP} \cdot I_{UCAP}}{V_{DC}}$$

(b)

Figure 5-6. UCAP ESR-related Issues at high current operation condition: (a) UCAP voltage window utilization, and (b) UCAP efficiency Vs. UCAP current.

Figure 5-6(a) shows that, during high-current operation, the ESR results in a large internal voltage drop that can significantly weaken the utilization of the available voltage windows. In this specific case, the 2kV UCAP string has a recommended operation voltage window between 1200V and 2000V for maximum UCAP lifetime. However, for a 1kA charging or discharging current, the internal voltage drop related to ESR is already about ±300V. Ideally, if the ESR is zero, the UCAP is designed to operate at a nominal voltage of 1600V, hence the voltage window, equivalent to the available charge/discharge energy, should be ±400V. However, with the large (300V) internal ESR drop, the voltage window is reduced to ±100V. Additionally, Figure 5-6(b) clearly shows that UCAP efficiency decreases consistently with increasing output current, and the decreasing slope of efficiency is proportional to ESR. Because of large ESR of a 2kV UCAP string, the efficiency can be less than 80% during high-current (>1kA) charge/discharge. For high-power application, the UCAP thermal management and the voltage balancing among UCAP modules and cells are also challenging issues.

5.3 Control of CMC-based Ultracapacitor Energy Storage System

The schematic diagram of the wye-connected UESS is shown in Figure 2-1, which is the same as its STATCOM counterpart except that the DC source is UCAP. The magnitude and phase of each modular VSC output voltage V_O can be regulated through the turn-on/turn-off of VSC switches, so that the VSC output current I_O can be controlled by having any phase angle and magnitude only limited by V_O operation range. Here, I_O is equal to the sum of the VSC output voltage V_O minus the voltage at an AC point of common coupling V_{PCC} divided by the

impedance of coupling reactor. In other words, the real power and reactive power of a UESS can be controlled through regulating the magnitude and phase of VSC output voltage V_O.

For closed-loop control, the UESS small-signal model and open-loop transfer functions is the same as its STATCOM counterpart, which is shown in the chapter 2. Considering the proposed topology, UCAP ESR limitation and the derived CMC small-signal model above, the UESS closed-loop control strategy is introduced and shown in Figure 5-7. V_{PCC} is sampled to calculate the synchronous angle in a PLL block for Park Transformation. H_{id} and H_{iq} are the two independent current-loop compensators and obtained through the loop gain shaping method to achieve the satisfactory bandwidth, gain margin and phase margin. Therefore, the UESS output current can respond to the I_{dref} and I_{qref} command with high-bandwidth (hundreds Hz). In other words, the UESS can respond to the real power and reactive power command in a subcycle.

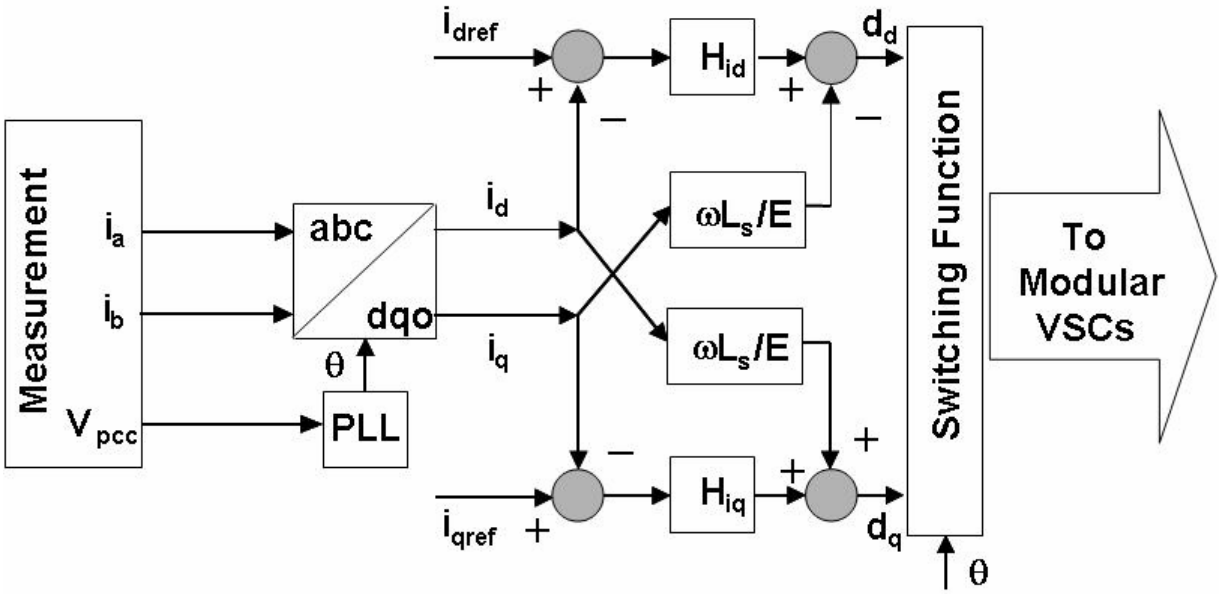


Figure 5-7. UESS control block diagram.

With the control strategy above, UESS is allowed to perform as an independent, 4-quadrant real power and reactive power controller. As shown in Figure 5-8, any combined real power and reactive power command inside the circle can be designed to respond in a subcycle with desirable stability margin. The size of the circle is determined by the power rating of the ETO-based VSC, as well as the UCAP energy storage.

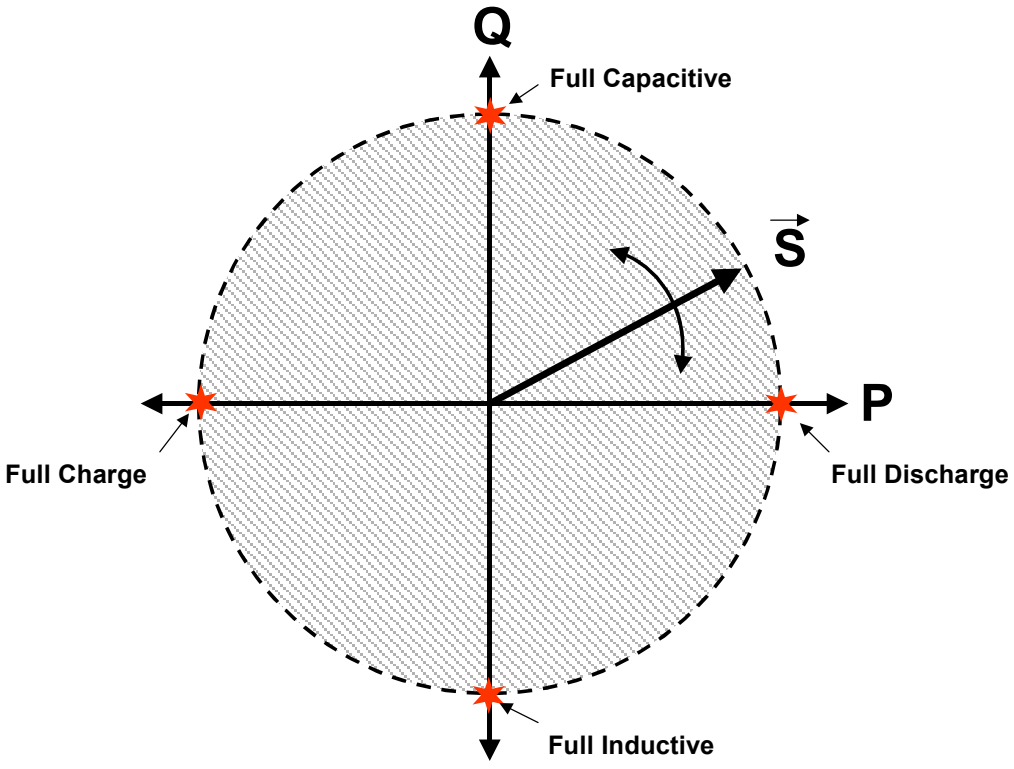
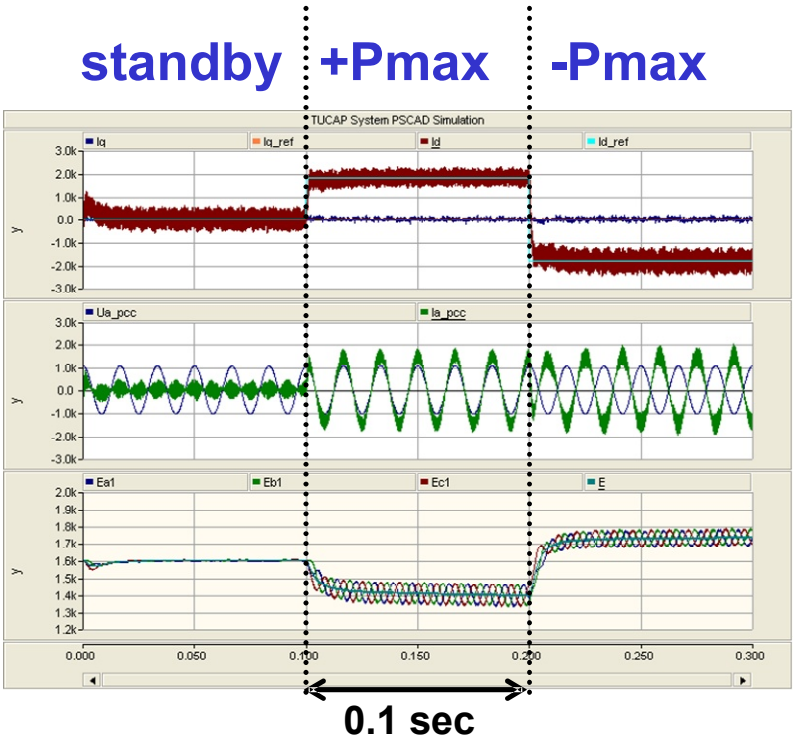


Figure 5-8. Typical operation range of a UESS.

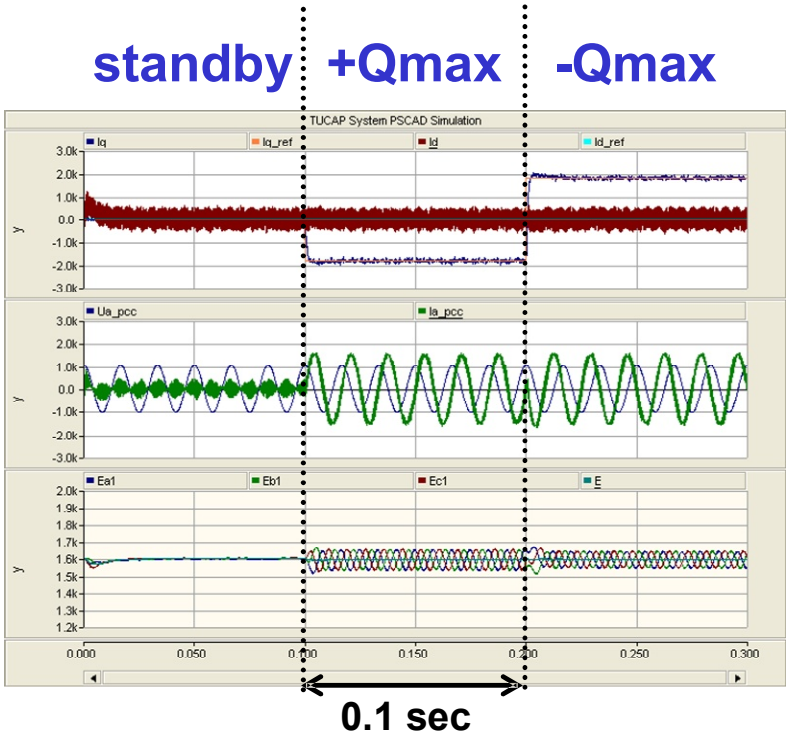
The designed UESS system specifications are listed in Table 5-1. Detailed switching model simulation of the designed UESS system is conducted in PSCAD/EMTDC. The simulation results of UESS step response for four typical operation points (full discharge or +Pmax, full charge or -Pmax, full capacitive or +Qmax, full inductive or -Qmax) are shown in Figure 5-9, which verifies the fast-response and control strategy of UESS system.

TABLE 5-1. UESS PROTOTYPE SYSTEM SPECIFICATION

Three-Level CMC-based TUCAP	
Configuration	Three-Phase Three-Wire Wye-Connection
PCC Line-to-line Voltage	1280V
Individual DC Bus Voltage	1200V ~ 2000V
Rated RMS Reactive Current	1060A
Individual Switching Frequency	1kHz
Ultracapacitor Impedance	(320m-j/(ω ×3F)) Ω/Phase
DC-link Capacitor Impedance	(0.071m-j/(ω ×11.9mF)) Ω/Phase
Coupling Reactor Impedance	(8.72m+j ω ×230 μ H) Ω/Phase



(a)



(b)

Figure 5-9. UESS simulation results: (a) real power control, and (b) reactive power control.

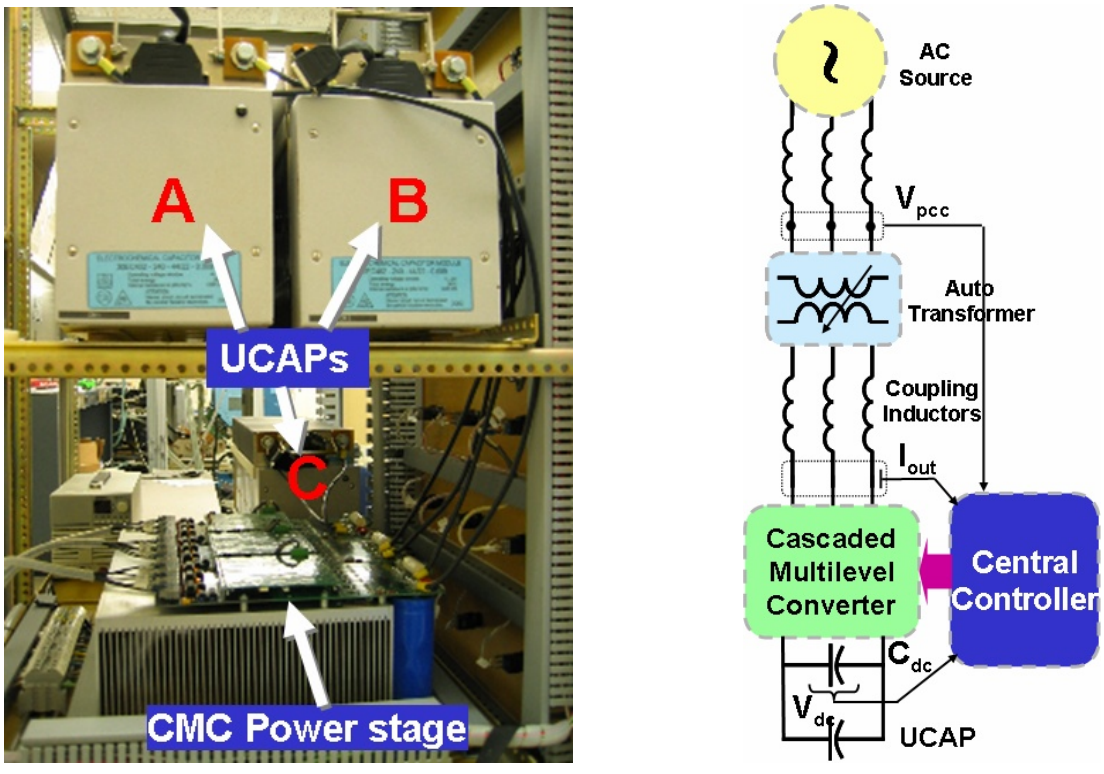
In addition to the hardware development of the 2 kV UCAP, a 4.5MVA PCS prototype system is also developed that utilizes three 1.5MVA modular VSCs based on ETO thyristor switching at 1kHz. The three phase converter system effectively forms a 3-level CMC. The PCS prototype is currently configured and demonstrated as a STATCOM, which has been presented in the section 2.5.

5.4 TNA System and Experimental Results of CMC-based UESS

To validate the UESS control hardware and software, a low-power scaled-down UESS TNA system was built. The TNA's power stage parameters and control parameters are listed in Table 5-2. Shown in Figure 5-10(a), a 3-level CMC was constructed using low-power IGBT modules, and three 45V ESMA, 30EC402 UCAP modules are separately shunt-connected with DC-link capacitors on each VSC. The schematic of the scaled UESS TNA is shown in Figure 5-10(b). The controller of the UESS is implemented by a 64-bit DSP (TMS320C6701) and a FPGA (Xilink XCV50). The DSP, as the central processing unit of the entire controller, computes the main feedback control algorithm, monitors system operation and executes the protection command if necessary. FPGA, performing as the DSP buffer, communicates bi-directionally with DSP to transfer in the feedback signals and transfer out the duty cycle commands, and also calculates the SPWM (Sinusoidal Pulse Width Modulation) algorithm to translate duty signals into practical IGBT switching signals through interface boards and optical fibers. The normal and emergency operation modes of UESS can be controlled through the operator panel.

TABLE 5-2. UESS TNA SYSTEM PARAMETERS

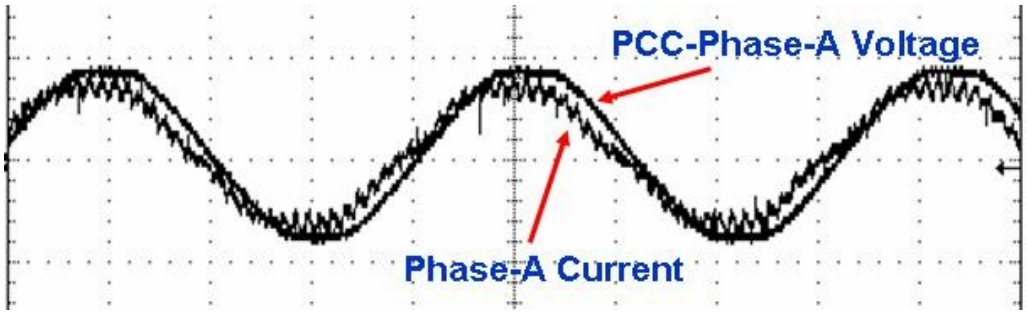
3-level CMC-based TUCAP Testbed	
Electrical Parameters	
PCC Line-to-line Voltage (V)	41
Output Current (A)	6
Switching Frequency (Hz)	1000
Passive Component Parameters	
DC Voltage (V)	44-22
DC-link Capacitance (mF/phase)	2
UCAP (F/phase)	200
AC coupling inductance (mH/phase)	2
Control Parameters	
Bandwidth (Hz)	200
Phase Margin (degree)	48
Gain Margin (dB)	9
Kp	0.06
Ki	10



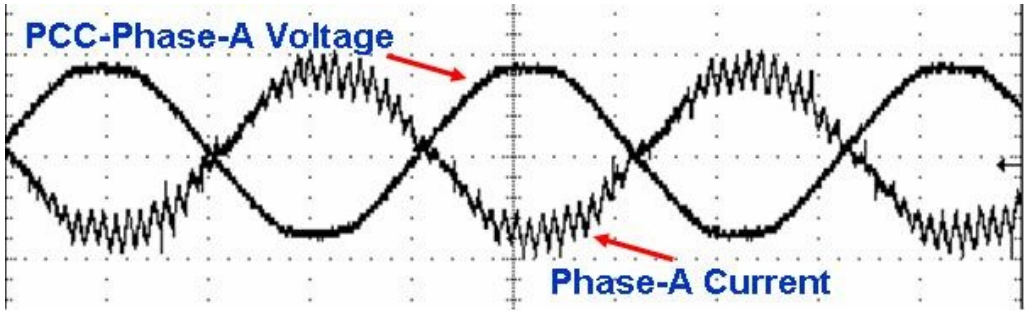
(a) (b)

Figure 5-10. Scaled-down UESS TNA system: (a) TNA setup, and (b) TNA schematic.

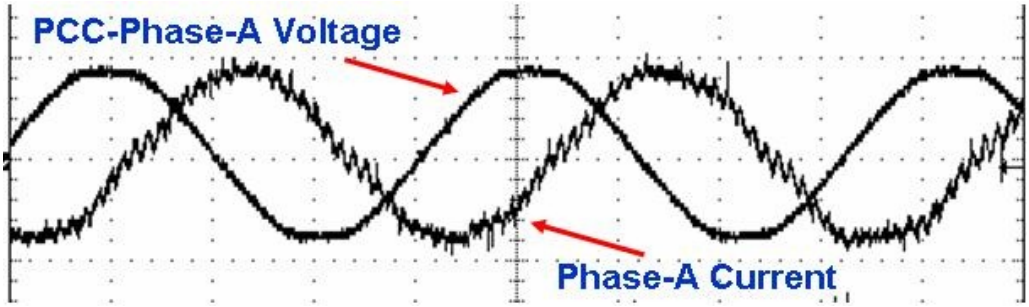
Figure 5-11 shows the TNA experimental results in four typical operation modes (full discharge, full charge, full capacitive, full inductive). The switching ripples on the UESS output current are due to the 1kHz switching of the converter. Figure 5-12 shows the UESS step response from +Q to –P and from –Q to +P in a subcycle. These experiments successfully verify the UESS control hardware and software, UCAP modeling, and UESS control strategy. Currently, the full-rating demonstration of the UESS system at 4.5 MJ (4.5 MW and 1second) is also under plan.



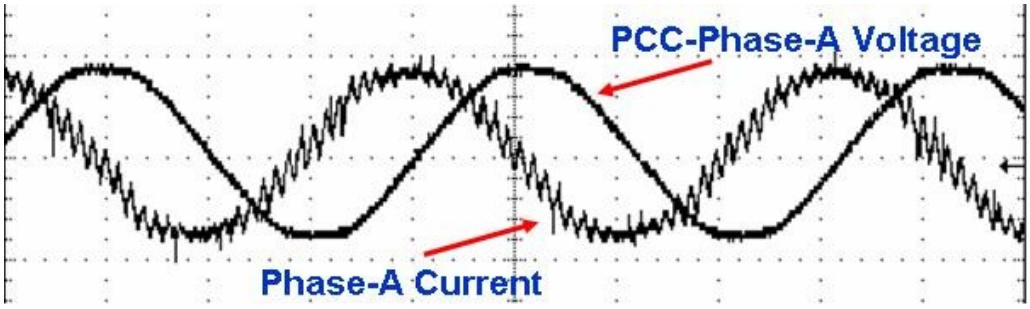
(a)



(b)

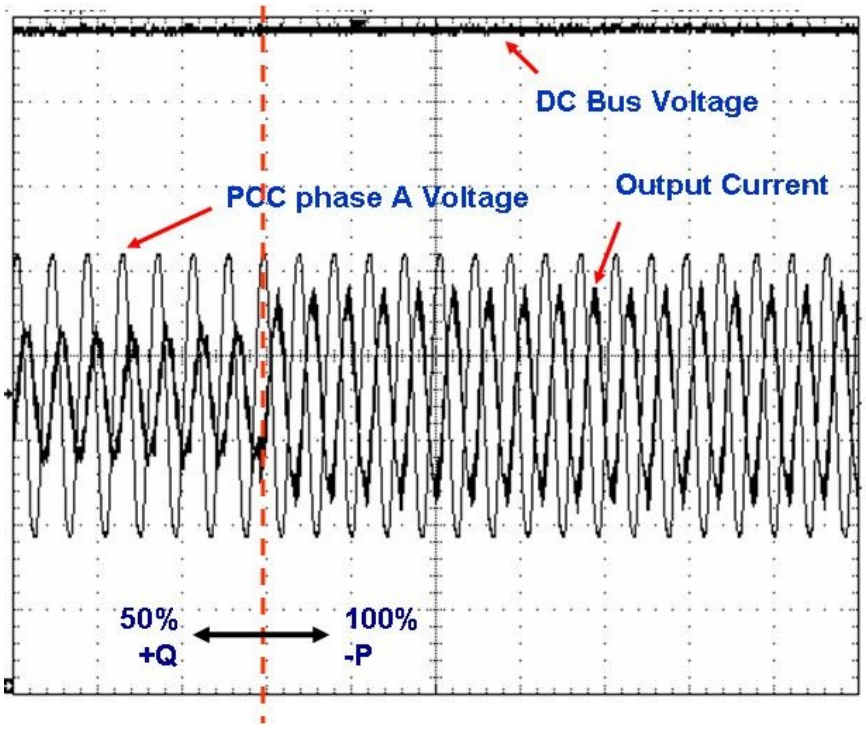


(c)

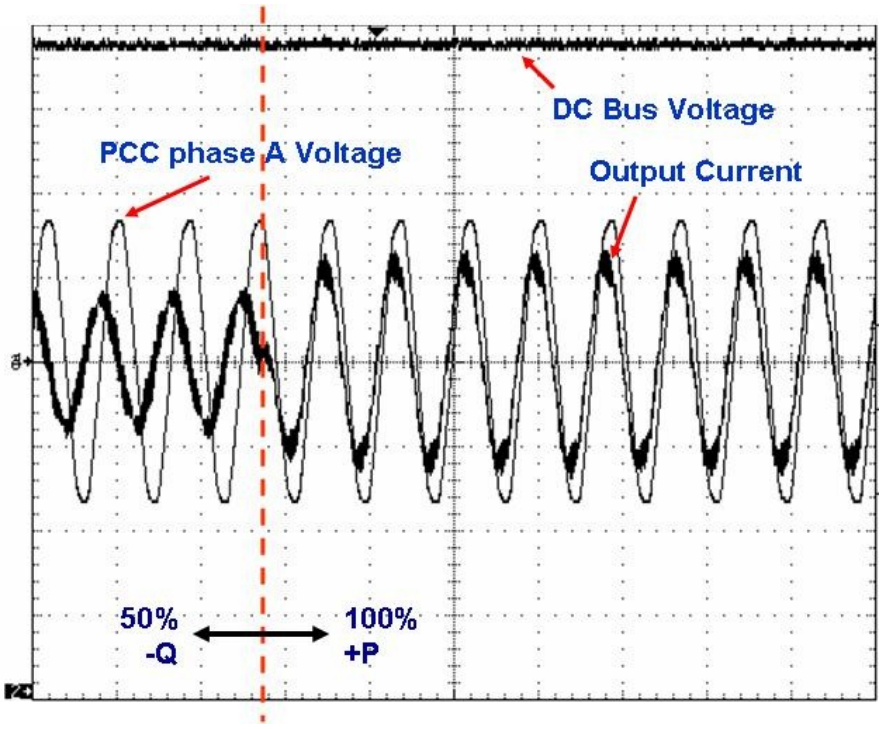


(d)

Figure 5-11. Experimental results of UESS four typical operating modes: (a) full discharge mode, (b) full charge mode, (c) full capacitive mode, and (d) full inductive mode.



(a)



(b)

Figure 5-12. Experimental results of UESS step response: (a) step change from +Q to –P, and (b) step change from -Q to +P.

5.5 Conclusion

In this chapter, the modeling, integration, and control of a UESS energy storage system are presented in details. The UCAP model is obtained through UCAP cell testing, and the full-size 2kV UCAP model parameters are extracted from the discharge experiment. Considering the features of UCAPs and modular VSCs, the potential issues of UCAP for high power operation are pointed out, and an effective and simple interface to integrate the UCAP and modular VSCs is proposed so that the UCAP's lifetime is extended by filtering its carrying high frequency components and the convertability between STATCOM and UESS is convenient and the bulky and costly DC-DC interface circuit is eliminated. With the developed UCAP and CMC model and proposed interface, the control strategy is designed for the UESS system. The simulation results verify the UESS modeling and design. With the developed scaled-down UESS TNA system, the experimental TNA results consistently verify the simulation results, and also validate the modeling and design of the proposed UESS.

In summary, by combining the advantages of the ETO semiconductor device, a CMC topology and its control technology, and a UCAP energy storage, UESS systems are promising FACTS/ESSs for high power applications. It is expected that the successful demonstration of UESS technology will result in a FACTS/ESS that is capable of extremely fast response and that is less costly per kW/kVA than FACTS/ESSs based on traditional energy storage/power electronics technologies.

Chapter 6 CONCLUSIONS AND FUTURE RESEARCH

6.1 Conclusions

STATCOM (static synchronous compensator) and ESS (energy storage system), as a shunt-link flexible AC transmission system (FACTS) controller, has shown extensive feasibility in terms of cost-effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. Recently, advances in power electronics technologies, such as the emerging kilohertz high power semiconductor switches, cascaded multilevel converter (CMC) topology comprising modular H-bridge voltage source converter (VSC), and digital control technology, have the potential to achieve the modularity and scalability design, lower the overall cost, and improve the reliability and functionality of power electronics-based controllers, hence, resulting in increasing applications of STATCOM/ESS. However, how to control a CMC-based STATCOM/ESS to realize excellent performance, high reliability and low cost poses the challenges to researchers.

On the other side, renewable large wind farms, as a fast growing power generation method, undergoes its inherent power quality and stability issues. How to develop the effective and accurate model of a wind power system and how to control STATCOM for wind power support are not in a classical textbook and posing challenges. Meanwhile, as an industrial customer of utilities, electrical arc furnace (EAF) is the major flicker source that degrades the grid power quality. How to economically and efficiently mitigate EAF flicker is a tough issue bothering utility professionals for decades. As a promising solution, STATCOM/ESS with its high

bandwidth, which requires advanced semiconductor switches, converter topology and its control technology, can be used.

This dissertation is dedicated to a comprehensive study of CMC-based STATCOM and its ultracapacitor energy storage system (UESS), and its applications in power system dynamic voltage management, specifically, wind farm voltage fluctuations suppressions and electric arc furnace flicker mitigation.

First, the work of CMC-based STATCOM modeling and control by previous researchers is reviewed. To further understand and analyze the controlled CMC-based STATCOM plant, the full-order transfer functions of a generalized CMC-based STATCOM are derived and compared to the reduced-order transfer functions derived by previous researchers. The relationship between full-order and reduced-order transfer functions are illustrated; and the conditions where the reduced-order transfer functions can be used for closed-loop control design is pointed out; and a clear and simple control design guideline of CMC-based STATCOM is given.

Based on the analysis of the derived control-to-current transfer functions, a DQ frame-based control method of AC-side close-loop direct enengization and de-enengization of a CMC-ased STATCOM, which eliminates the costly and bulky additional DC charge/discharge ciruit and flexibly controls the speed of enengization and de-enengization, is presented. With such a method, the control design is conducted by loop-gain shaping method without tuning compensators' parameters. The proposed method is verified by the simulation and experimental results.

To deal with unbalanced DC voltages at each phase in a CMC-based STATCOM, a per-phase DC bus voltage balancing control strategy, based on the derived control-to-Vdc transfer function and imaginary DQ0-to-ABC Park Transformation, is presented. Based on the derived transfer functions, the balancing control loops are designed with desired bandwidth, phase margin and gain margin. Through the imaginary DQ0-to-ABC transformation method, the DQ frame-based balancing control loop is allowed to be applied at each individual phase for per-phase balancing control. The proposed method is not only a generalized design with ensuring bandwidth and stability margin, but also efficient for DSP/FPGA implementation and computation. The simulation and experimental results well proves the steady-state and dynamic performance of the proposed per-phase DC voltage balancing control strategy.

Moreover, a transformerless grid-connected demonstration of a 4.5 MVA ETO, CMC-based STATCOM prototype is presented. The system integration, passive components selection and digital controller of the demonstrated system are illustrated. The experimental results show not only the stable and fast reponse of the STATCOm, but also low harmonics, excellent DC voltage balance and cooling performance. Through such demonstration, not only three key technologies for next-generation power electronics-based transmission controllers, which are advanced power switch technology, modular converter technology and its control technology, but also a next generation STATCOM benchmark with high performance and low cost is illustrated and ready for full-rating field test.

For the wind farm voltage fluctuation suppression using a CMC-based STATCOM, the methodology to conduct an impact study of a STATCOM on the integration of a large wind farm into a weak loop power system is described. The specific issues and solutions of the studied wind

farm system are illustrated. For the system study, the models for the system, wind farm and STATCOM are developed, and the system model is validated with field data.

From obtained PV and VQ curves from the simulation, the size and location of STATCOM and the system stability are assessed. It indicates that while low-cost MSCs and TCs boost the steady-state voltage locally but are ineffective to suppress the voltage fluctuations (seconds to minutes) due to their nature of slow dynamic response, a 10MVAr STATCOM, which is a small percentage of wind farm rating, cannot only effectively suppress the voltage fluctuations of the wind farm and the whole 69kV loop system, but also inherently reduce the operation times of MSCs and TCs in the system so that the maintenance and replacement cost of MSCs, TCs and wind turbines can be reduced, and the power quality issues related to the switching of MSCs and TCs can also be lessened. The results also show the location of STATCOM selected at 35kV bus 5, the secondary side of the wind farm main transformer, can be a good tradeoff from cost-effectiveness point of view.

For this specific application of suppressing the wind farm voltage fluctuations, the dynamic simulation results for a continuous operation period also verify the effectiveness of the proposed STATCOM and its control strategy, which can adaptively deal with voltage fluctuation independent from a system steady-state voltage regulation by operations of MSCs and TCs, and even possibly mitigate the faster voltage fluctuations and flicker emissions from wind farms with a well-designed fast control bandwidth. Therefore, the effectiveness of the installation of a 10MVAr STATCOM system for integrating the specific 50MVA wind farm into the weak loop power system is verified.

To deal with the EAF flicker mitigation using a CMC-based STATCOM, with a specific studied EAF case, the steady-state analysis gives a generalized relationship of $\Delta V_{PCC}/V_{PCC}$, Q_C/S_{EAF}, and X_S/R_S and provides the steady-state evaluation of STATCOM's size for flicker mitigation, which is verified by the steady-state simulation results.

Based on the field data from 45 MVA EAF installed at TVA, the flicker mitigation and reactive power compensation requirements are quantitatively analyzed. The various compensation solutions are qualitatively compared, such as passive filter, SVC, and STATCOM. In addition, a field data-based EAF model is proposed and validated by simulation results. The simulation results based on field data show that a 4.5MVA rated STATCOM can, to some extent, mitigate voltage flicker caused by an 45 MVA EAF, whereas a 30 MVA rated STATCOM can completely mitigate the voltage flicker. The additional 14MVAr capacitor bank with the STATCOM improves the load power factor and bus voltage profile. These simulation results verify the steady-state analysis results. The effectiveness of STATCOM-based flicker compensator is also validated by the simulation.

For the modeling and control of the EAF flicker mitigation using a CMC-based STATCOM, an EAF worst-case model is proposed so that the deterministic impedance of EAF at specific operating points can be evaluated, which cannot be accomplished by previous EAF models mainly for harmonics analysis. Combining the developed small-signal models of a worst-case EAF flicker and a CMC-based STATCOM, a generalized hybrid model in dq0 frame of a system-EAF-STATCOM is obtained and STATCOM control-to-Vpcc is derived. With the derived transfer function, the model-based control strategy of CMC-based STATCOM for EAF flicker mitigation is proposed and, other than trial-and-error tuning in previous design, the TF-

based compensator design of the STATCOM external voltage loop gives the system a desired control bandwidth and stability margin.

To further verify the modeling and control of CMC-based STATCOM for EAF flicker mitigation, a scaled-down real-time TNA integrating CMC-based STATCOM with its digital controller and EAF flicker model is demonstrated. Compared to the simulation results, the TNA experiment results are matched very well with each other, and show that the CMC-based STATCOM system efficiently and rapidly mitigates the EAF flickers, and consistently verify the model and controller design, which provides the confidence for a future field demonstration of a CMC-based STATCOM for EAF flicker mitigation.

Finally, the modeling, integration, and control of a UESS energy storage system are presented in details. The UCAP model is obtained through UCAP cell testing, and the full-size 2kV UCAP model parameters are extracted from the discharge experiment. Considering the features of UCAPs and modular VSCs, the potential issues of UCAP for high power operation are pointed out, and an effective and simple interface to integrate the UCAP and modular VSCs is proposed so that the UCAP's lifetime is extended by filtering its carrying high frequency components and the convertability between STATCOM and UESS is convenient and the bulky and costly DC-DC interface circuit is eliminated. With the developed UCAP and CMC model and proposed interface, the control strategy is designed for the UESS system. The simulation results verify the UESS modeling and design. With the developed scaled-down UESS TNA system, the experimental TNA results consistently verify the simulation results, and also validate the modeling and design of the proposed UESS.

In summary, by combining the advantages of the ETO semiconductor device, a CMC topology and its control technology, and a UCAP energy storage, STATCOM/UESS systems are promising FACTS/ESSs for high-power applications. It is expected that the successful demonstration of STATCOM/UESS technology will result in a FACTS/ESS that is capable of extremely fast response and that is less costly per kW/kVA than FACTS/ESSs based on traditional energy storage/power electronics technologies and the increasing application of such FACTS/ESS controllers in utility power system.

6.2 Future Research

Although this dissertation has covered many of the interesting issues and challenges of the CMC-based STATCOM, additional work has been left for future research. The first part is advanced control of STATCOM/UESS, such as unbalanced control and/or per-phase control so that the STATCOM/UESS can deal with the more complicate system scenarios, such as a single-phase system, or an unbalanced system.

The second part is the fault-protection study for the CMC-based STATCOM. Due to the excessive number of semiconductor devices and passive components, how to design a fault-protection scheme to enhance the redundancy and ride-through capability in various fault scenarios remains an important challenge.

The last part is the external control design of the CMC-based UESS system. Although the integration and internal control of a UESS has been proposed and verified, for the utility application, such as EAF flicker mitigation and renewable wind power support, an external

control strategy is needed to maintain UESS energy within its limitations and coordinate the real power and reactive power output of UESS to realize a stable and cost-effective application.

REFERENCES

A. Flexible AC Transmission Systems

[A1] N. G. Hingorani and L. Gyugyi, "Understanding FACTS: concepts and technology of flexible AC transmission systems," IEEE Press, 2000.

[A2] M. Noroozian, A.N. Petersson, B. Thorvaldson, B.A. Nilsson, C.W. Taylor, "Benefits of SVC and STATCOM for electric utility application," IEEE-PES TDCE, vol. 3, pp. 1192-1199, Sept. 2003.

[A3] H. Akagi, "Active Harmonic Filters," in proc of the IEEE, vol. 93, no. 12, pp. 2128- 214. Dec 2005.

[A4] J. Sun, L. Hopkins, B. Shperling, B. Fardanesh, M. Graham, M. Parisi, S. MacDonald, S. Bhattacharya, S. Berkowitz, A. Edris, "Operating characteristics of the convertible static compensator on the 345 kV network," in proc of IEEE-PSCE, vol. 2, pp. 732-738. Oct. 2004.

B. Energy Storage Systems

[B1] Energy Storage Technologies and Applications Information, electricity storage association website.

[B2] W. V. Hassenzahl, "Superconducting Magnetic Energy Storage," Proc. IEEE, vol. 71, no.9, pp. 1089-1098, Sept. 1983.

[B3] R. H. Lasseter and S. G. Jalali, "Power conditioning systems for superconductive magnetic energy storage," IEEE Trans. Energy Convers., vol. 6, no. 3, pp. 381–387, Sept. 1991.

[B4] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Arsoy, Y. Liu, "Energy storage systems for advanced power applications," Proc. IEEE, vol. 89, no. 12, pp. 1744-1756, Dec. 2001.

[B5] A. B. Arsoy, Y. Liu, P. F. Ribeiro, F. Wang, "StatCom-SMES", IEEE Ind. Appl. Magazine, vol. 9, no. 2, pp. 21-28, Mar. 2003.

[B6] I. N. Varakin, A. B. Stepanov, V. V. Menukhov, "Capacitor With a Double Electrical Layer," PCT/RU 95/00171 (14 Aug. 1995), A. B. Stepanov, I. N. Varakin, V. V. Menukhov. US patent 5, 986, 876 {11 Apr. 1997}.

[B7] I. N. Varakin, A. D. Klementov, S. V. Litvinenko, N. F. Starodubtsev, A. B. Stepanov, "Application of Ultracapacitors as Traction Energy Sources," Proc. 7th International Seminar on Double Layer Capacitors and Similar Energy Storage Devices, Dec. 8-10, 1997, Florida, USA.

[B8] Ultracapacitor 30EC402 and 30EC502 Datasheet, available: esma-cap website.

[B9] Chong Han, Alex Q Huang, Ding Li, Haresh Kamath, Mike Ingram, Stanley Atcitty, "Modeling and Design of a Transmission Ultracapacitor (TUCAP) Integrating Modular Voltage Source Converter with Ultracapacitor Energy Storage," in *proc of IEEE-APEC*, pp. 1104-1110, Mar. 2006.

[B10] Chong Han, Alex Q. Huang, etc., "Progress on a Transmission Ultracapacitor (TUCAP) based on ETO thyristor and Ultracapacitor Energy Storage," in *EESAT conference*, Nov. 2005.

C. Electric Arc Furnace Flicker Mitigation

[C1] S. R. Mendis, M. T. Bishop, and J. F. Witte, "Investigations of voltage flicker in electric arc furnace power systems," IEEE Industry Applications Magazine, vol. 2, no. 1, Jan.-Feb.1996, pp. 28 – 34.

[C2] G. C. Montanari, M. Loggini, L. Pitti, E. Tironi, and D. Zaninelli, "The effects of series inductors for flicker reduction in electric power systems supplying arc furnaces," IEEE IAS'93, vol. 2, Oct. 1993, pp. 1496 – 1503.

[C3] C. D. Schauder, "STATCOM for compensation of large electric arc furnace installations," IEEE PES summer meeting, vol. 2, July 1999, pp. 1109 - 1112.

[C4] A. Garcia-Cerrada, P. Garcia-Gonzalez, R. Collantes, T. Gomez, and J. Anzola, "Comparison of thyristor-controlled reactors and voltage-source inverters for compensation of flicker caused by arc furnaces," IEEE Trans. Power Delivery, vol. 15, no. 4, Oct. 2000, pp. 1225 – 1231.

[C5] Tongxin Zheng, and E. B. Makram, "An adaptive arc furnace model," IEEE Trans. Power Delivery, vol. 15, no. 3, July 2000, pp. 931 - 939.

[C6] S. Varadan, E. B. Makram, and A. A. Girgis, "A new time domain voltage source model for an arc furnace using EMTP," IEEE Trans. Power Delivery, vol. 11, no. 3, July 1996, pp. 1685 – 1691.

[C7] J. G. Mayordomo, L. F. Beites, R. Asensi, M. Izzeddine, L. Zabala, and J. Amantegui, "A new frequency domain arc furnace model for iterative harmonic analysis," IEEE Trans. Power Delivery, vol. 12, no. 4, Oct. 1997, pp. 1771 - 1778.

[C8] Li Zhang, Yilu Liu, Michael R. Ingram, Dale T. Bradshaw, Steve Eckroad, and Mariesa L. Crow, "EAF Voltage Flicker Mitigation By FACTS/ESS," *IEEE PES Power Systems Conference & Exposition*, vol. 1, Oct. 2004, pp. 372-378.

[C9] IEEE std 519-1992 "IEEE recommended practices and requirements for harmonic control in electrical power systems," April 1993.

[C10] Chong Han, Z. Yang, Bin Chen, Alex Q. Huang, Bin Zhang, Mike Ingram, Aty Edris, "Evaluation of Cascade-Multilevel Converter based STATCOM for Arc Furnace Flicker Mitigation," to appear in IEEE Trans. Industry Application, *2007*

[C11] Chong Han, Zhaoning Yang, Alex Q. Huang, Mike Ingram, "Modeling and Control of a Cascade-Multilevel Converter-Based STATCOM for Electric Arc Furnace Flicker Mitigation," in *Proc. IEEE-IECON*, pp. 883 – 888, Nov 2005

[C12] Tomas Larrson, C. Poumarede, "STATCOM, an efficient means for flicker mitigation," in *Proc. IEEE PES winter meeting 1999*, vol. 2, pp. 1208 – 1213, Jan. 1999.

[C13] Li Zhang, Yilu Liu, Chong Han, Zhong Du, Alex Q. Huang, Michael Ingram, "Mitigation of EAF Induced Problems," in proc. of IEEE PSCE'06, Oct. 2006.

[C14] Chong Han, Alex Q. Huang, Subhashish Bhattacharya, Mike Ingram, "Field Data-based Study on Electric Arc Furnace Flicker Mitigation," in proc. of IEEE-IAS'06, Oct. 2006.

D. Semiconductor Device

[D1] Yuxin Li; Huang, A.Q.; Lee, F.C. "Introducing the emitter turn-off thyristor (ETO)", Industry Applications Conference, 1998. Volume 2, 12-15 Oct. 1998 Page(s):860 - 864 vol.2

[D2] B. Zhang, A. Q. Huang, Y. Liu, and S. Atcitty, "Performance of the new generation emitter turn-off (ETO) thyristor," in *Proc. IEEE-IAS*, 2002, pp. 559-563.

[D3] B. Zhang, Y. Liu, X. Zhou, J. Hawley, and A. Q. Huang, "The high power and high frequency operation of the emitter turn-off (ETO) thyristor," in *Proc. IEEE-IECON*, 2003, pp. 1167-1172.

[D4] Zhenxue Xu, Bin Zhang, S. Sirisukprasert, Xigen Zhou, Alex Q. Huang, "The emitter turn-off thyristor-based DC circuit breaker," IEEE PES Winter Meeting, vol. 1, pp. 288-293, Jan. 2002.

[D5] Tiger Zhou, Alex Q. Huang, "ETO-based DC Circuit Breaker," US patent.

[D6] Alex Q. Huang, Bin Chen, Chong Han, Zhong Du, Subhashish Bhattacharya, Mesut Baran, Abdel-Aty Edris, Mike Ingram, Stanley Atcitty, "Emitter Turn-Off (ETO) Thyristor: An Emerging Power Semiconductor Switch with Lower Cost, Improved Reliability and Scalability of FACTS Controllers", CIGRE 2006, B4-107, Aug 2006.

[D7] ABB IGCT, 5SHY 35L4511, data sheet

[D8] Mitsubishi CM900HB-90H IGBT datasheet

E. Cascaded-Multilevel Converters

[E1] J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," *IEEE Trans. Ind. Applicat.*, vol. 32, May/June 1996, pp. 509–517.

[E2] F. Z. Peng and J. S. Lai, "Multilevel cascade voltage-source inverter with separate DC sources," *U.S. Patent 5 642 275*, June 24, 1997.

[E3] Siriroj Sirisukprasert, "The Modeling and Control of a Cascaded-Multilevel Converter-Based STATCOM", Ph.D. Dissertation, Feb 2004, Blacksburg, Virginia.

[E4] S. Sirisukprasert, A. Q. Huang, and J. S. Lai, "Modeling, analysis and control of cascaded-multilevel converter-based STATCOM," in *Proc. IEEE-PES general meeting*, 2003, vol. 4, July 2003, pp. 13–17.

[E5] Chong Han, Zhaoning Yang, Bin Chen, Wenchao Song, Alex Q. Huang, Abdel-Aty Edris, Mike Ingram, Stanley Atcitty, "System Integration and Demonstration of a 4.5 MVA STATCOM based on Emitter Turn-Off (ETO) Thyristor and Cascade Multilevel Converter", in proc-IECON'05, Nov 2005, pp. 1329-1334.

[E6] Yiqiao Liang, C.O. Nwankpa, "A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM," IEEE trans on Industry Applications, vol. 35, no. 5, pp. 1118 – 1123, Sept 1999.

[E7] *Colin Davidson,* "Glenbrook STATCOM Design", presentation only, Areva, A2, FACTS users' group meeting 2005.

[E8] F. Z. Peng, J. S. Lai, J.W. McKeever, J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static VAr generation," *IEEE trans on industry appl,* vol. 32, no. 5, pp. 1130-1138, Sept. 1996.

[E9] F. Z. Peng, J. S. Lai, "Dynamic performance and control of a static VAr generator using cascade multilevel inverters," *IEEE trans on industry appl,* vol. 33, no. 3, pp. 748-755, May. 1997.

[E10] Chong Han, Bin Chen, Karan Tewari, Wei Liu, Alex Q. Huang, Mike Ingram, Abdel-Aty Edris, "An ETO Thyristor and Modular H-bridge PWM Converter-based 4.5MVA STATCOM: 480V/500A Transformerless Grid-Connected Experimentation", in proc-IEEE-IAS'06, Oct 2006.

[E11] Y.D. Han, etc, "Demonstration of a ±50Mvar STATCOM", presentation only, FACTS research group, Tsinghua University, April 2006.

[E12] Chong Han, Alex Q. Huang, "A Generalized Control Strategy of Per-Phase DC Voltage Balancing for Cascaded Multilevel Converter-based STATCOM," submit to *IEEE-PESC'07*, June. 2007.

F. Multilevel Voltage Source Converters

[F1] J. Rodriguez, J. S. Lai and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, Aug. 2002, pp. 724-738.

[F2] S. Sirisukprasert, Z. Xu, B. Zhang, J. S. Lai, and A. Q. Huang, "A high-frequency 1.5 MVA H-bridge building block for cascaded multilevel converters using emitter turn-off thyristor," in *Proc. IEEE-APEC*, 2002, pp. 27–32.

[F3] S. Bhathachaya, "Series Connected IGCT based High Power Three-Level Neutral Point Clamped Voltage Source Inverter Pole for FACTS Applications," in proc of IEEE-PESC, pp. 2315-2321, June 2005.

[F4] D. Soto, T.C. Green, "A comparison of high-power converter topologies for the implementation of FACTS controllers," IEEE trans on Industrial Electronics, vo. 49, no. 5, pp. 1072-1080, Oct 2002.

G. *Miscellaneous*

[G1] Dushan Boroyevich, "Modeling and Control of Three-phase PWM converter", course slides, Virginia Tech, 2002.

[G2] Frec C. Lee, "Power Converter Modeling and Control", course slides, Virginia Tech, 2001.

[G3] Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics, 2nd edition, Kluwer Academic Publisher, 2000.

[G4] J.C. Das, "Passive Filters – potentialities and limitations", IEEE trans on IAS, vol. 40, no. 1, pp. 232-241, Jan. 2004.

H. *Wind Power*

[H1] *Wind Power Today and Tomorrow: an Overview of the Wind and Hydropower Technologies Program,* U.S. DOE and NREL, 2004, [Online]. Available: http://www.nrel.gov/wind/.

[H2] Thomas Ackermann, *Wind Power in Power Systems*, Wiley, 2005.

[H3] J. W. Smith, D. L. Brooks, "Voltage impacts of distributed wind generation on rural distribution feeders," IEEE PES TDCE, vol. 1, pp. 492- 497, 28 Oct.-2 Nov. 2001.

[H4] A. Kehrli, M. Ross, "Understanding grid integration issues at wind farms and solutions using voltage source converter FACTS technology," IEEE PES general meeting, vol. 3, pp. 1822 - 1827, July 2003.

[H5] Z. Saad-Saoud, M. L. Lisboa, J. B. Ekanayake, N. Jenkins, G. Strbac, "Application of STATCOMs to wind farms," IEE Proc of Generation, Transmission and Distribution, vol. 145, no. 5, pp. 511 – 516, Sept. 1998.

[H6] F. Zhou, G. Joos, C. Abbey, "Voltage stability in weak connection wind farms," IEEE PES general meeting, pp. 610 - 615, June 2005.

[H7] L. T. Ha, T. K. Saha, "Investigation of power loss and voltage stability limits for large wind farm connections to a subtransmission network," IEEE PES general meeting, vol.2, pp. 2251 - 2256, June 2004.

[H8] E. Muljadi, Y. Wan, C. P. Butterfield, B. Parsons, "A study of a wind farm power system" Preprint. 14 pp.; NICH Report No. CP-500-30814, 2002,[Online]. Available: http://www.nrel.gov/docs/fy02osti/30814.pdf.

[H9] C. W. Taylor, *Power System Voltage Stability*, McGraw-Hill, 1994.

[H10] P. Kundur, *Power Stability and Control*, ch. 14, McGraw-Hill, 1994.

[H11] T. V. Cutsem, and C. Vournas, *Voltage Stability of Electric Power Systems*, Kluwer Academic Publishers, 1998.

[H12] A. Larsson, "Flicker emission of wind turbines during continuous operation," *IEEE Trans. Energy Conversion*, vol. 17, No. 1, pp. 114-118, Mar. 2002.

[H13] A. Larsson, "Flicker emission of wind turbines caused by switching operations," *IEEE Trans. Energy Conversion*, vol. 17, No. 1, pp. 119-123, Mar. 2002.

[H14] Chong Han, Alex Q Huang, Mesut Baran, Subhashish Bhattacharya, Wayne Litzenberger, Loren Anderson, Anders Johnson, Abdel-Aty Edris, "STATCOM Impact Study on the Integration of a Large Wind Farm into a Weak Loop Power System," to appear in *IEEE Trans. Energy Conversion*, Special issue on Wind Power, 2007.