ABSTRACT

Lee, Yi-Mu. Breakdown and reliability of CMOS devices with stacked oxide/nitride and oxynitride gate dielectrics prepared by RPECVD. (Under the direction of Professor Gerald Lucovsky)

Remote-plasma-enhanced CVD (RPECVD) silicon nitride and silicon oxynitride alloys have been proposed to be the attractive alternatives to replace conventional oxides as the CMOS logic and memory technology node is scaled beyond 100 nm. This dissertation is focused on the degradation and breakdown of RPECVD stacked oxide/nitride (O/N) and oxynitride gate dielectrics under constant-current stress (CCS) and constant-voltage stress (CVS). By monitoring the time-to-breakdown of the dielectrics, the device reliability can be determined and further used to evaluate the dielectric quality and the scaling limits of the dielectric thickness.

It is found that the breakdown behavior of the gate oxide and RPECVD gate dielectrics is influenced by the degree of boron penetration, which in turn leads to increases in the gate leakage current. During electrical stresses, positive charges and hole trapping are generated at the Si/SiO_2 interface and also in the dielectric layer, resulting in device degradation and final breakdown. We successfully use the RPECVD technique to incorporate an ultrathin (~0.6 nm) interfacial oxide layer and one monolayer of nitrogen in the gate stacks to improve the interface properties. Therefore, the stress-induced charges and trapping are suppressed and the device performance including SILC, threshold voltage instability, drive current and switching

characteristics is improved. In addition, shorter-channel devices show more degraded electrical properties compared to longer-channel devices due to the increased damaged region in the gate-drain overlap near the channel.

The TDDB reliability and lifetime of MOS devices with RPECVD O/N gate dielectric for the foreseeable mobile application are also investigated. This study is the first to reveal the trend of Weibull slopes and activation energy of O/N gate stacks. It has been found that Poisson area scaling is valid for O/N gate stack, indicating that the intrinsic breakdown is a random process and can be explained by the percolation model. Also, the voltage and temperature acceleration parameters are determined from TDDB. The projection of device lifetime based on total chip area and low percentile failure rate is demonstrated. The maximum tolerable operating voltage for a total gate area of 0.1 cm^2 and 0.01% failure rate at 125 °C is projected to be 1.9 V for 2.07 nm stacked O/N gate dielectrics.

Breakdown and Reliability of CMOS Devices with Stacked Oxide/Nitride and Oxynitride Gate Dielectrics Prepared by RPECVD

by

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Biography

Yi-Mu Lee was born in Kaohsiung, Taiwan, on November 14, 1970. He obtained his B.S. (Chem. Eng.) degree from National Cheng Kung University (Tainan, Taiwan) in 1993. After his undergraduate studies, he served in the R.O.C. Air Force for two years in Kaohsiung. From 1995~1996, he worked in the Reaction Dynamic Laboratory (under Dr. Yuan-Tseh Lee) of the Institute of Atomic and Molecular Science (IAMS), Acedemia Sinica, Taipei, Taiwan. He proceeded to the United States to study at the University of Missouri-Columbia, where he graduated with his M.S. (Chem. Eng.) in 1998 under the guidance of Professor D. Viswanath. Thereafter, he enrolled in the Ph.D. program at North Carolina State University, Raleigh. He joined the Electrical and Computer Engineering program and was awarded Fellowship by the Center for Advanced Electronic Material Processing. During the course of his research under the direction of Professor Gerald Lucovsky and Carlton Osburn, he achieved the reliability and lifetime projection of ultrathin oxide/nitride (O/N) and silicon oxynitride stacked layer as gate dielectrics for advanced CMOS technology.

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List of Abbreviations and Symbols

Symbol	Description
C_g:	Gate capacitance (F)
C_{ox}:	Oxide capacitance per unit area (F/cm^2)
D_{ot}:	Stress-induced oxide trap density (C/cm^3)
E_a:	Activation energy (eV)
E_{ox}:	Electric field across the oxide (V/cm)
EOT:	Equivalent oxide thickness (nm)
F(t):	Cumulative failure function
G_m:	Transconductance (S)
I_{dsat}:	MOSFET saturation current (A)
J:	Current density (A/cm^2)
K_B:	Boltzmann's constant (eV/K)
K_T:	Temperature acceleration factor
LPDR:	Local physically damaged region
m*:	Effective electron mass (kg)
P_{gen}:	Defect generation rate (cm^2/C)
q:	Electron charge (C)
Q_{BD}:	Charge-to-breakdown (C)
RPECVD:	Remote-Plasma-Enhanced Chemical Vapor Deposition
RPAO:	Remote-Plasma-Assisted Oxidation

SILC:	Stress-Induced Leakage Current
T:	Absolute temperature (K)
$T_{63\%}$:	T_{BD} at 63.2%
T_{BD}:	Time to breakdown (sec)
TDDB:	Time Dependent Dielectric Breakdown
$T_{eq\text{-}ox}$:	Equivalent oxide thickness (nm)
V_{FB}:	Flatband voltage (V)
V_{postbd}:	Post-breakdown voltage (V)
V_t:	Threshold voltage (V)
Ψ_{ox}:	Potential drop across the oxide (V)
Ψ_s:	Surface potential of silicon substrate (V)
$\Psi(x)$:	The amount of band bending at position x (V)
α:	Characteristic time-to-breakdown (sec)
β:	Weibull distribution slope (Weibull shape factor)
χ:	Semiconductor electron affinity (eV)
ε_{si}:	Permittivity of silicon (= $11.7\varepsilon_0$) (F/cm)
ϕ_{ms}:	Work function difference between gate and substrate (V)
γ:	Voltage acceleration factor (decade/V)
μ_{eff}:	Effective mobility (cm^2/V-s)
ρ:	Charge density per unit volume (C/cm^3)

CHAPTER 1

INTRODUCTION

1.1 Motivation

Oxide/nitride and oxynitride gate dielectrics prepared by remote-plasma-enhanced CVD (RPECVD) have been proposed to be the attractive alternatives to replace ultrathin gate oxides due to the reduction of boron penetration and direct tunneling current [1]. Furthermore, the device properties such as threshold voltage shift, channel mobility and charge-to-breakdown under constant current stressing are also improved [1, 2]. This dissertation is focused on the investigation of the degradation and breakdown characteristics of RPECVD oxide/nitride and oxynitride gate stacks in order to evaluate charge trapping behaviors and the changes in device performance during electrical stresses. TDDB reliability and lifetime projection are also discussed in this dissertation.

1.1.1 Oxide Degradation and Breakdown Mechanisms

Oxide degradation and breakdown have received increasing attention since they cause failure in advanced ULSI devices and, therefore, may impede the downscaling trend of oxide thickness and MOSFET size [3-5]. It is widely accepted that the breakdown of thin gate oxides is a two-stage mechanism, degradation of oxide films followed by breakdown [6, 7]. During the first stage, the immigration of hydrogen [8, 9] and injection of hot electrons [9] impact the Si/SiO_2 interface, which

damage gate oxides [8] by creating fast interface states [10-12] and positively charged slow traps [13]. Apte et al. [14] observed that the damage is mainly located at the Si/SiO_2 interface, and also demonstrated that the interfacial damage and degradation consisting of broken bonds is a critical precursor of oxide breakdown. Oxide degradation was also studied from the viewpoint of energy release. It has been proposed that the oxide films are damaged by the generation of the positively charged species due to the release of electron energy near the anode interface [15].

In the second stage, two different breakdown modes, soft breakdown (SBD) and hard breakdown (HBD), have been observed in very thin gate oxides (< ~5 nm) [16]. The SBD and HBD are believed to have the same physical origin [16], that is the local formation of a permanent conductive path between cathode and anode electrode due to the generation of defect and charge trapping in the bulk oxide [17] and the Si/SiO_2 interface [18]. In other words, both SBD and HBD events result from the opening of a percolation channel between the gate and the substrate [16]. SBD events, first identified by Okada et al. [19], show permanent multilevel gate fluctuations. It is believed that the injected electrons which transport through the oxide conduction band can trigger SBD [20] by creating a conductive path [14] due to localized physical damage [21]. The transformation from SBD to HBD is determined by the location of oxide breakdown spots, thermal energy for device discharge, and resistance of the percolation path [22]. Following the first SBD, the second breakdown event (SBD or HBD) also occurs randomly over the device area by showing a Poisson distribution of

the residual time [16]. The SBD and HBD phenomena explained by the percolation model related to the trap generation are illustrated more detail in Appendix C.1.

The concept of the critical defect density at breakdown was first introduced to investigate HBD phenomena by Sune et al. [7]. As the critical density of traps is reached, the gate oxide becomes destructive breakdown (i.e., HBD) [7, 23, 24]. Pantisano et al. [5] further proposed the concept of a critical density of neutral traps. They suggested that the neutral traps could capture an electron to become negative traps or capture a hole to become positive traps; both positive and negative traps can trigger the oxide breakdown. It has been shown that the value of the critical defect density for breakdown is around $5x10^{13}$ /cm^2 for thicker oxides (> 5 nm) [25], and this value can be used to predict the charge-to-breakdown (Q_{BD}) as well as defect generation rate [26].

It is well known that the breakdown modes of ultrathin oxide can be distinguished from the excessive leakage current at low field under high-field stress [27]. The post-breakdown I-V curves show the evolution from exponential I(V) after SBD to linear I(V) after HBD [28]. The huge difference between SBD and HBD leakage currents is due to the fact that the area of the HBD spots is larger than that of SBD spots based on the quantum point contact theory [29]. The increase in gate leakage current is referred to as the stress-induced leakage current (SILC), which is attributed to the reduction of the barrier height [30] resulting from the generation of

interfacial traps [3, 31] and positive charges [6, 11, 12]. A schematic illustrating this phenomenon is shown in Appendix B.3. Therefore SILC characteristics provide a direct evidence of charge trapping in the oxide [3]. Meanwhile, trapping or detrapping of holes or electrons also shows the transient SILC phenomena during Fowler-Nordheim stressing [8]. In ultrathin oxides with large direct tunneling, the increment of SILC is used to predict oxide breakdown due to its larger sensitivity [32]. The SILC will increase the densities of dangling bonds in the oxide [30], and degrade oxide quality by enlarging defect area [27]. Thermally trap-assisted tunneling through the locally reduced barrier height is generally accepted to be responsible for the SILC conduction mechanism [27], which is related to bulk oxide traps [33]. In other words, these traps generated in the oxide layer can serve as intermediate hopping sites, which enhance electron conduction between the anode and cathode [34]. It has been demonstrated that the SILC can be reduced by thermal nitridation process [8] and RPECVD technique, and the dielectric degradation and breakdown can be improved as well [35].

1.1.2 Reliability and Scaling Limit of SiO_2 gate dielectric

As the gate oxide thickness aggressively scales down, the increasing gate leakage current presents a major concern for deep submicron MOS technologies [15, 36]. During oxide degradation, SBD of an individual transistor does not induce significant degradation and device failure [37, 38]; however, the oxide lifetime is still limited by the larger chip-level off-leakage current enhanced by defect generation and

the SBD-mode SILC [39]. It has also been shown that charge-to-breakdown decreases with decreasing oxide thickness due to the reduction of the critical defect density under CVS [40]. In these regards, the reliability of ultrathin gate dielectrics will soon become another limiting factor for future ULSI development and manufacturing with the specification of 0.01% failure rate, total effective oxide area on a chip and ten-year lifetime [36]. Thus an accurate evaluation of ultrathin oxide reliability is required to determine the ultimate limit of gate oxide thickness [15, 41].

The scaling limit of the gate oxides has been proposed to be 1.4 nm due to the limitation of the direct tunneling [42], and to be about 2.2~2.6 nm for a 1 V supply voltage at room temperature [40]. The minimum oxide thickness with the consideration of the time to SBD was predicted to be 2.2 nm [40]. It has been proposed that high-k dielectrics and SiO_2-based dielectrics with nitrogen incorporation can provide better reliability [40, 43]. This is because larger physical dielectric thickness can increase time-to-breakdown (t_{BD}) by decreasing the leakage current [40].

N/O dual layer dielectrics [44] and silicon oxynitrides [45-49] have shown improved reliability compared to gate oxides, as well as reduced leakage current and boron penetration. This dissertation will investigate the reliability characteristics and device lifetime for RPECVD O/N and oxynitride gate stacks under constant voltage stress. These results along with the direct leakage current, will provide important information for future scaling of nitrided gate dielectrics.

1.2 RPECVD Oxide/Nitride and Oxynitride Gate Dielectric Stacks

Silicon gate oxide shows intolerable direct leakage current (~10 A/cm^2 at 1 V) as the thickness is scaled down to ~1.5 nm compared to Fowler-Nordeim (F-N) tunneling current (~1x10^{-12} A/cm^2 at 1 V) at ~3.5 nm. It has been shown that the high direct tunneling leakage will limit charge storage application and the operation of CMOS devices [50]. This is because the large direct tunneling current removes carriers faster than they are thermally generated and prevents the formation of inversion layer in an MOS capacitor. MOS devices made with stacked nitride/oxide (N/O) [35] and silicon oxynitride dielectrics [51] prepared by remote-plasma-enhanced CVD (RPECVD) have been proposed to replace conventional SiO_2 in the gate stack due to their relatively high dielectric constants and low interface charge density, and are relatively easy for the integration of the fabrication process.

In our stacked RPECVD gate dielectrics, an ultrathin interfacial remote-plasma-assisted oxidation (RPAO) layer was first grown since it is required to improve the poor interface and mismatch between Si substrate and nitrided dielectrics [52-55]. The presence of oxide may reduce at least 2 orders of magnitude in interfacial defects by reducing the average bonding coordination according to constrain theory [55]. Both P- and NMOSFETs with the buffer RPAO layer have shown improved electrical performance and are comparable to thermal oxide devices [56, 57]. Next, following the RPAO step, RPECVD interface nitridation precisely

introduces nitrogen at one monolayer level at the Si/SiO_2 interface, which provides an effective barrier to prevent boron penetration into the Si/SiO_2 interface and silicon substrate, and thus improves the device reliability [35, 53, 55]. Finally, Si_3N_4 or oxynitride layer was deposited on the top to complete the sandwiched NON structure. It has been demonstrated that a ~0.8 nm top nitride layer, corresponding to ~$4.5x10^{15}/cm^2$, is required to effectively suppress boron diffusion out of the heavily doped p^+ polysilicon gate [35, 58]. The result is also consistent with required nitrogen content (~$8x10^{14}/cm^2$) for the reduction of boron penetration [59].

RPECVD N/O and Oxynitrides dual layers have shown the reduction of tunneling current and boron penetration effect, flatband voltage shift minimization, improvement of device mobility and reliability as compared to thermal gate oxide. However, there is a lack of studies of dielectric degradation and its impact on the reliability of CMOS devices during electrical stress. Therefore, the breakdown and reliability characteristics of RPECVD O/N and oxynitride gate dielectrics should be studied to evaluate the device lifetime and then provide a trend for continuous downscaling of their thickness.

1.3 Overview of Dissertation

The main scope of this dissertation is the studies of the degradation and breakdown phenomena of ultrathin RPECVD oxide/nitride (O/N) and oxynitride gate dielectrics under constant-current stress (CCS) and constant-voltage stress (CVS). At

first, devices were stressed at a condition where both SBD and HBD are monitored in order to investigate the dielectric degradation and the changes in electrical properties. Then the effects of interface properties and structure dependence on the breakdown and reliability will be evaluated. Finally, the TDDB distributions and the lifetime prediction of the devices are demonstrated by accelerated stress testing. Throughout this research, the time-to-breakdown (t_{BD}) is determined with a hard breakdown criterion.

In Chapter one, the degradation and breakdown behaviors of conventional gate oxides are briefly reviewed. The relation between trap generation and SILC is illustrated. The post-breakdown conduction mechanism in ultrathin oxides is also discussed. This post-breakdown leakage current severely degrades the device reliability and also limits the scaling of gate oxide thickness. The structures of PECVD oxide/nitride (O/N) and oxynitride gate stacks are introduced in details.

In Chapter two, SBD and HBD phenomena of stacked O/N and oxynitride dielectrics are investigated under CCS. The thermal oxides show larger degree of boron penetration compared to O/N and oxynitride gate stacks, thus the dielectric breakdown is seriously impacted. Post-breakdown leakage current and gate voltages are monitored as a function of time. Polarity dependence of dielectric breakdown is investigated to the Si_3N_4 (or oxynitride)/SiO_2 and SiO_2/Si interface properties. The electrical properties and device performance after stress are evaluated.

Chapter 3 discusses the influence of interface nitridation and RPAO thickness on dielectric degradation and breakdown behaviors by CVS technique. Stacked O/N dielectric received interface nitridation shows improved dielectric breakdown, SILC and electrical characteristics after stressing with a evidence of the suppression of hole trapping in the gate-to-drain overlap region. In addition, dielectric breakdown and TDDB reliability are improved for thinner RPAO oxynitride device, which can be explained by the oxide thinning effect and the percolation model.

Chapter 4 discusses the structural dependence on device degradation and performance under CVS test. The channel-length dependence of dielectric breakdown and the corresponding SILC from the evolution of increased tunneling current will be releaved. Experimental evidence shows more severe breakdown and device degradation in the threshold voltage, drain current and transconductance for shorter channel PMOSFETs. These degradations result from the enhancement of hole trapping in the gate-drain overlap region as evidenced by a positive off-state drain leakage current. It will be shown that the off-state drain leakage leads to hard breakdown, and the complete failure of device functionality.

Chapter 5 discusses the voltage and temperature dependence on the TDDB reliability. The reliability parameters such as defect generation rate, Weibull slope and activation energy are also evaluated. The projection of device lifetime with the combination of temperature acceleration, area scaling and low percentile failure rate is

demonstrated. The maximum tolerable operating voltage for 2.07 nm O/N gate dielectric at 125 °C will be determined.

Finally in Chapter 6, we will summarize and conclude this research, and also provide a direction for future work. Several appendices are also included in this dissertation.

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CHAPTER 2

Soft Breakdown and Hard Breakdown of MOS Devices with Stacked Oxide/Nitride and Oxynitride Dielectrics under Constant Current Stress

2.1 Introduction

Recently, several groups have investigated the breakdown phenomena of devices with nitride or 2.5 nm oxynitride dielectrics under a constant voltage stress (corresponding stress current ~ 25 A/cm^2 at –3.6 V) [1] and constant current stress of 1 A/cm^2 [2], respectively. It was shown that the appearance of soft breakdown (SBD) increases the gate noise, which becomes more significant in ultrathin oxides. In their studies, no significant device degradation was observed as a result of SBD and no hard breakdown (HBD) was detected as well.

In this chapter we will investigate the SBD and HBD characteristics of the thermal oxide, stacked O/N and oxynitride gate dielectrics with thickness of sub-2 nm under constant current stress (CCS). The preparation of stacked gate dielectrics by RPECVD technique and MOSFET fabrication will be described. The time evolution of gate voltages and SILC characteristics are used to monitor both SBD and HBD under either gate or substrate injection. The suppression mechanism of charge trapping associated with the blocking of boron diffusion will be discussed. The electrical degradation of the MOSFETs performance such as drain current, subthreshold swing and transconductance is evaluated.

2.2 Experimental and Measurement Procedures

MOS field-effect-transistors (FETs) were fabricated on 0.05~0.07 ohm-cm <100> n-type Silicon substrates. Prior to gate dielectrics deposition, all the wafers received 1% HF dip to remove the 10 nm sacrificial oxide followed by a water rinse. The control thermal oxide was grown in furnace with 4.5% HCl at 700 °C for thickness of 2.0 nm. For O/N and oxynitride dielectrics, a 0.6 nm interfacial bottom oxide was formed using remote O_2-plasma oxidation for 18 sec. 0.2 torr interface nitridation for 90 seconds is performed by plasma flows of 60 sccm N_2 and 200 sccm He mixture. The top nitride layer is deposited by N_2/He (60 sccm/200 sccm) and SiH_4 (10 sccm) mixtures; oxynitride layer is formed by N_2 (47 sccm), N_2O/He (13 sccm) and SiH_4 (10 sccm) plasma deposition. The processing is carried out at 300 °C to minimize OH incorporation into the interfacial oxide. All dielectric stacks then receive a post-deposition RTA at 900 °C for 30 seconds in He to reduce the hydrogen concentration and interface oxide charge in top dielectric layer [3, 4]. The RTA process also drives nitrogen into Si/SiO_2 interface of ON dielectrics and results in a NON gate stack. A 200 nm poly-Si gate is then deposited by LPCVD at 410 °C. The polysilicon gate was patterned and etched followed by a 10 nm poly-reoxidized layer that was deposited in dry O_2 furnace in order to reduce the ion impact and junction depths. Source/drain regions and p^+-poly gate are performed with BF_2 ion implantation (20 keV, $5x10^{15}cm^{-2}$). Afterwards, a 200 nm LTO was deposited to reduce the dopant diffusion effect during rapid thermal activation for 40 seconds at

1000 °C in Ar ambient. After patterning aluminum gate and backside metallization, post metallization anneal (PMA) was conducted in 400 °C forming gas for 30 mins to passivate the dangling bonds and neutralize oxide trapped charges (Q_{ot}). Equivalent oxide thickness ($T_{eq\text{-}ox}$) was determined from high-frequency C-V data in strong accumulation region with correction of quantum-mechanical effects [5]. An HP4155B semiconductor parameter analyzer was used to perform constant current stress (CCS) to the gate of 10 μm x 10 μm, with source/drain and substrate grounded. The constant gate current for gate and substrate injection were –200 μA and 10 μA, respectively, to monitor both SBD and HBD from voltage-time characteristics. The initial corresponding gate voltage was ranged from 3.8 to 4.8 V. All measurements were taken at room temperature.

2.3 Effect of Nitrogen Incorporation on Breakdown Phenomena

Figures 1 and 2 show the wear-out and breakdown characteristics of thermal oxide, stacked O/N and oxynitride dielectrics as a function of stressing time under CCS for substrate and gate injection, respectively. At the onset of SBD, the gate voltage was gradually decreased. This voltage drop is believed to be the threshold energy for trap generation [6], and is associated with the appearance of a new breakdown spot [7]. The thermal gate oxide shows an early breakdown at 15 sec and 800 sec under substrate and gate injection, respectively. It has been reported that

oxide failure at shorter stress times is attributed to boron penetration [8] and high trap generation rates [3].

Stacked O/N and oxynitride dielectrics with interface nitridation show multilevel SBD during CCS for both bias polarities as in Figures 1 and 2. Compared to thermal oxide, O/N and oxynitride stacks show much less voltage drop and fluctuation, which indicates that trap generation related to boron penetration is significantly suppressed. In other words, top nitride (or oxynitride) layer and interface nitridation build the barriers at the gate/dielectric and Si/SiO_2 interfaces, and effectively block boron penetration into the dielectric layer and the substrate. As a result, breakdown precursor density and the strained bonds can be reduced (more discussion in next session).

Figure 3 shows the post-breakdown voltage (V_{postbd}) for thermal oxide breakdown and RPECVD gate stacks (10k sec stressing) for substrate and gate injection. It is clearly seen that the V_{postbd} of the thermal oxide is much lower than that of O/N or oxynitride dielectrics. In other words, there are more traps generated in the thermal oxide, showing large gate voltage shifts. Figure 3 also reveals a polarity dependence on dielectric breakdown under CCS. It is found that thermal oxide shows lower V_{postbd} under substrate injection, implying that more damage is created at the Si/SiO_2 interface by hole trapping due to the energetic electrons, showing more noisy gate voltages (Figure 1). However, O/N and oxynitride dielectrics reveal similar

values of the V_{postbd} under both gate biases. This is due to the fact that nitrogen incorporation relaxes the interfacial strain [4], thus suppresses the defect generation and stress-induced damage at the Si/SiO_2 interface.

2.4 Reduction of post-breakdown leakage current in O/N and Oxynitride stacks

The flatband voltages of thermal oxide, stacked oxynitride and nitride dielectrics are 1.10 V, 0.97 V and 0.90 V with equivalent oxide thickness of 2.02, 1.98 and 1.83 nm, respectively. The thermal oxide shows larger positive flatband voltage due to boron penetration. Increases in leakage current for the thermal oxide device under gate and substrate injection stressing are shown in Figures 4(a) and 4(b), respectively. Ohmic I-V characteristics are observed, indicating the occurrence of HBD event which is consistent with a sudden drop from time-gate voltages characteristics as shown in Figures 1 and 2. Instead of H-X bond breakage for SBD, it has been shown that Si-Si bond breakage is responsible for HBD [9].

The B mode SILC (B-SILC) [10] can be observed in ultrathin oxides (<5 nm), which is resulted from the partial breakdown at a local spot. Figure 5 illustrates the B-SILC characteristics of O/N and oxynitride dielectrics between each stress interval under substrate injection. The transient B-SILC effect can be attributed to the charge trapping in the gate dielectrics and also the lowering of conduction band as illustrated in Appendix B. After stressing up to 10k sec, O/N and oxynitride dielectrics only

show exponential post-breakdown I-V curves, which is indicative of the occurrence of SBD. Figure 6 compares the post-breakdown gate leakage of various gate dielectrics. As can be seen, post-breakdown leakage current of O/N and oxynitride dielectrics are lowered by 2-3 orders of magnitude under substrate injection, and 1-2 orders of magnitude under gate injection compared to thermal oxides. It is noted that the degree of the reduction in leakage current is correlated with the effect of boron penetration. Boron penetration was shown to increase the number of strained Si-O and dangling bonds in the oxide film, and these low-energy strained bonds were easily broken during stress, resulting in an increased precursor density and charged trapping centers [8]. Moreover, these trapping centers resulting from boron penetration will enhance hole trapping during the stress, leading to early SBD [8]. In contrast, when boron atoms diffuse in Si_3N_4 or oxynitride alloy, B^+ hopping can be trapped in N atom sites and form greater binding energy B^+-N bonds than B^+-O bonds [11]. In other words, trap generation related to dangling bonds and precursor density is suppressed in the oxide layer of stacked dielectric devices [12]. Yamada et al. [13] also verified that the precursor density can be reduced by nitrogen incorporation. Therefore, O/N and oxynitide gate stacks with interface nitridation improve dielectric breakdown (Figures 1 and 2) and the post-breakdown leakage current (Figure 6).

2.5 Comparison of Device Degradation under CCS

Figure 7 shows I_d-V_g characteristics of the thermal oxide device before and after gate injection stressing. One can see negative ΔV_t which provide a direct

evidence of interface trap generation and positive charges trapped in the oxide film. After 100 sec of stress, transistors with thermal oxide exhibit significant V_t shift in negative direction due to the hole trapping, then lose the switching function by the degraded I_d and subthreshold swing. Other group also observed the similar hole trapping behavior in stacked N/O dielectrics under CCS [14]. The transistors with O/N or oxynitride gate dielectrics also display negative threshold voltage shift after 10k sec stress as shown in Figure 8. However, O/N and oxynitride transistors still show good switching characteristics since SBD does not completely destroy the device operation [2]. Figure 9 shows the degradation of transconductance (G_m) for gate dielectrics under CCS. It is found that the transistors with O/N or oxynitride gate dielectrics show less than 10% degradation of G_m for both bias polarities; however, thermal oxide shows around 38% and 62% degradation of G_m for gate and substrate injection, respectively. The serious decreases in G_m can lead to a significant degradation of channel mobility and drain current.

Figure 10 shows I_d-V_d characteristics of fresh and stressed PMOSFETs. For a transistor with thermal oxide, the positive off-state leakage current is observed as in Figure 10(a), implying a leakage path created between the gate and drain region due to the propagation of hole trapping. Therefore, holes can transport from the anode electrode to the cathode through the leakage channel, leading to the positive drain leakage. However, after 10k sec of stress, the devices with stacked oxynitride dielectrics do not show significant off-state drain leakage for both bias polarities, as is

revealed in Figure 10(b). In summary, the effect of hole trapping is detrimental to the performance of oxide devices; however, RPECVD O/N and oxynitride dielectrics show much less degradation in electrical properties after the same stressing. It can be concluded that N incorporation in stacked dielectrics and the SiO_2/Si interface provides a robust interface to retard the propagation of stress-induced hole trapping, which improves the drain leakage current.

2.6 Conclusions

This chapter has dealt primarily with the breakdown characteristics and the post-breakdown leakage current of sub-2.0 nm thermal oxide, RPECVD stacked O/N and oxynitride dielectrics under CCS. Thermal oxide shows early SBD and HBD for both gate and substrate injection. In contrast, stacked O/N and oxynitride dielectrics with interface nitridation display only SBD after 10k sec of stress. Transient characteristics of B-SILC from SBD to HBD are observed due to trap generation in the gate dielectrics. The leakage current and breakdown characteristics are improved because the stress-induced traps are suppressed due to the blocking of boron penetration. The positive traps are generated in the gate dielectrics as evidenced by a decrease of the magnitude of gate voltage and negative V_t shifts. Thermal oxide devices stressed under substrate injection show harder breakdown and severe degradation, implying a larger amount of the stress-induced damage created at the Si/SiO_2 interface. Stacked O/N and oxynitride devices with reduced post-breakdown leakage current also show less degradation in I_{dsat}, and subthreshold swing. It is

concluded that, during CCS, N incorporation provides a robust interface to improve the off-state leakage current and the device performance by suppressing the hole trapping.

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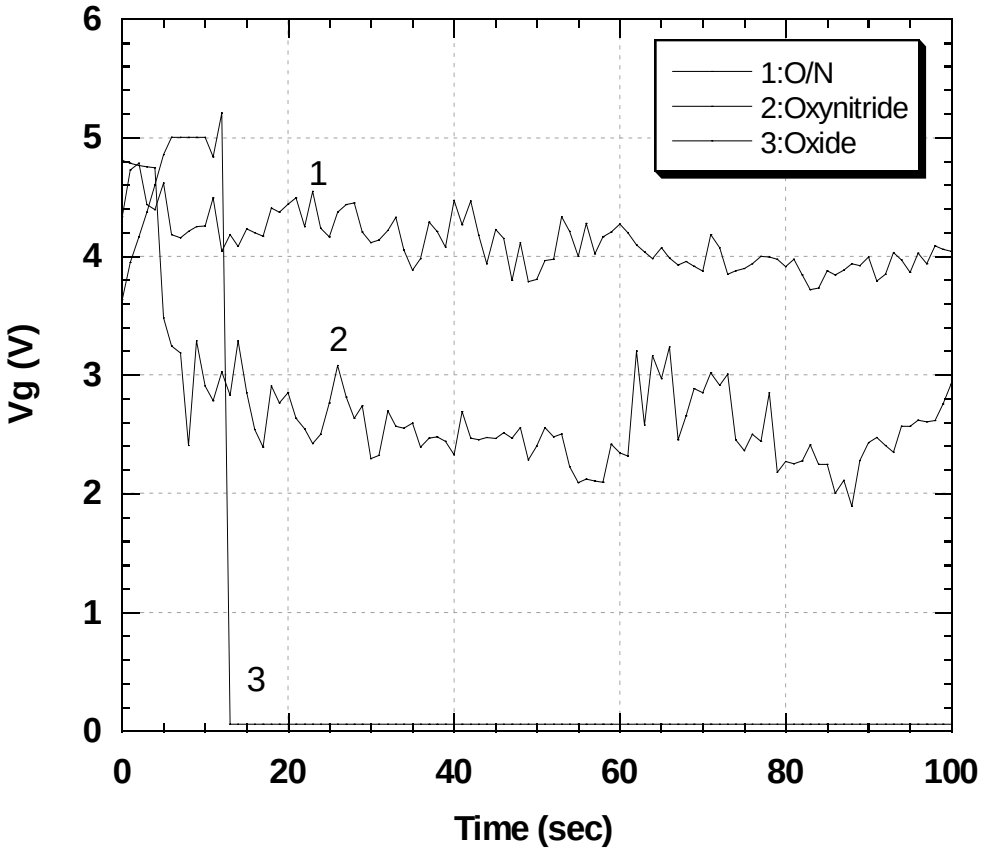


Figure 1 Time evolution of gate voltages for thermal oxide, O/N and oxide/oxynitride dielectrics (W/L = 10μm/10μm) under CCS for substrate injection.

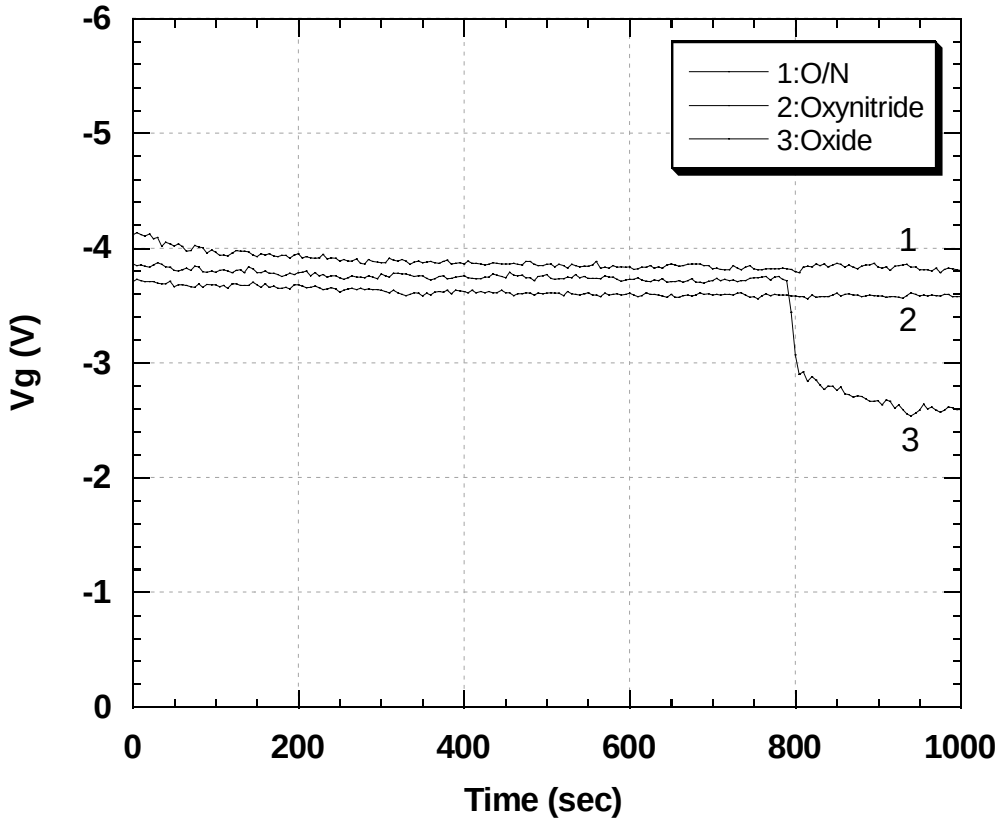


Figure 2 Time evolution of gate voltages for thermal oxide, O/N and oxide/oxynitride dielectrics (W/L = 10μm/10μm) under CCS for gate injection.

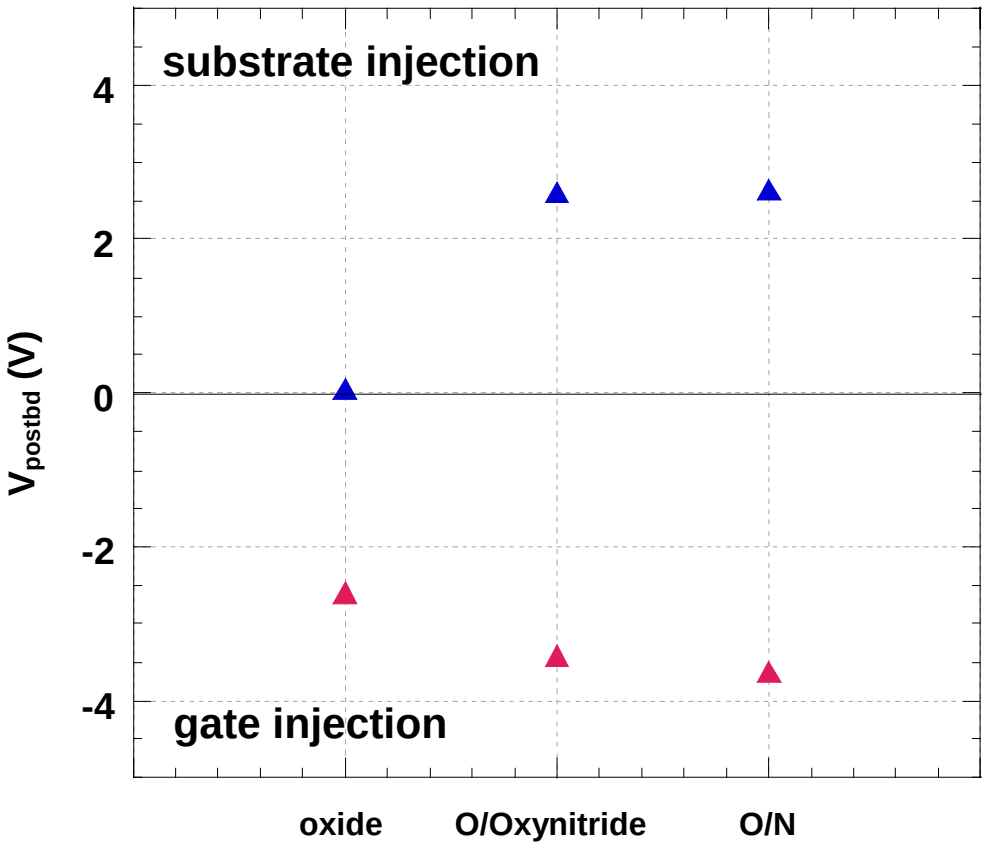


Figure 3 Post-breakdown gate voltages for thermal oxide (after HBD) and stacked oxide/nitride and oxynitride gate dielectrics (after 10k sec). The gate area is 10x10 μm^2. The initial corresponding gate voltage is around |4.3V|.

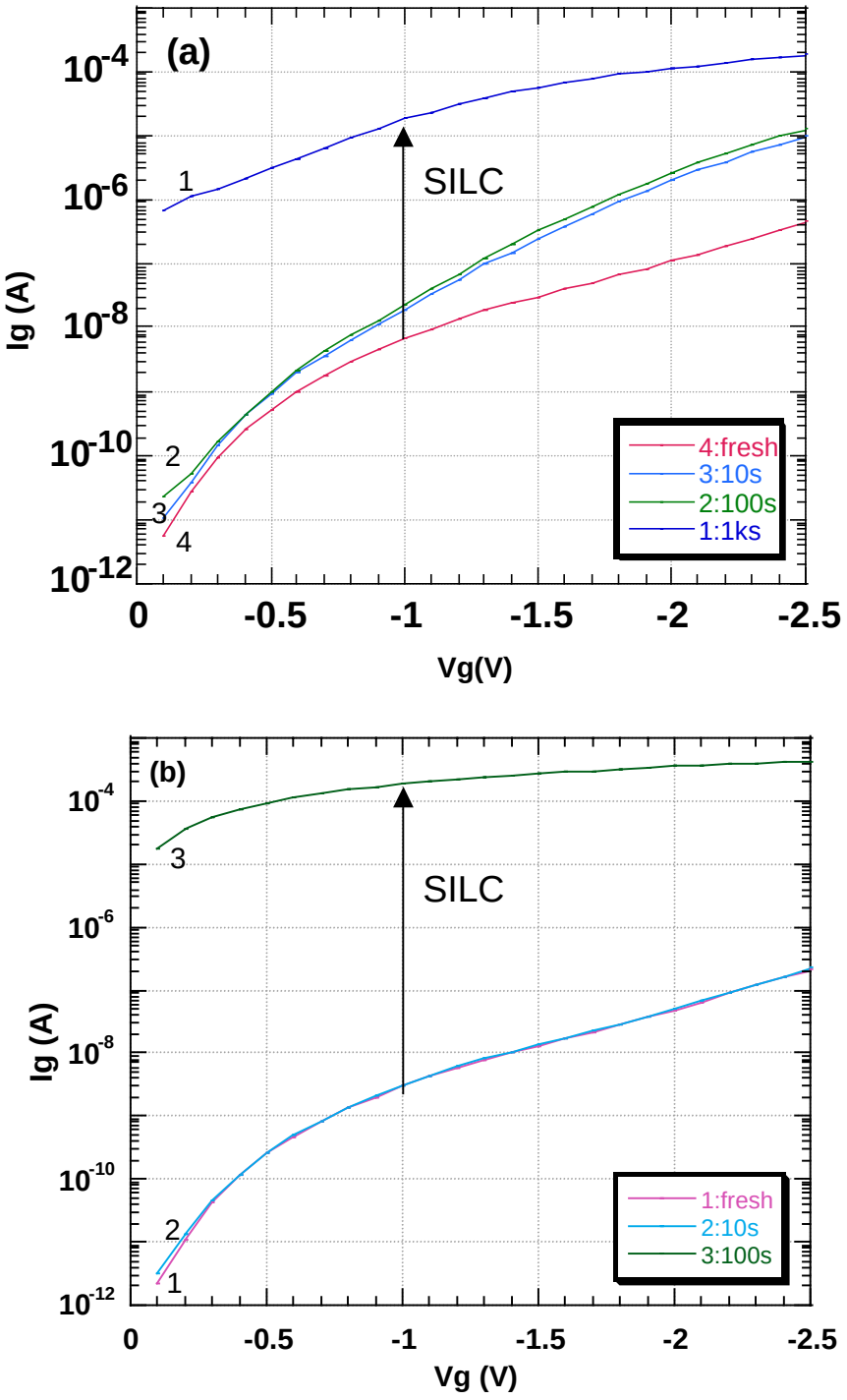


Figure 4 Evolution of stress-induced leakage current (SILC) of thermal gate oxide (W/L = 10μm/10μm) under (a) gate injection and (b) substrate injection.

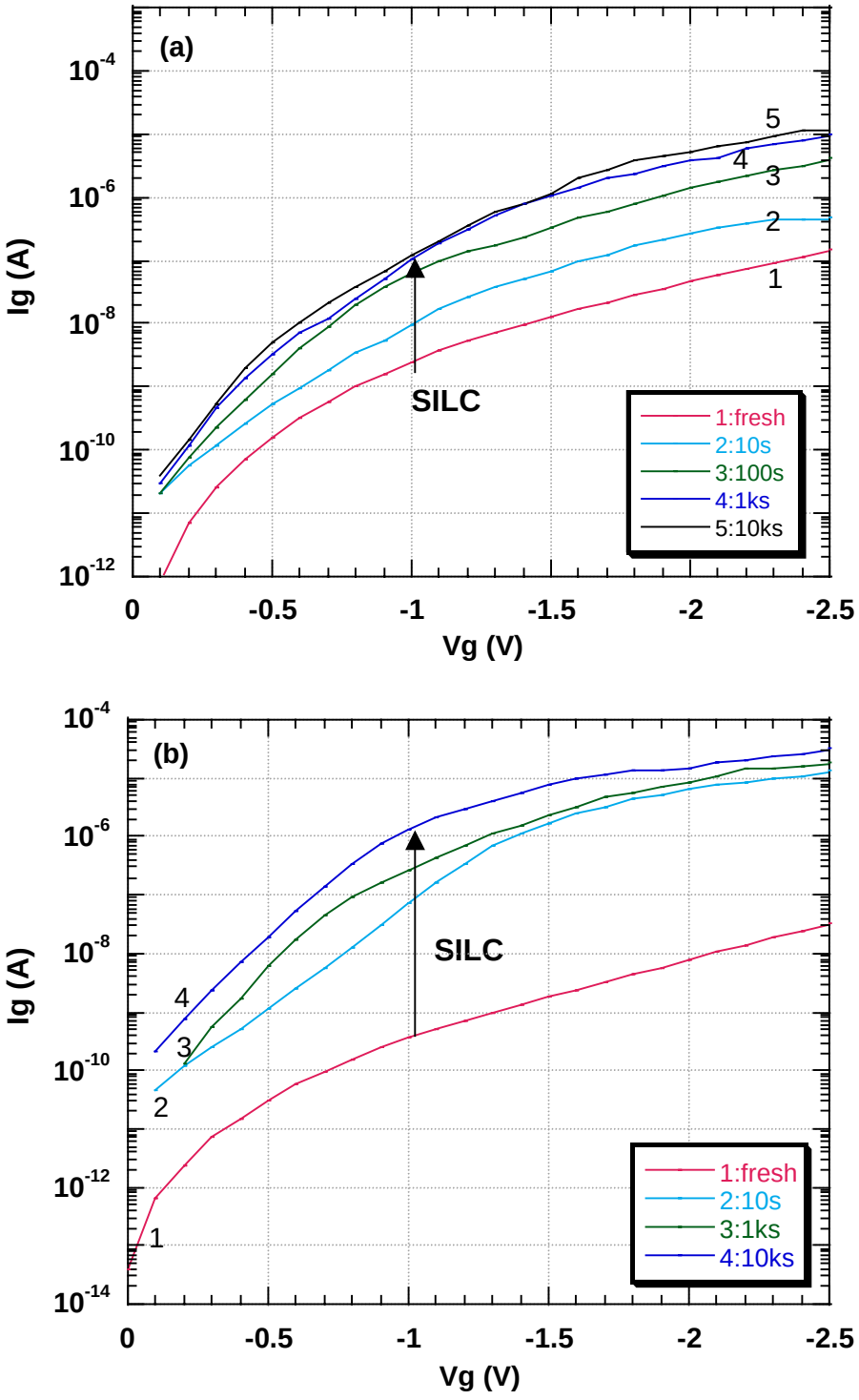


Figure 5 Evolution of stress-induced leakage current (SILC) of (a) O/N and (b) Oxynitride gate dielectric (W/L = 10μm/10μm) under substrate injection.

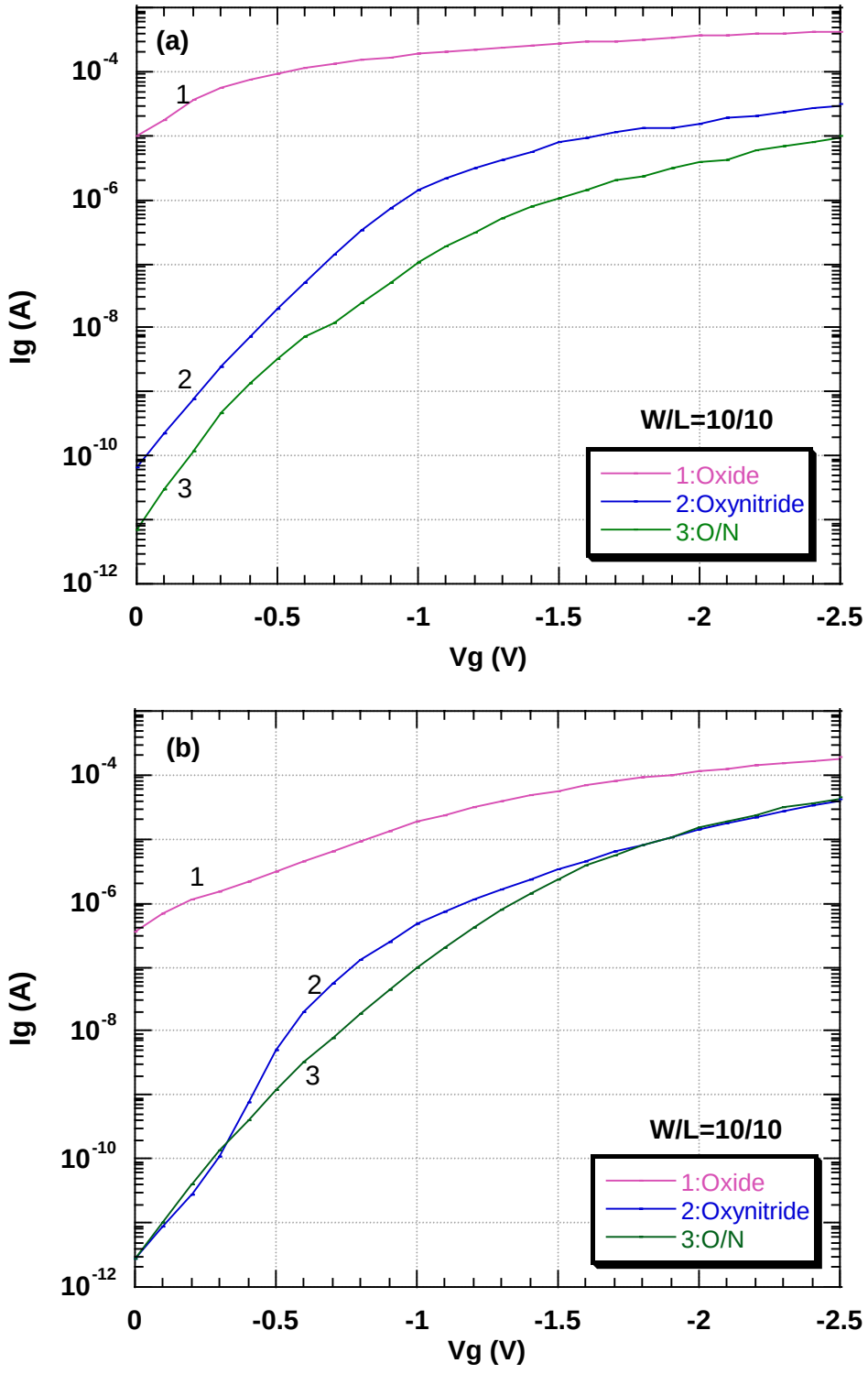


Figure 6 Comparison of post-breakdown leakage current under (a) substrate injection and (b) gate injection.

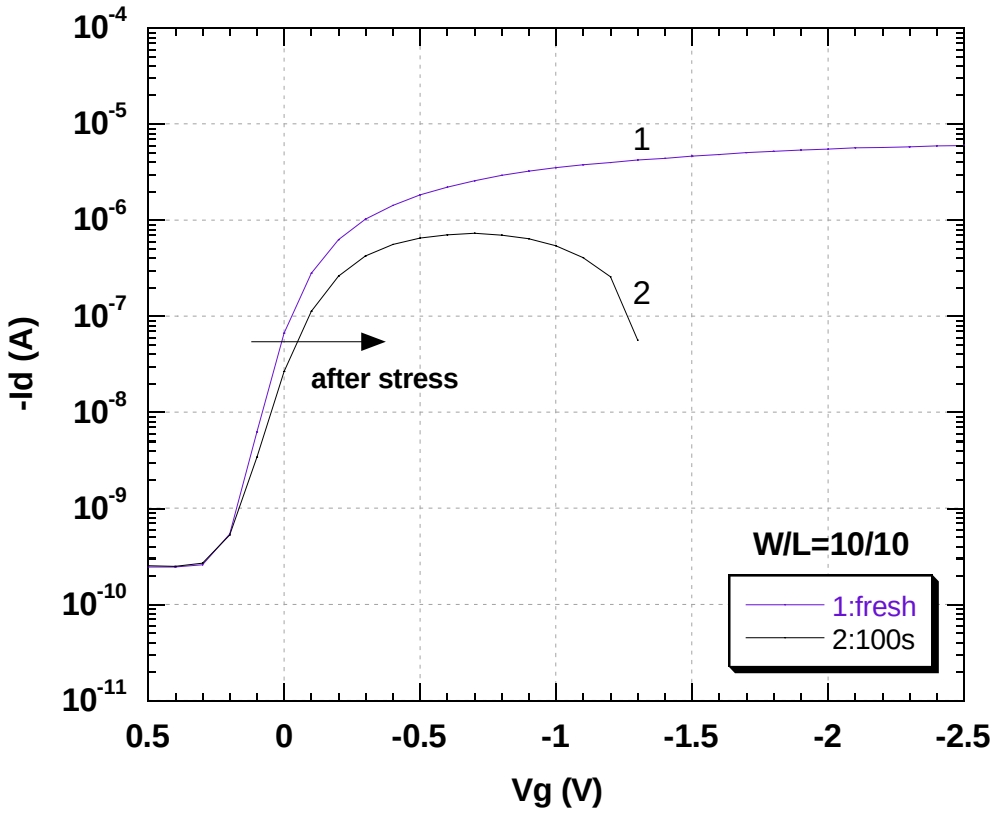


Figure 7 I_d-V_g characteristics of thermal oxide devices under gate injection. It is observed that after 100 sec of stress, the saturated I_d and subthreshold swing are severely degraded (from 77 mV/dec to 89 mV/dec).

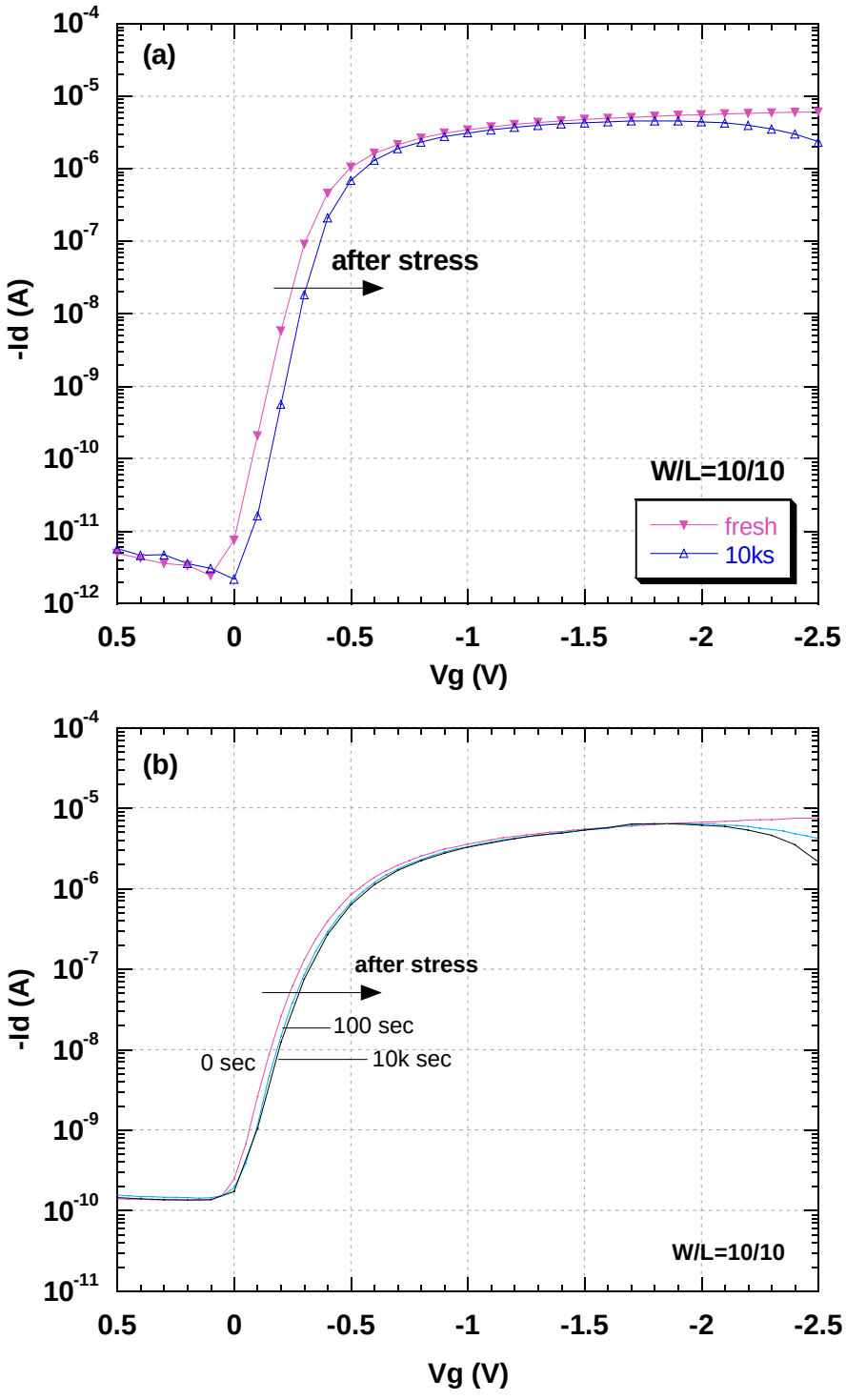
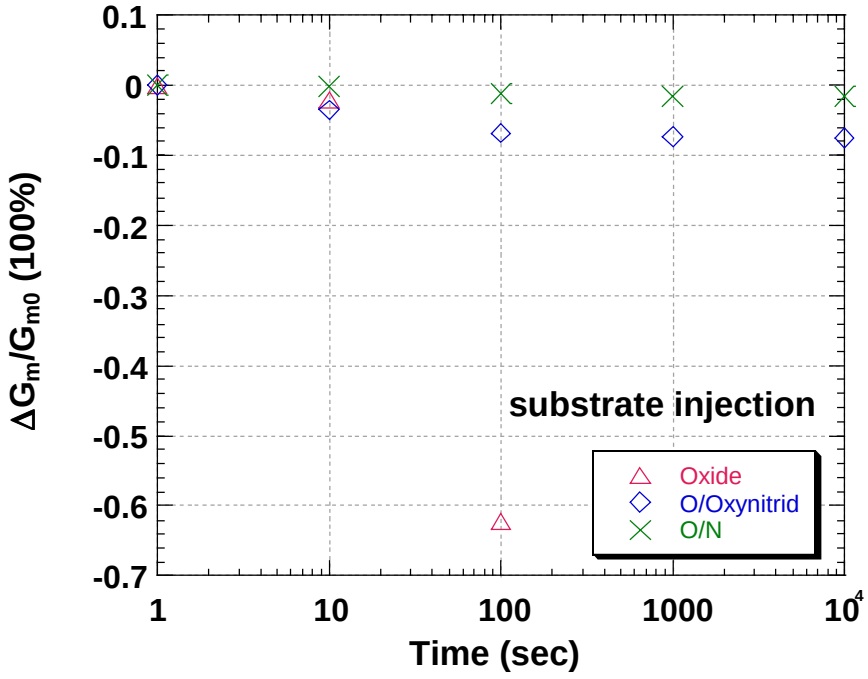
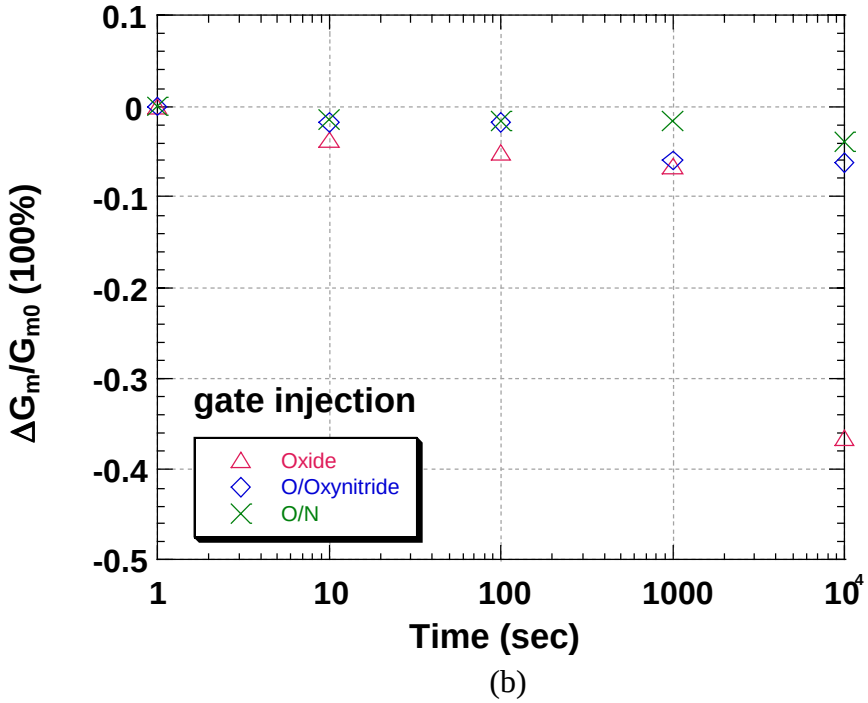


Figure 8 I_d-V_g characteristics of (a) O/N and (b) Oxynitride before and after CCS under gate injection. Subthreshold swing is slightly degraded from 74 mV/dec to 78 mV/dec.



(a)



(b)

Figure 9 Degradation of transconductance (G_m) for thermal oxide, oxide/nitride and oxynitride dielectrics (W/L = 10μm/10μm) for both bias polarities.

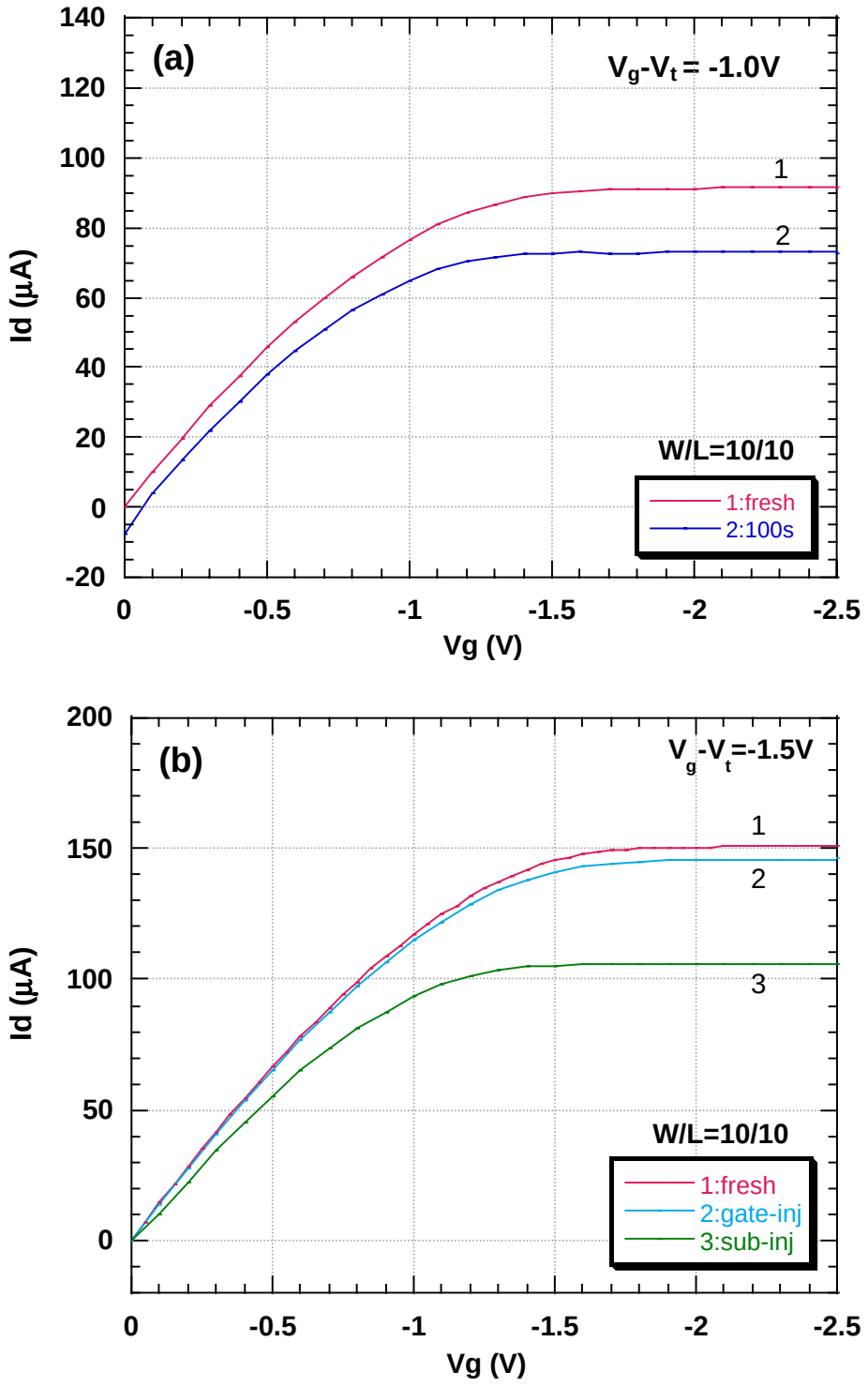


Figure 10 I_d-V_d characteristics of (a) thermal oxide for substrate injection (b) oxide/oxynitride dielectric for 10k sec of stress under bias polarities.

CHAPTER 3

Effects of Interface Properties on the Breakdown and Reliability of Oxide/Nitride and Oxynitride Gate Dielectrics under Constant Voltage Stress

3.1 Introduction

Trap generation and the localized physical damage near the Si/SiO_2 interface have been proposed to degrade gate oxide and then trigger SBD under electrical stresses [1-3]. Thus the interface properties should play a key role in the evaluation of the dielectric breakdown and reliability. In this chapter, the effects of Si/SiO_2 interface properties on breakdown and reliability of ultrathin RPECVD stacked O/N and oxynitride dielectrics are studied by a CVS test, which has been widely used in ultrathin dielectric regime. First, the fundamentals of the oxide breakdown statistics and the Weibull failure function are introduced. Second, we will demonstrate an improvement in the SILC effect and device performance due to the suppression of the trap generation at the SiO_2/Si interface by using RPECVD interface nitridation. Finally, the effects of interfacial RPAO thickness on the breakdown and electrical characteristics of stacked oxide/oxynitride devices are also investigated. PMOS and NMOS devices with 0.6 and 0.8 nm RPAO are tested by TDDB at various levels of stress voltages, and the reliability is evaluated. These devices exhibit C-V distortion characteristics during stress, which can be explained by the oxide thinning effect and the percolation model.

3.2 Experimental Procedures

PMOS devices with RPECVD oxide/nitride and $(SiO_2)_{0.5}(Si_3N_4)_{0.5}$ gate dielectrics were fabricated following the same process as was described in Chapter 2. A 0.6 nm (0.8 nm) remote-plasma-assisted oxidation (RPAO) layer was prepared using O_2 plasma at a RF (13.56 MHz) power of 30 W for 18 sec (1 min 12 sec). Interface nitridation (0.2 torr, 90 sec) was then performed by remote plasma process to incorporate N atoms at the monolayer level at the interface between the O/N dielectrics and the Si substrates. For n^+-poly/NMOSFET devices, 60 keV As ion implant was used with a dose of $5x10^{15}$ cm^{-2}. Dopant activation was done by rapid thermal annealing (RTA) in Ar at 1000 °C for 60 seconds. The poly-Si gate was aluminium-metalized to obtain good electrical contacts. All the wafers received a post-metal-anneal (PMA) in forming gas (10% H_2 in N_2) at 400 °C for 30 minutes.

An HP4155B semiconductor parameter analyzer was employed to perform constant voltage stress (CVS) to the gate, with source/drain and substrate grounded. The devices were stressed until the occurrence of HBD. The time to HBD is the time from the start of the test to the dramatic increase in the I_g-time plot; it also shows a linear I_g-V_g characteristic, indicating a destructive dielectric breakdown. The stresses have been periodically stopped in order to measure the electrical parameters and characteristics. C-V measurements were conducted by using an HP4284A inductance-capacitance-resistance (LCR) meter. For each breakdown distribution, 15 samples were tested by TDDB in the accumulation mode. The 63%-value in the Weibull

distribution plot was taken as a characteristic breakdown time. All measurements have been performed at room temperature in this study.

3.3 Breakdown and Reliability of CMOSFETs

3.3.1 TDDB and Weibull Failure Distribution

The time-dependent-dielectric breakdown (TDDB) test is a widely used technique to evaluate the reliability and lifetime of VLSI devices. It has been shown that TDDB of gate oxides thinner than 3 nm related with intrinsic reliability is one of the crucial concerns for future evolution of gate dielectrics [4]. In TDDB experiments, a constant voltage or current is applied to the devices until a sudden change in gate current or voltage at the critical breakdown point, respectively. The behavior of oxide breakdown is statistical in nature, thus it is usually described by using a Weibull function [5, 6] given by

$$F(t_{BD}) = 1 - \exp\left[-\left(\frac{t_{BD}}{\alpha}\right)^{\beta}\right] \tag{3.1}$$

where F is the cumulative failure function, t_{BD} is the time-to-breakdown, α is the characteristic time and β is the Weibull distribution slope (i.e., shape factor) which can be obtained by fitting t_{BD}-data. Equation (3.1) can be written as follows:

$$\ln[-\ln(1 - F(t_{BD}))] = \beta \ln t_{BD} - \beta \ln \alpha \tag{3.2}$$

In this way, β can be obtained from the slope of the line plotted on log-log scales; α can be found from the 37% reliability life (F = 63.2%) at which the Weibull function ln[-ln(1-F)] is equal to zero.

It has been proposed that the Weibull slope is related to the effective defect radius and the number of defects required for the local formation of the percolation path [7]. It was shown that Weibull shape factors are decreased with oxide thickness [5]. This shallower Weibull distribution in the thinner oxide is due to a larger spread of average critical defect density to form a percolation channel between the substrate and gate [5, 8]. In other words, this shape factor β is sensitive to the failure rate and area scaling [9], depending on the trap generation rate for a fixed dielectric thickness [10]. In addition, any breakdown of an individual transistor can cause the circuit failure of entire chip [6]. Therefore, the ten-year lifetime should be projected based on the consideration of the full gate area on the chip, and to a specified low cumulative failure rate by using the Weibull distribution plot, to be discussed in Chapter 5.

3.3.2 Effect of Interface Nitridation

The time evolution of the gate current through thermal oxide (EOT = 2.02 nm) and stacked O/N dielectrics (EOT = 1.83 nm) for a constant –4 V bias (gate injection) is presented in Figure 1. The occurrence of the complex fluctuations in the monitor current corresponds with breakdown characteristics. Stacked O/N dielectric without interface nitridation shows early SBD and hard breakdown (HBD) by a sudden current

jump after 400 sec of stress. In contrast, stacked O/N dielectric with nitridation treatment shows superior breakdown behavior compared to the thermal oxide and stacked O/N dielectric without interface nitridation. In order to monitor dielectric degradation and evaluate film quality, the stress-induced leakage current (SILC) expressed as $(I_g-I_0)/I_g$ [11] is presented in Figure 2. In the initial stage of stress (before 150 sec), there is no significant difference on the SILC behavior; however, in the later stage of stress, O/N gate stack with interface nitridation exhibits a saturated SILC, showing an improvement in dielectric degradation. Figure 3 shows the effect of interface nitridation on the post-breakdown leakage current. Stacked O/N device without interface nitridation shows a linear I_g-V_g characteristic, indicating the occurrence of HBD which is consistent with the evolution of the leakage current as shown in Figure 1. However, the post-breakdown leakage current can be reduced by ~4 orders of magnitude at V_g = -1V by using the RPECVD interface nitridation. It is believed that the incorporation of nitrogen at the monolayer level at the SiO_2/Si interface improves dielectric breakdown, SILC and the post-breakdown leakage current by reducing dangling bonds and interfacial strain relaxation [12].

Figure 4 shows the threshold voltage (V_t) shifts as a function of stress time during CVS. It is found that V_t becomes more negative, indicating the generation of positive charges in the gate dielectrics. These positive charges are believed to be resulted from hole trapping in the dielectric layer and/or at the Si/SiO_2 interface [13, 14]. It can be seen that nitrogen incorporation at the Si/SiO_2 interface by interface

nitridation improves the interface endurance during electrical stress [15, 16], thus effectively suppresses the hole trapping, showing less V_t shift. Figure 5 shows the saturated drain current $I_{d,sat}$ as a function of stress time during the stress. The I_d-V_d characteristics of PMOSFETs before and after 1000 sec of CVS are illustrated in Figure 6. O/N gate dielectric without interface nitridation exhibits drastic $I_{d,sat}$ degradation (~20%), which is much larger than the degradation (~7%) for O/N with nitridation. It is also noted that the transistor without interface nitridation shows increased off-state drain leakage after CVS. This positive drain leakage is attributed to the generation of these stress-induced defects and breakdown spots in the damaged gate/drain overlap region [17], which enhances charge trapping when holes transport from the drain to gate (V_g = -1.2 V and V_d = 0). In contrast, stacked O/N devices with interface nitridation show much less degradation on I_{dsat} (Figures 5 and 6) and the suppression of this positive off-state leakage current (Figure 6) due to the relaxation of interfacial strain and the suppression of interfacial traps [18]. It is concluded that the interface properties and the degradation of device performance can be improved by interface nitridation using RPECVD technique.

3.3.3 Effect of Remote-Plasma-Assisted Oxidation Layer Thickness

Figure 7 illustrates the influence of RPAO thickness on the time evolution of breakdown behavior for PMOSFETs with stacked oxynitride dielectrics (EOT = 1.95 nm) under CVS. Stacked oxynitride dielectric with 0.6 nm RPAO shows high endurance under CVS. In contrast, the 0.8 nm RPAO device shows early stage

multilevel gate fluctuations, indicating the occurrence of SBD events. Figure 8 shows the time evolution of SILC of the NMOS devices under gate injection. SILC is defined as $(I_g-I_0)/I_0$ with I_g being the leakage current measured at a given time and I_0 as the initial current. Similar trend is also observed on the NMOS devices.

We further study the changes in threshold voltages (V_t) in order to investigate the relation between RPAO thickness and the generation of the stress-induced traps. It is worth noticing that the generation of negative charges and/or filling of neutral electron traps [19] give rise to a positive ΔV_{FB} shift for NMOS capacitors stressed under gate injection. Compared to the 0.8 nm RPAO device, the 0.6 nm RPAO device shows less V_t shifts (Figure 9), indicating less oxide traps and damage created during CVS. The stress-induced trap density (ΔD_{ot}) is extracted from the changes in V_t. It is shown the ΔD_{ot} of stacked oxide/oxynitride dielectrics after 1k sec of CVS is around $8\sim9x10^{19}/cm^3$. The measurement of ΔV_{FB} shift has also been used to evaluate the total effective-trapped charge density in 1.93 nm HfO_2 [20]. In the case of Al/HfO_2/p-Si, the stress-induced trap density of $\sim2x10^{12}/cm^2$ was created after injected fluence of ~600 C/cm^2.

The effects of RPAO thickness on TDDB for P- and NMOS devices were also studied in accumulation mode. Figure 10 shows the Weibull failure distribution for PMOS devices under CVS ranged from 3.4 V to 3.65 V; the Weibull plot for NMOS

devices under CVS ranged from -3.5 V to -3.8 V is shown in Figure 11. It is found that there is no significant difference in the Weibull slope, implying the same effective defect radius and physical breakdown mechanism (discussed in next section). The TDDB reliability for P- and NMOS devices are demonstrated in Figure 12 and 13, respectively. The 63%-value of T_{BD} is fitted by hole-induced breakdown (1/E) model, which was first proposed by Chen et al. [21]. A 0.6 nm RPAO interfacial layer exhibits higher time-to-breakdown for both PMOS and NMOS capacitors.

3.4 C-V Analysis and Oxide Thinning Model

The concept of oxide thinning effect was first proposed to evaluate thin oxides and predict the lifetime of oxide devices in an integrated circuit [22]. The reduction of this effective oxide thickness is attributed to the formation of local physically damaged region (LPDR) [1, 23], which would trigger early SBD [24]. The oxide breakdown time has been studied with the consideration of oxide thinning effect [25]; it was found that T_{BD} is decreased with decreasing effective oxide thinning ratio [26]. Below we use this effective oxide thinning model associated with the local percolation breakdown model [11, 27] to explain the effect of RPAO thickness on TDDB reliability.

Figures 14 and 15 show the C-V characteristics before and after CVS for the devices with 0.6 nm and 0.8 nm RPAO, respectively. As can be seen, C-V curves show an increase in capacitance with stress time, and then lose the saturation in

accumulation region due to the oxide thinning effect. A C-V shift corresponding to positive charge generation is observed under negative-gate voltage stressing, which agrees with the results in a 5.1-nm gate oxide [28]. The phenomena of C-V curve shift and capacitance increases have also been shown for a 3.5 nm gate oxide under CVS [29]. It is noted that the 0.8 nm device shows strong oxide thinning effect after 100 sec of stress (Figure 15), indicating the occurrence of early SBD. However, no significant oxide thinning effect is observed in the 0.6 nm RPAO device until 750 sec of stress, as is illustrated in Figure 14. A schematic illustrating the oxide thinning effect and the percolation breakdown model is shown in Figure 16. It is found that a thicker strained layer with a greater density of weak bonds and breakdown spots is formed in the 0.8 nm RPAO device during the electrical stressing. Eriguchi et al. [30] have studied the effect of the thickness of the strained layer on the TDDB characteristics for the oxides formed by two processes. It was also suggested that the thicker strained layer enhances the defect generation rate and degrades the TDDB lifetime. It is believed that, during the stress, a larger number of broken Si-O and H-O bonds is created, thus the injected holes can attack the O vacancy [19] and are trapped in the strained RPAO layer after stressing. Therefore, a smaller amount of charges are trapped in the thinner strained RPAO thickness, leading the improvement in T_{BD}. In other words, EOT of stacked oxide/oxynitride dielectric with thicker RPAO is reduced at the local percolation spots during CVS, leading to harder breakdown and degraded reliability.

3.5 Conclusion

The impact of interface nitridation and RPAO thickness on sub-2 nm stacked O/N and oxynitride dielectric breakdown characteristics under CVS. It is demonstrated that interface nitridation effectively reduces the post-breakdown leakage current by ~4 orders of magnitude at V_g = -1V, and also suppresses the positive drain leakage current after 1k sec of stress. It is concluded that interface nitridation provides improved immunity of hole trapping at the SiO_2/Si and gate/drain interfaces against electrical stressing, leading to the improvements in dielectric breakdown and device degradation. Additionally, the devices with oxynitride dielectric interposed with the thinner RPAO exhibit reduced SILC and threshold voltage shift, indicating less hole trapping generated in thinner strained RPAO layer after CVS. The higher TDDB reliability in both PMOS and NMOS devices with 0.6 nm RPAO is also observed, which can be explained using the oxide thinning effect and the percolation breakdown model.

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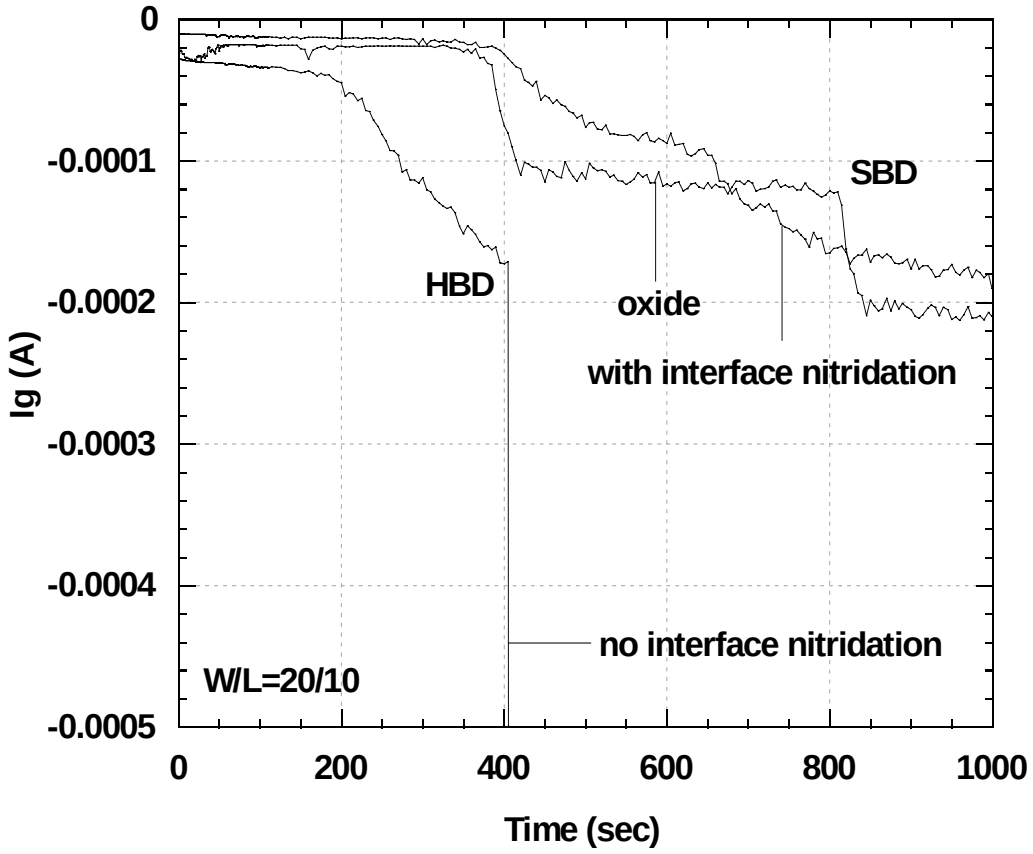


Figure 1 Time evolution of gate currents of different gate dielectrics during constant voltage stress (Vg = -4 V, $V_s = V_d = V_{sub} = 0$).

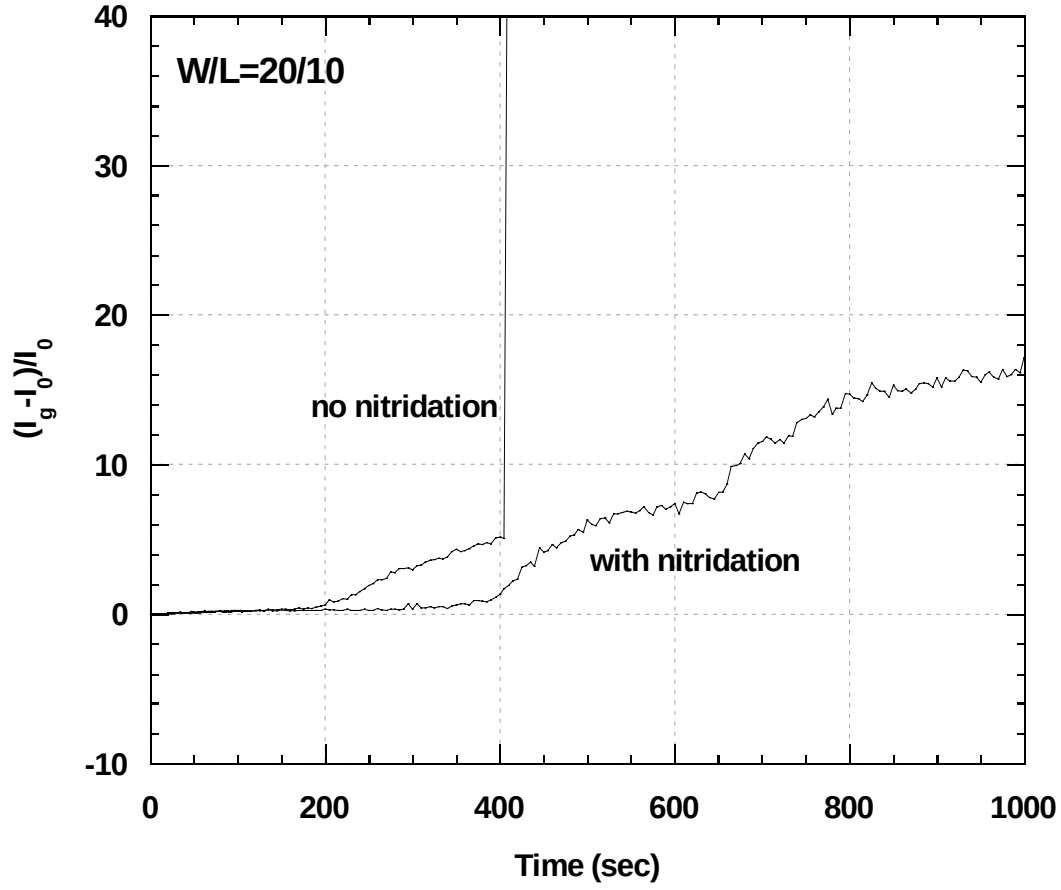


Figure 2 Effect of interface nitridation on stress-induced leakage current (SILC) characteristics during constant voltage stress (Vg = -4 V, $V_s = V_d = V_{sub} = 0$).

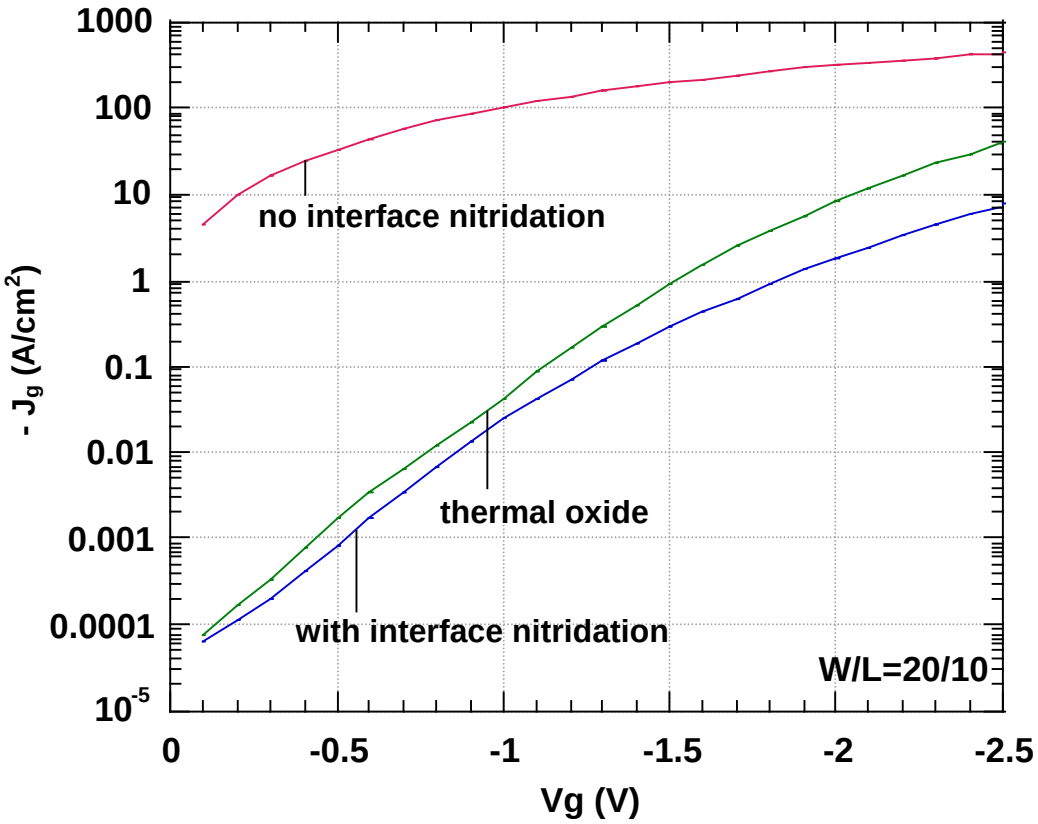


Figure 3 Effect of interface nitridation on the post-breakdown leakage current density for O/N without interface nitridation after 400 sec of stress, and for thermal oxide and O/N with interface nitridation after 1000 sec of stress.

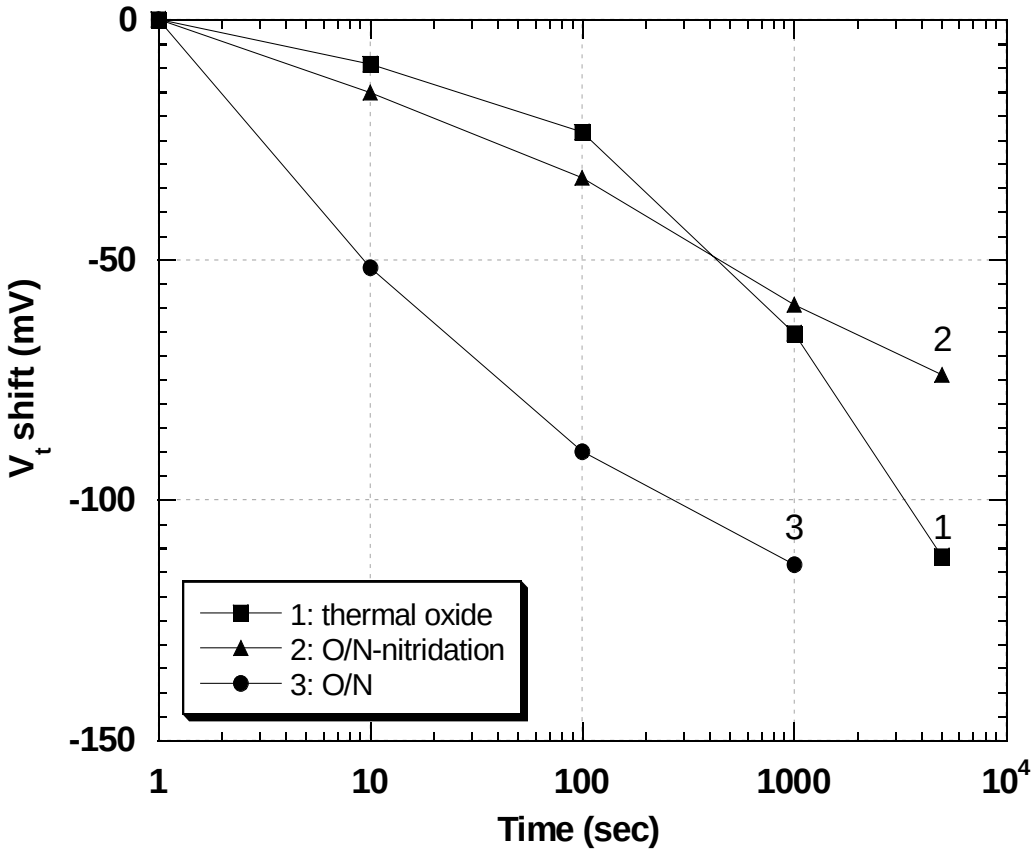


Figure 4 Threshold voltage shift as a function of stress time during CVS. (W/L = 20μm/10μm, V_g = -4 V)

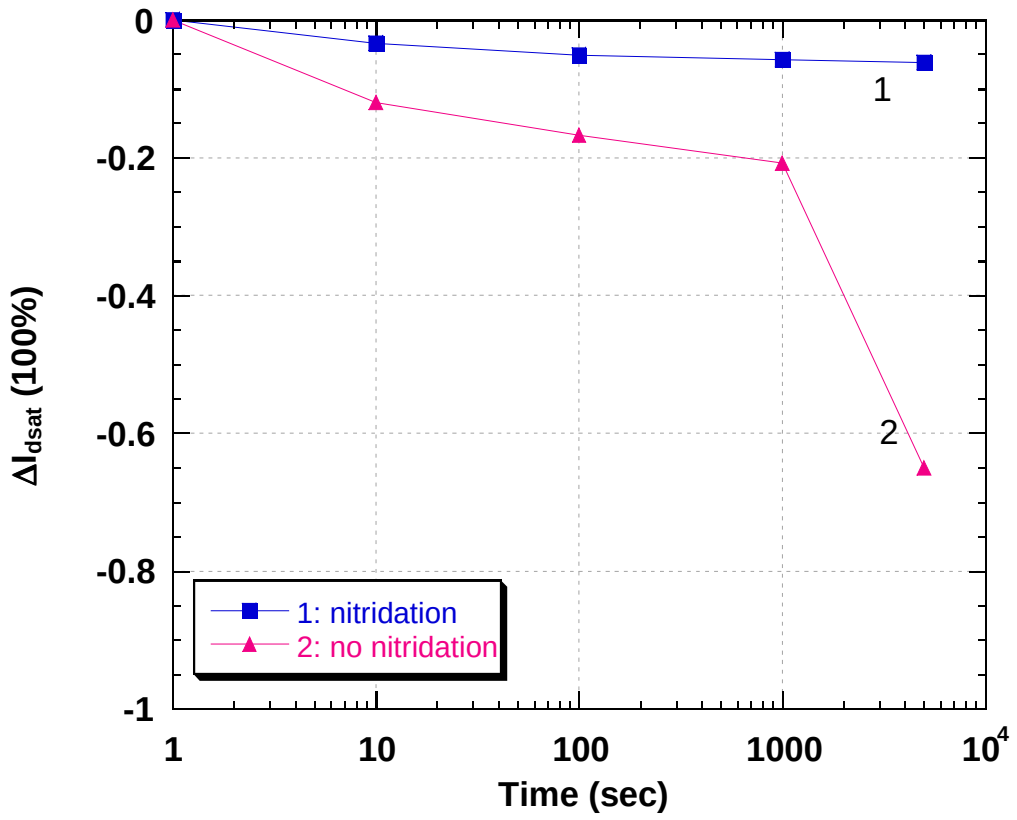


Figure 5 Effect of interface nitridation on I_{dsat} degradation as a function of stress time. I_{dsat} was measured at V_d = -2.5 V and V_g-V_t ~ -1.2 V (W/L = 20μm/20μm, under V_g = -4V).

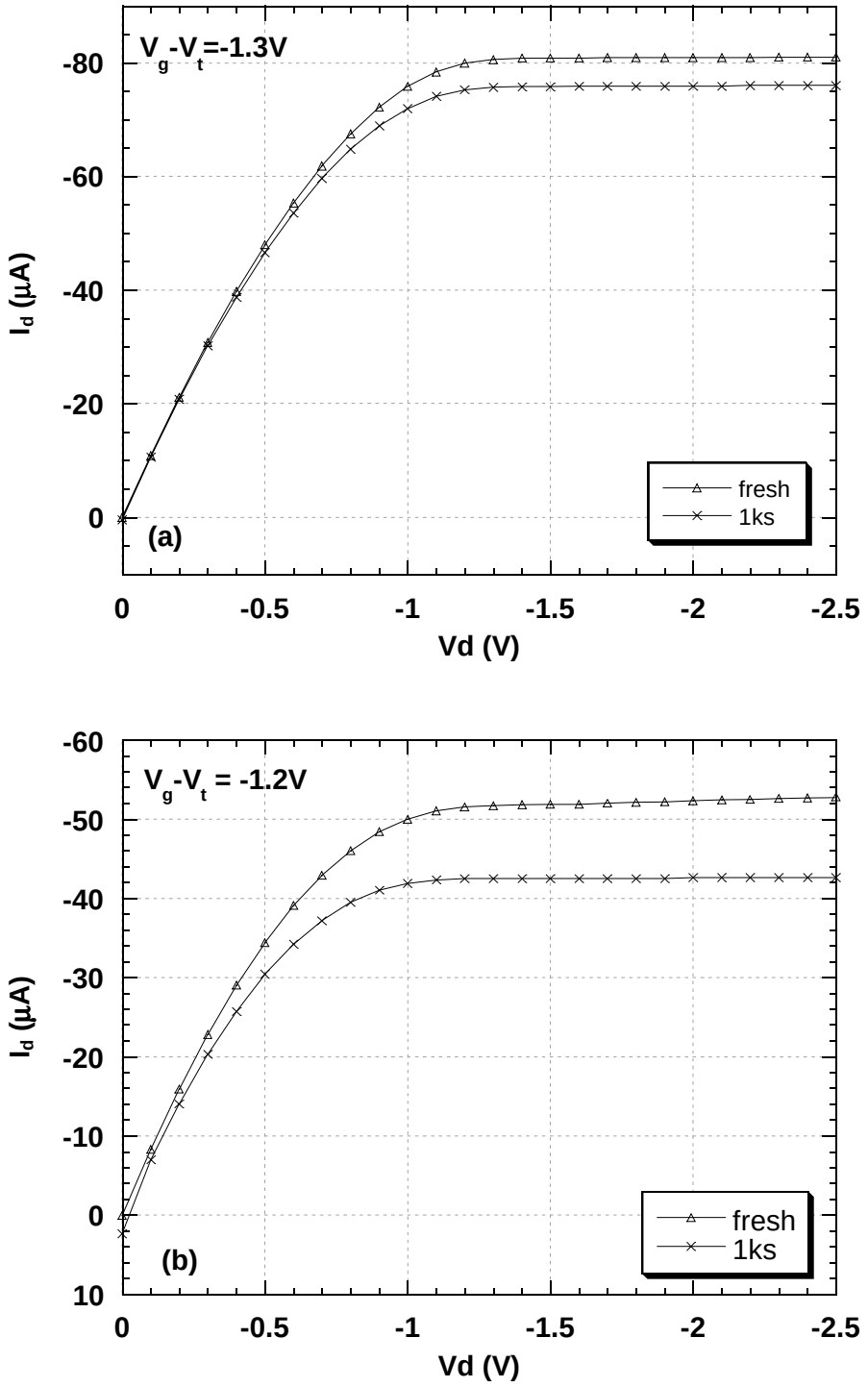


Figure 6 I_d-V_d characteristics for O/N (a) with interface nitridation and (b) without interface nitridation. (W/L = 20μm/20μm, under V_g = -4V)

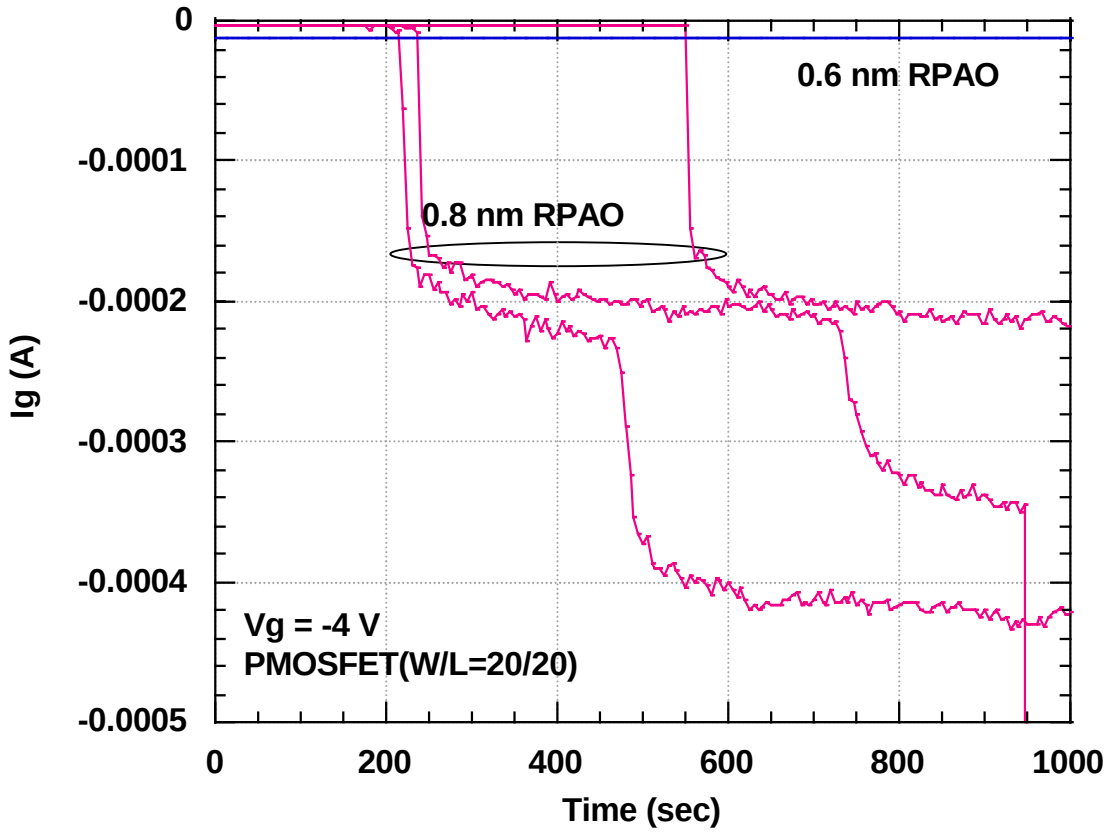


Figure 7 Effect of RPAO thickness on the time evolution of gate currents. Constant voltage stress was performed on 3 sites for each sample (Vg = -4 V, $V_s = V_d = V_{sub} = 0$).

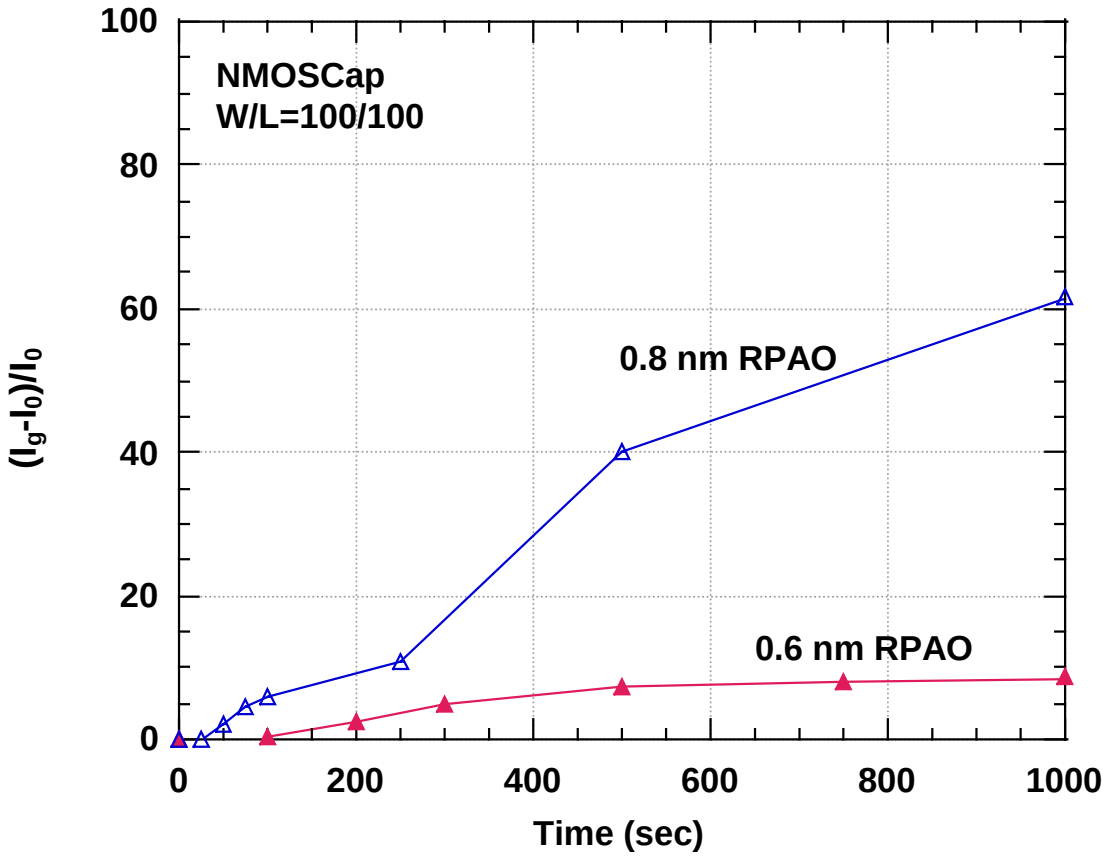


Figure 8 Effect of RPAO thickness on SILC effect during a CVS of -3.52 V. The 0.8nm RPAO device shows a larger SILC by a factor of 6 after 1000 sec of stress.

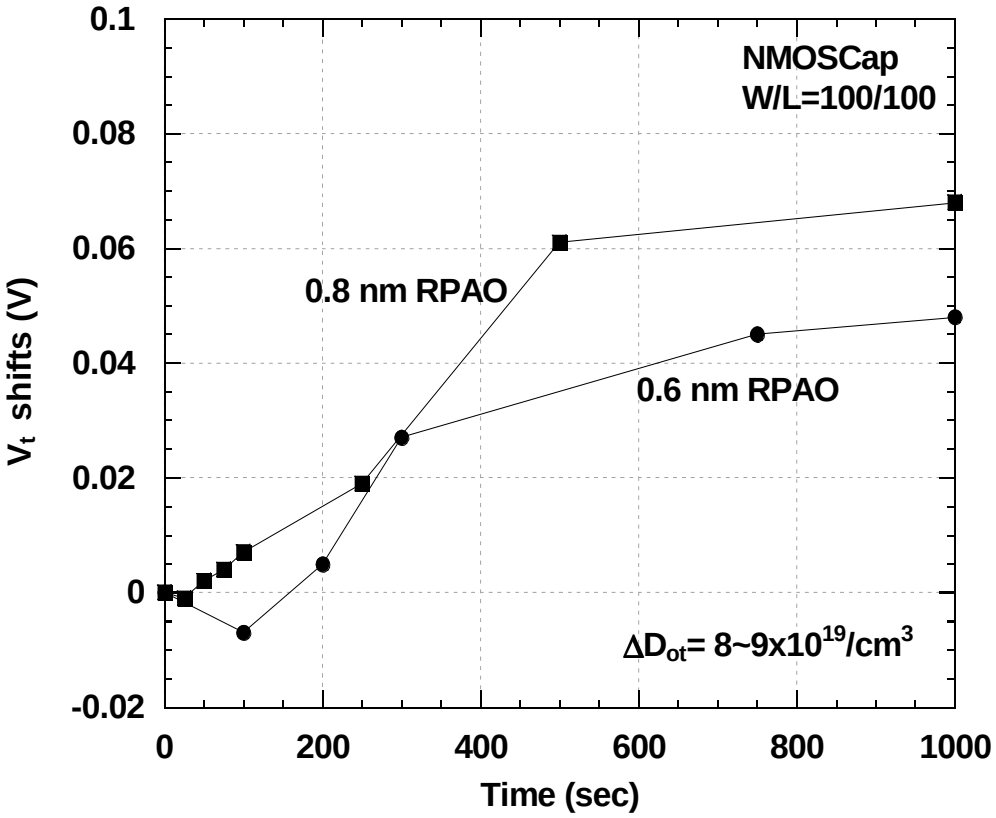


Figure 9 Effect of RPAO thickness on threshold voltage shift of NMOS devices during a CVS of -3.52 V. The generation of negative charges gives rise to a positive ΔV_{FB} after stress.

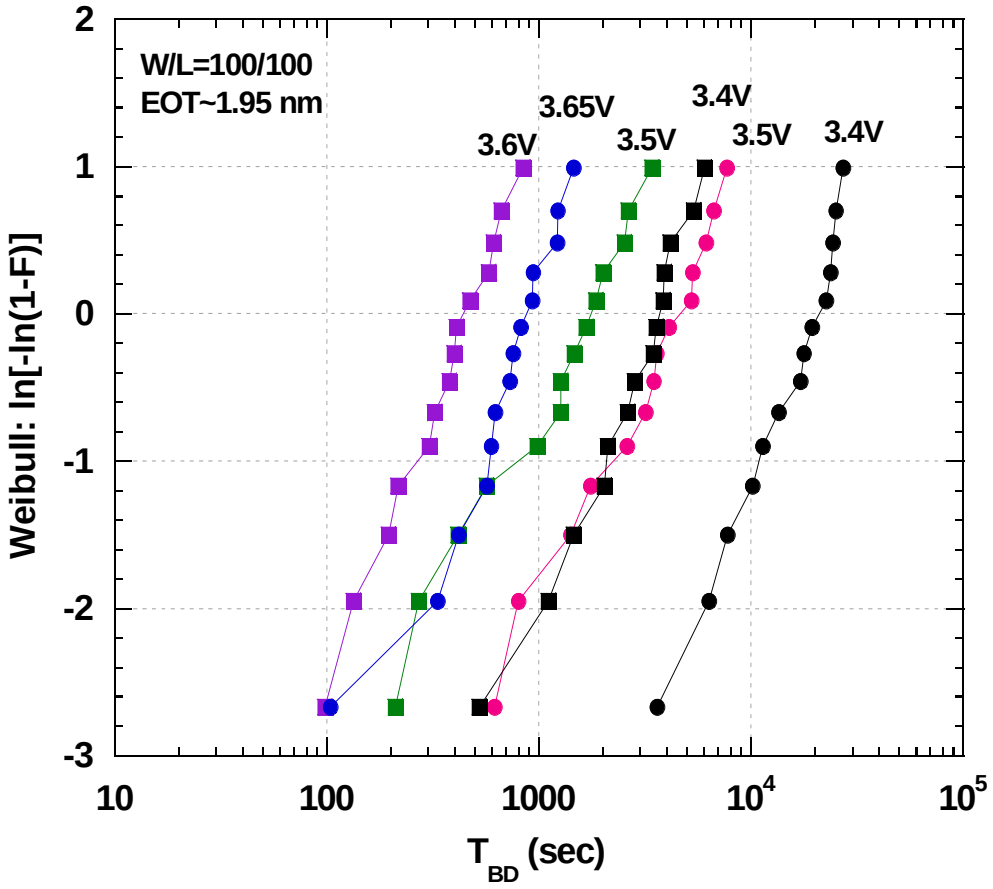


Figure 10 Time-to-breakdown (T_{BD}) distributions for PMOS devices (circles: 0.6 nm RPAO/oxynitride; squares: 0.8 nm RPAO/oxynitride). The stress voltage was ranged from 3.4 to 3.65 V under accumulation mode.

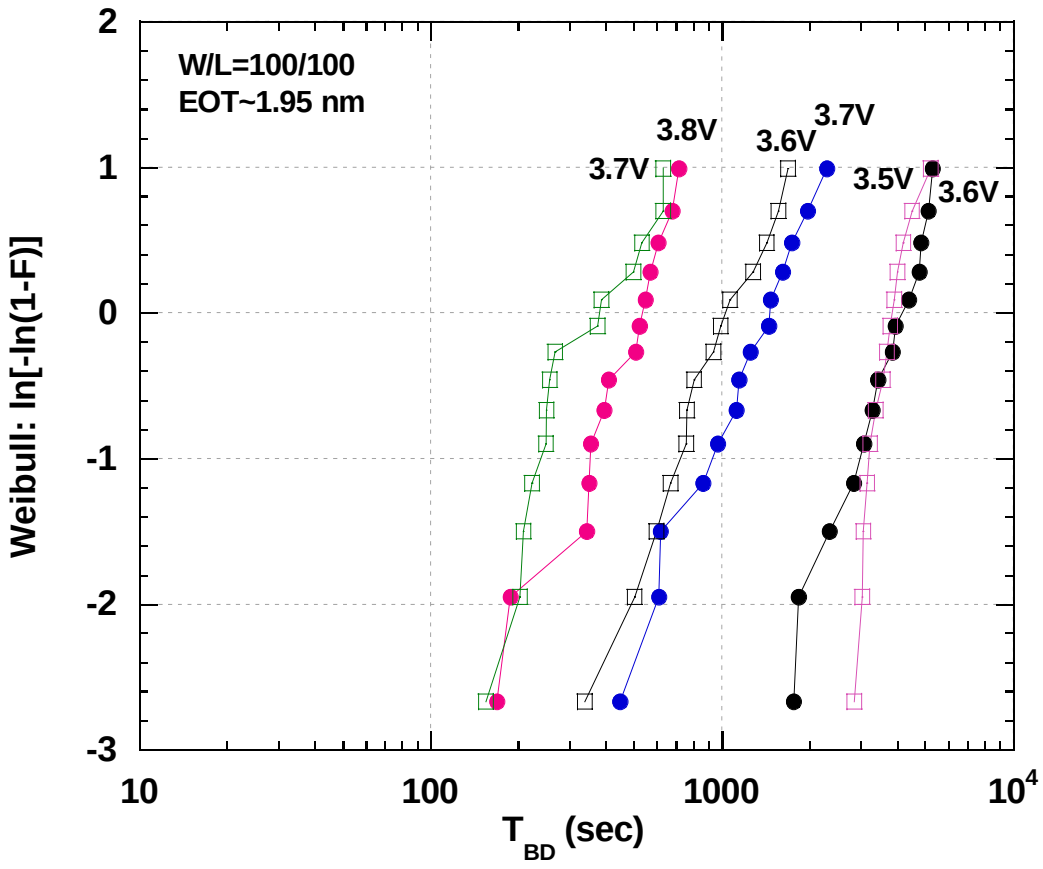


Figure 11 Time-to-breakdown (T_{BD}) distributions for NMOS devices (circles: 0.6 nm RPAO/oxynitride; squares: 0.8 nm RPAO/oxynitride). The stress voltage was ranged from -3.5 to -3.8 V under accumulation mode.

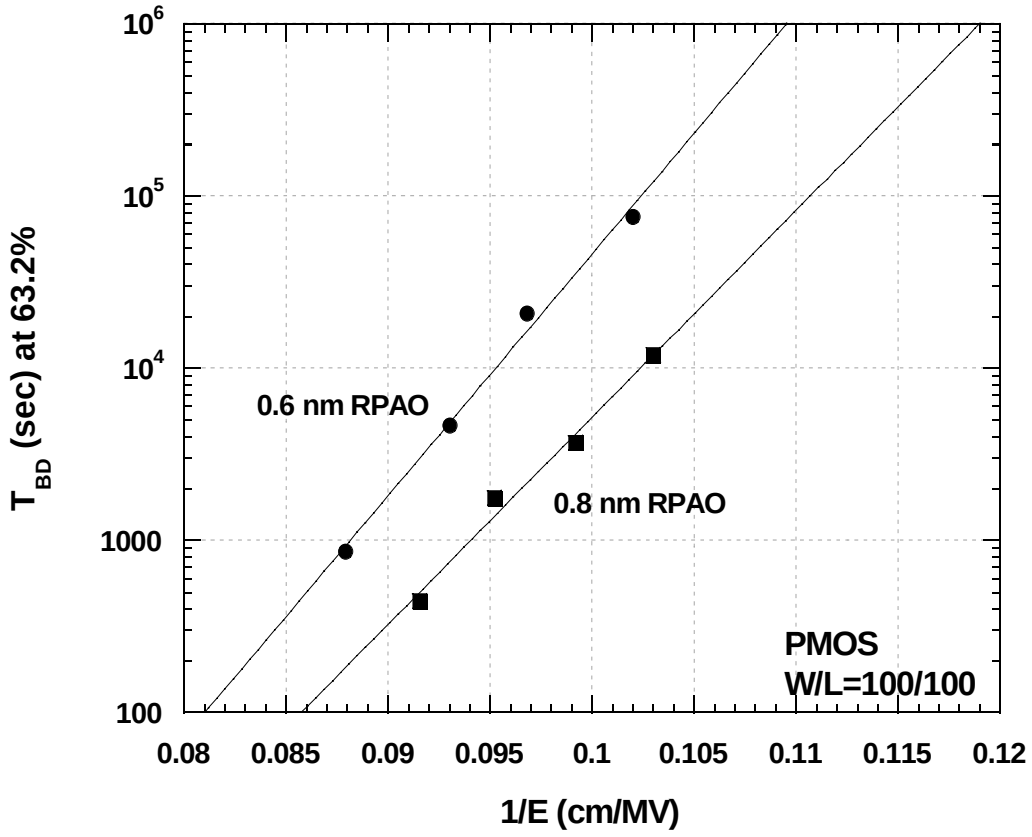


Figure 12 Comparison of TDDB characteristics on PMOS devices with 0.6 and 0.8 nm RPAO layer. The total number of tested samples is 120.

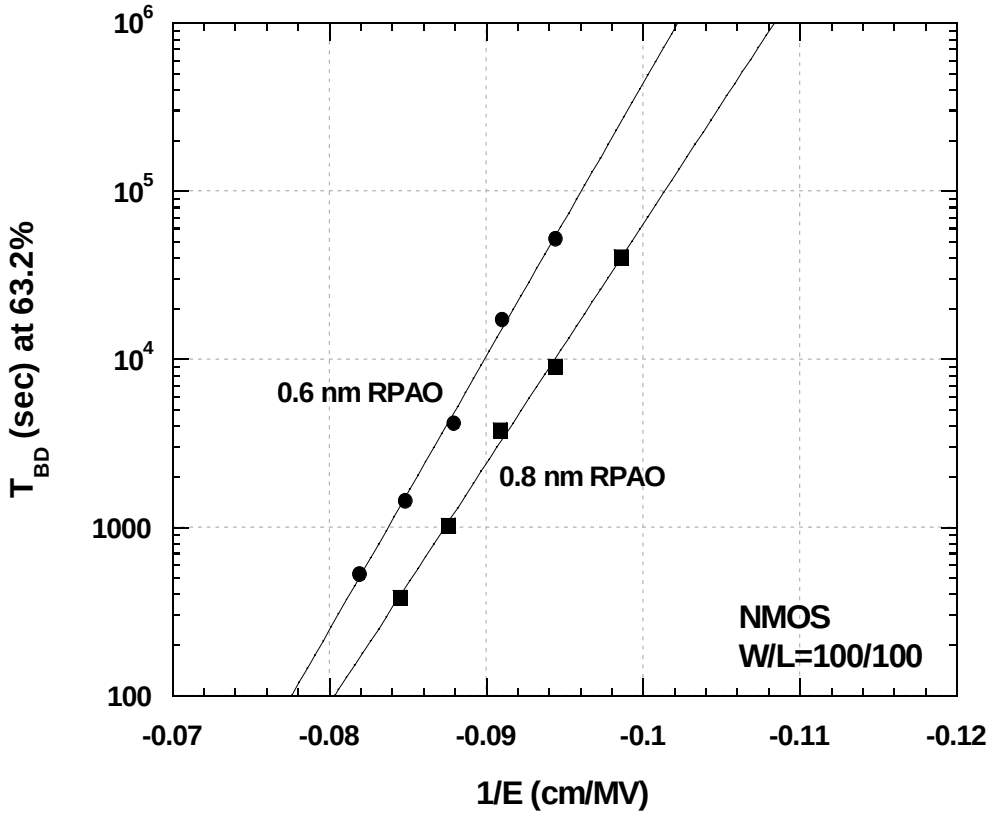


Figure 13 Comparison of TDDB characteristics on NMOS devices with 0.6 and 0.8 nm RPAO layer. The total number of tested samples is 150.

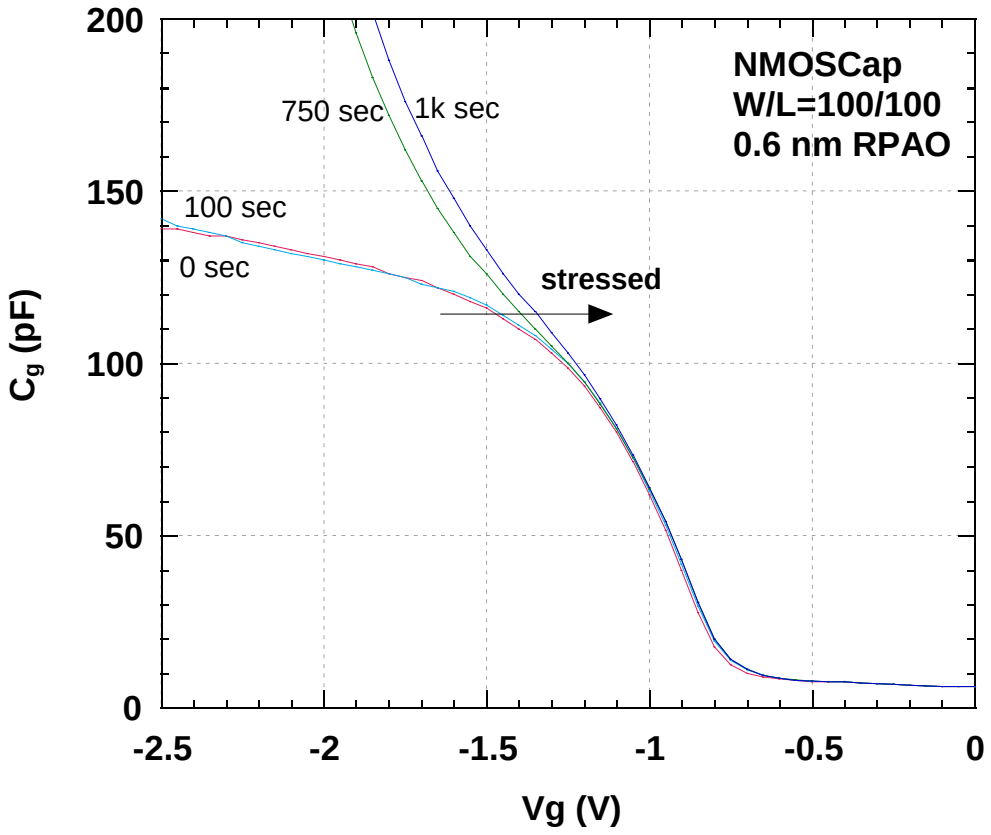


Figure 14 C-V characteristics for a NMOS capacitor with stacked 0.6 nm RPAO/oxynitride gate dielectrics before and after CVS at Vg = -3.52 V. The flat-band voltage of the fresh capacitor is –0.87 V.

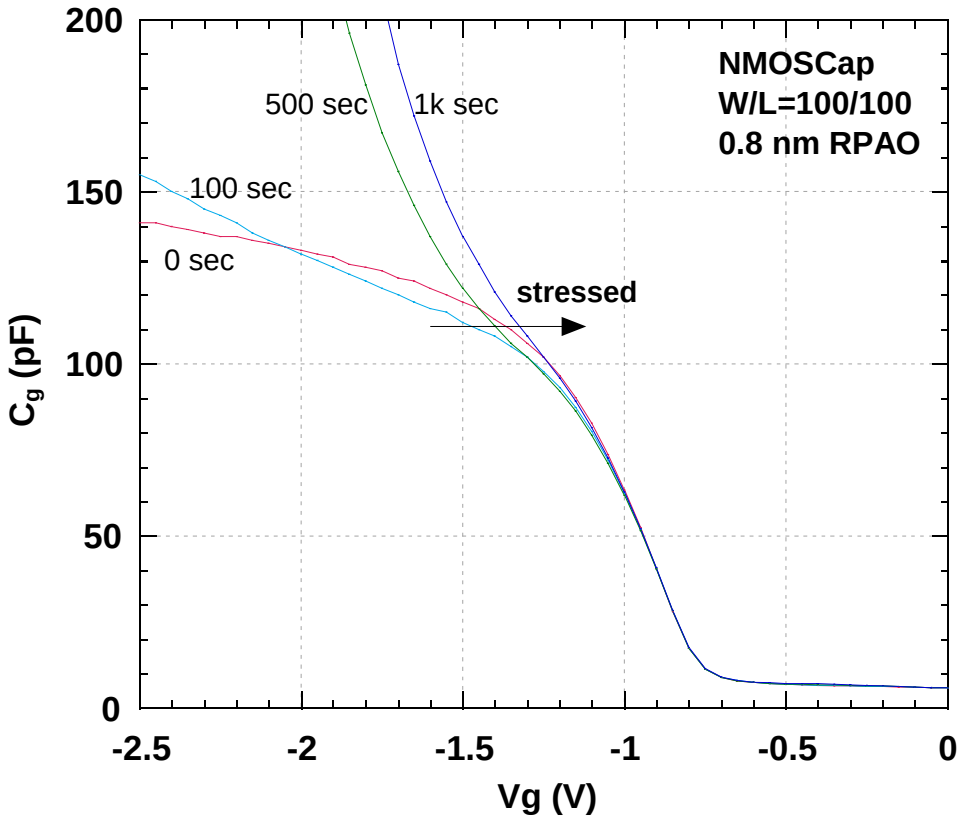
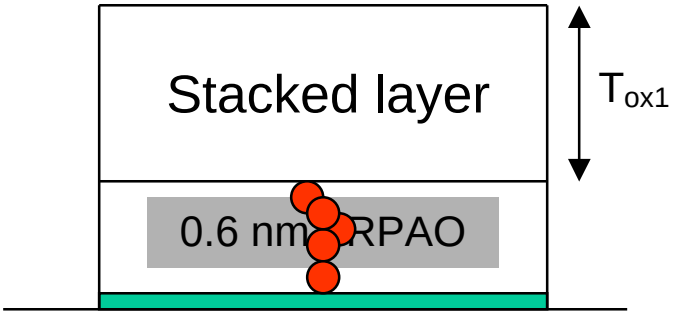
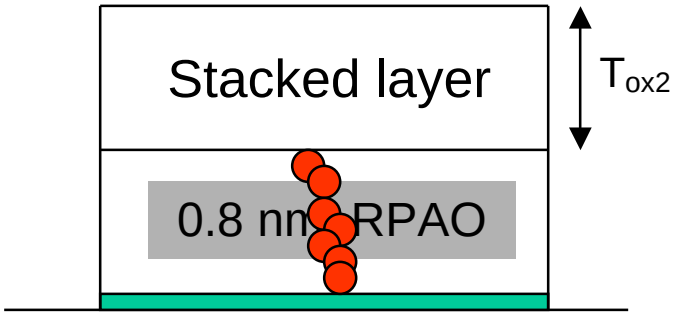


Figure 15 C-V characteristics for a NMOS capacitor with stacked 0.8 nm RPAO/oxynitride gate dielectrics before and after CVS at Vg = -3.52 V. The flat-band voltage of the fresh capacitor is –0.85 V. Significant oxide thinning effect is observed after 100 sec of stress.



(a)



(b)

Figure 16 Oxide thinning effect due to the percolation breakdown path on (a) 0.6nm (b) 0.8 nm RPAO gate stacks. 0.6 nm RPAO structure exhibits larger EOT after a formation of percolation path in the strain oxide layer.

CHAPTER 4

Structural Dependence of Breakdown Characteristics and Electrical Degradation in Ultrathin RPECVD O/N Gate Dielectrics

4.1 Introduction

In recent work [1], it has been shown that SBD in the oxide is not only dominated by a local breakdown mechanism, but is also influenced by geometrical areas of devices. The correlation between area dependence of SBD and the post-SBD conduction mode has also been studied [2]. It was found that a smaller area device showed a larger voltage drop under a constant current stress, and a higher current jump after SBD during CVS. A transition effect from SBD to HBD is observed as the channel length of the MOSFET becomes shorter; however, no significant channel-width dependence has been reported [3].

In this chapter, we further investigate the structural dependence of the breakdown characteristics and the SILC of MOSFETs with stacked O/N gate dielectrics under CVS. The changes in the SILC effect and the device parameters are monitored to evaluate the degradation in device performance during the stress. A carrier separation measurement is used to verify the role of drain leakage current in different gate-length devices.

4.2 Experimental Procedures

Constant voltage stress (CVS) was performed on PMOS field-effect-transistors (FETs) fabricated by standard poly-gate MOSFET processes. The control thermal oxide was grown in a furnace with 4.5% HCl at 700 °C for thickness of 2.0 nm, and stacked O/N dielectrics with interface nitridation were prepared by the RPECVD process [4, 5]. Equivalent oxide thickness (EOT) was determined from high-frequency C-V data in strong accumulation region with correction of quantum-mechanical effects [6]. A constant voltage of –4V was applied to the gate, with source, drain and substrate grounded for a CVS test. The areas of the gate dielectrics ranged from $1.6x10^{-7}$ to $4x10^{-6}$ cm^2. The stress was periodically removed to measure the time dependence of current-voltage characteristics after stressing using an HP 4155B Semiconductor Parameter Analyzer. The devices were stressed for 5k sec or until HBD occurred. The PMOSFET parameters such as V_t, S and G_m were extracted from I_d-V_g characteristics with low drain bias (V_{ds} = -50 mV) to evaluate the device degradation. All measurements in this study were carried out at room temperature.

4.3 Dielectric breakdown and SILC characteristics

Figure 1 (a) displays the time evolution of the gate current through the stacked O/N dielectric (EOT = 1.83 nm) under the application of a constant –4 V bias for gate injection. The stacked O/N dielectric includes a thin oxide interface, ~0.6 nm thick (O), a thicker RPECVD Si_3N_4 layer (N) and approximately one monolayer of N at the Si/SiO_2 interface formed by plasma nitridation. The values are medians of at least 3

tested devices. The gate fluctuations shown in the I-t characteristics for both gate dielectrics correspond to the occurrence of different breakdown spots [1]. The appearance of SBD and HBD is indicated by a small, and a significantly larger and more impressive current jump, respectively. Figure 1(b) provides insight into the small current scales to illustrate SBD phenomena for stacked O/N dielectrics with three different channel-lengths as a function of time. It is obvious that SBD events take place predominantly in the larger channel length transistors; however, the shorter channel transistors (L = 4 μm and 0.8 μm) show a steep current jump due to the appearance of HBD. In this study, SILC was determined by the increase of leakage current in the stressed devices. Figures 2(a)-(c) show the SILC in stacked O/N dielectrics as a function of applied voltages for different channel lengths. It is clearly seen that a continuous increase of SILC is observed as a function of stress time, implying the generation of interface and oxide traps. The SILC mechanism under negative applied bias has been shown to be due to inelastic trap-assisted tunneling by substrate hole injection in PMOSFETs [7]. In other words, hole trapping generated near the anode interface reduces the hole barrier height [8], causing an enhancement of SILC. Figure 2(d) compares the degradation of SILC in various channel length transistors after 1k sec of stress. A transition region from SBD to HBD is observed as channel length decreased. For larger channel-length devices (L = 20 and 8 μm), exponential I-V relationship indicates the onset of SBD. However, for shorter channel lengths (L = 4 and 0.8 μm), linear post-breakdown I-V characteristic indicate that the

occurrence of HBD, that is essentially independent of stressing time. These results reveal a strong channel-length dependence of SILC, which is consistent with the time evolution of breakdown characteristics shown in Figure 1. Based on the dielectric breakdown and SILC characteristics, it may be concluded that early SBD and HBD are triggered by large initial stressing currents, which may be associated with the formation of relative large breakdown areas in the shorter-channel devices [9].

4.4 Electrical degradation of stacked O/N dielectrics under CVS

The degradations in transconductance and threshold voltage shifts were used to evaluate increases in interface states and oxide traps during carrier injection. It has been shown that interface traps and hole trapping are generated in oxide and stacked O/N dielectrics under CVS as evidenced by more negative V_t shifts [10]. Figure 3 illustrates the electrical degradation of thermal oxide and O/N dielectrics by monitoring the change in subthreshold swing and threshold voltage as a function of time. Compared to the thermal oxides, the devices with O/N dielectrics show more V_t shifts at the early stage of stress due to the higher initial hole traps [11]. However, after 1k sec of stress, stacked O/N dielectrics show less degradation in V_t shifts, signifying the suppression of trap generation. Additionally, the oxide devices show more severe subthreshold swing degradation during stress as shown in Figure 3. This can be interpreted by the fact that the generation of defect and interface traps in stacked O/N dielectrics is suppressed by the incorporation of nitrogen at the monolayer level at the Si/SiO_2 interface. In other words, the breaking of strained Si-O

bonds is suppressed due to the formation of stronger Si-N bonds interposed at the anode interface, thus O/N devices show a decreased generation of interface traps and improved breakdown characteristics. Figure 4 depicts the evolution of transconductance degradation for shorter channel device (W/L = 20 μm /4 μm) before and after stress. It is found that transconductance is seriously degraded after 100 sec of stress, leading to mobility reduction and HBD due to the generation of a critical density of stress-induced traps. Figures 5 and 6 illustrate the degradation of transconductance and saturated drain current, respectively, as a function of time for different channel lengths. It is found that g_m is slightly decreased in all of the tested devices before 100 sec of stress; however, beyond 100 sec of stress, the shorter channel transistor shows more than 20% and approximately 10% degradation in g_m and I_{dsat}, respectively. When linear I_g-V_g characteristics (HBD) appear, device on-off characteristic is severely degraded, thus the device parameters such as g_m and subthreshold swing can not be properly extracted due to the high gate leakage current. Figure 7 shows the I_d-V_d characteristics of PMOSFETs after 1k sec of stress. A strong channel-length dependence of I_d degradation has been found. The drain current in the linear and saturation region is significantly degraded with decreased channel lengths due to the enhancement of hole trapping which is evidenced by the increased SILC effect, as was shown in Figure 2(d). In addition, the off-state leakage current (V_g-V_t = -1.8 V, V_d = 0V) is seriously degraded and becomes more positive as channel lengths decreased. This positive off-state drain current results from hole tunneling current from the drain to the gate [12]. Two current components, I_g and $I_{s/d}$, of the fresh and

stressed device with W/L = 20 μm /0.8 μm were measured by a carrier separation experiment, as shown in Figure 8. It can be seen, after 1k sec of stress, an increased positive $I_{s/d}$ appears, indicating an enhancement of hole tunneling from the drain to the gate. For higher gate voltages (> 2V), the gate leakage current is mainly attributed to $I_{s/d}$ which coincides with the value of the off-state leakage current ($I_d \sim 1.8x10^{-4}$ A at $V_d = 0V$) from I_d-V_d characteristics (Figure 7), leading to the degradation of switching capability (Figure 3). It has been proposed that the generation of hole traps at gate/drain junction interface decreases the resistivity of the gate-drain region [13] and the effective oxide thickness due to the formation of local physically damaged region (LPDR) near Si/SiO_2 interface [14]. B. Weir et al. [15] also observed the excess gate current flowing between the gate and the drain. It was indicated that the location of the breakdown spot may be closer to the drain for shorter-channel devices due to the increased probability of breakdown spots over the drain region. In other words, hole injection creates more LPDR near the anode gate-drain overlap region for shorter channel-length transistors and results in hole current tunneling from the drain to the gate, causing an increased off-state drain current. This degraded drain current then results in harder breakdown and more severe degradation.

4.5 Conclusions

The structural dependence of breakdown and electrical degradation in PMOSFETs with ultrathin stacked O/N dielectrics stressed by a CVS are investigated. It is shown that stacked O/N dielectrics with interface nitridation demonstrate less

degradation in subthreshold swing and threshold voltage shifts than the thermal oxide after stress, indicating the suppression of interface traps and hole trapping by the interfacial nitridation process. After 100 sec of stress, a strong channel-length dependence of SILC characteristics and electrical degradation has been observed. The shorter channel-length transistors show harder breakdown and more drastic degradation in device performance. It is concluded that a critical density of hole trapping is easily reached at gate/drain interface for shorter channel devices, causing an enhancement of a positive off-state leakage current. A carrier separation measurement has also been carried out to verify that the gate leakage is mainly attributed to the drain leakage ($I_{s/d}$) tunneling from the drain to gate. Also, the off-state drain current is found to be resulted form this drain leakage, leading to a loss of switching capability and device failure.

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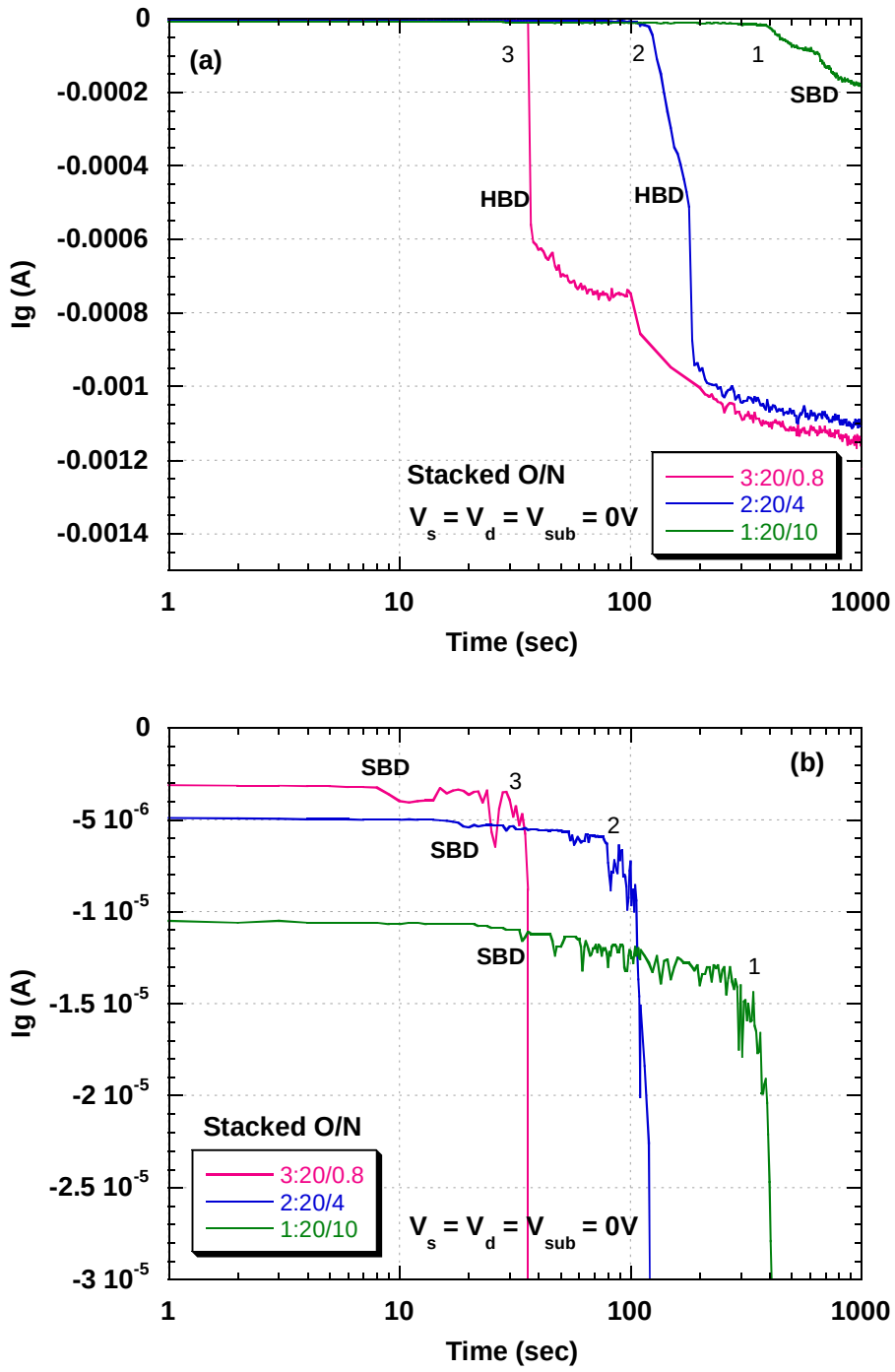

Figure 1 (a) The channel-length dependence of stacked O/N dielectric on the breakdown behavior under a -4 V stress. Stacked O/N devices with L = 4 and 0.8 μm show HBD characteristics. (b) Enlarged portion of (a) showing SBD characteristics.

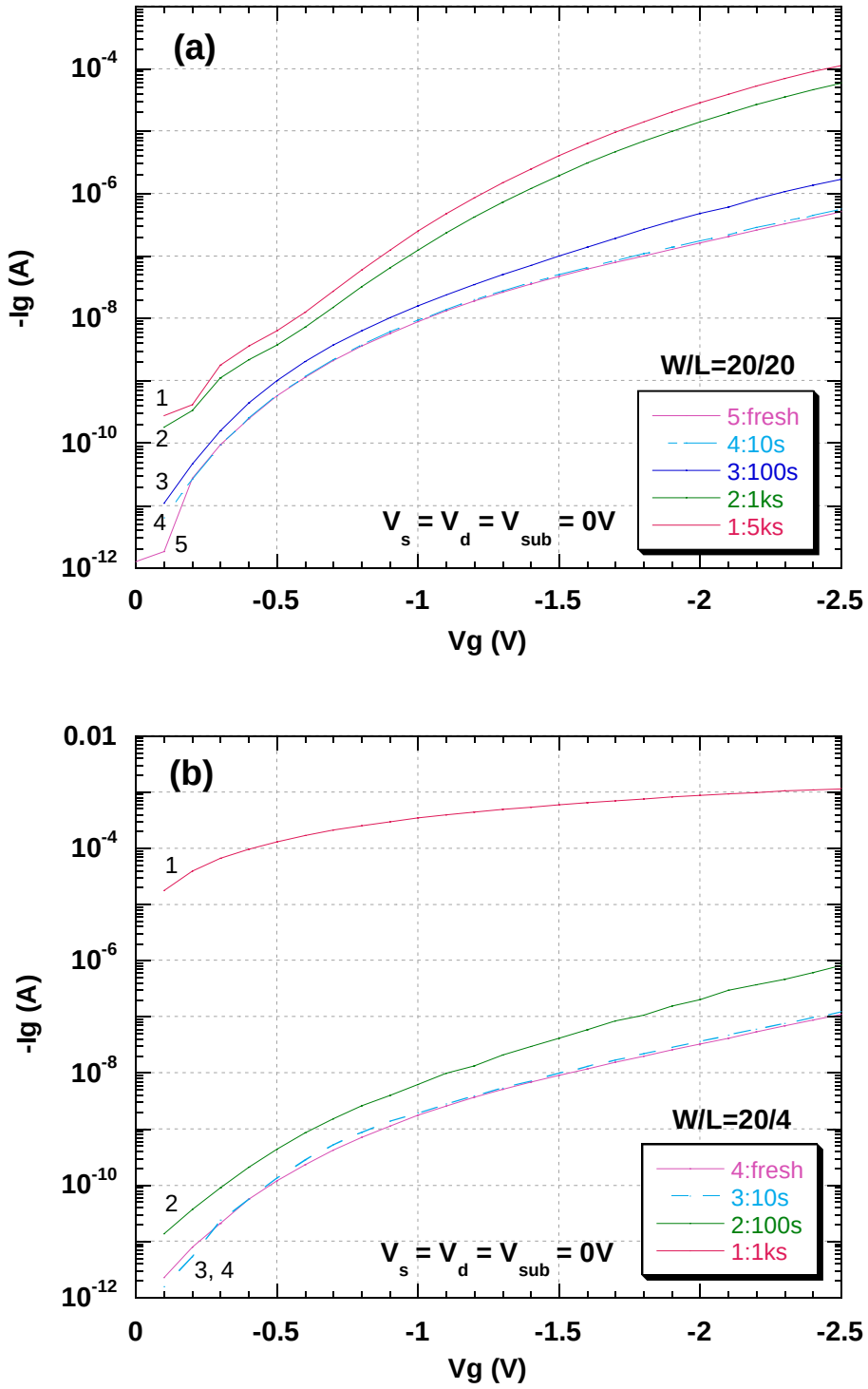

Figure 2 SILC characteristics of fresh and post-stressed O/N devices for different gate lengths (a) L = 20 μm, (b) L = 4 μm under V_g = -4V.

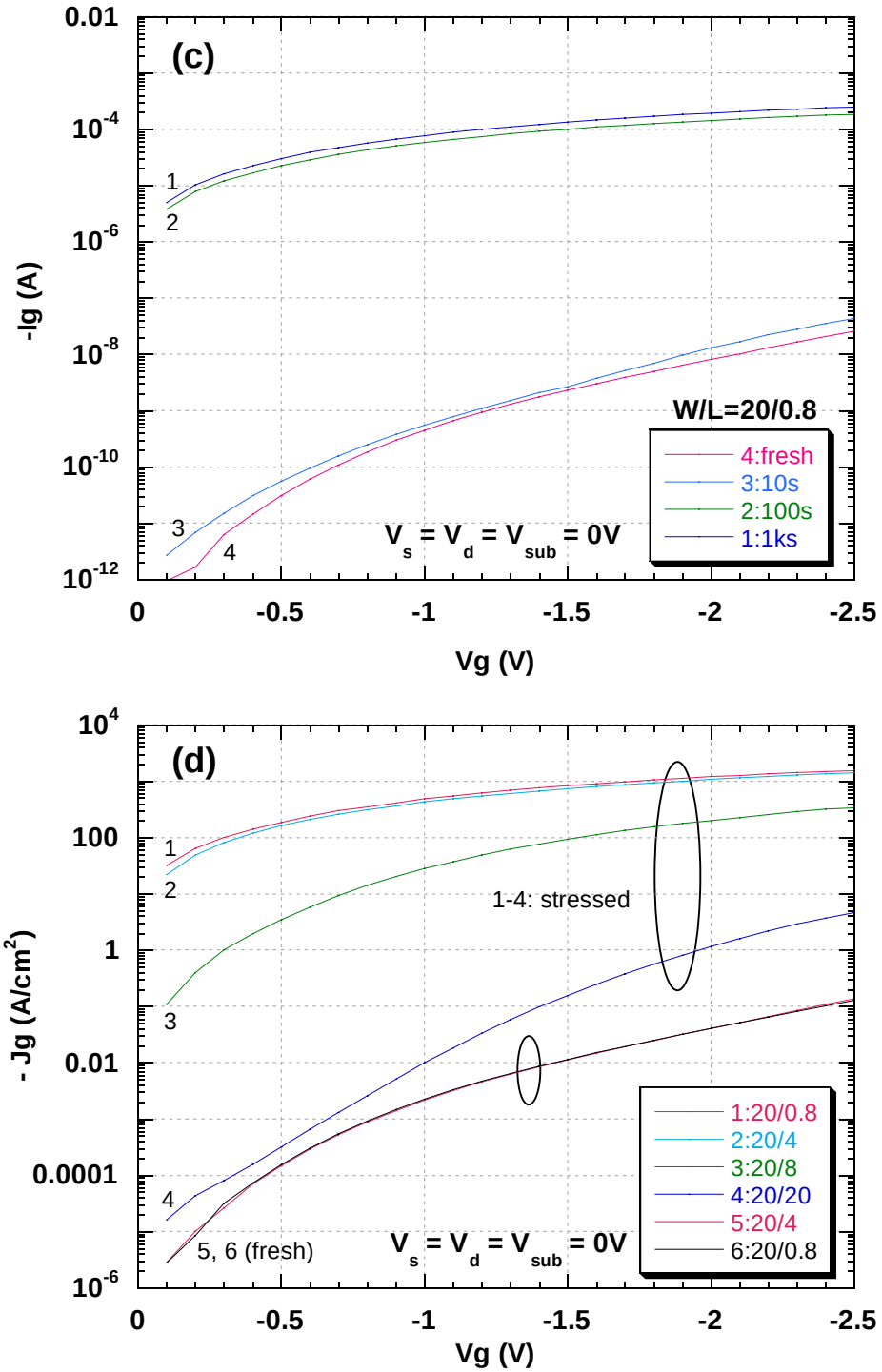

Figure 2 SILC characteristics of fresh and post-stressed O/N devices for different gate length (c) L = 0.8 μm, (d) comparison of SILC for various gate lengths after 1ks of stress (V_g = -4V).

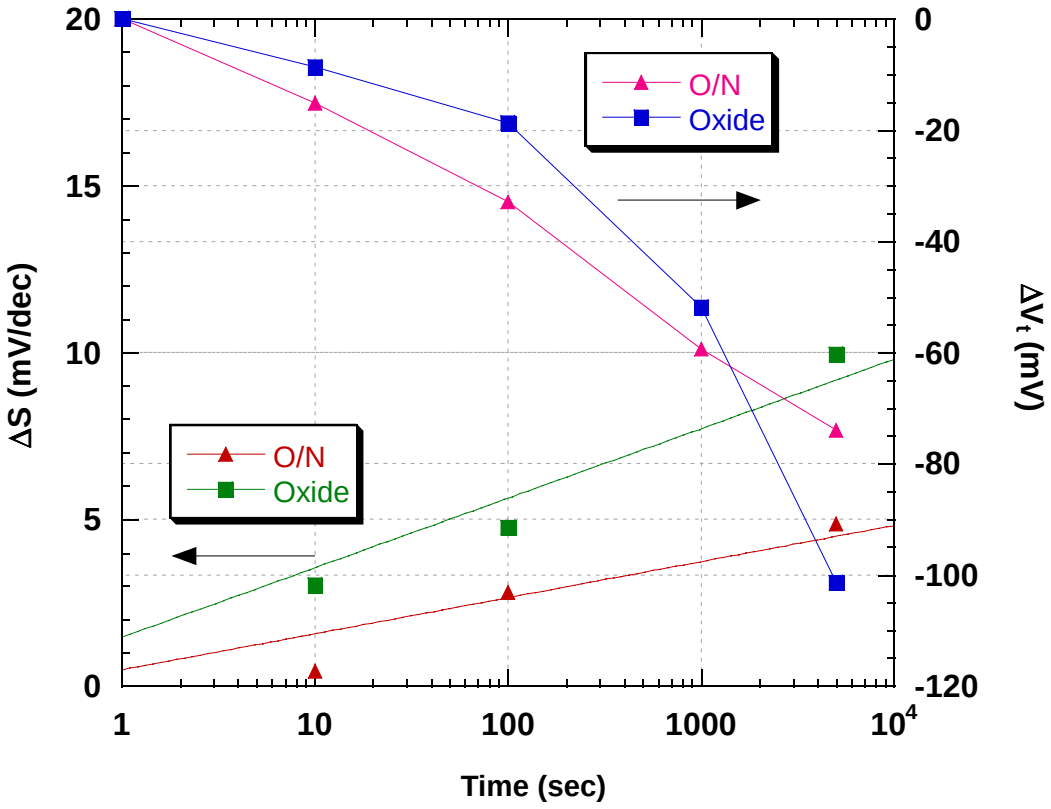

Figure 3 Degradation in threshold voltage (V_t) and subthreshold swing (S) for thermal oxide and O/N dielectrics with W/L = 20 μm/0.8 μm as a function of stress time. Subthreshold swing of fresh oxide and O/N is 76 and 69 mV/dec, respectively.

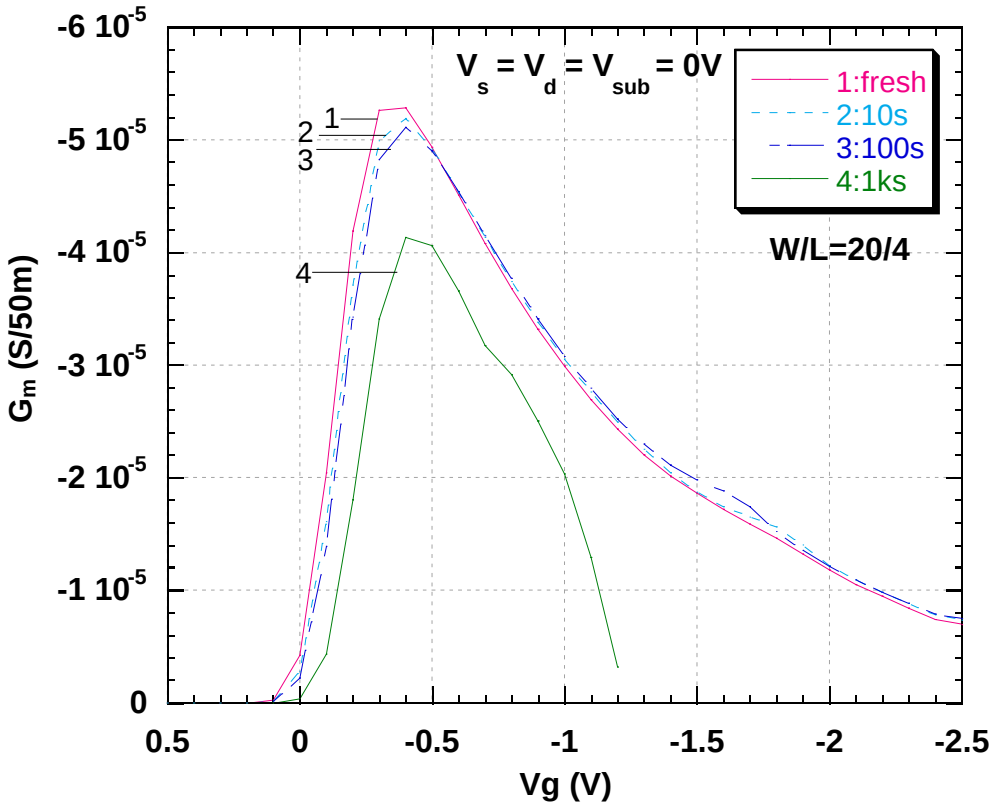

Figure 4 Degradation of stacked O/N devices in transconductance (G_m) as a function of stress time under a –4V stress.

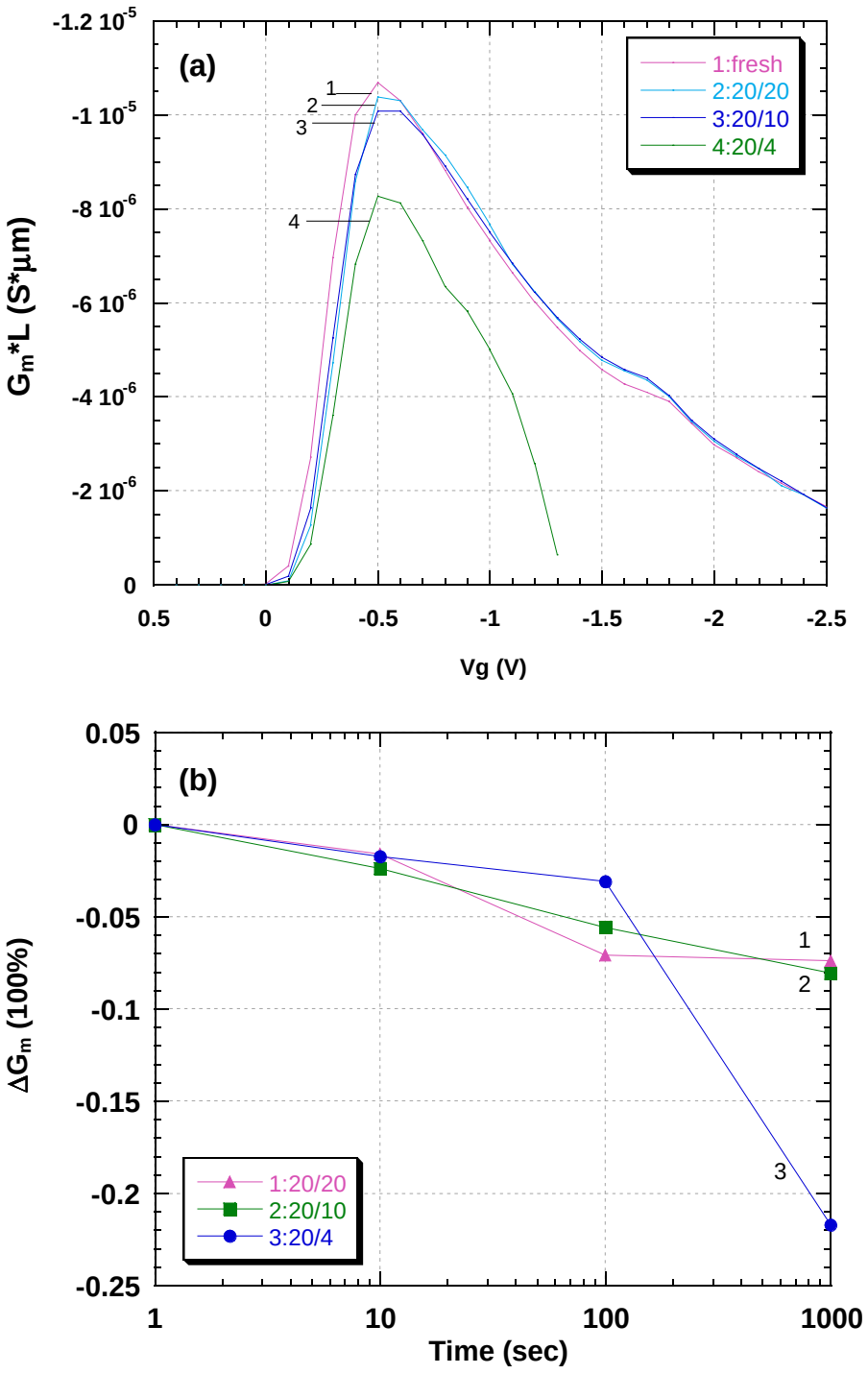

Figure 5 Degradation in G_m of stacked O/N devices for different gate lengths as a function of (a) gate voltages after 1k sec of stress and (b) stress time under a –4V stress.

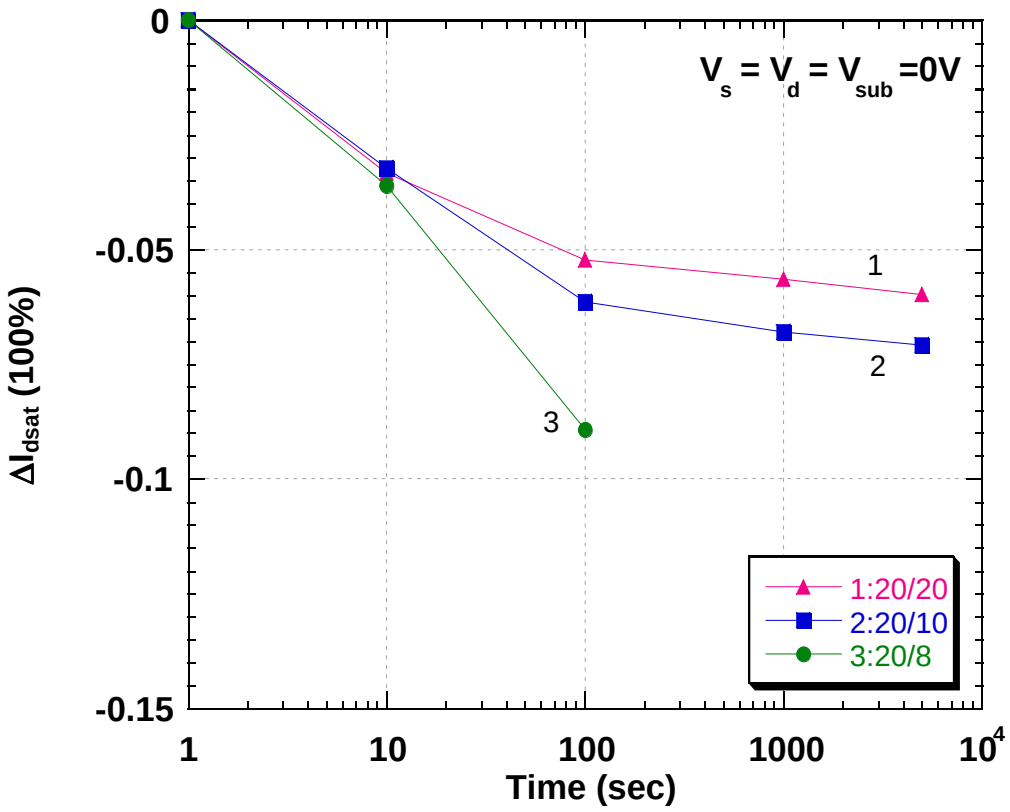

Figure 6 Structural dependence of I_{dsat} degradation as a function of stress time under CVS (V_g = -4V). I_{dsat} was measured at V_d = -2.5 V and V_g-V_t ~ -1.2 V.

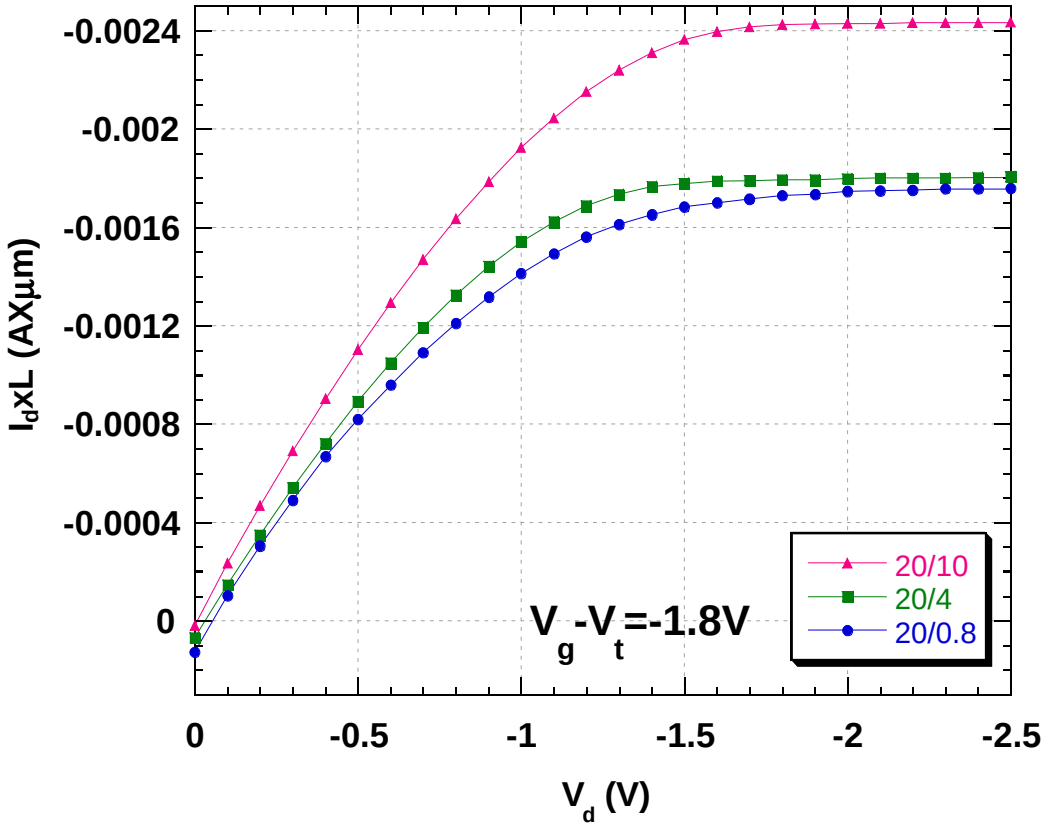

Figure 7 Post-stressed I_d-V_d characteristics for PMOSFETs after 1ks of stress. A positive off-state leakage current indicates hole current tunneling from drain to gate. (Stress condition: V_g = -4V, V_s = V_d = V_{sub} = 0V).

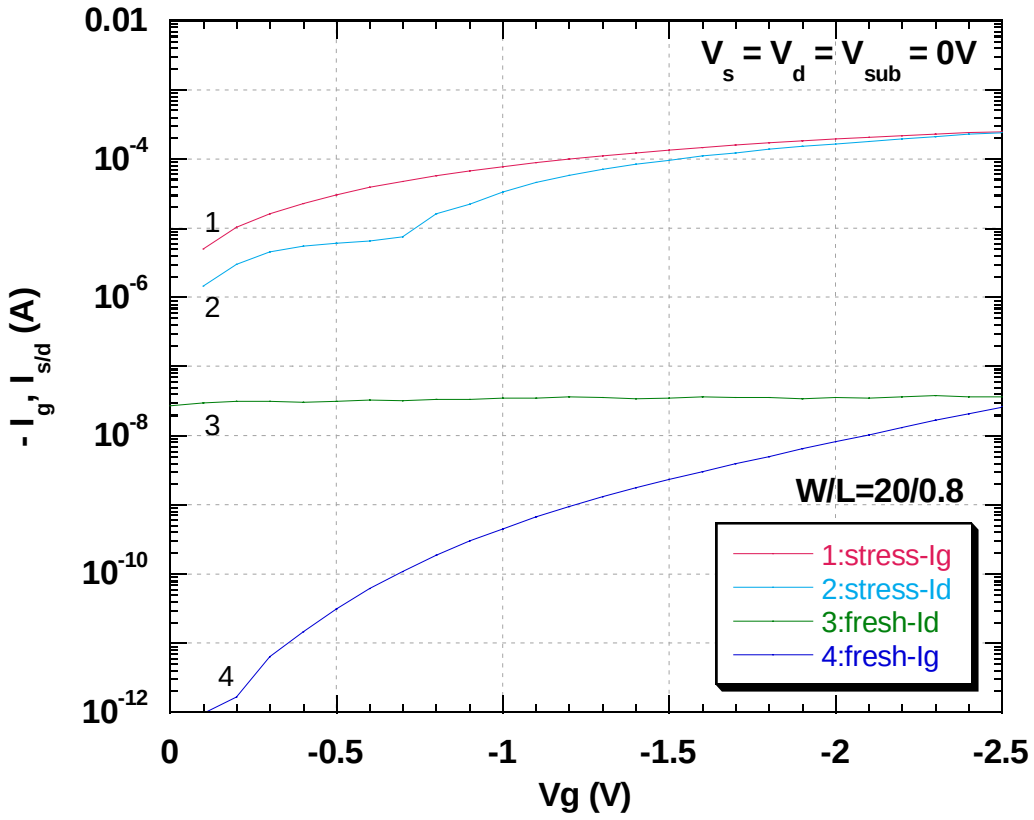

Figure 8 Fresh and post-stressed I_g, $I_{s/d}$ as a function of applied voltages measured by using a carrier seperation technique. ($V_s = V_d = V_{sub} = 0V$).

CHAPTER 5

Reliability Characteristics and Lifetime Projection of MOS Devices with RPECVD Oxide/Nitride Gate Dielectric for Mobile Applications

5.1 Introduction

Aside from increased tunneling leakage current, time-dependent dielectric breakdown (TDDB) is of increasing reliability concern and becomes another limiting factor for oxide scaling and power dissipation in deep-submicron semiconductor devices [1, 2]. The occurrence of TDDB is believed to be due to the formation of a percolation path between anode and cathode electrodes [3]. It has been revealed that TDDB lifetime is degraded at elevated temperatures due to the weaken oxide resistance to the hole transportation [4], increased trap generation rate [5], and a lowering of Si/SiO_2 barrier height [5]. A wide range of activation energies from 0.2 eV to 0.4 eV has been reported [6], which is dependent of the dielectric quality [6], oxide thickness [4, 5], temperature range, and the stress voltage [5, 6]. It was predicted that TDDB reliability may limit the scaling of oxide thickness to ~2.2 nm for a 1 V operating voltage at room temperature [7], and 3.4 nm for 2.5 V at 125 °C [4]. It has been suggested that the reliability of most future devices should be tested for 125 °C [2].

This chapter will focus on the investigation of the voltage and temperature dependence on reliability of ultrathin RPECVD O/N gate dielectric by using the

accelerated TDDB test. The activation energy is determined from the Arrhenius plot, and it can be used to predict the TDDB lifetime over a wide range of temperatures (25 °C to 125 °C) at different stress voltages. Additionally, the 10-year lifetime is projected including effects of temperature acceleration, specified low cumulative failure rate and gate area scaling using the Weibull plot. The maximum operating voltage for the 2.07 nm O/N gate dielectric based on the 10-year lifetime with 0.01% failure rate and total gate area of 0.1 cm^2 at 125 °C is projected.

5.2 Experimental

Devices were fabricated on 0.02~0.05 ohm-cm <100> n-type Silicon substrates using standard CMOS process. The deposition procedures of stacked O/N gate dielectric with plasma interface nitridation were described in Section 2.2 and [8]. The equivalent oxide thickness (EOT) of 2.07 nm was determined from high-frequency C-V curve with quantum mechanical correction [9]. An HP4155B semiconductor parameter analyzer was used to perform constant voltage stress (CVS) on the p^+-poly/n-Si capacitors to evaluate dielectric breakdown and reliability under substrate injection mode. The device breakdown is defined as a sudden increase in gate current. TDDB reliability was performed on PMOS capacitors of area $1x10^{-4}$ cm^{-2}. Every t_{BD} data point at 63.2%-value ($t_{63\%}$) was obtained from a Weibull distribution with 15 samples. The temperature dependence of TDDB was performed on one capacitor at 25, 75 and 125 °C.

5.3 Breakdown behavior and defect-generation rate

Figure 1 shows the time evolution of the gate current for 2.07 nm RPECVD O/N gate dielectric during CVS at 25 °C. In CVS, soft breakdown characteristic shows gate fluctuation, which is attributed to the generation of charge trapping-detrapping at the local percolation paths. A transition region from SBD to HBD is observed, showing increased gate noise. At the onset of HBD, which is triggered by Si-Si bond breakage [10], the abrupt jump in the gate current is about 1~1.5 decade.

The defect generation rate (P_{gen}) is defined as the generated defect density per injected electron, which can be expressed as follows [11]:

$$P_{gen} = \frac{N_{BD}}{Q_{BD}} \tag{5.1}$$

where N_{BD} is the critical defect density defined as $(\Delta J/J_0)_{BD}$ at the occurrence of breakdown event. Q_{BD} refers to the injected charge density at the onset of HBD stage, and is a key factor controlling the dielectric breakdown [12]. In this study, Q_{BD} is determined from the integration of leakage current density as a function of stress times, i.e. $Q_{BD} = \int_0^{t_{BD}} J(t)dt$. As can be seen in Figure 2, the defect generation rate (P_{gen}) at 25 °C shows an exponential dependence on gate voltages, implying that dielectric breakdown and defect creation are also controlled by electron energy for O/N gate

dielectric. It is also observed that P_{gen} for O/N dielectric HBD is lower than that of 2.2 nm SiO_2 [2], but slightly higher than that of SiO_2 (1.4~5.0 nm) modeled by J. Stathis et al. [13]. The difference is possibly due to the charging behavior of interface states and series resistance [13].

5.4 Voltage dependence of T_{BD} and Q_{BD}

The statistics of oxide breakdown described by the Weibull distribution function, given by Equation (3.1), have been introduced in Section 3.3.1. As all data presented in Figure 3, the t_{BD} cumulative distributions exhibit a single Weibull slope β of 1.9 for different stress voltages, indicating the same failure rate [7] and trap generation mechanism in O/N gate dielectric for various stress voltages. It has also been reported that the Weibull slope is voltage insensitive between 3.5 and 3.9 V [12]. This β-value is in good agreement with the measured Weibull slope (~1.8) for the oxides with similar physical thickness (2.8 nm) [12]. On the other hand, 2.07 nm O/N gate dielectric exhibits a larger β than that of SiO_2 (β ~ 1.0 [1, 13]), which in turn gives better lifetime scaling. Figure 4 shows the Weibull distributions of Q_{BD}, which is reduced at higher stress voltages due to the higher defect generation rate, as is shown in Figure 2.

5.5 Temperature acceleration and activation energy

It is widely accepted that higher temperatures degrade TDDB reliability, and a wide range of thermal activation energies has been reported to be a function of applied electric field, oxide thickness and temperature range [6]. For thicker oxides (> 6.5 nm), temperature dependence of field acceleration factor has been reported [14]. This strong temperature dependence may be due to the fact that the effective defect size increases at higher temperature [2, 5]. However, other group reported a constant voltage acceleration of T_{BD} at 63.2% between 30 °C and 200 °C for PMOS capacitors with 2.15 nm oxides [15].

Figure 5 demonstrates the effect of elevated temperature on the Weibull distributions for O/N gate dielectric under a CVS of 3.5 V. It is seen that the t_{BD} drastically decreases at higher temperatures due to higher tunneling current [11] and the increased trap generation rate [5]. There is no strong temperature dependence of shape factor β observed between 25 °C and 125 °C. Indeed, there still exists a debate whether the Weibull slope is dependent of temperature [5, 11, 16]. Since the $t_{63\%}$-value is directly obtained at the operating temperature (125 °C) from the Weibull breakdown distribution, the accurate determination of the temperature shape factor is not critical [5]. As illustrated in Figure 6, the activation energy of $t_{63\%}$ can be determined by the Arrhenius law from the linear relationship between $t_{63\%}$ and inverse temperature, i.e., $t_{63\%} \propto \exp(E_a/k_BT)$, where E_a is the activation energy for defect generation, k_B is Boltzmann's constant in electronvolts per Kelvin (i.e., 8.6×10^{-5}

eV/K), and T is the absolute temperature in kelvin. It is found that the HBD data fit well in the Arrhenius plot at various levels of stress voltages, indicating the same temperature acceleration with an average activation energy of ~0.39 eV. The activation energy was also found to be independent of applied field for oxide thickness thinner than 8 nm [4]. The temperature acceleration factor (K_T) can be predicted using the temperature acceleration model:

$$K_T = \exp\left[\frac{E_a}{k_B}\left(\frac{1}{T} - \frac{1}{T'}\right)\right] \tag{5.2}$$

Based on the exponential relationship in Figure 6, one can see that the temperature acceleration factor is slightly larger at lower temperature (from 25 °C to 75 °C) than that at higher temperature (from 75 °C to 125 °C). The trend is similar to that for ultrathin SiO_2, i.e., temperature acceleration factor decreases as temperature increases [6, 11]. In our devices, the average temperature acceleration factor is about 45 between 25 °C and 125 °C for the average activation energy of 0.39 eV.

5.6 Device lifetime projection by TBBD reliability

In this section, the conventional voltage and temperature acceleration models are used to predict the TDDB lifetime at elevated temperature, low voltage and low percentile failure rate. Figure 7 shows the TDDB lifetime and projection lines of p^+-poly/n-Si capacitors using the Weibull distribution. Fifteen data points were collected

for each applied voltage. The solid line is for a least-squares fit of $\ln(t_{BD})$ versus V_g, which yields a correlation coefficient of R ~ 0.99. For 2.07 nm O/N gate dielectric, the voltage acceleration factor, $\gamma = -\partial\ln(t_{BD})/\partial V$, of time-to-breakdown is calculated as 14.3 decade/V from the slope of the solid line, independent of temperature as suggested in [17]. There is a consensus that the breakdown spots are randomly created through the oxide according to a Poisson distribution as given below [18, 19]

$$\ln[-\ln(1-F)] - \ln[-\ln(1-F_\alpha)] = \ln\left(\frac{A}{A_\alpha}\right) \tag{5.3}$$

Thus the area dependence of the Weibull scaling factor is then given by [20]:

$$\frac{t_\alpha}{t_{BD}} = \left(\frac{A}{A_\alpha}\right)^{\frac{1}{\beta}} \tag{5.4}$$

where t_α and t_{BD} correspond to the cumulative functions on the area of the test structure A_α, and the total gate area A on a chip, respectively. Figure 8 shows the time evolution of gate current for various gate areas, at which the time-to-HBD can be determined. Figure 9 shows the normalized Weibull distributions for a CVS of 3.7 V at 25 °C. It is clearly seen that all t_{BD}-data fall on a line with slope of ~1.9, indicating that the breakdown can be explained by the percolation model [21] and Poisson area

scaling is also valid for RPECVD O/N gate dielectric. Furthermore, this result reveals that the defects are randomly generated during intrinsic breakdown. Figure 10 illustrates the Weibull distributions scaled from tested structure to the larger area (=0.1 cm^2) using Equation (5.4). The lifetime at low percentile failure rate can be scaled by $[F/F_\alpha]^{1/\beta}$ [7, 13], in which F is the failure rate at 63.2% and F_α is the desired low percentile failure rate. Figure 11 illustrates an example of a projection of the maximum operating voltage for 2.07 nm O/N gate stack by considering (1) temperature acceleration, (2) Poisson area scaling, (3) recalculation of failure rate and (4) gate voltage acceleration. The dotted lines in the figure represent the lifetime projection for 125 °C, low percentile failure rate of 0.01% and a total gate area of 0.1 cm^2 using γ and Equation (5.4) with the Weibull slope. It is projected that the maximum tolerable operating voltage is ~1.9 V for 2.07 nm O/N gate dielectric with a 10-year TDDB lifetime.

5.7 Conclusions

In this work, the voltage and temperature dependence on reliability for ultrathin RPECVD O/N gate dielectric has been investigated. There are no statistically significant differences in the values of the Weibull shape factor (=1.9) for different stress voltage levels. The activation energy of 0.39 eV is determined from the Arrhenius law, and the temperature acceleration factor is about 45 between 25 °C and 125 °C. It is also demonstrated that the use of a Poisson statistical model, i.e., area scaling, is valid for RPECVD O/N dielectric breakdown, which can be explained

by the percolation model. For the 10-year reliability projection, the maximum operating voltage for 2.07 nm O/N gate dielectric at 125 °C is estimated to be ~1.9 V for a total gate area of 0.1 cm^2 with 0.01% failure rate from a linear TDDB projection with Poisson area scaling and a constant voltage acceleration factor of 14.3 V^{-1}.

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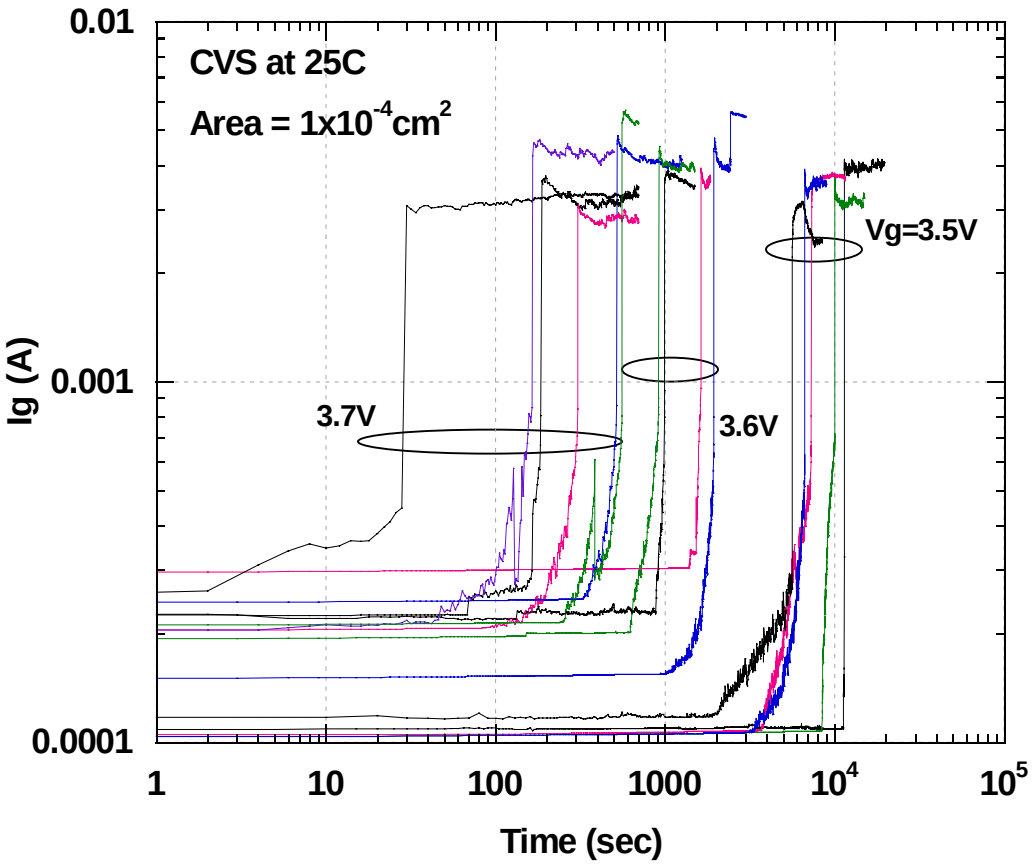


Figure 1 The time evolution of the gate current during stress for various stress conditions. The device breakdown can be clearly seen by the occurrence of a sudden current jump.

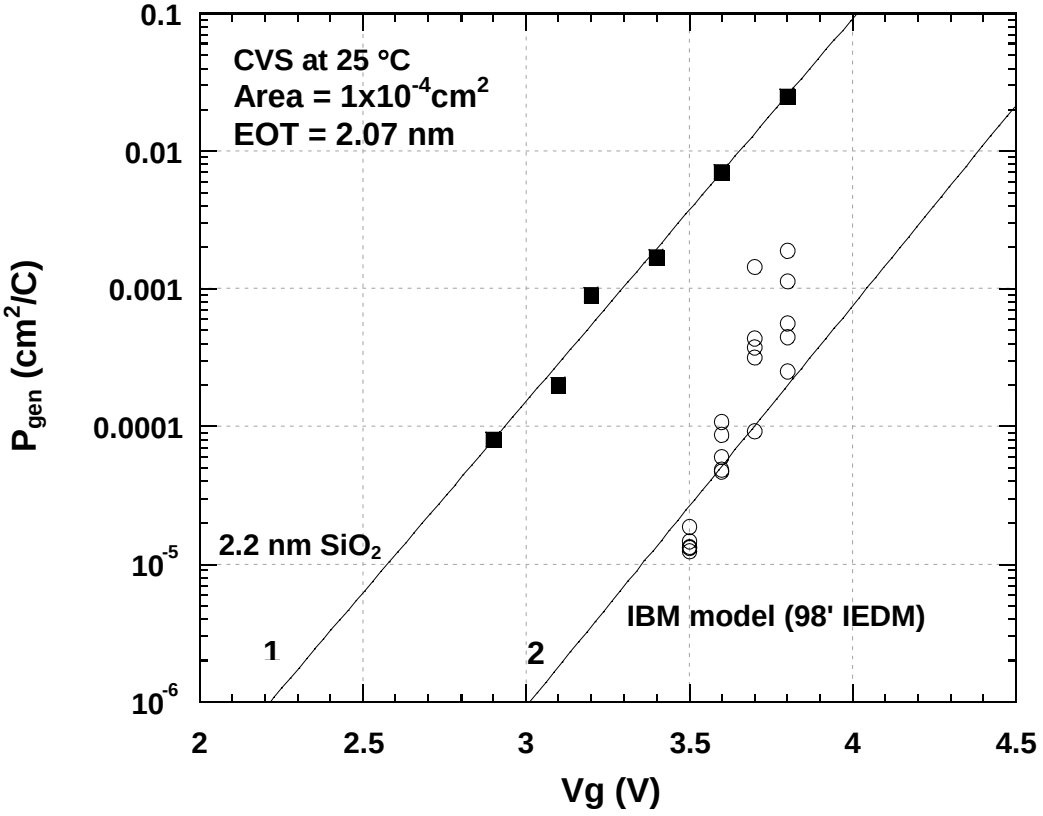


Figure 2 Defect generation rate (P_{gen}) as a function of stress voltages. (open circles: experimental data, line 1: 2.2 nm SiO_2 [2], line 2: IBM model for SiO_2 [13])

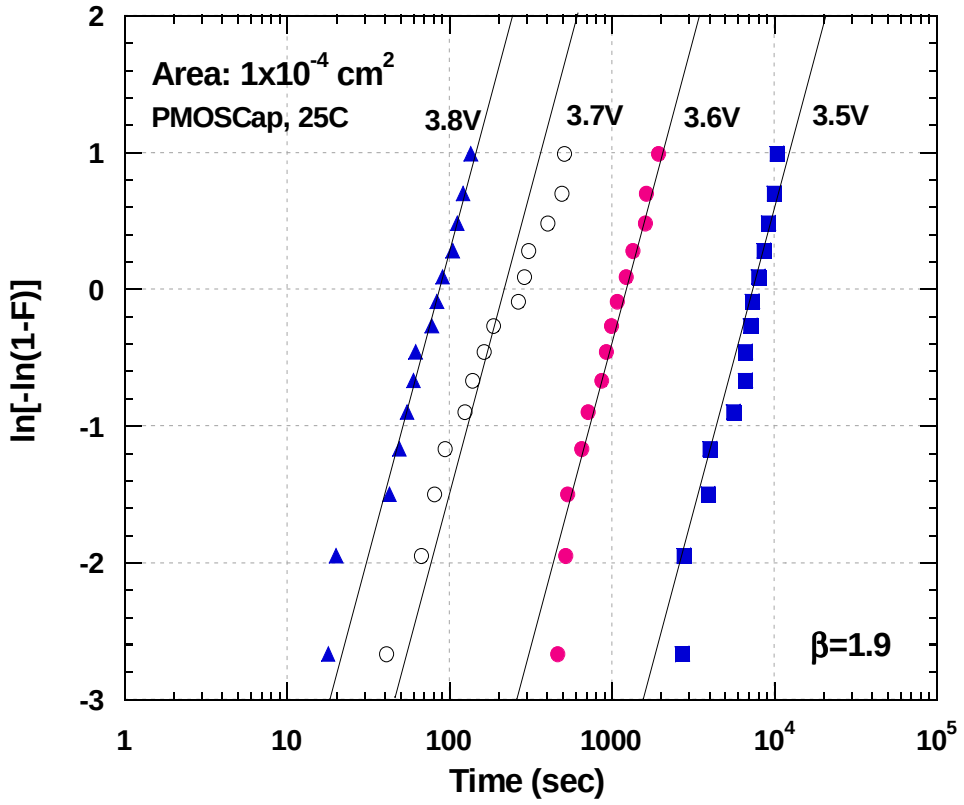


Figure 3 Time-to-breakdown (t_{BD}) distributions for several constant voltage stress levels fitted using a accurate maximum likelihood fitting algorithm. The label expressed as ln[-ln(1-F)] is the so-called Weibull scale. The physical dielectric thickness is 2.8 nm (EOT = 2.07 nm).

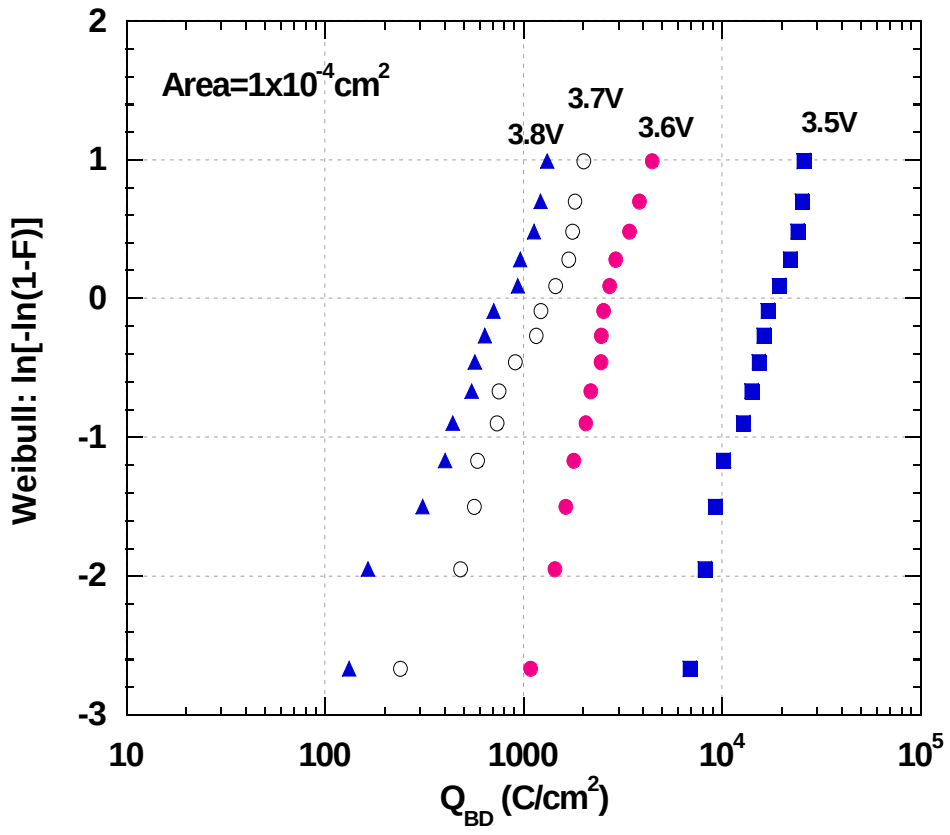


Figure 4 Charge-to-breakdown (Q_{BD}) distributions for PMOS devices with 2.07 nm O/N dielectric under CVS (from 3.5V to 3.8V) at 25 °C.

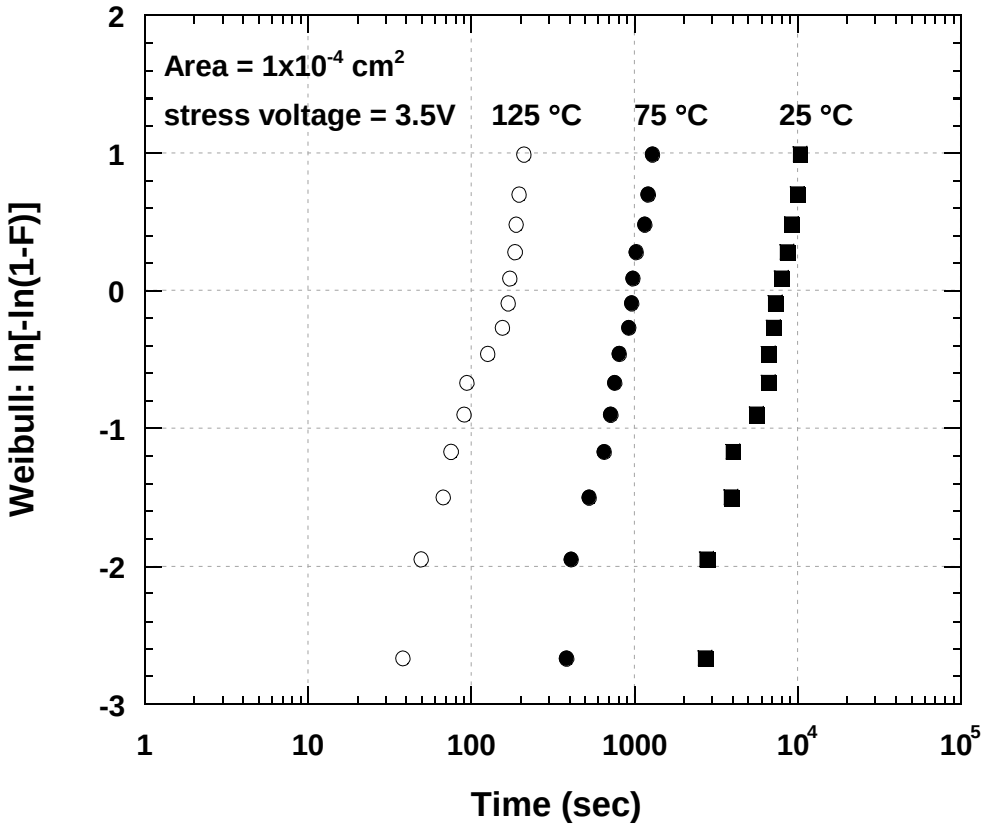


Figure 5 Weibull distributions of t_{BD} for 2.07 nm O/N gate dielectrics stressed at V_g = 3.5 V and elevated temperatures.

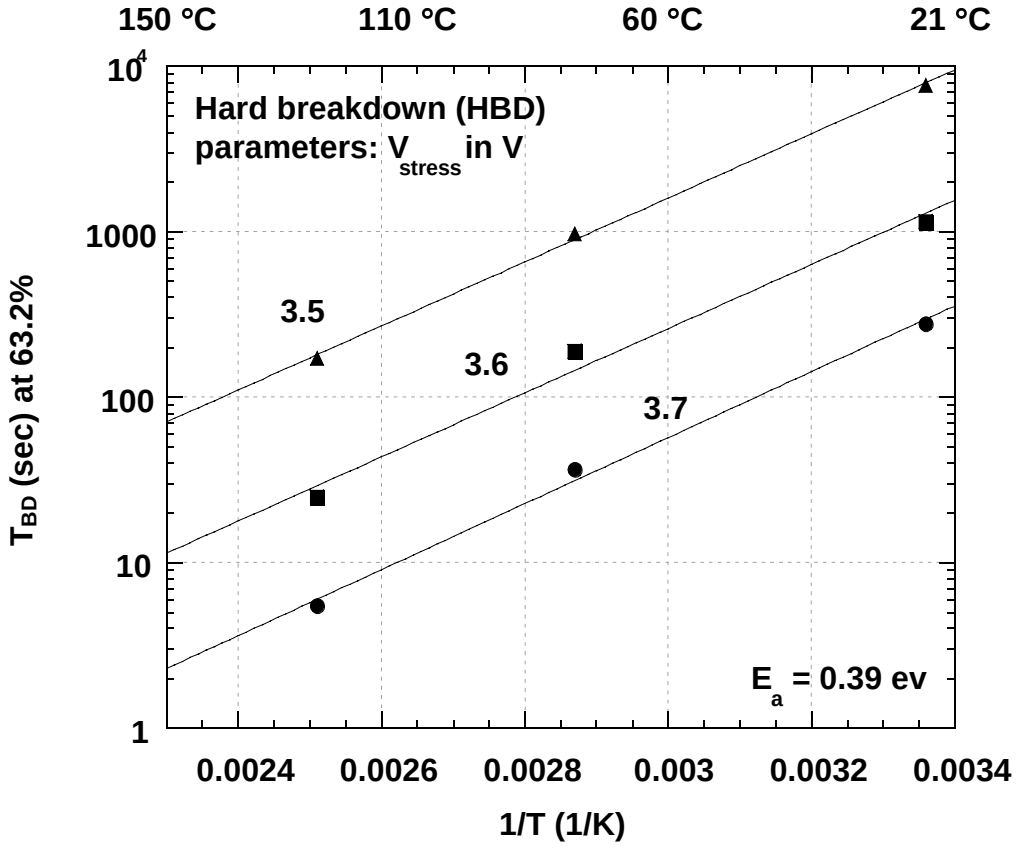


Figure 6 Arrhenius plot for t_{BD} at 63.2% under CVS. The activation energy was determined from the slope. The capacitor structure with $1x10^{-4}$ cm^2 was used. The total number of tested samples is 135.

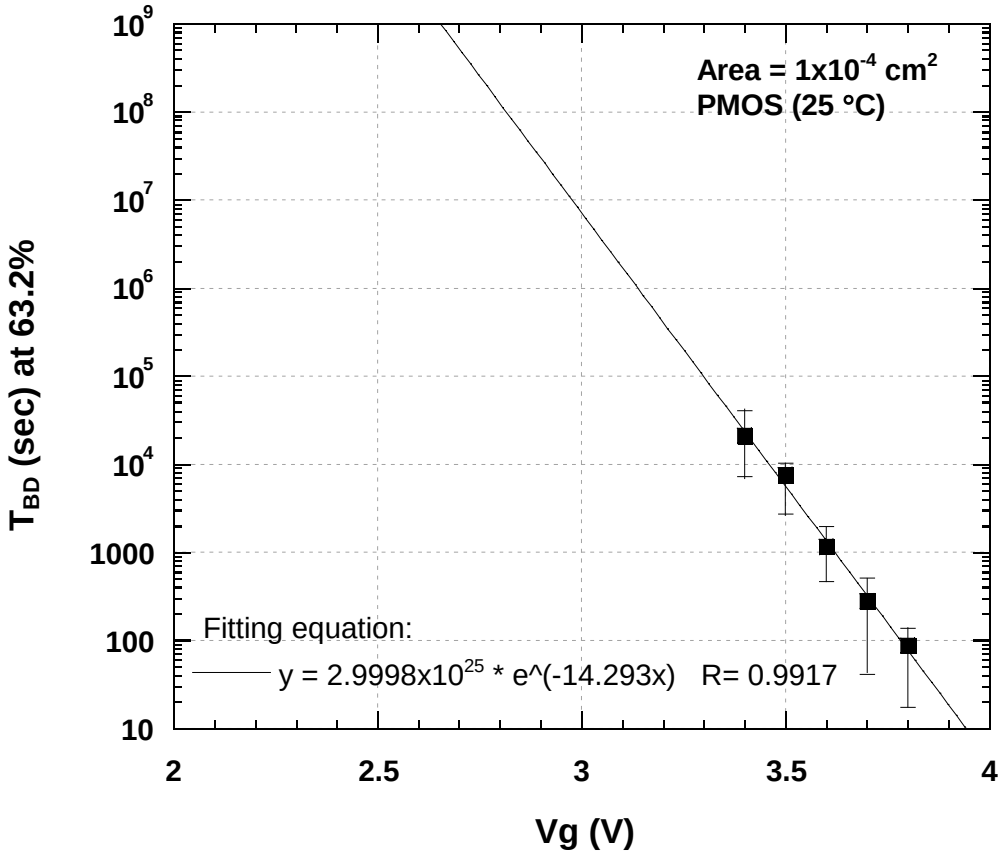


Figure 7 A typical TDDB plot for 2.07 nm stacked O/N gate dielectric at 25 °C. The solid line represents the fit of 63.2%-t_{BD} data; error bars show the upper and lower limits of each experimental data. A voltage acceleration factor of 14.3 V^{-1} is determined from the slope of the fitting line.

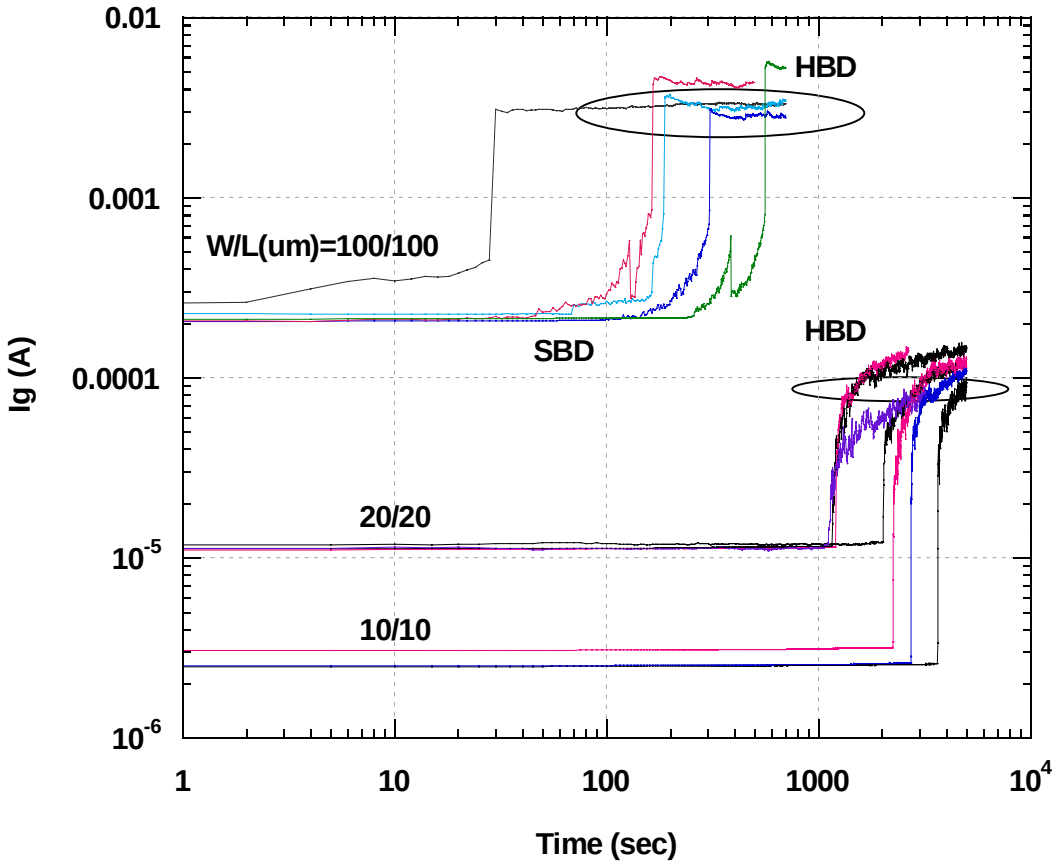


Figure 8 Observed soft and hard breakdown in stress current vs. time for 2.07 nm O/N gate dielectric with Vg = 3.7V at 25 °C.

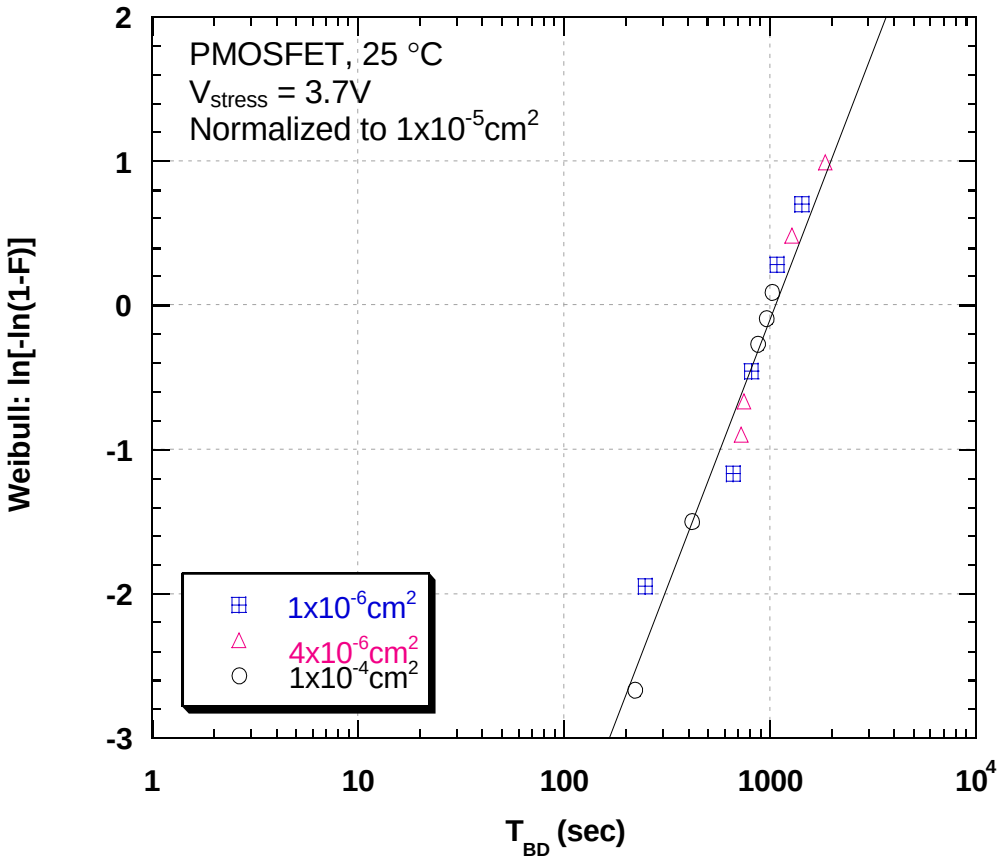


Figure 9 Normalized Weibull distributions (β is ~1.9) of 2.07 nm O/N dielectric with various capacitor areas using Poisson area scaling with the data given in Figure 8.

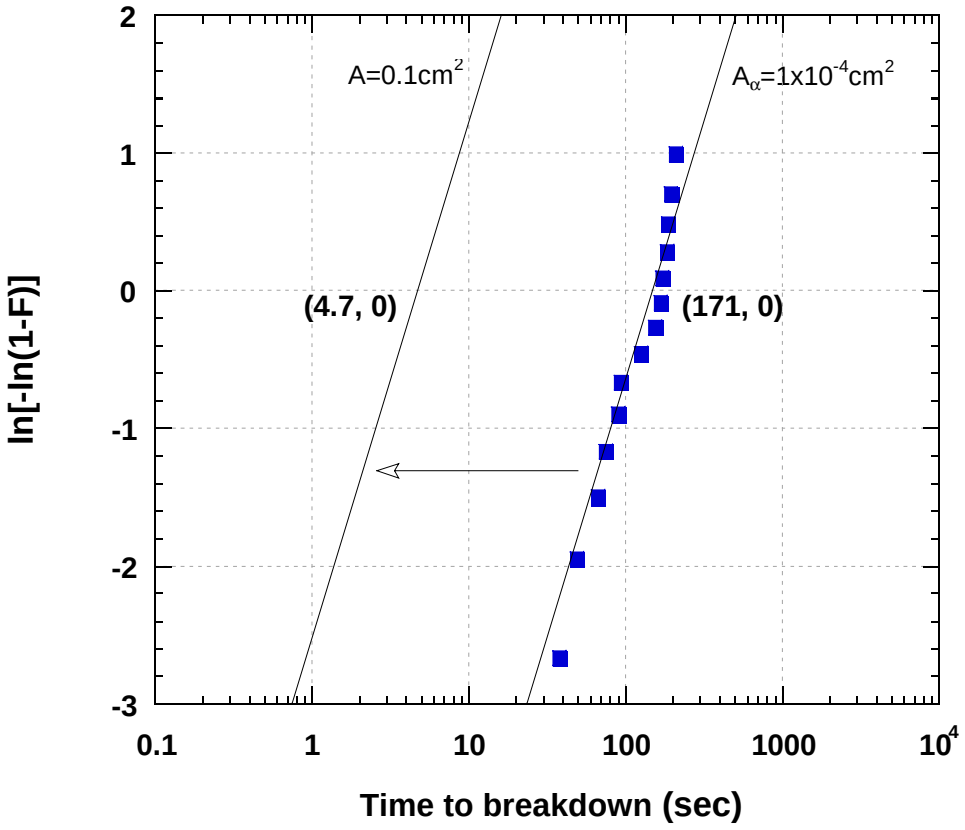


Figure 10 Scheme of the Weibull distributions for 2 areas using Poisson area scaling under a 3.5V stress at 125 °C. The Weibull slope β is ~1.9.

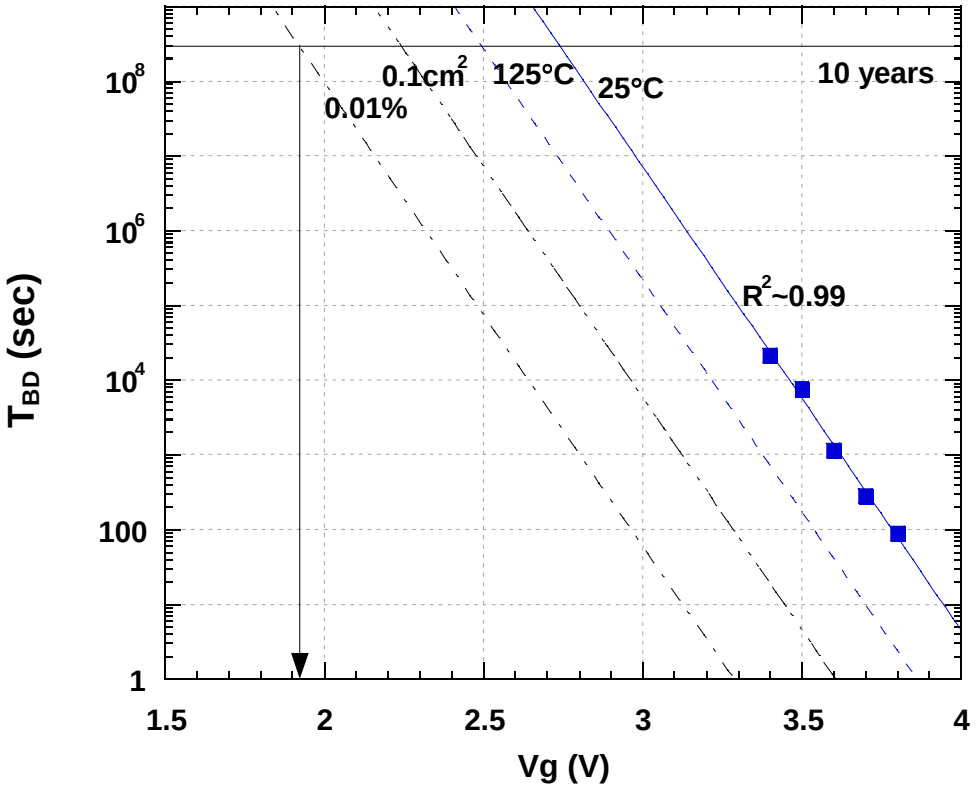


Figure 11 A prediction of the maximum operating voltage for 2.07 nm stacked O/N gate dielectric at low percentile failure rate of 0.01% by applying area scaling model and a voltage-dependent lifetime projection with a constant voltage acceleration factor of 14.3 V^{-1} (symbols: experimental data, solid and dotted lines: fitting lines).

CHAPTER 6

Thesis Summary and Future Research

This dissertation has focused on the breakdown and reliability characteristics of RPECVD oxide/nitride (O/N) and oxide/oxynitride gate dielectrics during electrical stress. The objectives of this research are: (1) to detect and investigate the breakdown behavior (SBD and HBD) of these RPECVD gate stacks under constant current stress (CCS) and constant voltage stress (CVS), (2) to characterize the charge trapping and its impact on the electrical properties of the devices during the stress, (3) to study the impacts of interface properties, interface nitridation and RPAO thickness, on the dielectric breakdown and TBBD reliability, (4) to investigate the dependence of channel gate-length on the dielectric degradation and breakdown, (5) to reveal the reliability parameters, such as the Weibull slope, temperature and voltage acceleration factor, and to project the maximum tolerable operating voltage for 10-year lifetime based on specific conditions.

6.1 Summary

(1) During CCS, the thermal oxide shows early SBD and HBD for both gate and substrate injection compared to stacked O/N and oxynitride gate dielectrics prepared by RPECVD technique. Also, O/N and oxynitride gate dielectrics show the reduced post-breakdown leakage current, which correlates with the blocking degree of boron penetration.

(2) For PMOS devices, the positive traps are generated in these gate dielectrics as evidenced by negative threshold voltage shifts under electrical stresses. In contrast, negative charges are created for NMOS devices under gate injection, which give rise to a positive ΔV_{FB} shift.

(3) The thermal oxide device stressed under substrate injection show harder breakdown and severe degradation than under gate injection, implying a larger amount of stress-induced damage created at the Si/SiO_2 interface. In contrast, nitrogen incorporation forms B^+-N bonds and reduces the dangling bonds and strained Si-O bonds in O/N and oxynitride gate structures. Therefore, RPECVD gate stacks show improved off-state leakage current and the electrical degradation after the stress.

(4) The hole trapping causes a detrimental impact on the thermal oxide, such as serious degradation and early breakdown. On the other hand, interface nitridation in RPECVD gate stacks improves immunity of hole trapping at the SiO_2/Si and gate/drain interfaces against CVS, thus reduces the post-breakdown leakage current and the positive drain leakage.

(5) The impact of RPAO thickness of stacked oxide/oxynitride dielectrics on the breakdown and reliability characteristics has been investigated. It is shown that the thinner RPAO layer (0.6 nm) exhibits reduced SILC and threshold voltage shift, indicating less damage and stress-induced trap density in thinner strained RPAO after stress. Therefore, both P- and NMOS devices with 0.6 nm RPAO give better TDDB reliability. Furthermore, the devices with

different RPAO thickness exhibit a similar Weibull slope β for a fixed gate voltage. This observation implies that the strained RPAO layer in the gate stacks affect the defect generation rate related to SILC, but the RPAO thickness does not affect the breakdown mechanism at which the percolation model is applied.

(6) A strong channel-length dependence on the breakdown characteristics of MOSFETs has been observed after 100 sec of CVS. The shorter channel-length transistors show harder breakdown and severe performance degradation with the presence of a positive off-state drain leakage. This is due to the increased probability of stress-induced damage at the gate-drain overlap region of the shorter channel. Furthermore, it has been demonstrated that the post-breakdown leakage current for shorter channel devices is mainly attributed to the off-state drain leakage, which is verified by a carrier separation measurement.

(7) It is proven that the stress-induced breakdown spots created near the gate/drain overlap region will enhance the hole tunneling from the drain to gate, which results in the degraded drive current and off-state drain leakage and finally leads to HBD and complete failure of device functionality.

(8) The TDDB reliability of RPECVD O/N gate dielectrics (EOT = 2.07 nm) is investigated by accelerated voltage/temperature tests. The reliability parameters such as the Weibull slope, voltage and temperature acceleration factors are revealed. We first reveal that the Weibull slope β is around 1.9 and

is insensitive in the voltages from 3.5 V to 3.8 V. The comparison of β value between O/N stacks and other high-k gate materials is presented. The voltage acceleration factor of 14.3 decade/V is then determined with a correlation coefficient of R ~0.99.

(9) The temperature acceleration factor is 45 from an Arrhenius relationship. The activation energy of 0.39 eV for 2.07 nm O/N gate dielectric from 25 °C to 125 °C is reported for the first time.

(10) It is demonstrated that Poisson area scaling is also valid for RPECVD O/N dielectric breakdown, indicating that the occurrence of breakdown sites is a random process and can be explained by the local percolation model.

(11) For 10-year reliability, the maximum tolerable operating voltage for 2.07 nm O/N gate dielectrics at 125 °C is estimated to be ~1.9 V for a 0.01% failure rate (100 ppm) and a total gate area of 0.1 cm^2 on a chip from a linear TDDB projection with the Poisson area scaling and a constant voltage acceleration factor of 14.3 decade/V.

6.2 Future Research

Additional studies of the SILC and voltage shift from C-V characteristics are required to investigate the stress-induced defect density and defect size for different stacked dielectric thickness. This would be very helpful to understand their physical breakdown mechanisms on the basis of the percolation model.

It would be interesting to investigate TDDB reliability based on different breakdown criterions (i.e., SBD and HBD). This is because the gate-area scaling behavior may be different between SBD and HBD. Also the polarity effects on the breakdown distribution in stacked gate dielectrics should be studied in details. Furthermore, the breakdown of RPECVD gate dielectrics limited by either charge traps in the bulk layer or interfacial RPAO also needs further investigation by the effect of stress polarities. If the reliability is limited by the trap generation in the bulk layer rather than in the RPAO layer, then a strong thickness dependence of Weibull slope β should be observed.

The intrinsic reliability of alternative gate dielectrics needs to be considered carefully besides the gate leakage current for the future scaling. As discussed in Section 5.1, even though the gate leakage is below the acceptable level (i.e., 1 A/cm^2), the gate material may not have the required reliability. This is because reliability projection is conducted based on the specific low failure rate, total gate area and the operating temperature. Therefore, the determination of Weibull slope β under accelerated test conditions becomes critical since it controls the acceleration parameters such as area scaling and voltage/temperature acceleration factors.

Temperature dependence of the Weibull slope for sub-2 nm O/N and oxynitride gate dielectrics is still an open question until now, even though a single β-

value is observed in this study. Therefore, acceleration testing with a wider temperature range between 25 °C and 200 °C is suggested to be carried out. Although an Arrhenius relationship is expected for a fixed gate voltage, the temperature acceleration may appear to be non-Arrhenius at lower temperature (below 25~30 °C). If this is the case, a universal model including the second-order term ($1/T^2$) should be developed to extract the activation energy. More research is required to complete the understanding of dielectric breakdown as a function of temperature.

Another issue of interest is the role of interface properties of ultrathin gate stacks on the TBBD reliability. This is because some of the alternative gate dielectrics may involve multiple interfaces, and defects may generate nonuniformly at these internal interfaces. This nonuniform defect generation would decrease the Weibull slope β, leading to degraded device lifetime. Therefore, improvements in the interface properties can provide more reliable reliability parameters to accurately predict the device lifetime. Additionally, the ultimate scaling of stacked oxide/nitride (or oxynitride) gate dielectrics may be performed by shrinking the thickness of RPAO thickness down to 3~5 °A. However, the trade-offs between electrical properties (e.g., boron penetration and mobility degradation) and better device reliability should be considered.

APPENDIX A
Fundamentals of Semiconductor Devices

First, we review the basic concepts of semiconductor devices. Secondly, the energy-band diagrams of MOS structure under flat-band, accumulation, depletion and strong inversion mode are discussed. Finally, the fundamental concepts and operations of MOSFETs are also reviewed.

A.1 Fundamental concepts and basic equations

One of the key equations governing the operation of VLSI devices is Poisson's equation:

$$\frac{d^2\psi(x)}{dx^2} = -\frac{dE}{dx} = -\frac{\rho(x)}{\varepsilon_{si}} \qquad \text{(A.1)}$$

where $\psi(x)$ is defined as the amount of band bending at position x, $\rho(x)$ is the charge density per unit volume at x and ε_{si} is dielectric constant of silicon. There are two kinds of charge in silicon substrate: fixed charge and mobile charge. Fixed charges are ionized acceptors (negative charges) and donors (positive charges). Mobile charges are holes and electrons. Therefore, for a homogeneous p-type or n-type silicon substrate with no applied field, the potential is constant throughout the material.

The next sets of equations are current-density equations. Each current component is the sum of drift and diffusion current density:

$$J_n(x) = q\mu_n n(x)E(x) + qD_n \frac{dn(x)}{dx} \tag{A.2}$$

$$J_p(x) = q\mu_p p(x)E(x) - qD_p \frac{dp(x)}{dx} \tag{A.3}$$

The next sets of basic equations are continuity equations based on the conservation of mobile charges as a function of time.

$$\frac{\partial \delta p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial x} - \frac{\delta p}{\tau_p} \tag{A.4}$$

$$\frac{\partial \delta n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} - \frac{\delta n}{\tau_n} \tag{A.5}$$

At thermal equilibrium, the recombination rate and generation rate are equal, Equations (A.4) and (A.5) can then be reduced to

$$\frac{\partial \delta p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial x}$$

$$\frac{\partial \delta n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} \tag{A.6}$$

The total current density is then the sum of the electron and hole current:

$$J(x) = J_n(x) + J_p(x) \tag{A.7}$$

A.2 MOS structure in different modes

When a voltage V_g is applied to the MOS gate, four kinds of potential changes are encountered:

1. The external gate voltage V_g
2. The potential drop across the oxide Ψ_{ox}
3. The surface potential of silicon substrate Ψ_s
4. The potential difference between metal and substrate ϕ_{ms}

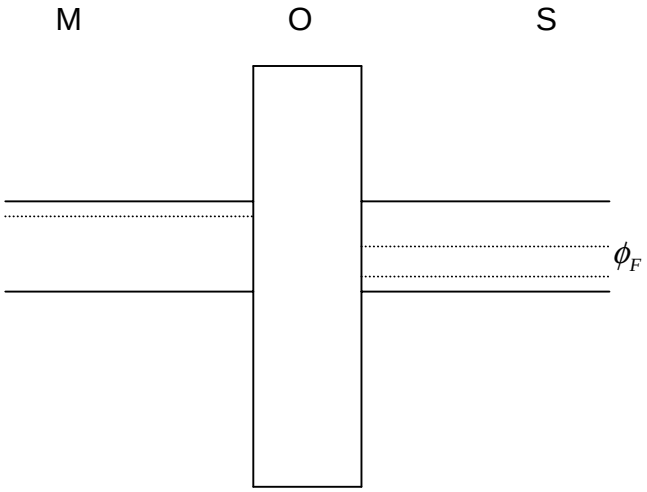
It is straightforward to see that

$$V_g = \psi_{ox} + \psi_s + \phi_{ms} \tag{A.8}$$

We also need to keep charge balance in the MOS system:

$$Q_G + Q_i + Q_b + Q_o = 0 \tag{A.9}$$

where Q_G is the charge on the gate, Q_i is the inversion charge, Q_b is the depletion charge and Q_o is the effective interface charge. Figure A.1 illustrates the band diagrams of a n^+-polysilicon/p-type MOS capacitor biased at different gate voltages.

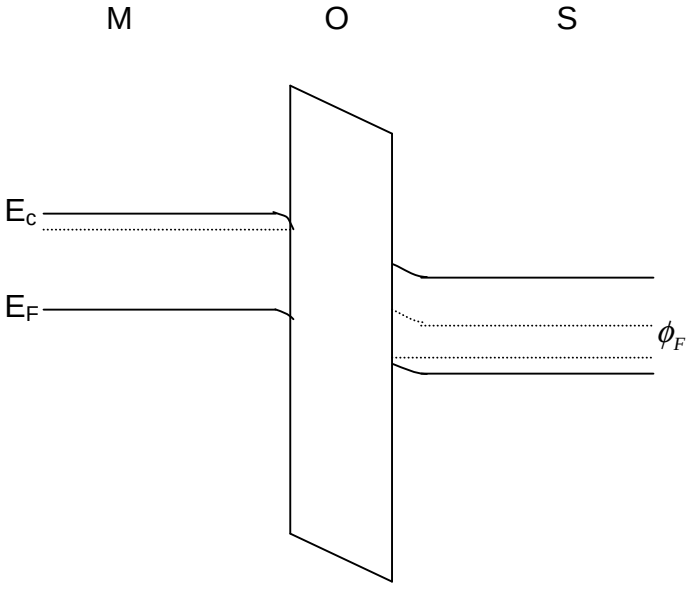


Flatband: Vg < 0
$Q_d = Q_I = 0$

$V_g = \phi_{ms}$

$\psi_{ox} = \psi_s = 0$

(a)

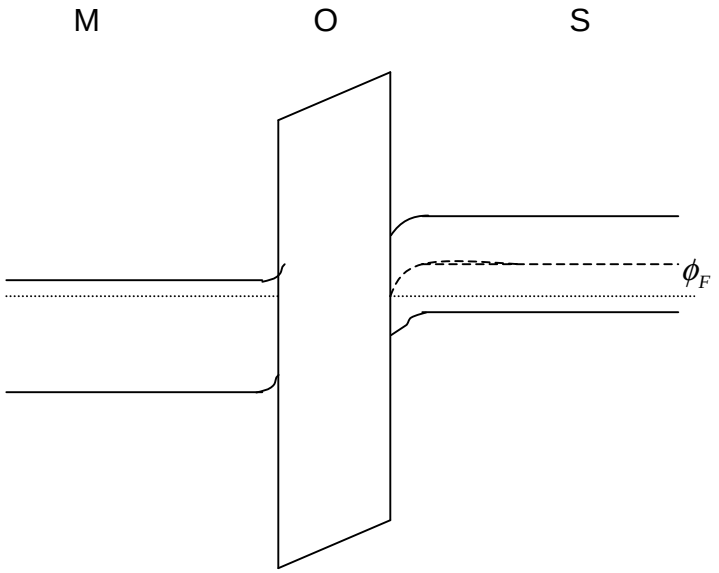


Accumulation: Vg < 0

$V_g = \psi_{ox} + \psi_s + \phi_{ms}$

$\psi_s < 0$

(b)

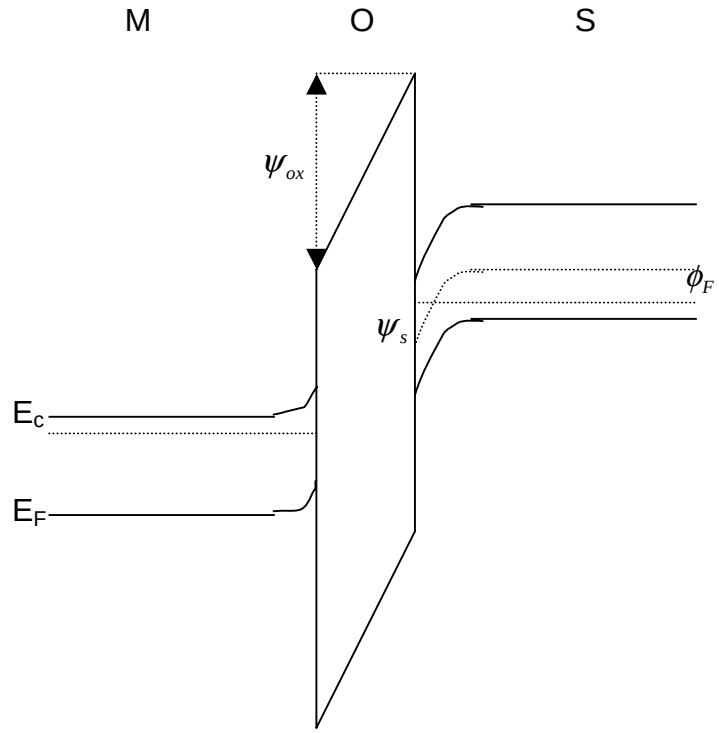


Depletion: Vt > Vg > 0

$V_g = \psi_{ox} + \psi_s + \phi_{ms}$

ψ_s >0

(c)



Onset of strong inversion:

$V_g = V_t$ $Q_I = 0$

$\psi_s = 2\phi_F$

$V_g = \psi_{ox} + 2\phi_F + \phi_{ms}$

(d)

Figure A.1 Energy-band diagrams of a MOS structure in (a) flatband, (b) accumulation, (c) depletion, and (d) onset of strong inversion.

A.3 MOS Field-effect Transistor

Characteristics in the Subthreshold Region

Below the threshold voltage, the drain current on a logarithmic scale is nonnegligible because the mobile carrier density in the channel is not zero when $V_g < V_t$. Instead, the inversion charge is an exponential function of (ψ, V_g).

$$Q_i = -q\int n dy \qquad \text{where } n = \frac{n_i^2}{N_a}\exp\left(\frac{q(\psi - V_g)}{kT}\right) \tag{A.10}$$

where ψ is defined as in Section A.1. In the subthreshold region, the normal electrical field is very small and the mobile carriers are not fully sweepted to the drain end. This creates a concentration gradient between the source and drain. Therefore, subthreshold conduction is dominated by the diffusion current, which can be written as follows:

$$I_{ds} = \frac{W}{L} I_M^{'} e^{(V_{gs}-V_M)/(n\phi_t)}\left(1 - e^{-V_{ds}/\phi_t}\right) \tag{A.11}$$

where V_M is the upper limit of weak inversion in terms of V_{gs}; I_M' and n are defined in [1].

The onset of pinch-off and current saturation

The MOSFETs are operated as a closed switch when $V_g > V_t$ and $V_{ds} < V_{dsat}$. The vertical electric field from V_g attracts the electrons in the inversion channel layer; the laternal electrical field due to V_{ds} rolls the channel electrons into the drain region. As the drain voltage increases (for a constant V_g), the drain current increases, but the inversion charge at the drain end decreases and eventually it goes to zero when $V_{ds} = V_{dsat}$. In this case, the drain current reaches a maximum value, and the surface channel is pinched off at the drain region of the inversion channel when saturation takes place. Beyond V_{dsat}, the drain current keeps constant at I_{dsat}, independent of V_{ds}. The voltage across the surface depletion region is V_d-V_{dsat}, while the voltage drop across the inversion channel is fixed to V_{dsat}. The concepts of MOSFETs in the case of pinch-off region is summarized as following:

1. The MOSFET operates as a gate voltage-controlled current device.
2. The depletion region has little influence on the drain current.
3. The drain current is controlled by the number of electrons at the edge of the depletion region.
4. The drain current is controlled by the number of the electrons in the channel, which is determined by V_g and is independent of V_d.

Characteristics in the Saturation Region

As low V_{ds}, I_{ds} increases following a parabolic curve until a maximum current is reached. The drain current can be approximated by

$$I_{ds} = \frac{W}{L}\mu_{eff}C_{ox}\left((V_g - V_t)V_{ds} - \frac{1+\delta}{2}V_{ds}^2\right) \qquad V_{ds} < V_{dsat} \tag{A.12}$$

$$I_{ds} = \frac{W}{L}\mu_{eff}C_{ox}\frac{(V_g - V_t)}{2(1+\delta)} \qquad V_{ds} \geq V_{dsat} \tag{A.13}$$

where δ will change with V_{ds}, V_{CB}, and surface potential.

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APPENDIX B

Tunneling Currents and Trap Generation in Gate Oxides

This appendix discusses two main gate current flow mechanisms in the MOS devices under different gate electric fields. The conduction mechanisms correlated with trap generation and trap-assisted tunneling processes are also illustrated.

B.1 Tunneling into and through silicon dioxide

When a large positive bias is applied to the gate electrode, electrons in the strongly inverted substrate surface can tunnel into the conduction band of the oxide layer and hence give rise to a Fowler-Nordheim (FN) tunneling as shown in Figure B.1(a). The FN tunneling current (I_{FN}) is given below [1]

$$I_{FN} = \frac{A_G q^3 E_{ox}^2}{16\pi\eta\phi_{ox}} \exp\left(\frac{-4\sqrt{2m^*}\phi_{ox}^{3/2}}{3\eta q E_{ox}}\right) \qquad \text{(B.1)}$$

where A_G is the gate area, η is the reduced Planck's constant, ϕ_{ox} denotes the Si/SiO_2 interface energy barrier for electrons, m^* is the effective mass of electron in the gate dielectric and E_{ox} (V/cm) is the electric field across the oxide. The effects of finite temperature and image-force barrier lowering are ignored in the above equation.

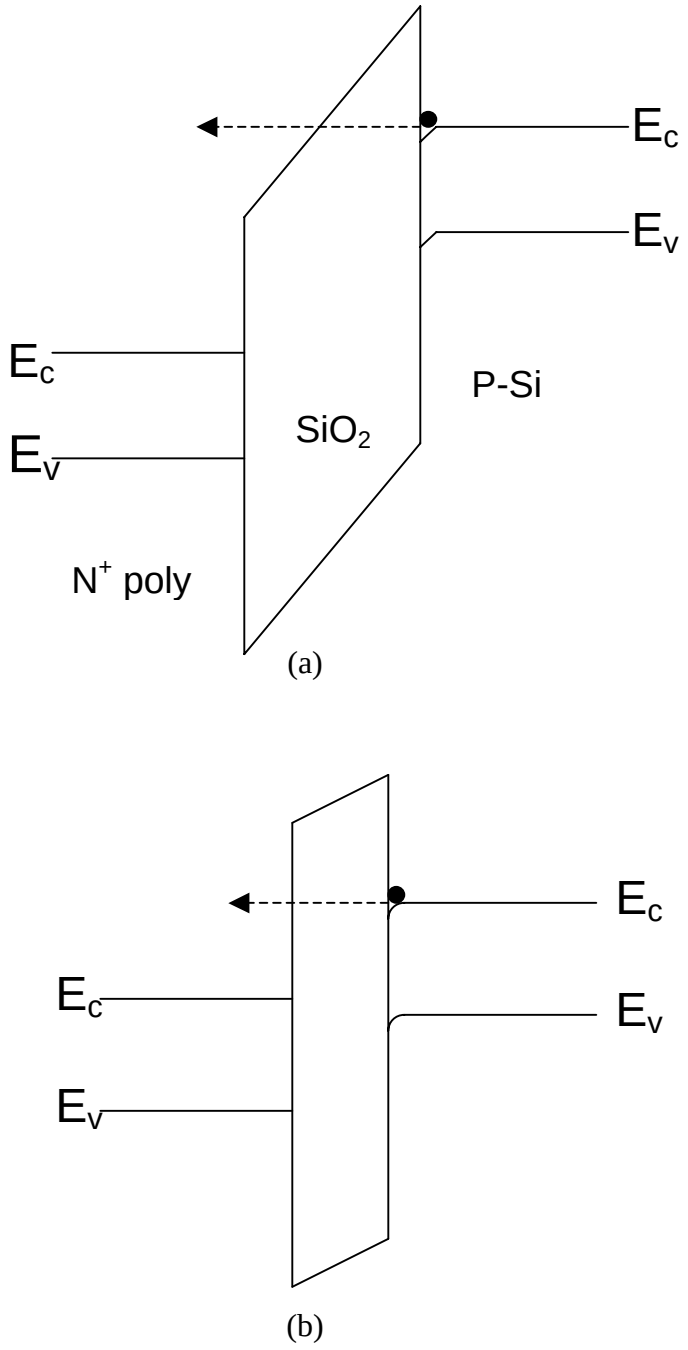

Figure B.1 Tunneling effects in an MOS capacitor structure: (a) Fowler-Nordheim tunneling ($V_{ox} > q\chi$), and (b) direct tunneling ($V_{ox} < q\chi$).

If the oxide thickness is less than 4 nm, electrons from the inverted silicon surface can directly tunnel through the forbidden energy gap of the SiO_2 layer, as is illustrated in Figure B.1(b). As the gate oxide thickness scaled down to 2-3 nm, direct tunneling current (I_{dir}) becomes dominant in MOSFETs. The current I_{dir} can be given by the expression

$$I_{dir} = A_G A E_{ox}^2 \exp\left(\frac{-B\left[1-\left(1-qV_{ox}/\phi_{ox}\right)^{3/2}\right]}{E_{ox}}\right) \qquad \text{(B.2)}$$

With E_{ox} in units of V/cm, A and B are given by [2]

$$A = 1.54x10^{-6}\,\frac{(m/m_{ox})}{\phi_B}\left[\frac{A}{V^2}\right] \qquad \text{(B.3)}$$

$$B = 6.83x10^{7}\sqrt{\frac{m_{ox}\phi_B}{m}}\phi_B\left[\frac{V}{cm}\right] \qquad \text{(B.4)}$$

It has been shown that oxide breakdown occurs at the local weak spots of the oxide [3]. Thus, carrier trapping in the oxide can cause small changes in the oxide field, leading to significant changes in the tunneling current, as can be seen from Equations (B.1) and (B.2).

B.2 Damage and trap generation caused by tunneling electrons

During high field stressing (FN stressing), damage is created at the SiO_2 conduction band due to the generation of traps. This is because electrons gain sufficient kinetic energy and then interact with atoms in the oxide [4, 5]. In other words, the injected electrons travel non-ballistically through the oxide as is schematically illustrated in Figure B.2(a). For the oxides between 3.5-5 nm, the injected electrons transport ballistically without colliding with SiO_2 lattice (not shown) [5]. As can be seen in Figure B.1(b), these generated traps then serve as intermediate tunneling sites, which enhance leakage current, i.e., trap-assisted tunneling [6], even at low-moderate oxide fields.

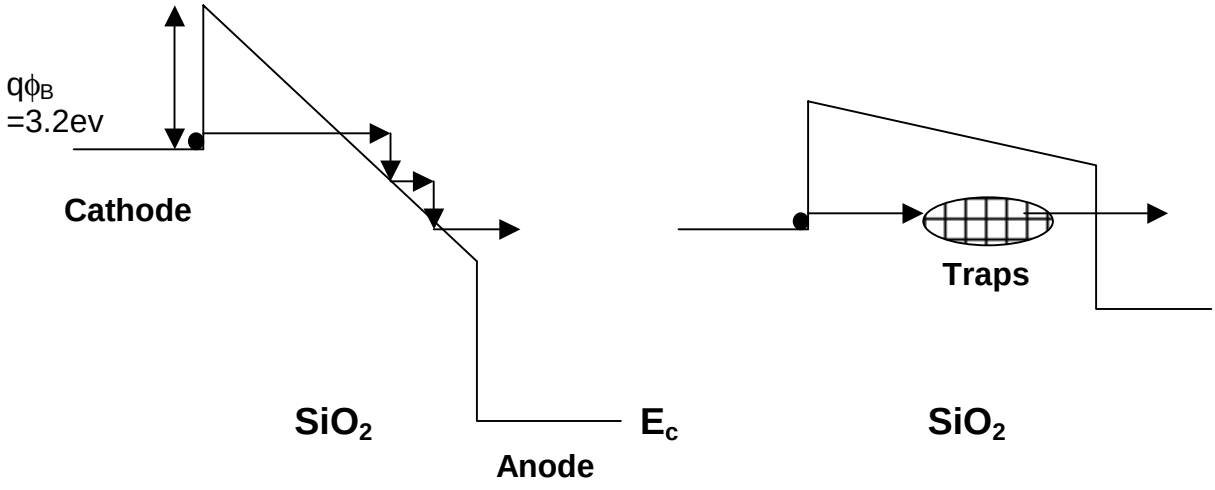

Figure B.2 Schematic of trap generation and conduction mechanism under (a) FN stressing (b) low (or moderate)-field stressing.

B.3 Effect of trapped charges on the tunneling current

Figure B.3 illustrates the barrier distortion which reflects the creation of negative and positive charges on the tunneling current through the SiO_2 [6]. The presence of positive charges will lower the SiO_2 barrier [7] and increase leakage current [7, 8]. In other words, the trapped holes enhance the electric field near the cathode, and decrease the electric field near the anode.

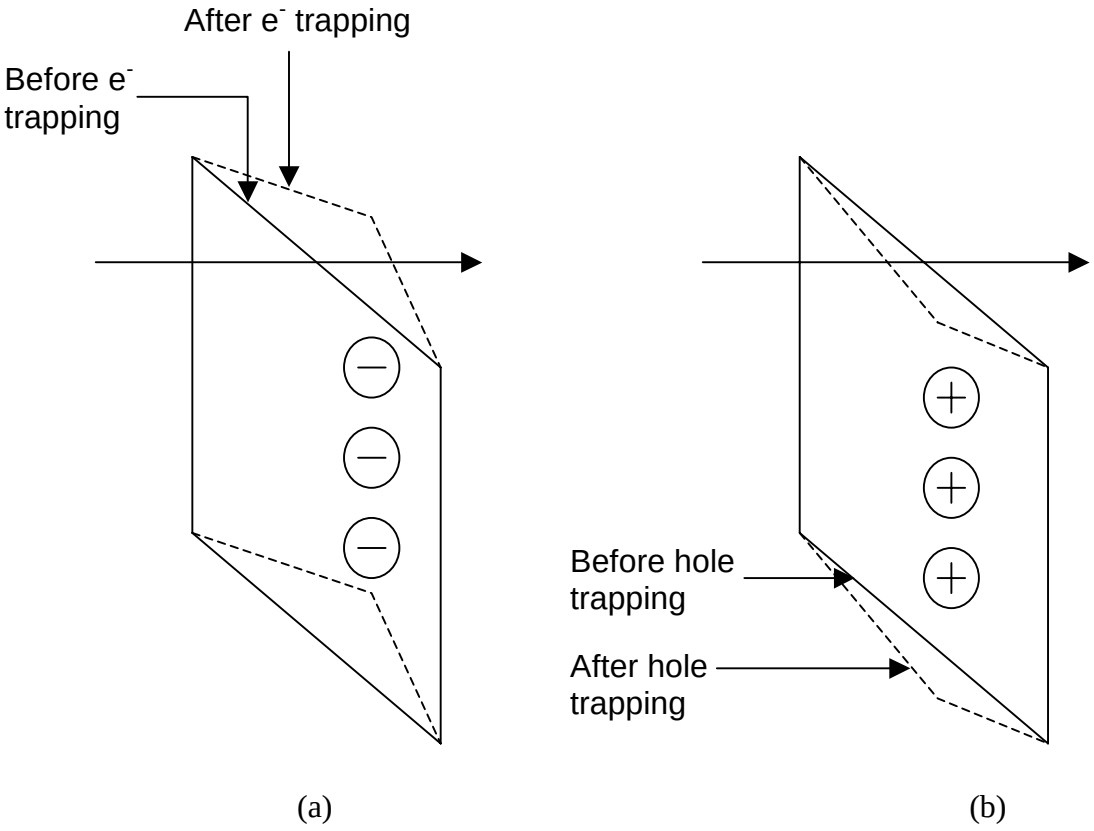

Figure B.3 Schematic diagram showing the trapping of (a) electrons and (b) holes in the SiO_2 layer.

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APPENDIX C

Oxide Breakdown Mechanisms and Breakdown Accelerated Models

During the oxide degradation and breakdown, there are electron and hole traps generated in the oxide layer. These traps can cause an impact on the tunneling current as discussed in Appendix B. We will review three oxide breakdown mechanisms, which were proposed by Stathis et al. [1], and their correlations with different breakdown accelerated models will be discussed as well.

C.1 Trap generation model

As discussed in Section 1.1.1, trap generation at the Si/SiO_2 interface is a random process and can result in a large impact on the performance and reliability of MOS devices due to the instabilities in both threshold voltage and flatband voltage. For ultrathin oxides, the driving force for defect creation has been shown to be the applied gate voltage [2]. Several groups [1, 3, 4] have proposed a trap generation model to evaluate the defect generation rate from the SILC during the oxide breakdown. As discussed in Section 5.3, the defect generation rate exhibits an exponential function of gate voltages, implying that it is electron energy which dominates defect generation and oxide breakdown [1]. It has been shown that trap generation will enhance SILC by a trap-assisted conduction mechanism [5, 6], as illustrated in Appendix B.2. Figure C.1 shows the formation of a conductive channel due to the trap generation and propagation between interface A and interface B. On

the other hand, the generation of new defects would depend on the local field produced by the neighboring defects, leading to a highly directed paths at high voltages [7, 8]. This percolation model has been widely used to illustrate the SBD and HBD phenomena.

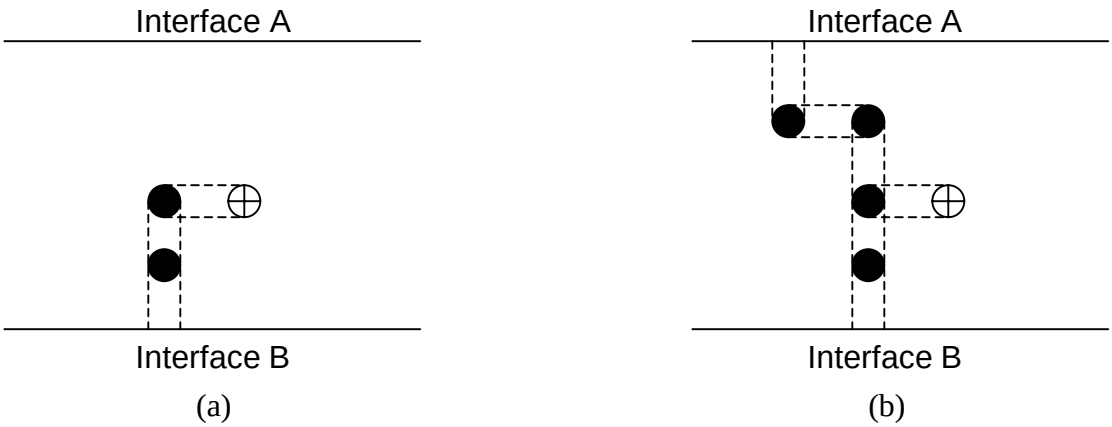

Figure C.1 Percolation model showing (a) SBD and (b) HBD due to the partial and complete formation of conduction channel between two interfaces, respectively. “Defects” are represented by filled circles; open circle represents the final breakdown spot.

C.2 Anode hole injection (1/E model)

During the stress, the injected electrons lose their energy at the anode interface and create electron-hole pairs. Then the valence-band electrons gain sufficient energy and are excited to the lowest available states, i.e., the bottom of anode conduction band, thereby creating hot holes. Some of these hot holes can tunnel back to the

cathode interface under the influence of the oxide field, leading to oxide degradation and structural breakdown [9-12]. With this model, time-to-breakdown (t_{BD}) can be predicted by the following expression

$$t_{BD} = \tau_0 \exp\left(\frac{G}{E_{ox}}\right) \tag{C.1}$$

where τ_0 is a constant, and the values of G vary from 290 to 390 MV/cm [13, 14], depending on stress type (CCS or CVS) and oxide thickness [13]. No temperature dependence of the G value was reported [14].

C.3 Thermo-chemical (E) model

The E model is developed based on the thermo-chemical model, which describes the dipole field interaction due to oxygen vacancy defects [15]. The E model predicts a linear relationship between the logarithm of t_{BD} and the oxide field:

$$t_{BD} = t_0 \exp(-\gamma E_{ox}) \tag{C.2}$$

where t_0 and γ are constants. Also, a unified model with approximate E dependence at low voltage and 1/E dependence at high voltage is developed [16-18].

The E versus 1/E model is mainly discussed in thicker oxide regiem (> 5 nm). For ultrathin oxides, the injected electrons transport ballistically through the oxide, thus electron energy at the anode determined by the applied voltage V_g becomes dominant and directly related to the oxide degradation. In other words, oxide breakdown and reliability projection is more accurate by using a voltage-driven model rather than a field-driven model [2]; therefore, CCS is usually replaced by CVS for an ultrathin gate oxide.

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