ABSTRACT

PITTS, WALLACE SHEPHERD. Partially Depleted Silicon on Insulator Phase Lock Loop. (Under the direction of Dr. Paul D. Franzon)

A 435-MHz, Digital Low-IF (1-MHz), Double Differential Phase Shift Keying (DDPSK) Transceiver circuit for space application was the motivation for engineering our low power Quadurature Phase Lock Loop (PLL). The PLL was designed to meet specifications set forth by NASA and JPL. In this thesis, you will gain knowledge of the implemented design, transistor sizes, the layout as a whole, and the calculations used for the system design. The design consists of two cross-coupled NMOS and PMOS pair analog Voltage Controlled Oscillators with a digital feed back loop.

Partially Depleted Silicon on Insulator Phase Lock Loop

By

Wallace Shepherd Pitts

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APPROVED BY:

PAUL D FRANZON
Chair of Advisor Committee

KEVIN GARD

GRIFF BILBRO

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DEDICATION

To my Parents, Wallace and Cathy Pitts, my Grandmother, Catherine Shepherd, my Aunts, Barbra Shepherd and Emily Glaser, my uncle, Wolfram Glaser, and my friends, especially Arianne Tanton, for their support in my endeavors.

BIOGRAPHY

Wallace Shepherd Pitts was born in Raleigh, North Carolina. He received a B.S. in Computer Engineering and a B.S. in Electrical Engineering from North Carolina State University, Raleigh in 2004, and is currently a M.S. candidate in Electrical Engineering at North Carolina State University, Raleigh. In summer of 2001, he was in the employment of Ericsson, in Research Triangle Park, as a summer intern. From 2002 to 2004, he worked as both an intern and a part time employee for Honeywell in Rocky Mount, North Carolina. His research interests include mixed signal circuit design for communication systems, low power systems, extreme environment systems, as well as the budding field of nanotechnology.

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Secondly, I would like to thank Dr. Gard for his constant patience and ability to steal five minutes of his time, even when he really knows that it means fifteen to thirty minutes. He has been a great wealth of knowledge for the tools and subject material for the chip design. I look forward to working on my Ph. D. research with Dr. Gard.

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Chapter 1 Introduction

1.1 Motivation

When designing a circuit for space application, or any mobile communications circuit for that matter, the primary benchmark is power consumption. The more power a circuit consumes, the less work can be done by other circuits that share the same platform. This will result in either larger solar cell arrays or larger batteries, and thus fewer sensors can be included in the same amount of payload.

Silicon on Insulator (SOI) devices are known for their low power nature, reduced substrate noise and decreased parasitic capacitances. The low power nature is due to the fact that there is a thin device layer, which is fabricated on top of an insulator that in turn is on top of a substrate, as shown in Figure 1.1. An intrinsic property of SOI, due to the fabrication processes, is its ability to isolate the individual devices' "bulk" connection (i.e. the fourth terminal), as shown in Figure 1.2. This yields the ability to create devices free from coupling noise through the substrate from other circuits sharing the chip. SOI chips are also intrinsically radiation hardened (Radhard), due to the fact radiation has less area to cause a voltage upset on the devices' smaller bulk. Another intrinsic property of SOI, is that by creating the source and drain junctions directly on the Substrate Insulator, the junction capacitance of the device is reduced which enables a speed advantage over traditional substrate technology. In addition to increased speed, the smaller capacitance transistors do not require as much power to switch the transistors. These advantages are crucial in designing an adequate circuit that meets the goals of the design specifications.

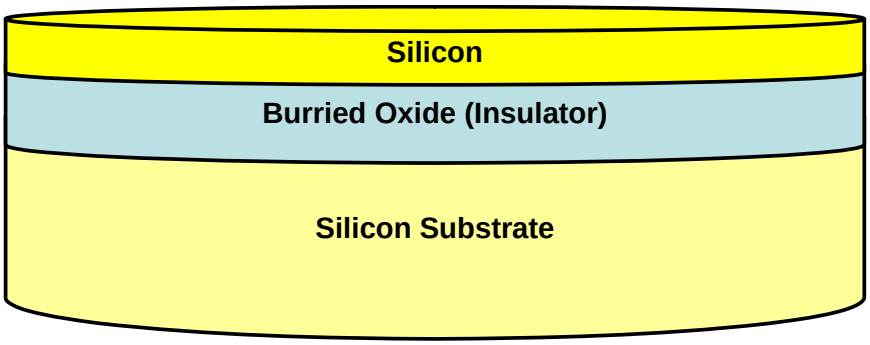


Figure 1.1: Cross section of a partially depleted SOI Substrate

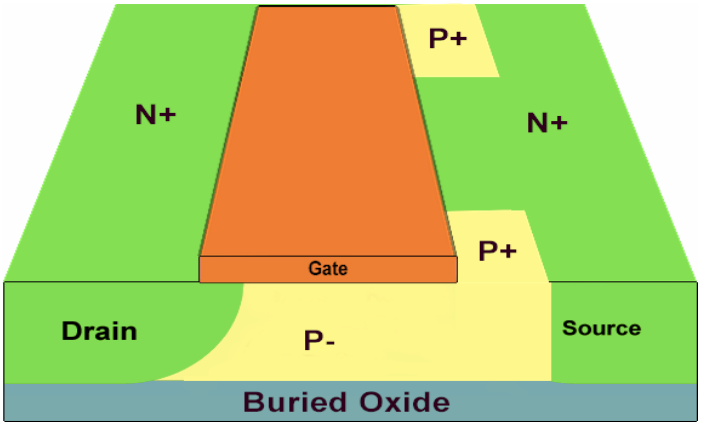


Figure 1.2: Cross Section of a partially depleted SOI device [1]

These design constraints are implemented in a low power integrated System on Chip (SOC). The research focused on the design of a subsystem of the SOC, the Phase Lock Loop (PLL) block that will generate the carrier frequency of 435 MHz, which is outlined in the design specifications. The PLL is designed in such a way, that no matter what the process variation of the chip foundry, or from the dynamic environment conditions, the desired carrier frequency will be reproduced faithfully.

PLL blocks are implemented in many of today's communication electronics, such as cordless phones, cell phones, radio's, etc. However, most of these electronics operate within a mild environment and are easily serviceable; unlike deep space. The short comings of the deep space environment force the design to be low power for long battery life, radiation hardened for operation in another atmosphere, and the ability to integrate

designs onto a single chip for size and signal integrity issues. The answer to this problem is to design and fabricate the device using a SOI process; more specifically in our case, the Partially Depleted SOI.

1.2 Acronyms

SOC – System on a Chip

SOI – Silicon on Insulator

PDSOI – Partially Depleted Silicon on Insulator

PLL – Phase Lock Loop

PFD – Phase Frequency Detector

VCO – Voltage Controlled Oscillator

DIV128 – 128 bit divider

DFF – Digital Flip Flop

Q – Quality Factor

DDPSK - Double Differential Phase Shift Keying

JPL - Jet Propulsion Laboratory

NASA - National Aeronautics and Space Administration

IPN - Inter Planetary Network

CAD - Computer Aided Design

ADS - Analog Design Suite

LVS - Layout Verses Schematic

Radhard - Radiation hardened

Chapter 2 Literature Review

Since there had been a previous fabrication run that tested individual components,there was the luxury of learning about areas to improve by discussing the PLL with the previous designer, Jeff Marks. During this discussion, he suggested several areas that he would have designed differently with the experience he has gained in industry. The discussion suggested to redesign/design:

- Prescaler
- Charge Pump
- Buffers & Common mode Voltage Isolation

In his opinion, when the VCO was at the maximum frequency, the Prescaler was being over run (i.e. could not count all the signal periods). The Prescaler was thus revisited and it was decided to implement the design from Chapter 3.3 . The previous design that was implemented was a ripple carry counter, Figure 3.6. The design in the literature was chosen because it was an asynchronous divide by 4/5, followed by a divide by 16/32 which yields a low critical delay and thus higher operating frequencies [6]. It was further discussed to increase the operating speed of the Prescaler by implementing a fast cross coupled divide by 2[5] circuit and reduce the divider circuit to divide by 64.

The Charge Pump was also reconstructed, Chapter 3.5 . It was discussed that they are probably better, more symmetric, and more error tolerant topologies. In another discussion on the design with one of my colleagues, Dr. Lei Luo, he suggested one of the circuits that he had fabricated and tested [8]. The advantage of Dr. Luo's design is that it uses NMOS switches as the up and down transistors instead of PMOS and NMOS. The

design was later improved upon by implementing circuitry that reduced the switching noise of the Up and Down transistors, Figure 3.27.

Designing buffers can be very critical, especially when working with analog circuits. A common mode offset can be the difference between a working buffer and a non- working buffer. Implementing common mode isolation is a very rudimentary task and it can, in fact, save your design incase of a short. After discussions with Dr. Luo, also covered in his design notes [10], the power tradeoffs and architectures of the design were discussed. He suggested that instead of using PMOS loads on the buffers, that it would be more practical to implement them as resistors; even though Resistive loads are susceptible to process variations. Optimizing the design for low power can be considered an art form. You want to design the buffer to meet swing performance (with a reasonable safety margin), while still meeting low power constraints. The signal swing is directly proportional to the resistive load size and tail current. An unavoidable drawback of analog buffer designs is that they constantly consume a static power.

Chapter 3 Architecture and Design

3.1 System on Chip Overview

A 435-MHz, Digital Low-IF (1-MHz), Double Differential Phase Shift Keying Transceiver, as shown in Figure 3.1, circuit for space application was the motivation for engineering our low power Quadurature PLL. The Transceiver chip was designed to be a low power front- end block for future Mars missions sponsored by NASA and JPL. Detailed specifications can be found in the NASA and JPL IPN Progress Report [2]. Figure 3.2 illustrates the type communications link proposed, and Figure 3.3 shows the final SOC layout.

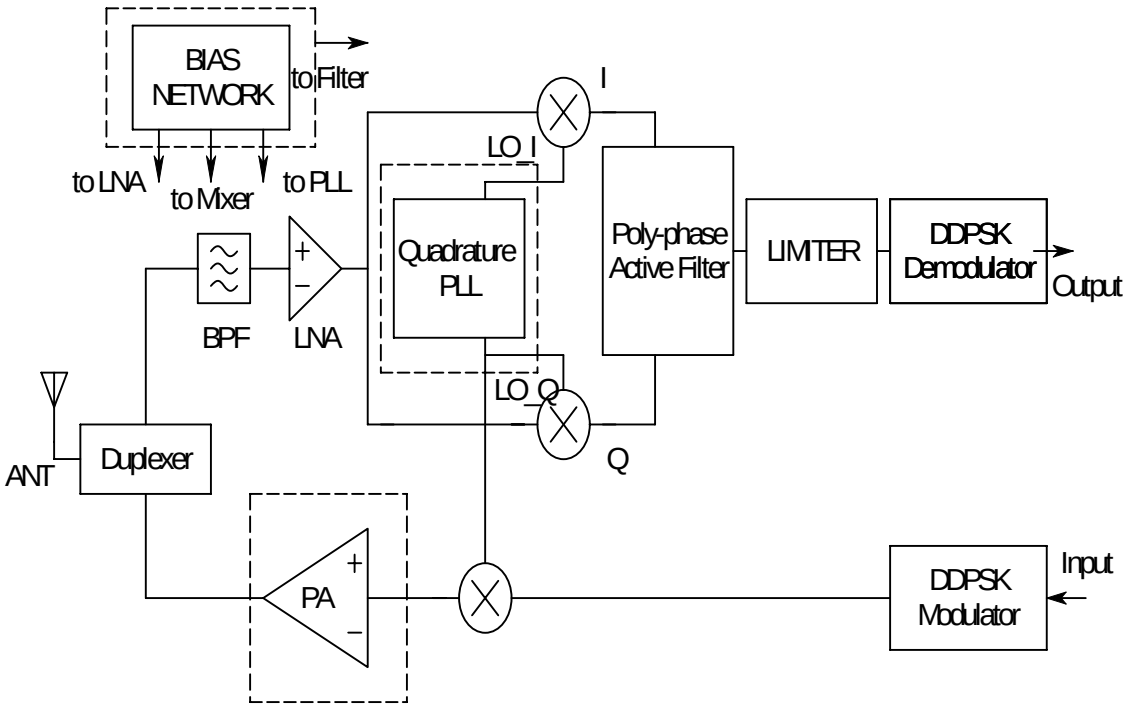


Figure 3.1: Block diagram of 435-MHz Digital Low-IF (1-MHz), DDPSK (Double Differential Phase Shift Keying) Transceiver [3]

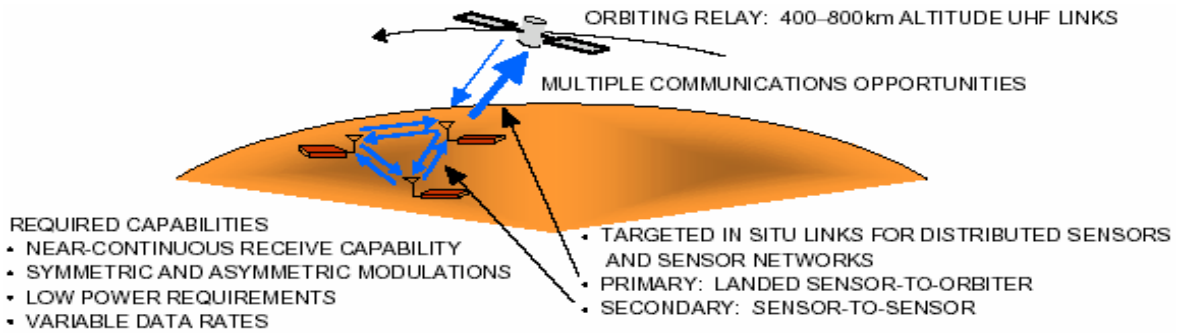


Figure 3.2: Communication links between Martian orbiter and landers [3]

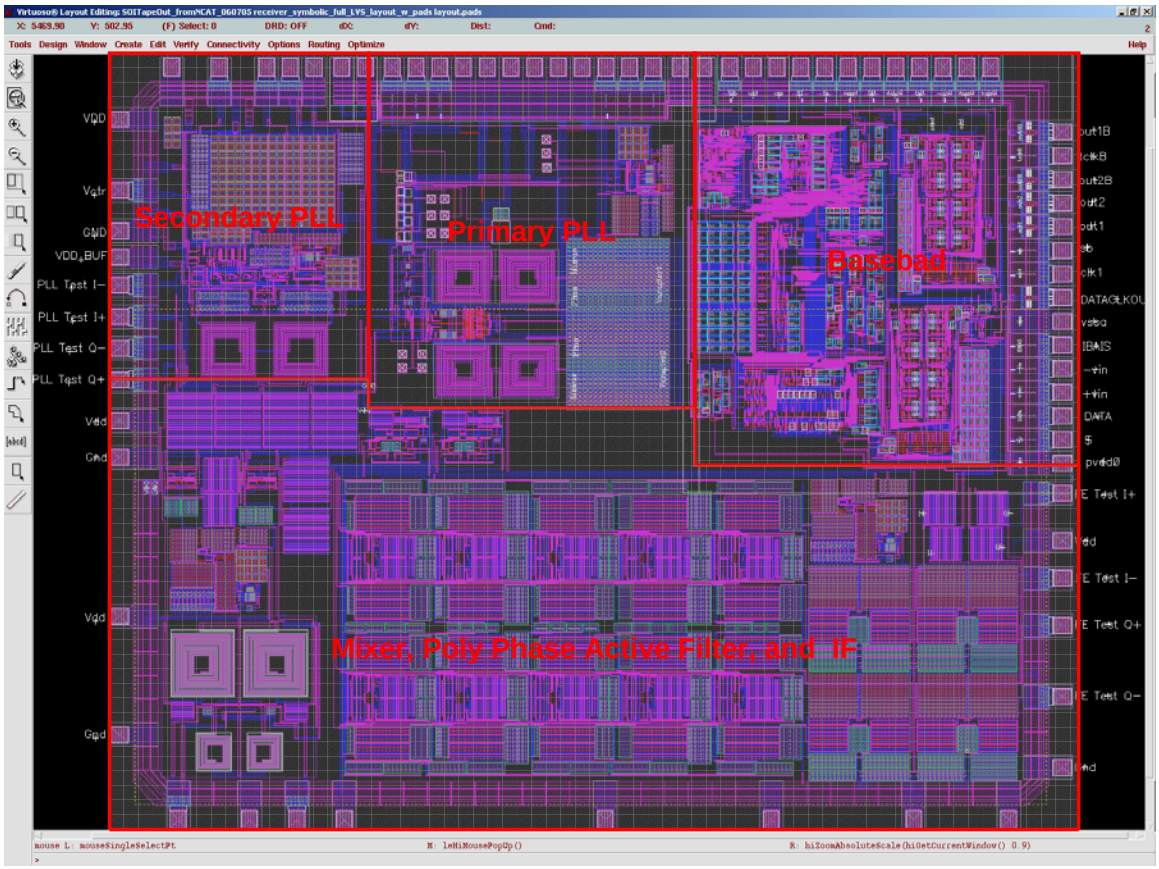


Figure 3.3: -MHz, Digital Low-IF (1-MHz), Double Differential Phase Shift Keying (DDPSK) Transceiver

3.2 Phase Lock Loop

3.2.1 Typical Phase Lock Loop

The essential building blocks of a PLL are a VCO, PFD, Charge Pump, and Loop Filter as shown in Figure 3.4. The purpose of the PLL is to take an adjustable high frequency signal and compare it to a several orders of magnitude lower benchmark frequency (typically a crystal). First, the high frequency signal is divided into a lower frequency. Next, the divided signal is compared in both phase and frequency to the benchmark frequency. Finally, the phase and frequency of the divided high frequency signal are adjusted to match the benchmark's phase and frequency.

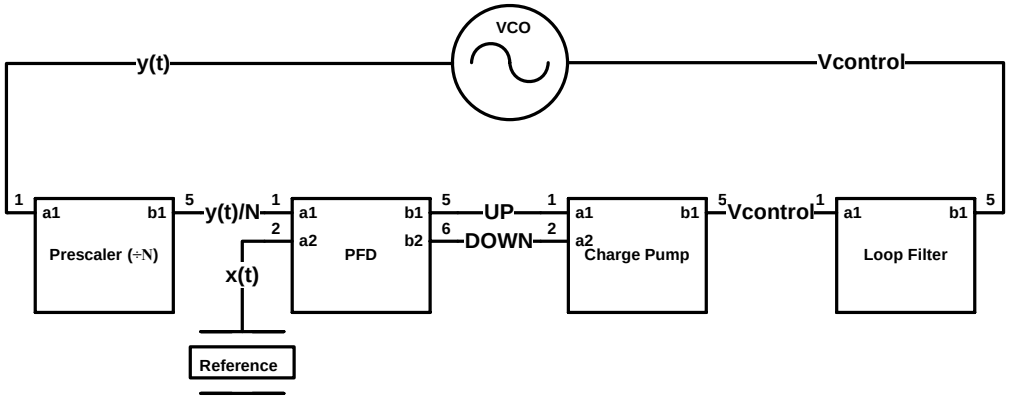


Figure 3.4: Combined Phase Frequency Detection PLL [7]

The reason this is done is to ensure a process and environment invariant design. When fabricating and mass producing designs, there is always variation from the engineers CAD transistor sizing and lumped element final values. The reason for this is outside of the scope of this paper. When the PLL is appropriately designed, it can be certain that both receivers' and transmitters' radios will have the same carrier frequency, thus ensuring a proper communication link.

3.2.2 Implemented Phase Lock Loop

Designing circuits falls under one of three categories:

1. Theoretical design
2. Schematic design and simulation
3. Parasitic extracted simulation

The theoretical design was first evaluated using the Cadence ADS. Once the typical design parameters for the Loop filter, Charge pump, and divider circuit were identified, they were then passed into Cadence Front to Back Designer, where parts of the system were implemented using Verilog and VerilogA models.

Once the system was tested and deemed to be working properly, the Schematic Design and Simulation took place. Each block that was modeled in Verilog/VerilogA was then redesigned in a Schematic block and tested independently. Next, each of the new Schematic blocks replaced the Verilog/VerilogA model blocks, and the system was then reevaluated to ensure proper operation. The parasitic extracted stages that the PLL circuit would be driving were then attached to load the PLL as shown in Figure 3.5; this helps to ensure that the circuit will be robust enough to perform even when the circuit is fully loaded.

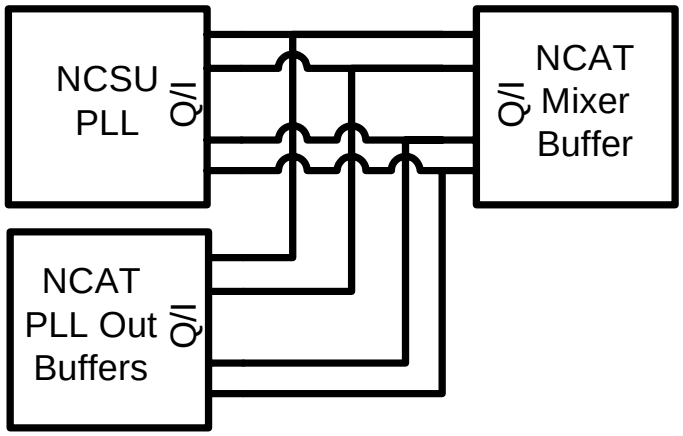


Figure 3.5: NCSU PLL driving NCAT Output Buffers and NCAT Mixer Buffers

After the Schematic simulations performed successfully, this would sometimes take several iterations of simulation and then adjusting transistor sizes to resolve performance issues, the individual blocks were then laid out in sub-blocks. Sub-blocks are a group of transistors that make up a piece of a larger block (i.e. the divide by 128 had a DFF, AND gate, etc sub-blocks). The circuit was then extracted, LVS checked, re-extracted with parasitic capacitances and resistances, and then re-simulated. Several iterations of this could be necessary to ensure correct performance.

Each sub-block was then laid out and extracted with parasitic capacitances and resistances. They were then verified on the stand- alone test bench using the hierarchy editor to use the extracted components instead of the schematics. Several iterations of circuit fine- tuning could again be necessary to ensure proper performance because of the added parasitic capacitances and resistances. Finally, the PLL design as a whole was combined in layout, extracted, LVS checked, re-extracted with parasitic capacitances and resistances and simulated. Once this stage is reached, the circuit it may be necessary to tweak and then iterate the method on each of the sub-blocks to ensure proper performance of the circuits, such as tweaking tail current transistors or the varactor, to ensure that the designed frequency is achieved in the middle of the tuning range, of the VCO. By locating the designed 435MHz frequency at the center of the circuit's voltage tuning range it helps to ensure that the PLL will indeed lock over process variation. After the design was validated at the typical NMOS and PMOS process model parameters, the design was then tested at the midpoints of the process models to ensure validity over process variation.

3.3 128-bit Divider

3.3.1 Frequency Divider circuits

Digital Frequency divider circuits are pretty straight- forward; it is a counter. As the name implies, they are used to reduce a higher frequency to a lower frequency. Frequency divider circuits can be visualized in both Analog and Digital methods. However, in this case a Digital Frequency Divider was decided upon because of its simplicity and integration with a combined PFD. The PFD is discussed in further detail in 3.4 .

The equation for determining the divider size is Equation 3.1.

$$N = \frac{Frequency_reference}{Frequency_VCO}$$

Equation 3.1

There are also quarter bit dividers that give the ability to divide even more accurately than traditional N-Bit Dividers. However, for this project the time limitation halted exploration of these dividers.

3.3.2 Fast divide by 2

In redesigning the PLL from the previous fabrication, it was suggested by the previous designer that the prescaler, Figure 3.6, circuit might be to slow for the VCO when it railed high. It was decided that the speed of the divider needed to be increased as a safety measure. To increase the speed of a larger divider; a faster and typically more power hungry divide by 2 circuit was implemented before a smaller redesigned divider circuit. In essence, a divide by 128 circuit is broken into a fast divide by 2 circuit in series with a normal divide by 64 circuit. For this design, a cross coupled pair of modified Tim Erlenmeyer DFF's [4] were used; Figure 3.7, Figure 3.8, Figure 3.9,and Table 3.1. The

design was improved, so that instead of a Dynamic DFF it would have a fast, strong, balanced, and static operation of both Q and Qbar.

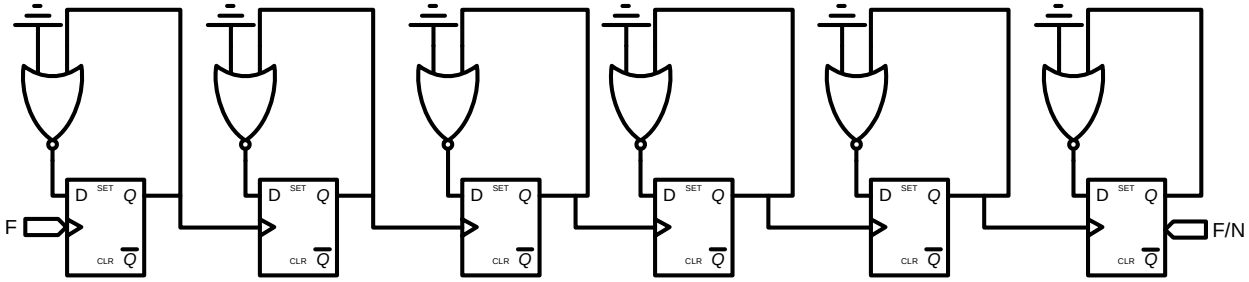


Figure 3.6: Previous implemented divider

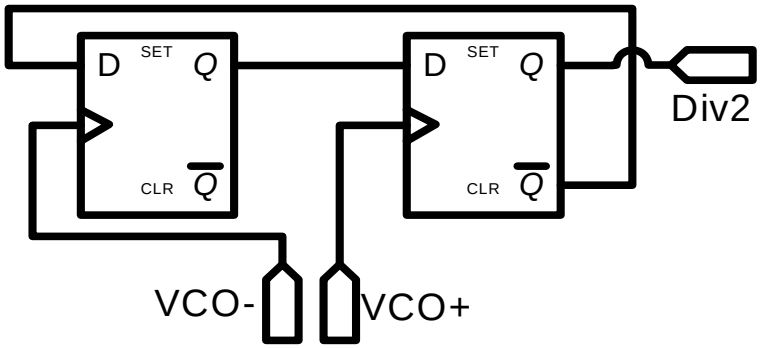


Figure 3.7: Fast Divide by 2 Block Diagram [5]

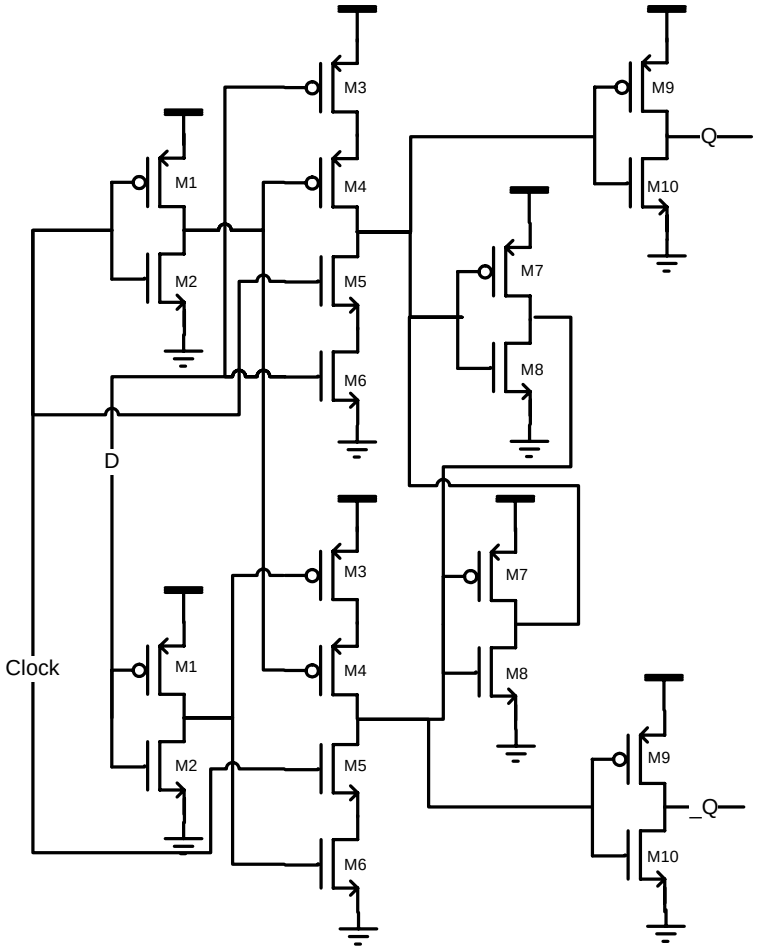


Figure 3.8: Fast Divide by 2 DFF Schematic[4]

Table 3.1: Fast Divide by 2 DFF

Transistor	W(μm)	L(μm)	m	f
M1	3.6	.5	1	1
M2	1.2	.5	1	1
M3	3.6	.5	1	1
M4	3.6	.5	1	1
M5	2.3	.5	1	1
M6	2.3	.5	1	1
M7	1.2	.5	1	1
M8	2	.5	1	1
M9	5	.5	1	1
M10	2.5	.5	1	1

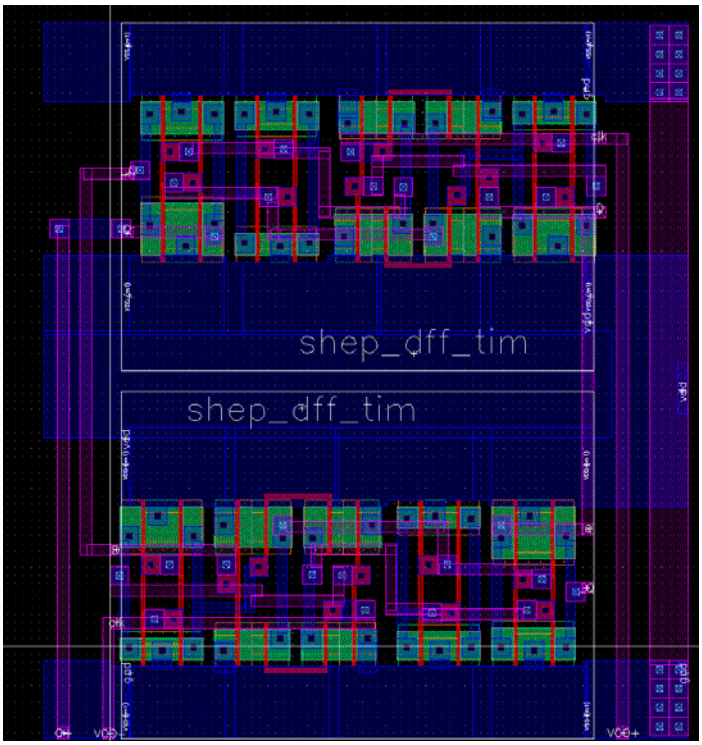


Figure 3.9: Fast Divide by 2 Layout

3.3.3 Divide by 64

Digital frequency dividers are common, and generally not the bottle design neck of a PLL. A divide by 128/129, Figure 3.10 [6], circuit was reduced into a divide by 64; Figure 3.11, Figure 3.12, Figure 3.13, Figure 3.14, Figure 3.15, Figure 3.16,

Table 3.2, Table 3.3, Table 3.4, and Table 3.5. This enabled the use of the fast divide by 2, Figure 3.7, in conjunction with the divide by 64 circuit as discussed in Chapter 3.3.2 .

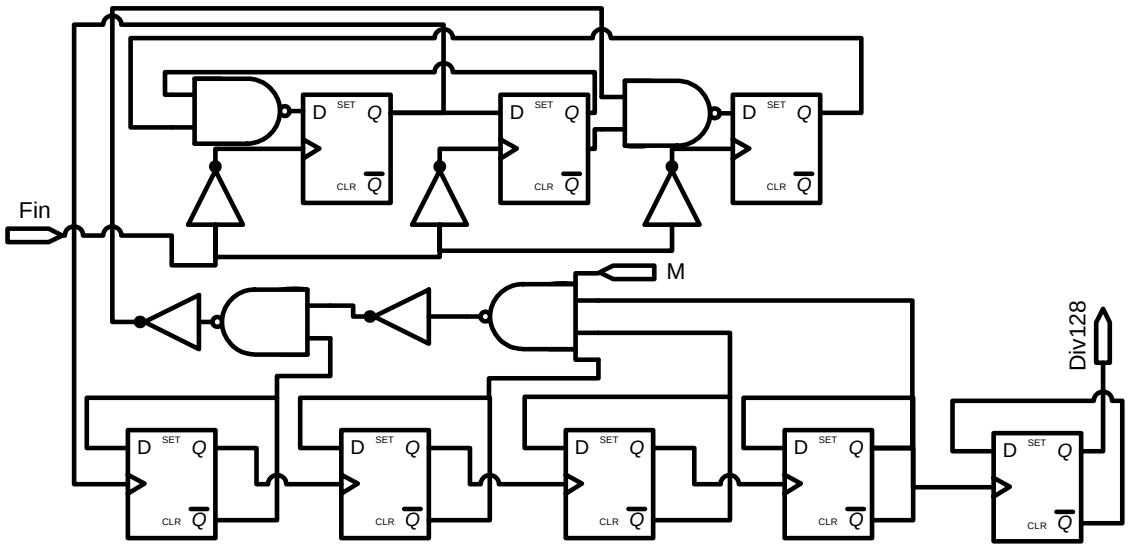


Figure 3.10: Divide 128/129 Prescaler Block Diagram [6]

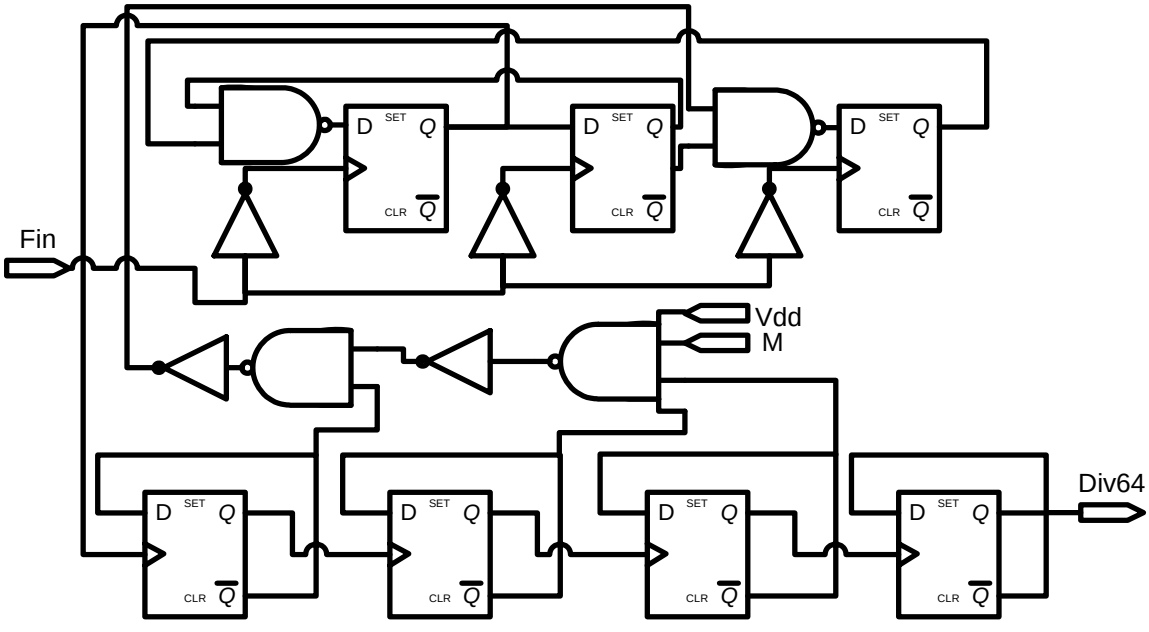


Figure 3.11: Divide by 64

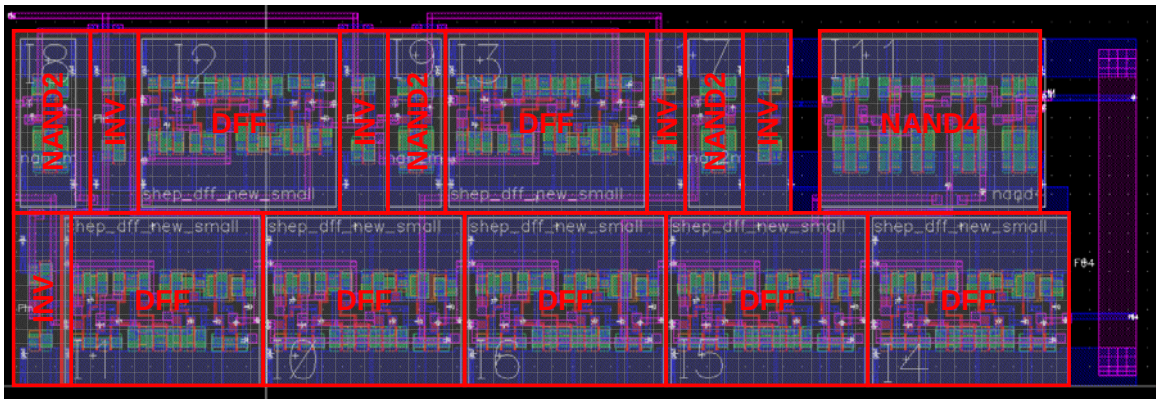


Figure 3.12: Layout Divide by 64

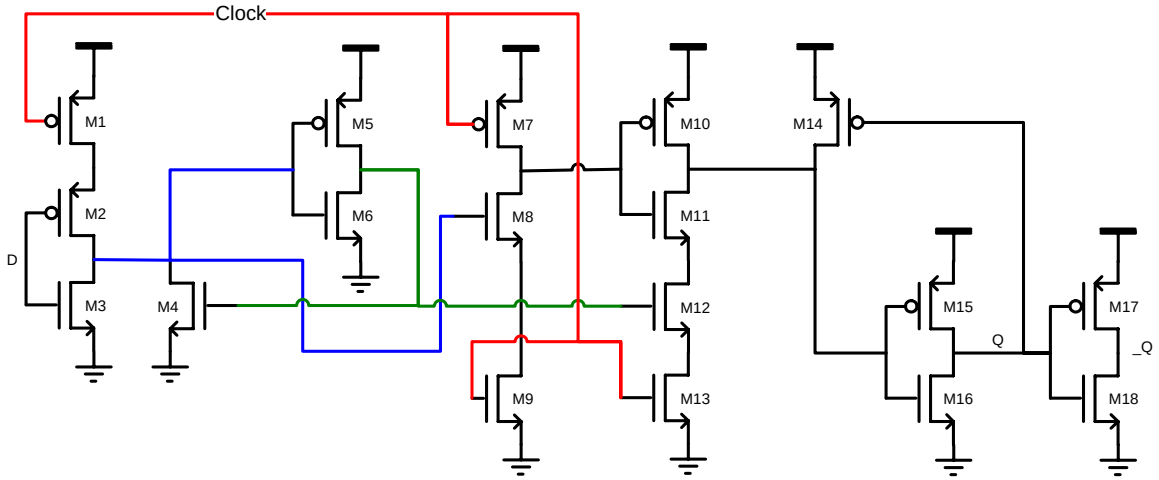


Figure 3.13: Divide by 64 DFF Schematic [5]

Table 3.2: Divide by 64 DFF Schematic

Transistor	W(μm)	L(μm)	m	f
M1	3.6	.5	1	1
M2	3.6	.5	1	1
M3	1.2	.5	1	1
M4	2.4	.5	1	1
M5	1.2	.5	1	1
M6	1.2	.5	1	1
M7	3	.5	1	1
M8	3	.5	1	1
M9	3	.5	1	1
M10	6	.5	1	1
M11	2	.5	1	1
M12	2	.5	1	1
M13	2	.5	1	1
M14	1.2	.5	1	1
M15	5	.5	1	1
M16	1.2	.5	1	1
M17	3	.5	1	1
M18	1.2	.5	1	1

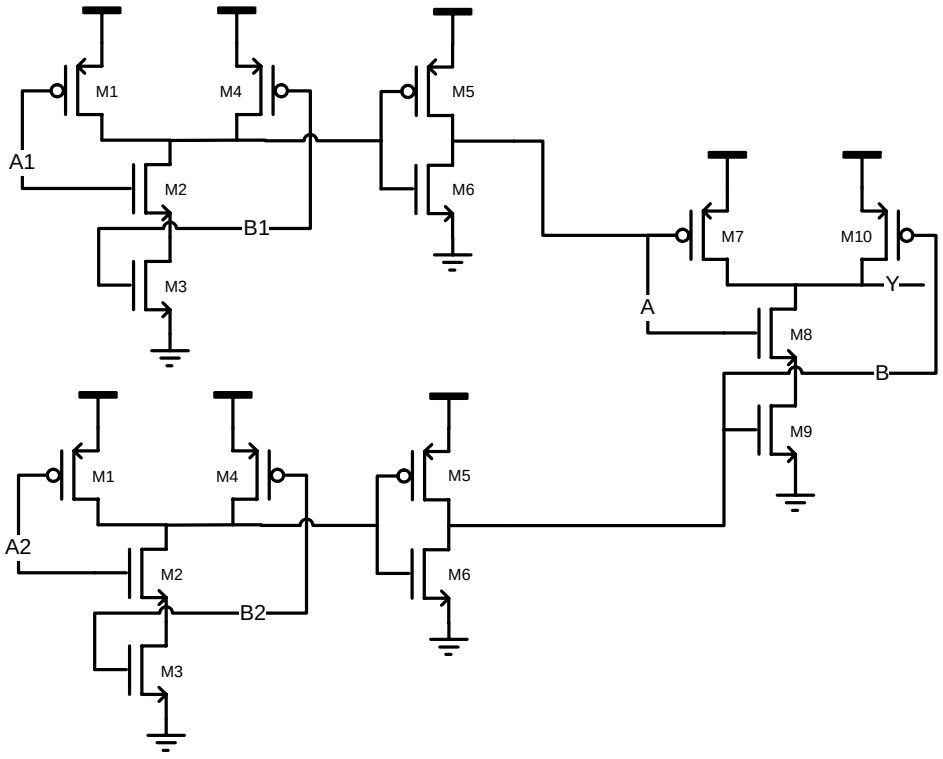


Figure 3.14: Divide by 64 NAND4 Schematic

Table 3.3: Divide by 64 NAND4

Transistor	W(μm)	L(μm)	m	f
M1	9	.5	1	1
M2	3.6	.5	1	1
M3	3.6	.5	1	1
M4	9	.5	1	1
M5	9	.5	1	1
M6	3.6	.5	1	1
M7	9	.5	1	1
M8	3.6	.5	1	1
M9	3.6	.5	1	1
M10	9	.5	1	1

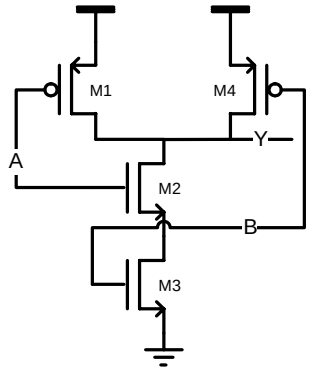


Figure 3.15: Divide by 64 NAND2 Schematic

Table 3.4: Divide by 64 N AND2

Transistor	W(μm)	L(μm)	m	f
M1	9	.5	1	1
M2	3.6	.5	1	1
M3	3.6	.5	1	1
M4	9	.5	1	1

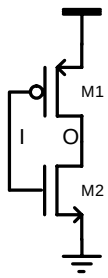


Figure 3.16: Divide by 64 INV Schematic

Table 3.5: Divide by 64 INV

Transistor	W(μm)	L(μm)	m	f
M1	4	.5	1	1
M2	2	.5	1	1

3.4 Phase & Frequency Detectors

3.4.1 Typical Phase & Frequency Detectors

Detecting and adjusting the Phase and Frequency is an essential part in the feedback path of a PLL. These functions can be implemented by having a double feedback path with both Phase feedback as well as Frequency feedback. It is important that these feedback paths vary as linear as possible with respect to the Frequency and Phase when a control voltage is applied; Figure 3.17.

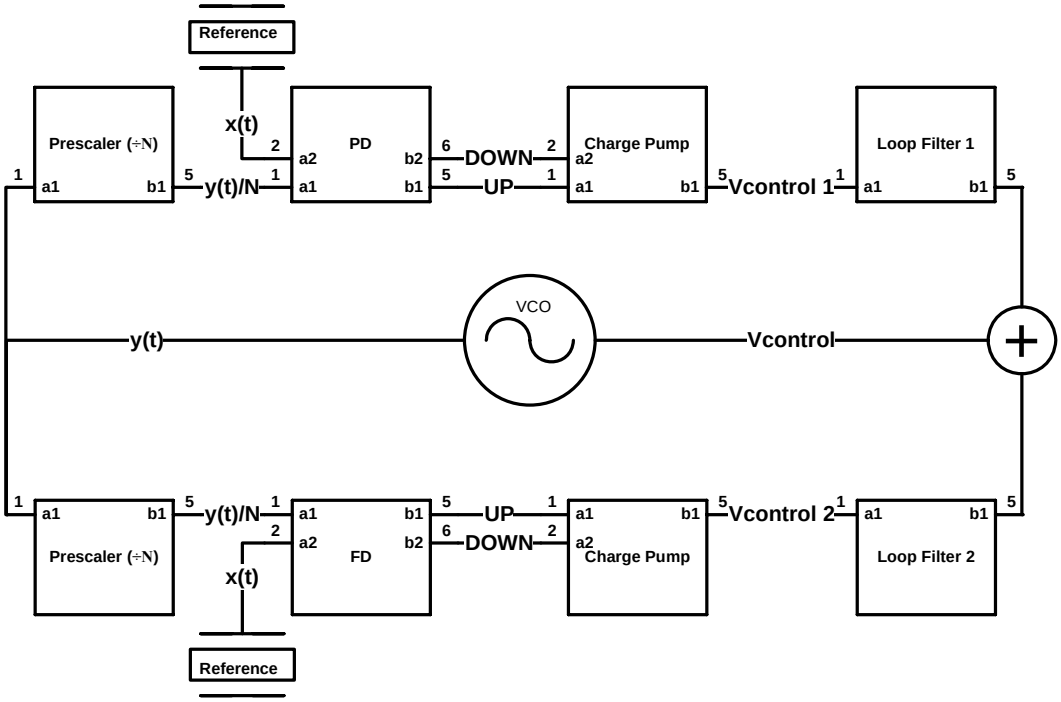


Figure 3.17: Phase and Frequency Detecting PLL [7]

A more concise way of implementing Phase and Frequency detection is through a combined Phase Frequency Detector (PFD); Figure 3.18, Figure 3.19, and Table 3.1. This easy to implement device works by comparing two "clock style" signals' frequency and phase at the same time as shown in Figure 3.20. The principal behind this circuit is to compare clock signal A to clock signal B. If clock signal A leads clock signal B, then the

PFD produces a pulse that is designed to speed up the VCO frequency. Similarly, if signal B leads signal A, then a signal is produced to slow the VCO frequency down.

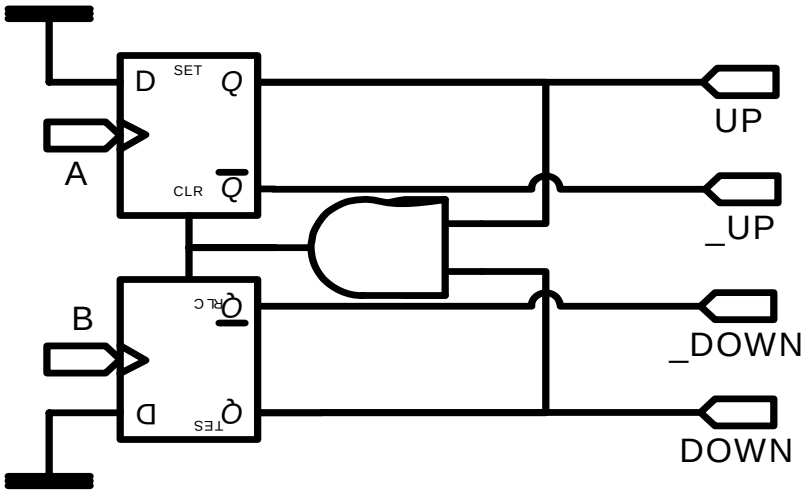


Figure 3.18: Typical Combined PFD [7]

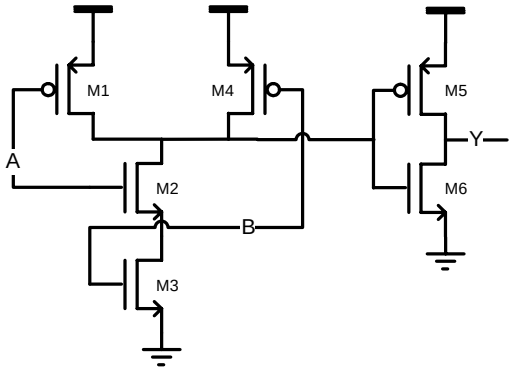


Figure 3.19: PFD AND2 Schematic

Table 3.6: PFD AND2

Transistor	W(μm)	L(μm)	m	f
M1	8	.5	1	1
M2	6.4	.5	1	1
M3	6.4	.5	1	1
M4	8	.5	1	1
M5	20.8	.5	1	1
M6	8.8	.5	1	1

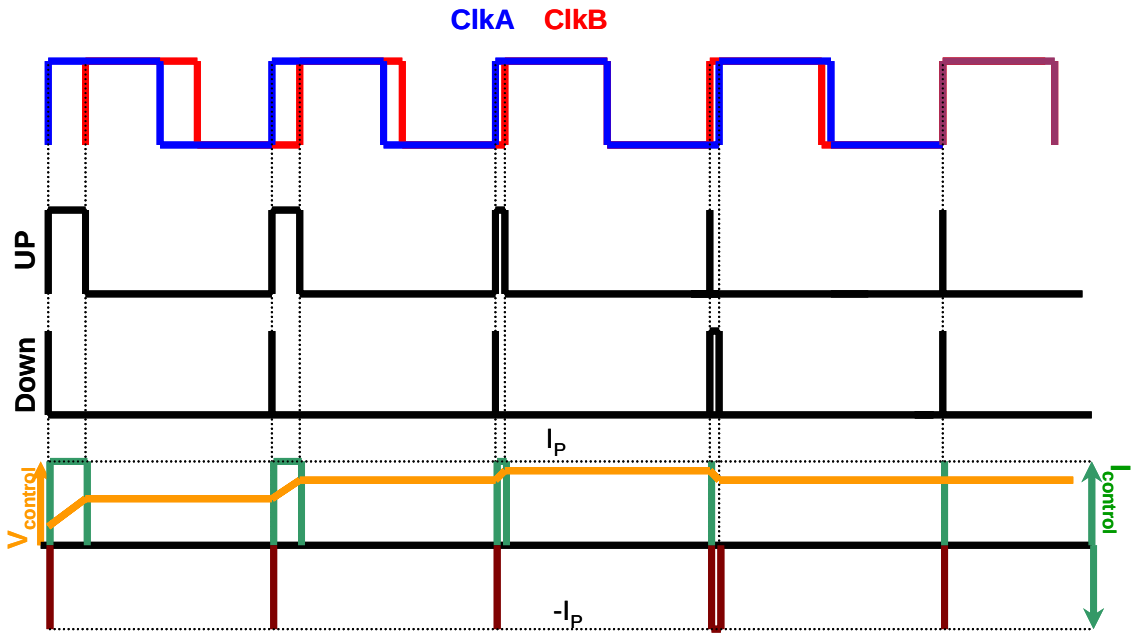


Figure 3.20: Operation of PFD and Charge Pump

This approach works because the PFD is constantly pushing and pulling the phase and frequency at incrementally smaller portions. In other words, the width of the control pulses becomes smaller until the two signals are locked at the comparison frequency and phase; Figure 3.21.

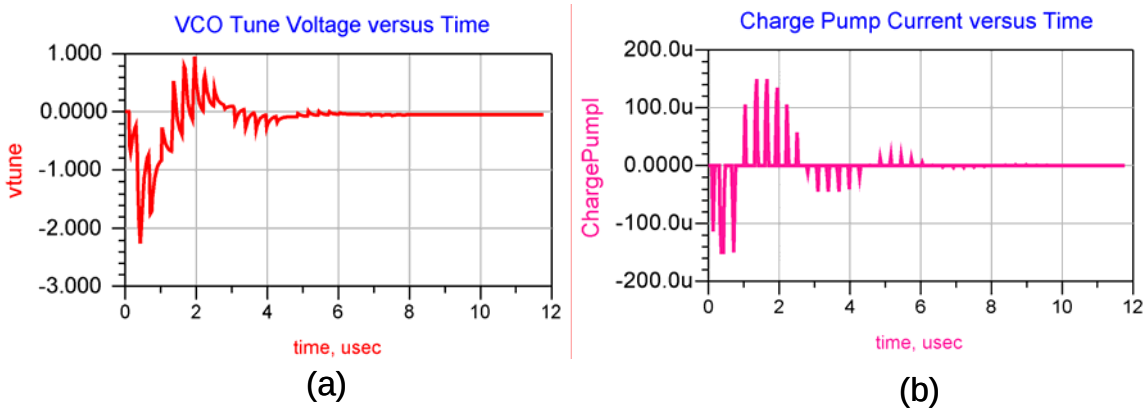


Figure 3.21: ADS Simulation of the PLL Achieving a Lock. (a) Control Voltage Locking. (b) Current injection/removal until lock

3.4.2 Implemention of a Modified Combined Phase Frequency Detector

The Typical Combined PFD, Figure 3.18, was analyzed and then modified to eliminate redundant transistors. When you look at the DFF in the PFD circuit, it is noted that the D

terminal is always connected to VDD, as shown in Figure 3.22. Since D is always VDD, V1 will always be 0 and V2 will always be VDD. Thus, we can eliminate M1, M2, M3, M4, M5, M6, and M12. If we then change the inputs of M7, M8, M9, and M13, we can significantly reduce the number of transistors to implement this circuit and reduced node capacitances, leakage paths, and performance drains. The transistor count was reduced by a factor of two when compared to the DFF's used in the 128 bit Divider; Figure 3.23, Figure 3.24, and Table 3.7.

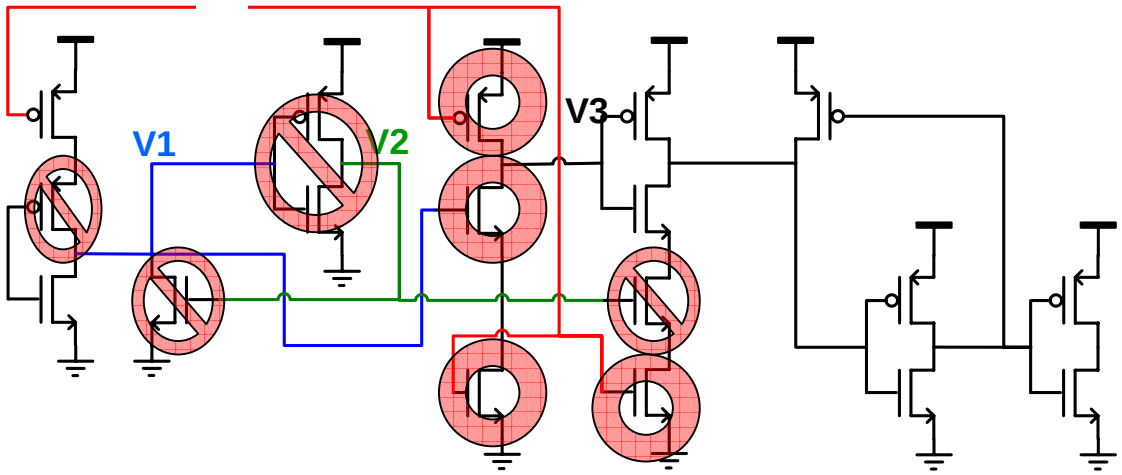


Figure 3.22: Reduction of Divide by 64 DFF [6] Schematic to PFD DFF Schematic

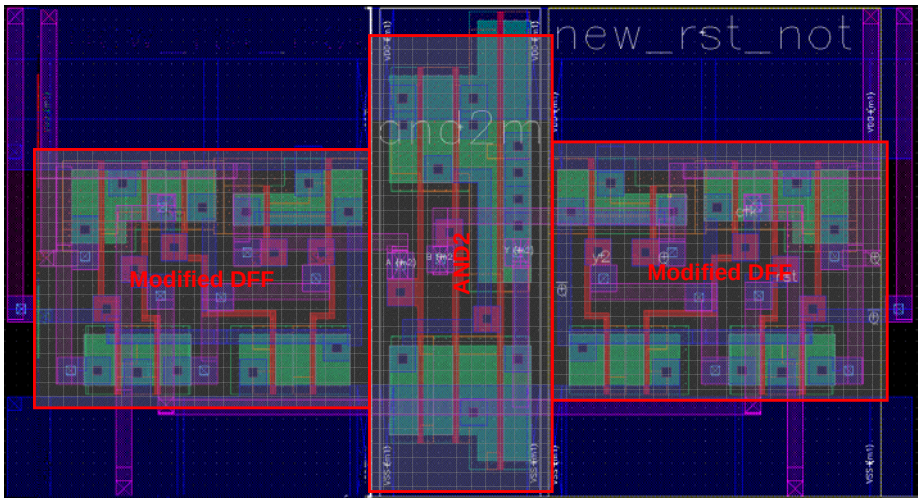


Figure 3.23: Modified Combined PFD Layout

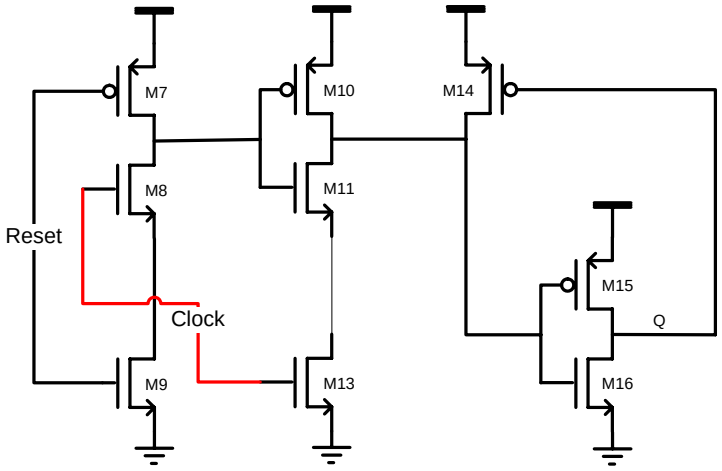


Figure 3.24: Modified PFD DFF Schematic

Table 3.7: Modified PFD DFF

Transistor	W(μm)	L(μm)	m	f
M7	3	.5	1	1
M8	3	.5	1	1
M9	3	.5	1	1
M10	3	.5	1	1
M11	3	.5	1	1
M13	2	.5	1	1
M14	1.2	.5	1	1
M15	5	.5	1	1
M16	1.2	.5	1	1

3.5 Charge Pump

3.5.1 Fundamental Charge Pump

The charge pump converts the Up and Down pulses of the PFD to adding and subtracting current from the Loop Filter. This can be realized crudely, by using a bias network to determine the current in a PMOS and NMOS stack using the middle two PMOS and NMOS devices as switches to direct the current; Figure 3.25. The fundamental charge pump has system expression of Equation 3.2.

$$K_{\text{chargepump}} = \frac{I_P}{2\pi}$$

Equation 3.2

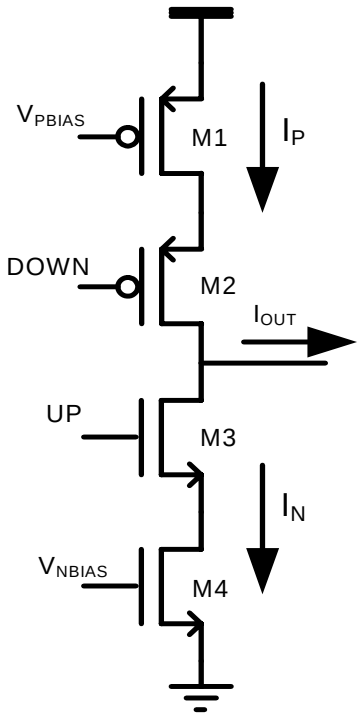


Figure 3.25: Fundamental Charge Pump [7]

3.5.2 Lei Luo's Charge Pump [8]

In a fundamental charge pump the currents will not be completely symmetrical, because the Up signal is triggering the NMOS device and the Down signal is triggering a PMOS

device. Since these two devices have different switching speeds, the amount of current injected or removed from the loop filter vs. time are not symmetric. However, Lei Luo's charge pump is very symmetric because it uses an NMOS for both the UP and DOWN Signals; Figure 3.26. The current charging/discharging the Loop filter is $I_4 - I_2$. By ignoring second order effects, while second order effects will cause slight current mismatch ignoring them can be done since transistor sizes are not minimal and there for not dominant, I_4 has to equal I_3 because M4 is diode connected to M3. This means $I_{out} = I_4$ or that when an Up pulse is signaled, I_3 no longer equals 0 and is reflected into I4. If the Down pulse has not signaled during the Up pulse, I_2 will equal 0 and the Loop filter will have I_4 injected into it. However, when the Down pulse is signaled, I_2 will no longer equal zero and if the Up signal has not signaled during the down pulse $I_1=I_3=I_4=0$. This means Iout = $-I_2$ or that the Loop filter will have removed out of it. If both the Up and Down signals occur at the same time, then $I_1=I_2=I_3=I_4$ or $I_{out} = I_4 - I_2 = 0$. To ensure that second order effects, such as Drain Induced Barrier Lowering which results in asymmetric currents in M1 and M2, $I_3 \neq I_4$, the transistors should be at least 4 times the minimal length.

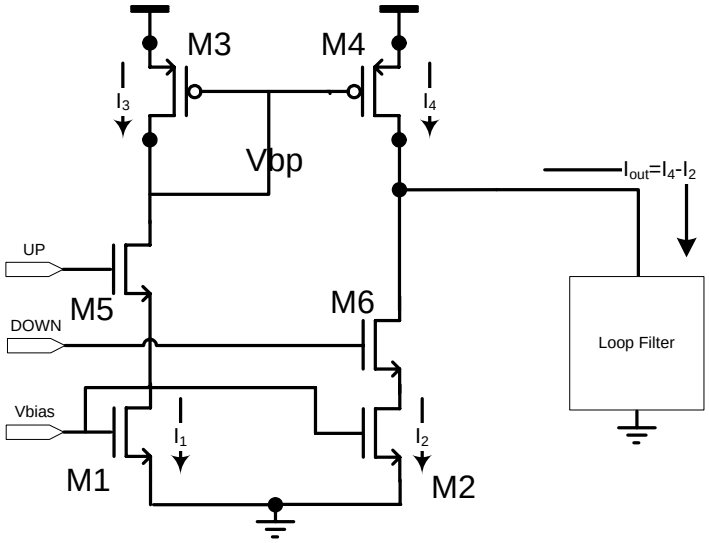


Figure 3.26: Lei Luo's Charge pump [8]

3.5.3 Modified Charge Pump

The proposed Modified Charge Pump would minimize switching noise. Switching noise is when a transistor is switched on or off, and there is a finite amount of current that will be injected or removed from the circuit due to the switching transistor. The circuit was modified to add a transistor of approximately half of the width of M5/M6 above and below it; Figure 3.27, Figure 3.28, and Table 3.8. These transistors will be connected to Up_not and Down_not signals. This will either accept or inject the extra charge that caused by the transistor switching on and off. This design methodology reduces the amount of "ripple" induced by the charge pump on the control voltage of the VCO.

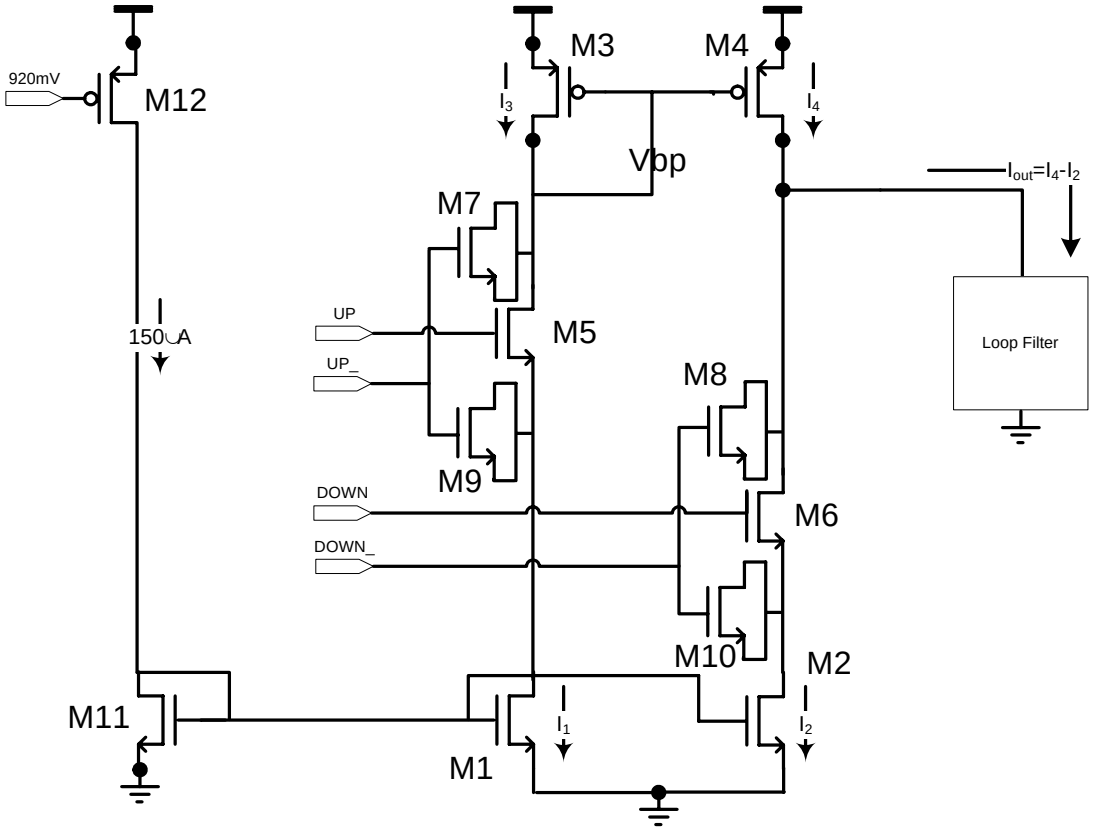


Figure 3.27: Modified Charge Pump

Table 3.8: Transistor Sizing for 150 μA Charge Pump

Transistor	W(μm)	L(μm)
M1,M2,M3,M4	10	1.4
M7,M8,M9,M10	2.3	.5
M5,M6	5	.5
M12	14	1.4
M11	8.4	1.4

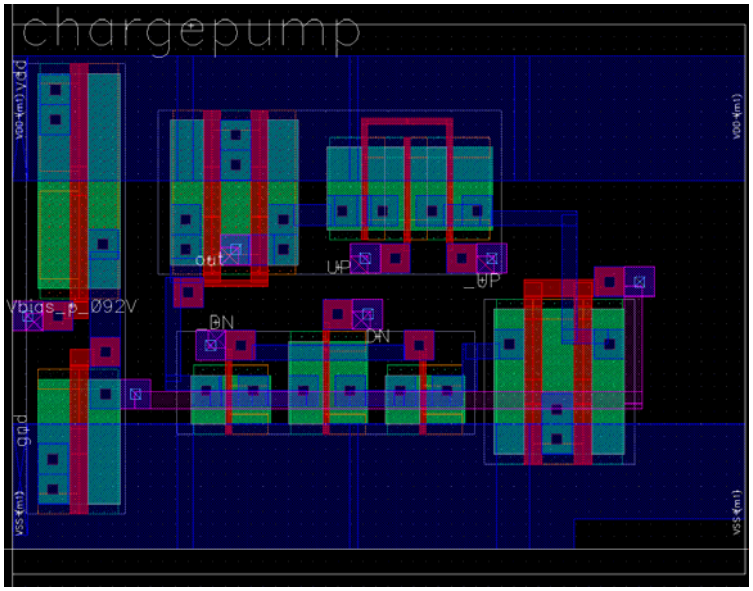


Figure 3.28: Layout of Modified Charge Pump

3.6 Loop Filters

The basic loop filter is designed to store charge injected/removed by the charge pump which provides a dynamic memory for the control voltage Figure 3.29.

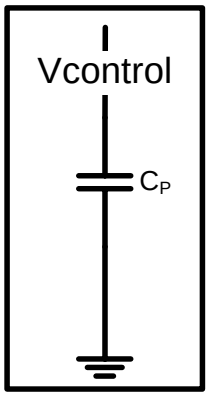


Figure 3.29: Basic Loop Filter [7]

However, Loop filter design is more complex than just adding a capacitor to the system. One major problem is that when a solely capacitive loop filter is used in the PLL at the system level; there will be a pole at the origin causing instability. To combat the stability issue, a series resistance, R_P, is placed in the loop filter. The stability issues of the loop filters will be discussed in further detail in 3.10 .

The bandwidth, Equation 3.3, of the Loop Filter will also be set from an RC time specification. R_{eff} can be approximated as R_P in Figure 3.30 when a second order loop filter is used.

$$\tau = R_{eff} C_P = Bandwidth^{-1}$$

Equation 3.3

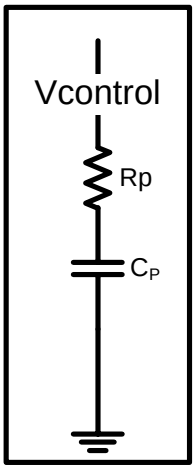


Figure 3.30: Stable Basic Loop Filter [7]

An inherent problem with the choice of the Stable Basic Loop Filter, Figure 3.30, is that each time the charge pump injects or removes current, a large jump can be observed in the control voltage given by Equation 3.4.

$$\Delta V_{control} = R_{eff} I_P$$

Equation 3.4

Adding a ripple reduction capacitor, C2 in Figure 3.31, mitigates the need for this. However, in adding a second pole, we change our loop filter from a first order to a second order loop filter. A problem with this technique is that a second order loop filter results in a third order PLL, which can cause stability issues. We can avoid this problem by making C_2 to be 1/5 to 1/10 of C_P. When C_2 is in the specified range, the result is the ability to approximate the loop filter as a first order loop filter which results in approximating the PLL as a second order PLL. More details will be discussed in 3.10 .

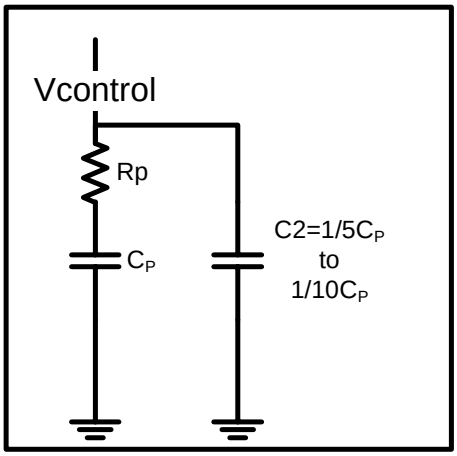


Figure 3.31: Stable (second order) Loop Filter with a "ripple" reduction capacitor [7]

The Loop Filter in Figure 3.31 was further modified to Figure 3.32, which gave the ability to reset the voltage applied to the PLL to ground. This was done to aid in trouble shooting the PLL by setting $V_{control}$ to a known value. The implemented layout and sizes are shown in Figure 3.33 and Table 3.9.

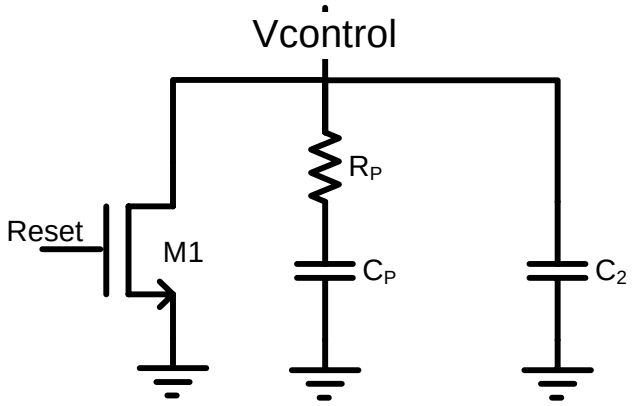


Figure 3.32: Implemented Loop filter (reset included)

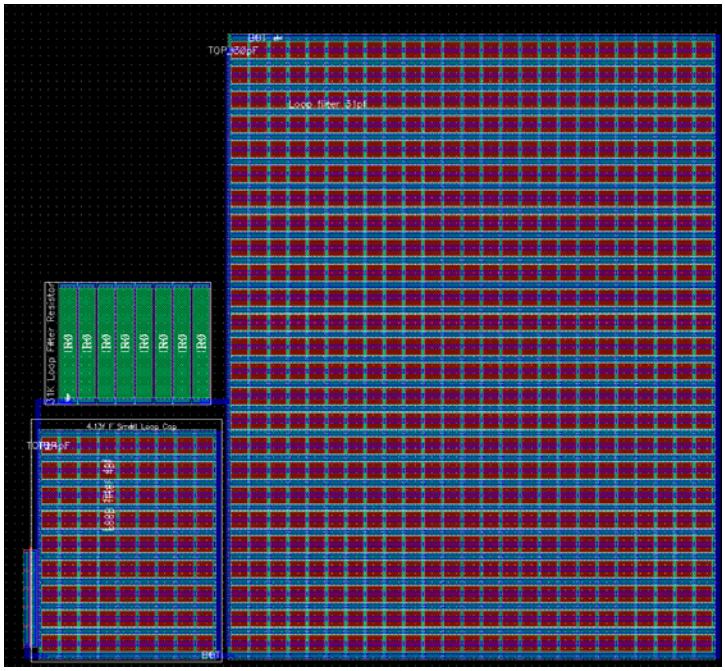


Figure 3.33: Layout of Loop Filter

Table 3.9: Loop Filter Elements

Element	Value
Rp	31kΩ
Cp	31.875pF
C2	4.131pF
M1	W=50 μm, L=.3μm

3.7 Voltage Controlled Oscillator

3.7.1 Typical Voltage Controlled Oscillators

Voltage controlled oscillators are heavily used in the communications market, because they can faithfully reproduce an accurate carrier frequency for a communication link. A simple realization of a VCO is a negative Gm cross- coupled pair NMOS LC tank; Figure 3.34. It is a common practice to achieve a larger voltage swing to use both NMOS and PMOS cross coupled pairs to build an effective amplified VCO; Figure 3.35. However, by increasing the amplitude of the VCO signal, we sacrifice the tuning range of the VCO due to the add parasitic capacitance of the PMOS devices. This is an acceptable trade in our case because we are building a Low power VCO and since Power = Current*Voltage. The same amount of voltage swing from half the current as the NMOS only cross coupled pair can be achieved by this method.

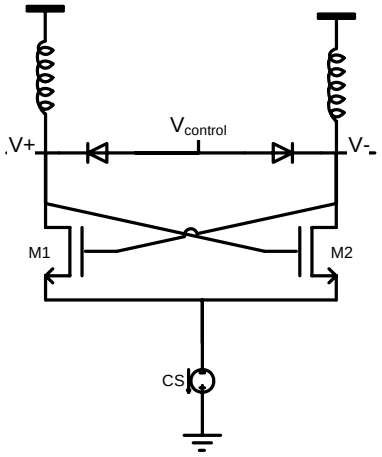


Figure 3.34: Negative GM NMOS Cross Coupled Pair VCO [7]

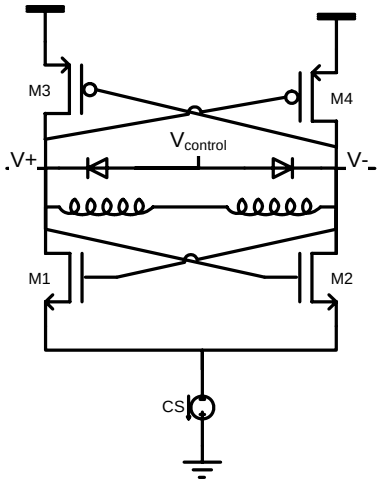


Figure 3.35: Negative GM NMOS and PMOS Cross Coupled Pair VCO [7]

An ideal VCO will generate an output frequency based on Equation 3.5, where Kvco is the VCO gain, $V_{control}$ is the control voltage, and W_{FR} is the slowest frequency of the VCO.

$$\omega_{out} = \omega_{FR} + KvcoV_{control}$$

Equation 3.5

This means that the output frequency can be modeled as a linear function of the control voltage. Creating a time varying equation for the VCO using Equation 3.6.

$$y(t) = A\cos(\omega_{FR}\, t + Kvco\int_{-\infty}^{t} v_{control}\, dt)$$

Equation 3.6

From the analysis of Equation 3.6, one can note that using $\cos(\omega + \phi)$ as an envelope the phase term can be extracted as Equation 3.7.

$$\phi_{out}(t) = Kvco\int v_{control}\, dt$$

Equation 3.7

Using a Laplace transform yields the transfer function Equation 3.8.

$$\frac{\Phi_{out}(s)}{V_{control}(s)} = \frac{Kvco}{s}$$

Equation 3.8

3.7.2 Quadurature Voltage Controlled Oscillator

A quadurature VCO can be implemented one of three ways:

1) Combining a VCO, Polyphase-filter, and output buffers/limiters
2) VCO at twice the frequency followed by master slave flipflops
3) Two cross-coupled VCO's

Implementing the first option requires four output buffers that consume a lot of power; which is contrary to a low power device. Another draw back is that by inserting the filter into the design, it increases the fixed tank capacitance resulting in lower VCO gain and higher power consumption. Also, these designs are usually area intensive due to matching networks required by the filters [9].

The second option would be an ideal choice if the primary concern of the design specification was area. Since there is only one VCO, the area advantage of the second choice over the third choice is significant, because there are now two LC tanks consuming area. In addition to just using one VCO, the LC tank is also reduced by an approximate factor of two because the VCO is operating at twice the frequency. A problem with this topology is that the master slave flipflops tend to consume a significant amount of power above 0.25μm [9].

This lead us to choose the third device despite the area penalty; Figure 3.36, Figure 3.37, Figure 3.38, Figure 3.39, and Table 3.11. This solution also offers a higher voltage swing, thus reducing the amount of current required to produce the same amount of swing. The

higher voltage swing can also be used to ease the design of mixing circuits and the prescaling circuit [9].

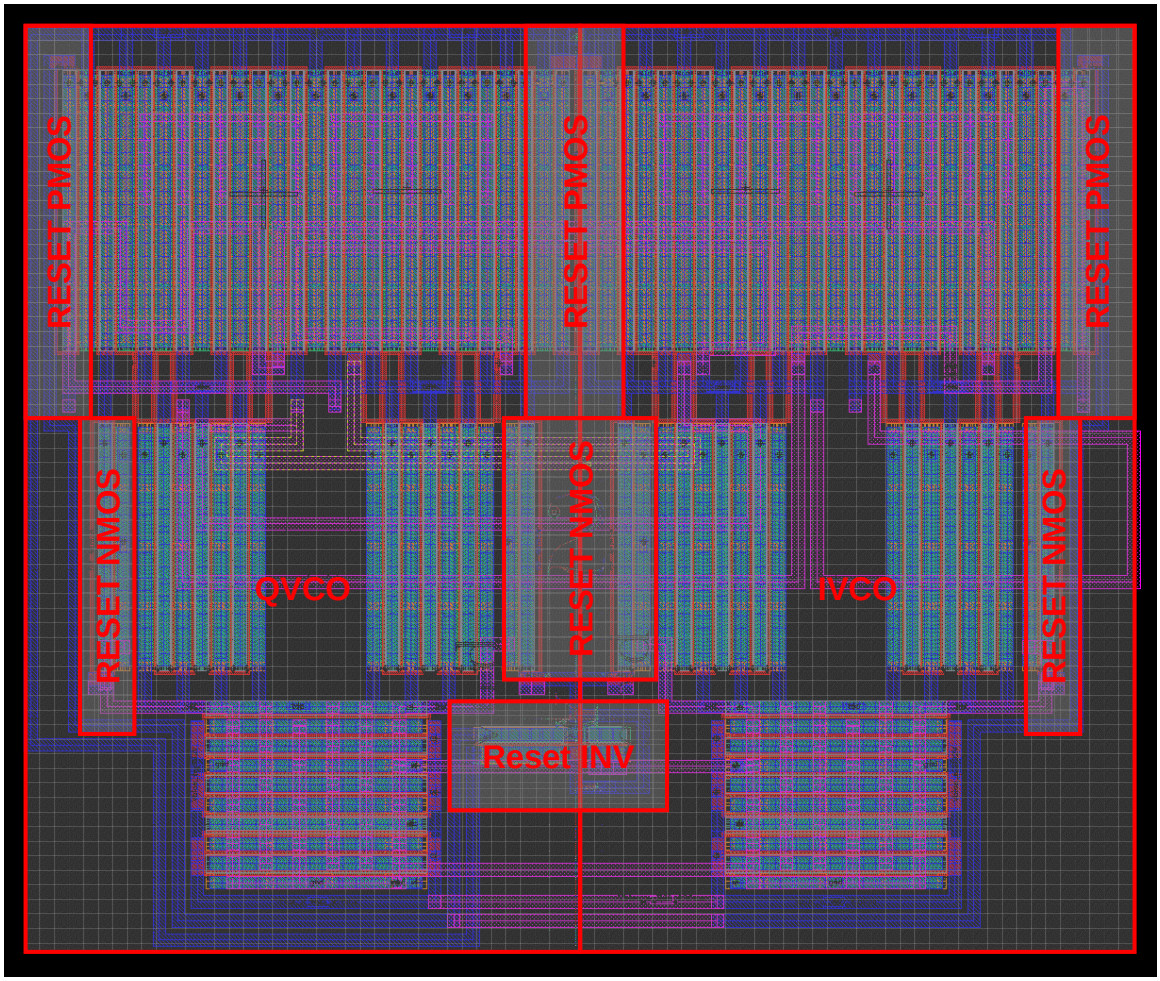


Figure 3.36: Layout of Quadurature VCO

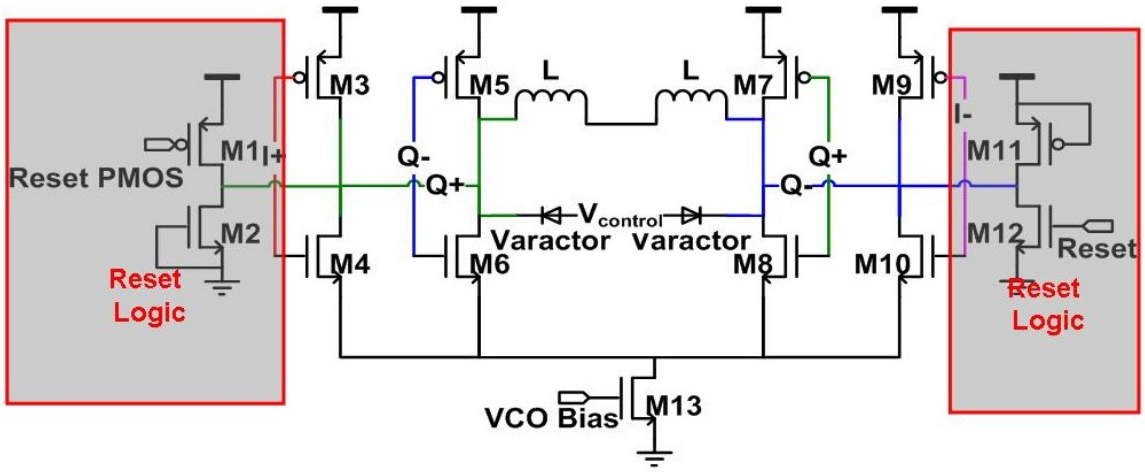


Figure 3.37: Quadurature Q+/-VCO Schematic

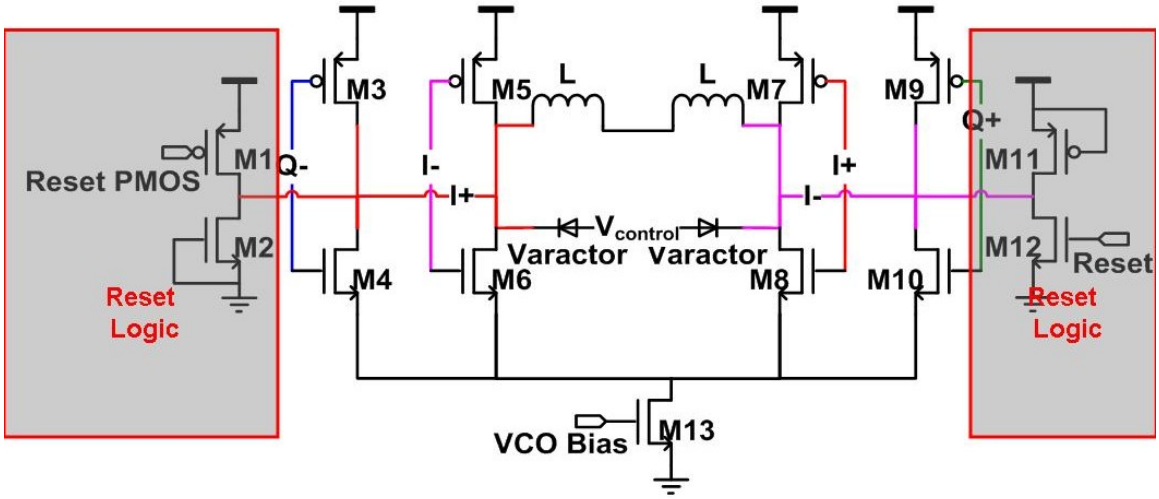


Figure 3.38: Quadurature I+/-VCO Schematic

Table 3.10: Quadurature VCO Transistor Sizes

ITEM	M	F	W (um)	L (um)
M1	**1**	**1**	**45**	**0.5**
M2	**3**	**1**	**40**	**0.5**
M3	**6**	**1**	**45**	**0.5**
M4	**3**	**1**	**40**	**0.5**
M5	**6**	**1**	**45**	**0.5**
M6	**3**	**1**	**40**	**0.5**
M7	**6**	**1**	**45**	**0.5**
M8	**3**	**1**	**40**	**0.5**
M9	**6**	**1**	**45**	**0.5**
M10	**3**	**1**	**40**	**0.5**
M11	**1**	**1**	**45**	**0.5**
M12	**1**	**1**	**40**	**0.5**
M13	**3**	**3**	**35**	**1**

	A (um)	**M**
D	**0.488**	**200**

	C (fF)	**R (ohm)**	**L (nH)**
L	**68**	**10**	**16.9**

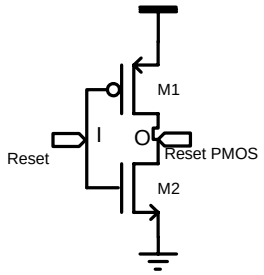


Figure 3.39: Reset INV Schematic

Table 3.11: Reset INV Transistor Sizes

ITEM	M	F	W (um)	L (um)
M1	**1**	**1**	**14.5**	**0.5**
M2	**1**	**1**	**5.5**	**0.5**

3.7.3 Comparison of Implemented Voltage Controlled Oscillators

Since this was the second fabrication of the system on chip design, we could learn from previous experiences on the new fabrication. After studying the previous design several conclusions were made:

1) Current consumption needed to be reduced to decrease power consumption
2) Varactor needed recalculation to ensure proper working range

3) The larger inductor was desired due to previous physical measurements

In the spirit of reducing current, an improvement was realized after analyzing the way the previous VCO was reset. If you analyze Figure 3.40, you will notice that when Reset is low (normal operation) there are static paths to VDD on transistor M1 and static paths to Ground on transistor M12. By changing the "Reset Logic" in Figure 3.40 to the "Reset Logic" in Figure 3.37, Figure 3.38, and Figure 3.39 there will no longer be a static path to VDD or Ground. The reset logic was designed to balance the VCO; in other words each VCO sees the same added load from the "Reset Logic." To further reduce the current of the previous design (Figure 3.40, Figure 3.41, and Table 3.12), the current was limited by a tail transistor, as shown in Figure 3.37 and Figure 3.38, to produce the desired current.

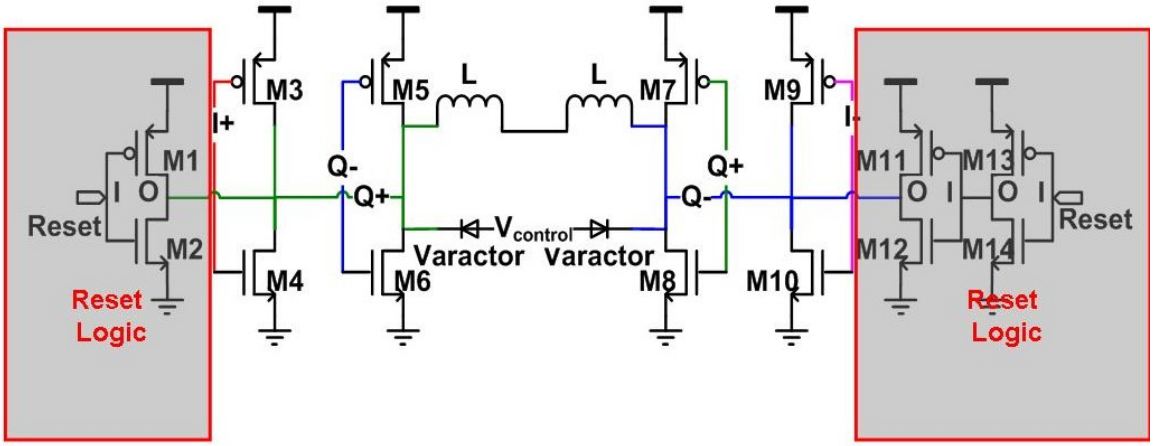


Figure 3.40: Old Quadurature QVCO Schematic

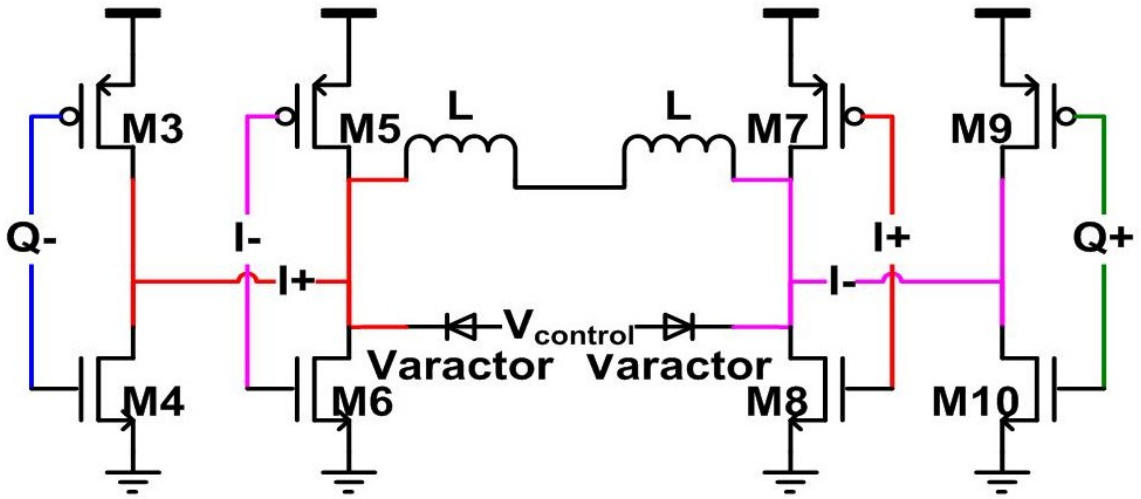


Figure 3.41: Old Quadurature IVCO Schematic

Table 3.12: Old Quadurature VCO Transistor Sizes

ITEM	M	F	W (um)	L (um)
M1	1	1	14.5	0.5
M2	1	1	5.5	0.5
M3	6	1	45	0.5
M4	3	1	40	0.5
M5	6	1	45	0.5
M6	3	1	40	0.5
M7	6	1	45	0.5
M8	3	1	40	0.5
M9	6	1	45	0.5
M10	3	1	40	0.5
M11	1	1	14.5	0.5
M12	1	1	5.5	0.5
M13	1	1	14.5	0.5
M14	1	1	5.5	0.5
	A (um)	M		
D	1.632	30		
		R		
	C (fF)	(ohm)	L (nH)	
L	52	6.4	8.9	

To roughly calculate the desired current, the transconductance, G_M, needed to achieve unity loop gain at the oscillations frequency, wo, from Equation 3.9 through Equation 3.16 is needed.

$$G_M = R_{eff}(\omega_O C)^2$$

Equation 3.9

$$R_{eff} = R_C + R_L + \frac{1}{R_P(\omega_O C)^2}$$

Equation 3.10

Where R_P is the parallel tank resistance, R_L is the inductor series resistance, and R_C is the varactor series resistance[cite]. The frequency of oscillation can be easily calculated by the LC tank components using Equation 3.11 and Equation 3.12.

$$\omega_O = 2\pi f_O$$

Equation 3.11

$$f_O = \frac{1}{2\pi\sqrt{LC}}$$

Equation 3.12

Solving these two equations for C

$$435\ MHz = \frac{1}{2\pi\sqrt{16.9nH}}$$
$$C = 7.9nH$$

Equation 3.13

Using the schematic model, which was derived from a previous physical characterization, the Series resistance, R_L, of the 8.5 turn 16nH inductor is 10ohms. Approximating the resistance of R_S and R_P as around 1ohm each estimates Reff as 12ohms. Then by solving Equation 3.9, we determine the GM required for unity loop gain operation; Equation 3.14.

$$G_M = R_{eff}(\omega_O C)^2 = 12(2\pi 7.9\,pF)^2 = 5.6ms$$

Equation 3.14

Designing to ensure that our device will indeed be in the unity loop gain operation an extra 2mS is added giving a total of 7.6mS. Using the drain current equation for a transistor, Equation 3.16, in saturation region and Equation 3.15 the estimated desired current for the VCO can be solved for; keep in mind this design has 2 VCO's.

$$V_{GS} - V_T = 0.3V$$

Equation 3.15

$$I_D = g_m(V_{GS} - V_T)/2 = \frac{(5.6mS + 2mS)*.3V}{2} = 2*1.14mA = 2.28mA$$

Equation 3.16

Through comparing the theoretical results, 2.28mA, to the current consumption results of the extracted Quadurature VCO, 2.29mA, it is noticed that the currents are identical. The

current consumed is nearly one twentieth when compared to the previous 45mA current. The corresponding transistor *W/L* ratios are noted in Table 3.10.

PN Junction diodes were used as variable capacitors, because when you apply a voltage to a diode the depletion region changes with respect to the voltage applied, as shown in Figure 3.42. In essence the depletion region is in distance between the two capacitance plates, and the capacitance is given by Equation 3.17.

$$C' = \frac{\varepsilon}{\text{distance}}$$

Equation 3.17

The diode count in the varactor had to be recalculated due to a change in the model. First the Junction capacitance, C_{jo}, of a pwell diode was extracted from the Spectre model files equaling 0.821fF per unit area. In Equation 3.18, we solved the number of diodes to be approximately 200.

$$\#\ diodes = \frac{C}{Cjo * A} = \frac{7.9\ pF}{0.821\ \frac{fF}{A} * .488\ A} = 197 \cong 200$$

Equation 3.18

$$\#\ diodes = \frac{C}{Cjo * A} = \frac{15.9\ pF}{0.186\ \frac{fF}{A} * 1.632\ A} = 52 \cong 60$$

Equation 3.19

Compared to the original design of 60, as solved in Equation 3.19, the diode count increased due to a change in the geometry of the vendors diode model, as shown in Figure 3.43. The area consumed by the implemented varactor was 650 μm X 1100 μm vs. 525 μm X 650 μm in the previous design.

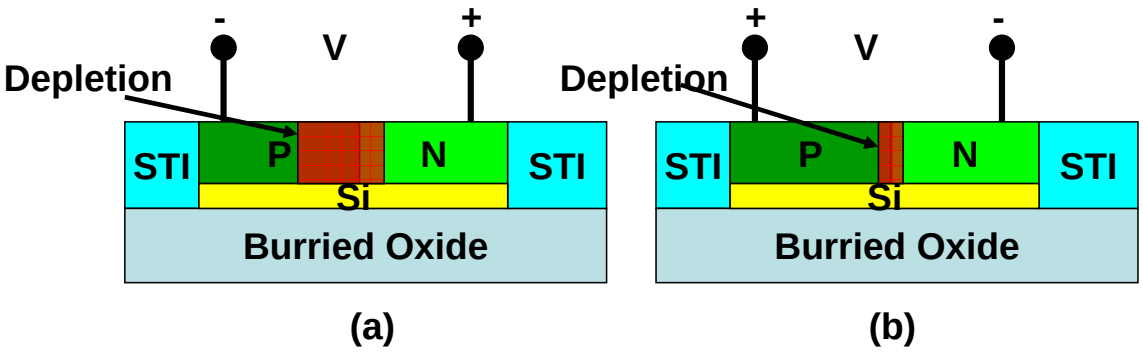


Figure 3.42: PN Junction Diode. (a) PN Junction diode with the P contact at $V_{diode\ break\ down}$<V<0. (b) PN Junction diode with the P contact at 0<V<$V_{diode\ turn\ on}$

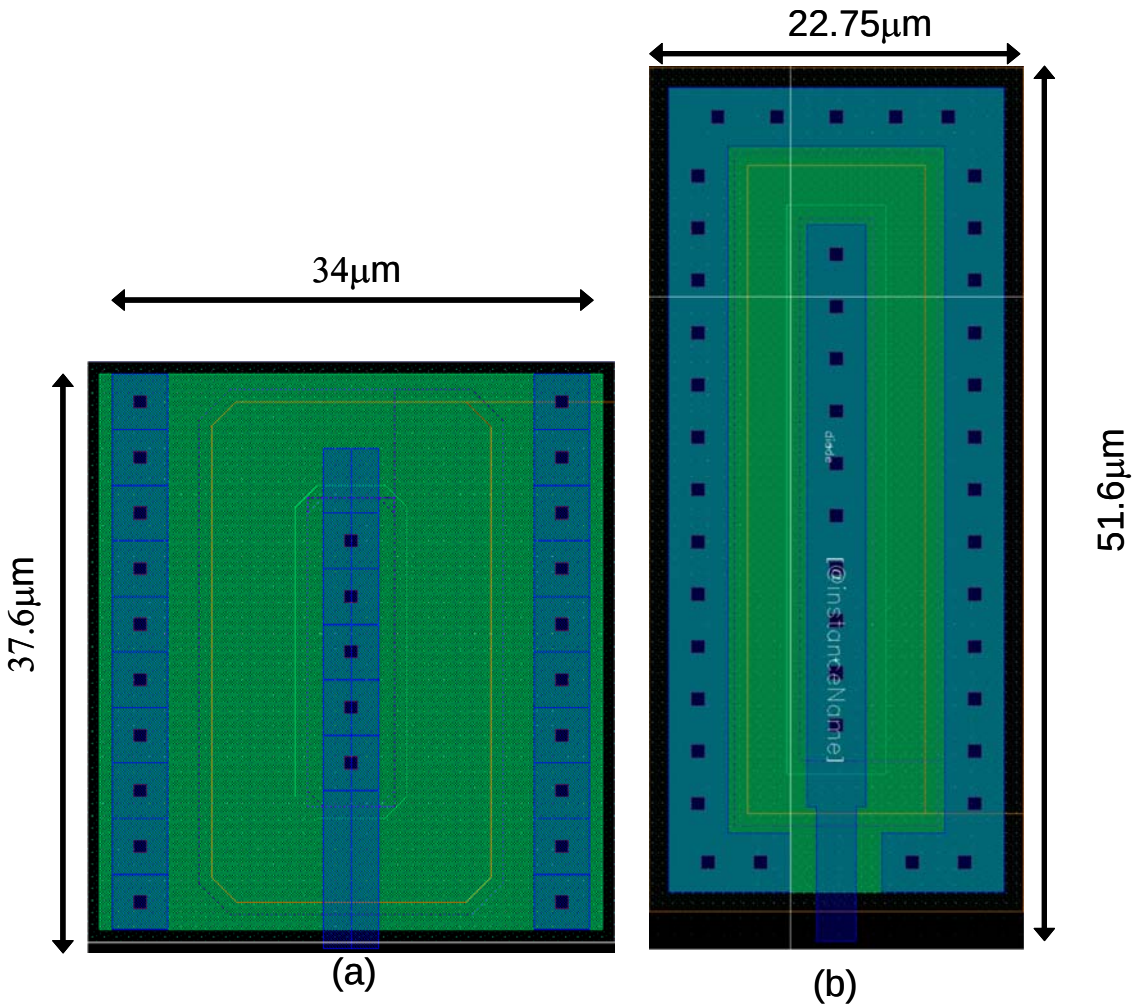


Figure 3.43: (a) Honeywell PDSOI Version 17 pwell Diode Layout. (b) Honeywell PDSOI Version 14 pwell Diode Layout.

The larger inductor was used for two reasons:

1) Area Consumption

2) High Quality Factor at 435MHz

If a smaller inductor was used, the capacitance would have to double. While this is good for tuning range of the varactor, the area would also double and since there are 4 varactors for the implementation, this would require too much area to implement. The measured Q at 435MHz for our implementation is approximately four, from Figure 3.44. Q is important because it is the ratio of power used over power lost due to parasitics. The inductors also take up a reasonable amount of area; 345 μm by 360 μm each.

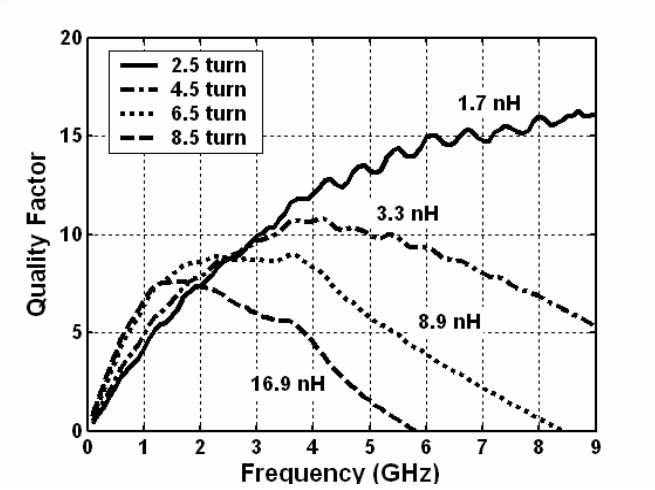


Figure 3.44: Quality factor vs. Frequency of the 1.7nH, 3.3nH, 8.9nH, and 16.9nH inductors [3]

3.8 Bandgap reference circuit

The implemented bandgap reference circuit, as shown in Figure 3.45, [3] is deemed outside of the scope of this paper. The reason is that this circuit was implemented and optimized elsewhere in the System on Chip. Our PLL design can utilize the on chip bandgap reference circuit or, in case of a bandgap reference circuit failure, off chip references can be utilized.

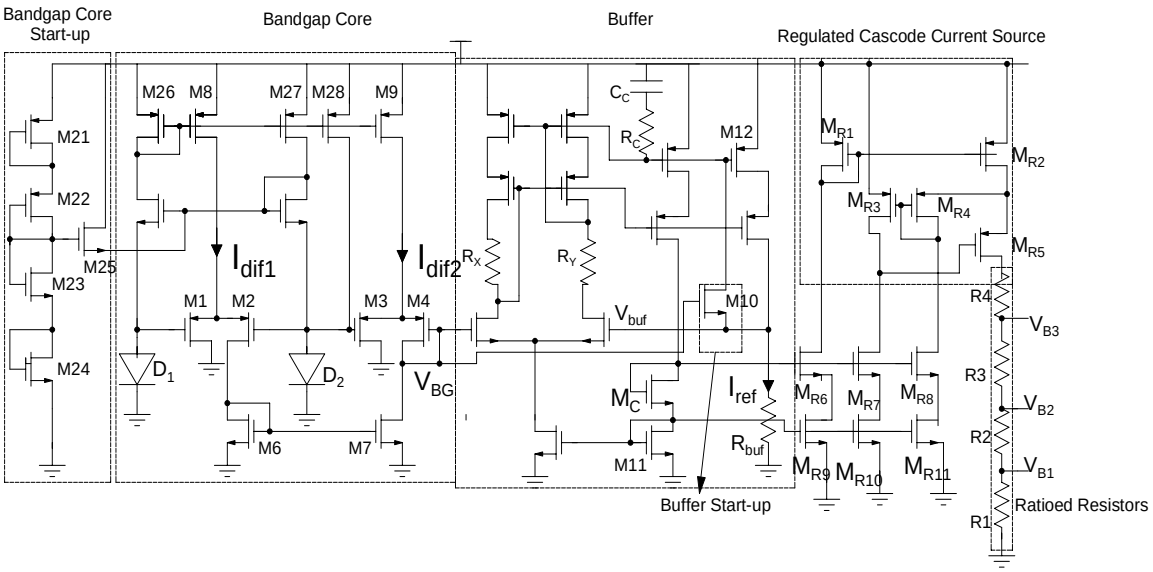


Figure 3.45: Bandgap voltage reference circuit with a regulated cascode output stage [3]

3.9 Output Buffers

3.9.1 VCO Common Mode Isolation

A common problem in buffer design, is to have common mode mismatches due to process variation. To design around this problem and ensure proper operation, Common Mode Isolation is a recommended practice. Common mode Isolation is the use of a series capacitor and shunt to a source with the desired common mode resistor, as shown in Figure 3.46. This enables two circuits with different common modes to still operate.

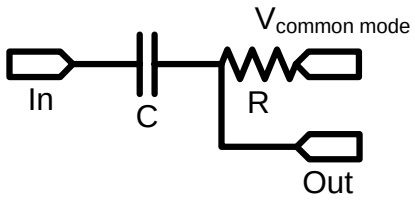


Figure 3.46: Common Mode Isolation Block Schematic

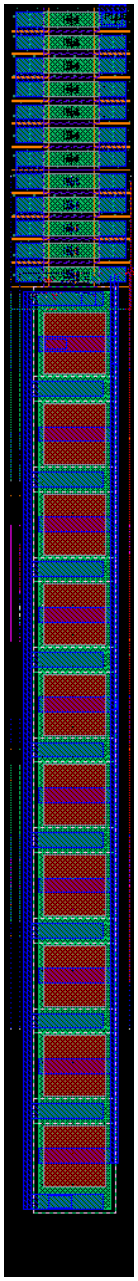


Figure 3.47: Layout of Common Mode Isolation Block

Table 3.13: Common Mode Isolation Block

Component	Values
R	200K
C	500fF
$V_{common\ mode}$	1.1V

3.9.2 VCO to Mixer Buffer

The mixer buffer, Figure 3.48, was designed to sync 1mA of current that will meet the peak to peak swing requirements of the mixer; 0.5V. The buffer needed to be designed to drive a 300fF load. First, we need to calculate the Resistive load, R, in Equation 3.20.

$$\tau = R * C \longrightarrow 435\ MHz^{-1} = R * 300\ fF$$
$$R = 7.5K\Omega$$

Equation 3.20

Next, calculate the tail current required to sustain an input swing from 0.92V to 2.5V in Equation 3.21.

$$Itail = \frac{\Delta V}{R} = \frac{(2.5 - 0.92)}{7.5K\Omega} = 0.211\ mA$$

Equation 3.21

Then, calculate Vp from Equation 3.22.

$$Vp > Max\ (Overdrive\ , INlow - Vth)$$
$$Vp > Max\ (0.25V, 0.92V - 0.7V) > .25V$$

Equation 3.22

Calculate the sizing of the M1 and M2 in Figure 3.48 by assuming IN_P=2.5V and design M1 and M2 to make sure Vp=0.25V. Also, calculate the sizing of the tail transistor (M0), making sure that you keep the tail transistor in the saturation region to get I_{tail}.

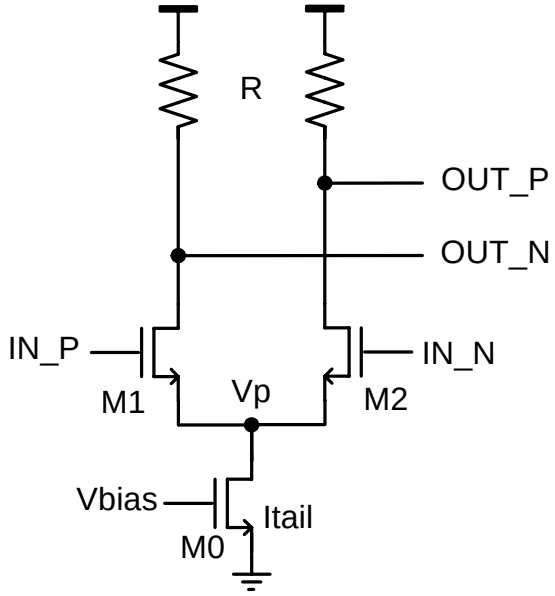


Figure 3.48: Schematic of VCO to Mixer Buffer [10]

The circuit output swing was then analyzed, and it was determined that we needed to sacrifice a higher Itail current for a higher voltage swing.

After designing the initial output buffers, another step was taken by extracting the actual first stage of the mixer and Ahmet's PLL output buffers. This was done to ensure that the PLL could indeed drive the Mixer while Ahmet's PLL was in the off state since this PLL and Ahmet's PLL shared a common interface. The final values of the buffer are in Table **3.14**.

Table 3.14: VCO to Mixer Output Buffer

Component	Values
Tail Transistor (M0)	W=35μm,L=1.5 μm,Fingers=21
M1,M2	W=15 μm,L=.350 μm,Fingers=10
Resistive Load (pwell Resistor)	1.5K ohm
Itail	1.8mA

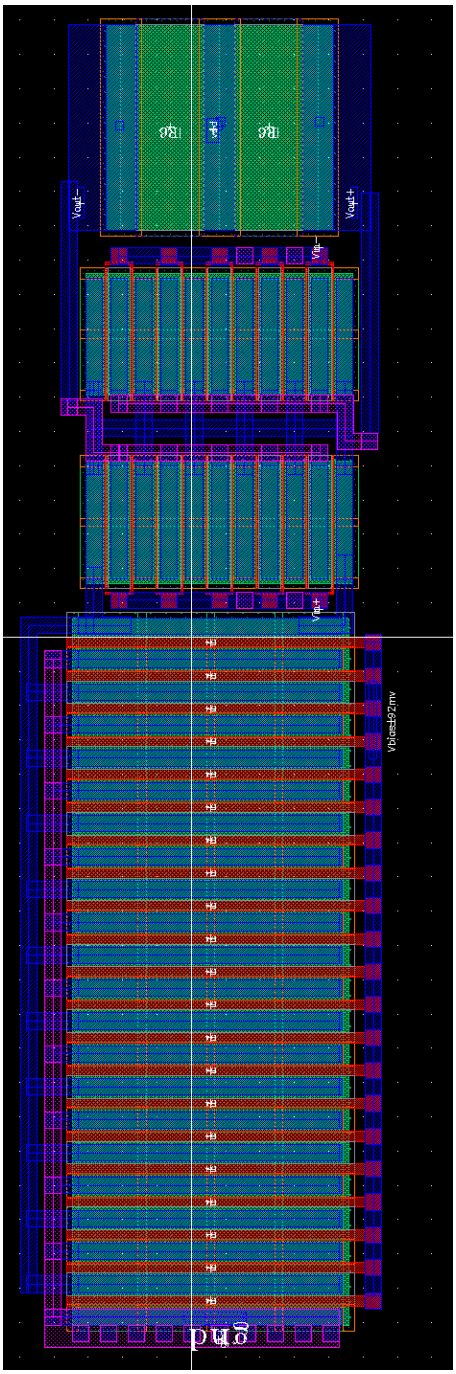


Figure 3.49: Layout VCO to Mixer Output Buffer

3.9.3 VCO to Prescaler Buffer

It is important to use a full swing VCO to Prescaler buffer, as shown in Figure 3.50, to ensure that the digital frequency divider can count each period. A series of gain buffers

similar to the VCO to mixer buffer were used; each stage separated by a common mode isolation stage. The first three buffers, Gain 1-3 from Figure 3.51, were designed using the methodology detailed in chapter 3.9.2 , Figure 3.48. Figure 3.50 was designed to amplify the previous stages to near full swing with the added inverters, Figure 3.57, finally bringing the buffer to full swing. Transistor sizes and device layouts are shown in the figures below.

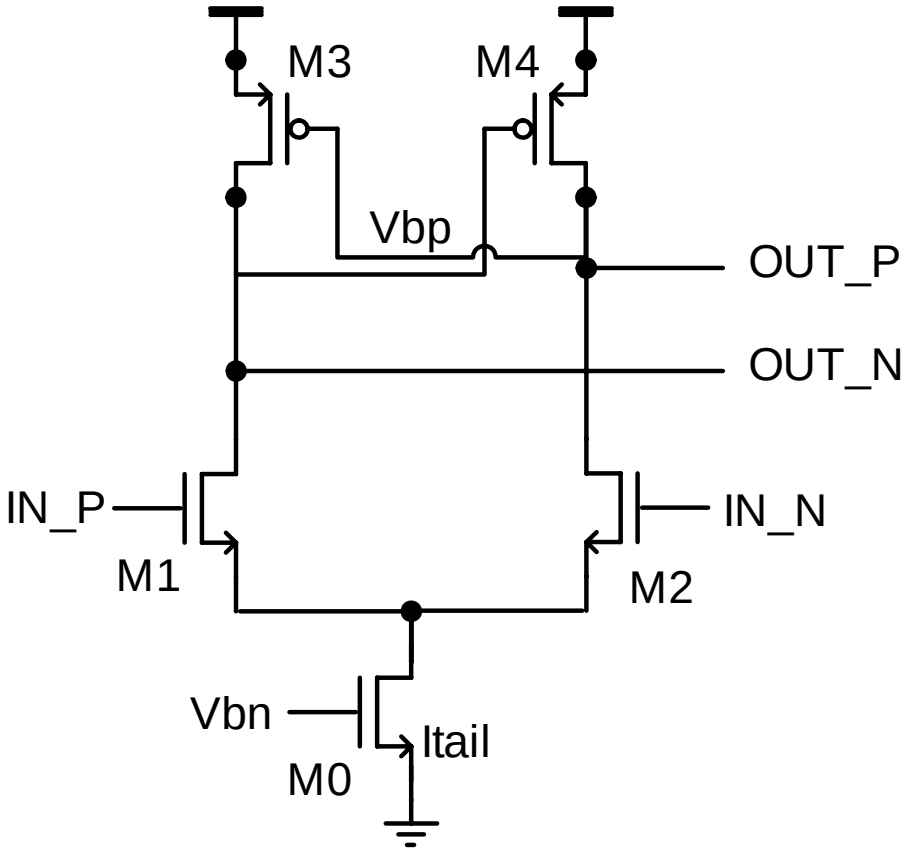


Figure 3.50: Full swing Buffer

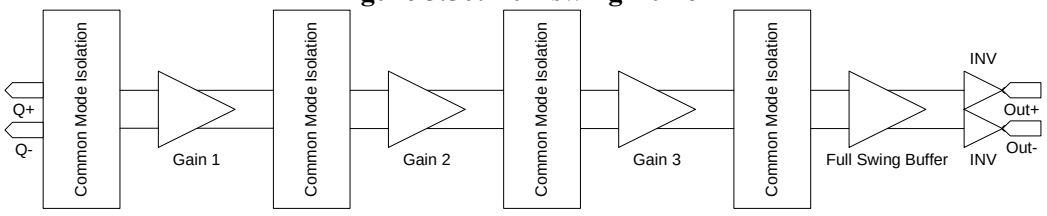


Figure 3.51: VCO to Prescaler Full Swing Buffer Chain

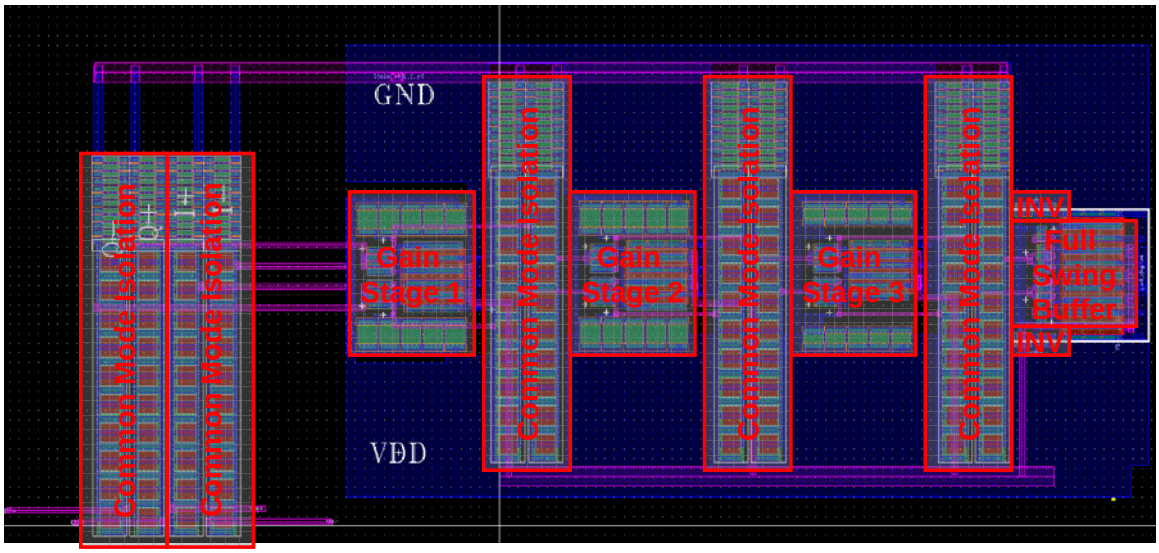


Figure 3.52: Layout of Prescaler Buffer as a whole

Table 3.15: Gain Stage 1

Component	Values
Tail Transistor (M0)	W=25µm,L=3.15 µm,Fingers=5
M1,M2	W=10 µm,L=.350 µm,Fingers=3
Resistive Load (pwell Resistor)	25K ohm
Itail	.17mA

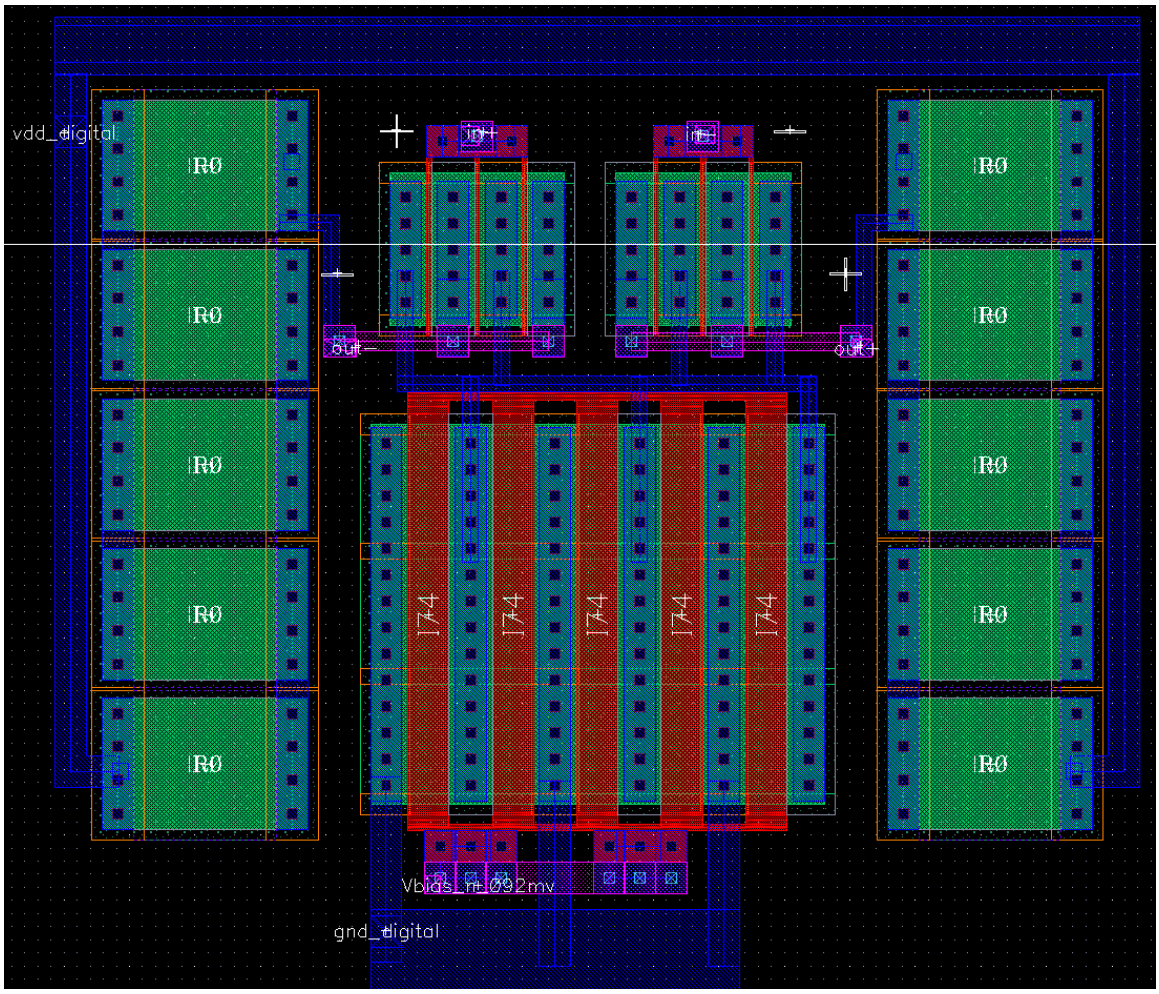


Figure 3.53: Layout of VCO to Mixer Buffer Gain Stage 1

Table 3.16: Gain Stage 2

Component	Values
Tail Transistor (M0)	W=25µm,L=3.15 µm,Fingers=5
M1,M2	W=10 µm,L=.350 µm,Fingers=3
Resistive Load (pwell Resistor)	25K ohm
Itail	0.245mA

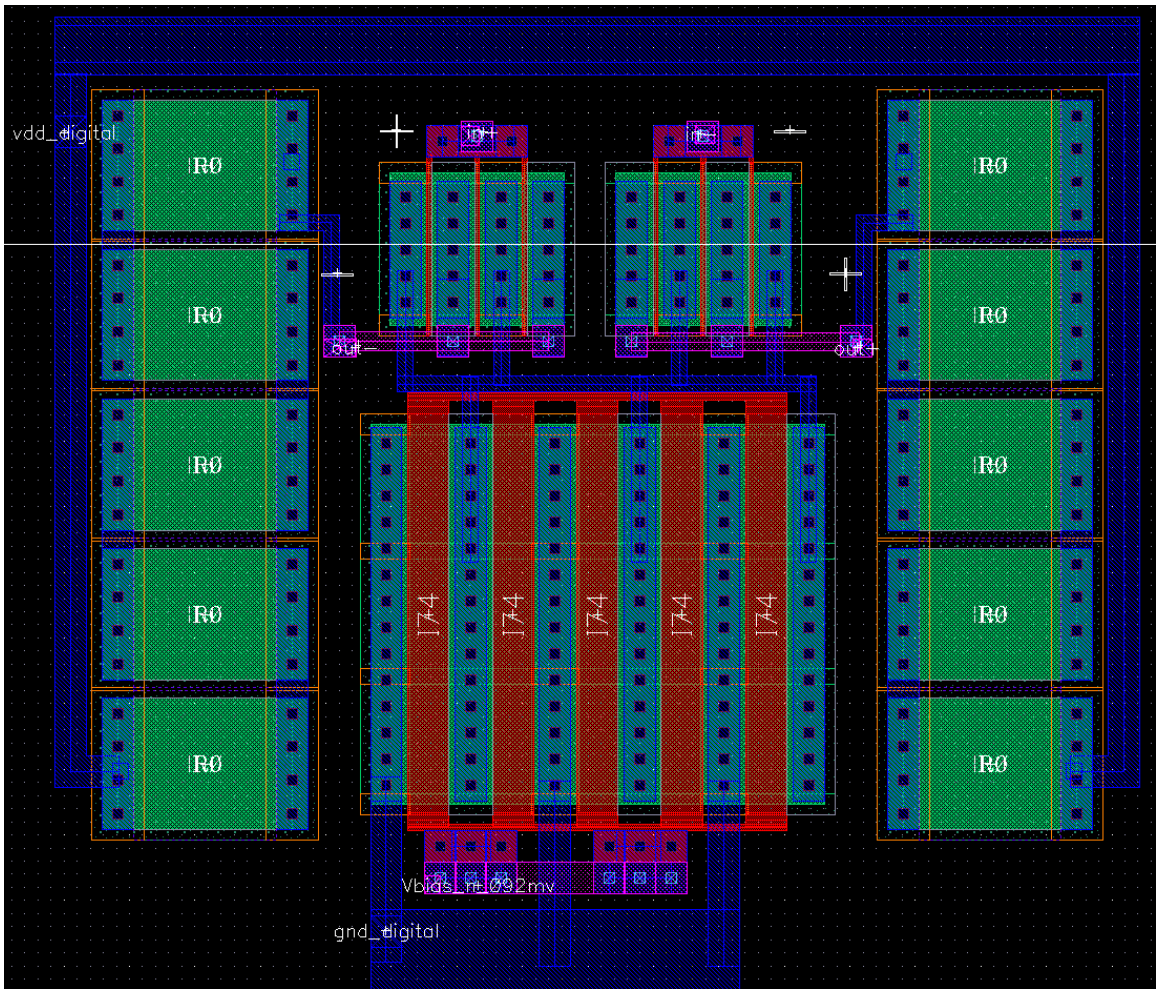


Figure 3.54: Layout of VCO to Mixer Buffer Gain Stage 2

Table 3.17: Gain Stage 3

Component	Values
Tail Transistor (M0)	W=25µm,L=2µm,Fingers=5
M1,M2	W=10 µm,L=.350 µm,Fingers=3
Resistive Load (pwell Resistor)	12K ohm
Itail	.245mA

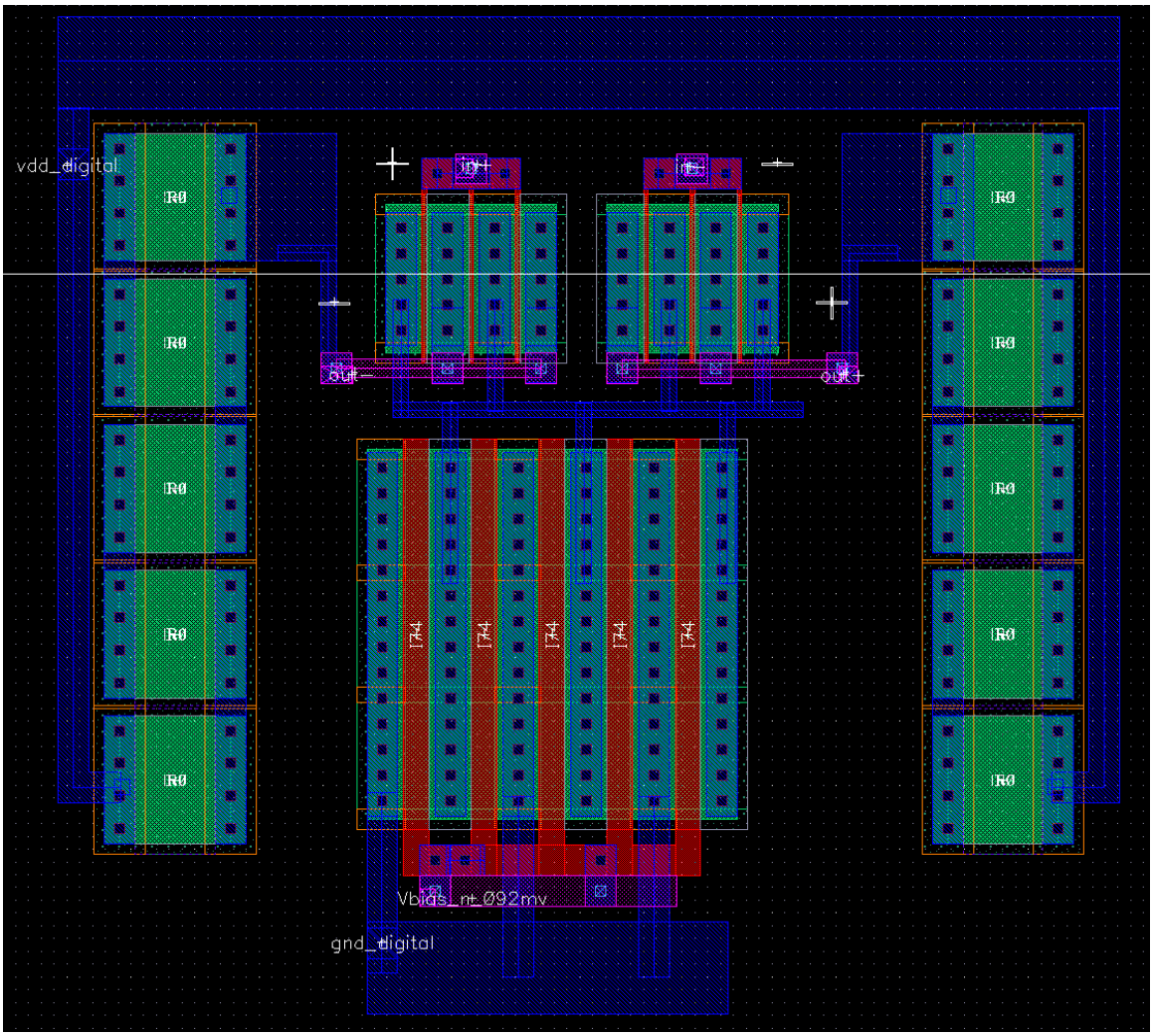


Figure 3.55: Layout of VCO to Mixer Buffer Gain Stage 3

Table 3.18: Full Swing Buffer Transistor Sizes

Component	Values
Tail Transistor (M1)	W=25µm,L=3.15 µm,Fingers=10
M1,M2	W=4.5 µm,L=.350 µm,Fingers=3
M3,M4	W=2 µm,L=.350 µm,Fingers=1
Itail	.265mA

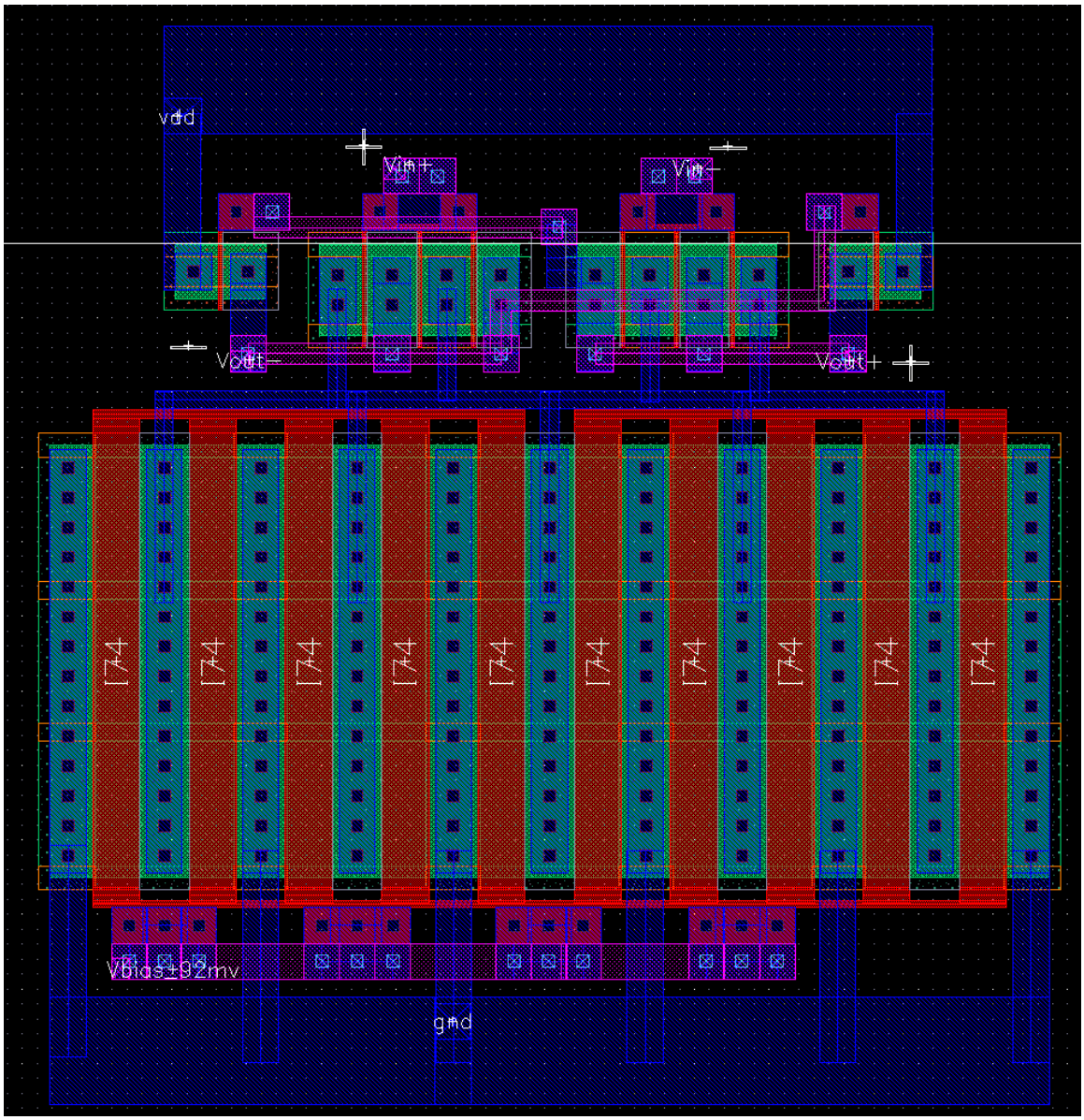


Figure 3.56: Layout of VCO to Mixer Full Swing Buffer

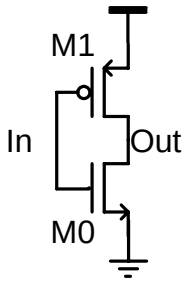


Figure 3.57: INV

Table 3.19: INV Transistor Sizes

Component	Values
M0	W=6μm,L=.5 μm,Fingers=1
M1	W=6μm,L=.5 μm,Fingers=1

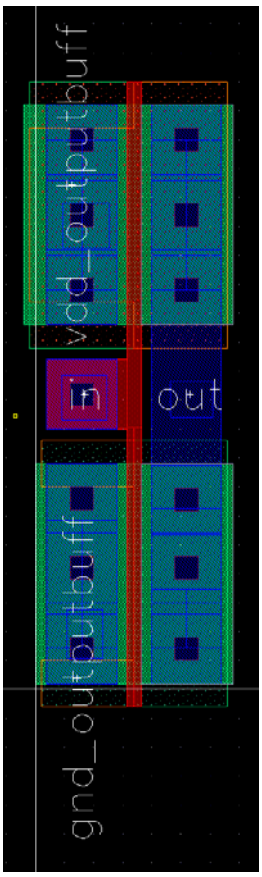


Figure 3.58: Layout of VCO to Mixer INV

3.10 PLL System Analysis

3.10.1 Text Book Analysis

A PLL needs to be analyzed as a whole system, as shown in Figure 3.4, to ensure stability since they are based on feedback. The contribution of the system as a whole, PFD/Loop Filter/Charge Pump/VCO, can be described in a Laplace transform as Equation 3.23.

$$G(s) = K_{\text{chargepump}} \; F(s) \frac{\Phi_{out}(s)}{V_{control}(s)}$$

Equation 3.23

Substituting from Equation 3.2 and Equation 3.8; Equation 3.23 can be rewritten as Equation 3.24.

$$G(s) = \frac{I_P}{2\pi} \frac{1}{C_p s} \frac{K_{VCO}}{s}$$

Equation 3.24

The general closed-loop transfer function, which includes the effect of the Prescaler, is expressed as Equation 3.25.

$$H(s) = \frac{G(s)}{1 + \frac{G(s)}{N}}$$

Equation 3.25

The closed-loop system equation is then expressed as Equation 3.26.

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi C_P}}{s^2 + \frac{I_P K_{VCO}}{2\pi N C_P}}$$

Equation 3.26

From Equation 3.26, it is noted that the closed-loop system contains two imaginary poles expressed in Equation 3.27.

$$s_{1,2} = \pm\sqrt{\frac{I_P K_{VCO}}{2\pi N C_P}}$$

Equation 3.27

These poles will cause the system to be unstable because of the two poles at the origin; this means that the combined PFD /Charge Pump/Loop Filter and VCO are two ideal integrators. When the Phase and Magnitude response are plotted, Figure 3.59(a), each of these integrators contribute a constant phase shift of 90^o, giving a constant 0^o Phase margin, which in turn allows the system to oscillate at the gain cross over frequency. The goal is to modify the phase characteristic, so that the phase shift is less than 180^o – which will cure our instability problem. The pole is shifted by adding a resistor in series with Cp, as shown in Figure 3.30. The adjusted pole will cause the PLL to have a phase margin greater than 0^o by adding a zero to the system. The new open-loop transfer function is plotted in Figure 3.59(b), and the amended open-loop system equation now becomes Equation 3.28.

$$H(s) = \frac{\frac{I_P K_{VCO}}{2\pi N C_P}(R_P C_P + 1)}{s^2 + \frac{I_P K_{VCO} R_P}{2\pi N} + \frac{I_P K_{VCO}}{2\pi N C_P}}$$

Equation 3.28

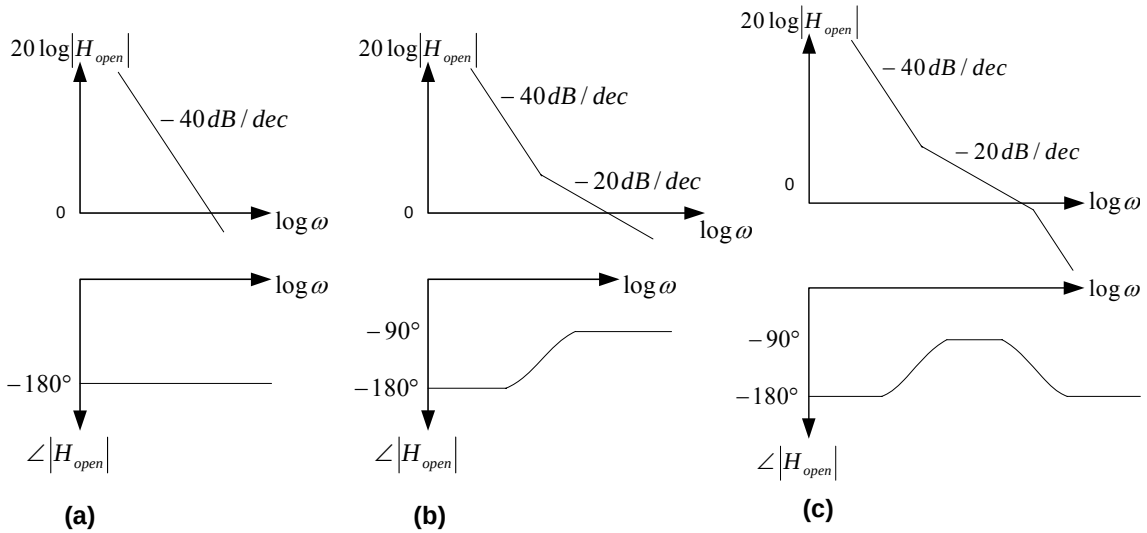


Figure 3.59: (a) Phase and Magnitude response for a 1 pole, (b) a phase margin modified 1 pole PLL, and (c) a phase margin modified 2 pole. [7]

As discussed in 3.6 , it is common practice to insert a ripple reduction capacitor; C_2 in Figure 3.31. However, as noted that in adding a second pole, we change our loop filter from a first order to a second order loop filter. A second order Loop filter, where C_2 is between 1/5 and 1/10 of C_P, has a Phase and Magnitude response of Figure 3.59(c). If C_2 is not in this range, then the loop filter can become unstable. This is further discussed in [cite] and is deemed outside the scope of this discussion.

Since a value of C_2 was chosen inside the range where it can be neglected from the System Design Equations, the system can be approximated as a second order PLL, there are some other important system performance parameters. The natural frequency (ω_n) the damping factor (ζ_n) , and the Loop Bandwidth (K_{loop}) are given as Equation 3.29, Equation 3.30, and Equation 3.31; respectively.

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi N C_P}}$$

Equation 3.29

$$\zeta_n = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi N}}$$

Equation 3.30

$$K_{loop} = 2\zeta\omega_n = \frac{R_P K_{\text{chargepump}} \quad K_{VCO}}{N}$$

Equation 3.31

3.11 ADS Computer Analysis

The equations given in Chapter 3.10.1 give an adequate hand analysis for constructing the system. However, in practice it is easier to facilitate design by the use of available software. The stability of the PLL system was designed by using iterative design in ADS. By using the Design Guide PLL menu, it was possible to use a template for the PLL design. The template is designed using a PLL configuration wizard, where the components of the PLL and the order of the system can be selected. This wizard facilitated the design process by allowing a quick iterative design process where one could simulate the stability of the system, check to see if the PLL design would indeed lock, tune the charge pump current, tune the loop filter, and check the loop bandwidth. Figure 3.60, Figure 3.61, and Figure 3.62 show that the PLL indeed locks the desired frequency. Figure 3.63 shows system stability and bandwidth of the loop filter. The system stability is shown by inspecting where the magnitude crosses the unity gain, or zero crossing. The system is stable because it achieved more than our 45^o minimal requirement.

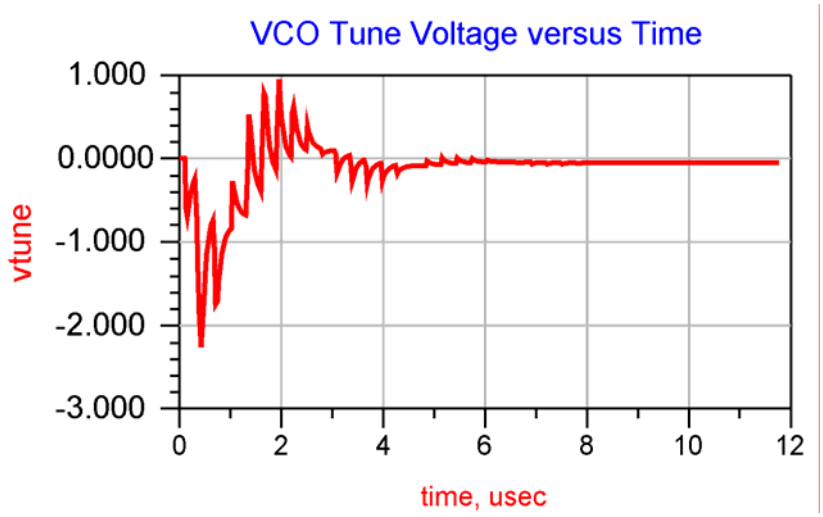


Figure 3.60: Vcontrol voltage when PLL is unlocked to locking at desired frequency

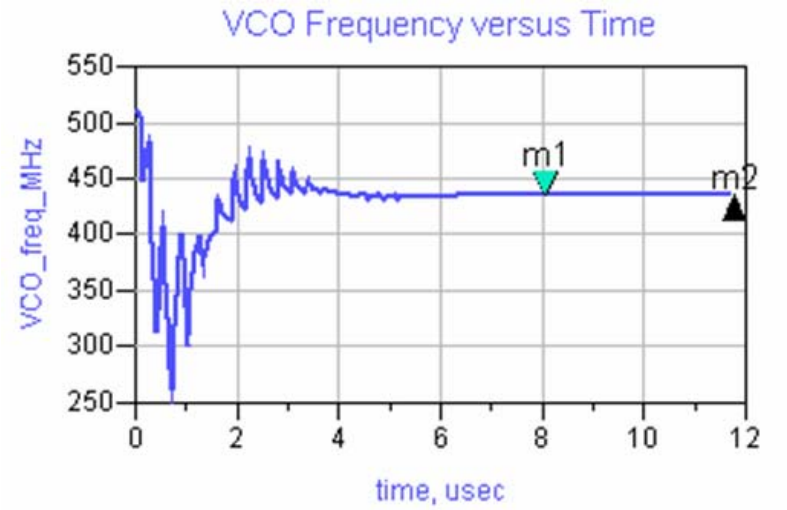


Figure 3.61: VCO Frequency when PLL is unlocked to locking at desired frequency

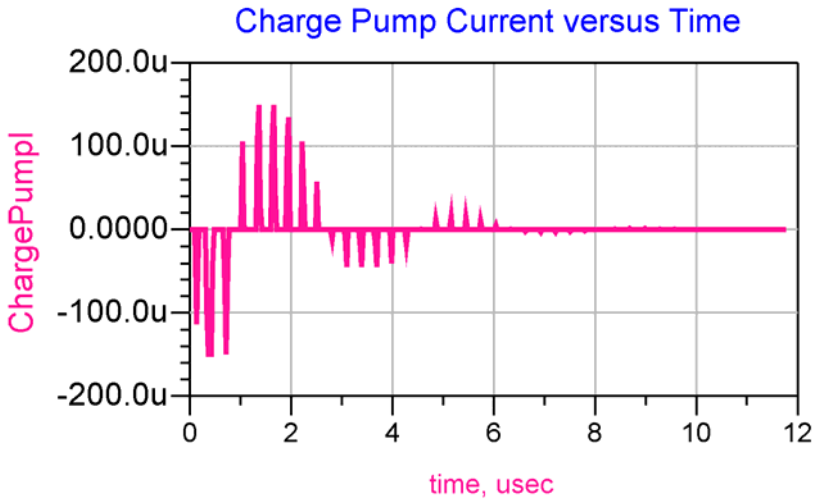


Figure 3.62: Charge pump current when PLL is unlocked to locking at desired frequency

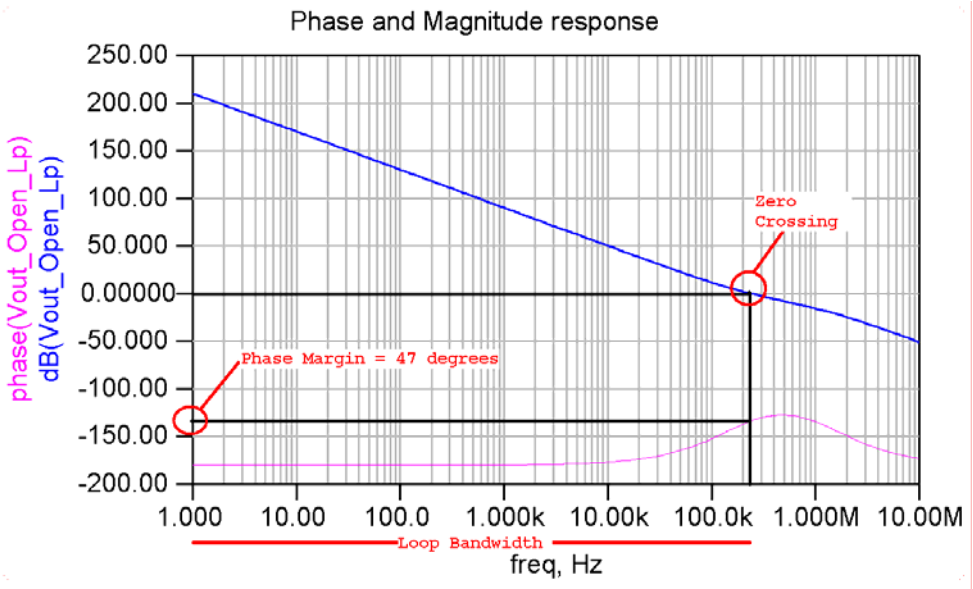


Figure 3.63: Phase and Magnitude response of the implemented loop filter

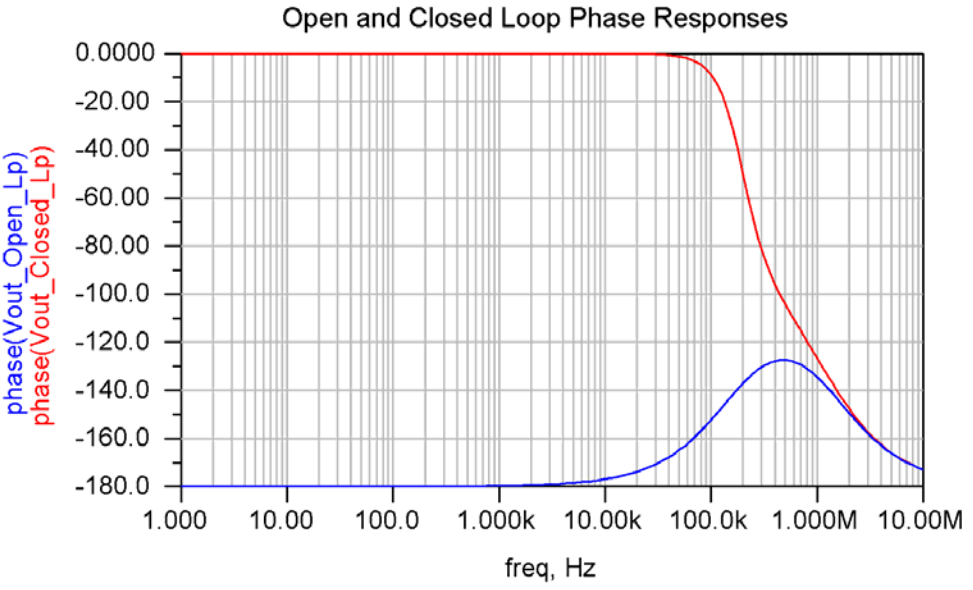


Figure 3.64: Open and Closed Loop Phase response of the system

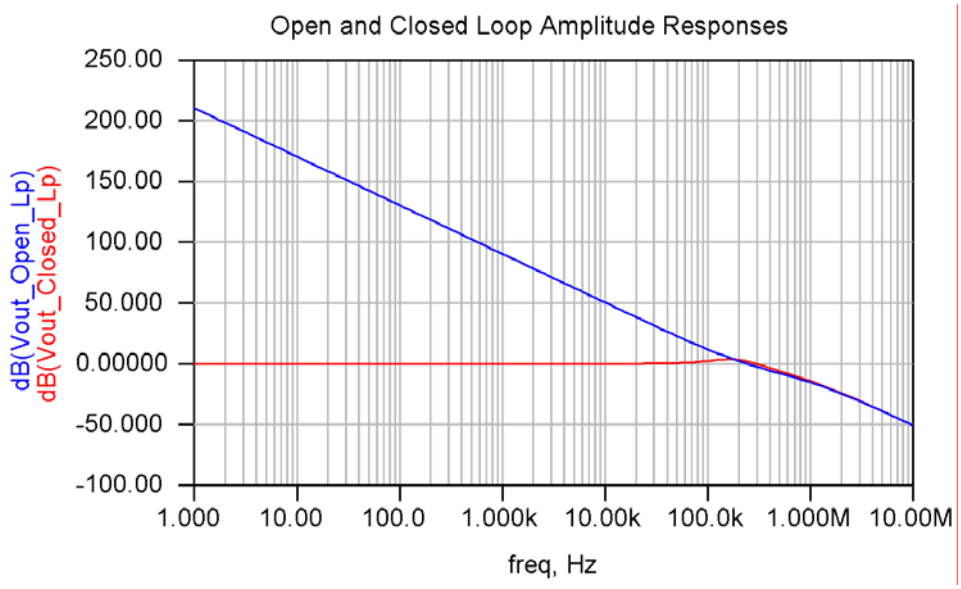


Figure 3.65: Open and Closed Loop Amplitude Responses.

3.12 Layout

The PLL was designed to fit in a 2.46mm X 2.26mm space, as shown in Figure 3.66. Decoupling capacitance was used to fill every available μm of the chip to help reduce noise on the power and ground lines. Each of the four varactors were laid out as close as possible to each other. Laying out the varactor in this manner helps reduce the effects due to x or y axis process variation. The inductors were laid out in such a way that it would be easy to make the interconnecting lines the same length. This helps to ensure that the VCO sees the same wire capacitance and resistance from the wires.

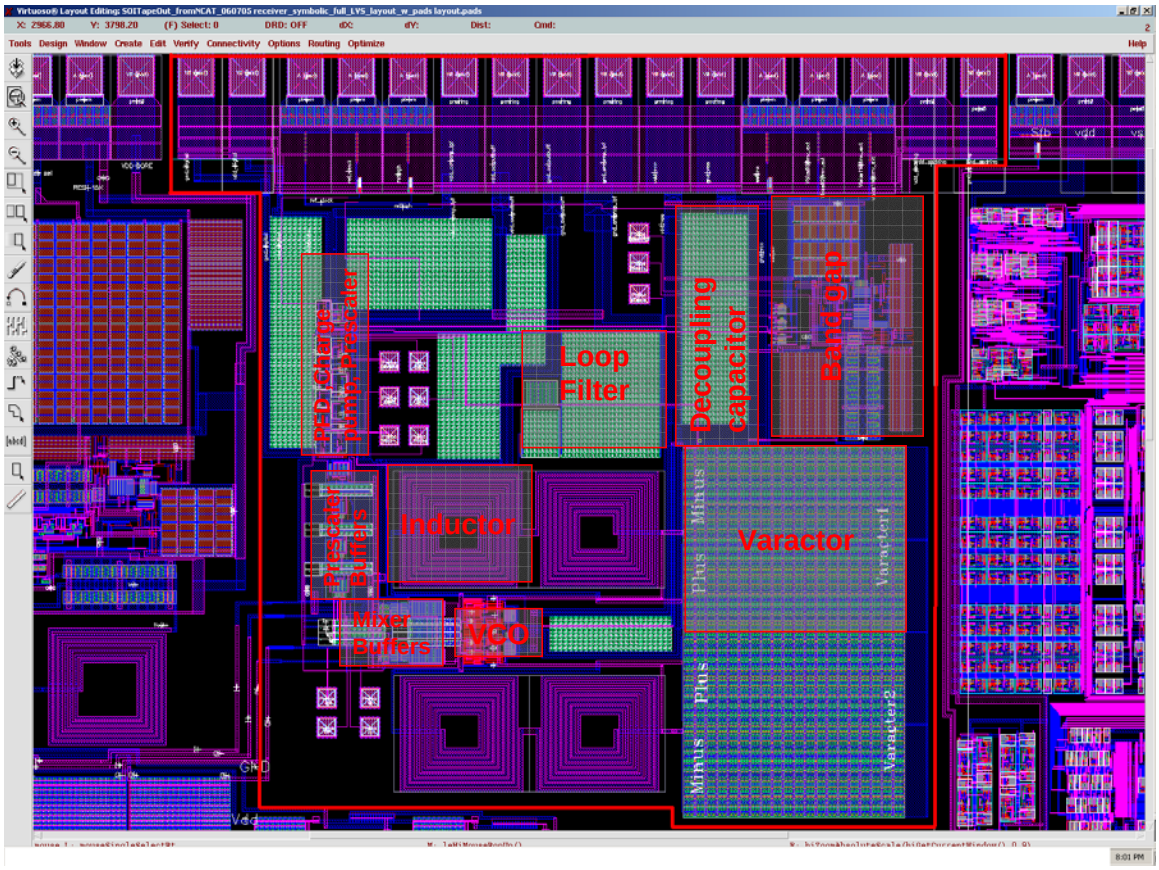


Figure 3.66: Layout of 435MHz PLL

3.13 Designing for Test Methodology

The PLL system was fabricated in order to facilitate stand alone testing in case of circuit performance issues. A major performance issue would occur if the PLL did not lock. To combat this, micropads were inserted in the layout to give incite to potential short comings of the system through use of a high impedance probe. These micropads, as shown in Figure 3.67, were inserted for the Quadurature output of the VCO, Prescaler (divide by 2 and divide by 64), PFD (UP_ and DOWN_), Vtune (VCO control Voltage), the 920mV and 1.1V bandgap reference, and inputs to the Prescaler (VCO+ and VCO-). The chip also has the ability to select an off chip bandgap reference voltages for the VCO, Output buffers, and Charge Pump (each independently). With all of these

micropads and selectable, through use of a multiplexer shown in Figure 3.68, bandgap reference voltages the PLL should, in the worse case scenario be able to be tweaked into working. However, there is high confidence that this design will work successfully, as the parasitic extracted fully loaded PLL has been simulated successfully.

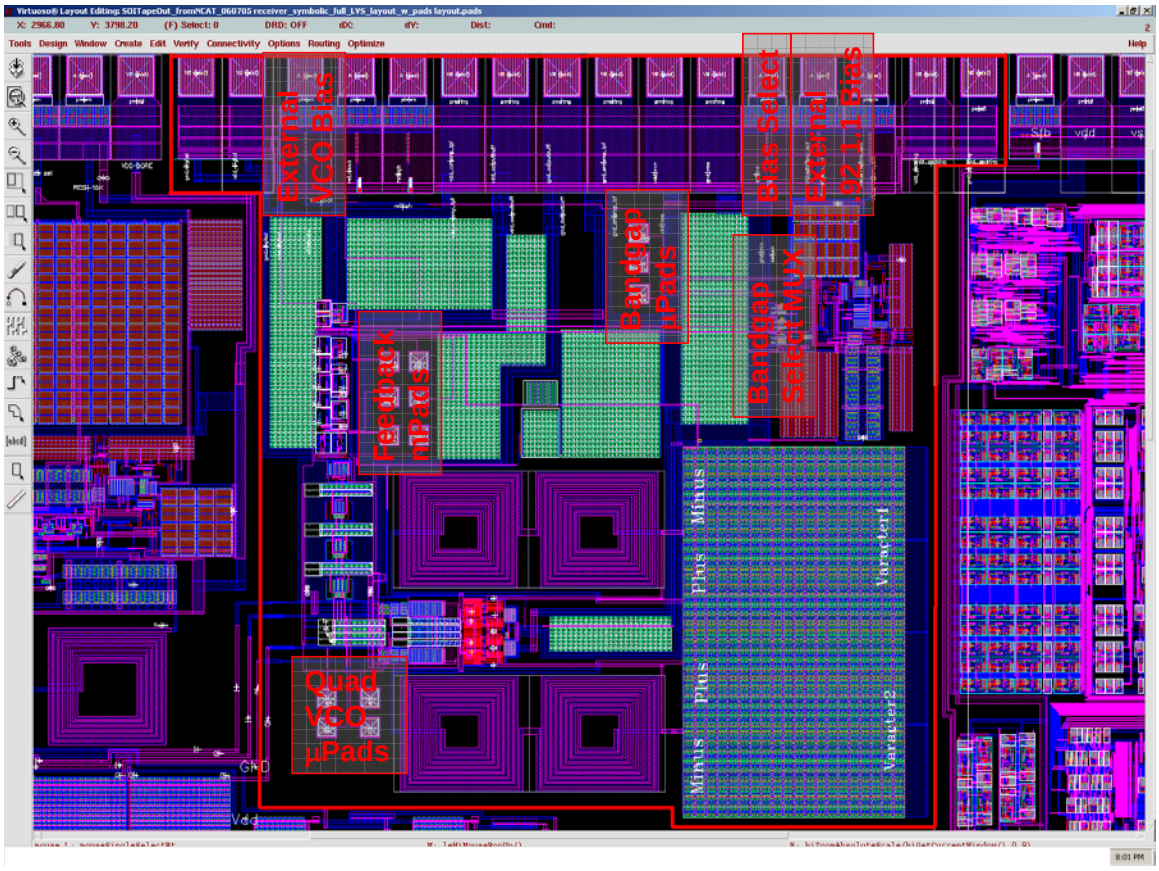


Figure 3.67: Micropads and Design for test components

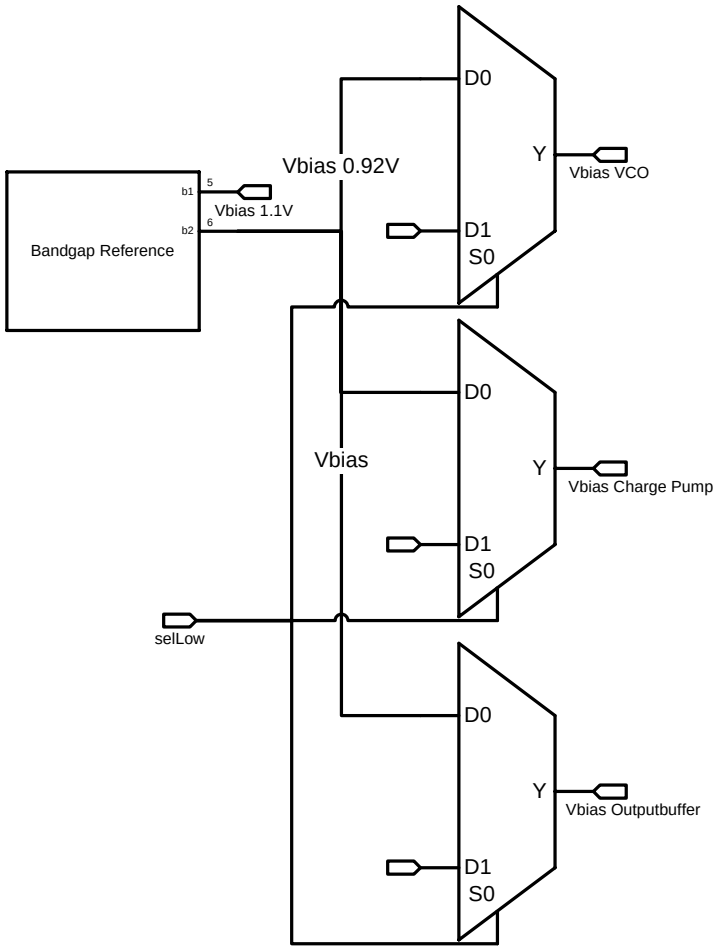


Figure 3.68: Bandgap Reference Multiplexer Block Diagram

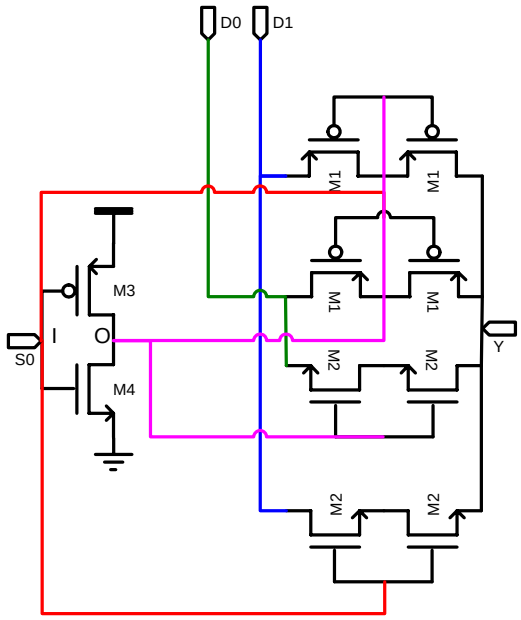


Figure 3.69: Bandgap Reference Multiplexer Schematic [11]

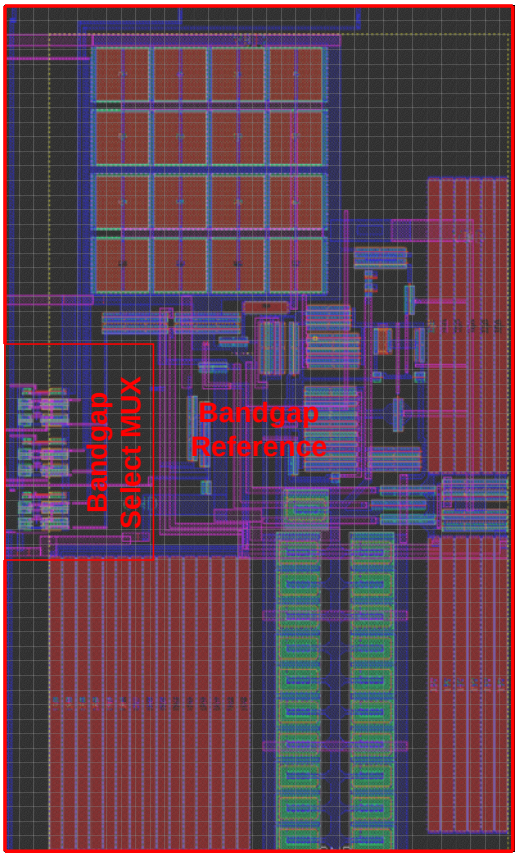


Figure 3.70: Bandgap Reference Multiplexer Layout

Table 3.20: Bandgap Reference Multiplexer Transistor Sizes

ITEM	M	F	W (um)	L (um)
M1	1	1	19.8	0.5
M2	1	1	8	0.5
M3	1	1	11.2	0.5
M4	1	1	4.4	0.5

Chapter 4 Results

The final design performance can only be analyzed by simulation results currently. There were two simulation programs used; ADS and Cadence. While ADS is a good system level design tool, our model files and layout tools are for Cadence. First, each component was generated in a stand alone format and analyzed to ensure proper operation using Cadence. Details on the proper operation of these components are outlined in their chapters:

- 128-bit Divider – 3.3
- Phase & Frequency Detectors – 3.4
- Charge Pump – 3.5
- Loop Filters – 3.6
- Voltage Controlled Oscillator – 3.7
- Output Buffers – 3.9

Next, each component was hooked up into a system level block diagram, schematics only. The sources in the system level diagram were defined and hooked up to complete the system. Finally, the device was simulated using the Cadence Analog Environment. At first glance, the PLL seemed to not work, as shown in Figure 4.1. The question was "what is wrong with the PLL?" To find this out, each physical block was evaluated using a stand alone test bench. All components worked to spec. So why didn't the PLL work at the system level? To isolate the problem a VerilogA representation of the PLL was implemented. Using the hierarchy editor in Cadence, you can replace any functional block with a mathematical model, extracted circuit, or schematic. After the VCO was replaced with the VerilogA model in the system level simulation, the PLL locked as

shown in Figure 4.2. What this showed is that the problem was in the interface to the VCO. It was discovered that the problem was found in the schematic version of the VCO. A wire was incorrectly connected to the system level block diagram. Once this problem was identified and fixed, the system locked. Bond wire inductances were then added to the system and simulated, as shown in Figure 4.3 and Figure 4.4.

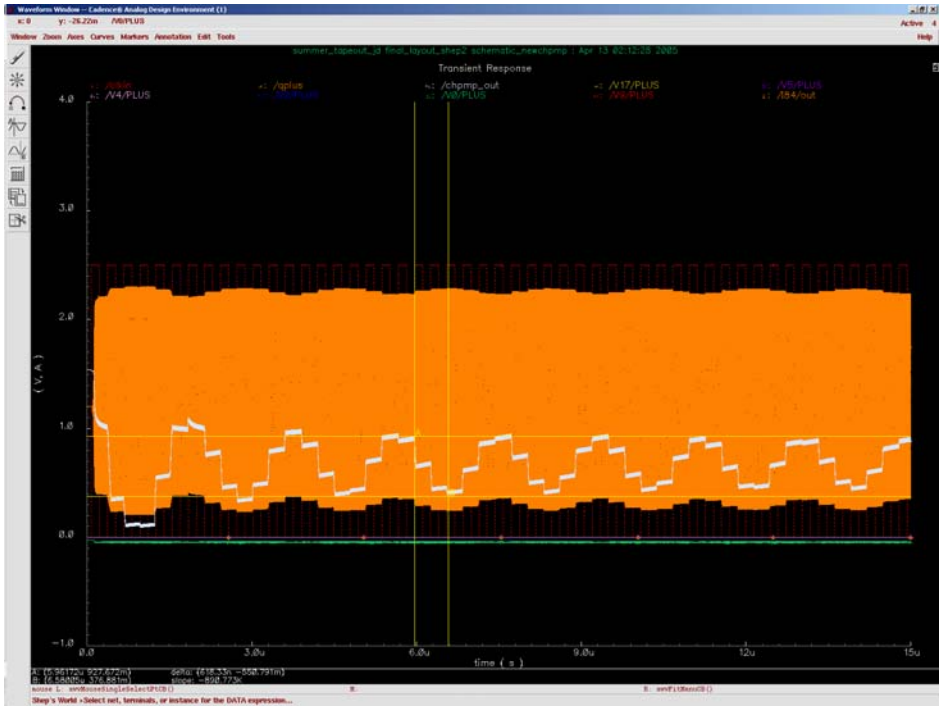


Figure 4.1: Not Locking PLL

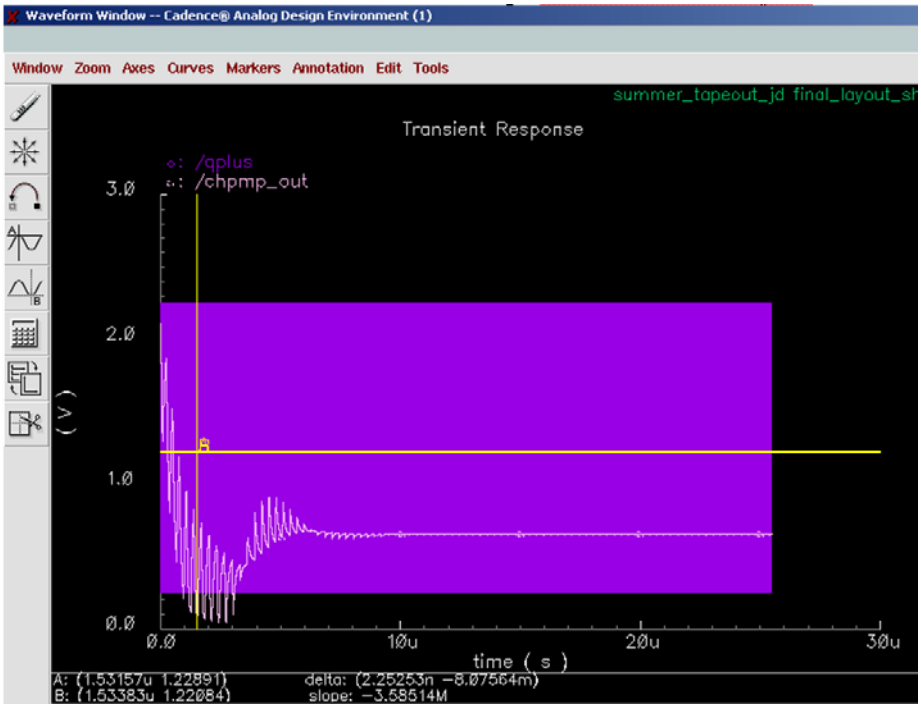


Figure 4.2: Locking PLL with VerilogA Modeled VCO

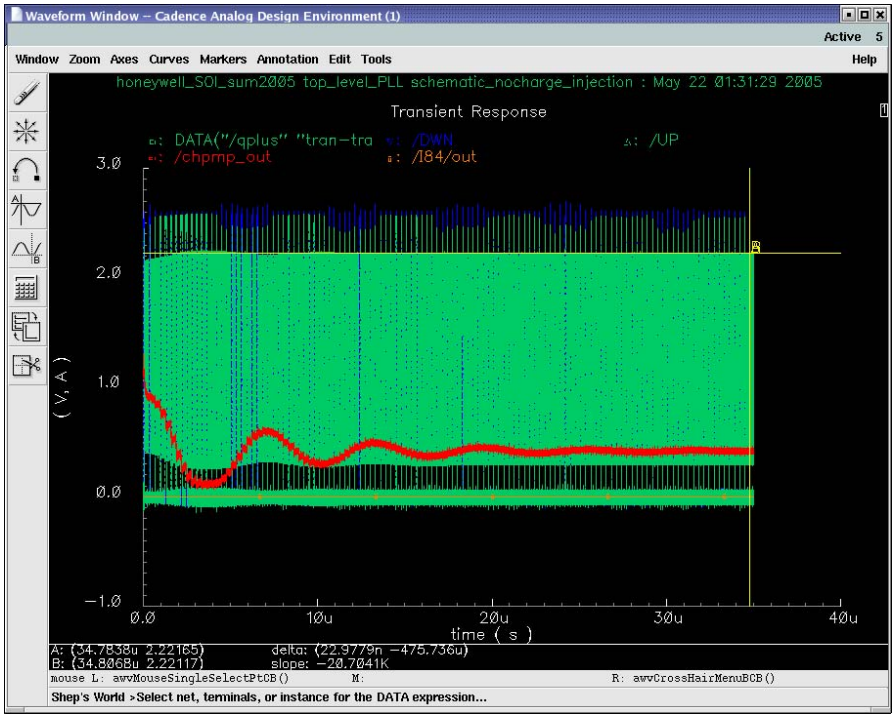


Figure 4.3: Locking PLL with switching noise reduced charge pump w/ inductors 2nh

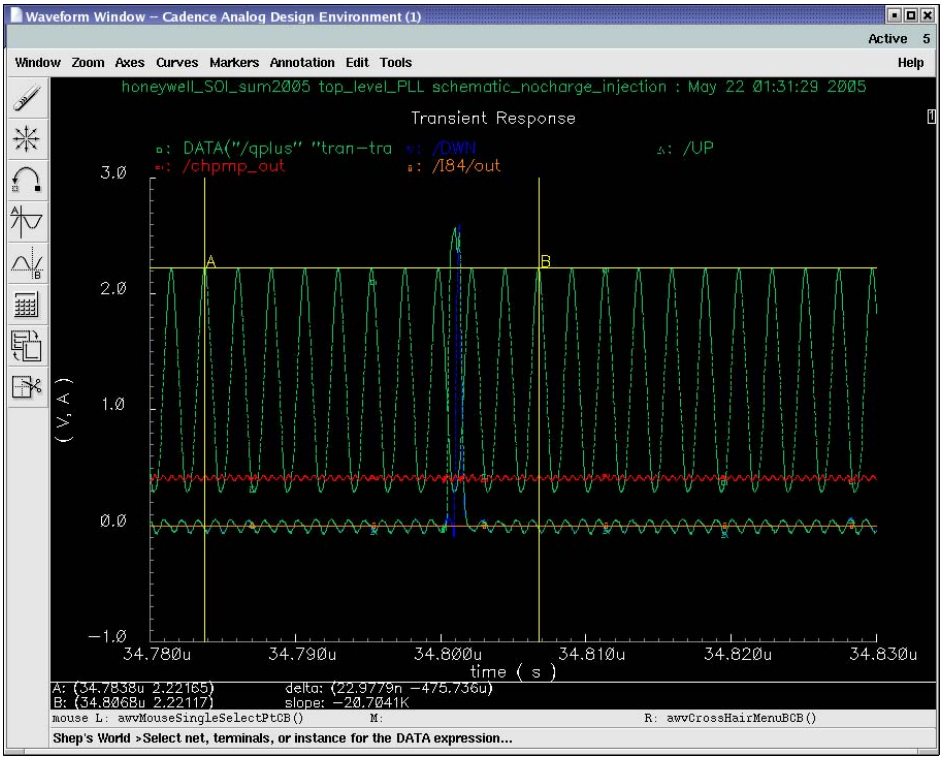


Figure 4.4: Locking PLL with switching noise reduced charge pump w/ inductors 2nh

Once the schematic versions with bond wire inductances locked and the PLL was optimized for lower power performance – this was achieved by adjusting buffer tail current sizes and looking for redundant circuitry to eliminate – the layout stage of the system began.

Each sub-block, which is a smaller component such as a DFF or Logic cell of a larger component block such as a Divider or PFD, was then laid out and extracted with parasitic capacitances and resistances. They were then verified on the stand alone test bench using the hierarchy editor to select the use of a extracted component instead of a schematic. Next, the system level simulation was run with the extracted building blocks. This enabled us to identify the location of the weak points in the PLL System before laying out the entire system. Once the system was working with the extracted versions of the building blocks, we began to increase the size of these building blocks to component

blocks (i.e. PDF, Charge Pump, VCO, etc) and then repeated the simulations and tweaked the components were needed. By building the system incrementally, it enabled us to build the system until a component failed and to address the issue while it was easily addressable. See Chapter 3.2.2 for more indepth details on the implementation.

Chapter 5 Conclusions

5.1 Contributions of this work

This design was an improvement on a previous design fabricated. The power consumption was decreased from 144mW to 15mW; which power was the key benchmark of the PLL circuit. Other contributions of this work include introduction of common mode isolation, design for test methodology, and Spice validated results. This circuit will provide a solution for generating the carrier frequency of the 435MHz Double Differential Phase Shift Keying (DDPSK) Transceiver.

5.2 Future work

It is a known fact that circuit simulations are only as good as the device models. In designing for extreme environments, a major problem is obtaining suitable device models. The commercial range is from -55^{o}C to 150^{o}C, and we need to research alternatives for ranges of -230^{o}C to 180^{o}C and beyond. During a preliminary research phase of extreme environment circuits, the question gave rise to just how accurate are the commercial models over temperature and still have acceptable deviations. By comparing the measured low temperature and high temperature MOSFET device data to the model, we noticed an intolerable amount of deviation. This indicated that in fact the commercial models are not accurate enough; compare Figure 5.1 and Figure 5.2.

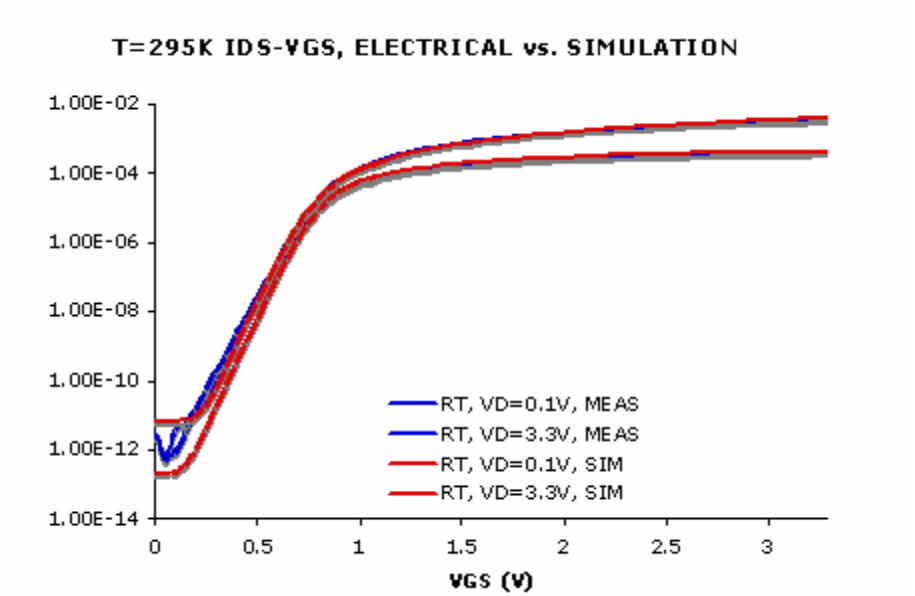


Figure 5.1: Room temperature Simulated vs. Modeled NMOS Device [11]

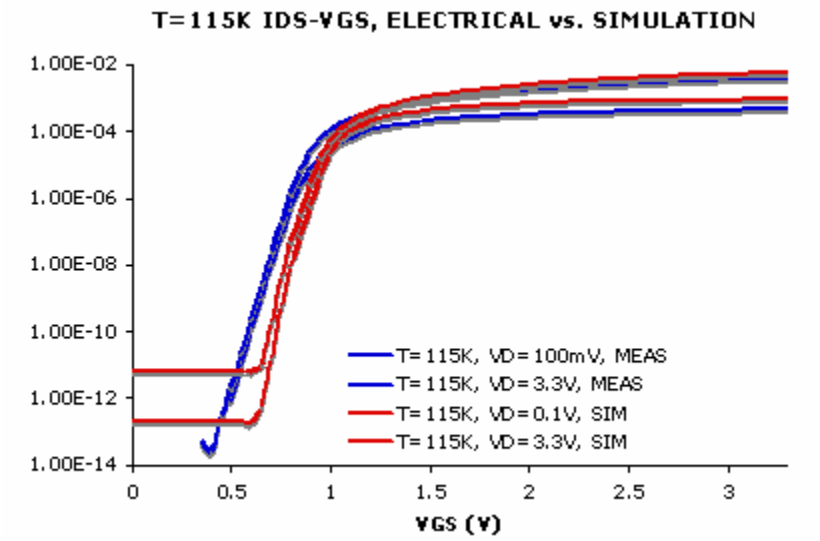


Figure 5.2: -158°C Simulated vs. Modeled NMOS Device [11]

A unique property of SOI devices, is the access to a devices bulk connection, as discussed in Chapter 1. Using this bulk connection, it was proposed that circuits could be adjusted to work over wide temperature ranges. The VCO from the thesis research was used in an initial investigation to validate if, in fact, we could use the bulk connection as a "knob" to adjust the circuits performance over temperature with our commercial

models. The device models have not been adjusted to accurately represent the transistors behavior over extreme temperatures.

The initial investigation seemed promising. Figure 5.3 shows a trend of body biases that keep the VCO operating with a minimum frequency of 400MHz to a maximum frequency of 500MHz, with amplitude of at least 100mV. However, there were some questions brought up about if the effects that were noticed as the temperature dropped were induced by an inaccurate model. These effects appear as a lower frequency amplitude oscillation, in addition to the correct frequency oscillation; Compare Figure 5.4 and Figure 5.5. An initiative was then set in motion to answer the question: "Is this model accurate enough to give high confidence in the results?"

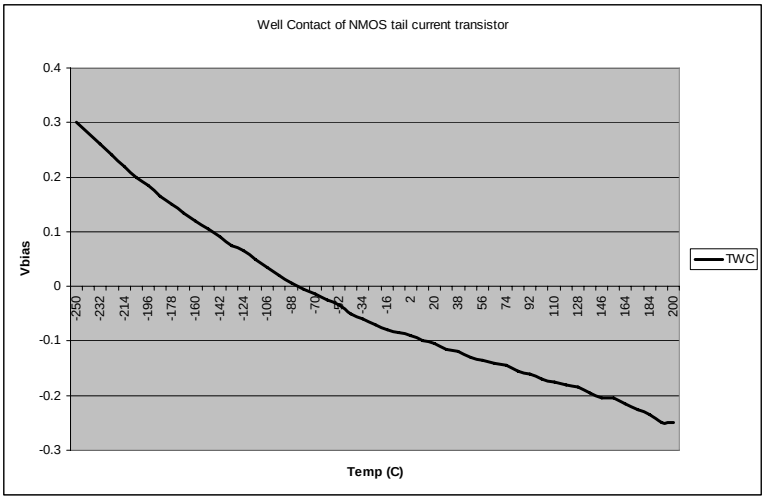


Figure 5.3: The NMOS well contact potential that allows the VCO to operate to spec. over temperature

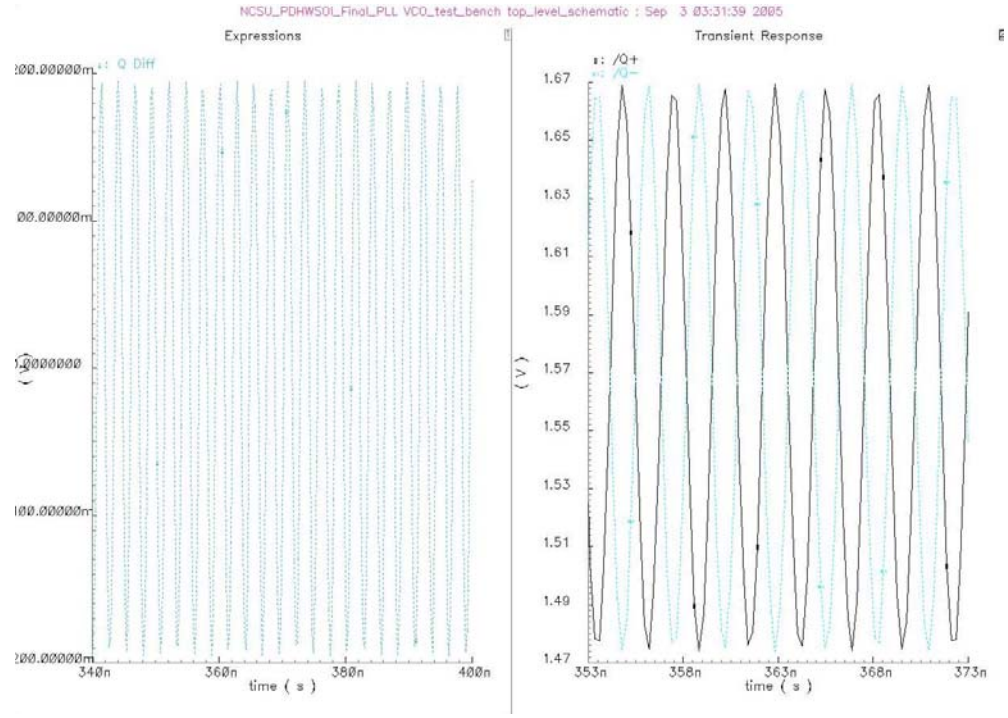


Figure 5.4: VCO operation at normal temperature with no body bias

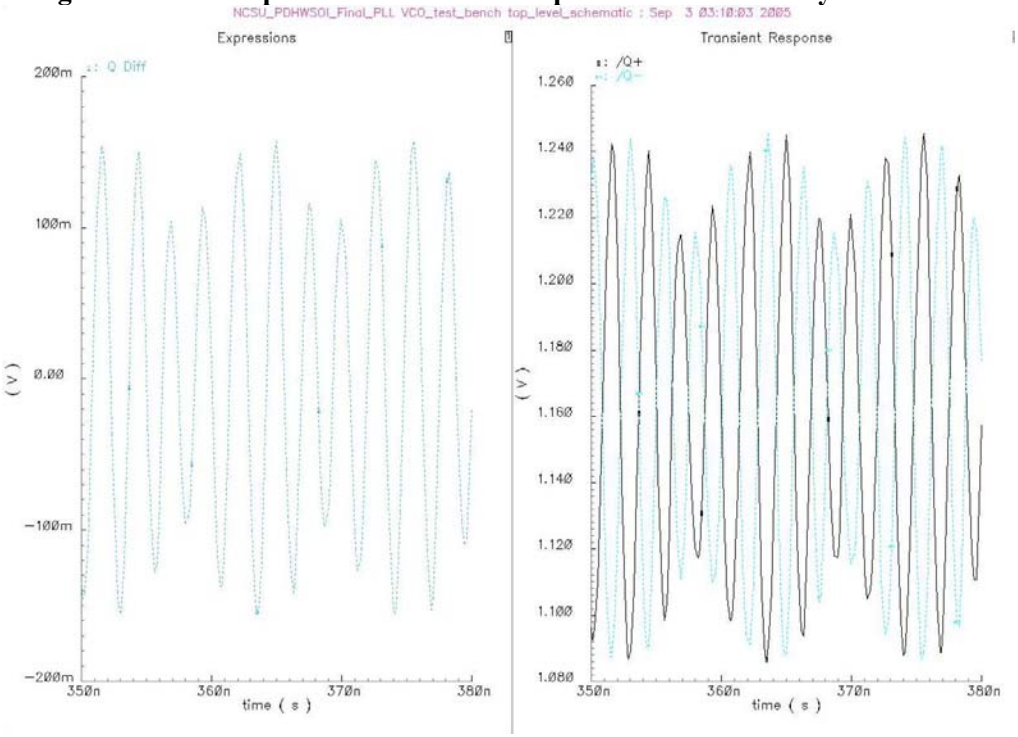


Figure 5.5: Figure 3: VCO operation at -250°C with body bias

Next, the decision was made to try and get some preliminary data that would lead to the ability to correctly model devices over the entire extreme temperature range. However, the method used for extracting key parameters really requires a different set of test

structures than previously fabricated. In an effort to use these devices for characterization and to avoid fabricating an additional set of test structures, it was decided to see if the current data could be salvaged. After gathering the raw data for the devices at low and high temperatures (-158^{o}C to 200+^{o}C), the phi and gamma variables were solved for. A problem was noticed that the nonlinear regression models available in Excel, SigmaPlot, etc for solving nonlinear equations were, in effect, "railing" out to several of the upper and lower bound constraints to the point of being "unphysical." After careful consideration and consulting some colleagues with a strong affinity for statistics, it was determined that there are other methods that can be used to solve such problems.

This led to further exploration of an algorithm called the "Complex Method of Box.[12,13]" The purpose of the Complex Method of M. J. Box is to solve a multivariable constrained nonlinear function with linear and/or nonlinear inequality constraints. This is accomplished by finding the maximum of an error function. In this case, the negative sum of differences squared is used. Basically, the function is solving for the values of the variables that give the sum of differences squared closest to zero. The method uses a sequential search to solve nonlinear functions, and requires no derivatives of the functions.

The Complex Method of Box randomly seeds the initial "guesses" for the variables with random numbers within the given constraints of that variable. The method has been best described as a multidimensional ameba, that looks around the maximizing function and starts to converge on a solution. However, since the initial parameter matrix covers the entire range of acceptable values (given the constraints), it tends to find the global maximum.

The future is looking bright from the research obtained thus far. From the data that has been gathered and the statistical tools that have been used, there are strong hopes of developing a model that will facilitate the development of an extreme temperature Phase Lock Loop device.

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