ABSTRACT

JASPER, DAVID BRIAN: RF pHEMT Switch Model for Multiband Cell Phone Circuits. (Under the Direction of Dr. Douglas Barlage)

Simulation of Radio Frequency Switches used in the cellular phone industry is the main focus of this study. The RF pHEMT's used in an antenna switch for multiband cell phone circuits requires the use of an accurate model during simulation of the RF system. The pHEMT model extracted in this study utilizes theoretical methods within the extraction software and an analysis of simulated data and measured data. This study describes the techniques of calibration, model extraction, and data analysis.

RF pHEMT Switch Model for Multiband Cell Phone Circuits

by

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I dedicate this thesis to my parents and family

Biography

David Brian Jasper was born on February 1, 1980 in Greenville, North Carolina. He attended elementary and secondary school in Greenville, graduating from J. H. Rose High School in Greenville. He was accepted into North Carolina State University in 1998 where he earned his Bachelor of Science degree in Electrical Engineering in 2002. In January 2003 he began studying for the degree of Master of Science in Electrical Engineering. While attending graduate school at North Carolina State University, he held a Teaching Assistant position for Dr. Michael Steer assisting the RF Design for Wireless (ECE-549) class. He also obtained a full time test engineer position with RF Micro-Devices, Inc. in December of 2003. His interests are in Radio Frequency testing and electromagnetics, which relate to RF power amplifiers and automated RF test systems.

Acknowledgements

I have gained many things from graduate studies at NC State. Not only have I gained knowledge, I have also experienced responsibility, teamwork, and met many lifelong friends.

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I would like to thank Mr. Chad Brady for help in preparing me to be a successful engineer. I have learned many things working with Chad and his contributions to my education and experience are priceless.

Finally, I would like to thank my entire family for their support throughout the years. Without their support, none of this would have been possible. Thank you, and I love you all.

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1. Introduction

The pHEMT (Pseudomorphic High Electron Mobility Transistor) has many uses in portable communication systems. A simulation model for the pHEMT is needed in industry to help in the design and development of switches by simulation as well as an effort to correlate simulation results with post-fabrication measurements. Portable communication systems will be further enable the direct integration of pHEMT switches with other cell phone circuitry. Furthermore, test systems as well as many other integrated circuit (IC) applications utilize RF switches and require a well-formed model for circuit design purposes. The most widely used Integrated Circuit (IC) application is for multiband cell phone switching.

1.1 Motivation/Thesis Concentration

Companies in the cellular market are interested in developing a pHEMT switch model to simulate and design in-house antenna switches [6]. Other alternatives are to have the phone manufacturer utilize an external switch or buy an internal switch from another company. Either of these solutions would be less cost effective than developing an in-house solution. All power amplifier modules developed would include all die made in-

house and therefore be less expensive to produce. The trend for smaller cellular phones with fewer components is driving component suppliers to provide solutions with higher levels of integration [3][16][17]. Simulation tools and models are vital to RF IC design. Utilization of these tools enables designers to predict the effects of elements within the system. Including simulation models of RF antenna switches improves the designer's ability to predict the overall performance of the RF system [2]. Some important reasons to simulate RF circuits and systems are "to understand the physics of a complex system of interacting elements, to test new concepts, and to optimize designs" [2].

1.2 pHEMT Switch Background

This document focuses on the use of the pHEMT as an RF antenna switch for cellular telephony from 800 MHz to 2 GHz (GSM850, GSM900, DCS1800, PCS1900) [17]. The purpose of an RF antenna switch in a multiband cell phone is to switch between transmit and receive modes at different times and between different TX and RX band inputs while using one antenna port. A good example of the way this switch is used would be to look at the standard GSM (Global system for mobile communications) frame of approximately 4.8 ms [17]. Each GSM frame is broken into 8 slots. In single slot operation during slot number 1, the transceiver and power amplifier are transmitting and the antenna switch is switched to the "TX" position. System specifications require that after approximately 600 μs, the power amplifier bias switches off and the antenna switch then switches to the "RX" position to feed a direct signal from the antenna port of the phone to the corresponding RX band input of the transceiver module as illustrated in Figure 1.1.

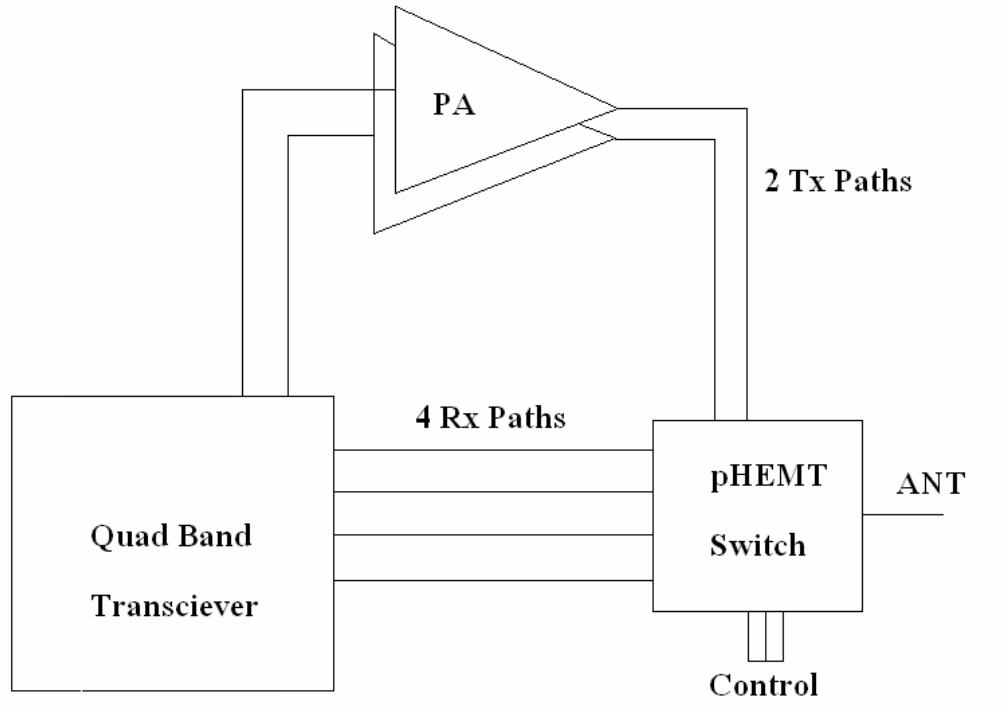

Figure 1.1: RF system block diagram

Two electronic devices are primarily used for antenna switches. Typical PCS systems utilize the "Pin Diode" structure for antenna switching [1]. These devices exhibit low loss and high linearity, which are both key requirements in an RF system. The low loss is important due to power dissipation and linearity is important when looking at modulation schemes and adjacent channel power levels. A major downfall of the Pin Diode Structure is that it requires a significant amount of control current. Using a Pin Diode also typically requires the use of a hybrid integration scheme.

Another structure used as an RF antenna switch is a FET (Field Effect Transistor), which includes MESFETs, MOSFETs, and pHEMTs [1]. There are a few advantages of the

FET type structure over the Pin Diode type structure: (a) the gate current for a FET is lower than the on current of a PIN diode and therefore consumes less power to control the structure [1]. The pHEMT is also smaller in size and easier to incorporate into an RFIC design. Some disadvantages in using FET structures include: (a) more rigorous lithography which can potentially lead to higher cost than the pin design; (b) pHEMT based switches have a lower breakdown voltage than the PIN architecture.; (c) parasitic elements increasing with frequency, the FET type switches are typically utilized for the lower frequency range [4] due to increasing impact of parasitic elements at higher frequencies and (d) The pHEMT is prone to create higher harmonic levels within the switch because the pHEMT has less linearity than the PIN diode.

Of the three types of transistors in the FET-type structure group, the pHEMT switch has the best insertion loss, as well as the best isolation. Isolation is a key parameter in the antenna switch due to RF leakage from the "Transmit" (TX) paths to the "Receive" (RX) paths, and needs to be maximized.

The actual pHEMT's that were modeled have a gate length of $L = 0.5$ μm with a variable width. The gate height is beyond the circuit and system designer's control because it is determined in the foundry's process. The supply voltages used in a practical application would be approximately 3 V. Typical operating conditions would indicate that the gate voltage (V_g) would be 3 V in the "ON" state. For switching to "Transmit" operation, V_{g_tx} is equal to 3 V while V_{g_rx} is equal to 0 V. For switching to "Receive" operation, V_{g_tx} is equal to 0V while V_{g_rx} is equal to 3 V. The cell phone industry requires these RF

switches to have a low on state resistance, R_{on}. This will allow usage in the linear region as well as reducing the loss from the drain to the source. The ideal case would be to have the drain and source voltages to have an equivalent value of (3 V). The Ron is chosen to be low so that the switch operation will be in the linear region. If the RF signal is large enough, the operation could possibly move beyond the linear region of operation and start degrading performance while operating in the knee of the transistor I-V curves. This degradation in performance is most notably seen in the higher power ranges.

The ideal condition for a pHEMT switch is to have very low insertion loss while having a higher isolation [1][5]. This isolation separates the receive port of the switch from the RF signal on the transmit path as well as separating the receive port from other receive ports. The power induced on the receive port due to the transmit port is referred to as Tx-to-Rx leakage. This leakage could cause problems when the device is connected to a transceiver. The insertion loss of the Tx path is also important due to the excess loss degrading part RF output power performance. The Rx insertion loss is important when trying to detect very low power levels on the receiver. If the power level is approximately 50 fW (an average sensitivity of a transceiver Rx input), which corresponds to approximately -103 dBm input power, the receiver can have detection issues with higher switch insertion loss. A significant insertion loss due to the pHEMT switch can dramatically reduce the performance and add errors in the modulation scheme and IQ signals. To reduce the insertion loss, we can increase the width of the gate. By increasing the width of the gate, the isolation suffers and the switch has a larger Tx-to-Rx leakage. One solution for this problem is to include a resistor from the drain to the

source. In the "off mode", the pHEMT looks like a capacitor (C_{off}) which is in parallel with the resistor and the resistor then help the isolation. In the "on mode", the pHEMT looks like a resistor (R_{on}) in parallel with another resistor of larger value (typically 15 kΩ). This will yield a total resistance slightly lower than the R_{on} of the pHEMT, therefore reducing the insertion loss in the "on mode" while increasing the isolation in the "off mode".

$$R_{on} \propto \frac{1}{W \times N_F} \quad \text{(eqn. 1.1)}$$

$$R_{on} \propto \frac{L}{W \times H} \quad \text{(eqn. 1.2)}$$

$$C_{off} \propto W \times N_F \quad \text{(eqn. 1.3)}$$

$$I_{dss} \propto W \times N_F \quad \text{(eqn. 1.4)}$$

Where,

N_F = number of fingers for the device

Figure 1.2 shows a simple SPDT RF switch using pHEMT's. R1 and R2 are gate resistors while R3 is a supply resistor to limit current. R4 and R5 are 15 kΩ resistors added for increased isolation. The DC blocking caps on the source of both legs are there to block the DC voltage from the output of the power amplifier and the input of the receiver.

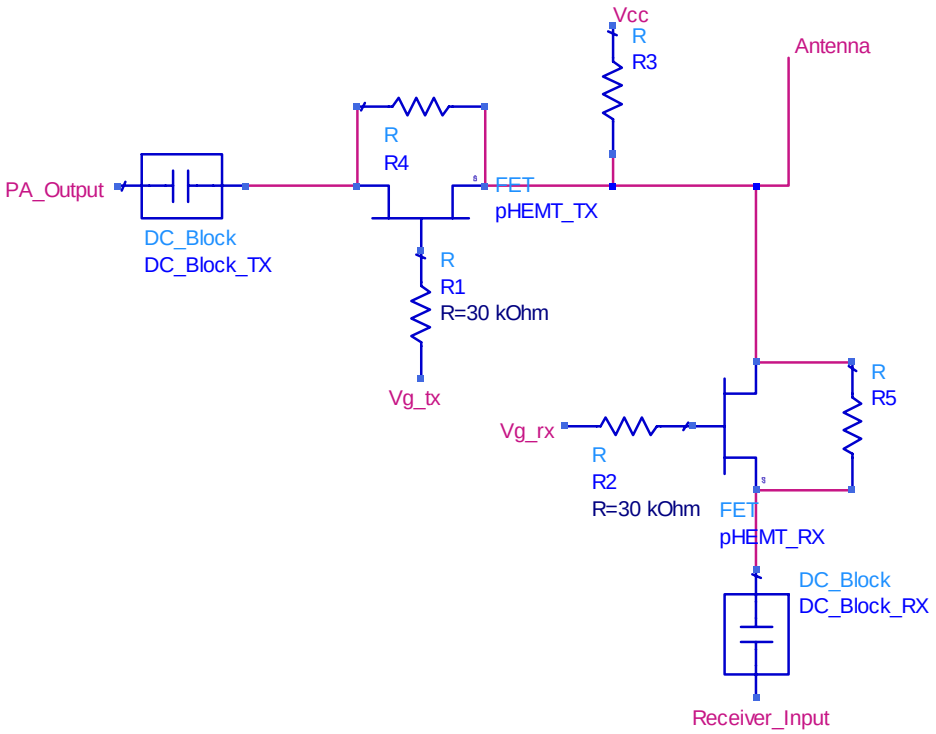

Figure 1.2: Simple pHEMT SPDT RF switch w/ isolation resistors included

Figure 1.3 shows a simple pHEMT RF switch design that utilizes two transistors per path. This design change has a slightly larger insertion loss, but with increased isolation. The additional path resistance due to the second pHEMT increases the insertion loss.

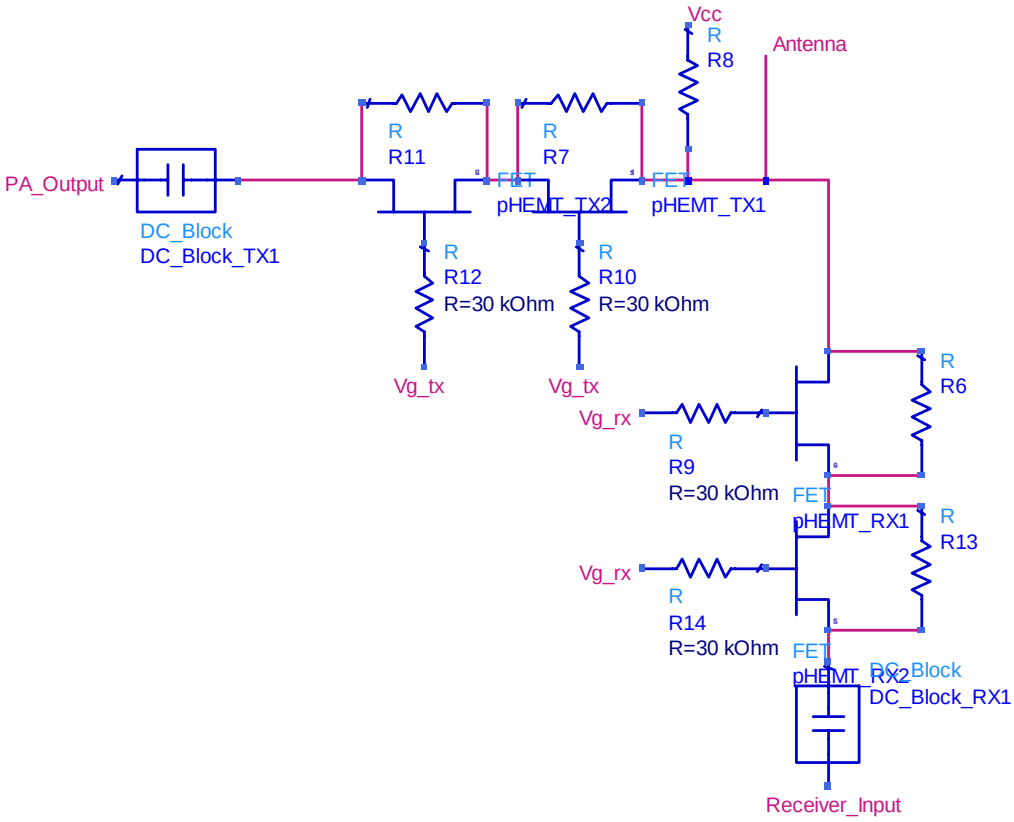

Figure 1.3: Simple pHEMT SPDT RF switch w/ increased isolation

1.3 Thesis Overview

This thesis describes the methods behind model extraction concentrating on pHEMT RF switches, which will be used in a simulation tool for better prediction of RF system performance.

Chapter 2 is a description of the calibration process and the equipment used for the model extraction. It describes methods and standards used for different types of calibration.

Chapter 3 is an overview of the extraction method and actual model extraction from measured data. This overview includes the extraction of intrinsic as well as extrinsic components.

Chapter 4 is a review of the results and comparison of simulated data and measured data. This chapter presents a quantitative evaluation of the model extraction procedure with respect to the measured data.

Chapter 5 is a conclusion that discusses the final findings and adjustments made. This chapter presents an overview of the extracted model and possible future improvements.

2. Measurement Methodology

The methodology used in the die level measurements included important steps and procedures that are vital to the accuracy of the measurements. When dealing with higher frequency test ranges, higher order effects become more prominent than at lower frequency test ranges. The steps that were followed in this pHEMT switch modeling procedure are as follows:

1. Equipment Selection and Setup
2. Equipment Calibration
3. Calibration Verification
4. Protective Test Setup
5. Agilent IC-CAP 2002 model extraction software setup (Macros)
6. Device Measurement

Calibration is critical to successful model extraction. Verification of the calibration before we take any measurements and this is the key to the validity of our subsequent measurements. We initially run a calibration with the SOLT (SHORT / OPEN / LOAD / THRU) standard as well as a LRM (LINE / REFLECTION / MATCH) standard. We then compare the data from the two calibrations and verify that the SOLT calibration is valid. This will be discussed in depth later in this section.

2.1 Equipment Selection

The equipment required for die level s-parameter and RF measurements are standard die level measurement devices. These pieces of equipment are a part of an RF Micro-Devices lab, utilized and designed for research and modeling. The major equipment needed for pHEMT model extraction includes a network analyzer, semiconductor parameter analyzer, and a personal computer [15]. The network analyzer is primarily used for the analysis of RF behavior and the semiconductor parameter analyzer is used for setting DC bias points. Next is a complete list of equipment needed for the pHEMT model extraction.

Part #	Manufacturer	Quantity	Description
E5270A	Agilent	1	SC Parameter Analyzer
E5281A	Agilent	4	SMU
E8362B	Agilent	1	Microwave Vector Network
PM8	Karl Suss	1	Probe Station
11612A	Agilent	1	Bias tee ($40V_{DC}$/0.5A max)
11612A	Agilent	1	Bias tee ($100V_{DC}$/2A max)
40A-GSG-100-DP	Pico Probe	2	100um Pitch Probe
	VIBRAPLANE	1	Anti-vibration Table
IC-CAP 2002	Agilent	1	Model Extraction Program

Table 2.1: Extraction station equipment

4 SMU's (Agilent E5281A) were used for this model extraction to prevent the need for setup change when measuring forward and reverse conditions [15]. The $40V_{DC}$ bias tee was connected to the Gate and the $100V_{DC}$ bias tee was connected to the drain of the pHEMT. This was due to the current limitations of the $40V_{DC}$ bias tee and the drain requiring a higher current bias tee. The VIBRAPLANE anti-vibrate table is crucial for any wafer measurements due to mechanical vibrations affecting the measurements as well as possibly destroying devices and damaging probes. The wafer is also suctioned to the platform by use of a vacuum system to hold the wafer in place. This is also used to hold the calibration devices in place during the next calibration step.

To continue with the model extraction, a full bench calibration needs to take place. The calibration is in two parts, the first of which being the network analyzer calibration and the second being the DC calibration.

2.2 Network Analyzer Calibration

The network analyzer calibration is used to determine the S-parameters induced by the cables and the probes. Two calibration standards were used and then compared to see if both are in line with one another. The two calibration methods used were the SOLT [15] calibration and the LRM which is comparable to the TRM (Thru, Reflection, Match) calibration method. Once the comparison is completed and all parameters have been verified, the SOLT calibration can now be used for our device parameter extraction. In Figure 2.1 below, we can see the four standards used for the SOLT calibration.

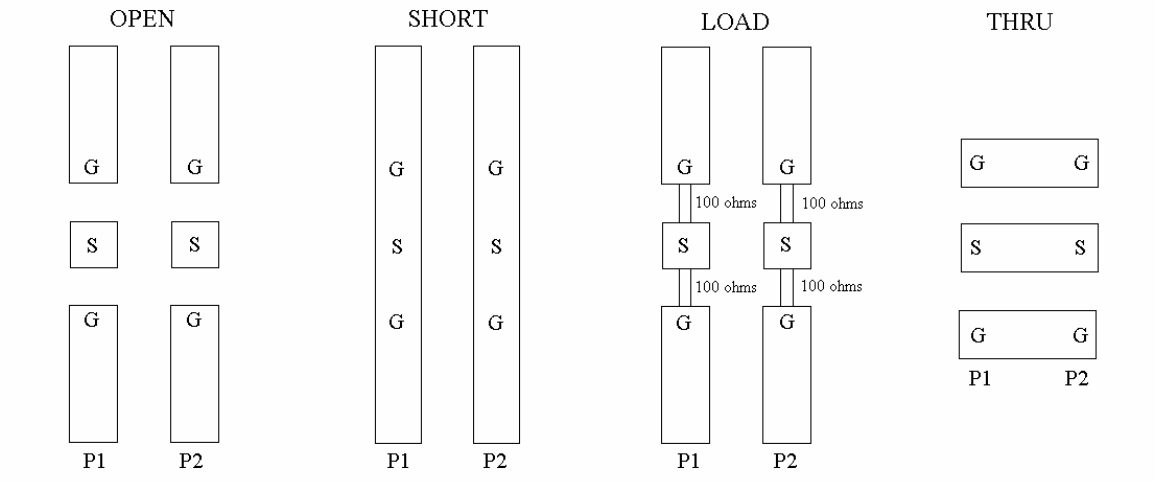

Figure 2.1: SOLT calibration structures

For the SOLT calibration, the open can also be calibrated with the probes in the air [15]. Placing the probes onto the corresponding calibration structures takes practice and experience. Once the probe makes contact with the structure, we can see that the tip of the probe bends with added pressure and then slides on the substrate. This slide is a common verification used to ensure adequate contact with the substrate. The typical dimension of this "slide" is verified visually and is normally on the order of 1-2 mils. The open calibration structure is simply an open circuit between Probe 1 ground and Probe 2 ground as well as Probe 1 signal and Probe 2 signal. From an electrical standpoint, the short calibration structure is the exact opposite of the open structure. Probe 1 ground is shorted to Probe 1 signal and Probe 2 ground is shorted to Probe 2 signal. The load calibration structure utilizes 100 ohm precision resistors connected between both ground lines and the signal line for both Probe 1 and Probe 2. The two 100 Ω resistors are in parallel and create a known 50 ohm load which is presented to each probe. The thru calibration structure connects the grounds of Probe 1 and Probe 2 and also connects the signal lines of Probe 1 and Probe 2. Placement of each probe is crucial in this step due to added inductance and phase shift associated with Probe 1 and Probe 2 being a certain distance apart. When placing the probes on the substrate, both probes' final position should be as close as possible to reduce the phase shift and loss in the line. The assumption in this calibration process is that the electrical line length is 0.

2.3 Calibration Verification

When verifying the calibration, we can compare the short and open phase difference. The phase difference should be 180^{o}. The log magnitude of the short and open verses the

load/thru should be greater than 10 dB difference (correlated with the dynamic range of the equipment). Calibration verification also consists of measurement repeatability. For this repeatability verification, two or more calibrations should be run for comparison. The "thru path" S_{21} log magnitude should be 0 dB $\pm$ 0.02 dB difference while the phase difference should be $\pm 0.1^{o}$ at 18 GHz. This corresponds to approximately 1 ps - 1.13 ps time shift. The "open path" should be 0 dB $\pm$ 0.1 dB and a phase difference of $\pm 0.5^{o}$ at 18 GHz. The "load path" should be verified by a return loss magnitude of greater than 40 dB. This return loss corresponds to a reflection coefficient (Γ) of 0.0099 and a VSWR of 1.02. It is crucial for the phase delay to be extremely accurate for switch modeling. Figure 2.2 and Figure 2.3 below illustrate the comparison of S_{11} and S_{22} of SOLT and LRM data in real/imaginary form (Figure 2.2) and log magnitude form (Figure 2.3). This data was taken with an open on the probes. From the data, we can see the return loss decrease with frequency and the phase shift across frequency. Both the SOLT calibration and the LRM calibration data correlate across frequency (DC – 20 GHz).

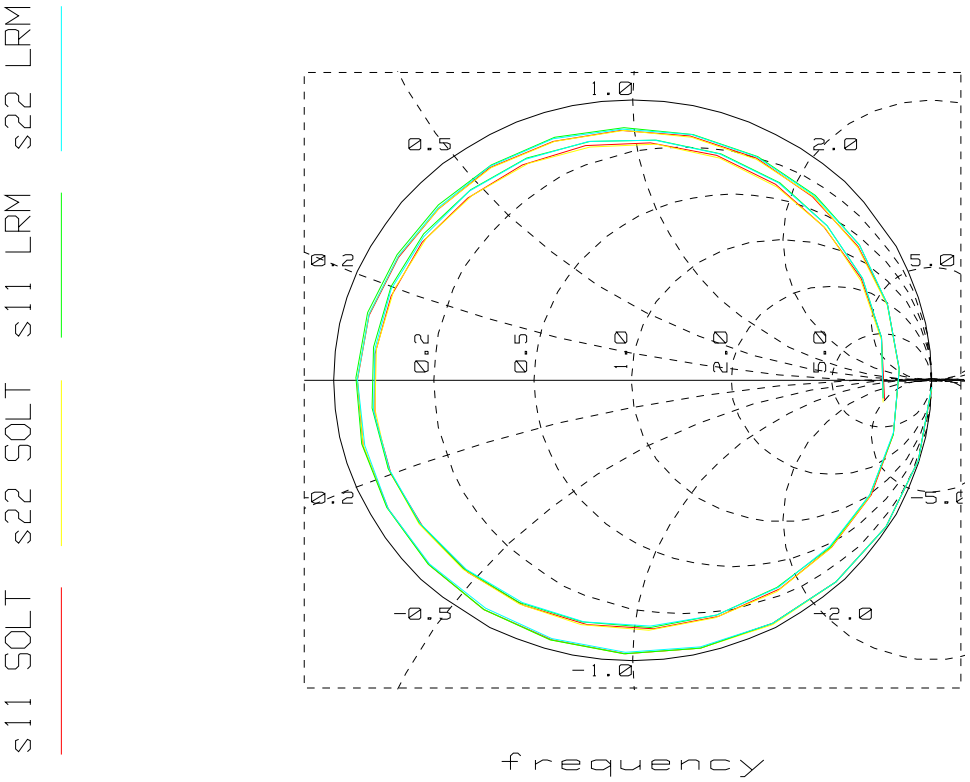

Figure 2.2: S_{11}/S_{22} comparison of SOLT and LRM calibration data

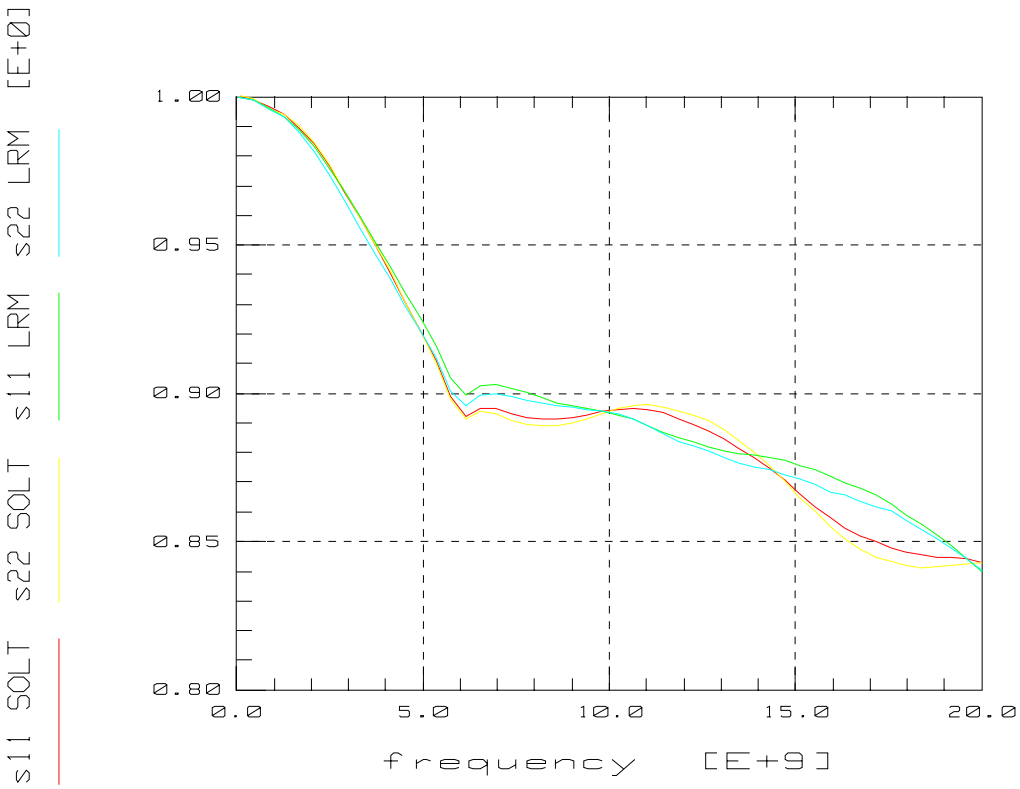

Figure 2.3: S_{11}/S_{22} Log Mag Comparison of SOLT and LRM calibration data

Figure 2.4 below displays the phase difference across frequency. S_{11} and S_{22} of SOLT and LRM calibrations correlate across frequency (DC – 20 GHz). The phase difference around 5 GHz is due to the transition point from -180^{o} to 180^{o}. This should not affect our measurement data.

The S-parameter calibration of the network analyzer has been verified by a comparison between the SOLT calibration standard and the LRM calibration standard. This verification of the calibration is necessary to ensure measurement repeatability/reproducibility and accurate data during the measurement process.

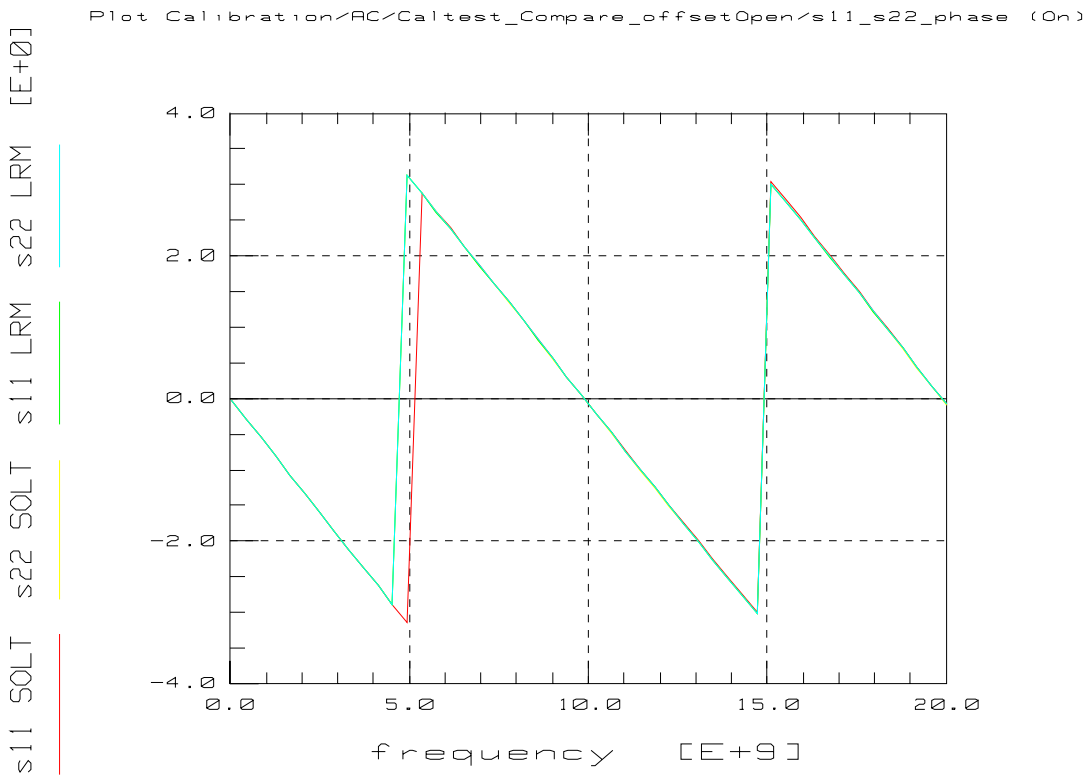

Figure 2.4: *S_{11}/S_{22} Phase Comparison of SOLT and LRM calibration data*

A calibration test structure was implemented on the wafer. These cal structures were basic AC open and AC short structures (inductor and capacitor respectively). These structures were used to verify the phase shifts and losses when compared to calculated data.

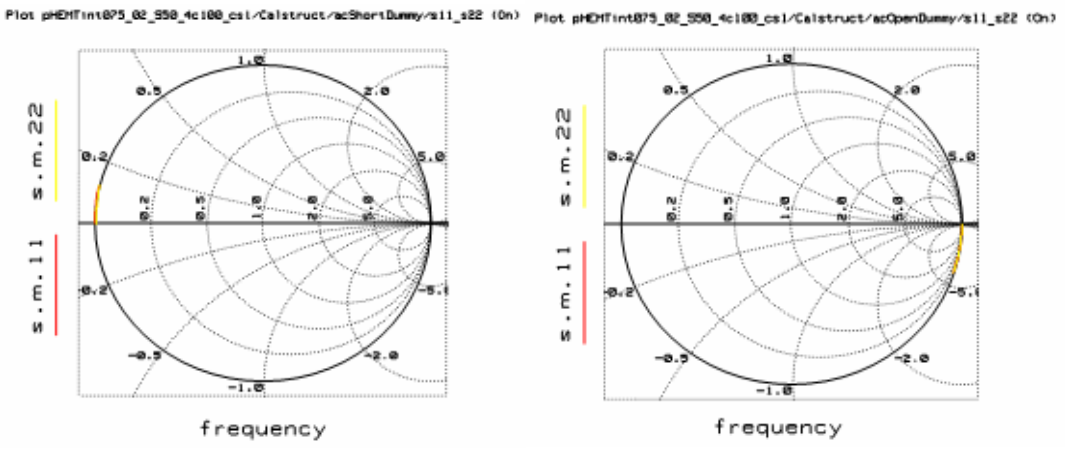

Figure 2.5: Actual results of AC Short and AC Open Phase Verification

2.4 DC Calibration

The DC calibration was taken by analyzing the loss through each bias tee across varying gate voltages (V_g). The gate bias tee was found to have approximately 0.7 Ω of loss while the drain bias tee was found to have approximately 0.9 Ω of loss. The raw data (gate current across varying V_g) is presented in Figure 2.6 below. Since our plot is current (I) across voltage (V_g), resistance is the inverse of the slope, $R = \frac{V}{I} = \left(\frac{I}{V}\right)^{-1} = Slope^{-1}$. Figure 2.7 shows resistance versus gate voltage (V_g) for each bias tee.

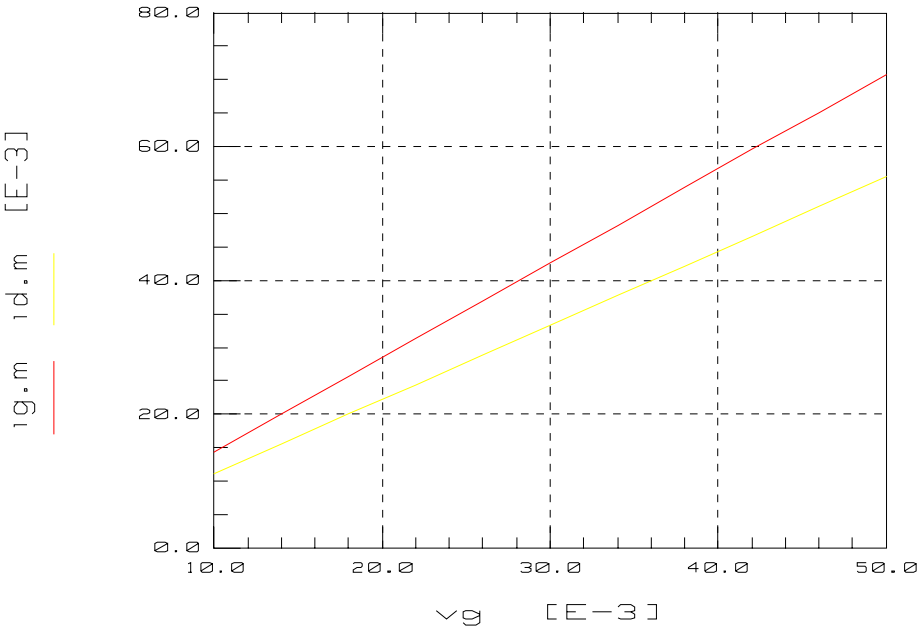

Figure 2.6: DC bias tee Current vs. gate voltage (V_g)

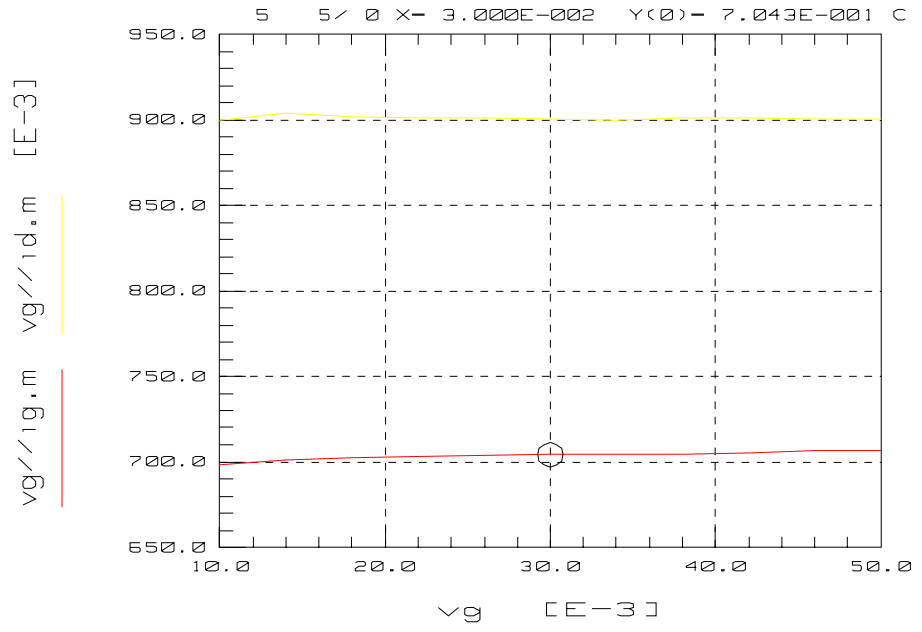

Figure 2.7: DC bias tee Resistance vs. gate voltage (V_g)

2.5 Protective Test Setup/IC-CAP Macro Setup

The idea behind the protective test setup is to ensure that the model extraction does not set conditions that could damage the device and degrade performance. Due to the analysis of the process physics, the safe maximum I_g (gate current) is 0.5 mA for a 0.1 mm device. A 0.1 mm device corresponds to a pHEMT with a single gate finger. As we noted earlier, $I_{dss} \propto W \times N_F$ so therefore we can calculate the max Ig for any device (i.e. 2 mA for a 0.4 mm device). Our test device is a 0.4 mm comb pHEMT device ($N_F = 4$). The device is then connected to the test setup and an initial gate current (I_g) measurement is taken. The gate-to-source voltage (V_{gs}) is taken from the data that corresponds to a gate current (I_g) of 2 mA for a 0.4 mm device. This is set as the max V_{gs} for the extraction process. From the same set of measurement data, the I_{dss} is obtained at the max V_{gs}. This gives I_{ds_max} for the drain current. For the 0.4 mm device, $I_{ds\_max} = 140$ mA. The next setup test is a measurement of drain current (I_d) vs. gate-to-source voltage (V_{gs}) while the drain-to-source voltage (V_{ds}) is 1.5 V. Once this measurement is taken, we can find the pinch-off voltage (V_{TO}). This threshold voltage is found to be -0.884 V. The value for the threshold voltage (V_{TO}) is the value of V_{gs} when $I_d = 1\%$ of I_{dss}. The knee voltage (V_{knee}) can also be determined from the measurement data and is found to be 0.75 V for the 0.4 mm, 4 finger, comb pHEMT. Once all the protective and analytical data is determined, the measurement range can be set in IC-CAP and then macros can be executed for the rest of the device parameter extraction. At this point, the data taken in the protective setup is then backed up to prevent data loss.

3. Model Extraction

The actual model extraction that takes place within IC-CAP software is an integrated set of measurements designed to extract each model parameter. There are many different methods to model extraction as well as different methods for different types of devices. Large signal device model extraction involves a large number of S-parameters to be measured and then converted into equivalent circuit format [8]. IC-CAP from Agilent does this extraction process in a compact format. In this section, the details of the direct extraction of Intrinsic Components [11] as well as the additional methods used by IC-CAP are outlined and detailed.

3.1 Direct Extraction – Intrinsic Components

The direct extraction of intrinsic components refers to the process of converting measured S-parameters to small-signal parameters. A hybrid-pi model is created from the intrinsic elements [11]. In this hybrid-pi model, the voltage across C_{gs} (gate-to-source capacitance) controls I_d (drain current) [16]. In Figure 3.1, the small-signal model for a pHEMT device is displayed. This topology is the standard topology for GaAs-based FET devices as well as HEMT devices [11]. This model clearly indicates that R_g (gate

resistance), R_s (source resistance), and R_d (drain resistance) are included. These parameters are parasitic elements and are measured during the de-embedding process and then utilized when deriving the small-signal parameter values.

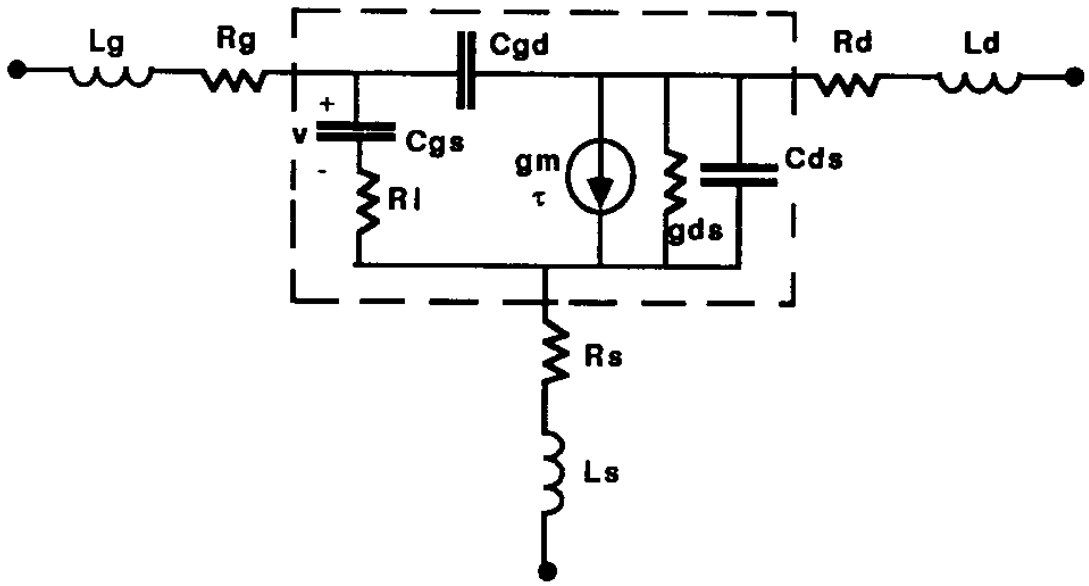

Figure 3.1: Small-Signal circuit of a GaAsFET/HEMT device [7][8]

L_g, L_d, and L_s are the extrinsic parasitic inductances. The direct extraction assumes that the parasitic resistances are known. [8]. Parasitic resistances can be derived from data taken during DC measurements. The model extracted in this paper utilized DC measurements completed by IC-CAP to derive these DC parameters. This process will be discussed in detail later in this section.

The intrinsic elements of the small-signal equivalent circuit include g_m, g_d, C_{gs}, C_{gd}, $R_i(R_{gs})$, and τ. All of these parameters are dependent on the bias applied to the device [9]. The elements outside of the intrinsic model are the extrinsic parameters. These

include L_g, R_g, L_s, R_s, R_d, and L_d. The extrinsic parameters do not depend on the transistor biasing. When deriving the intrinsic component values, Gilles Dambrine [9] notes that the use of Y-parameters (admittance parameters) simplifies the circuit analysis due to the hybrid-pi topology. According to Dambrine, these intrinsic Y-parameters are:

$$y_{11} = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \quad \text{(eqn. 3.1)}$$

$$y_{12} = -j\omega C_{gd} \quad \text{(eqn. 3.2)}$$

$$y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{gs}\omega} - j\omega C_{gd} \quad \text{(eqn. 3.3)}$$

$$y_{22} = g_d + j\omega(C_{ds} + C_{gd}) \quad \text{(eqn. 3.4)}$$

with $D = 1 + \omega^2 C_{gs}^2 R_i^2$.

By using a prescribed procedure, the intrinsic Y matrix above can be determined from measured data. The following is the procedure for determining the intrinsic Y matrix [9], [11]:

1. Perform S-parameter measurements of the extrinsic device.
2. Use the standard S-parameter to Z-parameter (impedance parameters) transformation to subtract the series elements. Series L_g and L_d parameter values can then be subtracted.
3. Use the standard Z-parameter to Y-parameter transformation to subtract the parallel elements. Parallel C_{pg} and C_{pd} parameter values can then be subtracted.
4. Convert back to Z-parameters by using the standard Y-parameter to Z-parameter transformation to subtract the series elements R_g, R_s, L_s, and R_d.
5. Convert back to Y-parameters to yield the final intrinsic Y-matrix.

The conversions needed to convert S-parameters to Z-parameters, Z-parameters to Y-parameters, and Y-parameters to Z parameters are listed in many available sources.

The following expressions for the intrinsic component values have been discussed in detail by many authors [9][10][11]. The intrinsic parameter value C_{gd} can be expressed as:

$$C_{gd} = -\frac{\mathrm{Im}(y_{12})}{\omega} \qquad \text{(eqn. 3.5)}$$

C_{ds} can be determined by analyzing the imaginary terms of y_{22} and y_{12}. C_{ds} can be expressed as:

$$C_{ds} = \frac{\mathrm{Im}(y_{22}) + \mathrm{Im}(y_{12})}{\omega} \qquad \text{(eqn. 3.6)}$$

Rds is calculated as being the inverse of the real part of y_{22}. Rds can be expressed as:

$$R_{ds} = \frac{1}{\mathrm{Re}(y_{22})} \qquad \text{(eqn. 3.7)}$$

C_{gs} and R_{gs} (otherwise known as Ri) can be derived from the intrinsic Y-matrix as well. C_{gs} can be expressed as:

$$C_{gs} = \frac{\mathrm{Re}(y_{11})(1+\omega^2 k^2)}{k\omega^2} \qquad \text{(eqn. 3.8)}$$

Since C_{gs} is now known at this point, we can calculate R_{gs} by diving k (the Boltzmann's Constant) by C_{gs}. R_{gs} can be expressed as:

$$R_{gs} = \frac{k}{C_{gs}} \qquad \text{(eqn. 3.9)}$$

In order to derive G_m and τ, $G_m \cdot e^{-j\omega\tau}$ must be known. We can replace $G_m \cdot e^{-j\omega\tau}$ with $G_m r + jG_m i$. Gm and τ can be expressed as:

$$G_m = (G_m r^2 + G_m i^2)^{1/2} \qquad \text{(eqn. 3.10)}$$

And

$$\tau = -\frac{1}{\omega}\tan^{-1}\left(\frac{G_m i}{G_m r}\right) \qquad \text{(eqn. 3.11)}$$

Where

$$G_m r = \mathrm{Re}(y_{21}) - \mathrm{Im}(y_{21})R_{gs}C_{gs}\omega - \omega^2 C_{gd}C_{gs}R_{gs} \qquad \text{(eqn. 3.12)}$$

And

$$G_m i = \mathrm{Re}(y_{21})R_{gs}C_{gs}\omega + \mathrm{Im}(y_{21}) + \omega C_{gd} \qquad \text{(eqn. 3.13)}$$

3.2 Bias Independent Parameter Extraction

As stated before in section 3.1, the extrinsic device parameters do not depend on biasing levels. These extrinsic parameters include L_g, R_g, L_s, R_s, R_d, and L_d for the gate (g), source (s), and drain (d) respectively. There are several methods to extract these parameters.

The method outlined in IC-CAP for extracting the source resistance (R_s) is very similar to the Yang and Long Method [13]. The Yang and Long Method analyzes the change in gate voltage (V_g) with a change in drain current (I_d) and requires a sweep of gate current (I_g) values that are between 50 and 100 times smaller than two different drain currents (I_d) while measuring the gate-to-source voltage (V_{gs}). These two drain currents are within the linear region of operation (where $V_{ds} < 0.25$ V). Variations in V_{gs} from two different drain currents (I_d) will correspond to the difference in the source common lead resistance (R_s) and the transistors gate-to-source diode resistance (R_{gs}). Assuming we know R_{gs} (by measuring I_s and the ideality factor n of the gate-to-source diode), we can relate V_{gs}, I_{ds}, and R_s as follows:

$$\Delta V_{gs} = R_s \cdot \Delta I_{ds} \qquad \text{(eqn. 3.14)}$$

When deriving expressions for I_s (reverse saturation current) and the ideality factor n, we measure the gate current (I_g) with respect to the gate voltage (V_g). For this derivation, we can reference the diode equation:

$$I_D = I_s \left[e^{\frac{qV_D}{nkT}} - 1 \right] \qquad \text{(eqn. 3.15)}$$

Where q is the change of an electron, V_d is the applied voltage V_{gs}, k is the Boltzmann's constant, and T is temperature in Kelvin [14]. When we substitute I_g for I_d and substitute V_{gs} for V_d, we have:

$$I_g = I_s\left[e^{\frac{qV_{gs}}{nkT}} - 1\right] \qquad \text{(eqn. 3.16)}$$

With the gate current I_g being in a log scale, we can compute the ideality factor n to be related to the slope of the line by:

$$n^{-1} = \frac{qm}{kT} \qquad \text{(eqn. 3.17)}$$

Where m is the slope of $\log(I_g)$ vs. V_g. The slope m is also equal at the junction resistance R_{dy}^{-1} [9]. We can calculate the slope to be:

$$m = \frac{\log(I_{g1}) - \log(I_{g2})}{V_{g1} - V_{g2}} = R_{dy}^{-1} \qquad \text{(eqn. 3.18)}$$

By knowing the equation for the ideality factor n and the slope m, we can compute the value of n as follows:

$$n = \frac{kT}{q}\left(\frac{\log(I_{g1}/I_{g2})}{V_{g1} - V_{g2}}\right) \qquad \text{(eqn. 3.19)}$$

We can also find the gate-diode's I_s (reverse saturation current) [14] value by analyzing the same data used for deriving the ideality factor n. "I_s" is the value of the gate current when the gate voltage is 0 V or when the $\log(I_g)$ is 1 [13].

According to the IC-CAP documentation [13], when extracting the drain and gate resistances, R_d and R_g respectively, IC-CAP utilizes S-parameter data at three to five

forward bias points. The extrinsic elements are constant while the gate and channel elements change [13]. The corresponding S-parameters are then converted to Z-parameters are the imaginary part of the intrinsic Z_{12} is plotted and the resistance values are extracted. Another method is described by Dambrine. After converting the initial measured S-parameters (at $V_{ds} = 0$ V) to the intrinsic Z-parameters as outlined in Step 4 of the conversion procedure, we can add the parasitic resistances and inductances to the intrinsic Z-parameters. The intrinsic Z-parameters with series resistances and inductances added are as follows: [9]

$$z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} + j\omega\left(L_s + L_g\right) \qquad \text{(eqn. 3.20)}$$

$$z_{12} = z_{21} = R_s + \frac{R_c}{2} + j\omega L_s \qquad \text{(eqn. 3.21)}$$

$$z_{22} = R_s + R_d + R_c + j\omega\left(L_s + L_d\right) \qquad \text{(eqn. 3.22)}$$

Where R_c is the channel resistance under the gate [9].

Since the measurements were on wafer with a probe station, the influence of the parasitic inductances L_s, L_d, and L_g can be ignored. By ignoring the extrinsic parasitic inductances, the intrinsic z matrix can be simplified to:

$$z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} \qquad \text{(eqn. 3.23)}$$

$$z_{12} = z_{21} = R_s + \frac{R_c}{2} \qquad \text{(eqn. 3.24)}$$

$$z_{22} = R_s + R_d + R_c \qquad \text{(eqn. 3.25)}$$

If our inductance values were not ignored, they could be determined by plotting the imaginary components of the converted Z-parameters. The source inductance, L_s, could be determined from $\mathrm{Im}(Z_{12})$, the gate inductance, L_g, from $\mathrm{Im}(Z_{11})$, and the drain inductance, L_d, from $\mathrm{Im}(Z_{22})$ [9].

Dambrine [9] also states that the value of the channel resistance R_c can be determined from the channel technological parameters and the source resistance R_s which was calculated earlier. With those values, we can obtain the rest of the extrinsic parameters by analyzing the impedance parameters noted above.

IC-CAP uses several more formulas to calculate model parameters that are not part of the intrinsic and extrinsic small-signal parameters that are not important to the model for switching performance The description of the methodology can be found in the help section of IC-CAP or ADS (Advanced Design System), both available only from Agilent.

4. Results

The pHEMT used for the model extraction process is a transistor that is currently being utilized in RFIC antenna switches. The gate layout is a "comb" type of structure, instead of the differing "meandering" gate. The pHEMT's total gate width is 400 μm. The transistor contains four gate fingers 100 μm wide to comprise the total gate width of 400 μm. The gate length is 50 μm wide and is a single gate device. The name of the structure used is 075_02_S50_4c100_cs1. The name breaks down as:

075 = lot

02 = wafer

S50 = single gate, 50 μm gate length

4c100 = 4 fingers (channels), c=comb gate structure, 100 μm is gate width

Total gate width = 400 μm

cs = common source

As we can see, the probe pads are located on the left and right sides of the pHEMT layout in Figure 4.1. The ground of the probes is connected to the source while Port 1 is connected to the gate and Port 2 is connected to the drain. Figure 4.2 shows a more detailed layout of the actual pHEMT device without the probe pads.

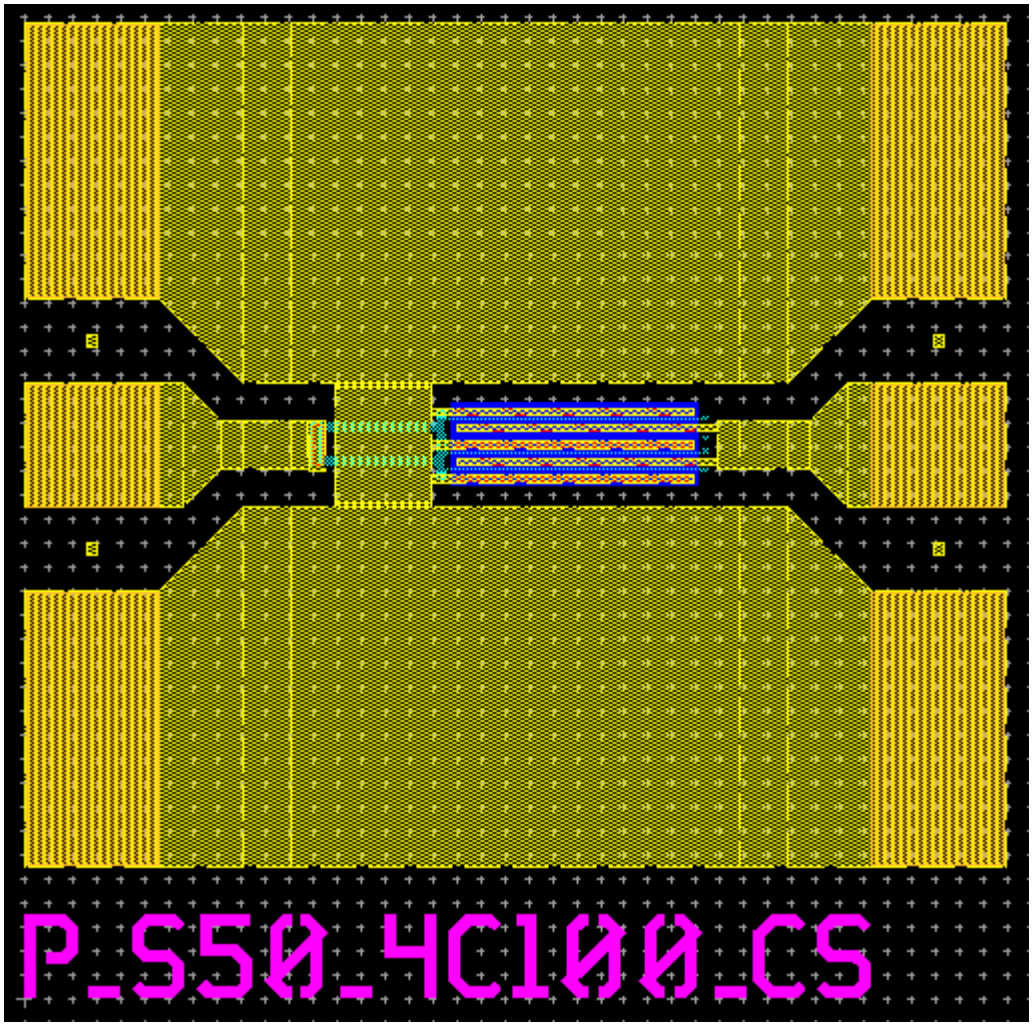

Figure 4.1: Probe Structure with a 4x100 pHEMT

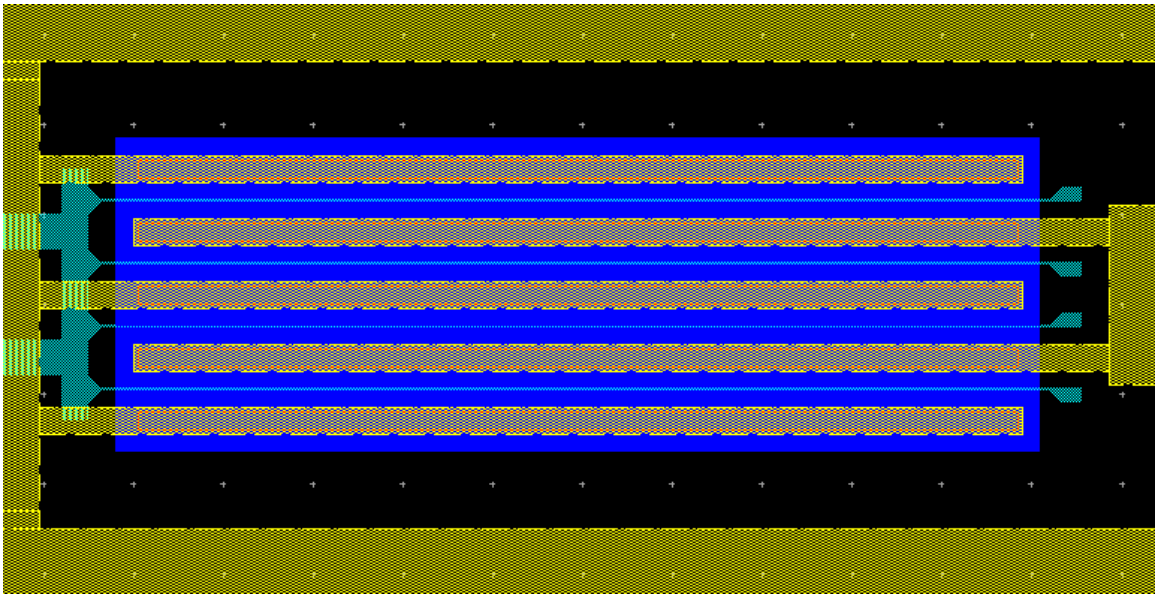

Figure 4.2: Detailed version of the 4x100 pHEMT in Figure 4.1

The structure for de-embedding the parasitic elements is identical to the probe structure seen in Figure 4.1.

IC-CAP utilizes the methods described in chapter 3 to extract and determine the model's small signal parameters that are to be used in the final model file used by circuit simulators. The model file text below is the complete model extracted from IC-CAP for the 4x100 µm comb gate pHEMT. This includes intrinsic component values, extrinsic component values, as well as many other model factors.

```
; EEfet3 circuit definition
;
define mnseefet3 (G D S)
L:lg g2 g3 L=0.001n
L:ld d2 d3 L=0.001n
L:ls s2 s3 L=80ph
C:cxgd g2 d2 C=0.01f
C:cxds d2 s2 C=0.01f
C:cxgs g2 s2 C=0.01f
Short:gate g g1 Mode=0 ;current meter
Short:drain d d1 Mode=0 ;current meter
Short:source 0 s1 Mode=0 ;current meter
TL:tg g1 S g2 S Z=50 L=0.0 V=1.0
TL:td d1 S d2 S Z=50 L=0 V=1.0
TL:ts s1 S s2 S Z=50 L=0 V=1

EEFET3:fet d3 g3 s3 Ugw=0 N=0
model EEFET3 EE_HEMT1 \
Rg=0.5        \
Rd=0.5        \
Rs=0.5        \
Is=1e-12      \
N=1.5         \
Gmmax=0.861   \
Gamma=0.005126 \
Kapa=9.87m    \
Peff=100      \
Vto=-3.37     \
Vtso=-100.0   \
Vdelt=183u    \
Vch=1.0000    \
Vsat=2.032    \
Vgo=-0.782    \
Vdso=5.21     \
Vco=10        \
Mu=0          \
Vba=1.0       \
Vbc=1.0       \
Deltgm=0.0    \
Deltgmac=0.0  \
Alpha=0.001   \
Gmmaxac=0.9812 \
Gammaac=0.015 \
Kapaac=180u   \
Peffac=100.0  \
Vtoac=-3.4    \
```

```
Vtsoac=-100.0  \
Vdeltac=0.277  \
Rdb=1G         \
Cbs=0.16p      \
Gdbm=0.0667    \
Kdb=0.204      \
Vdsm=249u      \
C11o=1.5p      \
C11th=11.8f    \
Vinfl=-2.7     \
Deltgs=7.4     \
Deltds=0.95    \
Lambda=0.03    \
C12sat=786f    \
Cgdsat=786f    \
Kbk=0.03       \
Vbr=25         \
Nbr=2.0        \
Idsoc=1.893    \
Ris=0.13       \
Rid=0.13       \
Tau=5ps        \
Cdso=1.3p      \
Ugw=1.0        \
Ngf=1.0        \
Kmod=103       \
Kver=1000
end mnseefet3
```

4.1 Preview Measurements

The measurements in the preview section of IC-CAP are the measurements taken for the "Protective Test Setup" described in Section 2.5 as well as data not utilized in this investigation. The preview measurements contain fewer number of data points due to time constraints, a rough trend instead is used for the analysis The full measurement utilizes a more broad set of conditions for actual model parameter extraction.

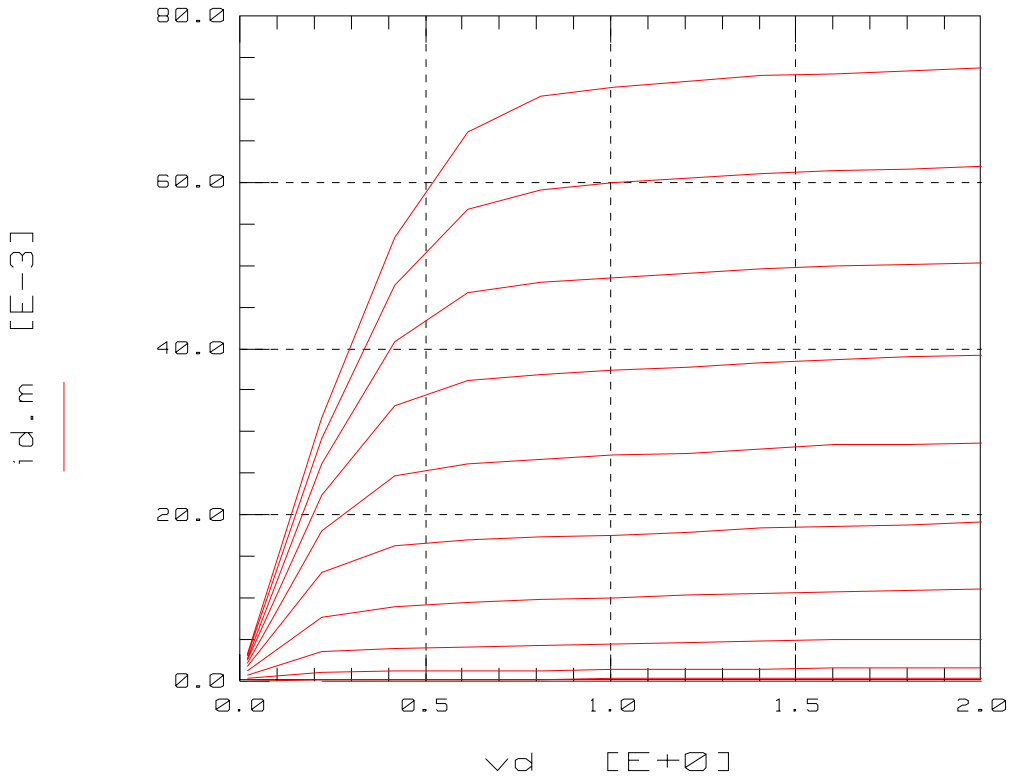

Figure 4.3: DC IV curves which correspond to the drain current I_d and the drain-to-source voltage (V_{ds}, or V_d in a common source configuration)

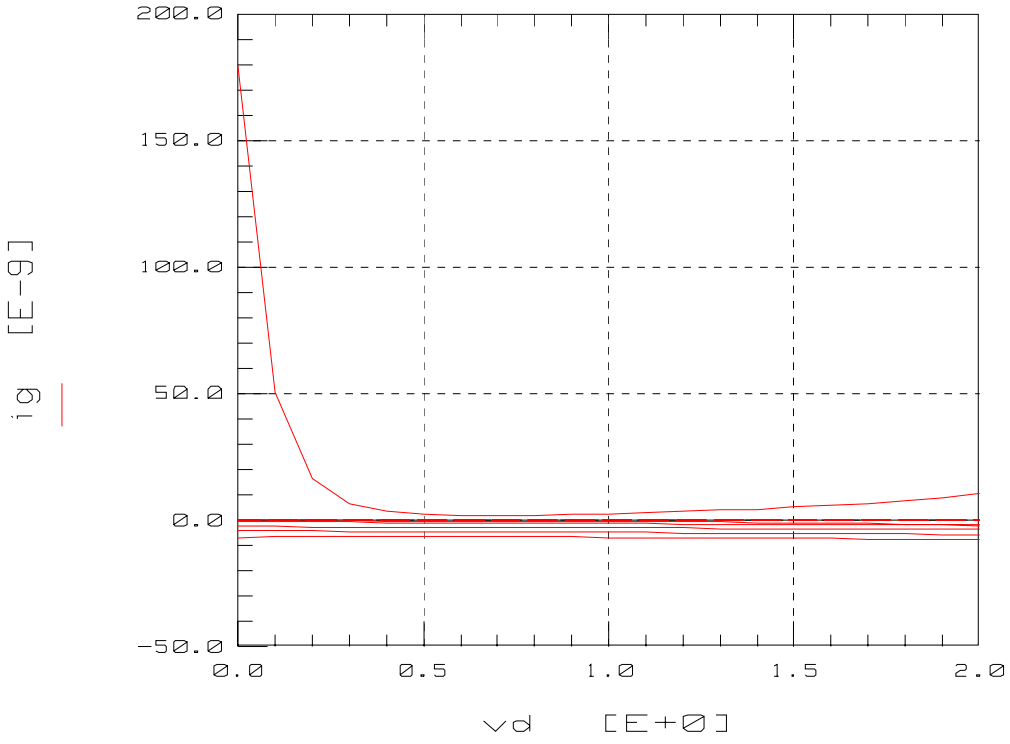

Figure 4.4: Gate current (I_g) vs. drain voltage (V_d) across varying bias conditions

Figure 4.4 above shows the relationship of the gate current (I_g) to the drain-to-source voltage (V_{ds}) with varying gate voltages (V_g). The different measurement data series are due to the change in gate voltages and are then swept across drain voltage (V_d).

The gate diode test in the preview measurement section consists of the plot used for the extraction of I_s and the ideality factor n as was discussed in Section 3.2. This log plot is pictured in Figure 4.5 below.

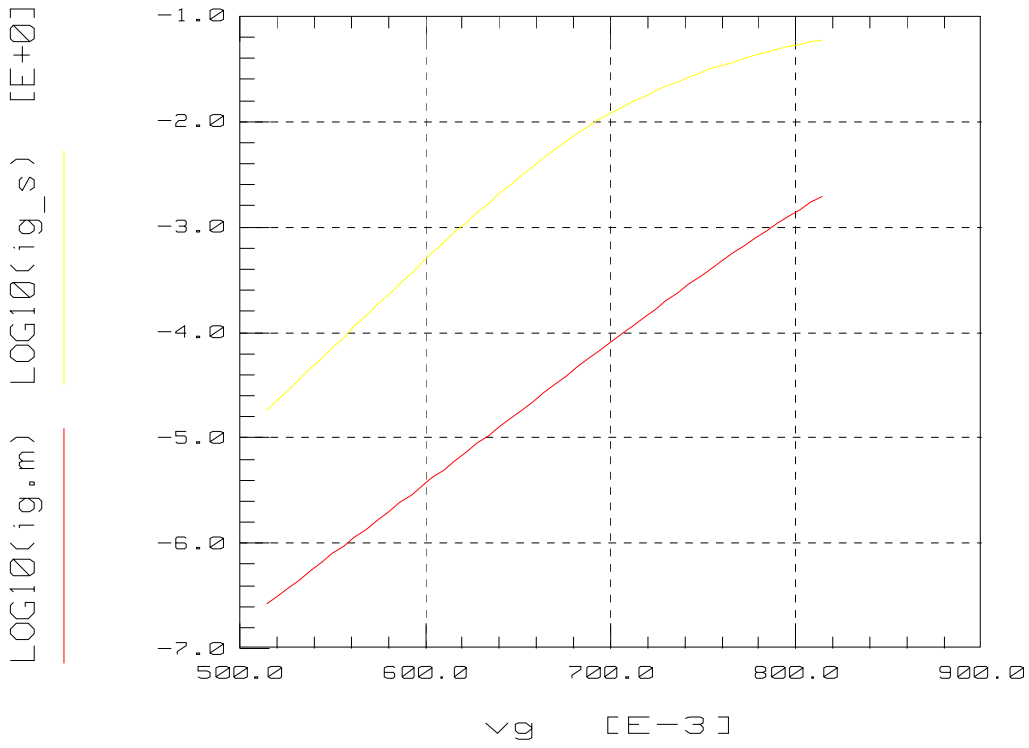

Figure 4.5: Log plot of I_g vs. V_g (measured and simulated) across varying bias conditions

4.2 DC data

The DC data collected is mostly in terms of IV curves, voltage vs. voltage curves, etc. This data is extremely useful when extracting parameters that are bias dependent. Standard IV curves as well as different plots of current and voltages make the DC data extraction possible. Within the DC IV extraction section of IC-CAP, the following data and plots are included:

1. ig_Is_N

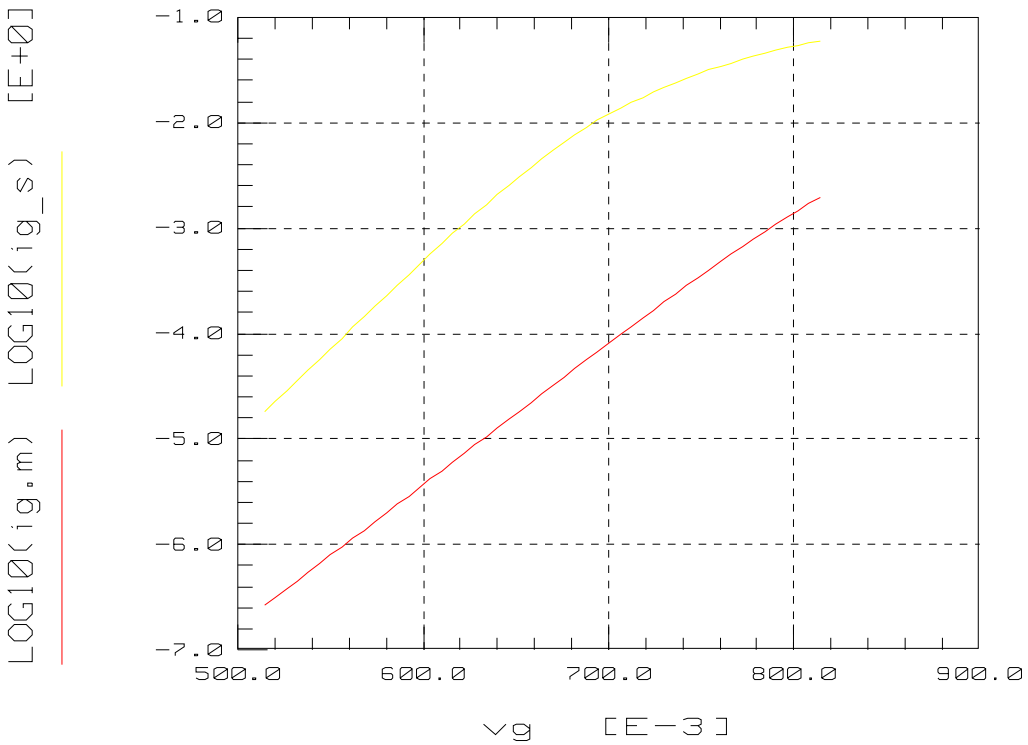

Figure 4.6: Log Plot of gate current (I_g) vs. gate voltage (V_g) for extraction of parameters I_s and N.

2. id_vgs_at_vdso

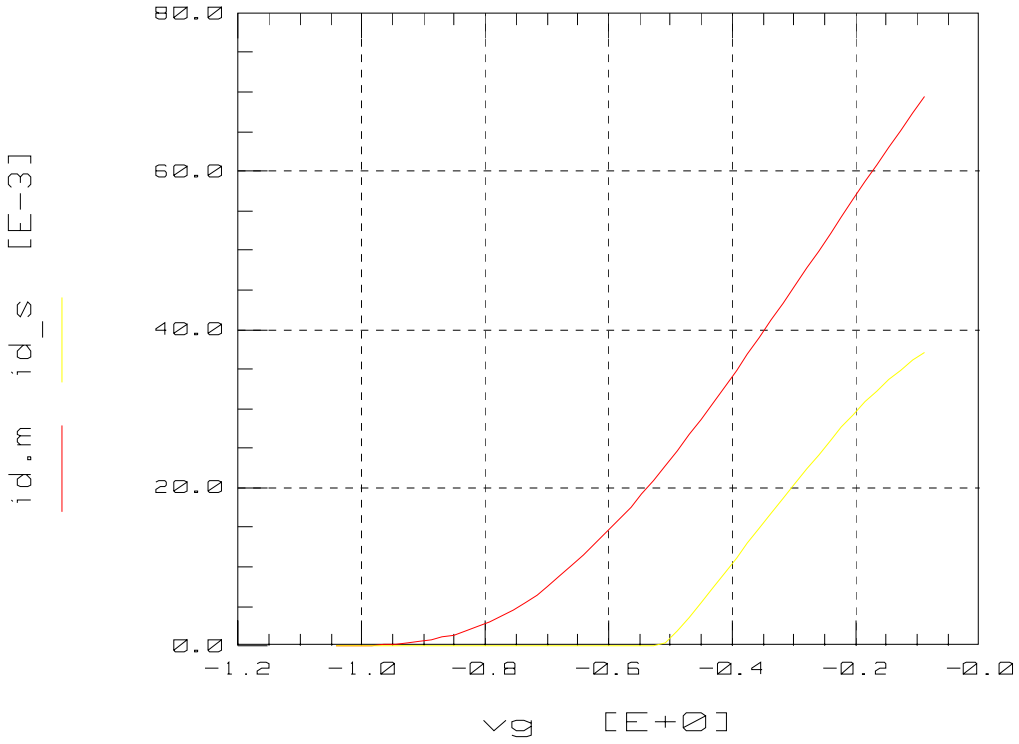

Figure 4.7: Drain Current (I_d) vs. gate voltage (V_g) at the condition of V_{dso} (output voltage "V_{ds}" where Vo "V_{ds},V_d" dependence disappears from equations [13]*)*

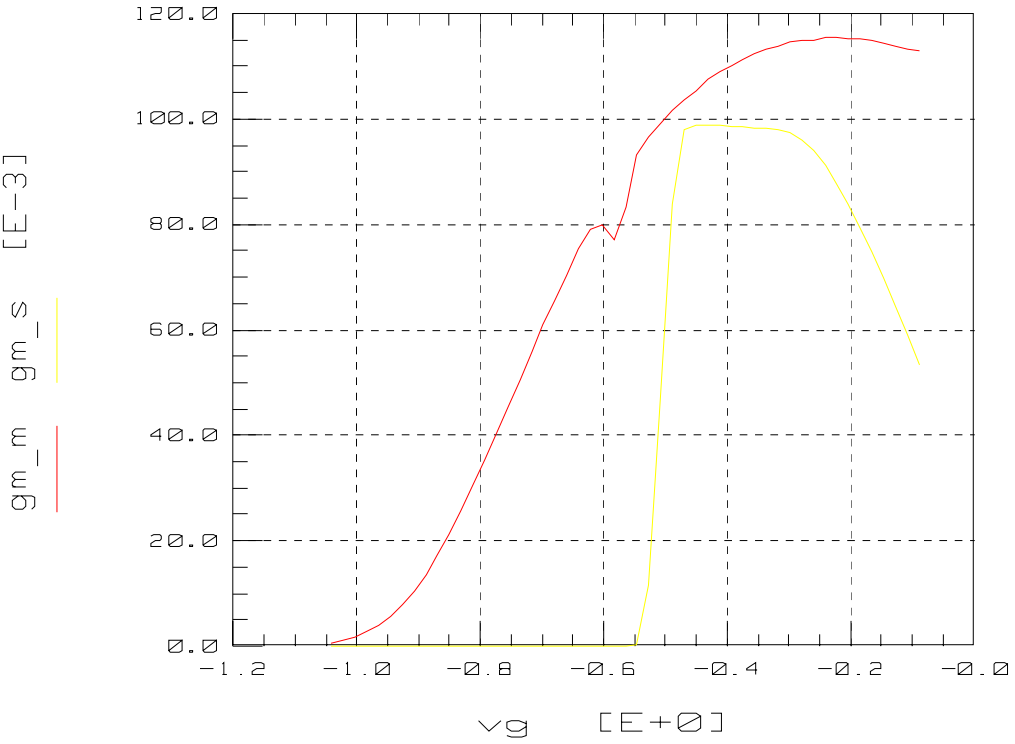

Figure 4.8: Preview of transconductance (g_m) vs. gate voltage (V_g)

3. id_vgs

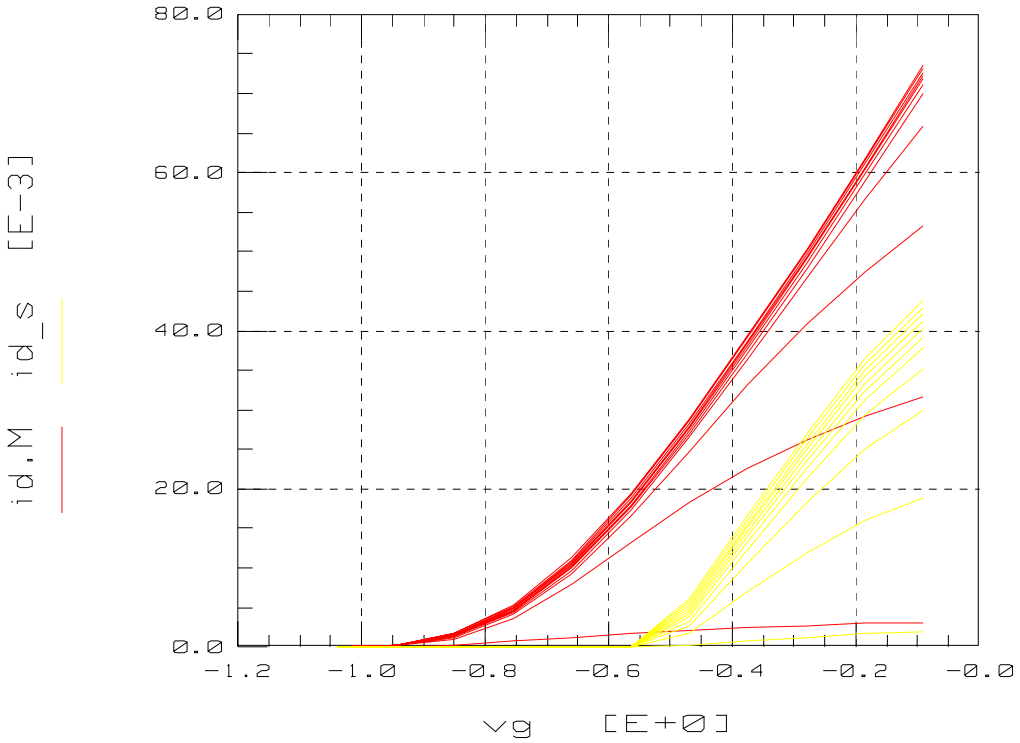

Figure 4.9: drain current (I_d) vs. gate voltage (V_g) with varying drain voltage (V_d)

4. id_vds

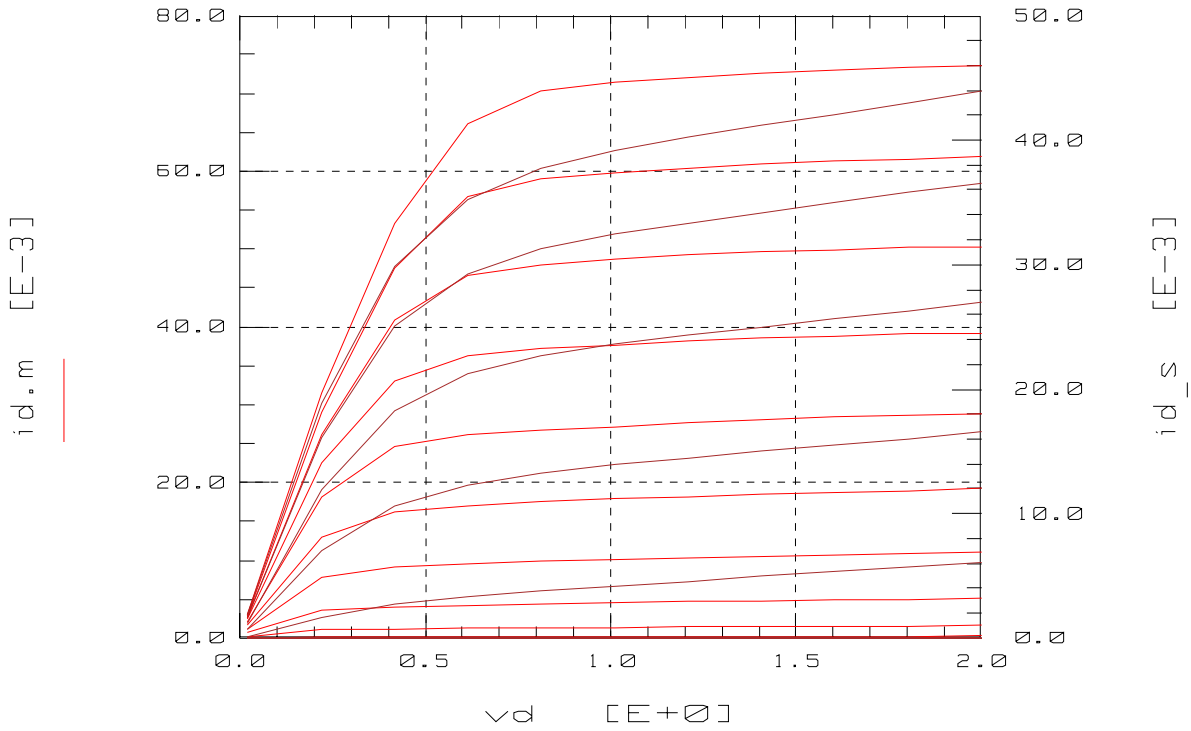

Figure 4.10: Measured and simulated drain current (I_d) vs. drain voltage (V_{ds}, or V_d)

4.3 Capacitance Measurements/ Basic Small Circuit Parameter Measurements

The capacitance measurements within the EEHEMT model extraction macro within IC-CAP utilizes extraction methods from data collected for the gate-to-drain capacitance (C_{gd}) and the drain-to-source capacitance (C_{ds}) as well as the input capacitance, C_{11}. The following plots show the measured and simulated data.

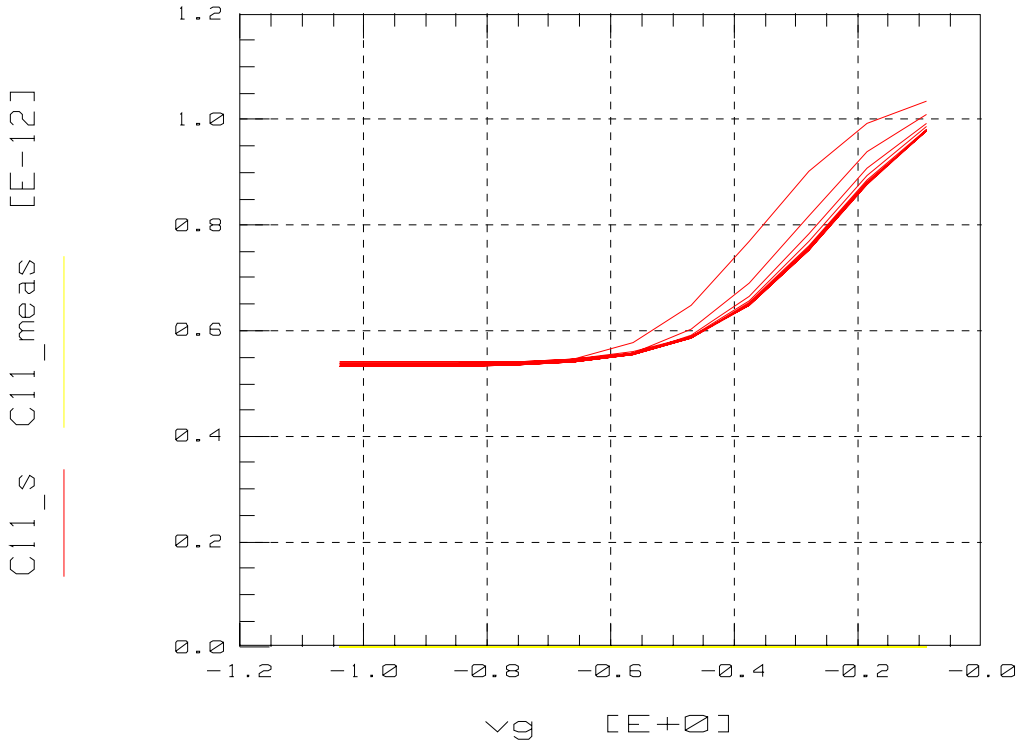

Figure 4.11: C_{11} simulated vs. negative gate voltage (V_g)

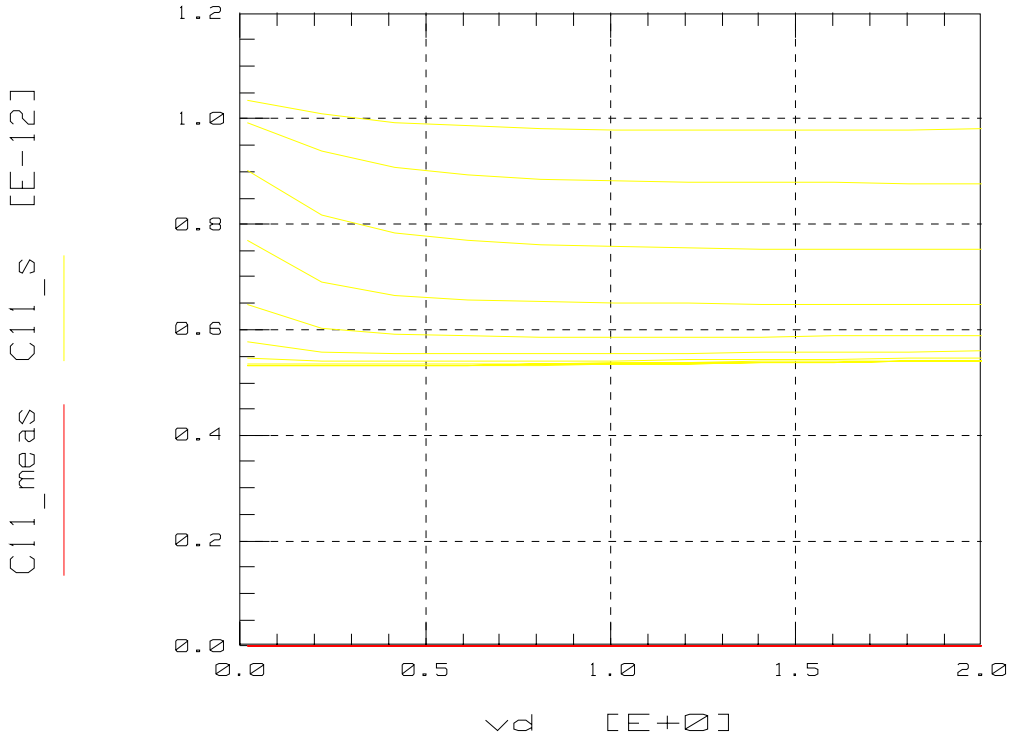

Figure 4.12: C_{11} *simulated vs. positive gate voltage* (V_g)

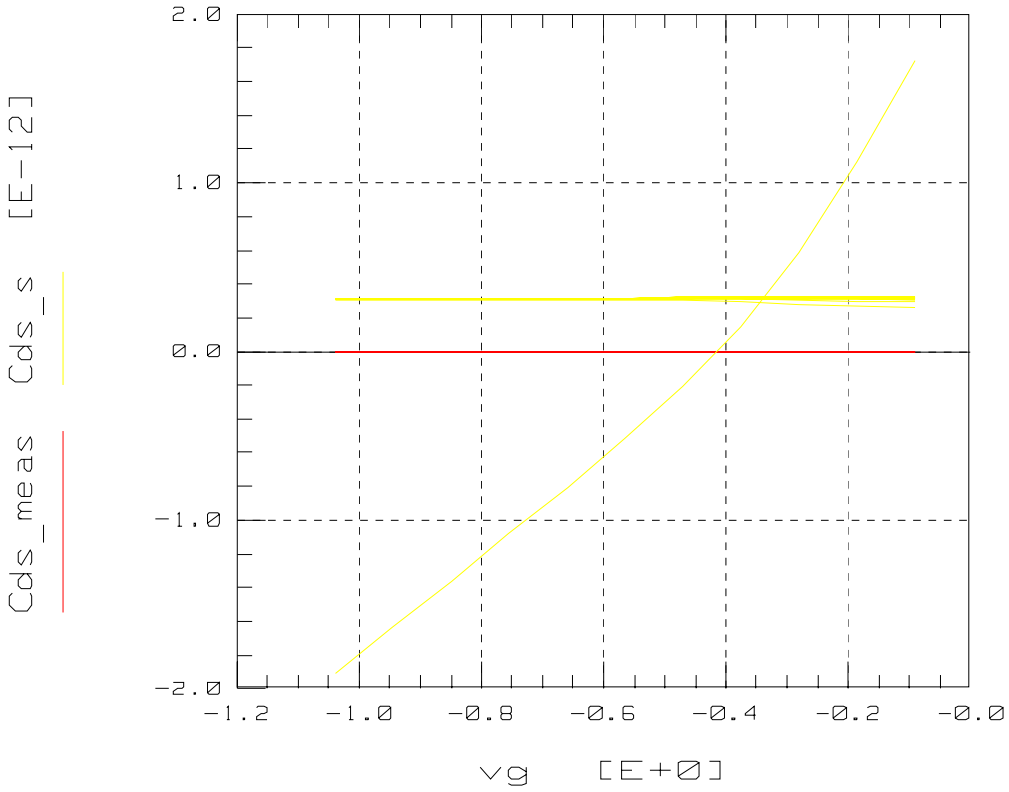

Figure 4.13: C_{ds} *simulated vs. negative gate voltage* (V_g)

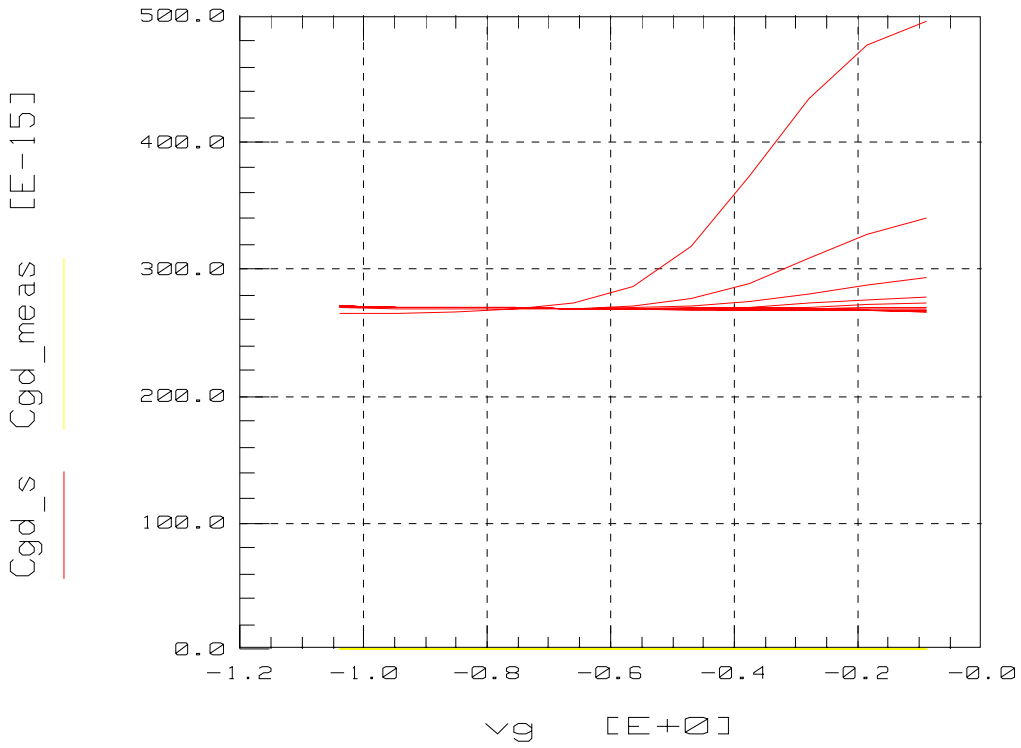

Figure 4.14: Gate-to-drain capacitance (C_{gd}) vs. gate voltage (V_g) over different bias conditions.

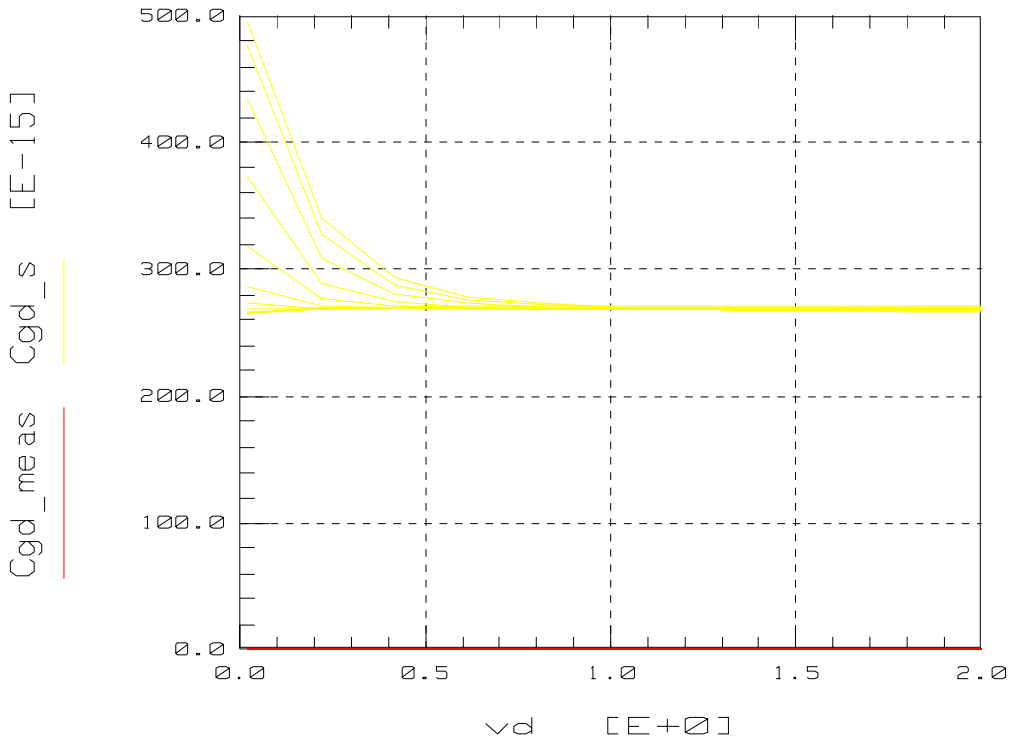

Figure 4.15: Gate-to-drain capacitance (C_{gd}) vs. drain voltage (V_d) across different gate voltages (V_g)

This section also includes other parameters of the pHEMT model: tau (τ), the drain-to-source conductance (g_{ds}), and the transconductance (g_m). Tau (τ) is the model representation of the gate transit time delay and drain-to-source conductance (g_{ds}) is the inverse of the drain-to-source resistance (R_{ds}) or otherwise known as the "on resistance", R_{on}.

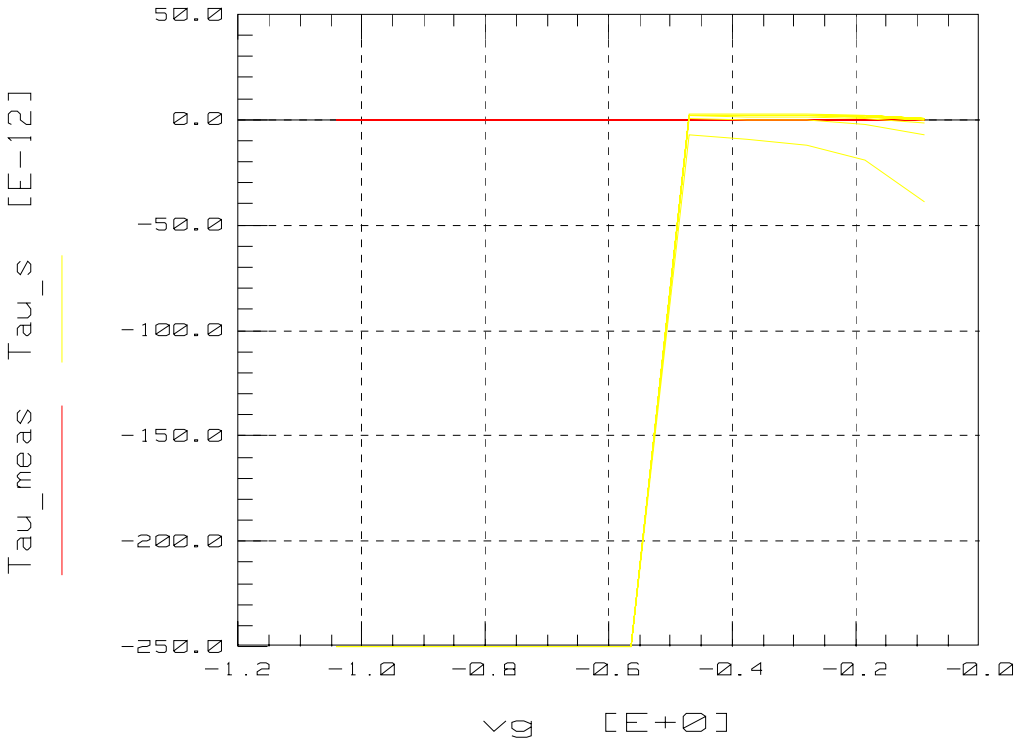

Figure 4.16: Gate transit time delay (τ) vs. gate voltage (V_g)

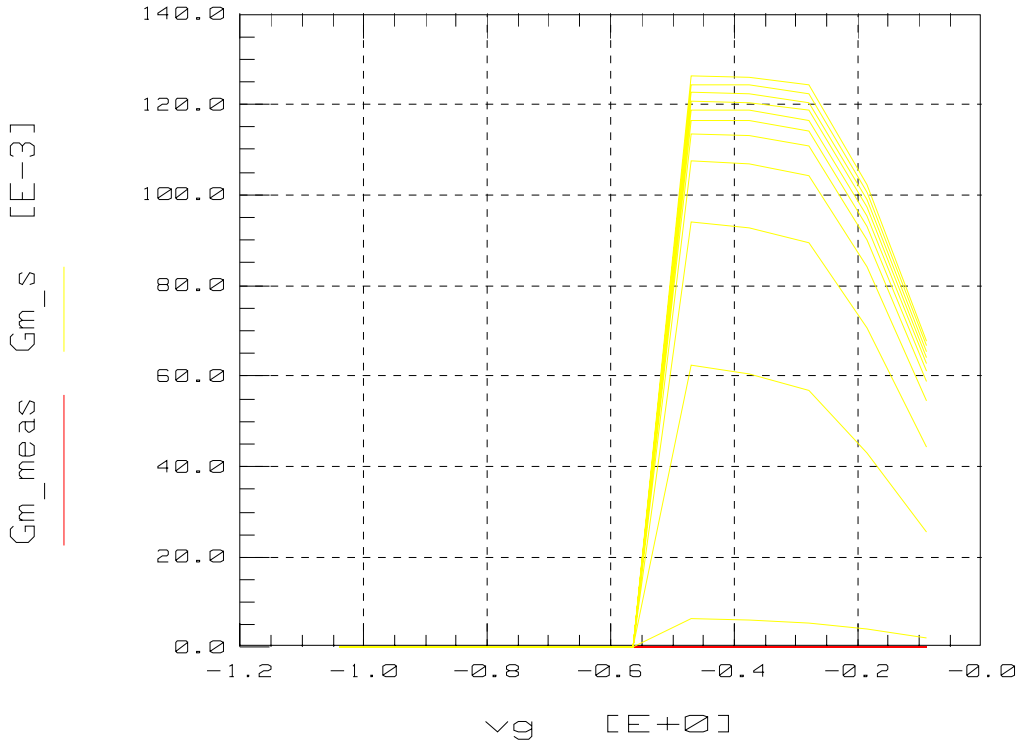

Figure 4.17: Transconductance (G_m) vs. gate voltage (V_g) as function of drain voltages (V_d)

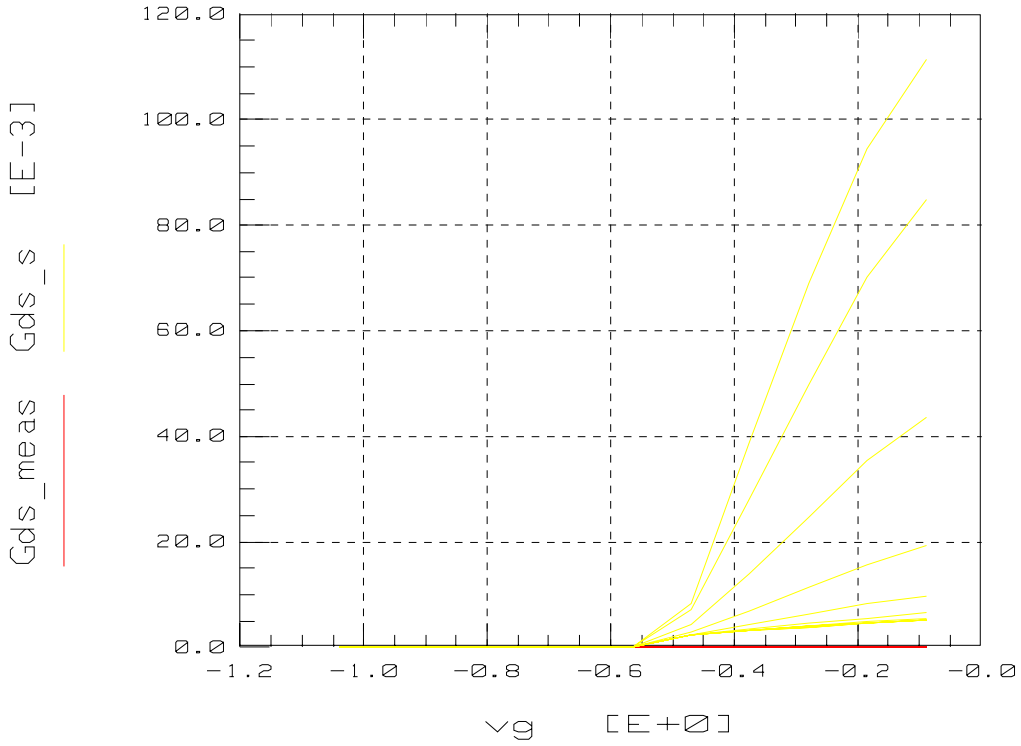

Figure 4.18: Drain-to-source conductance (G_{ds}) vs. gate voltage (V_g) for various drain voltages values (V_d) from -0.5 - 0.5 V

4.4 S-Parameter Measurements

The S-parameter measurements taken on this pHEMT device are separated into different bias conditions. S_{11}, S_{21}, S_{12}, and S_{22} were measured at each bias condition. Each test sequence is uniquely named to correspond to the variable settings within IC-CAP. AC_ON1, AC_ON2, and AC_ON3 test setups all utilize linear sweeps of each parameter. AC_ON4 uses a synchronous sweep of the gate voltage (V_g) depending on the drain voltage (V_d).

Below is a list of test names and conditions for AC_ON1-AC_ON4 as well as AC_OFF1 and AC_OFF2. The actual measured levels will be presented in the corresponding sections below.

AC_ON1

Frequency:	FREQ_START	FREQ_STOP	FREQ_POINTS
V_{gs}:	VGS_ON1_start	VGS_ON1_stop	VGS_ON1_coarse
V_{ds}:	VDS_ON1_start	VDS_ON1_stop	VDS_ON1_coarse

AC_ON2

Frequency:	FREQ_START	FREQ_STOP	FREQ_POINTS
V_{gs}:	VGS_ON2_start	VGS_ON2_stop	VGS_ON2_coarse
V_{ds}:	VDS_ON2_start	VDS_ON2_stop	VDS_ON2_coarse

AC_ON3

Frequency:	FREQ_START	FREQ_STOP	FREQ_POINTS
V_{gs}:	VGS_ON3_start	VGS_ON3_stop	VGS_ON3_coarse
V_{ds}:	VDS_ON3_start	VDS_ON3_stop	VDS_ON3_coarse

AC_ON4

Frequency:	FREQ_START	FREQ_STOP	FREQ_POINTS
V_{gs} Ratio:	VGS_ON4_slope		
V_{gs} Offset:	VGS_ON4_offset		
V_{ds}:	VDS_ON4_start	VDS_ON4_stop	VDS_ON4_fine

AC_OFF1

Frequency:	FREQ_START	FREQ_STOP	FREQ_POINTS
V_{gs}:	VGS_OFF1_start	VGS_OFF1_stop	VGS_OFF1_coarse
V_{ds}:	VDS_OFF1_start	VDS_OFF1_stop	VDS_OFF1_coarse

AC_OFF2

Frequency:	FREQ_START	FREQ_STOP	FREQ_POINTS
V_{gs} Ratio:	VGS_OFF2_slope		
V_{gs} Offset:	VGS_OFF2_offset		
V_{ds}:	VDS_OFF2_start	VDS_OFF2_stop	VDS_OFF2_fine

(AC_ON1)

For this case, the DC biasing is at fixed values. The frequency sweep from 45 MHz to 20 GHz , with a total number of frequency points of 50. The gate voltage (V_g) was swept from -0.5 V to 0.5 V with 6 steps. The drain voltage (V_d) was swept from 0 V to 1.3 V with 6 steps. The different bias conditions can be seen in the following plots of S-parameters (Figures 4.19, 4.20, and 4.21) across the previously mentioned frequency span.

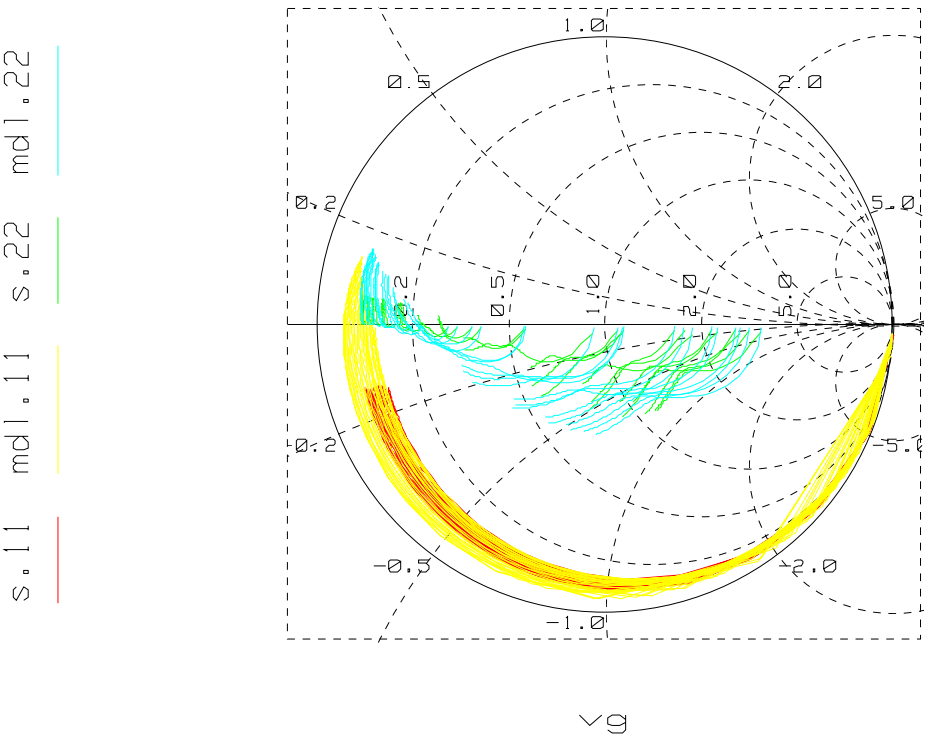

Figure 4.19: Measured and modeled S_{11} and S_{22} data for the AC_ON1 bias conditions.

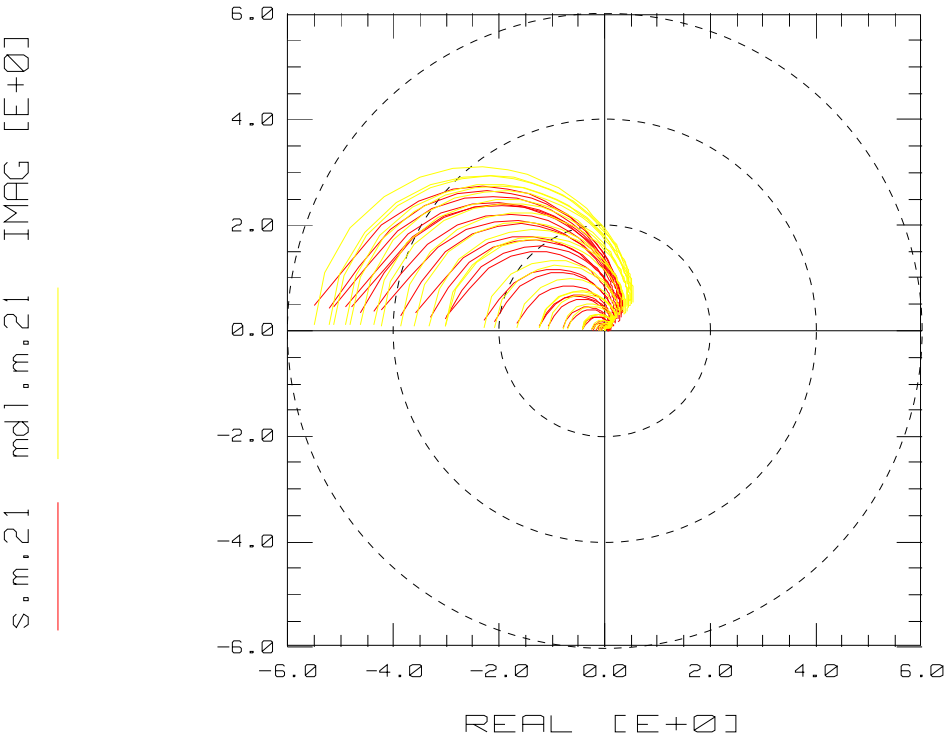

Figure 4.20: Measured and modeled S_{21} data across frequency on a polar plot.

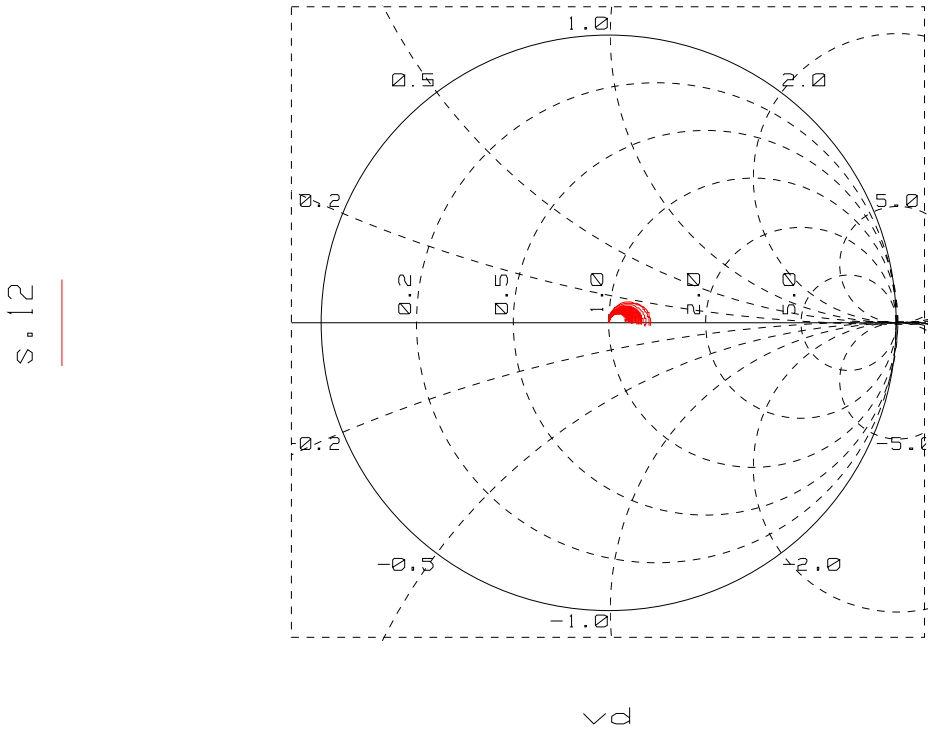

Figure 4.21: Measured S_{12} across frequency and bias conditions of AC_ON1.

(AC_ON2)

For this case, the DC biasing is at the second chosen levels. The frequency sweep started at 45 MHz and was swept to a final frequency of 20 GHz as in the condition set of AC_ON1. The number of frequency points was 50. The gate voltage (V_g) was swept from -0.5 V to 0.5 V with 6 steps. The drain voltage (V_d) was swept from -0.5 V to 0.5 V with 6 steps. The different bias conditions can be seen in the following plots of S-parameters (Figures 4.22, 4.23, and 4.24) across the previously mentioned frequency span.

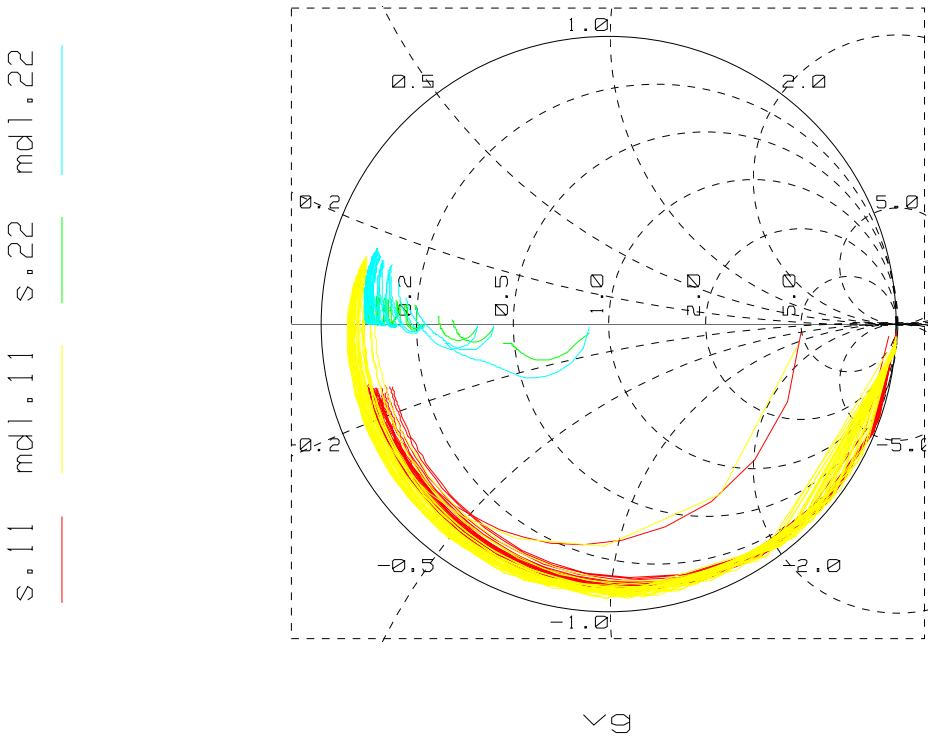

Figure 4.22: Measured and modeled S_{11} and S_{22} data for the AC_ON2 bias conditions.

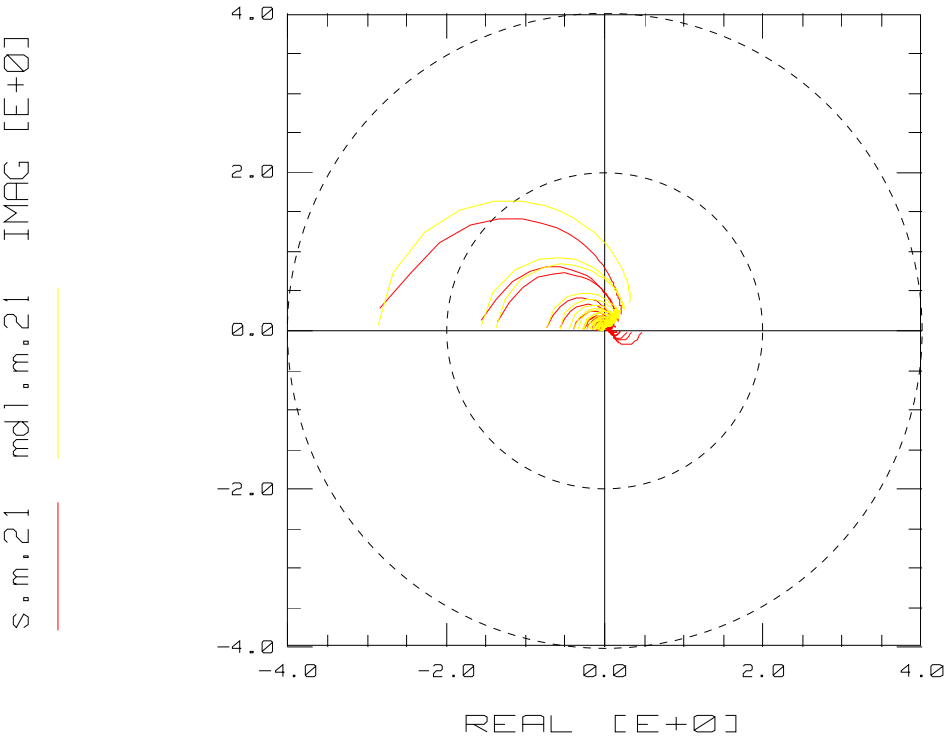

Figure 4.23: Measured and modeled S_{21} data across frequency on a polar plot.

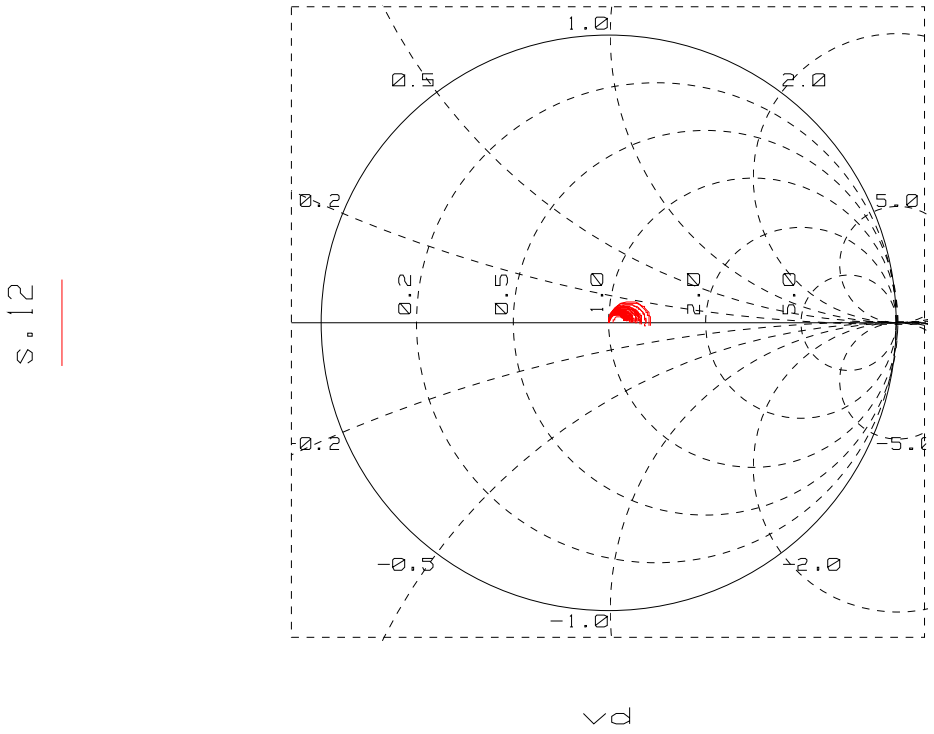

Figure 4.24: Measured S_{12} across frequency and bias conditions of AC_ON2.

(AC_ON3)

For this case, the DC biasing is at the third chosen levels. The frequency sweep started at 45 MHz and was swept to a final frequency of 20 GHz as in the condition set of AC_ON1 and AC_ON2. The number of frequency points was 50. The gate voltage (V_g) was swept from -0.5 V to 0.5 V with 6 steps. The drain voltage (V_d) was swept from -0.5 V to 0.5 V with 6 steps. The different bias conditions can be seen in the following plots of S-parameters (Figures 4.25, 4.26, and 4.27) across the previously mentioned frequency span. This condition set is exactly the same as AC_ON2 and therefore provides the same data set.

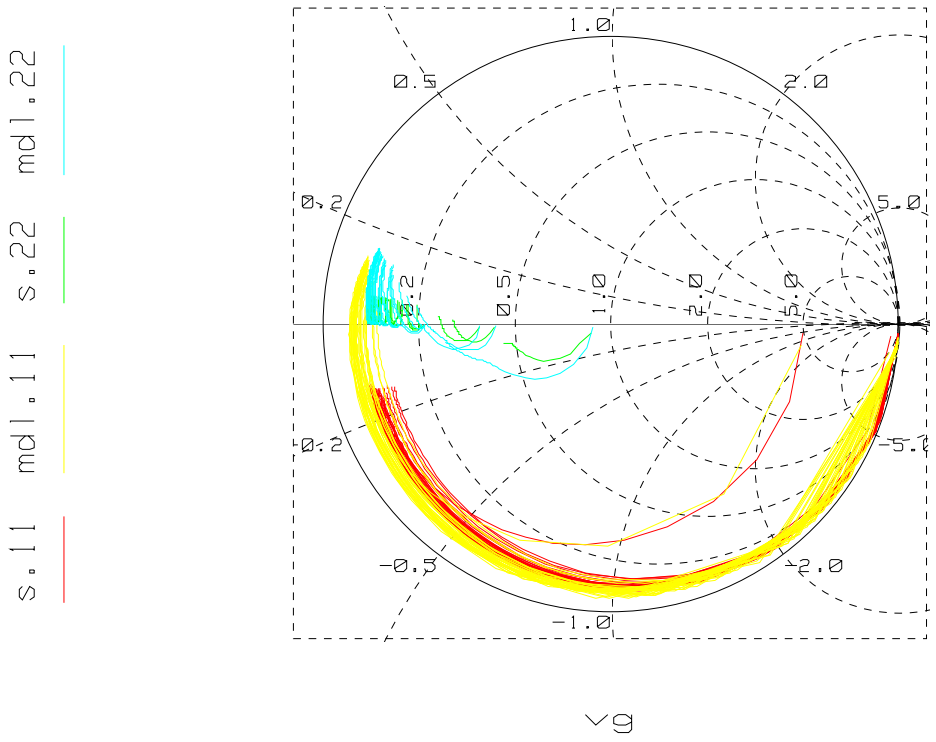

Figure 4.25: Measured and modeled S_{11} and S_{22} data for the AC_ON3 bias conditions.

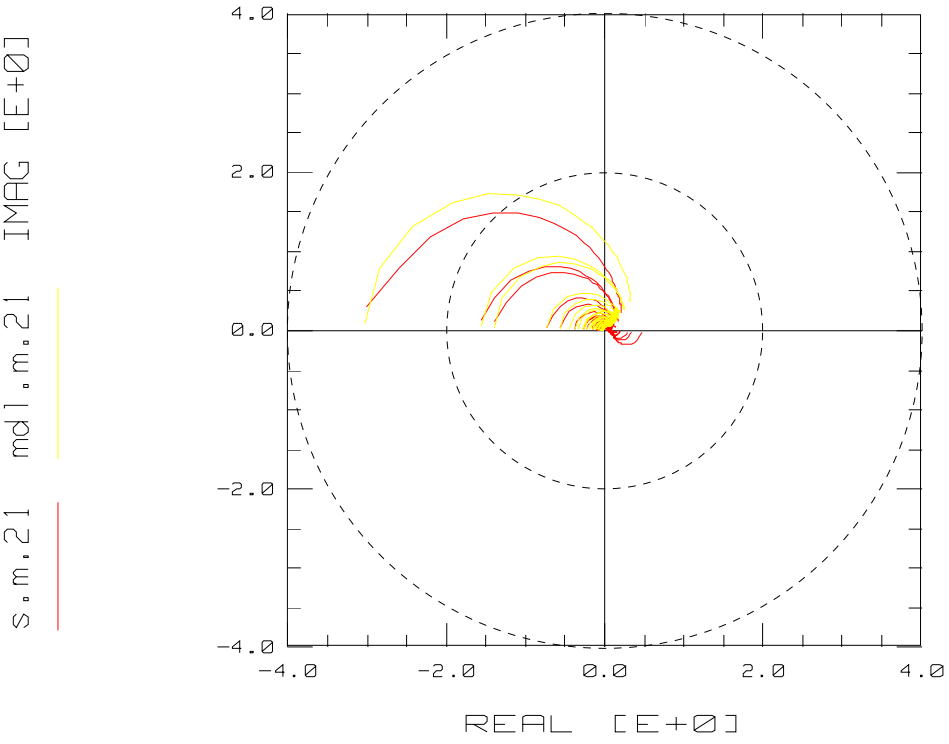

Figure 4.26: Measured and modeled S_{21} data across frequency on a polar plot.

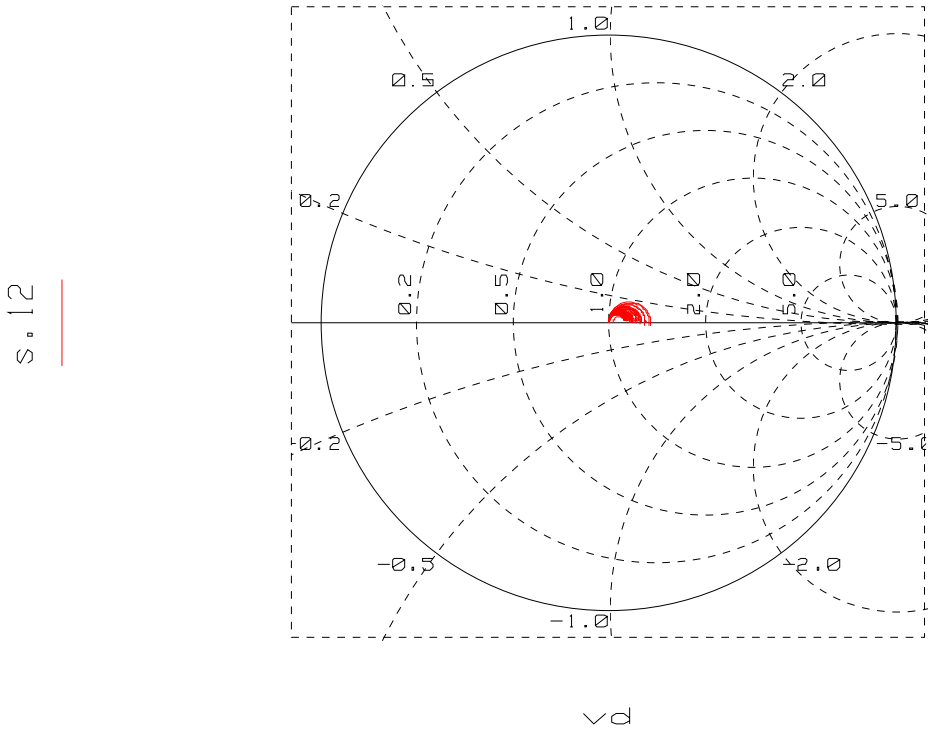

Figure 4.27: Measured S_{12} across frequency and bias conditions of AC_ON3.

(AC_ON4)

For this case, the DC biasing is at the fourth chosen levels. The frequency sweep started at 45 MHz and was swept to a final frequency of 20 GHz as in the condition set of AC_ON1, AC_ON2, and AC_ON3. The number of frequency points was 50. The gate voltage (V_g) was swept in sync with the drain voltage. The slope of the gate voltage (V_g) was 0.5 while the offset was 0V. The drain voltage (V_d) was swept from -1.3 V to 1.3 V with 41 steps. The different bias conditions can be seen in the following plots of S-parameters (Figures 4.28, 4.29, and 4.30) across the previously mentioned frequency span.

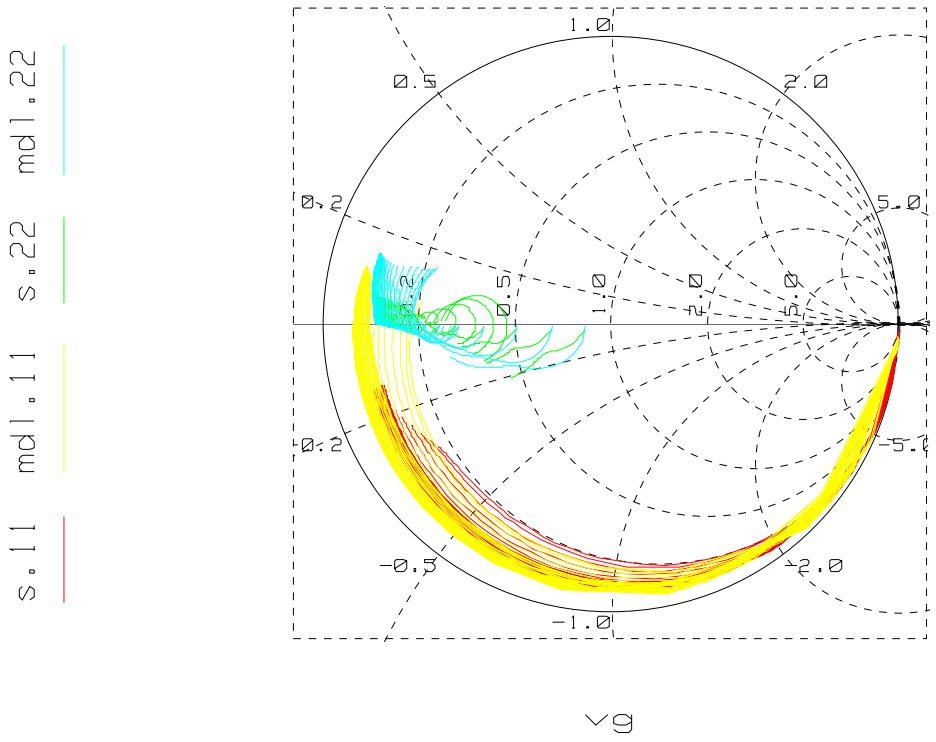

Figure 4.28: Measured and modeled S_{11} and S_{22} data for the AC_ON4 bias conditions.

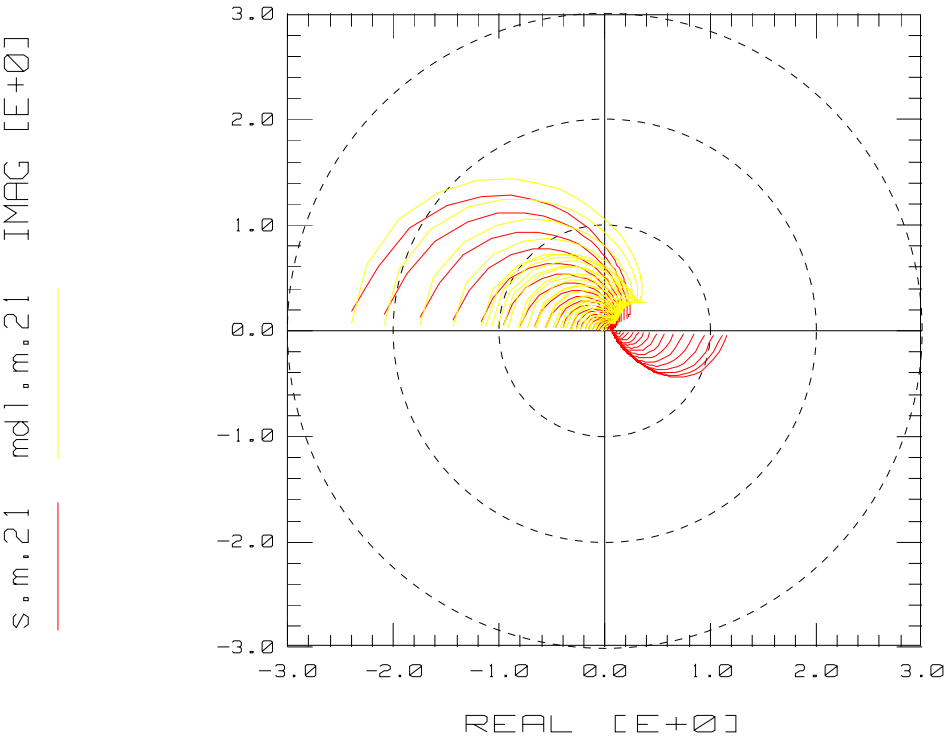

Figure 4.29: Measured and modeled S_{21} data across frequency on a polar plot.

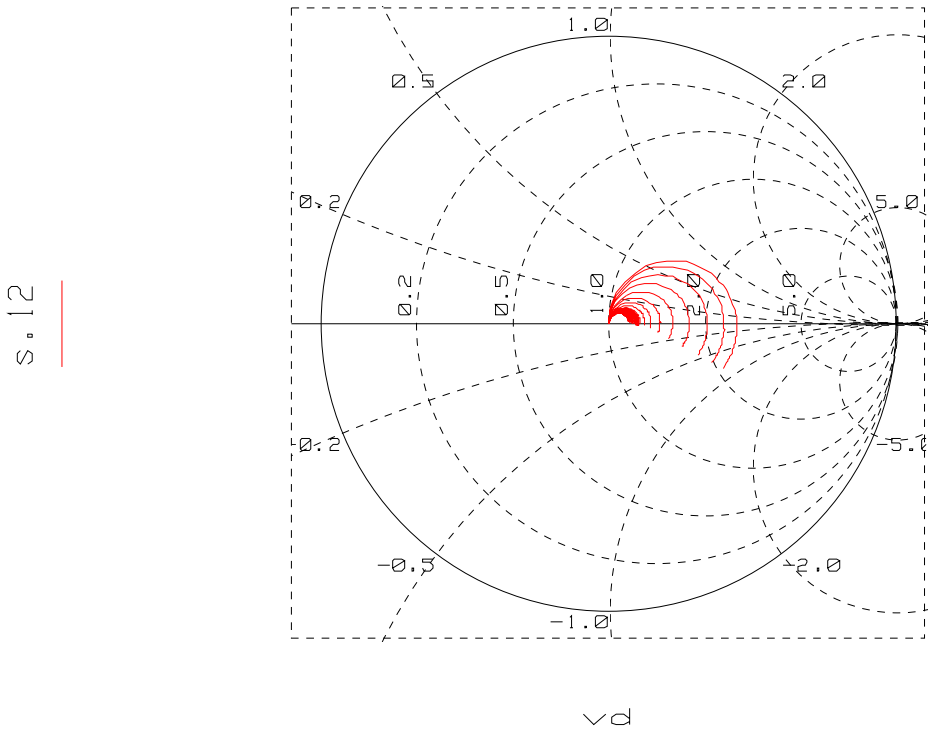

Figure 4.30: Measured S_{12} across frequency and bias conditions of AC_ON4.

(AC_OFF1)

For this case, the DC biasing is at the fifth chosen levels. The frequency sweep started at 45 MHz and was swept to a final frequency of 20 GHz as in all previous condition sets. The number of frequency points was 50. The gate voltage (V_g) was from -5 V to -0.8 V. This voltage is never allowed to go positive, so therefore the pHEMT is always in the "OFF" condition. The drain voltage (V_d) was swept from 0 V to 3 V with 6 steps. The different bias conditions can be seen in the following plots of S-parameters (Figures 4.31, 4.32, and 4.33) across the previously mentioned frequency span.

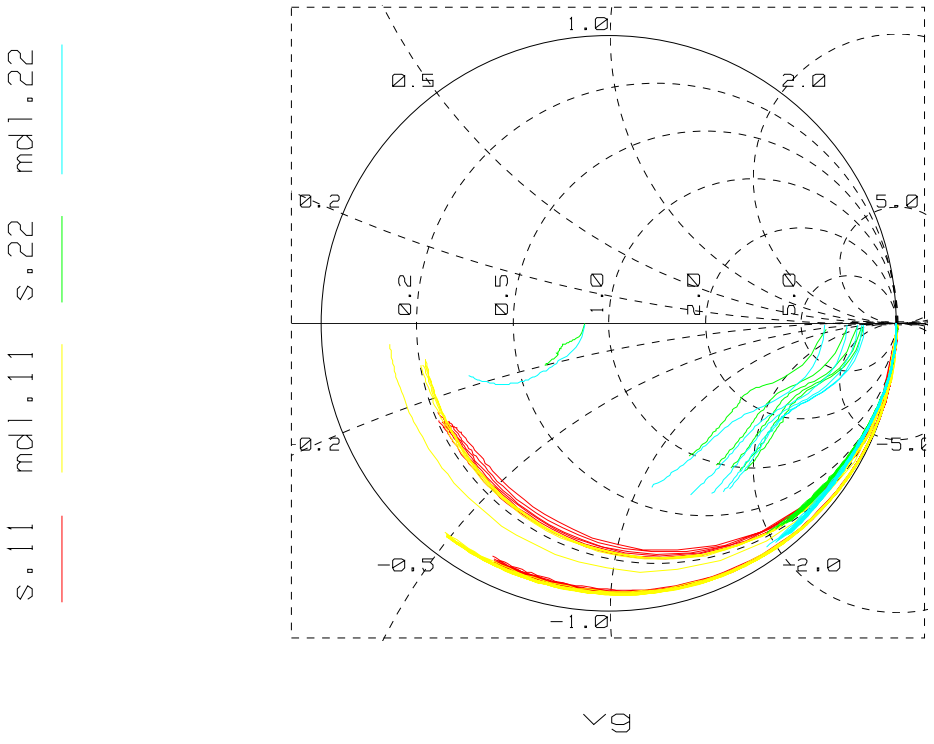

Figure 4.31: Measured and modeled S_{11} and S_{22} data for the AC_OFF1 bias conditions.

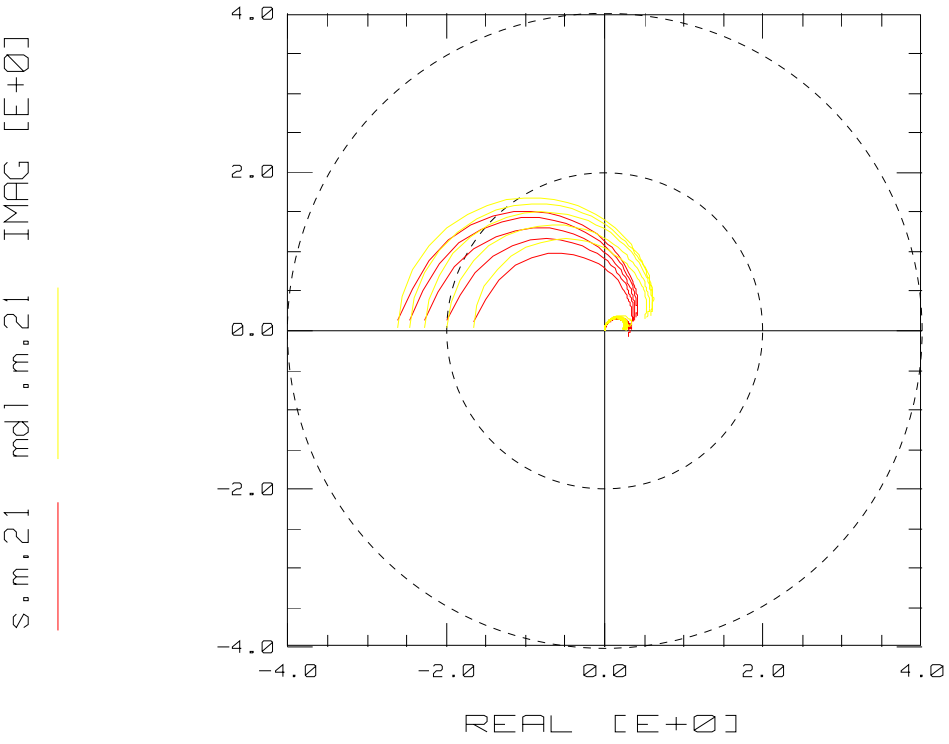

Figure 4.32: Measured and modeled S_{21} data across frequency on a polar plot.

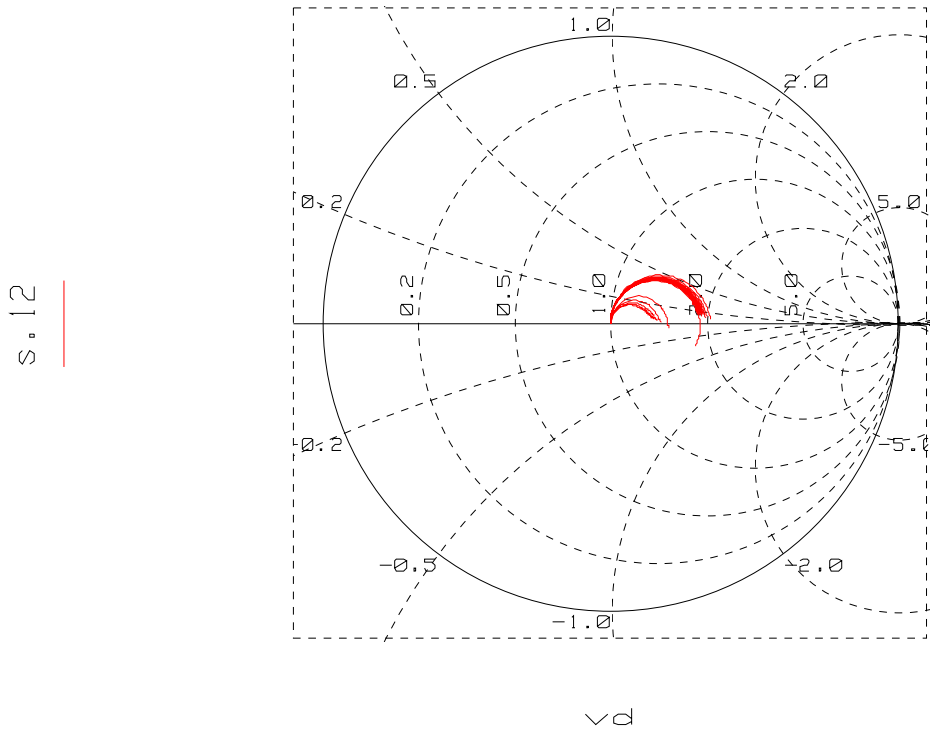

Figure 4.33: Measured S_{12} across frequency and bias conditions of AC_OFF1.

(AC_OFF2)

For this case, the DC biasing is at the sixth chosen levels and is operating in the "OFF" mode. The frequency sweep started at 45 MHz and was swept to a final frequency of 20 GHz as in all previous condition sets. The number of frequency points was 50. The measurement and simulation was a sync measurement, and the gate voltage (V_g) had a slope of 0.5 dependent on the drain voltage (V_d). The drain voltage (V_d) was swept from -5 V to 5 V with 41 steps. The different bias conditions can be seen in the following plots of S-parameters (Figures 4.34, 4.35, and 4.36) across the previously mentioned frequency span.

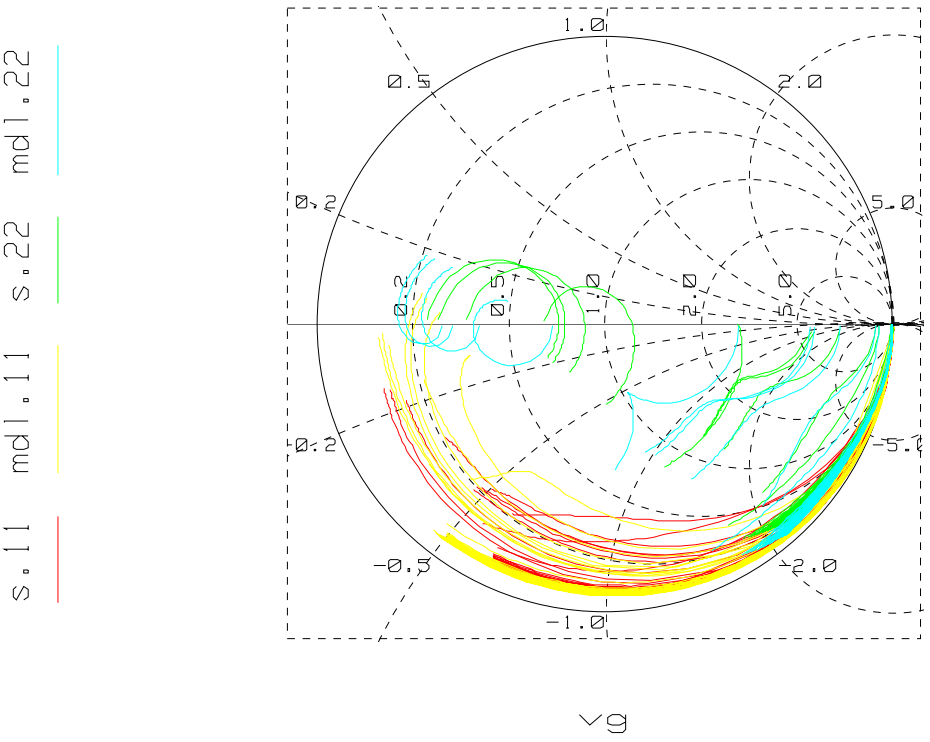

Figure 4.34: Measured and modeled S_{11} and S_{22} data for the AC_OFF2 bias conditions.

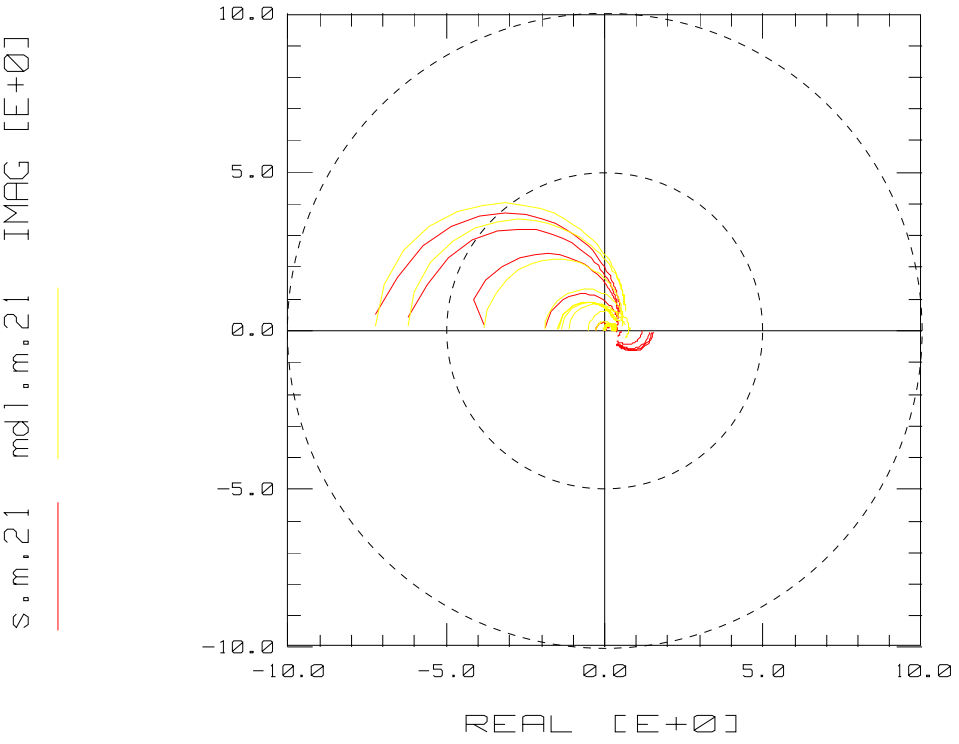

Figure 4.35: Measured and modeled S_{21} data across frequency on a polar plot.

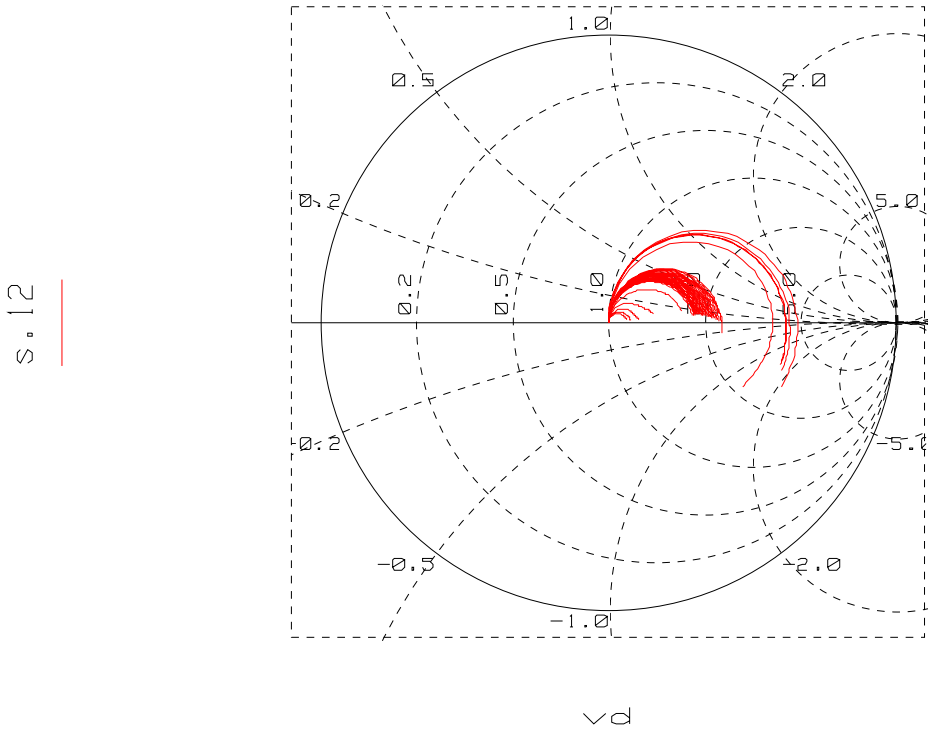

Figure 4.36: Measured S_{12} across frequency and bias conditions of AC_OFF1.

4.5 Data Comparison

When looking at the data and trying to determine whether the extracted model is acceptable for simulation use in the market, the calculation of "% Error" is vital. With this model extraction, "% Error" was calculated for three of four S-parameters across frequency. Random bias conditions were chosen to reduce the number of data plots. "% Error" was calculated by the formula [11]:

$$\%Error = \frac{S_{ij\_meas} - S_{ij\_sim}}{S_{ij\_meas}} * 100 \qquad \text{(eqn. 4.1)}$$

Random conditions of "% Error" for S_{11}, S_{21}, and S_{22} were calculated and reported in the following set of figures. S_{12} was not calculated due to the IC-CAP setup not reporting S_{12} modeled data.

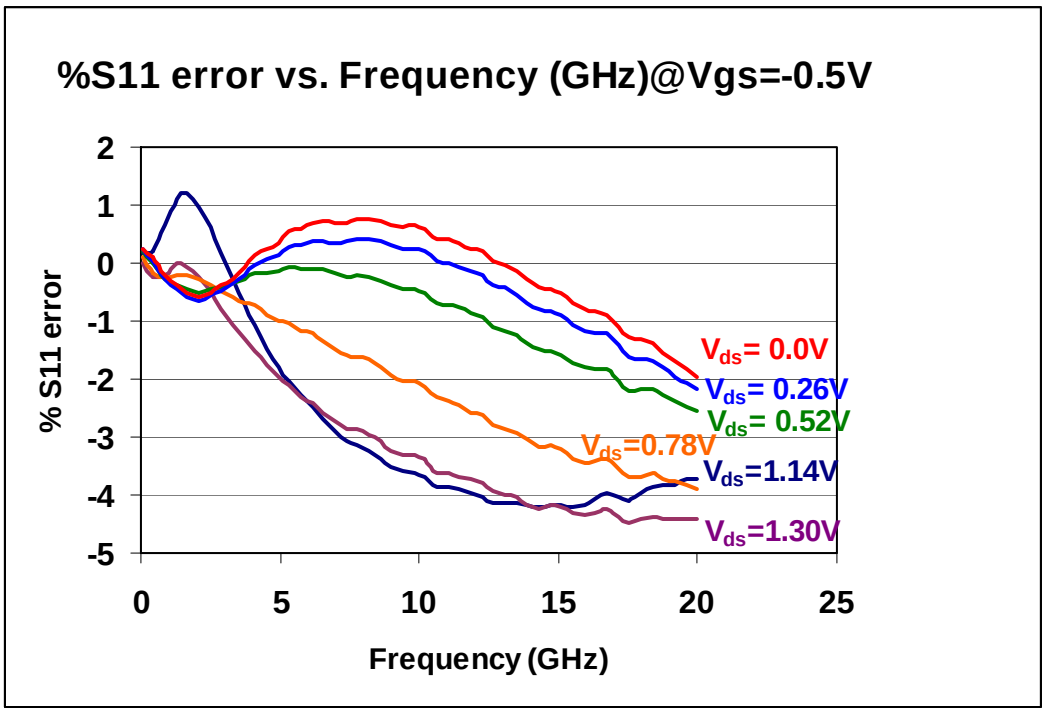

Figure 4.37: % S_{11} Error calculation across frequency for V_{gs}=-0.5 V and a V_{ds} sweep from 0 - 1.3 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

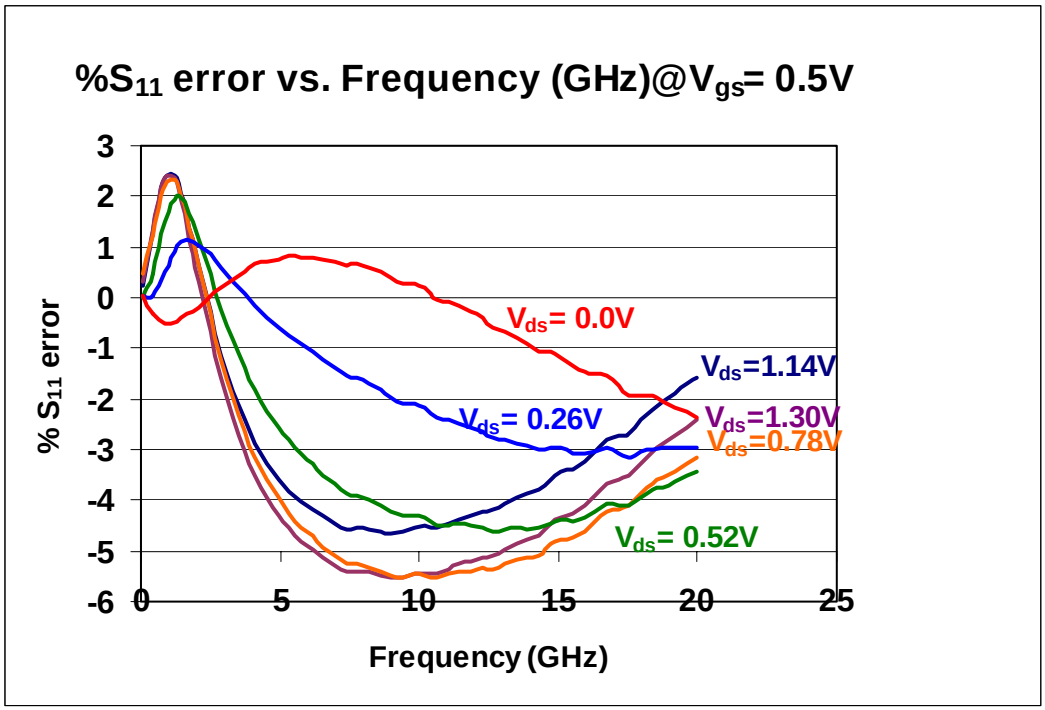

Figure 4.38: % S_{11} Error calculation across frequency for V_{gs}=0.5 V and a V_{ds} sweep from 0 - 1.3 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

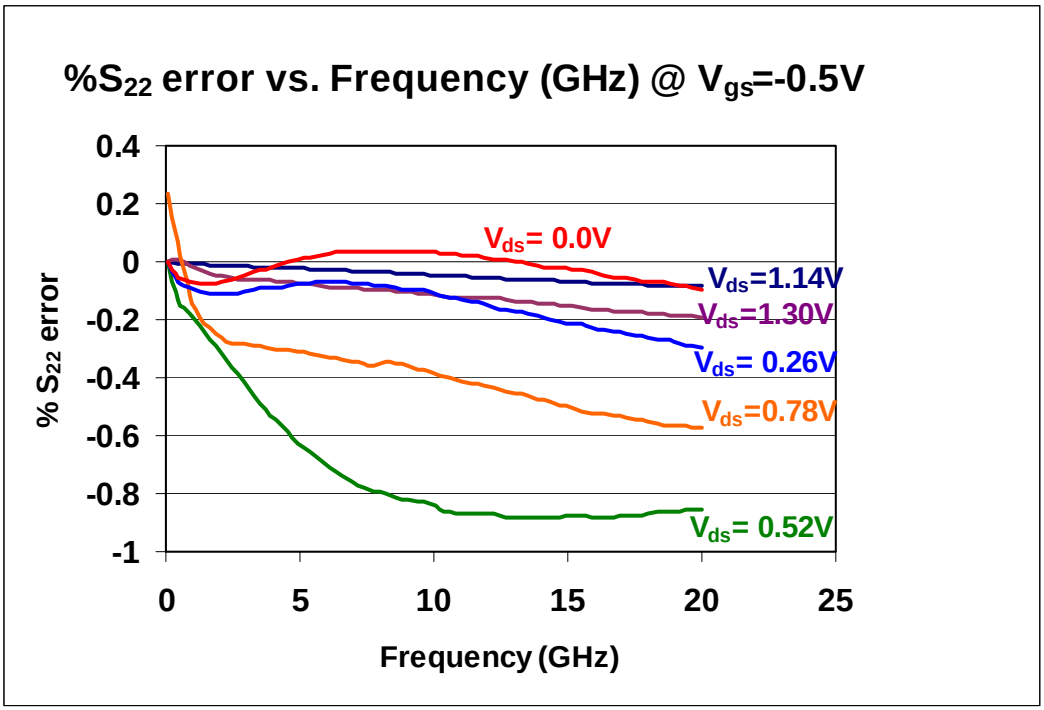

Figure 4.39: % S_{22} Error calculation across frequency for V_{gs}=-0.5 V and a V_{ds} sweep from 0 - 1.3 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

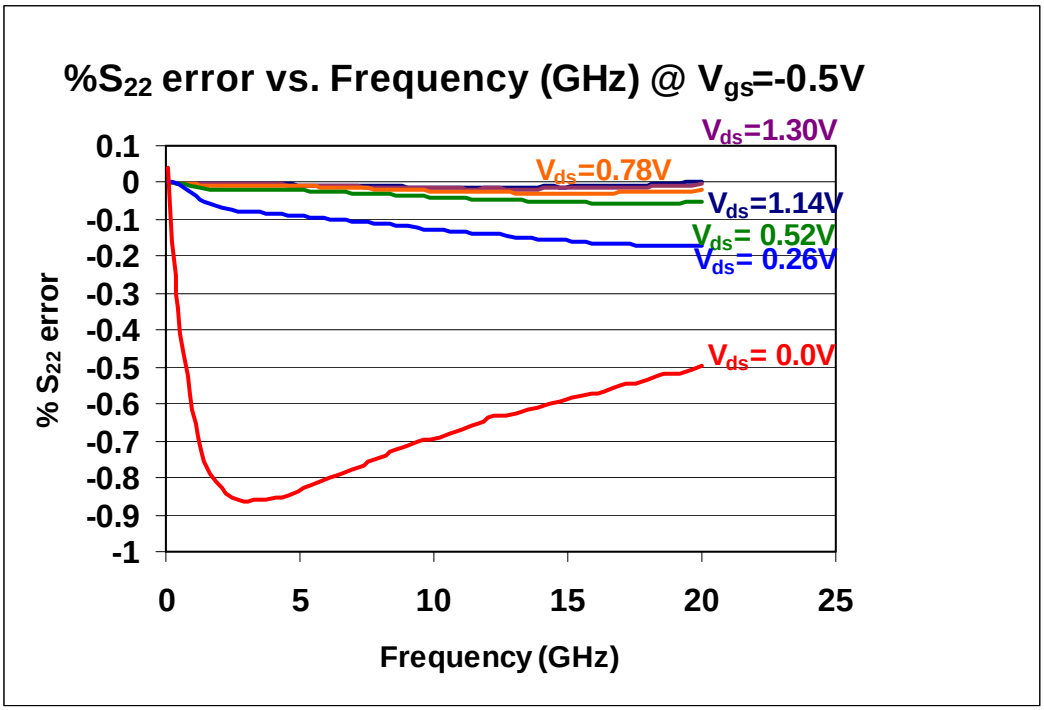

Figure 4.40: % S_{22} Error calculation across frequency for V_{gs}=-0.5 V and a V_{ds} sweep from 0 - 1.3 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

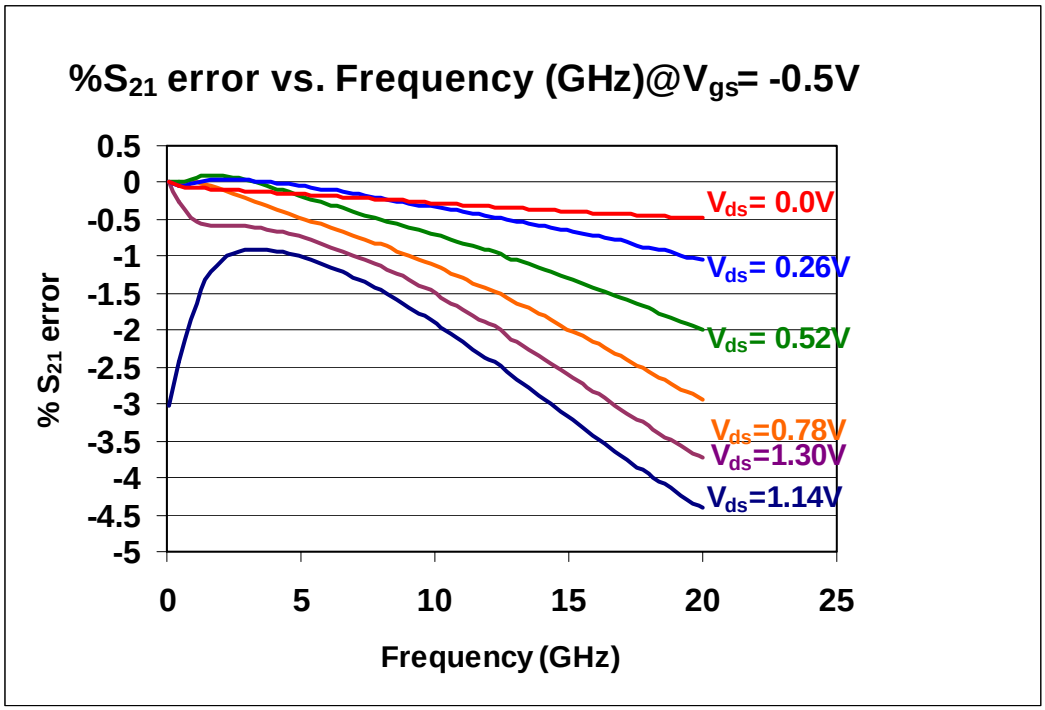

Figure 4.41: % S_{21} Error calculation across frequency for V_{gs}=-0.5 V and a V_{ds} sweep from 0 - 1.3 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

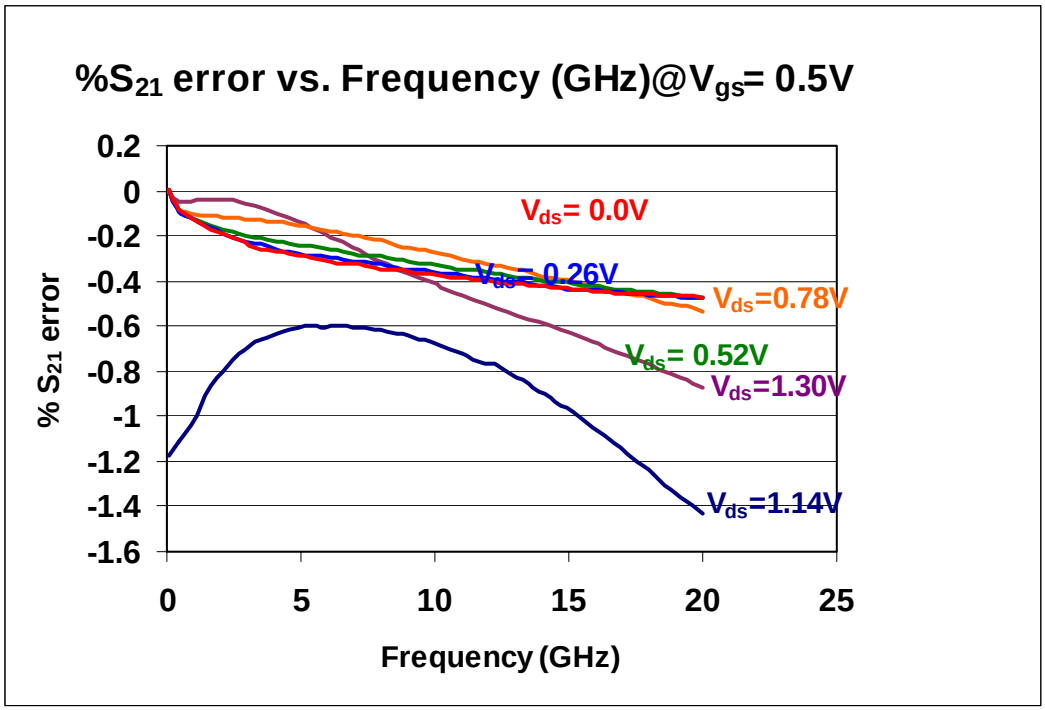

Figure 4.42: % S_{21} Error calculation across frequency for V_{gs}=0.5 V and a V_{ds} sweep from 0 - 1.3 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

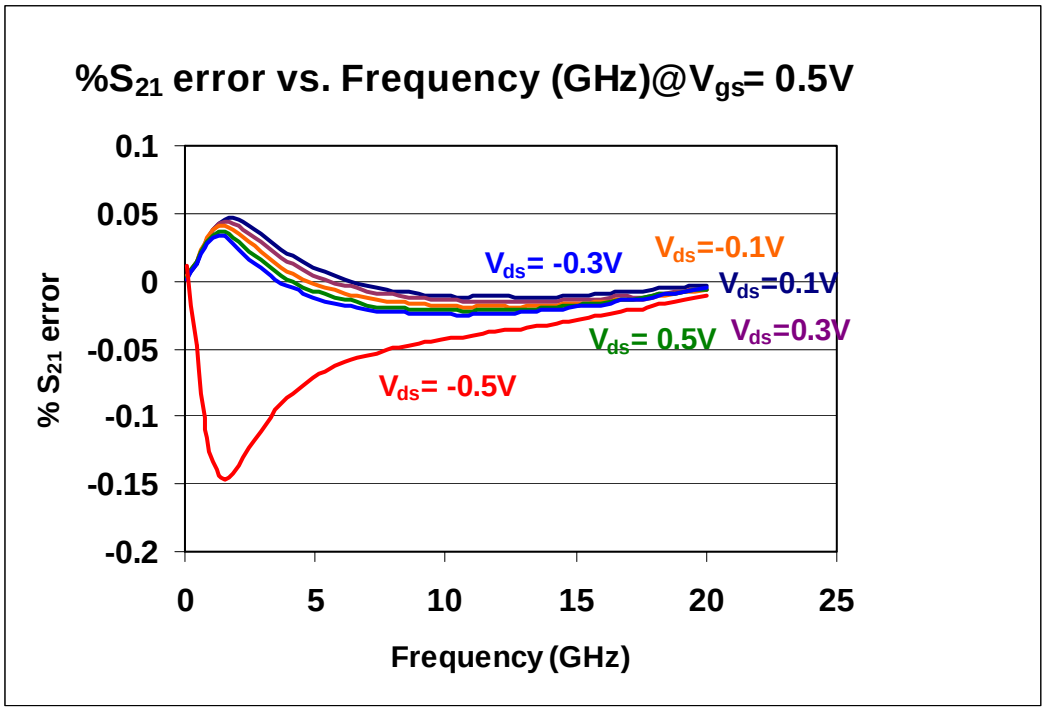

Figure 4.43: % S_{21} Error calculation across frequency for V_{gs}=0.5 V and a V_{ds} sweep from -0.5 – 0.5 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

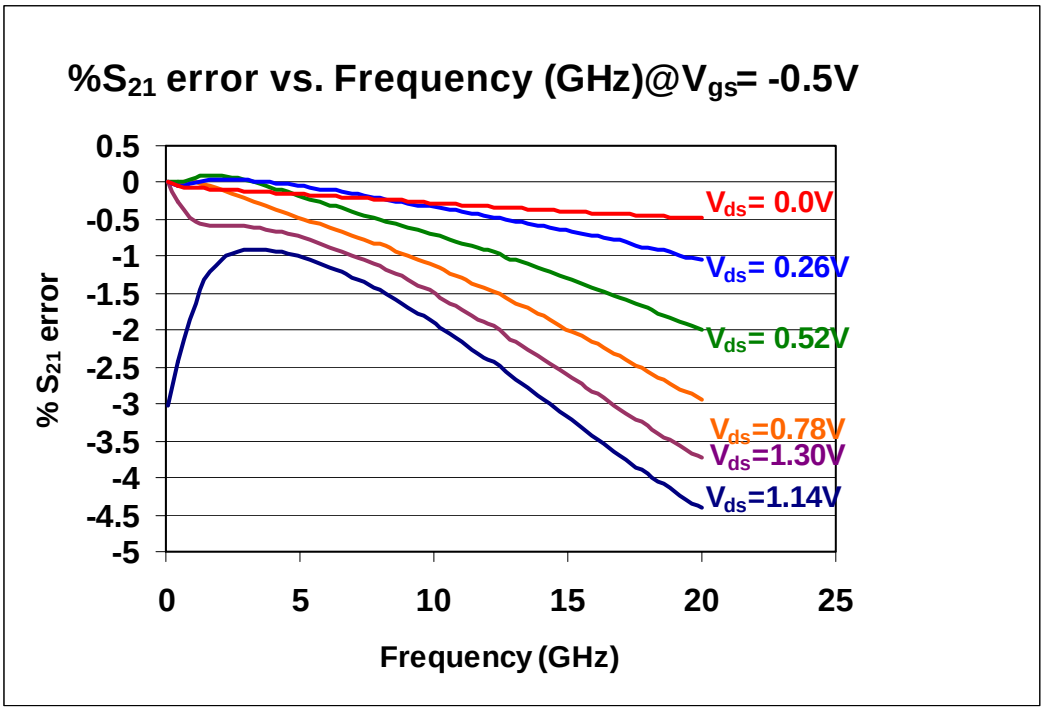

Figure 4.44: % S_{21} Error calculation across frequency for V_{gs}=-0.5 V and a V_{ds} sweep from 0 - 1.3 V. Spot Checks were made through all bias ranges of interest and % error remained under 5.5% throughout.

5. Conclusion

This thesis describes a preliminary model and extraction procedure for a pHEMT used as an RF switch. The methods investigated and used are largely a description of a collection of best known practices used for industrial applications. This Chapter outlines the results of the model extraction.

5.1 Model Accuracy

The AC model has a low % Error on magnitude. To reduce the magnitude and phase error, the model's small-signal parameters can be tuned (post extraction) to obtain a more accurate curve fit. This will obtain better model simulation in the ON and OFF regions of operation, but will change the DC model as well. Since S_{21} data % Error is low, this signifies that the DC model error is a software tuning issue and not a device issue.

A large-signal response analysis hasn't been completed at the current time and is not strictly required for accurate modeling for switching applications. This model is expected to encounter difficulties as a large-signal model. For large-signal response analysis, tracking the IV curves alone is not sufficient. Derivative tracking must be analyzed to properly address the large-signal response. It is expected that the model will not track the derivative of the triode region well, since this model extraction utilizes the hyperbolic tangent function. We can see this issue somewhat in the transconductance extraction as mentioned earlier.

The DC response requires additional refinements. By analyzing the simulation results verses the measured results, the accuracy is shown to vary by as much as 50%. This analysis is done in chapter 4. The preview measurements show the pinch-off voltage to be approximately 0.2V higher than the optimized data and "I_s" appears to be approximately 2 orders of magnitude different than measured data. The drain-to-source conductance (g_{ds}) also increases more than desired when sweeping gate voltage (V_g). This causes the IV curves to vary with increasing gate voltage (V_g). When looking at the extracted transconductance (g_m), a mathematical glitch can be seen. Since g_m is extracted from the derivative of the drain current curve, this glitch shouldn't be included and is probably the result of software issues. Manual methods should be employed to correctly determine the pinch off voltage and will be used for future model extractions.

Another possible issue can arise when trying to model longer devices (long gate lengths). The model could possible not be sufficient enough to match the distributed effects of

longer gate lengths. An investigation into this possible issue requires another model extraction be preformed utilizing a pHEMT with a longer gate structure.

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