ABSTRACT

SILVA, PRADEEP CHARLES. Intracellular Recording with Low-power Low-noise CMOS Voltage and Current Clamp Circuits. (Under the direction of Dr. Kevin Gard.)

The measurement and processing of electrophysiological signals is a fundamental task performed by neuroscientists, as a means to gaining an insight into how biological systems respond to external stimuli and communicate with each other. Recently, the advent of microelectrode arrays has created the need to design low-power implantable electronic systems that are capable of recording neural activity while not causing permanent damage to the neural systems under observation. Such systems would prove invaluable in furthering our understanding of the electrical function of neurons in regard to drug interactions and mental functions and their interactions with other neurons and muscles.

This work investigates the design of the electronic components of such an implantable recording system. Low-power and low-noise current-clamp and voltage-clamp recording setups are designed. In addition, automated methods to combat the non-idealities in the recording introduced by the presence of electrodes for interfacing with neurons are proposed. Simulations have shown these methods to be effective in reducing the stray capacitance to $<$1 pF and to achieve 100% series resistance compensation while ensuring closed-loop stability. The power consumed in each of these recording setups is $<$500 μW . We also propose a system that will enable voltage-clamp controlled current-clamp recordings from cells for the measurement of action potentials or synaptic potentials while allowing the experimenter to determine the averaged membrane potential at which such recordings are performed.

This automated and integrated approach to intracellular recording will facilitate the implementation of system-on-chip solutions that can be integrated onto the intracellular electrode. Such configurations would aid neuroscientists in performing accurate and high-throughput experiments *in-vitro* and ultimately, *in-vivo*.

Intracellular Recording with low-power low-noise CMOS voltage and current clamp circuits

by

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A thesis submitted to the Graduate Faculty of
North Carolina State University
in partial satisfaction of the
requirements for the Degree of
Master of Science

Electrical Engineering

Raleigh, North Carolina

2007

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BIOGRAPHY

The author was born in Bombay, India on the 9^{th} of February, 1984. He earned a Bachelors degree in Electronics and Telecommunications Engineering from the University of Mumbai, India in June 2005. Thereafter, he has pursued graduate studies in Electrical Engineering at North Carolina State University. He has worked with Dr. Christal Gordon as a Research Assistant since August 2006. His interests include low-power analog circuit design, RF transceiver and data converter design.

ACKNOWLEDGEMENTS

Foremost, I would like to thank Dr. Christal Gordon for giving me an opportunity to work with her and for exposing me to novel applications of circuit design catered to biological applications. She has been an endless source of guidance and much good advice; within and beyond the research we undertake as part of her group.

My sincere appreciation is due to Dr. Kevin Gard, who kindly consented to chair my committee. I have learnt a great deal from the courses I have taken with him and I value the inputs he has given me along the way. I would also like to acknowledge Dr. Davis and Dr. Barlage for being a part of my committee. All the knowledge I have gleaned from the last two years of my studies is due in no small part to these and other professors here at NC State and I will remain indebted to them.

A special note of appreciation to the other students in Dr. Gordon's research group; Jingzhen, Gary, Ting and Peter for their help and enlightening discussions over the past year.

I am grateful to my friends here in Raleigh and those back home in Mumbai for providing moments of respite and good cheer from what is a generally taxing schedule for a grad student. Most especially Sarita, who has been a tremendous support during the last couple of years and never fails to bring a smile to my face.

My family is the primary reason behind what I have accomplished so far. I thank my brother and my grandparents for all they have meant to me. I owe everything to my parents; they have always provided me with opportunities, encouragement and much love. I dedicate this work to them.

Contents

List of Tables

List of Figures

Chapter 1

INTRODUCTION

Intracellular recording of the neural activity of living cells provides great insight into their physiology and processes therein. While microelectrodes have been utilized for such recording purposes since the early 20th century, it is in the last decade that rapid advances have been made in the fabrication of miniature microelectrode arrays that facilitate simultaneous measurements from multiple cell sites. The availability of these arrays has in turn driven a need to create integrated systems as an interface to make this data available to neuroscientists.

State-of-the-art recording setups are only present in the form of large boxes of equipment. Such systems are typically suited to observing single cells *in-vitro* in a laboratory setup. The ultimate goal, however, is the creation of a system that could be used to observe the stimulus and interaction of a group of cells operating in conjunction with each other *in-vivo*. Discrete equipment detracts from the benefit of having extremely small microelectrode arrays and would be entirely unsuitable if one desired to implant these devices into a living organism and observe its behavior. If an entire integrated recording setup, replete with micro-electronic instrumentation and micro-electrode arrays were created, it would also enable the real-time stimulation of cells based on the recordings of neural activity made available via such a system. The benefits of such a system over a conventional discrete recording system are illustrated in Fig. 1.1.

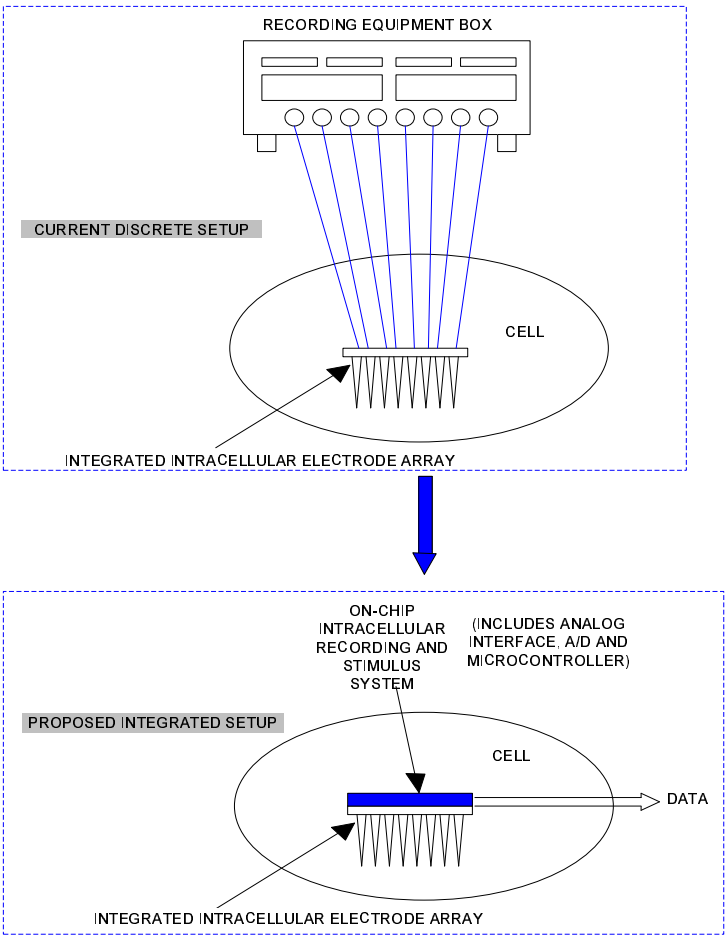


Figure 1.1: Discrete and integrated intracellular recording systems.

This work marks the first step in the formulation of such an integrated system by attempting to design integrated circuitry that would act as a suitable analog interface for the recording and stimulation of cells *in-vivo*. It does not however incorporate data conversion or microcontroller elements; these would be added in subsequent designs. In addition, by having the data conversion off-chip in this version, it affords flexibility to the neuroscientist conducting the experiment to digitize signals at varying rates depending on the type of signal that he is interested in observing.

This work investigates the design of an integrated intracellular recording system with both current-clamp and voltage-clamp configurations. Fundamental requirements of this system is that it should consume very low-power

and not introduce extraneous noise into the measurements. In addition, the presence of recording electrodes creates errors in the measurements and a solution to overcome these problems must therefore be incorporated into the system. In particular, this work incorporates novel automated systems that provide input capacitance neutralization and series resistance compensation.

An overview of the recording system is provided in Chapter 2 and its general requirements are discussed. This chapter also introduces electrophysiological signals and the problems associated with intracellular recording. Chapter 3 explores the design of a low-power low-noise neural amplifier that forms the core of many circuits in the system in addition to associated reference and bias circuits. Chapter 4 discusses the response of a membrane to a voltage clamp simulation. The circuits that solve intracellular recording problems such as capacitance neutralization and series resistance compensation are then designed. Details of how these tasks will be performed automatically through a computer interface are also included. Chapter 5 introduces the neuron model that is used to test the performance of the intracellular recording system and the simulation results of the designed system are consequently discussed. Chapter 6 concludes the thesis by discussing the limitations of this system and the potential for future work that would incorporate such a system.

Chapter 2

INTRACELLULAR RECORDING

2.1 Electrophysiology

Electrophysiology deals with the flow of ions in biological cells, the mechanisms that influence this activity, and instrumentation that is capable of measuring and controlling this ionic current and associated potentials across the membrane of the cell.

2.1.1 The Hodgkin-Huxley Neuron Model

All neurons are composed of a variety of ion channels which are electrochemical pores through which different types of ions are able to permeate. The specific permeability of a cell to a particular type of ion will vary depending on the function of the cell and its location in the organism. The ion channel itself will open or close in response to a variety of stimuli; ion channels may voltage-gated, ligand-gated, pH-gated or mechanically gated. The most common ions to which an ion channel is permeable to are sodium, potassium, calcium and chloride among others. For more details on ion channels, the reader is referred to [38]. Hodgkin and Huxley [1] devised a parallel conductance model shown in Fig. 2.1 to explain the magnitude of the ionic current and its causes.

The model consists of sodium, potassium and leakage conductances per unit area that account for the ion permeability of the membrane to these particular types of ions. Leakage ions primarily consist of chloride ions but do include other types of ions. In reality, neurons are more complex but this model sufficiently captures significant neuron behaviour and has proved to be an invaluable tool in electrophysiology. The parallel capacitance element represents the capacitance of the cell itself.

The total ionic current can then be given by

$$I_m = C_m \frac{dV_m}{dt} + (V_m - E_{Na})G_{Na} + (V_m - E_K)G_K + (V_m - E_L)G_L$$

where
I_m = membrane current per unit area
C_m = membrane capacitance per unit area
V_m = transmembrane potential
E_{Na}, E_K, E_L = Nernst potentials for sodium, potassium and leakage ions
G_{Na}, G_K, G_L = sodium, potassium and leakage conductance per unit area.

On the basis of their experiments, Hodgkin and Huxley determined that the membrane conductance for sodium and potassium were functions of transmembrane potential and time, while the leakage conductance was con-

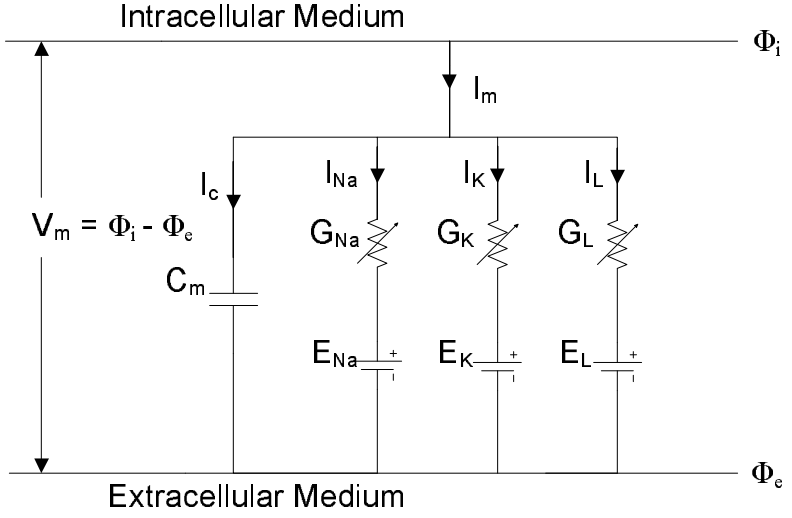


Figure 2.1: Equivalent circuit of the Hodgkin-Huxley model.

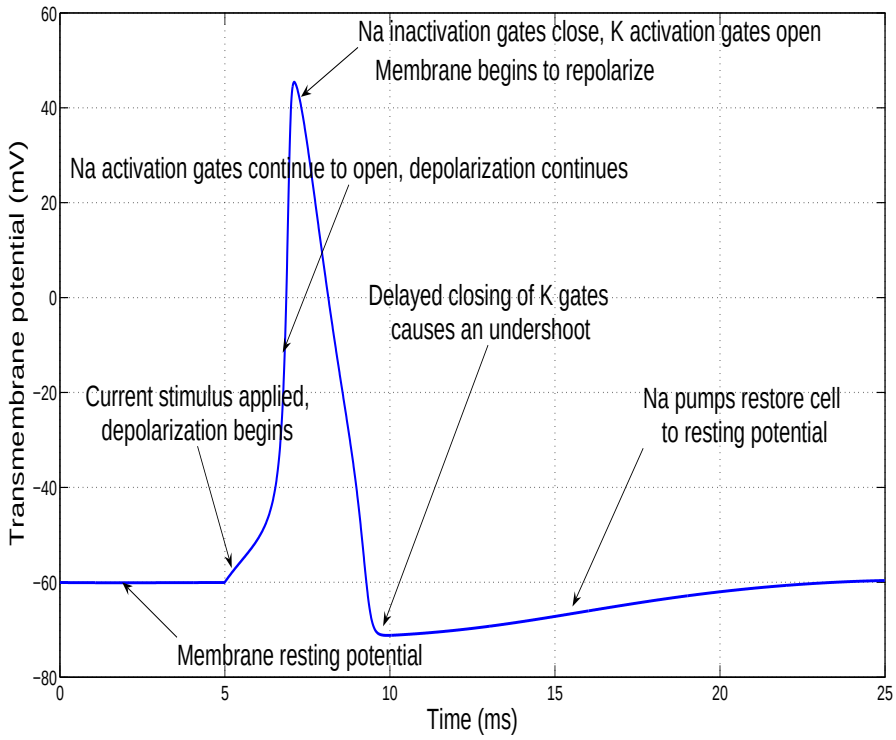


Figure 2.2: Phases of an action potential (generated from MATLAB using [1] and [41]).

stant. Thus, if the voltage across the membrane is fixed, the conductances would only vary with time. In addition, there would be no capacitive current since $dV_m/dt = 0$. This would lead to the voltage-clamp configuration, which will be discussed in detail later.

Hence, the transmembrane potential is a function of the distribution of various types of ions across the membrane and its permeability to each of those ions. When no stimulus is applied to the cell, the voltage across the membrane is the *resting potential* and is approximately -65 mV. This value is closer to the Nernst potential for potassium (E_K = -80 mV) than sodium (E_{Na} = +70 mV) since potassium leak channels in the cell are always open.

An action potential is an abrupt change in the polarity of a membrane experienced due to the application of an external signal as shown in Fig. 2.2 The maximal conductances for the various channels in mS/cm^2 used in the program are G_{Na}=120,G_K=36 and G_L=0.3 and the battery potentials of

each type of channel are E_{Na}=115, E_K=-12 and E_L=10.6. These particular values are obtained from [41]. When a stimulus is applied to the cell at t=5 ms, voltage-gated sodium channels begin to open causing an influx of sodium ions. The intracellular potential now becomes less negative and more sodium channels begin to open. More and more sodium ions begin to enter the membrane and there is a rapid depolarization in the transmembrane potential. The membrane potential peaks at around 50 mV, which is the point at which sodium inactivation channels close and restrict any further influx of sodium ions.

Simultaneously, voltage-gated potassium channels open and there is a large outflux of potassium ions from the membrane resulting in the intracellular potential becoming more negative in a repolarization phase. Rather than settling to the resting potential however, there is an undershoot in the response. Voltage-gated potassium channels have a delayed response, causing potassium ions to continue to flow out of the cell for a short duration and the potential to become more negative than the resting potential. Finally, sodium pumps restore the cell to its resting potential during the refractory period. An action potential cannot be induced during this period because almost all of the sodium channels are inactivated.

2.1.2 Neural Recording Mechanisms

In order to be able to record these current flows and transmembrane voltages, both intracellular and extracellular techniques exist. In extracellular recording, the electrode is attached to the exterior of the cell and the field potentials outside the cell are amplified and filtered to record cell activity. In contrast, an intracellular recording experiment involves the penetration of the cell using electrodes and then recording voltages and currents using a more elaborate closed loop method of control.

While extracellular recording is non-invasive and is essentially suited to *in-vivo* recordings, it is not an exclusive connection to an individual cell but is instead an averaged representation of the activity of several cells located in the vicinity of the probe. Perhaps more crucially, it does not provide any

information about the DC behaviour of a cell. It is hoped that many crucial questions related to cell behaviour could be answered if neuroscientists were able to accurately measure the activity of single cells *in-vivo*.

Intracellular recording offers the following advantages over extracellular recording:

- Increased dynamic range since intracellular potentials are of the order of 100 mV which is approximately 40 dB more than the range of extracellular potentials (50-500 μV).
- Information about the membrane resting potential since it is possible to record DC information.
- Shape and timing of action potentials which yields crucial information about ionic channels within the cell.
- Stimulation of the cell by a constant current or controlling the transmembrane potential.

2.1.3 Intracellular probe arrays

Micro-Electro-Mechanical-Systems (MEMS) devices have been explored extensively for neural recording systems due to their small feature size, capability to fabricate multi-site recording elements and a simple interface with integrated electronics at the probe site itself. MEMS probes have been traditionally geared towards extracellular recording systems which are easier to implant and are more suited to long-term recording. Cells are cultured in a nutrition electrolyte to which these extracellular probes interface [6, 5]. Recent implementations have included on-chip electronic systems to amplify, filter and digitize these extracellular signals [7].

Intraceullar probes are more difficult to successfully fabricate because they need to be sufficiently long (> 300 μm) and sharp (< 1 μm) to effectively bend and penetrate the cell [2]. The probe must be able to penetrate the cell without causing it trauma that would lead to long-term damage since these measurements are ultimately intended to be performed in living animals. Micro-machined silicon needles suited for intracellular recording were

first fabricated at the University of Washington [3]. The same group has recently reported the integration of the micro-machined silicon needles to an aluminium base where electrical contacts can be made, using flexible interconnects [4]. This configuration permits arrays of such silicon needles to be fabricated meaning that the absence of integrated intracellular electronics is the only bottleneck that remains in the creation of an integrated intracellular recording system.

These fabricated intracellular MEMS probes were used to detect action potentials in the neurons of the sea slug *Tritonia diomedea*. Results show that the magnitude of the action potentials is attenuated by a factor of about 10, which is attributed to imperfect insulation. This has an impact on the recording electronics; low-noise performance is critical to ensure that the attenuation by the electrode does not adversely affect the quality of the measurement.

2.1.4 Voltage Clamp

The Hodgkin-Huxley neuron model dictates that various membrane conductances are functions of both *voltage* and *time*. The voltage clamp uses a feedback amplifier to hold the membrane potential at a fixed value while the ionic flow can be observed as membrane current variations. This technique allows the experimenter to observe ionic current variations in isolation from capacitive current variations in the membrane since no capacitive current will flow due to the fixed transmembrane potential.

A schematic of the two-electrode voltage clamp (TEVC) is shown in Fig. 4.1(a). The measured pipette potential V_p is first buffered and then fed to a high-gain differential amplifier. The reference input to the differential amplifier is a control voltage V_r that is decided by the experimenter in order to activate certain voltage-gated ion channels within the membrane. The output is then used to drive a signal through the current-passing electrode in order to force $V_p = V_r$. The membrane itself is modelled as a parallel R-C circuit.

When the command voltage is stepped, the membrane capacitance is

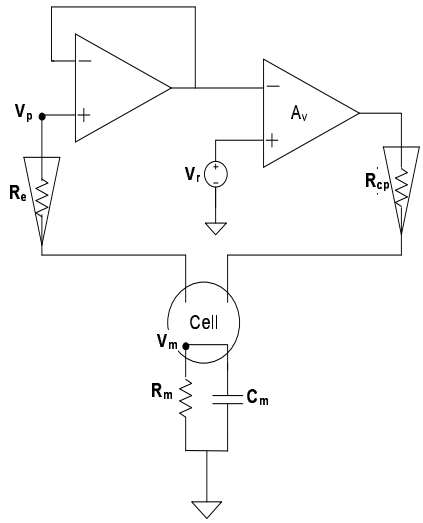


Figure 2.3: Two-electrode voltage clamp.

initially charged up and the steady-state transmembrane potential is

$$V_p = \frac{A_{cp}A_v}{A_{cp}A_v + 1}V_r. \tag{2.1}$$

where A_v is the gain of the differential amplifier and A_{cp} is the voltage division created by the current-passing electrode resistance R_{cp} and the membrane resistance R_m given by

$$A_{cp} = \frac{R_m}{R_{cp} + R_m}.$$

From (2.1), it is seen that the larger the open-loop gain of the differential amplifier, the closer the membrane potential V_m will approach the command potential V_r. For example, an open-loop gain of 60 dB will force these two voltages to be within 0.1% of each other assuming the attentuation A_{cp} is unity i.e. the membrane resistance is much higher than that of the current-passing electrode. It is therefore necessary to utilize a low-resistance electrode for current-passing. However, there is a solution even if this is not possible; a sufficiently high open-loop gain will negate most adverse effects of this attenuation factor. The speed and stability of the voltage clamp response will be analyzed in detail in chapter 4.

The voltage-clamp and current-clamp techniques find applications in most

realms of neuroscience and are a critical analytical tool in the stimulation and observation of neural activity. Single-electrode clamps have been applied to study neurons within deep layers of the brain [32] to compare periodic responses as well as synaptic currents and membrane potentials in order to determine dendritic and somatic conductance changes with external stimuli. These experiments also control voltage-gated conductances in order to stimulate only one type of ionic current or use pharmacological agents to block certain types of ionic currents.

The voltage-clamp has been used to study the role of different types of ionic currents governing the cardiac action potential [33]. Observing the action potential in a voltage-clamp yielded information about the role played by different Ca^{2+} channel types in muscle development [34]. Currents in transfected cells were measured using the whole-cell voltage clamp technique in clinical testing and yielded important information about sudden death associated with inherited short-QT syndrome [35].

2.1.5 Current Clamp

The current-clamp technique in intracellular recording incorporates a negative feedback system that injects a constant current pulse into the cell and is used to observe the variations in the membrane potentials as a consequence. If the injected current is $I = 0$ the cell's resting potential can be effectively observed without allowing an external stimulus to activate it. An injected pulse of current can then be used to depolarize or hyperpolarize the cell and thereby observe synaptic potentials within the cell. Such synaptic potentials in the activated membrane may fall into one of two categories - EPSP (excitatory post synaptic potential), or IPSP (inhibitory post synaptic potential). The distinction between these two types is based on the ion that the post-synaptic membrane is more permeable to. Sodium ions cause a depolarization of the cell and if this is the variety that the membrane is more permeable to, then the potential is classified as an EPSP. This is because an influx of Na^{+} ions will move the cell towards the firing threshold. On the other hand, if the membrane is now more permeable to hyperpolarizing ions

such as potassium, the cell moves away from the threshold (inhibits firing action) and the potential is classified as an IPSP.

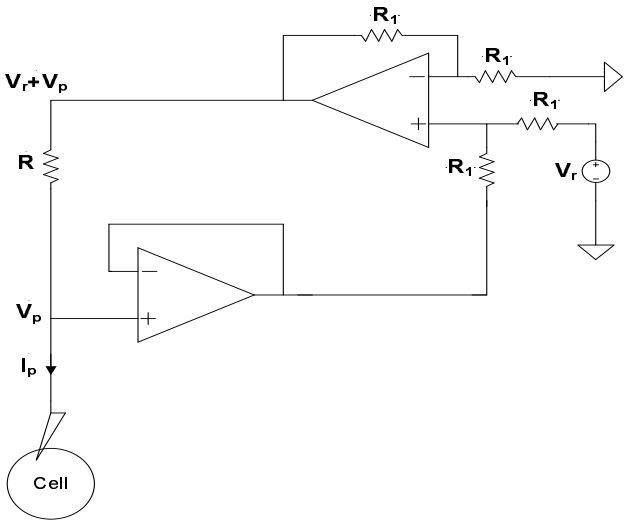


Figure 2.4: Current Clamp.

A schematic of the current-clamp recording setup is shown in Fig. 2.4. A voltage follower is used to buffer the pipette potential V_p which is then summed along with a command potential V_r. This ensures that the voltage drop across the resistor R is equal to V_r, thereby causing a constant current to flow into the membrane which is given by

$$I_R = \frac{V_r}{R}.$$

The current-setting resistor is of a high value ($> 10\ M\Omega$) so that only small currents flow into the cell and do not damage it irreparably. The control of the current flowing through the membrane permits the current-clamp to control ionic concentrations in the cell and is thus a very useful way to control and record cell activity.

The dynamic clamp protocol [31] is a more recent development and seeks to use the current-clamp setup to inject artificial synaptic currents as opposed to the conventional step waveforms. This configuration may be used to undertake a detailed study of cardiac, endocrine and neural function by introducing artificial conductances into these types of cells [36].

The applications listed in this chapter are by no means an exhaustive list but are meant to provide an insight into the varied uses of intracellular recording techniques. They have a role to play in disease analysis, central nervous system and deep brain studies of neuronal activity, cardiac activity and drug delivery amond numerous other applications.

2.2 System Level Block Diagram

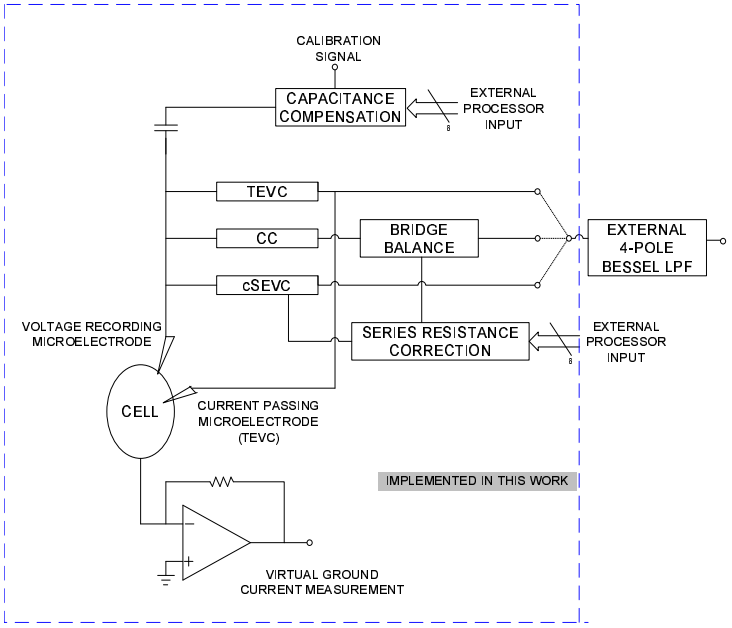


Figure 2.5: System level block diagram of an integrated intracellular recording system.

The block diagram in Fig. 2.5 illustrates the components of the integrated electrophysiological recording system. Three configurations are provided for experimentation - two-electrode voltage clamp (TEVC), current-clamp (CC), and the continuous single-electrode voltage clamp (cSEVC) which will be discussed in Chapter 5.

The presence of the microelectrodes themselves create inaccuracies in the recordings. These are diminished through the use of the series resistance correction and capacitance neutralization controls. The calibration input is

used to create a signal that is then curve-fitted to estimate electrode and cell parameters in an external processor. These values are then fed back to the series resistance and capacitance neutralization blocks to remove these errors from the recorded signals.The bridge balance is a form of series resistance correction used in the current-clamp mode. A virtual ground current measurement circuit in the form of an I/V converter is used to determine the current flowing through the membrane and is connected to the bath electrode.

2.3 Power and Area Requirements

Since the circuits designed herein will be operating in close proximity to living tissue, the heat generated by the integrated electronics must be sufficiently low so as not to cause damage to the cells. A system dissipating less than 5 mW of power will not raise the temperature of the surrounding tissue by more than 1℃[8]. For a recording system that has 16 electrodes, each recording channel should consume approximately 300 μW of quiescent power. The prototype discussed in this work is designed to fit on a MOSIS chip in an AMI 0.5 μm process having 0.9 mm$\times$0.9 mm active area. The area available would prove to be a limiting factor in low-noise design since flicker noise cannot be minimized beyond a limit for a given area, as will be shown in the following chapter.

Chapter 3

LOW-POWER LOW-NOISE NEURAL SIGNAL AMPLIFIER

A low-power low-noise amplifier is essential to all the circuits in the proposed intracellular recording system. In order to gain an insight into designing such an amplifier, it is necessary to understand how MOSFETs perform in terms of noise depending on their size and the region they are biased in. Each stage of a two-stage Miller compensated amplifier in first discussed in isolation and thereafter a design procedure is developed for sizing transistors in the neural amplifier.

3.1 Noise models

Throughout the design, BSIM3v3 noise models are used to simulate noise performance using the SPECTRE simulator [39]. The thermal and flicker noise models are briefly discussed as they will prove useful in estimating the noise performance of the amplifier through hand calculations prior to simulation.

The equation for thermal drain current noise that is used by the model

and is appropriate for all bias points is

$$\overline{i_d^2} = \frac{4k_BT\mu_{eff}Q_{inv}}{L^2}\Delta f. \tag{3.1}$$

where k_B = Boltzmann's constant, T = temperature, μ_{eff} = effective channel mobility, Q_{inv} = channel charge and L = effective channel length

Q_{inv} can be expressed as [11]

$$Q_{inv} = WLC_{ox}(V_{GS} - V_t)\frac{1 - n + \frac{n^2}{3}}{1 - \frac{n}{2}}. \tag{3.2}$$

The thermal noise coefficient is defined as

$$\gamma = \frac{1 - n + \frac{n^2}{3}}{1 - \frac{n}{2}}. \tag{3.3}$$

The values for γ in different regions of inversion have been presented in [10]. In weak inversion $\gamma = 1/2$ and in strong inversion, $\gamma = 2/3$.

The drain-source conductance is given by

$$g_{ds} = \frac{\mu_{eff}Q_{inv}}{L^2}. \tag{3.4}$$

Substituting the drain-source conductance from (3.4) in the expression for drain current noise in (3.1),

$$\overline{i_d^2} = 4k_BT\gamma g_{d0}\Delta f. \tag{3.5}$$

Substituting the values of γ and neglecting body effect so that $g_{d0} = g_m$, we get

$$\overline{i_d^2} = 2k_BTg_m\Delta f \qquad \text{in weak inversion} \tag{3.6}$$

$$= \frac{8}{3}k_BTg_m\Delta f \qquad \text{in strong inversion} \tag{3.7}$$

This thermal noise current can now be reflected back to the gate in order

to give the input-referred noise voltage ($\overline{v_g^2} = \overline{i_d^2}/g_m^2$) as

$$\overline{v_{g_T}^2} = \frac{2k_BT}{g_m}\Delta f \qquad \text{in weak inversion} \tag{3.8}$$

$$= \frac{8k_BT}{3g_m}\Delta f \qquad \text{in strong inversion} \tag{3.9}$$

This equivalent noise voltage source will be used to determine equivalent amplifier input-referred noise. In order to minimize the noise voltage at the gate for a given drain current, the subthreshold region of operation is preferred to the strong inversion region.

Noise models for $1/f$ noise in different regions of operation have been provided in [13] and measured results have been correlated to noise models used by the SPICE/SPECTRE simulators. The drain noise current is given by

$$\overline{i_d^2} = \frac{KF_{WI}{I_d}^2}{C_{ox}WLf}\Delta f \qquad \text{in weak inversion} \tag{3.10}$$

$$= \frac{KF_{SI}I_d}{C_{ox}L^2f}\Delta f \qquad \text{in strong inversion} \tag{3.11}$$

KF is a process dependent parameter that must be determined empirically [13]. It must be noted that KF has different values in the weak inversion and strong inversion regions as well as units of A-F and F respectively. Once again, we must reflect this noisy drain current back to the gate to obtain the input-referred noise voltage, similar to the operation carried out for thermal noise. The gate transconductance in each region of operation is given by

$$g_m = \frac{\kappa I_d}{V_T} \qquad \text{in weak inversion} \tag{3.12}$$

$$= \sqrt{2I_d\mu C_{ox}\frac{W}{L}} \qquad \text{in strong inversion} \tag{3.13}$$

V_T is the thermal voltage kT/q and κ is the subthreshold gate coupling coefficient and has a typical value of 0.7. The expression for g_m in the subthreshold region is obtained from the EKV model [12] and will be explained

while considering amplifier design. Using the values of g_m from (3.12) and (3.13) in order to reflect the flicker noise current back to the gate, we get

$$\overline{v_{g_{1/f}}^2} = \frac{KF_{WI}{V_T}^2}{\kappa^2 WLC_{ox}f}\Delta f \qquad \text{in weak inversion} \tag{3.14}$$

$$= \frac{KF_{SI}}{2\mu C_{ox}^2 WLf}\Delta f \qquad \text{in strong inversion} \tag{3.15}$$

3.2 Differential Input Stage

The differential input stage of the neural amplifier is significant because it determines the noise performance of the overall amplifier. The signal at the output of this first stage is amplified sufficiently so that noise from the second stage will be divided down by the high gain of this first stage and hence will not impact overall noise performance. Hence it is critical to minimize the input-referred noise contribution of the first stage while using small bias currents to reduce power consumption of this stage.

A current mirror OTA has been implemented as the input differential transconductance stage. The noise performance of this architecture will now be examined in detail so as to provide design guidelines while sizing the transistors in an attempt to minimize the input-referred noise.

3.2.1 Current-Mirror OTA

In the current-mirror OTA shown in Fig. 3.1, the input differential pair M_1-M_2 is assumed to be ideally matched and the current mirror transistors M_3-M_6 are of the same size, as are M_7-M_8. The total output noise current is first calculated and this is then reflected back to the input to obtain the input-referred noise voltage as

$$\overline{i_o^2} = 2\overline{v_{g_1}^2} + 4g_{m_3}^2\overline{v_{g_3}^2} + 2g_{m_7}^2\overline{v_{g_7}^2} + \frac{g_{m_{ncas}}^2}{(1+g_{m_{ncas}}r_{d_6})^2}\overline{v_{g_{ncas}}^2} + \frac{g_{m_{pcas}}^2}{(1+g_{m_{pcas}}r_{d_8})^2}\overline{v_{g_{pcas}}^2}. \tag{3.16}$$

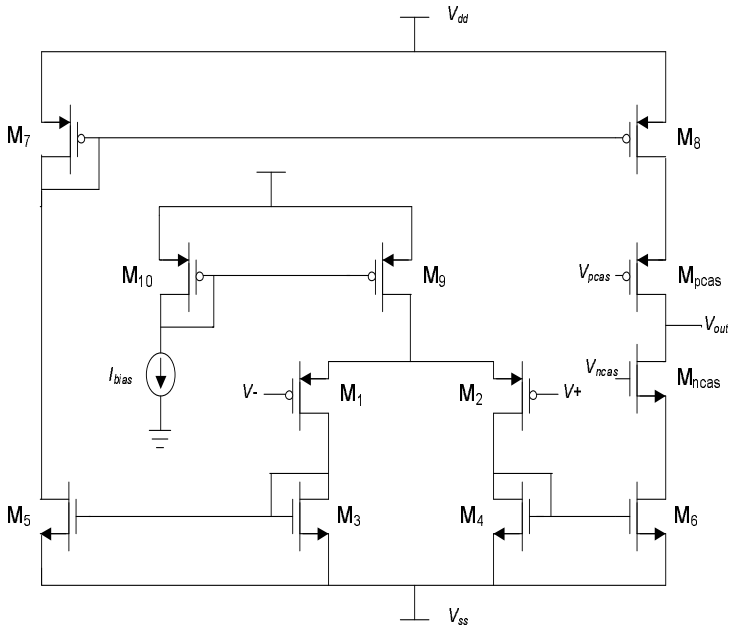


Figure 3.1: Current-Mirror OTA.

The last two cascode terms can be neglected because of the large $g_m r_d$ products in the denominators, leading to the input-referred noise voltage as

$$\overline{v_{ni}^2} = 2g_{m_1}^2 \overline{v_{g_1}^2} + 4\frac{g_{m_3}^2}{g_{m_1}^2}\overline{v_{g_3}^2} + 2\frac{g_{m_7}^2}{g_{m_1}^2}\overline{v_{g_7}^2}. \tag{3.17}$$

The major noise contribution is from the differential pair. The noise contributions from the current mirrors M_3-M_6 and M_7-M_8 can be minimized by reducing the transconductances of the PMOS and NMOS current mirrors and increasing the transconductance of the input pair. However, this cannot be done arbitrarily as there will be parasitic poles created at the current mirror nodes and this will reduce the phase margin of the amplifier.

3.2.2 Input-referred thermal and flicker noise of the Current Mirror OTA

In order to obtain the input-referred thermal noise voltage of the current-mirror OTA, (3.8) and (3.9) are substituted in (3.17). It is also assumed that

only the input differential pair will be operated in weak inversion while the other transistors in the OTA will be biased in the strong inversion region.

$$\overline{v_{ni_T}^2} = \frac{8k_BT}{g_{m_1}} + \frac{16k_BT}{3g_{m_1}}(\frac{4g_{m_3}}{g_{m_1}} + \frac{2g_{m_7}}{g_{m_1}}). \tag{3.18}$$

Similarly, the input-referred flicker noise is given by substituting (3.14) and (3.15) in (3.17) as

$$\overline{v_{ni_{1/f}}^2} = 2\frac{KF_{WI}{V_T}^2}{\kappa^2 W_1 L_1 C_{ox} f} + 4\frac{KF_{SI}I_{d_3}}{C_{ox}{L_3}^2 f}\frac{1}{{g_{m_1}}^2} + 2\frac{KF_{SI}I_{d_7}}{C_{ox}{L_7}^2 f}\frac{1}{{g_{m_1}}^2}. \tag{3.19}$$

Thus in order to minimize the input-referred flicker noise:

- The input pair must have as large W and L as possible so as to minimize its contribution to flicker noise.
- The current mirrors M_3-M_6 and M_7-M_8 must have large L.
- The input pair transconductance must be made as large as possible, which amounts to operating it in weak inversion by increasing the W and L.

3.3 Low power Class AB output stage

Low power design is one of the primary considerations in designing any biomedical system and in keeping with this design strategy, class AB design serves to reduce power consumption of the output stage of an amplifier compared to a Class A design. The class AB topology implemented herein is that proposed in [14] and shown in Fig. 3.2 which utilizes a series of current mirrors to achieve an increased transconductance in the output stage.

The input signal to this class AB stage is split by the output transistor M_{p4} on the one hand and M_{p1} and the current mirrors $M_{p2} - M_{p3}$ and $M_{n1} - M_{n2}$ on the other. A useful metric to quantify the improvement in power consumption is the g_m/I_d ratio which for this output stage as compared to

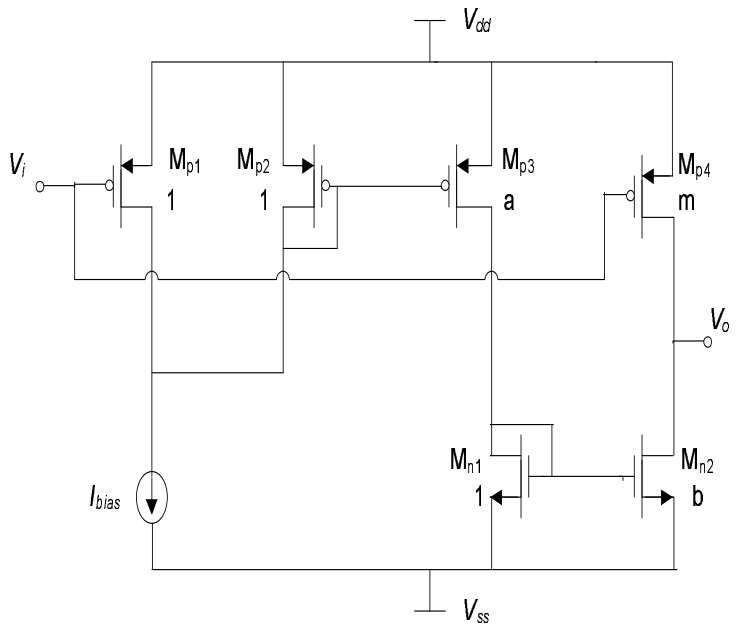


Figure 3.2: Class AB Output Stage.

that of a conventional class A output stage can be expressed as

$$k = \frac{(g_m/I_d)_{AB}}{(g_m/I_d)_A} = \frac{1 + \frac{ab}{m}}{1 + \frac{1}{a} + \frac{1}{ab} + \frac{1}{m}} H(s). \tag{3.20}$$

H(s) is the frequency response of this stage and is given by

$$H(s) = \frac{1 + \left(\frac{1}{\omega_p} + \frac{1}{\omega_n}\right)\frac{s}{k} + \frac{1}{\omega_p \omega_n}\frac{s^2}{k}}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{\omega_n}\right)}. \tag{3.21}$$

The pair of current mirrors introduces a pole-zero doublet each according to (3.21) with the frequencies ω_p and ω_n given by $g_{m_{p2}}/C_{g_{p2}}$ and $g_{m_{n1}}/C_{g_{n1}}$ respectively. This pole zero doublet introduces a phase shift in the frequency response and compromises the overall phase margin of the amplifier. This effect worsens with an increase in the multiplying factor k and hence puts an upper limit on the increase in the g_m/I_d ratio that can be achieved with this configuration.

3.4 Amplifier Design

The complete two-stage Miller compensated amplifier with a differential current mirror OTA input stage and class AB output stage is shown in Fig. 3.3. The design procedure involved will now be discussed. Flicker noise is an im-

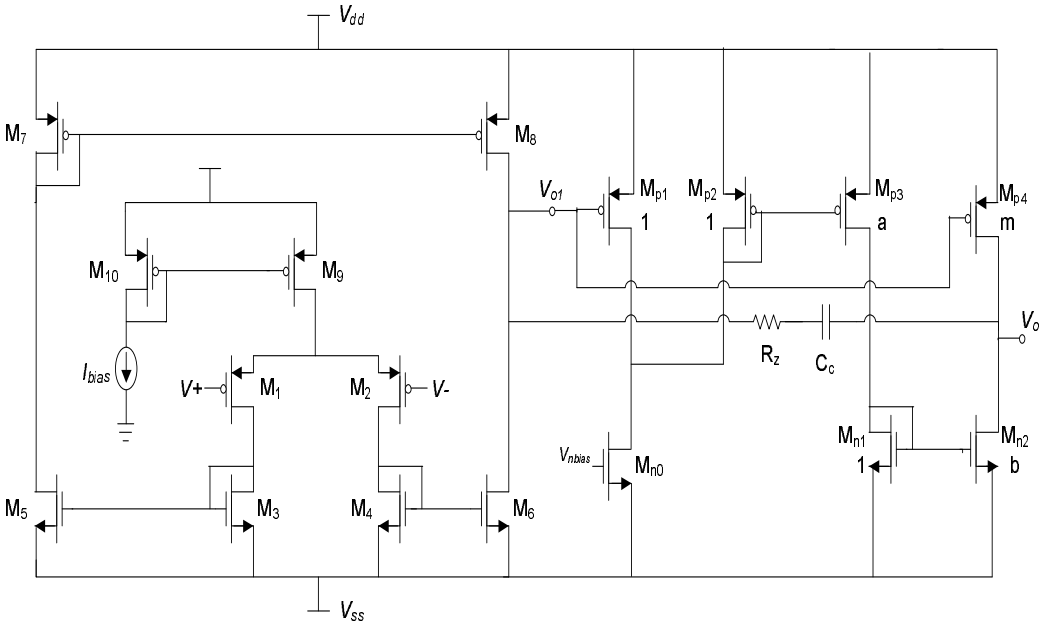


Figure 3.3: Miller compensated two-stage amplifier.

portant concern in low-frequency microsystems and can dominate the noise performance of the amplifier. To mitigate the effects of $1/f$ noise, the input transistors are selected as PMOS devices since they usually have flicker noise an order of magnitude lower than their NMOS counterparts when V_{GS} is not much greater than the threshold voltage [13]. All transistors in the input stage should be made as large as possible, but there is a penalty to the phase margin which will be illustrated soon. Using this data, the input transistors are sized according to the transconductance predicted by the EKV model as follows. Although the BSIM3v3 models were accurate enough to describe the noise behavior of the MOS transistors in each region of inversion, they are not as accurate in describing small-signal parameters in weak and moderate inversion as compared to the EKV model [12].

The first step is to fix the current consumption of the amplifier. (3.18) is then used to calculate the transconductance required in the input stage to limit thermal noise in the input stage. The moderate inversion characteristic current I_s is given by

$$I_s = \frac{2\mu C_{ox} V_T^2}{\kappa} \frac{W}{L}. \tag{3.22}$$

The Inversion Coefficient (IC) is then the ratio of the drain current to I_s [40]

$$IC = I_D / I_s. \tag{3.23}$$

IC can be used to determine the region of inversion that the transistor operates in; a device with $IC < 0.1$ operates in weak inversion, one with $0.1 < IC < 10$ is in moderate inversion while an $IC > 10$ indicates strong inversion operation. The transconductance estimate provided by the EKV model which is valid in all regions of operation is given by

$$g_m = \frac{\kappa I_D}{V_T} \frac{1}{\sqrt{1 + 4IC}}. \tag{3.24}$$

A plot of the variation of the g_m/I_d ratio in different regions of operation is shown in Fig. 3.4. It can be seen that the weak inversion region is suited for micropower operation since it provides optimum performance for a given value of drain current. A transistor will be forced to operate in weak inversion by increasing its W/L ratio and thereby increasing I_s for a given value of I_D.

Once the input transistor size is decided, the compensation capacitor can be fixed in order to decide the unity gain bandwidth of the amplifier which is

$$GBW = g_{m1}/C_c. \tag{3.25}$$

The remaining transistors in the OTA viz. $M_3 - M_6$ and $M_7 - M_8$ are designed to have large gate areas and minimized transconductance so as to reduce their contribution to the input-referred noise as given by (3.18) and (3.19). However there are also parasitic poles at these current mirror nodes given by g_{m3}/C_{g3} and g_{m7}/C_{g7} which means that the gate areas and

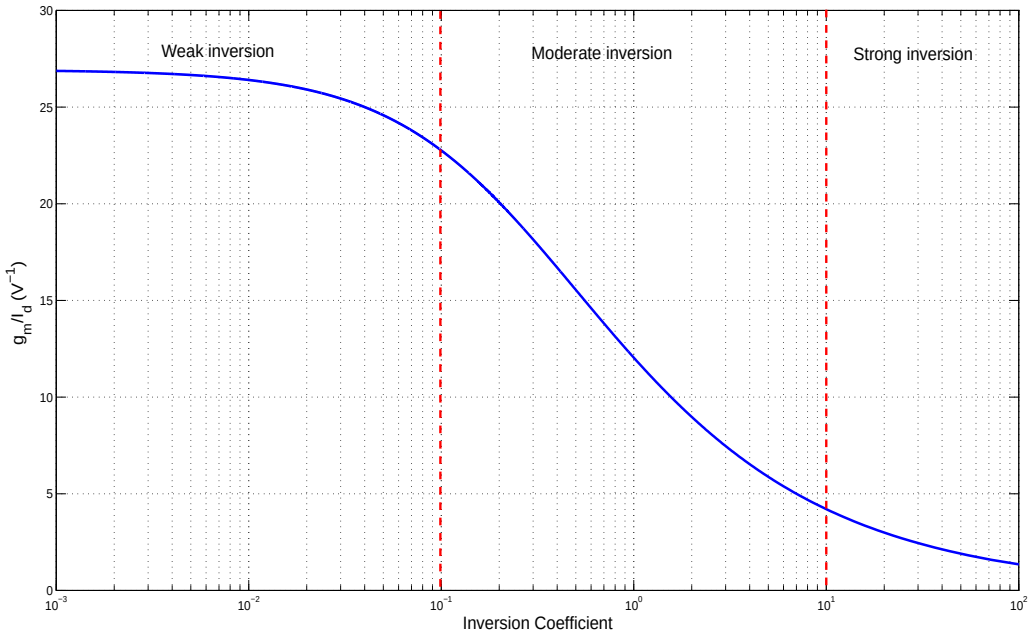


Figure 3.4: Variation of g_m/I_D against inversion coefficient.

the transconductance cannot be optimized arbitrarily. Their sizing involve a tradeoff with the phase margin of the amplifier.

The transistors in the second stage need not be sized too large according to noise considerations because any noise generated in the output stage is divided down by the high gain of the first stage when referring it to the input. As a result, stability considerations dominate the sizing issues with these transistors, specifically the transconductance multiplication ratio given in (3.20). The current mirrors in the output stage create two pole-zero doublets which cause a phase shift in the response as given in (3.21) and impact the phase margin of the amplifier. A non-dominant pole is created by the capacitance at the output node given by

$$\omega_o = g_{m_{AB}}/C_L. \tag{3.26}$$

All these non-dominant poles must be calculated carefully to ensure a particular phase margin for the amplifier. In addition the zero-nulling resistor R_z serves to cancel out the feedforward zero induced in the output stage by

the Miller capacitor and must be given by

$$R_z = 1/g_{m_{AB}}. \tag{3.27}$$

The bias current of the input tail source was set to 8 μA and the output current was set to 2 μA. The performance of the amplifier is summarized below.

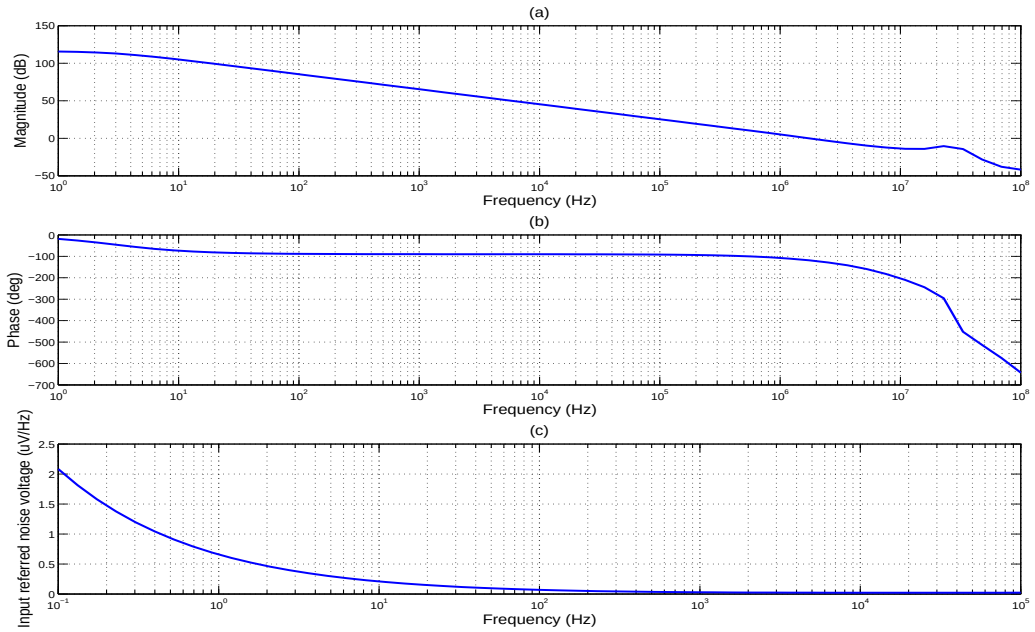


Figure 3.5: Performance of the two stage Miller compensated operational amplifier : (a)Gain response (b)Phase response and (c)Input-referred noise voltage.

The simulation results shown below in Fig. 3.5 illustrate the open-loop gain and phase of the designed neural amplifier along with the input referred noise voltage. An open loop DC gain of 115 dB is obtained with the designed amplifier and the unity gain bandwidth is seen to be 1.76 MHz with a phase margin of 61° guaranteeing sufficient stability margins. The flicker noise corner is seen to be approximately 200 Hz and the integrated value of the noise voltage over a 10 kHz bandwidth was 3.4 μV_{rms}. The total harmonic distortion (THD) with the class AB output stage was observed to be 0.2 % which shows that the use of this type of stage does not cause undue

Table 3.1: Performance summary for the designed neural amplifier.

Parameter	Simulated Value
Open loop DC gain	115 dB
Phase Margin	61°
Unity gain bandwidth	1.76 MHz
Input referred noise	3.4 μV_{rms}
CMRR (1 Hz-16 kHz)	$\geq$80 dB
PSRR (1 Hz-16 kHz)	$\geq$50 dB
Supply voltage	$\pm$1 V
Power	40 μW
Area	0.05 mm^2

distortion to the signal being amplified. This test was conducted in a closed loop configuration with a gain of 40 dB and an input signal of 60 Hz with magnitude 10 mV_{pp}. The other important results are listed in Table 3.4.

3.4.1 Comparison with other neural amplifier designs

In order to compare this design with similar low power neural amplifiers, a metric known as the Noise Efficiency Factor (NEF) first used in [15] is used to quantify its performance. NEF is used to illustrate the tradeoff between noise and power and is defined as

$$NEF = V_{ni_{rms}} \sqrt{\frac{I_{tot}}{\pi V_T 4 k_B T BW}}. \tag{3.28}$$

The amplifier was configured in a closed-loop resistive-feedback configuration in order to set the gain to 40 dB and the observed 3 dB bandwidth was 10 kHz which gives NEF=5.2. Fig. 3.6 compares the performance of this work to various other recently reported designs. A suitable tradeoff has been achieved between power consumption and the maintenance of a low enough input-referred noise level since both these factors are crucial in the implementation of the intracellular recording system.

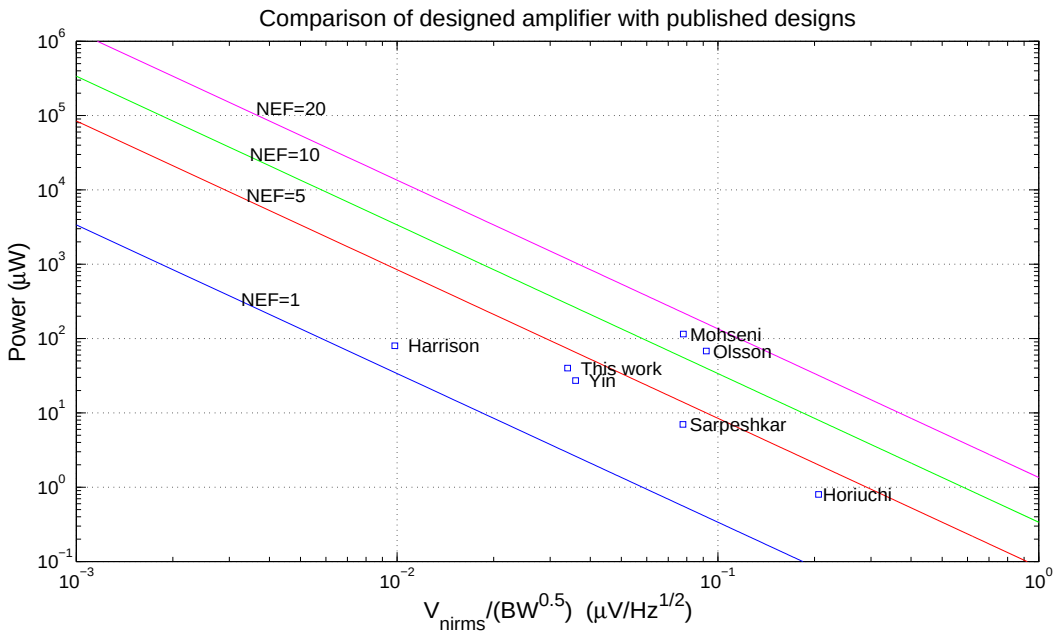


Figure 3.6: Comparison of designed amplifier with published designs in terms of power, noise and bandwidth.

3.5 Supply Independent Bias Circuit

With relation to integrated circuit design for biomedical applications, temperature insensitivity is not a major issue since the temperature can be assumed to be that of the cell or organism under test, which is relatively constant around room temperature. However, implantable biomedical devices are often inductively powered through remote coupling and the supply voltage can vary over a comparatively large range. In order to guarantee system performance under varying power supply conditions, it becomes necessary to design a supply independent bias circuit. The beta-multiplier with associated start-up circuitry depicted in Fig. 3.7 is used for this purpose.

Applying Kirchoff's voltage law to the loop containing the gate-source voltages of M_1 and M_2, we get

$$V_{GS1} = V_{GS2} + I_o R. \tag{3.29}$$

The gate-source voltage of the MOSFET can be expressed in terms of its

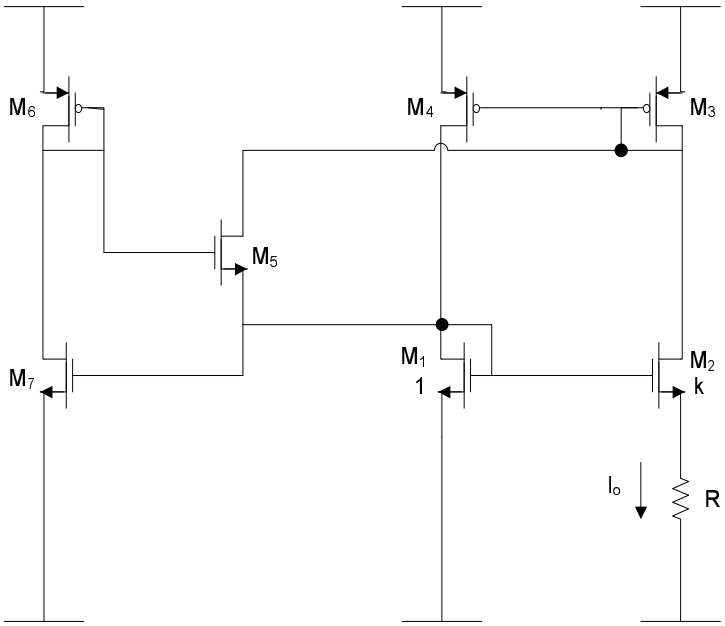


Figure 3.7: Beta-multiplier current reference circuit.

drain current and threshold voltage as

$$V_{GS} = \sqrt{\frac{2I_D}{\beta}} + V_t. \tag{3.30}$$

M_2 is sized k times as large as M_1 and hence $\beta_2 = k\beta_1$ and the current in the reference branch is then given by

$$I_o = \frac{2}{\mu_n C_{ox} \frac{W_1}{L_1} R^2} \left(1 - \frac{1}{\sqrt{k}}\right)^2. \tag{3.31}$$

This is the optimal case; however, there is another stable operating point when I_0=0. To avoid this zero-current case, start-up circuitry comprising transistors M_{5-7} is incorporated. Zero current flows when $M_{1,2}$ have their gates at V_{SS} while the gates of $M_{3,4}$ are at V_{DD}. When this condition occurs, the gate of M_6 is between V_{DD} and V_{DD}-V_{tp} and this causes M_7 to turn on in the linear region and leak current to the gates of $M_{1,2}$. The output current exits its zero-state and simultaneously M_7 also turns off. This ensures that the start-up circuit does not interfere with normal operation.

3.5.1 Current-Splitter cells

As will be discussed in Chapter 4, in addition to a master reference current, we will also require weighted current sources that can be digitally switched into filter circuits in order to vary their frequency response. It is not possible to generate separate current references for each bit; the space occupied by the resistor for the smaller currents would be too large. One solution would be to have a set of ratioed current mirrors; however, the accuracy of this method is not very good. Far more important is the space on chip occupied by this technique, 8-bit accuracy will require the largest transistor to be 128 times the smallest in the current sources. This is therefore not an acceptable solution.

Instead, we choose to implement current-splitter cells as proposed in [28] and shown in Fig. 3.9. At each splitter stage, the current is reduced by half while the remaining current passes through to the subsequent stages. Thus 8-bit accuracy can be easily achieved without having overtly large transistors.

The circuit functions in much the same manner as an R-2R converter with the transistors used to set the resistance ratios. The current in the i th branch is given by

$$I_i = \frac{R_z}{R_y} I. \tag{3.32}$$

The current in the $i+1$ th branch is given by

$$I_{i+1} = I - I_i = \left(1 - \frac{R_z}{R_y}\right). \tag{3.33}$$

The ratio between currents in consecutive branches is then given by

$$M = \frac{I_{i+1}}{I_i} = \frac{R_y}{R_z} - 1. \tag{3.34}$$

The final branch (containing R_z) is used to terminate the line of splitter cells so that it appears infinite. In order to do this, the last branch must draw the same current as the penultimate branch. This can be achieved by selecting

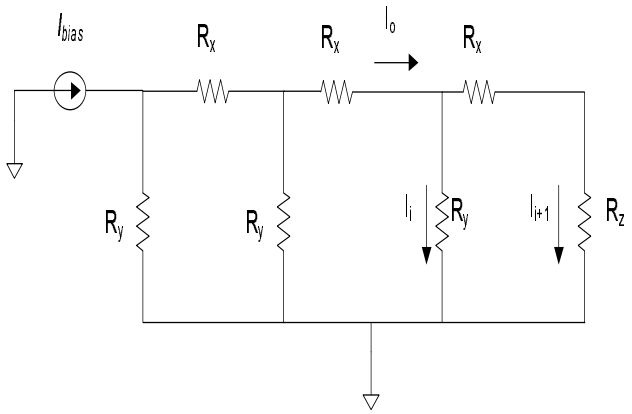


Figure 3.8: Equivalent circuit of the current splitter chain.

$$R_z = (R_x + R_z) \parallel R_y. \tag{3.35}$$

Finally (3.34) and (3.35) are solved to yield the value for R_x as

$$R_x = \frac{(1-M)^2}{M} R_y. \tag{3.36}$$

In order to generate binary-weighted currents in each branch the ratio of $R_x : R_y : R_z$ must be selected as 1:2:1. The transistors are therefore sized in this manner with a series connection of two unit transistors used to generate the resistor R_y. From the master bias generator described earlier, a chain of splitter cells are tapped as shown in Fig. 3.9. The currents in each branch are indicated in the figure.

Simulation results for the currents in each branch are indicated in Fig. 3.10 as the supply voltage is varied. The subsequent curve shows the ratio between currents in the various branches as a function of supply voltage. The reference current is shown to be relatively insensitive to power supply and the ratios between branch currents are also independent of power supply variations.

Fig. 3.11 shows the variation of the base 2 logarithm of the splitter cell currents with supply voltage variation. Since the curves are evenly spaced at 1 dB apart, this indicates the current in a branch is half of that observed in the previous branch. This will permit the addition of binary-weighted

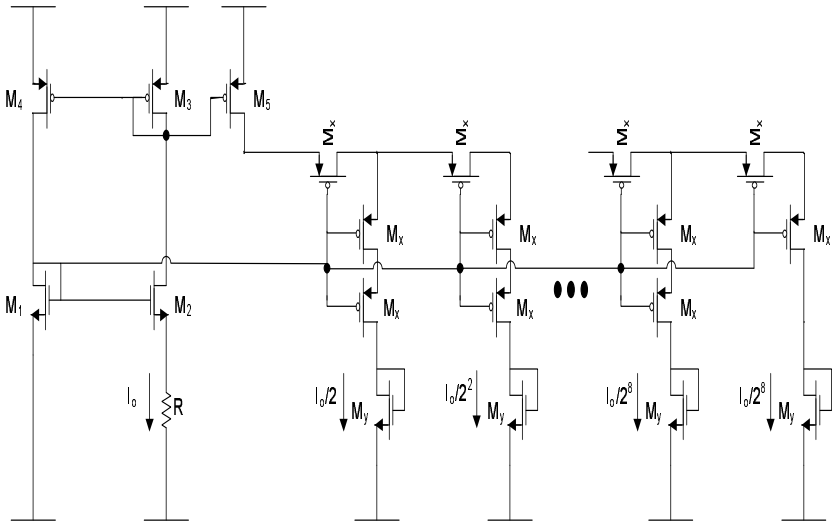


Figure 3.9: High dynamic range current splitter bias generator.

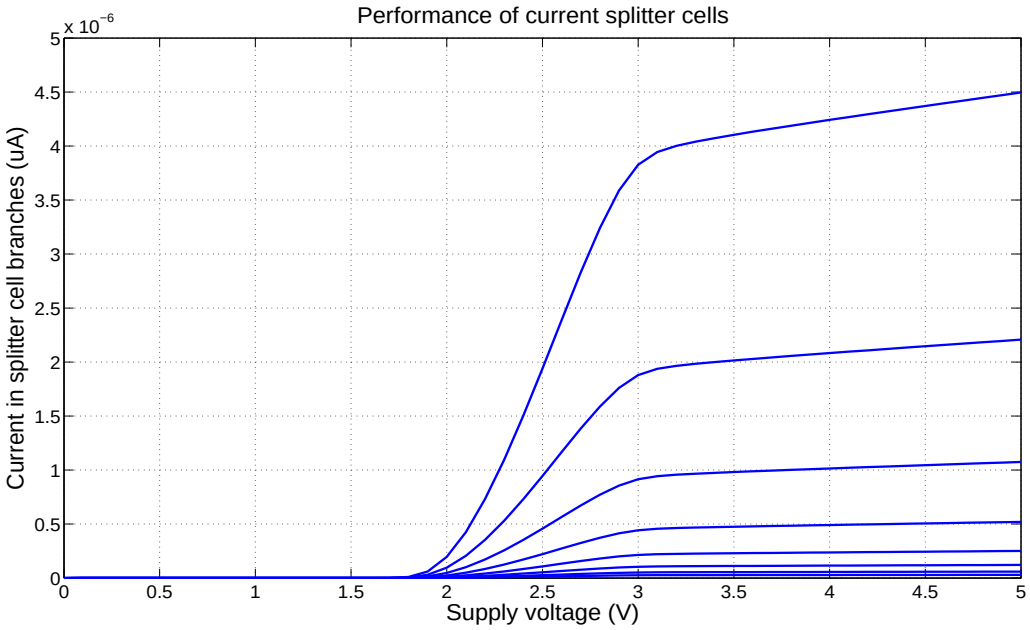


Figure 3.10: Branch currents in splitter cells with variation in supply voltage.

currents in susbsequent circuits to vary their bias conditions. The currents range in magnitude from 4 μA down to 25 nA.

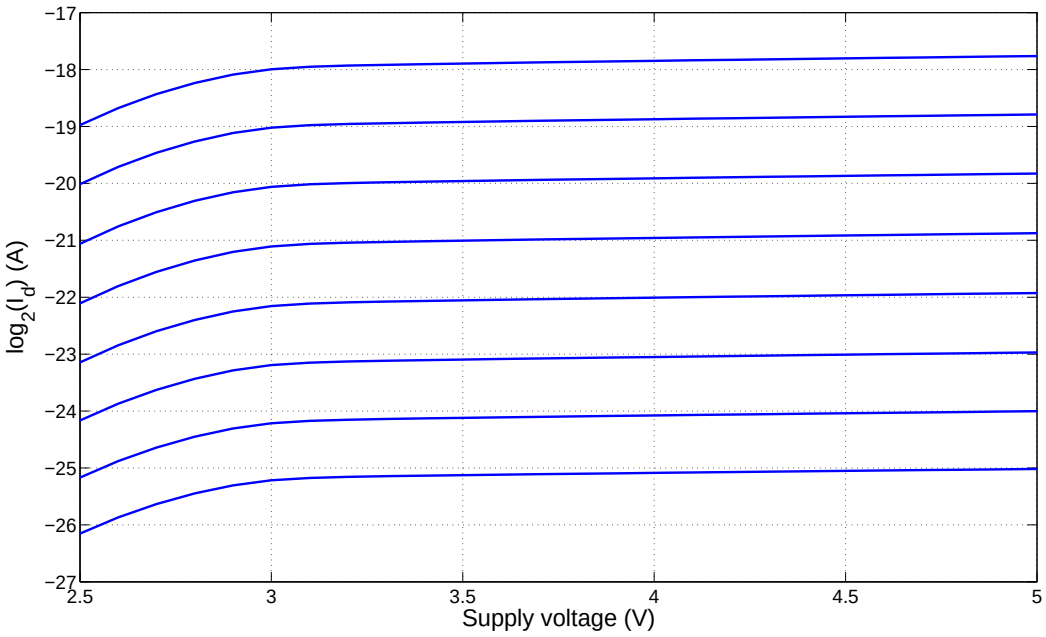
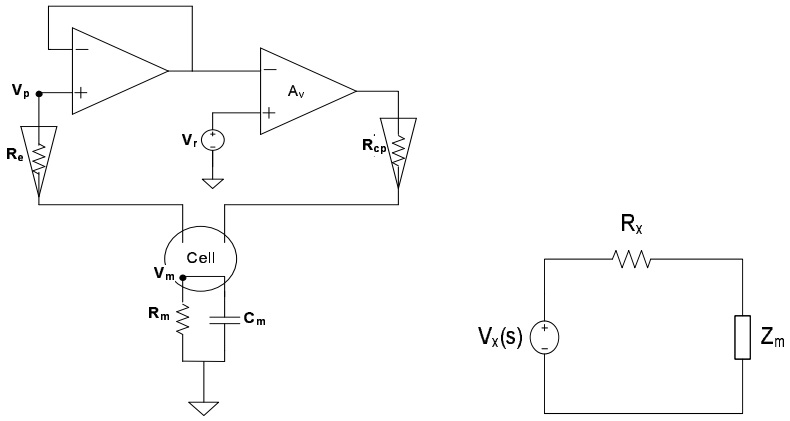


Figure 3.11: Logarithmic values of Branch currents in splitter cells with variation in supply voltage.

Chapter 4

DESIGN OF VOLTAGE AND CURRENT CLAMPS AND COMPENSATION CIRCUITS

An important facet of the performance of the voltage clamp circuit is to determine the response of the membrane parameters such as ionic current once a change in reference potential occurs. This chapter begins by discussing this response as well as how stable it is in a real voltage clamp. It is then shown how a simple gain amplifier in the feedback loop of the voltage clamp is inadequate to achieve the necessary performance and why a proportional-integral controller is necessary. This controller is then discussed in detail. A technique to compensate for stray capacitances at the input of the system is then introduced. This is followed by an introduction of the single electrode voltage clamp and its associated problems in contrast to the two electrode version. A technique of series resistance cancellation that is inherently stable is discussed. Finally, a method to determine the actual values of resistances and capacitances that need to be compensated is explored.



(a) Two Electrode Voltage Clamp. (b) Thevenin Equivalent.

Figure 4.1: Two Electrode Voltage Clamp and a simplified Thevenin equivalent circuit.

4.1 Speed and stability of Two Electrode Voltage Clamp

If one were to analyze the voltage clamp circuit shown in Fig. 4.1(a) as a closed-loop system, we identify the feedback path as the voltage recording microelectrode with resistance R_e and the buffer amplifier A_1. The forward path is the high-gain differential amplifier A_2, followed by the current-passing microelectrode with resistance R_{cp} and the membrane equivalent R-C circuit. A detailed analysis of the performance of the voltage clamp is performed in [16]; the important results are included here. Evaluating the response of this closed system, the transfer function can be shown to be

$$\frac{V_m(s)}{V_r(s)} = \frac{\eta}{1 + s\tau_0}. \tag{4.1}$$

where η is the steady state clamp error and τ_0 is the time constant governing the speed of the clamp response and these are given by

$$\eta = \frac{A_v A_{cp}}{A_v A_{cp} + 1} \tag{4.2}$$

$$\tau_0 = \frac{R_m R_{cp} C_m}{(A_v + 1)R_m + R_{cp}} \tag{4.3}$$

In order to obtain the time domain response, the inverse Laplace transform is applied to (4.1) with the input being a voltage step $V_r(s) = V_r/s$ to give

$$V_m(t) = \eta V_r[1 - e^{-t/\tau_0}]. \qquad t > 0. \tag{4.4}$$

The membrane potential V_m rises as a decaying exponential towards the reference potential V_r with a rise time (10-90%) given by

$$t_r = \frac{2.2 R_{cp} C_m}{A_v}. \tag{4.5}$$

The next step in the analysis is to study the membrane current responses to changes in reference potential. The analysis is simplified if one were to consider the Thevenin equivalent circuit of the voltage clamp circuit shown in Fig. 4.1(b) where the voltage source and series resistance are evaluated as

$$V_x(s) = \frac{A_v}{A_v + 1} V_c(s). \tag{4.6}$$

$$R_x = \frac{R_{cp}}{A_v + 1}. \tag{4.7}$$

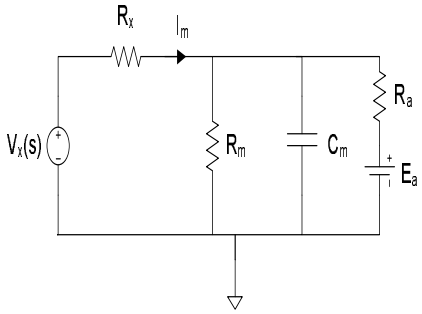


Figure 4.2: Thevenin equivalent circuit of the voltage clamp with passive membrane model.

The membrane load Z_m in this equivalent circuit can now be replaced by its component resistance R_m, capacitance C_m and the activable membrane resistance R_a which is infinite at rest but carries the ionic current supplied by the activable membrane voltage E_a when the cell is activated. This equiv-

alent can now be used to derive the transfer function of interest to the experimenter $I_m(s)/V_c(s)$. The currents through each branch are summed to give an expression for $I_m(s)$ as

$$I_m(s) = \frac{sC_mV_x(s) + G_mV_x(s) + G_a(s)[V_x(s) - E_a(s)]}{sC_mR_x + G_mR_x + G_a(s)R_x + 1}. \tag{4.8}$$

For the membrane at rest, the activable resistance R_a is infinite and the transfer function is evaluated as

$$\frac{I_m(s)}{V_c(s)} = \frac{\eta(1 + s\tau_m)}{R_m(1 + s\tau_0)}. \tag{4.9}$$

Most voltage clamp experiments consist of applying a voltage step in the reference potential and observing the corresponding change in membrane current and it is therefore useful to examine the step response of this transfer function.

$$I_m(t) = \frac{\eta V_r}{R_m}[1 - (1 - \tau_m/\tau_0)e^{-t/\tau_0}]. \qquad t > 0. \tag{4.10}$$

When the reference potential is stepped up, $I_m(t)$ has an initial peak at $t = 0$ and then decays exponentially to its steady-state value with time constant τ_0. The inital peak is given by $\eta V_r\tau_m/R_m\tau_0$ and is much greater than the steady state value if $A_vA_{cp} \gg 1$.

The final step in the analysis is to determine the changes in membrane current due to changes in activable membrane conductance G_a. The solution can be obtained by assuming that $G_a(t)$ steps from 0 to G_a at t=0 and that the initial condition for $V_m(t)$ is that its value is $V_{m_{0-}}$.

$$I_m(s) = \frac{sC_m(V_x - V_{m_{0-}}) + G_mV_x + G_a(V_x - E_a)}{s(1 + G'_mR_x + sC_mR_x)} \tag{4.11}$$

where

$$\begin{aligned} G'_m &= G_m + G_a \\ V_{m_{0-}} &= \frac{R_m}{R_m + R_x}V_x. \end{aligned}$$

The time domain response is once again determined by the inverse Laplace transform as

$$I_m(t) = \frac{I_a \tau_0'}{\tau_x}(1 - e^{-t/\tau_0'}) + I_b e^{-t/\tau_0'}. \qquad t > 0. \tag{4.12}$$

where

$$\begin{aligned} I_a &= [G_m V_x + G_a(V_x - E_a)] \\ I_b &= (V_x - V_{m_{0-}})/R_x \\ \tau_x &= R_x C_m \\ \tau_0' &= (R_x \parallel R_m')C_m \end{aligned}$$

Thus the time constant governing the response of the membrane current to a change in activable membrane conductance is identical to the membrane voltage settling time constant with the exception that R_m is now in parallel with R_a.

4.2 PI Controller

The previous section assumes a proportional control scheme. In order to reduce the steady state clamp error to zero, it is necessary to have a large voltage gain. However, the phase shifts caused by the stray capacitance and membrane capacitance renders this method unstable even at frequencies of a few kHz when a large gain amplifier is used in the loop. Fig. 4.3 are magnitude and transient responses of a proportional control scheme with clamp gains varied from 22 dB to 26 dB (amplifier gains of 20 and 30 respectively) and capacitance compensation applied to diminish the effect of stray capacitance (as will be explained in the following section). It is clearly seen that as the gain increases beyond 25 dB, the system becomes unstable and oscillations would occur. This is not suitable because a significant steady state error of approximately 10% is still present in the response.

A controller that would enable the system to clamp the membrane voltage rapidly while still allowing zero steady state error is the proportional-integral

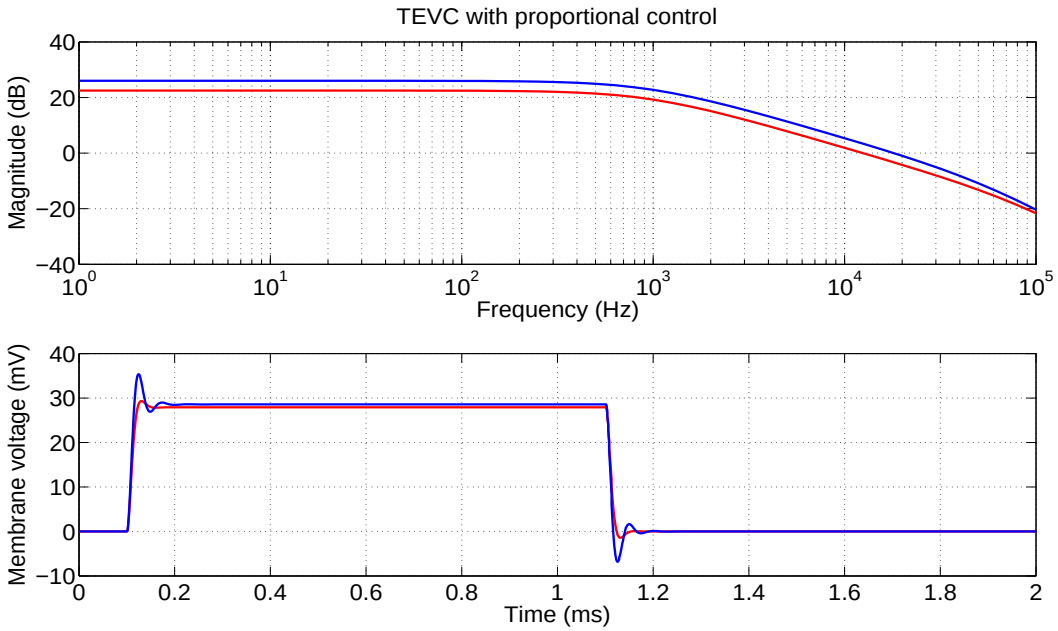


Figure 4.3: TEVC with proportional control : Open-loop gain and transient response with proportional gains of 20 and 30. Model parameters are R_e = 5 MΩ, C_s = 1 pF, R_m = 10 MΩ, C_m = 50 pF.

(PI) controller. The proportional component has a moderate gain and is designed to react to instantaneous changes in the membrane potential while the integral component reduces the steady state error to zero because of the pole at the origin.

The transfer function with the PI controller included in the feedback loop is given by

$$H(s) = \left(\frac{1 + sk\tau_c}{s\tau_c}\right)\left(\frac{A_{cp}}{1 + s\tau_0'}\right)\left(\frac{1}{1 + s\tau_e}\right). \tag{4.13}$$

where k=proportional gain of the controller, τ_c=integrator time constant of the controller and τ_e=low-pass time constant formed at the voltage recording electrode.

The low-pass filter at the input of the clamp will be neutralized by capacitance compensation and so the term involving τ_e can be neglected. The PI controller is designed so that the membrane time constant is compensated

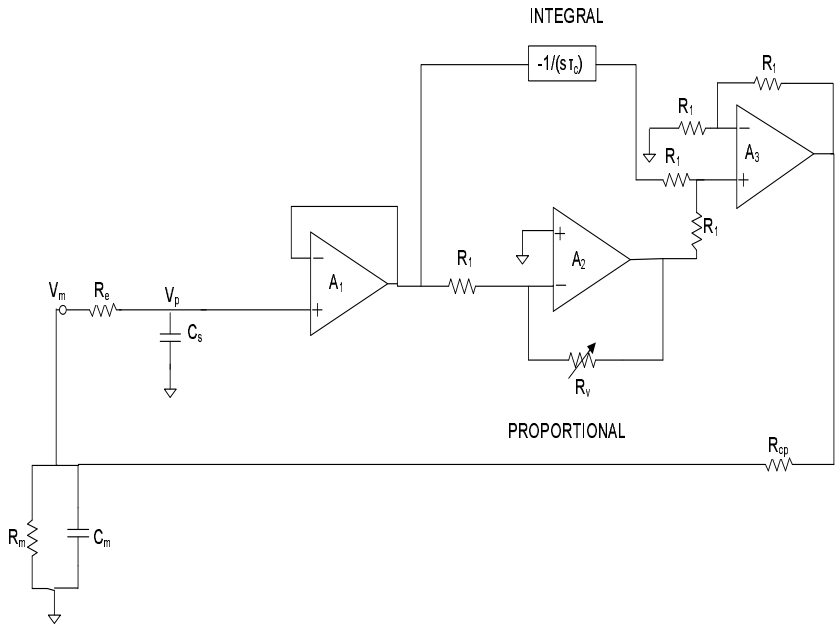


Figure 4.4: TEVC with PI controller.

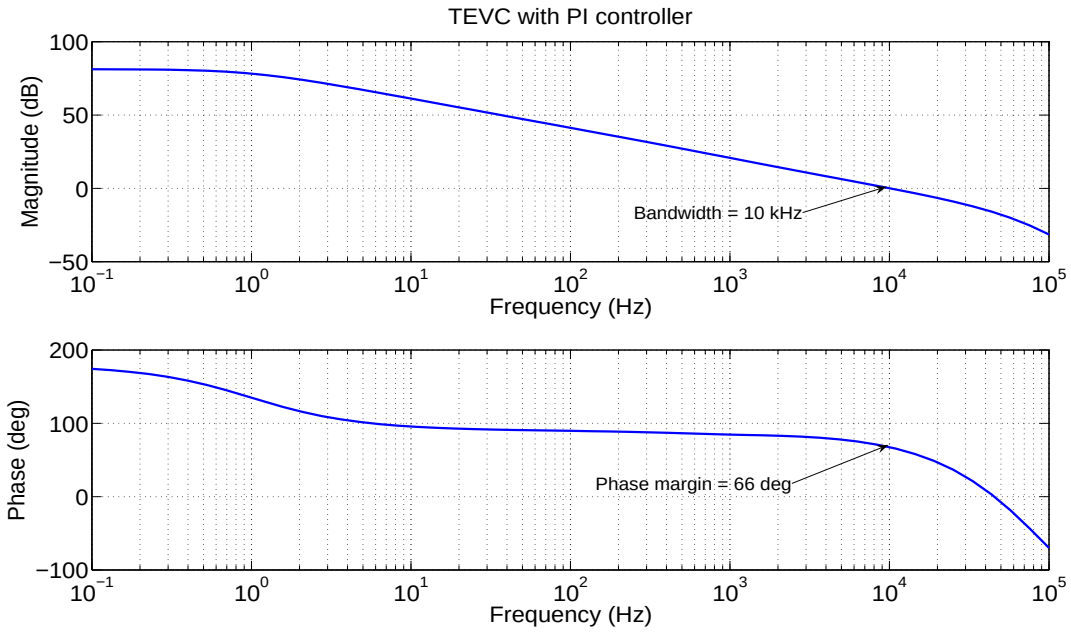


Figure 4.5: Magnitude and phase response of the TEVC with PI controller.

for by the zero in the controller by selecting

$$1 + sk\tau_c = 1 + s\tau_0'.$$

The pole created by the origin due to the term τ_c will provide a high DC gain and reduce the steady-state error to zero. In addition, the proportional gain will determine the bandwidth of the circuit. By selecting $k = Z_{m(@10kHz)}/(R_{cp} + Z_{m(@10kHz)})$, we design the system to achieve a closed-loop bandwidth of 10 kHz which is sufficient to clamp rapid ionic currents as well as respond quickly to changes in reference voltage.

4.3 Capacitance Compensation

A problem that arises in all neural recording setups is that of stray capacitance at the input of the recording circuitry causing the bandwidth of the circuit to degrade excessively. The microelectrode itself is of extremely high resistance(of the order of MΩ) and any stray capacitance at the input of the electronics forms a first-order lowpass R-C circuit. As a typical example if a microelectrode of resistance 10 MΩ is shunted by a stray capacitance of 10 pF, the resulting 3 dB bandwidth of this input filter is 1.59 kHz and high-bandwidth electronics are of no consequence thereafter. In order to compensate the effects of parasitic capacitances, a circuit which performs capacitance neutralization shown in Fig. 4.6 is used.

The neutralizing current is given by

$$I_n = \frac{A_n V_p}{\frac{1}{j\omega C_n} + \frac{R_e}{j\omega R_e C_{in} + 1}}. \tag{4.14}$$

If $R_e \gg 1/j\omega C_s$ this equation simplifies to

$$I_n = A_n V_p j\omega \frac{C_n C_{in}}{C_n + C_{in}}. \tag{4.15}$$

This can be made equal to the current through the stray capacitance $I_{in} = V_p j\omega C_{in}$ provided that

$$A_n = 1 + \frac{C_{in}}{C_n}. \tag{4.16}$$

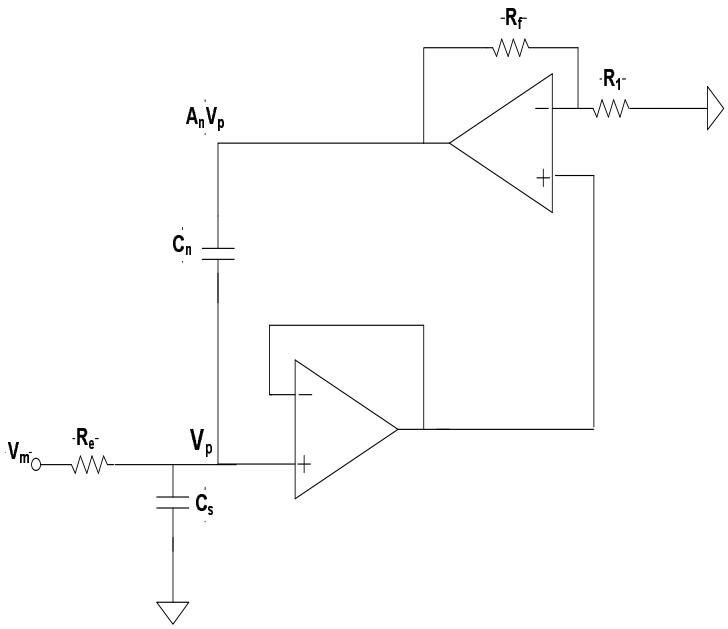


Figure 4.6: Capacitance neutralization circuit diagram.

With this setting of the feedback amplifier, the transient current through the stray capacitance is provided by the neutralizing capacitance to a first-order and a significant improvement in the frequency response can be obtained. The neutralizing capacitance C_n must be chosen as a small value, typically 1-5 pF so that the neutralization circuit itself does not amplify noise inherent to the amplifiers in the circuit. The noise increases by 20 dB/decade at frequencies greater than $[1/2\pi R_e(C_{in} + C_n)]$ and hence attempts must be made to minimize both C_{in} and C_n as much as possible.

In the preceding analysis, second-order effects caused by the finite bandwidth of the feedback amplifier are ignored. These effects ensure that the stray capacitance cannot be completely compensated and also cause instability in the response. Assuming that the fraction of capacitance that is compensated is given by $\alpha C_{in} = (A_n - 1)C_f$ and that the amplifier is a single-pole system with the pole at τ_a, the ratio of the pipette potential to the membrane potential is given by

$$\frac{V_p(s)}{V_m(s)} = \frac{1}{1 + sR_e[C_t - A(s)C_f]}. \tag{4.17}$$

Substituting the value of A(s) in (4.17),

$$\frac{V_p(s)}{V_m(s)} = \frac{1}{1 + sR_e\left[C_t - \dfrac{A_n C_f}{1 + s\tau_a}\right]}. \tag{4.18}$$

On simplifying (4.18), we get

$$\frac{V_p(s)}{V_m(s)} = \frac{1 + s\tau_a}{s^2\tau_a C_t R_e + s(R_e C_t - kR_e C_f + \tau_a) + 1}. \tag{4.19}$$

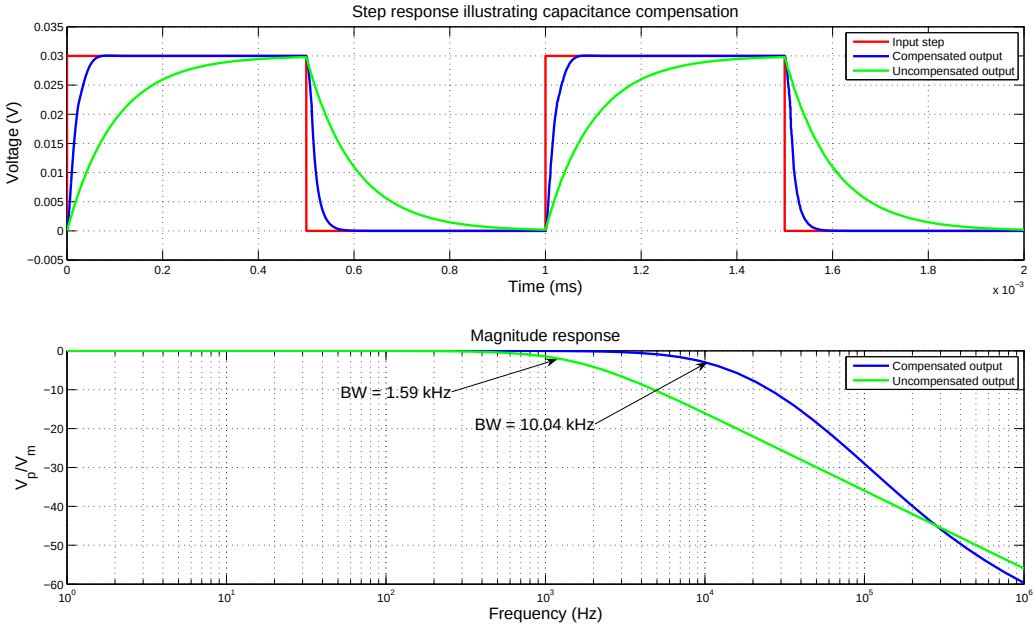


Figure 4.7: Capacitance neutralization transient and AC response.

Comparing the denominator with a standard second-order system, the natural frequency and damping ratio are given by

$$\omega_n = \frac{1}{\sqrt{\tau_a R_e C_t}} \tag{4.20}$$

$$\zeta = \frac{\alpha R_e C_{in} + \tau_a}{2\sqrt{\tau_a R_e C_t}}. \tag{4.21}$$

The critical damping ratio is unity; if it falls below this value, the circuit is

underdamped and oscillations occur which could damage the specimen under observation. This restricts the maximum compensation can be achieved and is given by

$$\alpha \leq 1 - \frac{2\sqrt{\tau_a R_e C_t} - \tau_a}{R_e C_{in}}. \tag{4.22}$$

4.4 Series Resistance Cancellation for the cSEVC

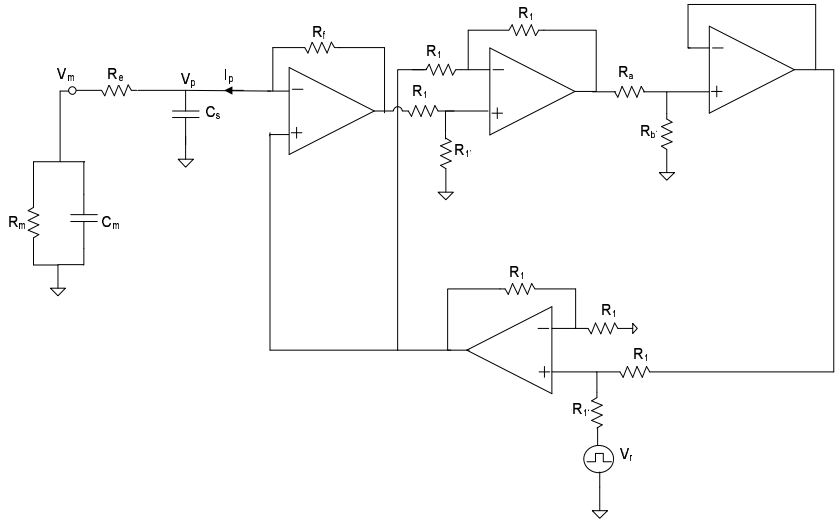


Figure 4.8: Continuous single electrode voltage clamp with series resistance compensation using the prediction method.

In the continuous Single Electrode Voltage Clamp (cSEVC), the potential recorded at the pipette tip is not the voltage across the membrane. A whole-cell current of 1 nA through a microelectrode of resistance 10 MΩ causes a steady-state voltage error of 10 mV. In addition, the membrane capacitance is charged through this series resistance and the bandwidth of the voltage clamp system reduces to R_eC_m. With a typical C_m value of 10-100 pF, the bandwidth is only of the order of a few hundred Hz. Typically, it may be necessary to clamp rapid ionic currents with bandwidths approaching 10 kHz. Hence there must be a method to compensate for this series resistance in order to reduce steady-state errors and improve the transient response.

The conventional method of compensating this series resistance is to monitor the membrane current and add a multiplied version of this current signal to the reference voltage. The feedback loop is analyzed in a similar manner to the capacitance compensation circuit. The membrane current is first converted to a voltage signal by the I/V converter and is then fed into a voltage divider with a gain of $k_R = (1 + R_a/R_b)$to obtain the compensating voltage. The I/V converter is assumed to have a transimpedance given by Z(s). The ratio of the membrane potential to the reference potential is given by

$$\frac{V_m(s)}{V_r(s)} = \frac{1}{1 + sC_m[R_e - k_R Z(s)]}. \tag{4.23}$$

Assuming that the I/V converter has a single pole at τ_z and that the amount of resistance compensated is given by βR_e, this transfer function simplifies to

$$\frac{V_m(s)}{V_r(s)} = \frac{1}{1 + sC_m\left[R_e - \dfrac{\beta R_e}{1 + s\tau_z}\right]}. \tag{4.24}$$

$$\frac{V_m(s)}{V_r(s)} = \frac{1 + s\tau_z}{s^2\tau_z R_e C_m + s(1-\beta)R_e C_m + 1} \tag{4.25}$$

Comparing the denominator with a standard second-order system, the natural frequency and damping ratio are given by

$$\omega_n = \frac{1}{\sqrt{\tau_z R_e C_m}} \tag{4.26}$$

$$\zeta = \frac{(1-\beta)\sqrt{R_e C_m}}{2\sqrt{\tau_z}}. \tag{4.27}$$

The limit of critical damping is then given by

$$\beta \leq 1 - 2\sqrt{\frac{\tau_z}{R_e C_m}}. \tag{4.28}$$

To achieve 90% series resistance compensation in the closed-loop system, for typical R_s and C_m values of 10 MΩ and 50 pF, the bandwidth of the

current measurement circuitry must be in excess of 130 kHz which can be difficult to achieve in practice. An even greater problem is created when capacitance neutralization circuitry is introduced; the residual capacitance must be reduced to <0.05 pF [17] which is practically not attainable.

It was therefore decided to use an alternative method of series resistance compensation first proposed in [18]. This configuration attempts to mimic the TEVC : from the pipette potential and current, an estimate of the membrane potential V'_m is calculated and is compared with the reference signal V_r. The error signal between these two is then converted to a current I_p using a voltage-controlled current source similar to that used in the current clamp.

The membrane potential is given by

$$V_m = (1 + s\tau_p)V_p - I_p R_s. \tag{4.29}$$

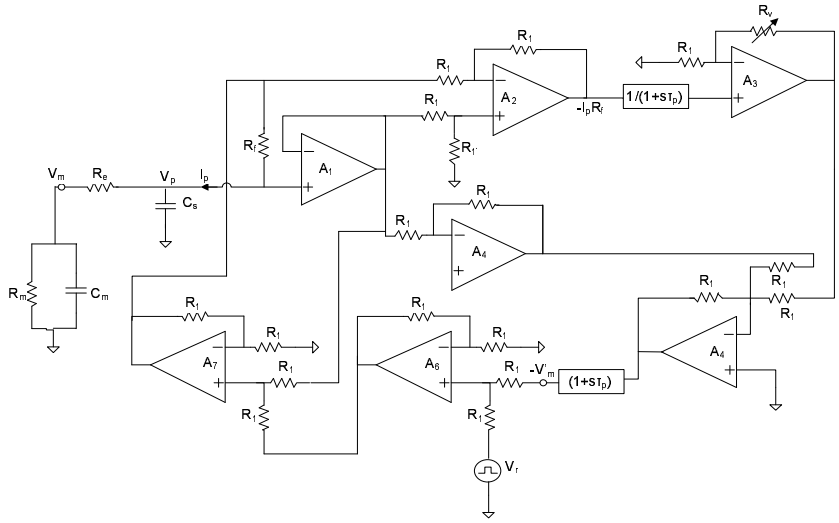


Figure 4.9: Series resistance compensation using membrane state estimator.

In order to implement this transfer function, the circuit shown in Fig. 4.9 is used which incorporates the low noise amplifiers designed earlier. As opposed to a conventional patch-clamp amplifier, which uses an I/V converter headstage, a buffer amplifier is used in the headstage. The current drive is provided by amplifier A_7 which acts as a controlled current source. The

voltage drop across resistor R_0 is used to monitor the current flowing into the pipette. It is multiplied by a variable gain amplifier in order to generate the I_pR_s product. This current signal is then low-pass filtered with a time constant τ_p which is given by the R_1C_1 product. It is summed with the pipette potential in A_4. The resulting signal is then multiplied by $(1+\tau_p)$ using A_5 and finally compared with the reference signal in A_6.

The overall transfer function is then given by

$$V'_m = \left(V_p - \frac{I_p R_s}{1 + s\tau_p}\right)(1 + s\tau_p). \tag{4.30}$$

This equation, on simplifying yields (4.29) which shows that this method should be able to compensate for the drop across the series resistance of the electrode.

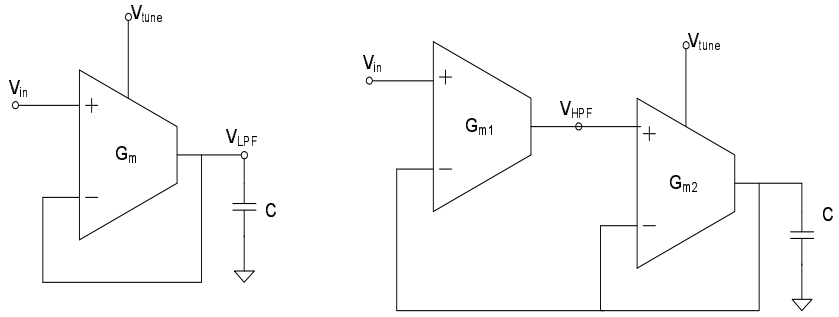


Figure 4.10: Integrator and differentiator structures.

In order to generate the transfer functions having time constant τ_p, G_m-C integrator and differentiator topologies are implemented as suggested by [27] and shown in Fig. 4.10. For the integrator topology, small signal analysis reveals the transfer function to be

$$\frac{V_{LPF}}{V_{in}} = \frac{1}{1 + \dfrac{sC}{G_m}}. \tag{4.31}$$

The current biasing the transconductor element is varied digitally using the splitter chain described earlier. The differentiator can be thought of as generating a difference between the input voltage and its low-pass filtered

version. The resulting transfer function of the differentiator is evaluated as

$$\frac{V_{HPF}}{V_{in}} = \frac{1 + \dfrac{sC}{G_{m2}}}{1 + \dfrac{sC}{G_{m2}(1 + A_1)}}. \tag{4.32}$$

where A_1 is the open loop gain of the OTA with transconductance G_{m1}. Again, the bias voltage that determines the transconductance G_{m2} is varied using the digitally controlled current source so as to vary the frequency at which the magnitude response will begin increasing at 20 dB/decade.

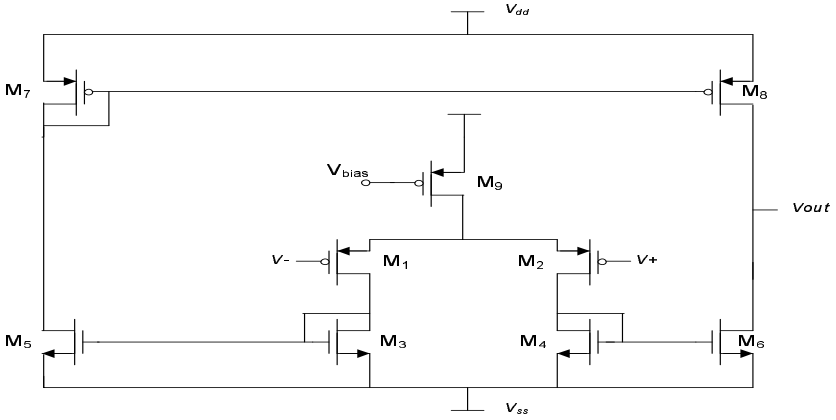


Figure 4.11: Tunable transconductor used in G_m-C integrator and differentiator.

The results of implementing a series resistance compensation scheme can be easily observed using the transient response to a step in the reference potential.

First of all, the speed of the response is much faster : the system is able to clamp the membrane potential in 200 μs as opposed to a large time constant without compensation of about 10 ms. Secondly, the steady state error due to the drop across the electrode resistance is now compensated for and the membrane potential is equal to the reference potential.

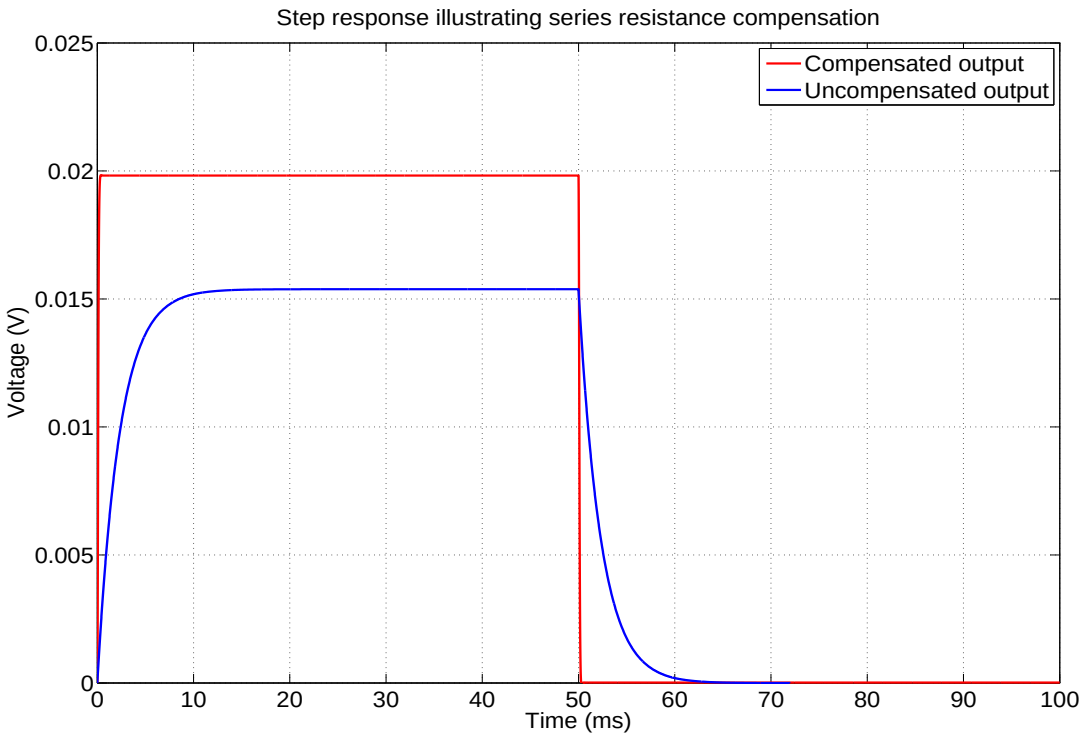


Figure 4.12: Transient response with and without series resistance compensation : Response to a 20 mV step in the reference potential at t=0.

4.5 Voltage-Clamp controlled Current-Clamp Configuration

The current clamp configuration is generally used to record action potentials or postsynaptic potentials from excitable membranes. In this setup, only the current through the membrane is fixed at a reference value but the membrane potential is allowed to vary. However it is sometimes required to ensure that the average membrane potential is fixed while activating these action potentials. Conventional patch, voltage and current clamp setups do not allow for this mode of recording.

In order to perform current-clamp recording at a fixed holding potential, a voltage-clamp controlled current-clamp configuration was proposed [19, 20]. [20] uses a conventional patch-clamp amplifier and filters the recorded membrane potential using a low-pass filter with a high time constant in order

to hold the average voltage at a steady value.This setup cannot be used with conventional microelectrodes and hence [19] creates the same function in a dSEVC configuration. This work has focused on the design of the cSEVC and we therefore propose an implementation of this configuration in the cSEVC. The mechanism remains much the same - a large time constant is used to filter the voltage signal in order to maintain the steady voltage at an average value while the current is clamped in order to activate action or postsynaptic potentials.

However, it is difficult to implement large time constant filters on chip. In fact, the time constants required in the low pass filter for the voltage-clamp controlled current-clamp are of the order of multiple seconds. We therefore use the modified current-mirror OTA topology shown in Fig. 4.13.

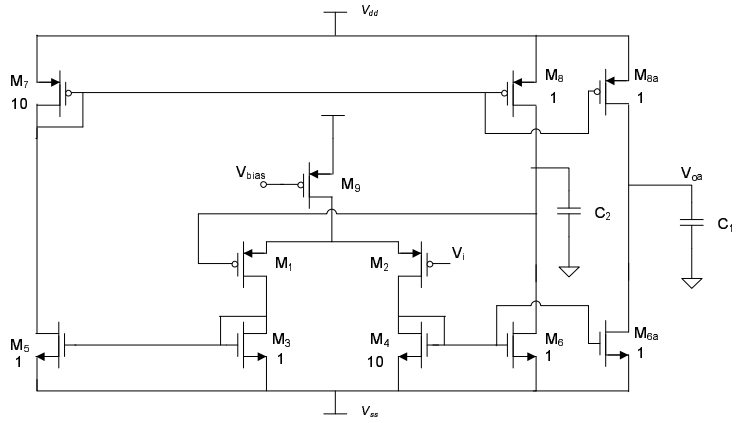


Figure 4.13: Low pass g_m-C filter to implement large time constants of the order of seconds on chip.

The current mirror ratio of 10:1 ensures that the dc biasing current in the output branch is an order of magnitude lower than the current through the input differential pair $M_{1,2}$. The output current with the negative feedback to M_1 and a ratio of B:1 of the current mirrors is given by

$$i_o = \frac{g_m/B}{1 + g_m r_o/B} v_i = \frac{v_i}{r_o}. \tag{4.33}$$

This output current is mirrored to the branch M_{6a}-M_{8a} to generate the

output voltage given by

$$v_{oa} = \frac{(v_i/r_o)r_o}{1 + sr_oC_L} = \frac{v_i}{1 + sr_oC_L}. \tag{4.34}$$

Thus the low pass filter topology implemented uses negative feedback to reduce the gain to unity using the first closed-loop but simultaneously allows the output stage to operate in open-loop so that the low cutoff frequency is preserved. It is therefore possible to implement large time constants of the order of several seconds on-chip.

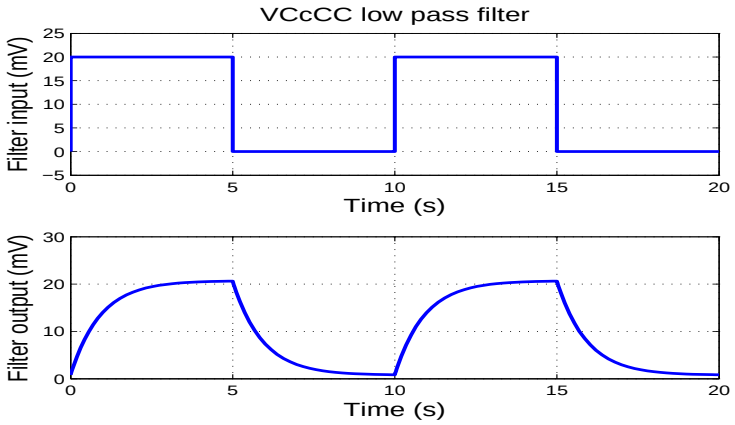


Figure 4.14: Transient response of low pass filter used in the VCcCC loop.

In order to have such large time constants, the original tail current through the differential pair should also be very small, of the order of 1-10 nA. This is achieved by adding three more splitter cells to the chain in order to achieve a biasing current of 3 nA. The curve showing the transient response to the filter to a square wave input is displayed in Fig. 4.14 and it is observed that the time constant achieved is around 4 s.

4.6 Estimation of Series Resistance and Compensation Capacitance

In order to precisely set series resistance cancellation and capacitance neutralization controls, it is necessary to obtain accurate estimates of the parameters

to be compensated for. A common and rather simplistic method to obtain these estimates is to inject a current pulse of i nA and observe the pipette voltage in response to it. The steady state voltage would be $V = i(R_m + R_e)$. The rise of this voltage would be divided into two distinct regimes; the initial fast rise governed by the electrode time constant R_eC_s and a following gradual rise governed by the membrane time constant R_mC_m.

However, this is an idealized assumption since very often the two time constants are of similar magnitude and cannot be distinguished from one another in the response of the pipette voltage. We therefore choose to implement a modified method proposed in [29]. In this technique, a current step is again applied and thereafter a curve is fitted by maximum likelihood to the response. The curve that is fitted is given by

$$v(t) = i[ae^{-\mu_1(t-t_0)} + be^{-\mu_2(t-t_0)} + c] + v(t_0). \tag{4.35}$$

where

$$\mu_1 = \frac{R_eC_s + R_mC_s + R_mC_m}{2R_eC_sR_mC_m} + \frac{s}{2} \tag{4.36}$$

$$\mu_2 = \frac{R_eC_s + R_mC_s + R_mC_m}{2R_eC_sR_mC_m} - \frac{s}{2} \tag{4.37}$$

$$s = \frac{\sqrt{R_e^2C_s^2 + 2R_eR_mC_s^2 - 2R_eC_sR_mC_m + R_m^2C_s^2 + 2R_m^2C_mC_s + R_m^2C_m^2}}{R_eC_sR_mC_m} \tag{4.38}$$

$$a = (-\mu_2 c - 1/C_s)/s \tag{4.39}$$

$$b = (-\mu_1 c - 1/C_s)/s \tag{4.40}$$

$$c = R_e + R_m \tag{4.41}$$

These equations are then solved in order to obtain the cell and electrode parameters as follows.

$$s = \mu_1 - \mu_2 \tag{4.42}$$

$$C_s = \frac{2}{s(b-a)+c(\mu_1+\mu_2)} \tag{4.43}$$

$$x_1 = R_e C_s R_m C_m = \frac{4}{4(\mu_2+s/2)^2 - s^2} \tag{4.44}$$

$$x_2 = 2\Big(\mu_2 + \frac{s}{2}\Big)x_1 - cC_s \tag{4.45}$$

$$R_e = \frac{x_1}{x_2 C_s} \tag{4.46}$$

$$R_m = c - R_e \tag{4.47}$$

$$C_m = \frac{x_2}{R_m} \tag{4.48}$$

In order to examine the effectiveness of this method of determining cell parameters, two simulations and subsequent fits are performed. The first uses parameters that realise a cell time constant that is much larger than the electrode time constant while the second simulation uses cell and electrode time constants of a similar magnitude. The results of the curve fits are shown in Fig. 4.15 and Fig. 4.16.

In the first simulation, two distinct time constants can be observed in the voltage curve since the pipette and membrane time constants are vastly different. The equations on solving yield resistance and capacitance values that match well with the actual values as seen in 4.6.

In the second simulation however, it becomes impossible to distinguish separate time constants since those of the pipette and membrane are of similar magnitude. In fact, on observing the equations (4.36) and (4.37), it becomes apparent that the two time constants each contain terms which include all four of the resistance and capacitance parameters. This problem is solved by the curve fit and subsequent equations which yield values shown in 4.6 which are once again in good agreement with the actual resistance and capacitance values.

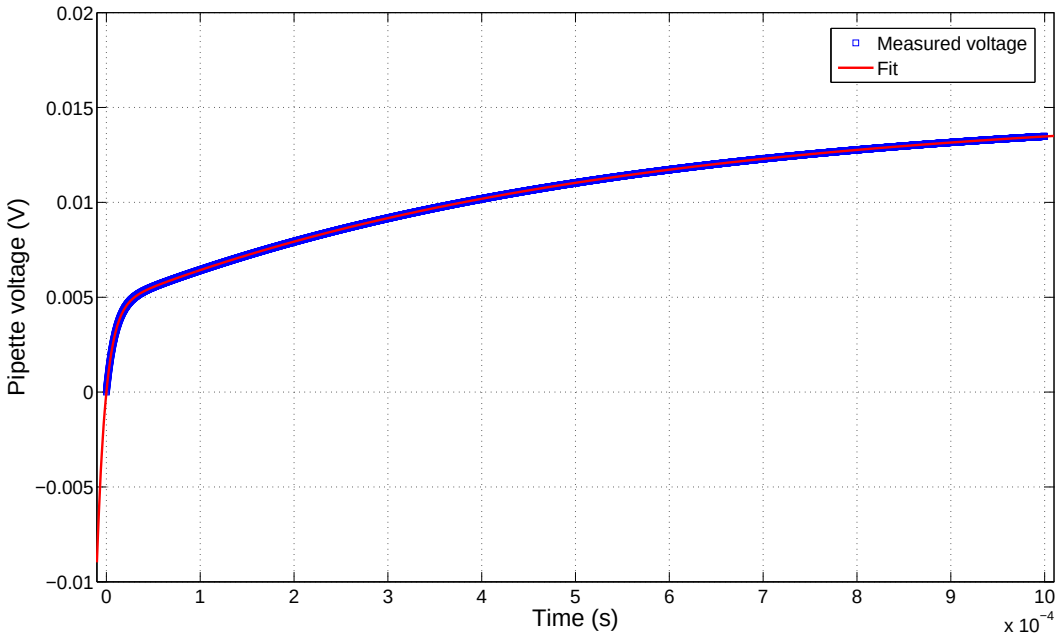


Figure 4.15: Curve fit for model with parameters given in Table 4.6.

Table 4.1: Cell and electrode parameters obtained from the fit in Fig. 4.15.

Parameter	Actual value	Estimated value
R_e	5 MΩ	4.99 MΩ
C_s	2 pF	1.98 pF
R_m	10 MΩ	9.989 MΩ
C_m	50 pF	49.85 pF

It is observed that this method is extremely accurate even when the electrode and membrane time constant are of comparable value and is therefore a significant improvement over the simplistic method of dividing the response into two significant time constant regimes. As with other estimation methods, this method relies on the parameters remaining constant during the estimation which indicates that the pulse of current must not hyperpolarize the cell as this would change R_m significantly during the course of the estimate.

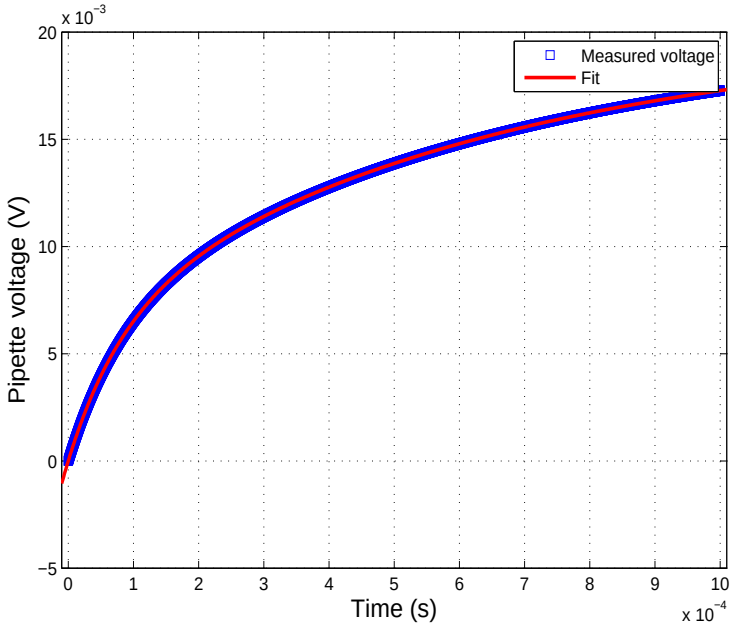


Figure 4.16: Curve fit for model with parameters given in Table 4.6.

Table 4.2: in Fig. 4.16.

Parameter	Actual value	Estimated value
R_e	10 MΩ	10 MΩ
C_s	10 pF	9.996 pF
R_m	10 MΩ	10 MΩ
C_m	50 pF	50.18 pF

Chapter 5

SIMULATION RESULTS

5.1 Neuron Model

In order to test the performance of the intracellular recording circuits developed in this work, it was necessary to create a neuron model that could be used for simulation using SPECTRE. Most membrane models implemented for testing such circuits are simple passive R-C parallel combinations. However, it is crucial to determine how the intracellular recording circuits designed in this work respond to dynamic changes in membrane conductance. For this purpose, a dynamic analog neuron model is implemented as proposed in [37].

The basic properties that the circuit should possess are a resting potential across the membrane in addition to a repetitive firing characteristic when stimulated by external current pulses. This suggests a voltage-controlled oscillating circuit as depicted in Fig. 5.1.

In order to implement this circuit, the steady state conductance and capacitance of the membrane are implemented as R_1 and C_1 in order to define the membrane time constant. The negative resistance is implemented using transistors M_1-M_3 which as shown in Fig. 5.2. From the transfer characteristic, it can be observed that as the voltage input is increased, the current supplied by the source decreases. This is because the required current is now being supplied by the pMOS current mirror $M_{2,3}$.

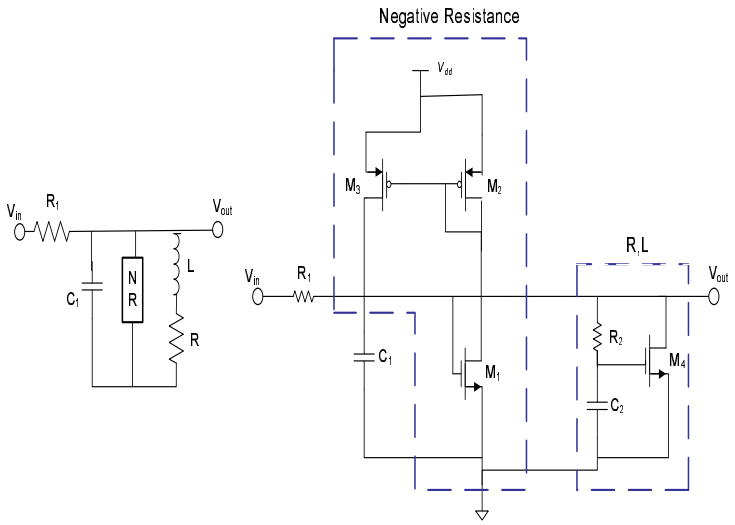
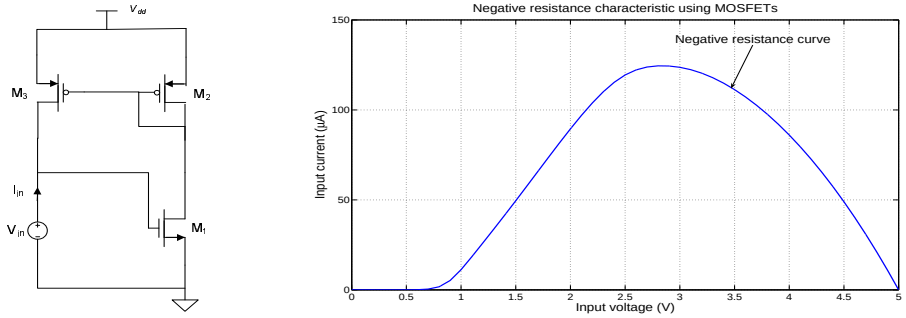


Figure 5.1: Equivalent circuit of the neuron model [37].



(a) Negative resistance circuit.

(b) V/I characteristic.

Figure 5.2: Voltage-controlled negative resistance.

Finally the inductance is obtained through R_2-C_2 and the transistor M_4. Evaluating this circuit using the small-signal model of M_4, it is found that the input impedance is given by

$$Z_{in} = \frac{1 + sR_2C_2}{g_m}.$$

This is equivalent to a series combination of a resistance and an inductance. Thus the circuit using MOSFETs and passive components is used to realise an excitable model of a membrane that can be used to check the

performance of voltage and current clamp circuits. The transient response to an input stimulus is seen to reflect the various phases of an action potential including hyperpolarization, repolarization, an undershoot and finally a recovery to the resting membrane potential as described in Chapter 2.

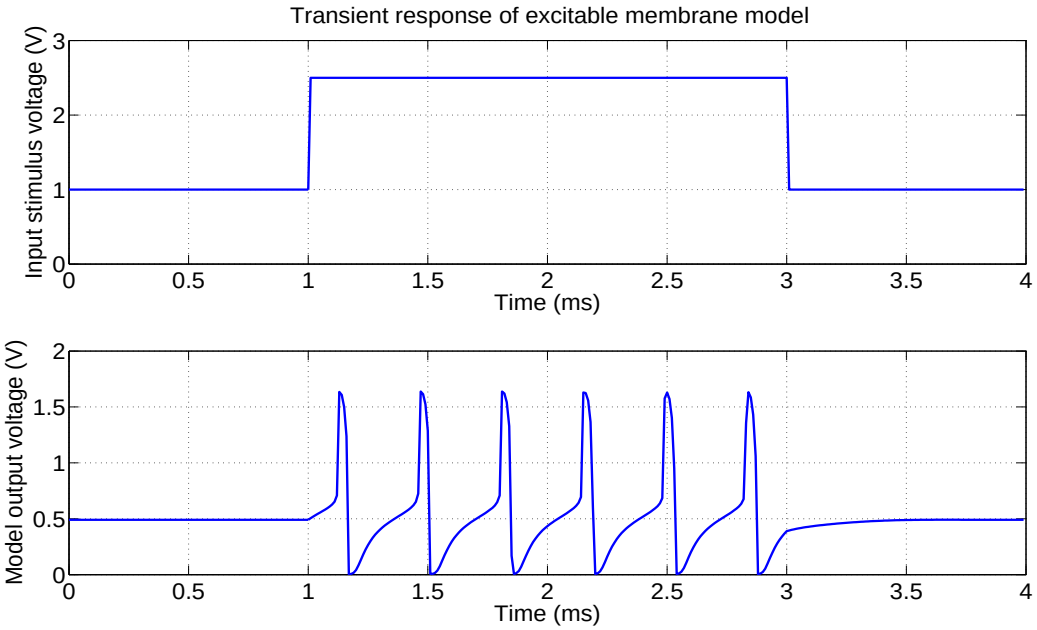


Figure 5.3: Response of the excitable neuron model to input stimulus voltage.

5.2 Performance of the designed clamp circuits

5.2.1 Current Clamp

The excitable membrane model is typically suited to simulation of the current clamp where a current pulse injected into the model causes the membrane potential to cross a threshold and action potentials are thereby generated. These action potentials can then be observed while maintaining a constant stimulus current as depicted in Fig. 5.4.

For the circuit with which the simulation is performed a 3 nA current is passed through the membrane in order to generate the action potentials.

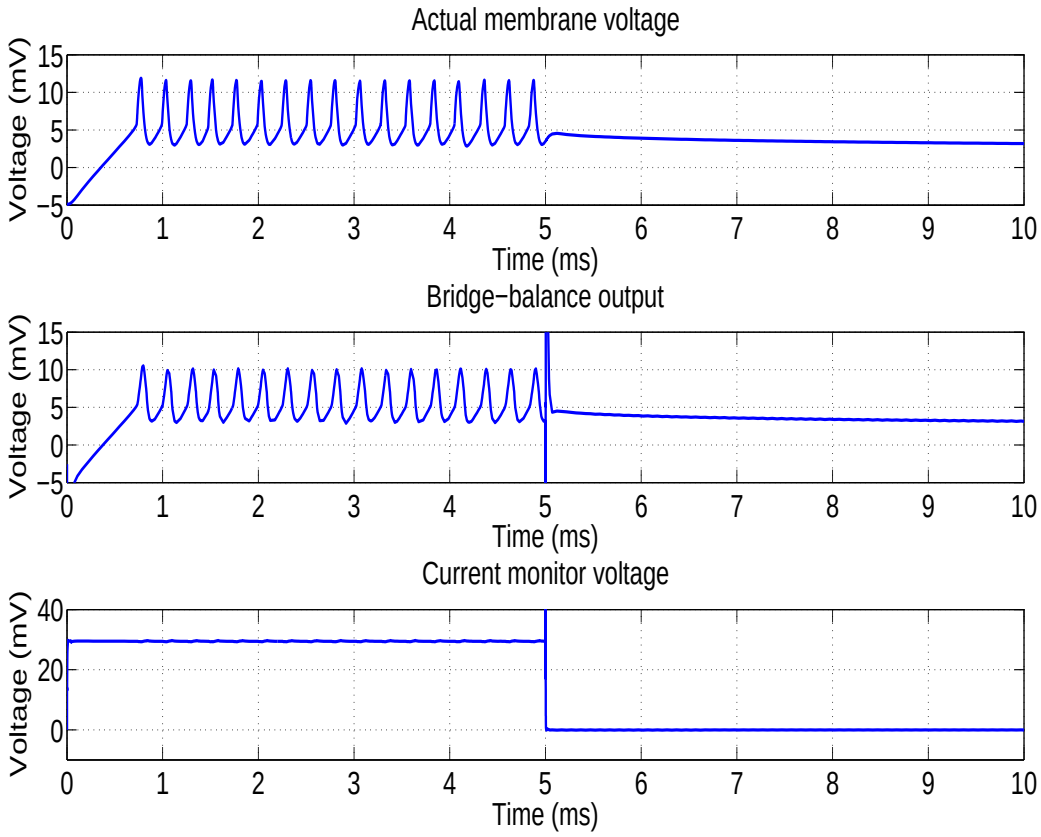


Figure 5.4: Transient simulation of the current clamp circuit with the neuron model stimulated by a 3 nA current pulse. Cell parameters are R_m=10 MΩ, C_m=100 pF, R_e=10 MΩ, C_p=10 pF.

However the CMOS membrane model requires currents of the order of 1-5 μA to stimulate action potentials and hence the reference current is multiplied by a factor of 100 using a current controlled current source (CCCS) for the purpose of the simulation. In addition the action potential is divided by a factor of 100 in order to realise realistic magnitudes in the mV range. It must be noted that these operations are simply for the purpose of demonstrating that our circuit works satisfactorily and *in-vitro* tests would confirm the performance of the design. A more accurate model would no doubt be useful in simulation work but as of now, the most effective way of testing these circuits would be through fabricating them and actually interfacing them with neurons in an *in-vitro* environment.

The spike observed during a transition to a new reference current is due to the charging of the stray capacitance at the clamp input and no useful transient data is available during this period [30].

5.2.2 Two-electrode Voltage Clamp

The voltage clamp is simulated using a parallel RC circuit. In the TEVC configuration, the PI controller scheme ensures that there is no steady state error in the membrane voltage while the rise time is of the order of 50 μs which is suitable for clamping rapid ionic currents upto about 10 kHz.

The transient response of the TEVC to a stimulating pulse voltage is

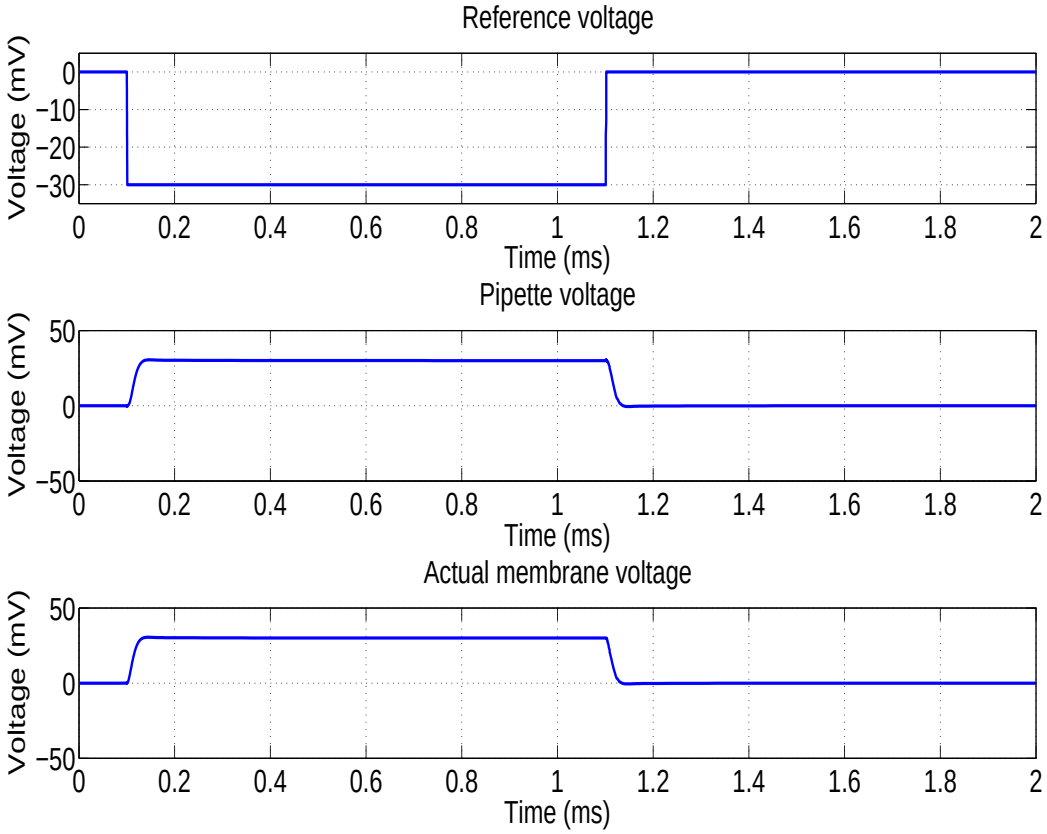


Figure 5.5: Transient simulation of the TEVC circuit with a parallel RC model stimulated by a 30 mV voltage pulse. Cell parameters are R_m=10 MΩ, C_m=50 pF, R_e=5 MΩ, C_p=2 pF.

shown in Fig. 5.5. A slight overshoot in the response gives the fastest rise to the reference potential. The fast response is tuned by varying the gain of the proportional section of the controller. The integrator section provides a DC gain of >80 dB as shown in chapter 4 and hence the steady state error is reduced to zero as is evident in the membrane potential being exactly equal to the reference potential. The capacitance neutralization circuit is used to compensate for the 2 pF stray capacitance at the input terminal which would otherwise make the response sluggish.

5.2.3 Continuous Single Electrode Voltage Clamp

The cSEVC configuration including the series resistance compensation is able to clamp the membrane voltage within about 70 μs typically, thereby allowing it to clamp rapid ionic currents almost as well as the TEVC setup. In addition, 100% series resistance compensation removes the steady-state error from the response.

The frequency response of the cSEVC and its transient response to a stimulating pulse voltage is shown in Fig. 5.6. The crossover frequency is 8 kHz and the potential of the membrane is clamped rapidly, within 50 μs which is a significant improvement over configurations without series resistance cancellation, or the conventional method of series resistance cancellation which is stable only upto about 85%. The initial spike during a reference change is due to the charging of the stray pipette capacitance.

Another important simulation is performed to determine how the circuit responds to sudden changes in channel conductance in the membrane, as this indicates its ability to clamp rapid ionic currents. Initially the membrane resistance is 500 MΩ and after a time of 1 ms has elapsed, it is stepped down to 50 MΩ. From the transient simulation results shown in Fig. 5.7, the cell is clamped to the reference voltage with a fall time of about 35 μs which proves that the design is indeed capable of clamping currents upto 10 kHz frequency.

If the series resistance compensation method is to be reproducible for different values of series electrode resistance and stray parasitic capacitance

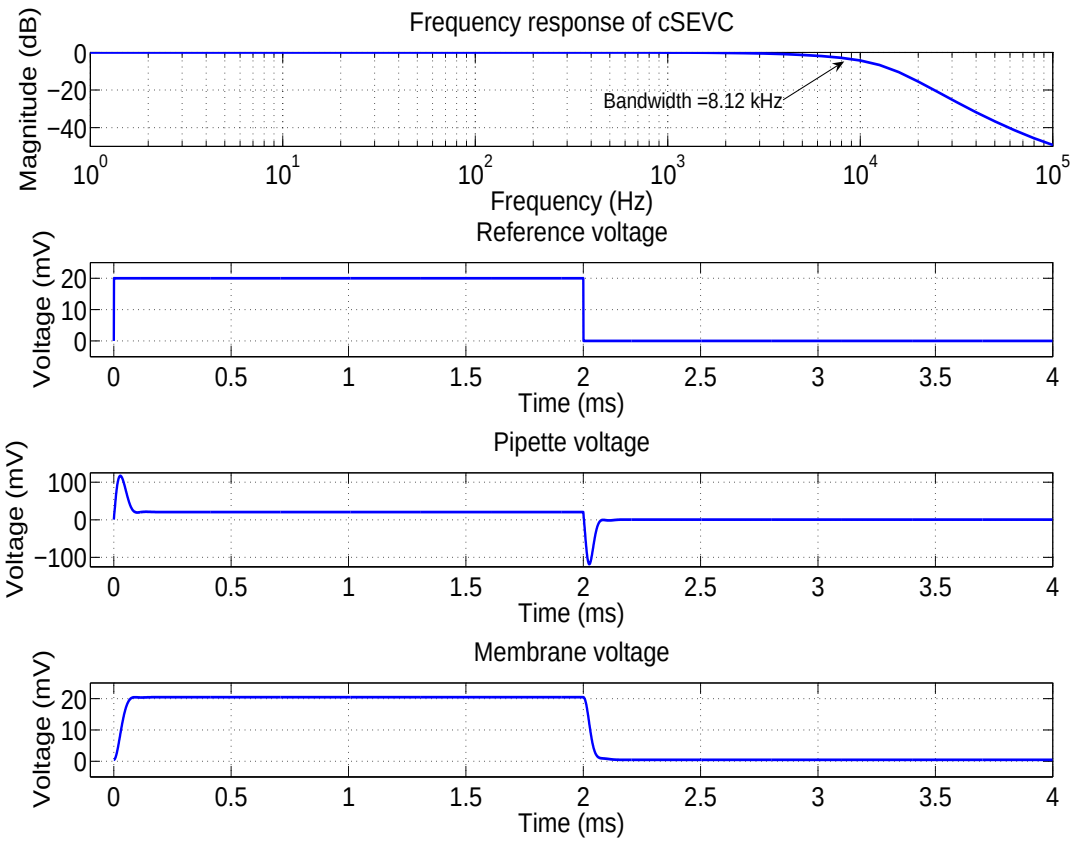


Figure 5.6: Magnitude response and transient simulation of the cSEVC circuit with a parallel RC model stimulated by a 20 mV voltage pulse. Cell parameters are R_m=20 MΩ, C_m=50 pF, R_e=5 MΩ, C_p=2 pF.

at the clamp input, it becomes necessary for the integrator and differentiator that determine the closed-loop frequency response to have tunable time constants. To perform this function, the current-splitter cells are used to provide digitally selected bias current values with 8-bit selectivity to the transconductance cells in the integrator and differentiator. The variation of the cutoff frequencies in these high-pass and low-pass structures with the digital input used to select the currents are illustrated in Fig. 5.8 and Fig. 5.9.

We have assumed electrode resistance values varying from 5-20 MΩ and stray capacitance values varying from 1-10 pF. This requires cutoff frequencies of the filters to be in the range of 0.8-32 kHz. Capacitance and bias values are selected accordingly and the responses shown indicate that the

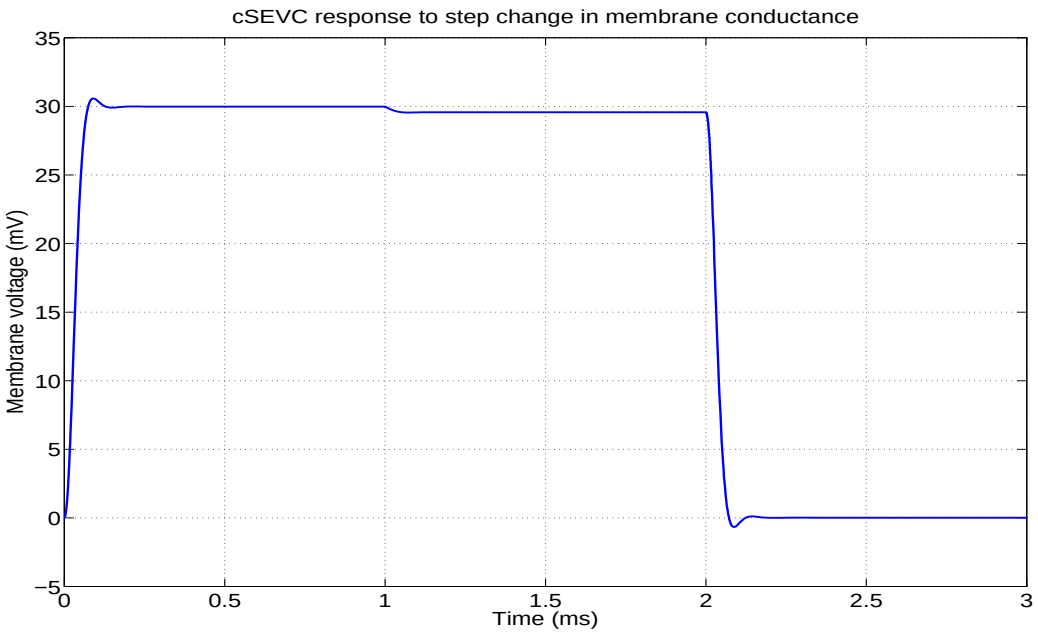


Figure 5.7: Transient simulation of the cSEVC circuit with a parallel RC model stimulated by a 30 mV voltage pulse. Cell parameters are R_m=20 MΩ, C_m=50 pF, R_e=5 MΩ, C_p=2 pF. At t=1 ms, R_m is stepped down from 500 MΩ to 50 MΩ.

cutoff frequencies of the designed circuits can be tuned over this range.

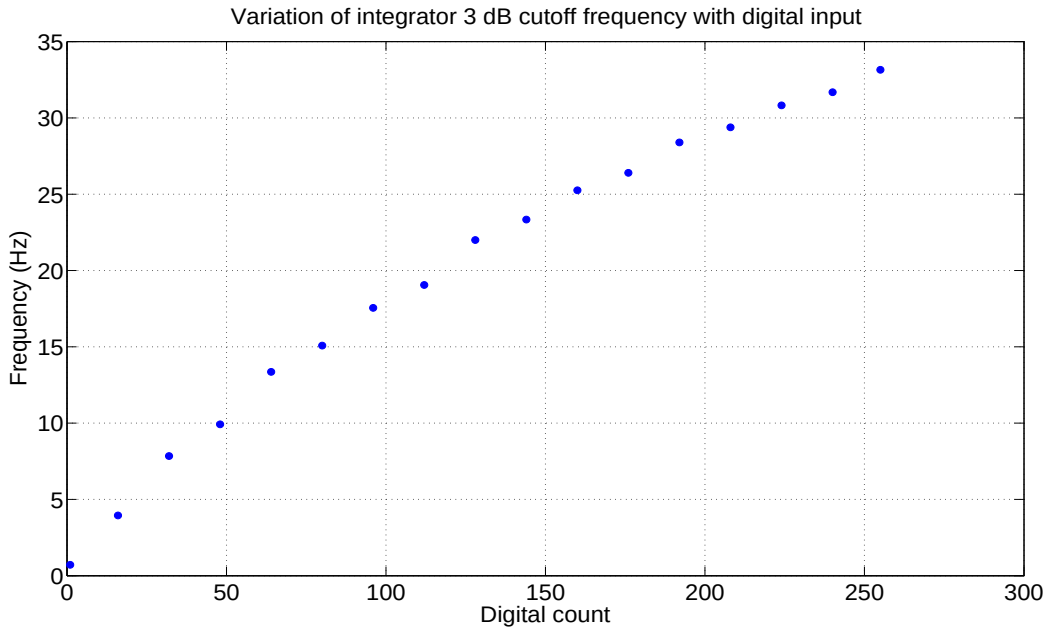


Figure 5.8: Variation of the integrator cutoff frequency with digital input bits controlling the bias currents.

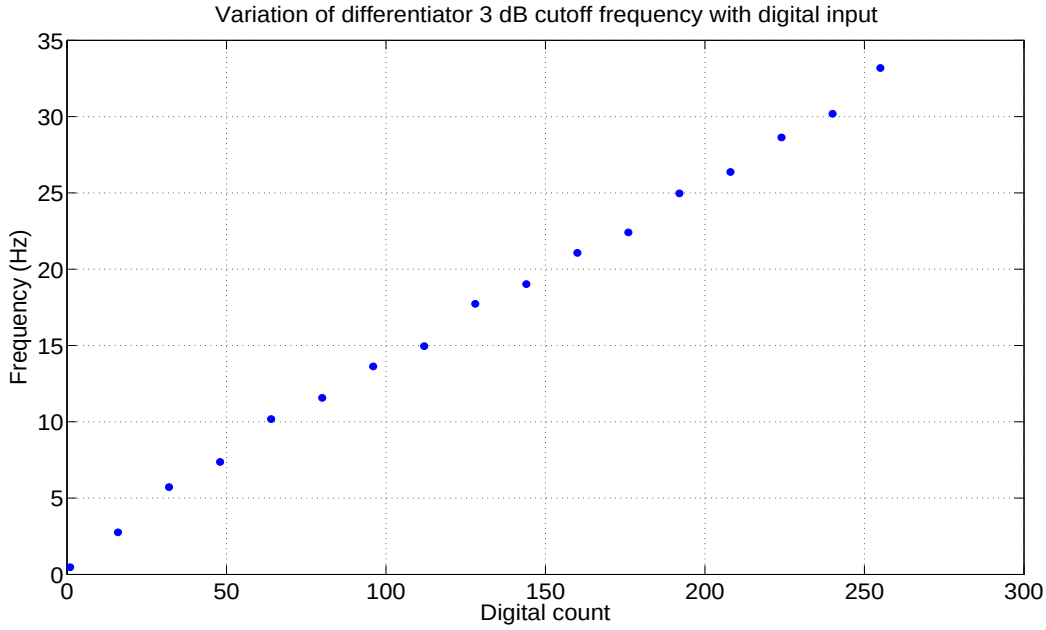


Figure 5.9: Variation of the differentiator cutoff frequency with digital input bits controlling the bias currents.

Chapter 6

CONCLUSION AND FUTURE WORK

The work described in this thesis demonstrates the ability to record intracellular neural signals in a closed-loop manner for the purpose of recording membrane electrical parameters as well as the response of cells to current and voltage stimuli generated by the experimenter. Conventional two-electrode voltage clamp and current clamp circuits are designed along with a continuous single electrode voltage clamp that will prove useful in recording ionic currents from small cells.

The speed of the response of all these circuits is shown to be sufficient to record and control rapid voltage and current changes within the cell and they are therefore suitable for recording from a large range of cell sizes and characteristics. All these configurations are shown to be stable and low-power as well, which is an important consideration when designing devices that may ultimately be implantable. The response of most of these circuits is tunable and can be adjusted according to the cell under observation and the electrodes used to record intracellular activity.

A low-power, low-noise neural amplifier forms the core of the majority of the circuits used in this work and careful attention is paid to its design in order to optimize the noise performance for a limited power budget. This amplifier may also be utilized in an extracellular recording configuration since

it has been shown to have similar performance to other neural amplifiers proposed in literature. Bias circuitry that generates digitally selectable current sources with a high dynamic range are designed and could prove to be extremely useful as reference generators for many types of implantable devices.

Layout has been done using the AMI 0.5 μm process and the chip will be fabricated in the coming months. Significant work still remains in proving this design to be a viable intracellular recording option. Foremost among this is fabricating and testing the chip; although much post-layout simulation work has been presented, only measurements from a fabricated device would confirm the performance of the circuits described in this work. *In-vitro* testing would be of much importance in these measurements since passive and active circuit models of the cell are incapable of fully capturing its characteristics.

This design can also be taken as an important step towards the design of a CMOS dynamic clamp [31] in which artificially generated conductances are introduced into actual biological neurons to create interfaces between real and model neurons. Essentially one can think of this as a current clamp with the reference current being an artificially generated synaptic current that is used to mimic one that would be generated in a real neuron. The dynamic clamp is an important tool in measuring voltage-dependent conductances and observing the dynamics of the interaction between neurons.

Integrated intracellular recording setups are a much needed tool to neuroscientists and it is hoped that the implementation of these circuits on-chip and their integration with silicon microelectrodes will enable researches to perform fast and accurate measurements of intracellular activity leading to important results in the years ahead.

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APPENDIX

Appendix A

Transistor Sizing and Layout

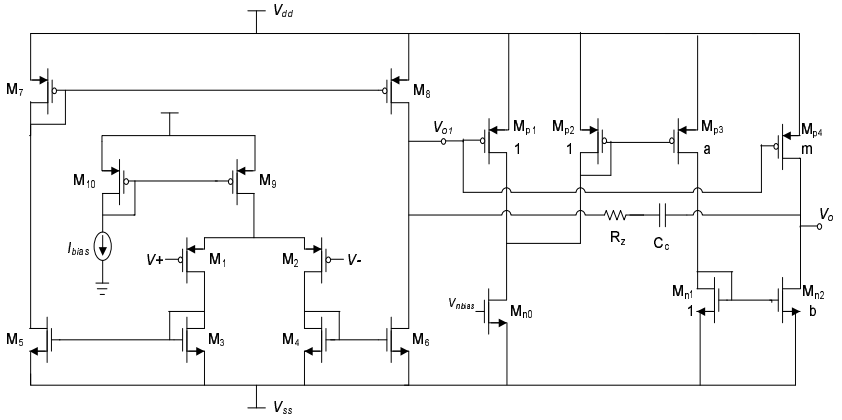

Figure A.1: Miller compensated two-stage amplifier.

$M_{1,2}$	$550.8\mu/1.8\mu$
M_{3-6}	$3.9\mu/19.95\mu$
$M_{7,8}$	$9\mu/9\mu$
M_{n0}	$3\mu/1.2\mu$
$M_{p1,p2}$	$1.5\mu/1.5\mu$
M_{p3}	$3\mu/1.5\mu$
M_{p4}	$1.5\mu/1.5\mu$
M_{n1}	$1.5\mu/1.5\mu$
M_{n2}	$6\mu/1.5\mu$

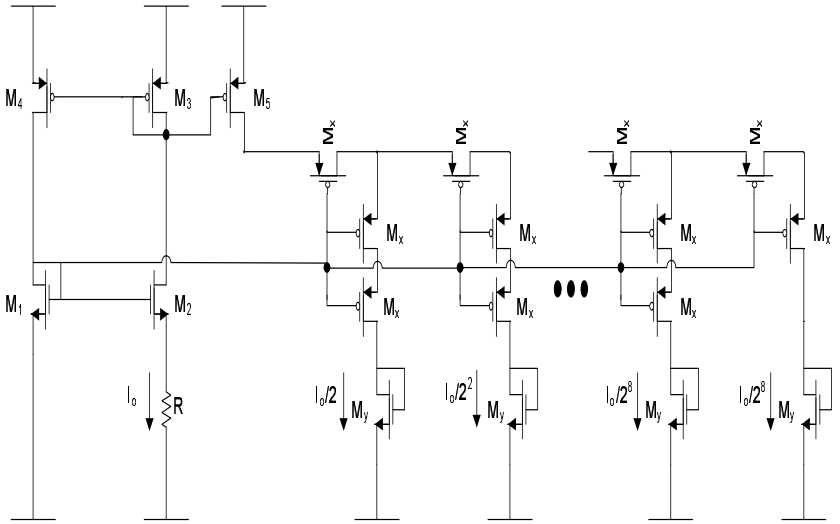

Figure A.2: High dynamic range current splitter bias generator.

M_1	$10.05\mu/1.95\mu$, m=2
M_2	$10.05\mu/1.95\mu$, m=8
$M_{3,4}$	$20.1\mu/4.95\mu$
M_x	$10.05\mu/4.95\mu$
M_y	$10.05\mu/1.95\mu$
R	$8.2k$

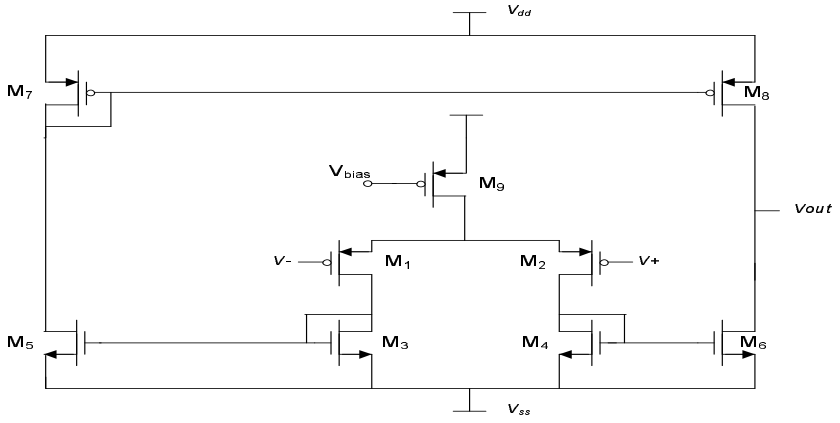

Figure A.3: Tunable transconductor used in G_m-C integrator and differentiator

$M_{1,2}$	$550.8\mu/1.8\mu$
$M_{3,5,6}$	$3.9\mu/19.95\mu$
M_4	$3.9\mu/19.95\mu$, m=10
M_7	$9\mu/9\mu$, m=10
M_8	$9\mu/9\mu$

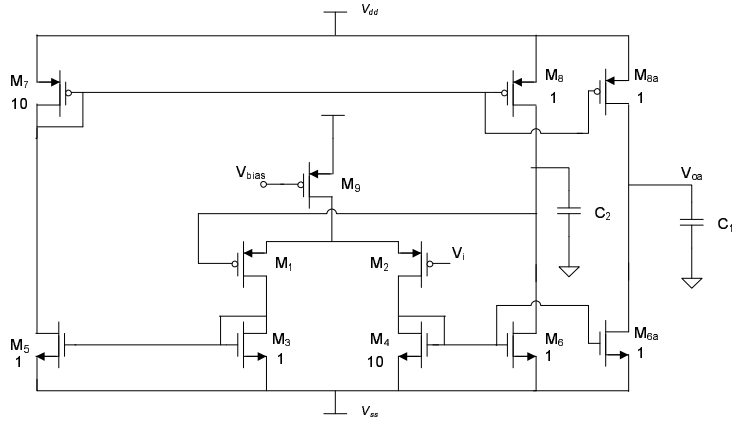

Figure A.4: Low pass g_m-C filter to implement large time constants of the order of seconds on chip.

$M_{1,2}$	$6\mu/1.2\mu$
$M_{3,5,6}$	$3.9\mu/19.95\mu$
M_4	$3.9\mu/19.95\mu$, m=10
M_7	$9\mu/9\mu$, m=10
M_8	$9\mu/9\mu$
M_{6a}	$3.9\mu/19.95\mu$
M_{8a}	$9\mu/9\mu$
C_1	10p
C_2	500f

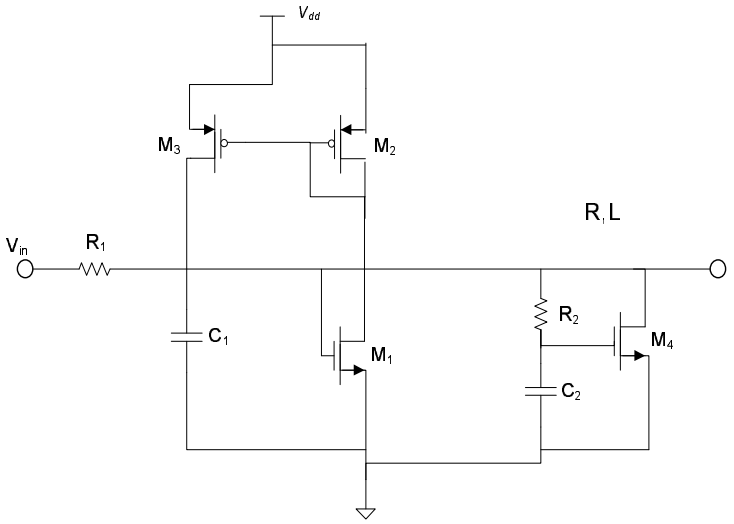

Figure A.5: Excitable neuron model.

R_1	10 M
C_1	100 p
M_1	$18\mu/1.2\mu$
M_2	$15\mu/2.4\mu$
M_3	$15\mu/2.4\mu$
R_2	1 M
C_2	100p
M_4	$12\mu/0.6\mu$
C_2	500f

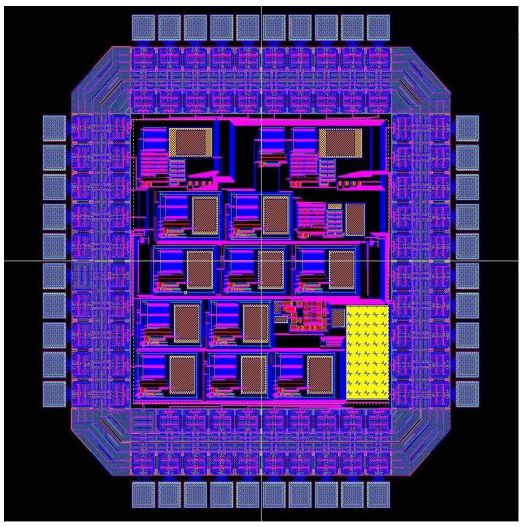

Figure A.6: Layout of a single channel of current clamp, two-electrode voltage clamp and single-electrode voltage clamp on a MOSIS tiny chip using AMI 0.5 μm process.