ABSTRACT

KWAK, BYUNG-IL. Formation of Stacked SiGe Nano-Bridges. (Under the direction of Dr. Mehmet C.Öztürk.)

We have successfully demonstrated a novel method to form a three-dimensional array of Si or $Si_{1-x}Ge_x$ nanowires that are horizontally aligned to the Si substrate. Unlike previous attempts, the nanowires of desired diameters and lengths can be readily formed at desired locations on a standard Si substrate. The process has been accomplished by epitaxial growth of Si and $Si_{1-x}Ge_x$ layers, conventional lithography, reactive ion etching and selective etching of Si with respect to $Si_{1-x}Ge_x$. Therefore sensors and thermoelectric devices of nanowires can be readily integrated on Si chips, and nanowires themselves can serve as the channels of MOSFETs allowing three dimensional integration of MOSFETs for increased current drive. Among the four steps of the whole process, the thesis focuses on selective etching Si over $Si_{1-x}Ge_x$. TMAH, which is an anisotropic etchant and does not contain any alkali metals, was adopted for selective etching. It has been shown that the Si vertical etch rate is at least 300 times faster than the etch rate of $Si_{1-x}Ge_x$ at 73 °C. For lateral selective etching, it turned out to be crucial to align the patterns along a certain direction. When the patterns are aligned to $\langle 110 \rangle$ direction, exposed $\{111\}$ planes have the lowest etch rate and the etching proceeds only until two $\{111\}$ planes meet at the center of a Si layer sandwiched between the top and bottom $Si_{1-x}Ge_x$ layers. After this, etching continues very slowly. On the other hand, if the patterns are aligned to $\langle 100 \rangle$, $\{110\}$ planes

are exposed but etched faster than {100} planes: the desired etch rate and the selectivity to $Si_{1-x}Ge_x$ nanowires can be obtained.

Formation of Stacked SiGe Nano-Bridges

by

BYUNG-IL KWAK

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Dedication

To my family

Biography

Byung-il kwak was born on April 20th, 1973 in Seoul, Korea. He received his B.S. and M.S. degrees in ceramic engineering from Yonsei University in Seoul, Korea in 1998 and 2000, respectively. After graduation, he joined Hynix Semiconductor Inc. where he worked for 6 years as a transistor designer. He plans to continue his graduate study after receiving his M.S. degree in Electrical Engineering.

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My research was made enjoyable by many past and present graduate students. I enjoyed many interesting conversations with Yan Du, Emre Alptekin, Bongmook Lee, and Steven Novak.

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Chapter 1

Introduction

1.1 Motivation

During more than three decades, the progress of information technology has relied on the dimensional down-scaling of the silicon-based Complementary Metal Oxide Semiconductor (CMOS) technology. Gordon Moore, who is one of the co-founders of Intel, observed in 1965 that the number of transistors in a chip doubled every two years [3], which is now referred to as "Moore's law". After three decades, Moore said that "no exponential is forever but 'forever' can be delayed!" [4]. This statement describes many challenges that the semiconductor industry will face when the feature size approaches the physical limit. To sustain the historical scaling trend, the International Technology Roadmap for Semiconductors(ITRS) has explicitly proposed one-dimensional nanostructures such as carbon nanotubes (CNT) and semiconductor nanowires (NW) as potential successors [5] to Si based CMOS. Semiconductor nanowires can offer a surrounding gate geometry which is a highly desirable device structure for further down-

scaling and electrostatic control. Multi-gate structures such as FinFET [6] and tri-gate transistor [7] offer improved control over the channel, and nearly ideal sub-threshold slope. Silicon MOSFETs with wrap-around gates with gate lengths of 5 nm have already been realized [8]. The nanowire-based field-effect transistors can also be used as ultra-sensitive sensors which detect gases, chemicals, and biological species such as DNA, proteins, and viral particles [9–11]. When the dimensions approach the nanometer scale, the surface-to-volume ratio increases making the surface more influential in determining the properties of the nanowire. For example, the thermal conductivity becomes extremely size-dependent at the nanometer scale, which happens to be one of key drivers for this study. It has been shown that the phonon transfer is greatly impeded in thin, one-dimensional nanostructures as a result of increased boundary scattering and reduced phonon group velocity stemming from phonon confinement. This phenomenon becomes important when the nanowire diameter is close to the mean free path of phonons in the material [12].

Nanowires can also provide the path to fabricating fully depleted MOSFETs as well as sensors based on electrostatic switching. Due to the small volume of the nanowires, the charges that attach to the nanowires can easily deplete or accumulate the 'bulk' of the nanowires [9].

1.2 Nanowire Fabrication Techniques

The early work focused on techniques that resulted in nanowires that grew vertically on the substrate plane. A major disadvantage of vertical nanowires is the difficulty of forming reliable, low-resistivity contacts to them. Often, the nanowires are broken off the substrate and flown in a solution with the hope that they will land on suitable planar contact pads. The alternative approach is to form wrap-around contacts, which is quite a challenging task. Recently, a new technique was developed to grow horizontal nanowires between two vertical walls with some success [13]. One of the major goals of the present work was to develop a process that would enable fabrication of horizontal nanowires using a process compatible with Si manufacturing.

1.2.1 Vertical Nanowires

Since the early 1990's, much research on nanowire synthesis has been performed resulting in a wide spectrum of methods including vapor-liquid-solid (VLS) [14–20], surface diffusion and epitaxy [21,22], oxide-assisted growth (OAG) [23], solution-based growth [24, 25], and template-directed assembly [26–29]. In recent years, the dominant technique involves nano-dots of a metal-catalyst, which confines growth to one dimension. Depending on the phases involved in the reaction, this approach is typically referred to as the vapor-liquid-solid (VLS) [30], solution-liquid-solid (SLS) [31, 32] or vapor-solid (VS) [33] method. As shown in Figure1.1, in VLS growth, the metal nano-particles are heated above

the eutectic temperature for the metal-semiconductor system in the presence of a gaseous source of the semiconductor material, leading to a liquid droplet of the metal/semiconductor alloy. The continued supply of the semiconductor reactant into the liquid droplet supersaturates the eutectic, resulting in nucleation of the solid semiconductor. The solid-liquid interface forms the growth interface, which acts as a sink causing continued semiconductor incorporation in the lattice resulting in the growth of the nanowire with the alloy droplet always remaining on the top of the nanowire [34]. The gaseous semiconductor reactants can be produced through decomposition of precursors in a chemical vapor deposition(CVD) system, through pulsed laser ablation [14] or molecular beam epitaxy (MBE) [35] from solid targets. In the case of silicon, silane (SiH_4) and Au nanoparticles are typically used as the precursor and catalysts, respectively. In addition to the nanowires of the group IV materials (i.e. Si, Ge, SiGe and C), nanowires of III-V and II-VI compounds were also produced using the VLS method. For such materials, metal-organic chemical vapor deposition (MOCVD) [36], or pulsed laser ablation [37] are typically used to provide the reactants.

These nanowires were used in a variety of device applications. Examples include, nanometer-scale field-effect transistors [38, 39], p-n diodes [10], light-emitting diodes (LEDs) [10], bipolar junction transistors [10], complementary inverters [10], and nanoscale lasers [40].

Compared to vapor-solid growth [33] and solution-liquid-solid (SLS) [31, 32], the VLS method provides axial and radial heterostructures. The term "axial het-

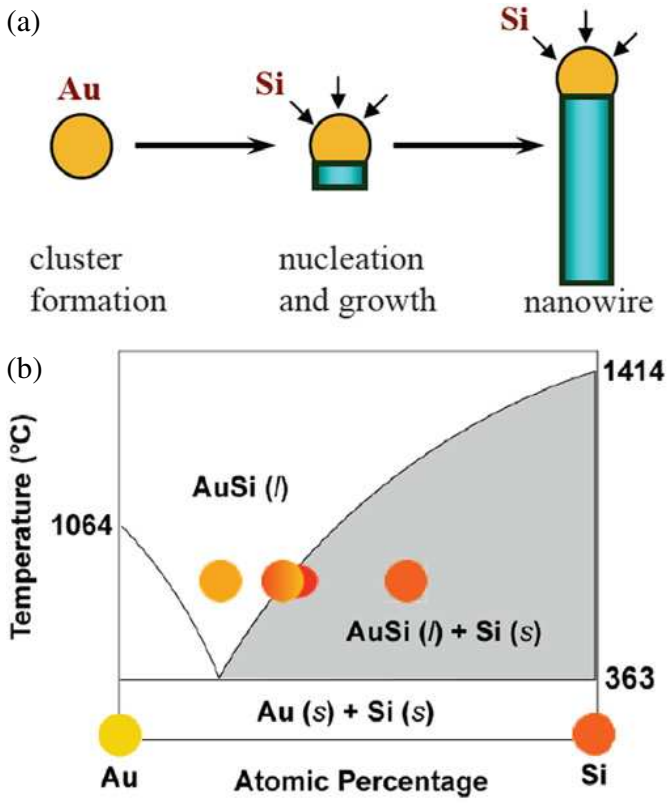

Figure 1.1: Si nanowires grown by the VLS technique: (a) A liquid alloy droplet AuSi is formed above the eutectic temperature (363°C) from Au and Si. The continued supply of Si from the vapor phase into the liquid causes supersaturation of the liquid, resulting in nucleation and directional growth. (b) Binary phase diagram for Au and Si illustrating the thermodynamics of VLS growth [34].

erostructure" implies that sections of different materials with the same diameter are grown along the same axis, while "radial heterostructure" refers to concentric shells of different materials. If the vapor decomposition/adsorption continues exclusively at the surface of the catalyst nano-cluster site, crystalline growth of the new semiconductor will continue along the axial direction (Figure 1.2(c)). On the other hand, if the decomposition of the new vapour/reactant on the surface of the semiconductor nanowire cannot be neglected, a shell of the material will grow on the original nanowire surface (Figure 1.2(d)). Repeated modulation of the reactants in a regime favoring axial growth leads to the formation of a nanowire superlattice, as shown in Figure 1.2(e), while changing reactants in a radial-growth regime will result in core-multi-shell radial structures, as shown in Figure 1.2(f). These methods were used to form p-n junctions [41] and heterostructures of Si-Ge [42], [18] and InAs-InP [43].

Devices based on the nanowires formed using the techniques discussed above are still in an embryonic stage from an industrial point of view. First of all, to use the nanowires on complex integrated circuits precise positioning techniques will be needed, which is certainly not a practical approach compared to planar processing used to fabricate billions of transistors simultaneously. For applications that do not require such high level integration (e.g. sensors) some progress in manipulating the nanowires has been achieved including techniques such as electric field-directed assembly [45], fluidic-flow-directed assembly [40], Langmuir-Blodgett [46], and patterned chemical aseembly [40, 46].

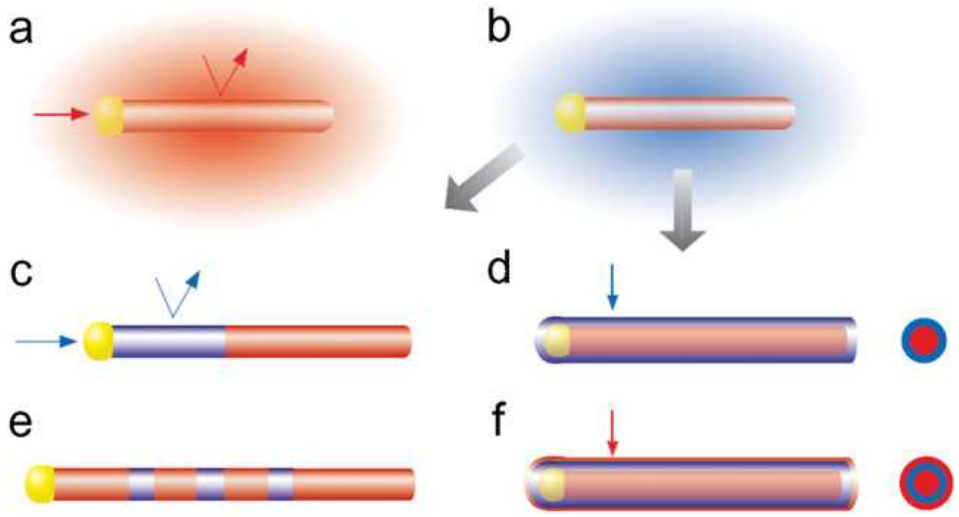

Figure 1.2: Formation of nanowire shaped heterostructures (a) Preferential reactant incorporation at the catalyst (growth end) leads to 1D axial growth. (b) Changing the reactant may lead to either (c) axial or (d) radial growth depending on how the reactant is incorporated. In (c) the catalyst is the sink. In (d) the growth is uniform on the surface. Alternating the reactants may be used to produce (e) axial superlattices or (f) core-multi-shell structures [44]

Another challenge of this approach in Si processing is that gold, which functions successfully as a catalyst for many materials systems including Si, Ge, SiGe, InAs, and InP creates deep level traps in the silicon bandgap. Therefore, a compatible catalyst or catalyst-free growth method must be developed [47].

A key disadvantage of these nanowires is the quality of their contacts. In many cases, connection of the nanowires to their electrodes requires fairly complex process steps. As mentioned above, vertical nanowires are typically detached from their substrates and then flown in a liquid solution for assembly. Metal electrodes may then be deposited onto the nanowires to secure them on the desired locations and achieve electrical connection to the nanowires. Clearly, this technique offers little flexibility in cleaning the nanowire surface prior to the contact formation.

On Si nanowires, it is virtually impossible to avoid formation of the thin native oxide. Hence, the charge carriers must tunnel through this oxide, which inevitably leads to a poor contact resistance most likely wiping out the advantages of the nanowires. For MOSFETs, It is very difficult to fabricate a surrounding gate structure using this approach [48].

It is important to note that the above mentioned methods do not employ lithographic techniques to determine the nanowire dimensions. This is partly because nanolithography was simply not available when the work on nanowires began as shown in Figure 1.3 [1].

Additionally, ability to grow many nanowires without the need for lithography was apparently attractive. Nevertheless, these nanowires are in general not suitable for electronic applications. As discussed above the key disadvantage is the fact that contacts must be formed at both ends of the nanowires and in the case of MOSFETs, the wrap-around gates must be formed around vertical nanowires, which happens to be just as challenging.

1.2.2 Horizontal Nanowires

Recently, researchers at Hewlett-Packard proposed a new technique to address the positioning and contact formation challenges of the Si nanowires. They have developed a technique that enabled nanowire growth on vertical sidewalls resulting in horizontal nano-bridges hanging between two facing Si walls [13]. The

[1] In the early 1990's the minimum lithographic dimension was approximately 500 nm obtained using i-line steppers.

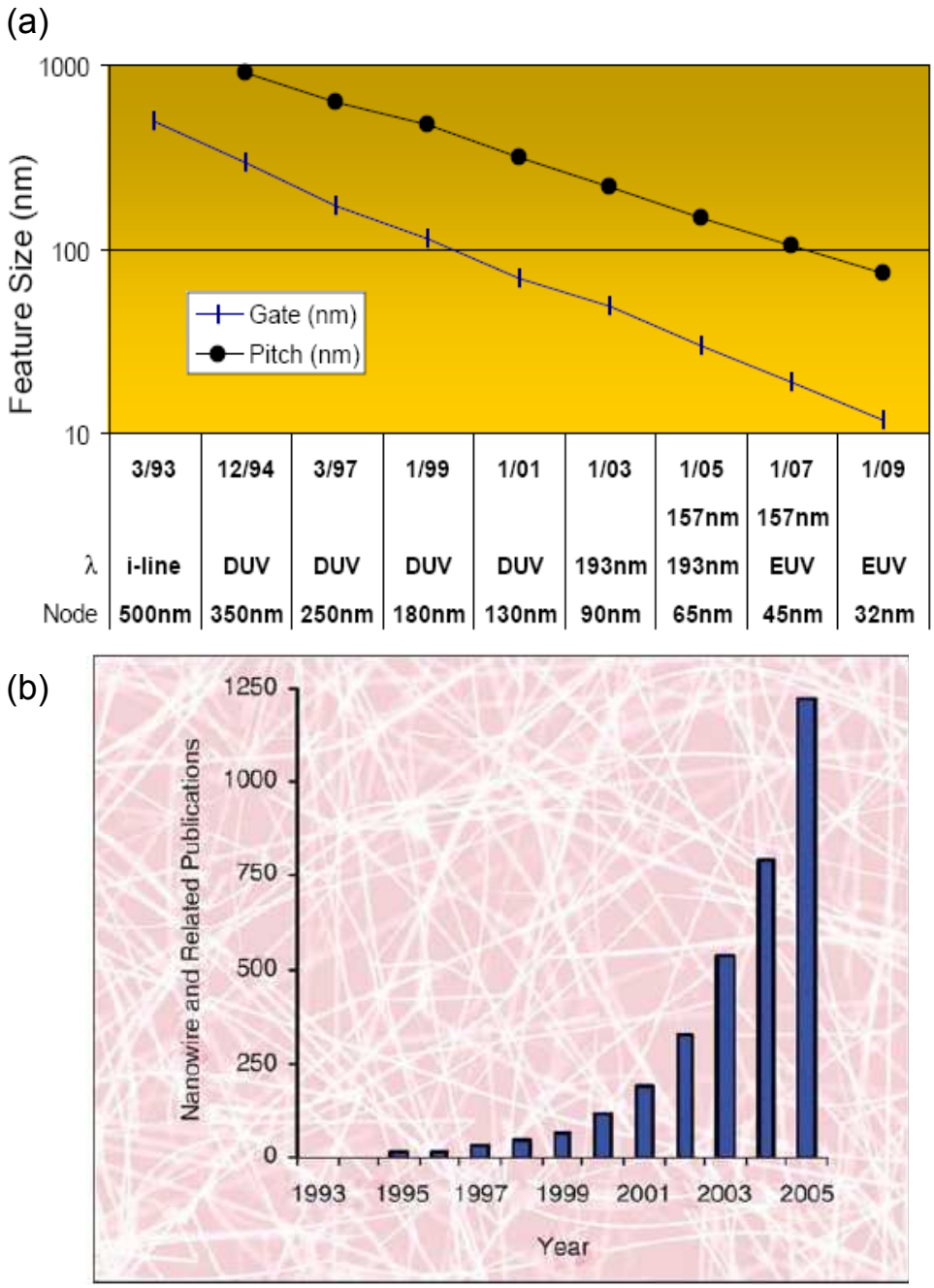

Figure 1.3: (a)Intel Lithography Roadmap [1],(b)Plot illustrating the number of published papers relating to nanowires each year since the early 1990s [2]

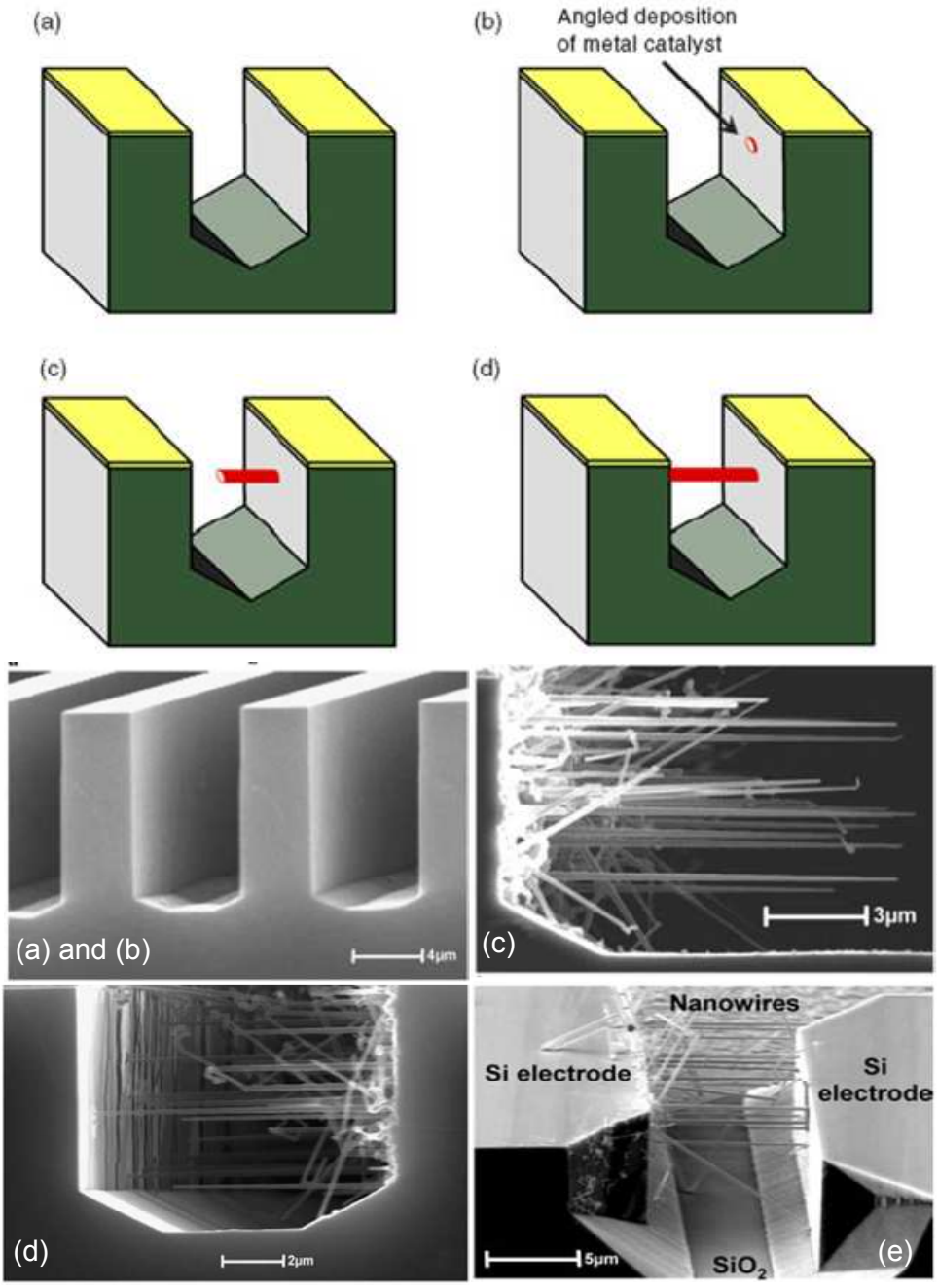

Figure 1.4: Schematic diagrams of nanobridge proposed by Saif Islam [13] (a) trench formation, (b) catalyst deposition, (c) lateral nanowire growth, (d) bridge across trench.

cartoon and the scanning electron microscope (SEM) images illustrating this idea is shown in Figure 1.4. In this approach, to obtain a dense array of nanowires between two vertical Si planes, the nanowires are grown from one electrode toward the facing electrode. This approach relies on the fact that Si nanowires grow perpendicular to the (111) planes [49, 50]. In order to obtain vertical (111) planes facing each other, (110)-oriented Si wafers were chemically etched in a solution that provided anisotropic etching. After forming the vertical Si walls, a thin catalyst layer is deposited on the walls and then annealed to form isolated nano-particles of the catalyst material. The structure is then exposed to a silicon-containing precursor gas in a chemical vapor deposition reactor. The decomposition of the gas is slow on bare silicon surfaces, but is greatly accelerated on the surface of a catalyst nano-particle. The size of the nano-particles depends on the thickness of deposited catalyst layer and subsequent annealing. After this point, the growth is essentially governed by the VLS mechanism. The nanowires grow across the trench toward the (111)- oriented side wall of the opposing electrode. When the nanowire reaches the opposite sidewall, it is attached to it by decomposition of the catalyst material. The connection is found to be mechanically strong. Compared to the previous 'pick and place'[2] method, the new method has many advantages including

[2]i.e. after forming the nanowires, they are picked and placed in desired positions for device fabrication.

- The nanowires are confined between the electrodes.
- The contact resistivity will improve because a tunneling barrier does not exist between the nanowires and the contact.
- 3-D integration provides a high nanowire density.

A disadvantage of this technique is that relatively expensive SOI (Silicon on Insulator) wafers are needed for electrical isolation between the two electrodes unless a very deep pn-junction is formed. Another disadvantage is that, majority of the nanowires grow in random directions, which makes it very difficult to fabricate transistors around them. Finally, some nanowires grow on the top surfaces of the electrodes. To overcome this problem, gold was evaporated at an angle smaller than 45° such that the catalyst layer deposited on the top surface is too thin for nanowire nucleation. Unfortunately, this approach also resulted in thinner catalyst deposition on the vertical sidewalls, which reduced the nanowire density.

While the approach proposed by the HP group is an improvement over the conventional method, it has its own disadvantages. Furthermore, it does seem likely that the method is suitable for forming transistors or any device that relies on nanowires of a single diameter and orientation.

1.3 NCSU Method

With the aforementioned disadvantages of the HP process in mind, we have proposed a novel process to form three dimensional stacks of Si or $Si_{1-x}Ge_x$ nanowires. While this report is focused on $Si_{1-x}Ge_x$ nanowires, Si nanowires can be formed using the same procedure. The reason behind this focus is twofold. First, there are established recipes for selective etching of $Si_{1-x}Ge_x$. In fact, the standard SC-1 clean used in Si processing is commonly used to etch $Si_{1-x}Ge_x$. On the other hand, there is far less information on selective Si etching. More importantly, $Si_{1-x}Ge_x$ nanowires are great candidates for future thermoelectric applications due to their reduced thermal conductivity. In fact, the thermal conductivity of bulk $Si_{1-x}Ge_x$ with 30% Ge is close to that of Si nanowires. Therefore, any further reduction in the thermal conductivity of $Si_{1-x}Ge_x$ due to phonon scattering will only make the material a better candidate for such applications.

The NCSU concept for forming the nanowires is illustrated in Figure 1.5. In this process, a $Si/Si_{1-x}Ge_x$ superlattice is first grown by an epitaxial process. A thin layer of oxide is deposited by low-pressure chemical vapor deposition followed by conventional lithography used to define the nanowires in a thin photoresist layer. Using the photoresist as a mask, reactive ion etching is first used to etch the oxide to create a hard mask and then anisotropically etch the superlattice down to the silicon substrate creating parallel vertical walls. Si or $Si_{1-x}Ge_x$ is then selectively etched to form the nanowires. In this work, we have focused on chemical etching methods, however, a suitable plasma etching process may also

be developed in the future.

Considering the fact that Si MOSFETs with gate lengths as small as 45 nm are under production and 22 nm MOSFETs are already being developed, it makes sense to rely on lithographic techniques to define the nanowires. Using this method, nanowires can be formed wherever we desire them to be. We can also fabricate nanowires of different lengths and widths if we need to.

The method described above has the potential to increase the nanowire density substantially over what can be possible with the HP method. Because the epitaxial layers can be in-situ doped, pn- junction isolation can be easily implemented simplifying the isolation scheme. It is also compatible with industrial silicon electronics, and thus could be readily implemented in silicon integrated circuits. Given the fact that selectively grown $Si_{1-x}Ge_x$ layers are used in state of the art CMOS integrated circuits, nanowires can be integrated to standard chips with minimal effort.

In the next Chapter, we describe the method used to grow epitaxial layers of Si and $Si_{1-x}Ge_x$. Chapter 3 includes selective etching of Si against $Si_{1-x}Ge_x$ with varying etch conditions, which constituted the bulk of the work carried out in this research program.

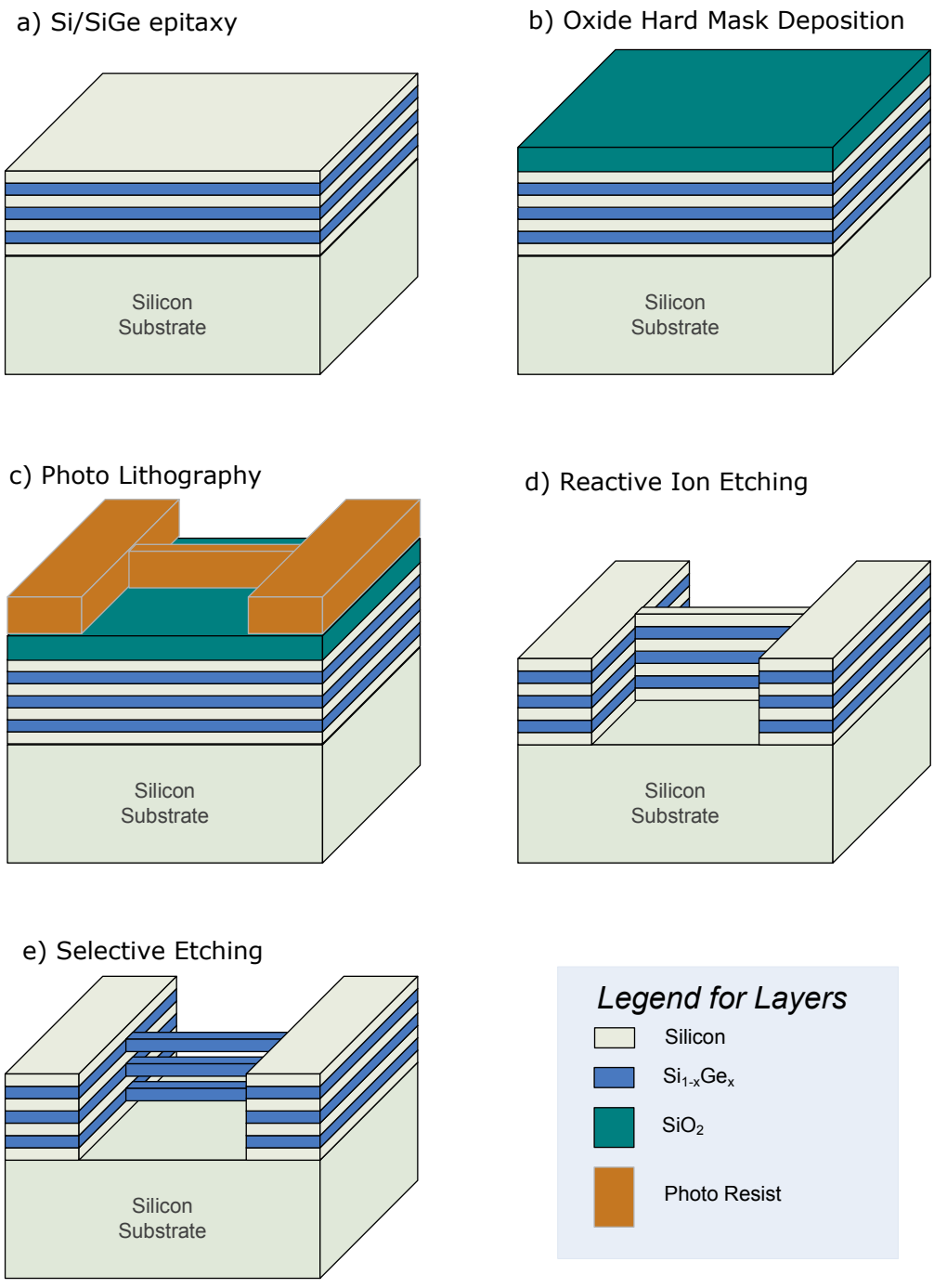

Figure 1.5: Proposed process flow for nanowire fabrication

Chapter 2

Si and $Si_{1-x}Ge_x$ Epitaxy

Epitaxial Si and SiGe films used in this study were grown by ultrahigh vacuum rapid thermal chemical vapor deposition (UHV-RTCVD) [51,52]. In this chapter, basic principles of this growth technique are discussed and the tool used to grow the epitaxial layers is described in detail.

2.1 UHV−RTCVD System

UHV-RTCVD combines the advantages of RTCVD [53] with the clean growth environment of a UHV reactor [54]. A schematic diagram of the reactor is shown in Figure 2.1. The system consists of three chambers a) sample entry chamber or load-lock; b) intermediate chamber(IC); and c) main process chamber(MPC). The sample entry chamber is pumped by a molecular drag pump backed by a diaphragm pump. The base pressure of this chamber is about 10^{-5} torr. The intermediate chamber serves as a vacuum buffer between the load-lock and the main process chamber to minimize the contamination of the process chamber

during wafer transfer. It is pumped by a cryopump down to a base pressure of 10^{-9} torr. The main process chamber is pumped by a cryopump and a hybrid turbomolecular - molecular drag pump. This pump is backed up by a dry (oil-free) mechanical pump. All pumps and gate valves on the system are oil-free to minimize the hydrocarbon contamination. The MPC is a water-cooled stainless steel chamber with double wall construction. A quartz bell jar sits on top of the MPC sealed by two differentially pumped O-rings. A molecular drag pump is used to pump between the o-rings.

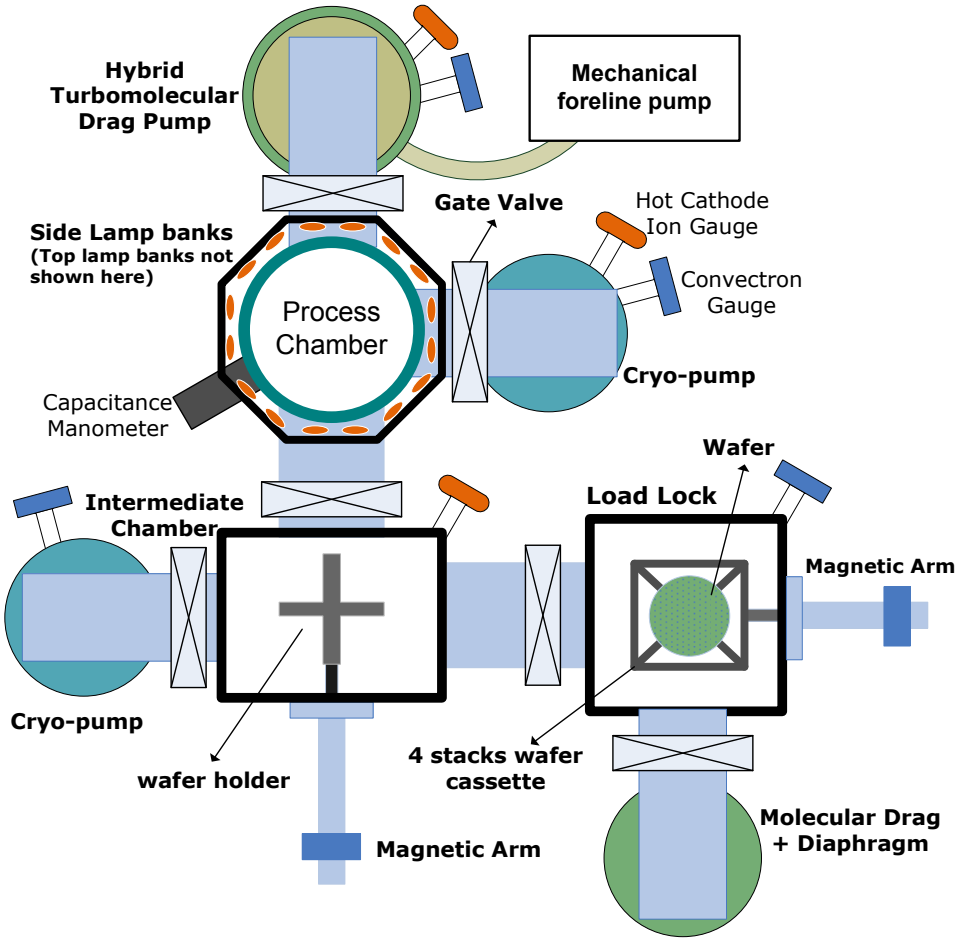

Figure 2.1: Top view of the UHV-RTCVD system

A schematic diagram of the MPC is shown in Figure 2.2. After a wafer is tranferred into the main process chamber, it is placed on a rotatable quartz wafer holder and then raised to the desired height. During epitaxy, the wafer is heated by the two tungsten halogen lamp banks. The top lamp bank consists of eight 2 kW tungsten halogen lamps. A gold-plated reflector is used behind the lamps to focus the infrared radiation from the lamps onto the wafer to achieve a uniform temperature; The second lamp bank consists of sixteen 1 kW lamps around the bell jar featuring a water-cooled aluminum reflector. This lamp bank compensates the heat loss from the edges of wafer The wafer edge provides additional surface area for heat-loss via radiation. Consequently, without additional heating focused on the wafer edge, the temperature of the wafer decreases as we move away from the wafer center. The improved thermal uniformity through this configuration provides a relatively uniform growth rate over a six inch wafer [55]. The wafer temperature is monitored by two optical pyrometers(λ=4.9μm) monitoring the temperature on the wafer backside at two different locations. One of the pyrometers measures the temperature at the wafer center. The signal from this pyrometer is used in a closed loop feedback control system to control the wafer temperature.

The gases used in this work include Si_2H_6, GeH_4(10% diluted in H_2), B_2H_6(3% diluted in H_2). All gases used were UHP grade[1] as defined by the gas supplier Voltaix Inc. The gas purity of process gases is an important factor in growing high

[1]The concentration level of H_2O, which is a major species detrimental to epitaxy, is 1ppm.

quality epitaxial layers. In fact, the contamination introduced into the growth ambient by the process gasses is much more than the background pressure. For example, if the total growth pressure is 100 mtorr and the gas purity is 1 ppm, this corresponds to a contaminant level of 10^{-7} torr. This means that there is not much gained by the UHV ambient during growth - the contamination introduced by the process gasses is two orders of magnitude higher[2].

[2]In comparison, the batch UHV-CVD process developed at IBM uses 1 mtorr of total pressure to grow Si [54], thus enabling the use of 10 ppm pure process gases.

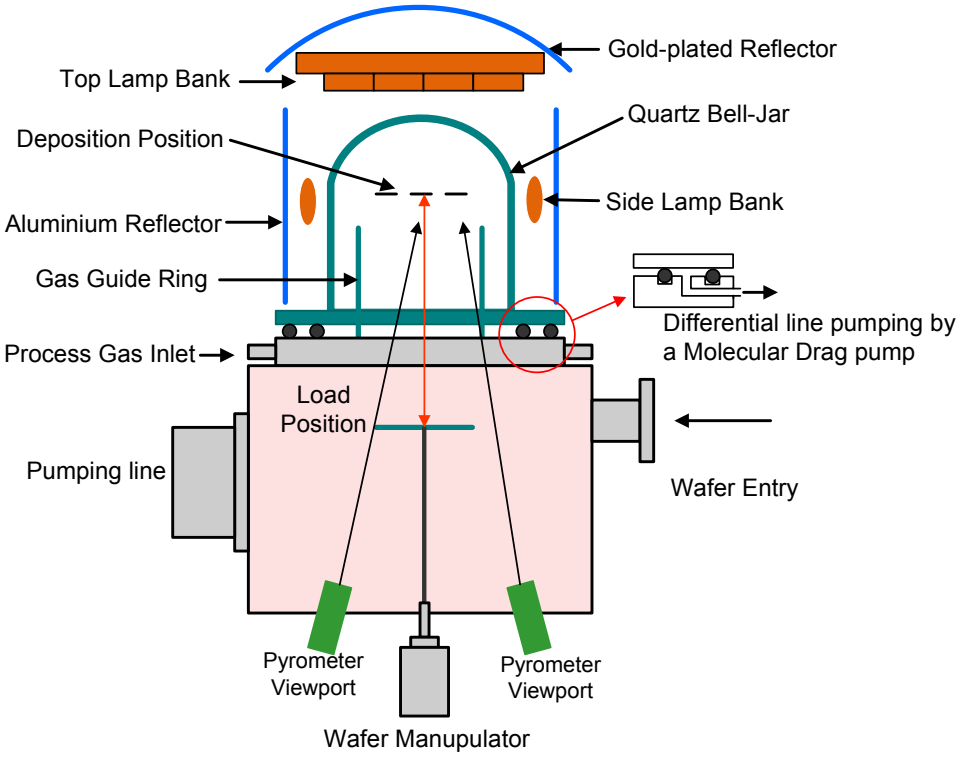

Figure 2.2: The main process chamber of the UHV-RTCVD system

2.2 Surface Preparation Prior to Epitaxy

For epitaxial growth, cleaning the growth surface prior to epitaxy is an important step because any defects that nucleate during the first few epitaxial layers determine the quality of the rest of the epitaxial layer. A key challenge is to remove the native oxide on Si prior to epitaxy.

The surface preparation method used in this study is based on obtaining a hydrogen passivated surface by an ex-situ clean [56]. The ex-situ clean consists of a standard SC1(NH_4OH + H_2O_2 + $5H_2O$) clean of organic contaminants removal and SC2(HCl + H_2O_2 + $5H_2O$) to remove metallic particles. Both processes were performed at 75 °C and they were followed by a 30 second dip in a 1% HF solution. The HF dip removes the chemical oxide grown during the RCA clean and passivates the dangling bonds on the Si surface with hydrogen. After the HF dip, the wafer is dried with N_2 and immediately loaded into the load-lock chamber. It typically takes about 10 minutes for the load-lock to reach a pressure of 10^{-5} torr. This passivation is reasonably stable at room temperature and allows sufficient time for wafer loading [56]. Once the wafer is hydrogen terminated, it can be transferred into the growth chamber and growth may be commenced immediately without a high-temperature preclean step. The hydride layer desorbs at about 400°C. This type of process is then preferred primarily for low-temperature processes such as MBE and low thermal budget epitaxy. Details of the process can be found in earlier work by two former NCSU graduate students, Mahesh Sanganeria and Muhsin Celik who worked on surface preparation

for UHV-RTCVD as part of their doctoral dissertations [57, 58].

Then the wafer cassette, which holds four wafers, is transferred into the IC. After reaching approximately 10^{-8} torr in this chamber, one of the wafers from the cassette is transferred into the MPC. After reaching the base pressure in MPC, pumping is switched to the hybrid turbomolecular drag pump for growth. The wafer is then ramped to the epitaxial growth temperature, and the gas flows are started. At the end of the growth cycle, both the lamp and the gas flows are turned off simultaneously. A typical deposition cycle is illustrated in Figure2.3.

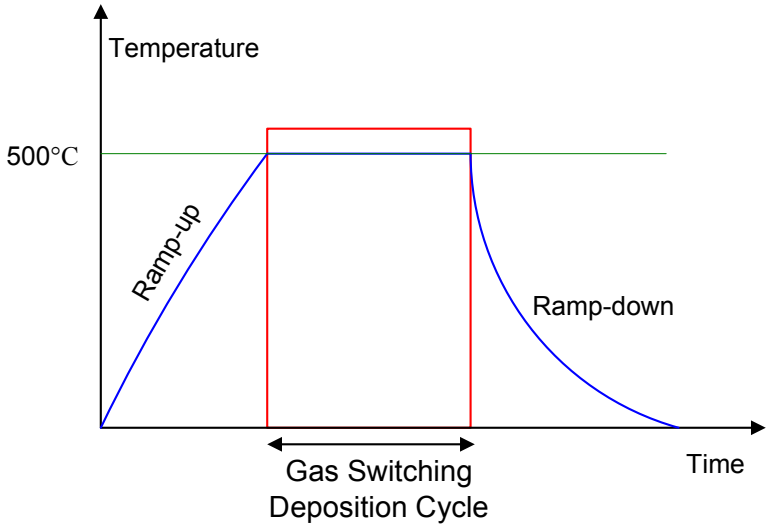

Figure 2.3: A typical deposition sequence used in $Si_{1-x}Ge_x$ and Si epitaxy

Chapter 3

Nanowire Formation

In this chapter, the details of the process flow used to fabricate the $Si_{1-x}Ge_x$ nanowires is presented. Experiments were performed to optimize the process flow. Fundamental work was carried out to develop a novel method to selectively etch the remaining Si between the $Si_{1-x}Ge_x$ nanowires.

3.1 Epitaxy of Si/SiGe superlattices

The Si/SiGe superlattices were grown by UHV−RTCVD following the procedure described in chapter 2. The maximum number of Si/SiGe pairs used in this study was five, and the conditions are provided in Table 3.1. It can be seen that while the $Si_{1-x}Ge_x$ layers are grown at 500-550 °C, the Si layers were grown at 800°C. A slightly thicker, silicon buffer layer is grown on top of the superlattice to protect the underlying superlattice during reactive ion etching.

Table 3.1: Typical process conditions for Si and $Si_{1-x}Ge_x$ epitaxy used in this work

Germanium Content	Si		Ge = 50%		Ge = 28%		Ge = 17%	
Doping [cm^{-3}]	None	10^{21}	None	10^{21}	None	10^{21}	None	10^{21}
Temperature [°C]	800		500		550		550	
Pressure [mtorr]	51	64	320	382	182	235	121	168
Si_2H_6[sccm]	10		10		15		25	
10% GeH_4 in H_2[sccm]	0		750		450		300	
3% B_2H_6 in H_2[sccm]	0	100	0	100	0	100	0	100
Growth Rate [nm/min]	80		35		40		25	

3.2 Photolithography

In photolithography, the wavelength of the light determines the ultimate resolution that can be achieved. Therefore, in order to resolve structures with dimensions on the order of 100 nm, a light source with a very short wavelength is needed. In this work, an ASML 5500/950B scanner, which employs a 193 nm ArF Excimer laser was used to form the nanowires. In addition to this short wavelength, a relatively thin, 300 nm thick photoresist layer with a 80 nm thick Bottom antireflectcive Coating(BARC) was used. It is important to note that the BARC should be able to tolerate the resist developer to avoid undercutting of the resist patterns. Therefore, after exposure and development, the BARC is patterned by dry-etching in oxygen. Table 3.2 lists the key steps followed for defining the nanowires by lithography.

Table 3.2: Process Module for the photolithography step using the ASML scanner

Step	Conditions	Description
Spin BARC	30 sec at 3000 rpm	80 nm of BARC(AR23-820)
Soft Bake	90 sec at 210°C	
Spin Photoresist	30 sec at 3000 rpm	Epic V41-0.28, 300 nm
Soft Bake	60 sec at 115°C	remove the solvent
Expose	Dose= 18 mJ/cm^2, Focus= 0.3	Energy Dose and focus determined from an energy-focus matrix calibration sample
Hard Bake	60 sec at 115°C	
Develop	193 nm developer for 30 sec	

3.3 Reactive Ion Etching

After photo patterning followed by the hard mask deposition, reactive ion etching was performed for the final pattern transfer. In this work, the materials to be etched are BARC, oxide, and the Si/SiGe superlattice. Etching of the BARC and the oxide was performed in O_2 and CHF_3/O_2 plasmas in 'Semigroup RIE TP1000' which is a parallel plate etcher operating at the frequency of 13.56 MHz. To ensure a highly anisotropic profile for $Si/Si_{1-x}Ge_x$ etching, Cl_2 was used in the 'Plasma Therm SLR720' etcher.

3.3.1 Hard Mask

Because the photoresist(VR-41) used in this process is too thin to serve as a protective layer during RIE of $Si/Si_{1-x}Ge_x$[1], deposited oxide(LTO) or nitride

[1]As in Cl_2 etch recipe given in Table 3.6, VR-41 and silicon have the etch rates of 42 and 53 nm/min, respectively. Thus, VR-41 can not be used as an etching barrier when etching silicon

were used as the hard mask. The required thickness for the hard mask depends on how thick the Si/SiGe superlattice is. For five pairs of Si/SiGe, the thickness of the superlattice is 900 nm which is the thickest layer etched in this work. This required an oxide thickness of at least 45nm because the etch selectivity of silicon over oxide is about 20:1 in the 'Plasma Therm SLR720' etcher, however, considering 'within wafer' and 'wafer to wafer' thickness variations, the oxide was overetched to ensure complete removal.

Table 3.3: Etch Rates for materials used in the recipe given in Table 3.6

Materials	Etch Rate [nm/min]
VR-41	46
SiO_2	2.6
Si	53

3.3.2 Selection of the RIE Chemistries

For any etching to take place, the chemical bonds need to be broken. Therefore, the bond energies can be used as a guide for choosing the etchant gases(Table 3.4). For example, reactions that lead to bonds stronger than the Si−Si bond will etch silicon; and if the products have stronger bonds than the Si−O bond, silicon dioxide will be etched. Thus, for Si etching, both F and Cl based etchants can be used while for oxide etching only the F-based etchants will work.

which is much thicker than VR-41.

Oxide Etching

Any fluorine containing gas can be used as an etchant for oxide. Examples include CF_4 or SF_6. However, since both gasses etch silicon as well, and they are suitable for non-selective etching only. Since Si or $Si_{1-x}Ge_x$ layers should be protected, CHF_3 was used to etch the oxide. It provides fluorine and carbon for etching (SiF_4, CO_2 etch products), and CF_2^* radicals, which are polymer precursors. Polymerization takes place on the silicon surface. On the oxide surface polymerization can not take place due to the oxygen supply: ion bombardment-induced reactions on the oxide result in CO_2 formation.

Silicon Etching

Fluorine, chlorine and bromine based etchants (e.g. Cl_2 and HBr) can be used for silicon etching. Fluorine based chemistries are generally safer, however, they are seldom fully anisotropic. Chlorine based processes result in vertical sidewalls, and the same is true for bromine based processes. Unfortunately, both gasses

Table 3.4: Bonding Energies of various compounds

Bonds	Bonding Energy [kJ/mol]
C−O	1080
Si−O	470
Si−Si	227
Si−N	437
Si−F	550
Si−Cl	403
Si−Br	307

are highly toxic. Hence, the equipment for Cl_2 or HBr etching must be equipped with a load-lock. The recipes used in this work are tabulated in Table 3.5 and Table 3.6.

Table 3.5: Etching conditions for BARC and LTO in the Semigroup RIE TP1000 etcher.

conditions	step1(BARC)	step2(LTO)
CHF_3[sccm]	0	100
O_2[sccm]	5	0.5
Power[W]	90.72	100.8
Pressure[mtorr]	60	60
time[min]	1.25	5.5

Table 3.6: Etching conditions for anisotropic RIE of $Si/Si_{1-x}Ge_x$ in the Plasma Therm SLR720 etcher.

conditions	step1	step2
Cl_2[sccm]	20	20
O_2[sccm]	0	0.6
Power[W]	100	100
Pressure[mtorr]	15	15
time[min]	0.5	variable

3.4 Selective Chemical Etching of Si

The final step in forming the nanowire array is selective etching of silicon over $Si_{1-x}Ge_x$. This etching should be isotropic such that the etchant can penetrate through the exposed Si sidewalls. While it might be possible to find a plasma chemistry which can isotropically etch Si but not SiGe, in this study, we have

preferred to focus on wet etching because of its relative simplicity, promise for selectivity and reduced cost.

A wet silicon etch can be isotropic or anisotropic [59]. Isotropic etchants etch in all directions at the same rate whereas anisotropic etchants etch much faster in one direction than others [60]. A popular isotropic Si etchant referred to as HNA combines hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH) [59]. Anisotropic etchants shape or 'machine' desired structures in crystalline silicon and are more powerful but they typically need etching temperatures higher than the room temperature (typically 80 - 90°C). Anisotropic silicon etchants are extensively used in the field of Micro-Electro-Mechanical Systems (MEMS). Other anisotropic silicon etchants include EDP (ethylene diamine, pyrocatechol and water), KOH (potassium hydroxide) and TMAH (tetramethylammonium hydroxide). Important properties of these etchants are listed in Table 3.7 [60–63]. Every etchant has its advantages and disadvantages. Especially the well known KOH is not fully CMOS compatible because it contains alkali ions (potassium), which can introduce mobile charge into the MOS gates of transistors and cause threshold voltage shifts [59]. Furthermore, it corrodes aluminum and its selectivity with respect to silicon dioxide is poor. EDP is more attractive than KOH because it does not contain the mobile potassium ions and has a high selectivity with respect to dielectrics. This etchant however is not selective to aluminum and it has a serious drawback: it is toxic and mutagenic [59], hence it is very difficult to handle. Of the available etchants, TMAH stands out be-

cause it is relatively inexpensive, it is safe, and it is already used in IC processing as a positive resist developer [61]. Most importantly it has some selectivity to aluminum [59].

Table 3.7: Comparison of the general features of various anisotropic etchants

	EDP	KOH	TMAH
Si etch rate† [μm/min]	0.75 - 1.25	1 - 2	≈ 1
SiO_2 etch rate [nm/min]	1 - 80	1 - 10	0.05 - 0.025
Si_3N_4 etch rate [nm/min]	0.1	very low	0.05 - 0.25
(100)/(111) etch ratio	35	400	10 - 35
Si roughness	low	very low	moderate
Al selectivity	no	no	yes
Au selectivity	yes	yes	yes
P^{++} etch stop [cm^{-3}]	B>7×10^{19} $\rightarrow$ ER/50	B>1×10^{20} $\rightarrow$ ER/20	B>2×10^{20} $\rightarrow$ ER/40
Alkaline ions	no	yes	no
Cost	high	low	moderate
Disposal	easy	difficult	moderate
Safety	low	moderate	high

† measured on the (100).

The $Si_{1-x}Ge_x$ etch rate can be further reduced by implantation of carbon [64], nitrogen [65], and boron [63]. Implantation is probably not a preferred process for the nanowires, however, in-situ boron doped $Si_{1-x}Ge_x$ layers might be useful. The highly boron-doped $Si_{1-x}Ge_x$ is indeed used as an etch-stop in SOI wafer fabrication.

While TMAH etching of Si has been studied before, the previous work was geared toward developing a vertical Si etch while using SiGe as an etch stop. In

this work, our focus was on lateral Si etching to remove the sacrificial Si between the SiGe nanowires.

3.4.1 Anisotropic Etching Characteristics of Alkaline Solutions

The differences in the etch rates of different crystallographic planes can be explained by considering the location and number of covalent bonds that must be broken in order to remove the atoms from the lattice sites.

As shown in Figure 3.1 (a), to etch the (100) plane, two neighboring cells must be removed. That is, in the previous etch step, two neighboring cells were removed. In addition, it can be seen that in order to remove the cell from the crystalline lattice, two covalent bonds must be broken. These bonds lie below the etch-front plane. When considering the etch front for the (110) plane in Figure 3.1 (b), there are three etch-front atoms. In order to expose these cells, only one neighboring cell must be removed in the previous step. In order to remove any of these cells from the crystal lattice, three covalent bonds must be broken. It is important to note that two of these three bonds lie in the etch front plane, thus making them easier to break. Finally, for the (111) plane, there is only one etch-front atom. One neighboring cell must be etched in a previous step to expose the etch-front atom. In order to remove this cell, three covalent bonds must be broken. Each of these three covalent bonds lie below the etch-front plane. Interestingly, the reason why acidic media lead to isotropic etching and alkaline

media to anisotropic etching was, until recently, not addressed.

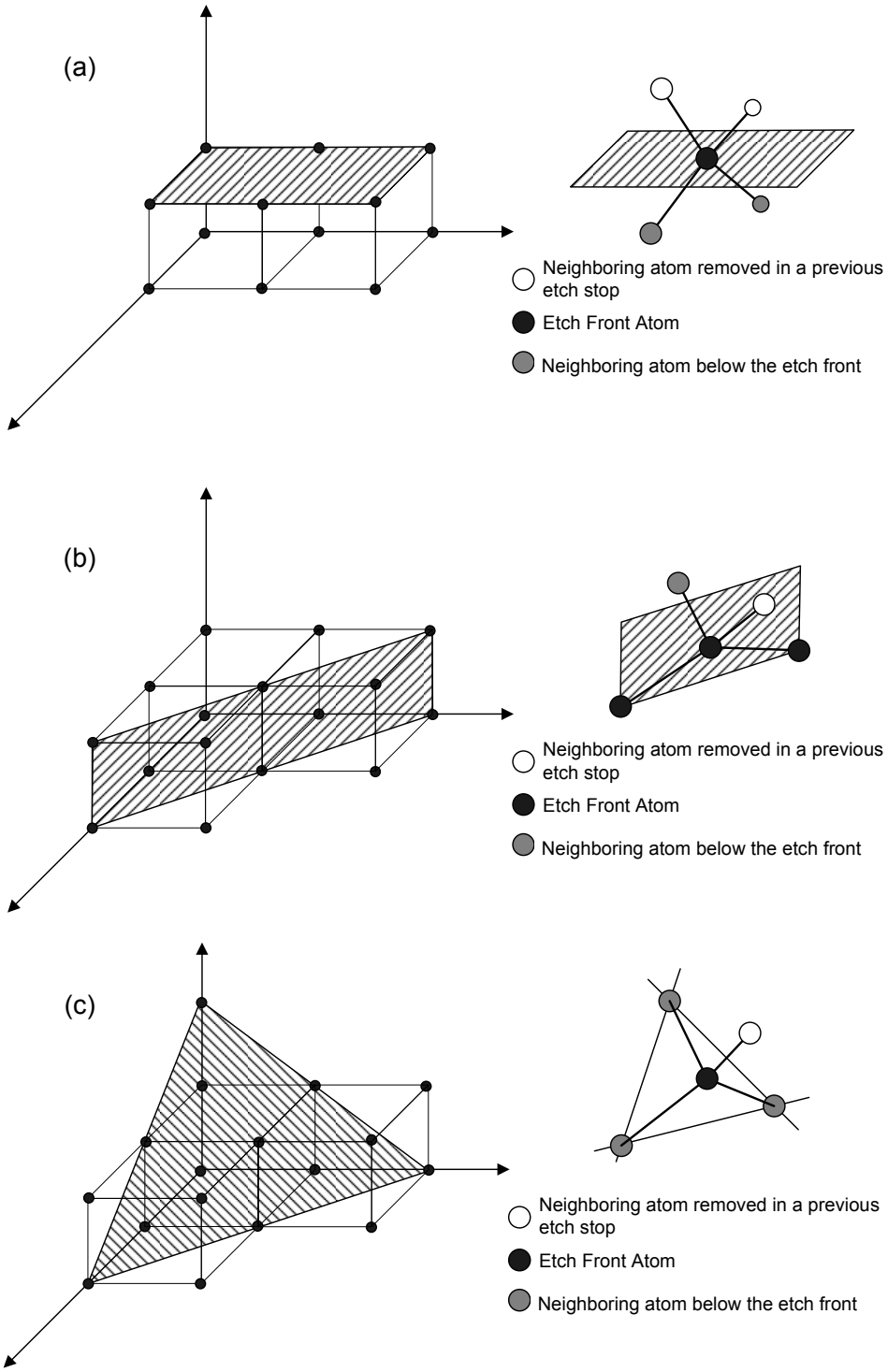

Figure 3.1: the cells/atoms contained in the $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ silicon crystal planes, (a), (b), and (c), respectively.

3.4.2 Orientation-Dependent Anisotropic Etching

As shown in Figure 3.2 (a), if the patterns are aligned along the [110] direction, that is, either horizontal or perpendicular to the major flat of the wafer, that etching leaves only the {111} planes exposed. Because both sides of a Si section sandwiched between two SiGe nanowires are exposed to the etching solution, etching proceeds at the same rate on both sides. Using the geometry of Figure 3.2 (a), the maximum Si etch depth at the center of the Si section where the two (111) planes meet can be expressed as:

$$depth = \frac{thickness/2}{\tan 54.7}$$

where 54.7 is the angle between the (100) and (111) planes. In the case of a 100 nm thick silicon layer sandwiched between two $Si_{1-x}Ge_x$ layers, this depth can be found as approximately 35 nm. Further etching can remove the rest of the silicon layer, which proceeds very slowly[2], while etching the $Si_{1-x}Ge_x$ layer at an even slower rate.

On the other hand, if the patterns are aligned along the [100] direction, that is, 45° off the wafer flat as shown Figure 3.2(a), {100} planes are exposed to the etchant from the beginning. On the other hand, the {110} planes, that etch faster than the {100} planes, are not exposed. As a result of this rotation, the lateral etch proceeds just like the vertical {100} etch without seeing any rate-limiting planes [63]. In selective etching for releasing the SiGe nanowires, the

[2]The etch rate of (111) is thirty-fold slower than that of (100).

above mentioned rotation proves very useful.

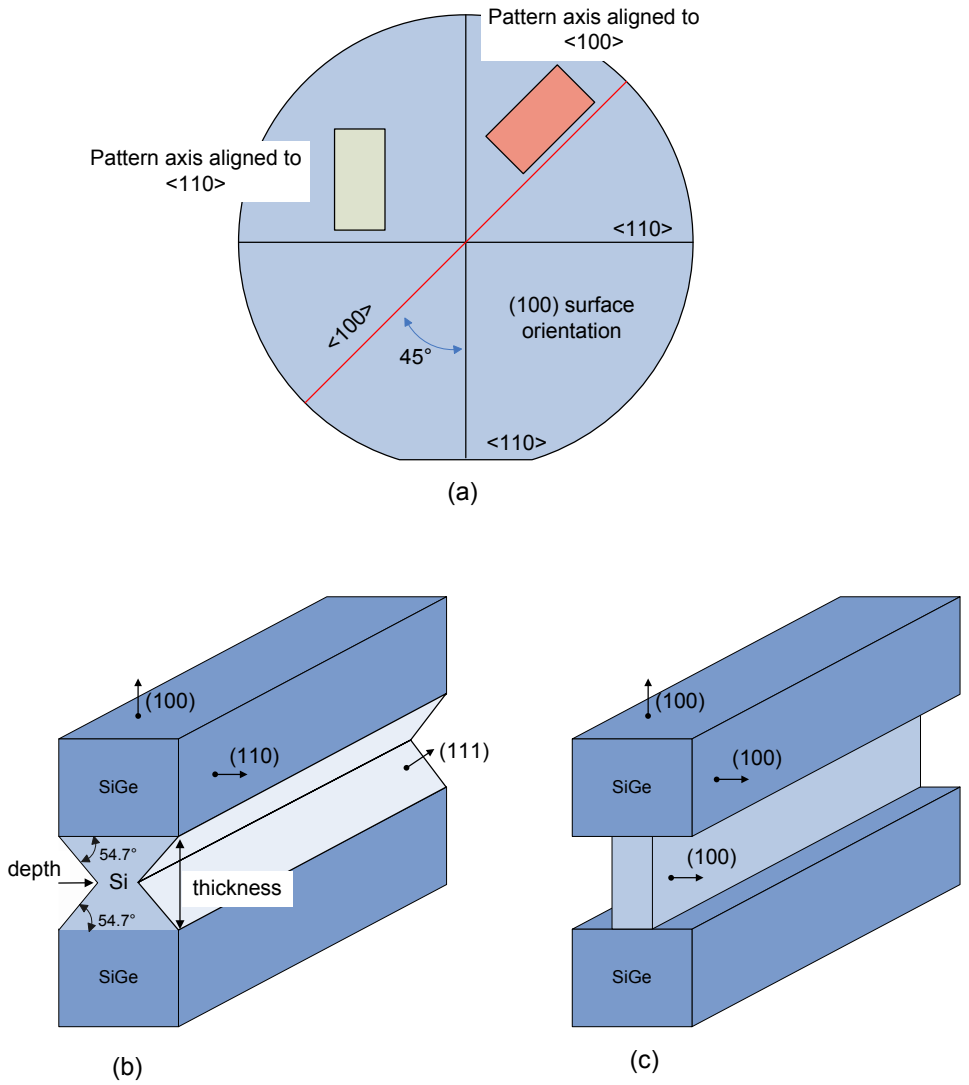

Figure 3.2: the orientation dependent anisotropic etching (a) the (100) wafer with two alignments (b)the cross-section aligned along $< 110 >$ (c)the cross-section aligned along $< 100 >$

3.4.3 Vertical Etch Rate and Selectivity

Initial experiments on the vertical etch rate and selectivity were geared toward verifying the reported etch rates for Si and $Si_{1-x}Ge_x$. The test structure used to measure the etch rate is shown in Figure 3.3. This is a simple test structure based

on defining a pattern on an oxide/$Si_{1-x}Ge_x$ stack, chemical etching in TMAH and using atomic force microscopy to measure the step height after etching. Since the thicknesses of the oxide is known beforehand, the measured step height can be used to determine the etch depth in $Si_{1-x}Ge_x$, hence the $Si_{1-x}Ge_x$ etch rate. Similarly, the same pattern is used to determine the Si etch rate without the $Si_{1-x}Ge_x$ epitaxial layer. The Si etch depth in TMAH is plotted in Figure 3.4 as a function of the etching time. As shown, a very close linear fit to the experimental data has been obtained yielding a Si etch rate of 309 nm/min at 73°C. The etch rate of $Si_{1-x}Ge_x$ in the same solution was found to be less than 1 nm/min promising a selectivity of 300 to 1, which was originally thought to be highly promising.

Figure 3.5 shows the vertical etch rate as a function of inverse temperature. The data reveals an activation energy of 0.73 eV, which is slightly higher (by 0.09 eV) than the value reported previously [66]. We believe that the difference is within the range of experimental errors, which may include errors in measuring the temperature, and the freshness of the etching solution.

3.4.4 Lateral Etch Rate and Selectivity

Our follow-up experiments clearly indicated that lateral etching of Si in TMAH progressed much more slowly in the previous experiments. Because the formation of $Si_{1-x}Ge_x$ nanowires depended on this selective etching process, it was necessary to overcome this challenge.

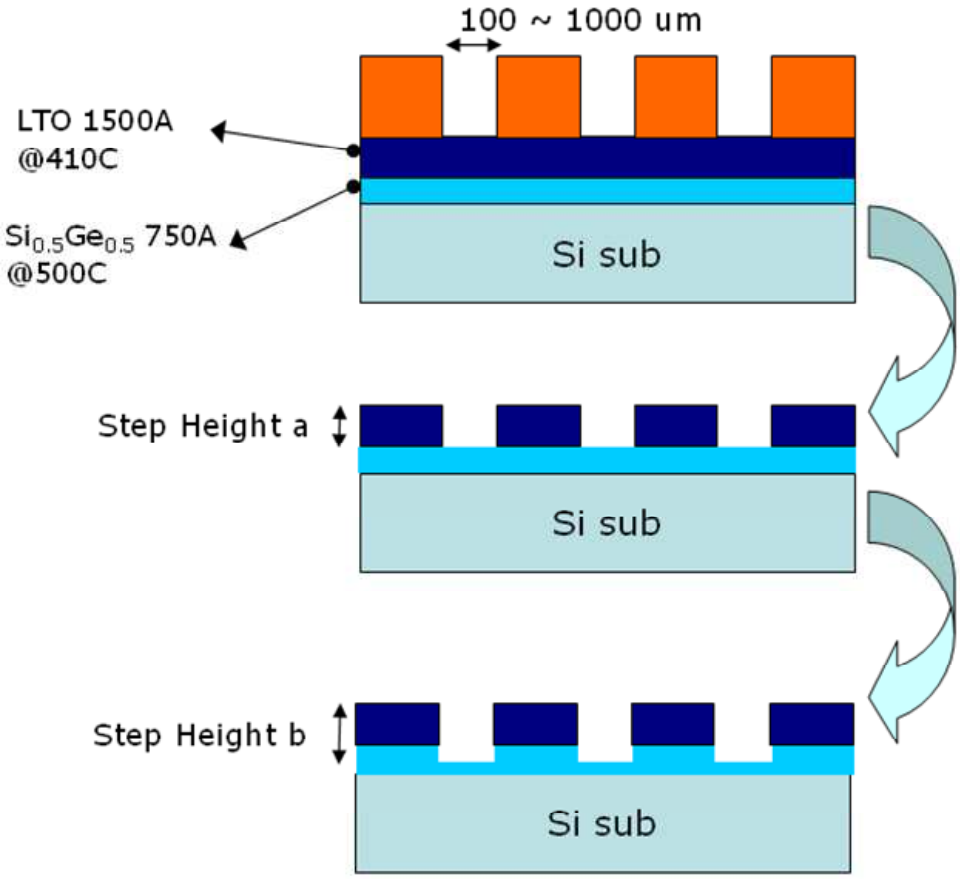

Figure 3.3: Test structure used to measure the Si and $Si_{1-x}Ge_x$ etch rates in TMAH

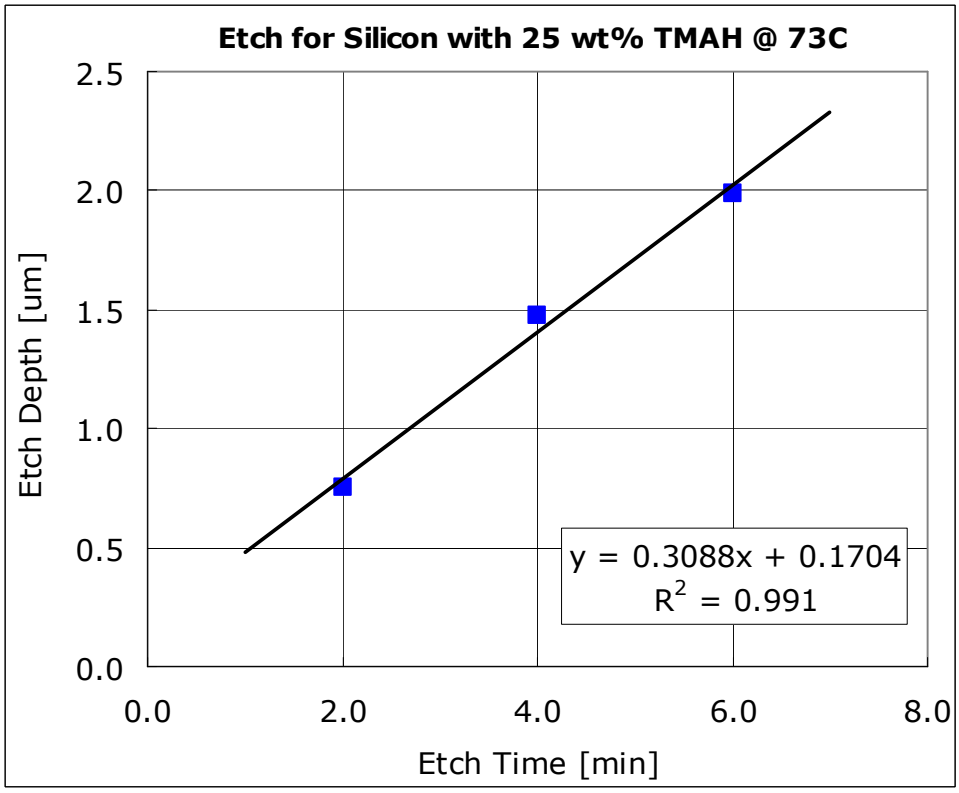

Figure 3.4: Si Etch depth after etching the pattern in TMAH

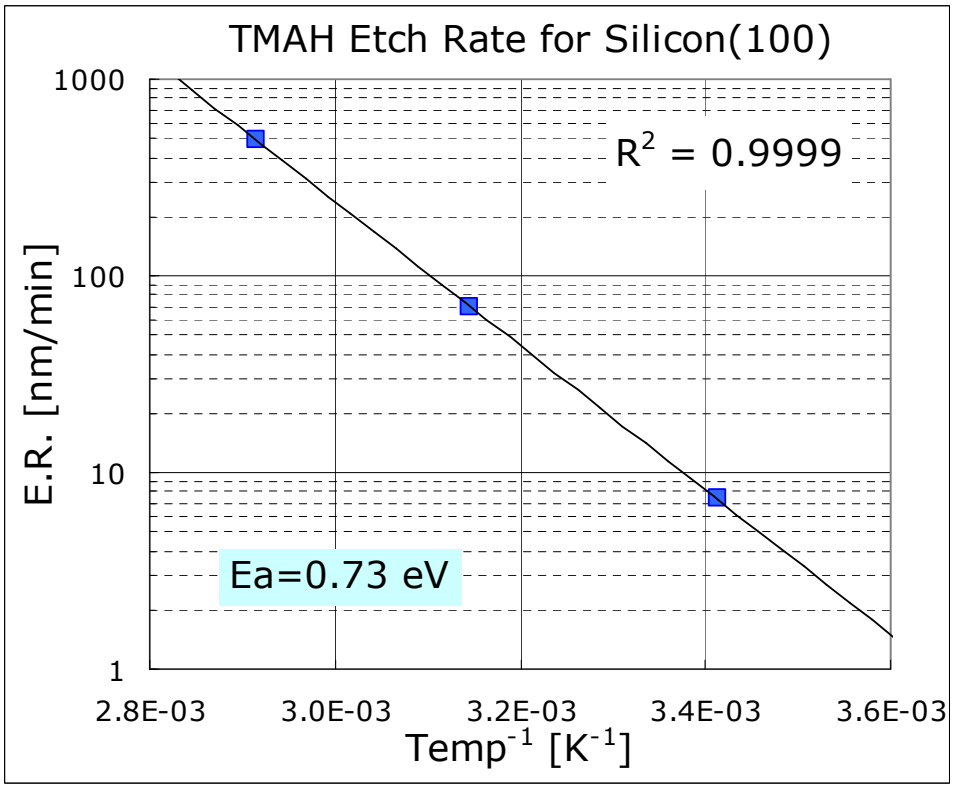

Figure 3.5: Vertical etch rate as a function of the inverse temperature

Our results showed that the Si etch rate was extremely small if the etching was carried out on Si wafers with major flats oriented along the [110] direction such that the nanowires are either parallel or perpendicular to the major flat. This created a significant challenge for us to form the $Si_{1-x}Ge_x$ nanowires by selective etching of Si, which prompted us to carry out experiments to characterize the Si etch rate in different orientations.

To characterize the etch rate, lithographic patterns of two different orientations ([110] and [100]) were defined on the same wafer as shown in Figure 3.6. In order to test the impact of Ge concentration, three different Ge concentrations of 17, 28 and 50% were employed. Finally, the samples were etched at three different temperatures of 20, 45 and 70 °C. Different samples included in this experiment are listed in Table 3.8. Shown in Figure 3.7 is the test structure used to characterize the lateral etching of Si. As shown, the structure consists of an epitaxial stack of $Si_{1-x}Ge_x$ and Si with a silicon nitride cap. The lateral etch rate of Si can be obtained with respect to either the $Si_{1-x}Ge_x$ or nitride, since both materials etch at about the same very slow rate, the measurement of which is beyond the accuracy of the experimental set-up used. Figure 3.8 shows SEM images obtained after etching various samples at 45°C for 2 minutes. The first row of images was obtained from features oriented parallel to the major flat of the Si wafer, hence, they have the [110] orientation. The second row was obtained from features rotated exactly 45 degrees with respect to the major flat resulting in an orientation of [100]. A striking difference between the

Figure 3.6: Nanowire patterns created in 100 and 110 orientations using the ASML scanner

Table 3.8: Sample set used to characterize the TMAH etch rate in (100) and (110) oriented patterns

Samples	20°C		45°C		70°C	
	0°	45°	0°	45°	0°	45°
2k11(17%)			O	O		
2k17(28%)	O	O	O	O	O	O
3k01(50%)			O	O		

two rows is that without rotation, the (111) facet is formed during etching while 45 degree rotation results in the vertical, (100) plane with no sign of faceting. Facet formation appeared to have some temperature dependence however, since the samples etched at 20°C did not show faceting while samples etched at higher temperatures clearly did.

The etch rate data obtained from this study is summarized in Table 3.9. It can be seen that both temperature and crystallographic orientation can significantly impact the etch rate. For example, at room temperature, the Si etch rate is negligibly small without orientation, while it is 5.9 nm/min with 45° rotation. On the other hand, when the etching is performed at 45°C, the etch rate is 23.5 nm/min even without rotation. It is important to note however that a facet is formed under these conditions as shown in Figure 3.8. At this temperature, the etch rate is even higher with 45°orientation and it is within 66.7 to 68.2 nm/min. It can be seen that the same etch rate was obtained for three different Ge concentrations. Since the Si etch depths were obtained with respect to $Si_{1-x}Ge_x$, we can conclude that the $Si_{1-x}Ge_x$etch rate is not a strong function of the Ge

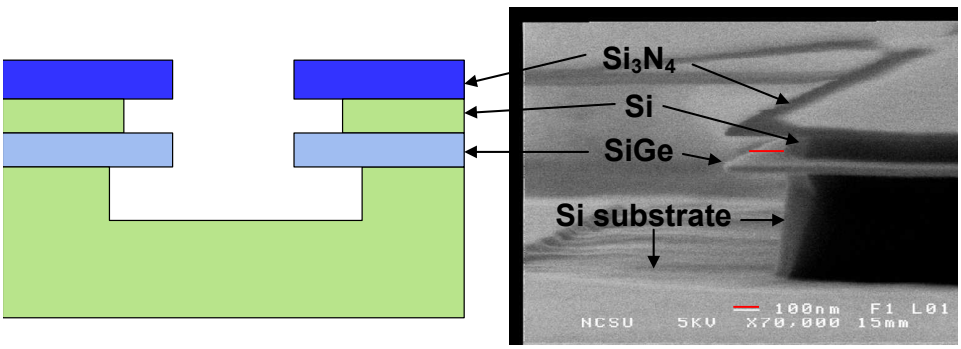

Figure 3.7: The test structure used in selective lateral etching experiments

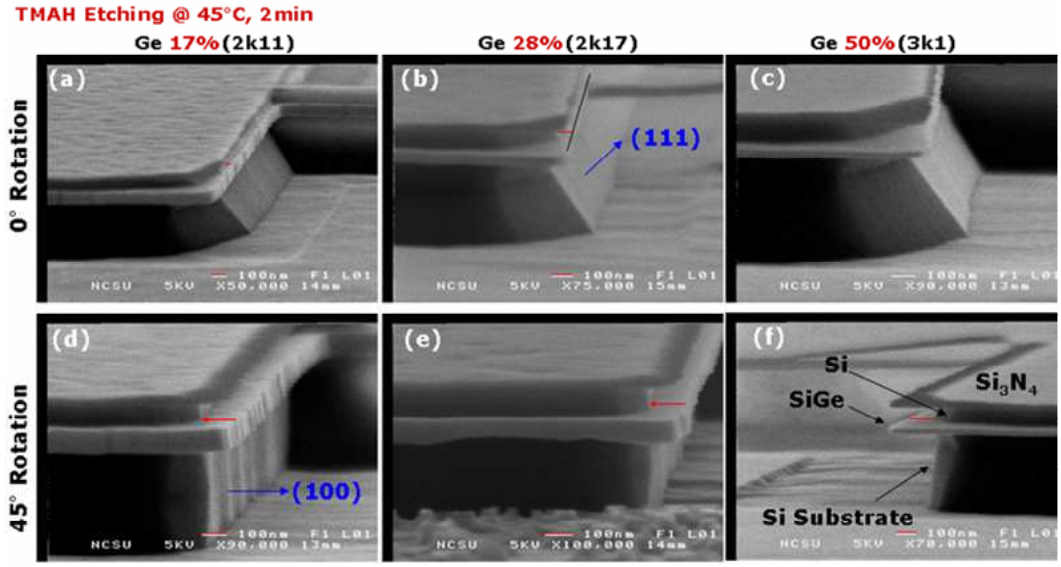

Figure 3.8: SEM Images obtained from samples formed using different Ge concentrations and different crystallographic orientations.

content, at least within the experimental range of this study. At 70°C, the Si etch rate is above 400 nm/min with 45° rotation and we were not able to measure the same without rotation.

The best news from Table 3.9 is that with 45° rotation, the Si etch rate obtained at different temperatures is almost identical to the vertical etch rate (given in Figures 3.4 and 3.5) promising an excellent selectivity with respect to $Si_{1-x}Ge_x$. We stress the fact that on none of the SEM images, we were able to observe any appreciable $Si_{1-x}Ge_x$ etching to quantify its etch rate.

Utilizing the excellent selectivity obtained above, we were able to demonstrate the first $Si_{1-x}Ge_x$ nanowires by orienting the patterns along the [100] direction as shown in Figure 3.9. The nanowires indicated complete etching of the Si in between the $Si_{1-x}Ge_x$ nanowires with excellent selectivity with respect to Si.

Figure 3.10 shows a dense array of SiGe nanowires fabricated using this

Table 3.9: Vertical and Lateral Si etch rates obtained from SEM and AFM analysis of the sample. Etch depths and etch rates are given in nm and nm/min respectively.

Conditions	Sample ID	Lateral E.R [nm/min] (by SEM)		Vertical E.R [nm/min] (by AFM)
		0°	45°	
20°C/15 min	2k17(28%)	N/A	5.9	7.0
45°C/2 min	2k11(17%)	23.5	66.7	9.0
	2k17(28%)	32.0	63.6	69.0
	3k01(50%)	N/A	68.2	69.0
70°C/1 min	2k17(28%)	N/A	462.5	495.0

method, which shows the potential of the technique in forming an array of nanowires in bio/chemical sensor and thermoelectric applications. The stack consists of four planes of $Si_{1-x}Ge_x$ nanowires. The spacing between the nanowires is about 100 nm.

Another interesting aspect of the new experiments is the mechanical stability of the nanowires. Figure 3.11 illustrates deformation observed in 10 μm long nanowires. The nanowire diameter is close to 50 nm. No deformation was observed in shorter nanowires (e.g. 2 μm shown in Figure 3.10). While this result is not surprising, studies must be carried out to understand the fundamental mechanisms behind this deformation. We believe that stress may play a significant role in addition to gravity. In particular, we expect the $Si_{1-x}Ge_x$ planes to be under biaxial compression laterally and under tension vertically. As such, we expect the $Si_{1-x}Ge_x$ nanowire bridges to be under compression, which might

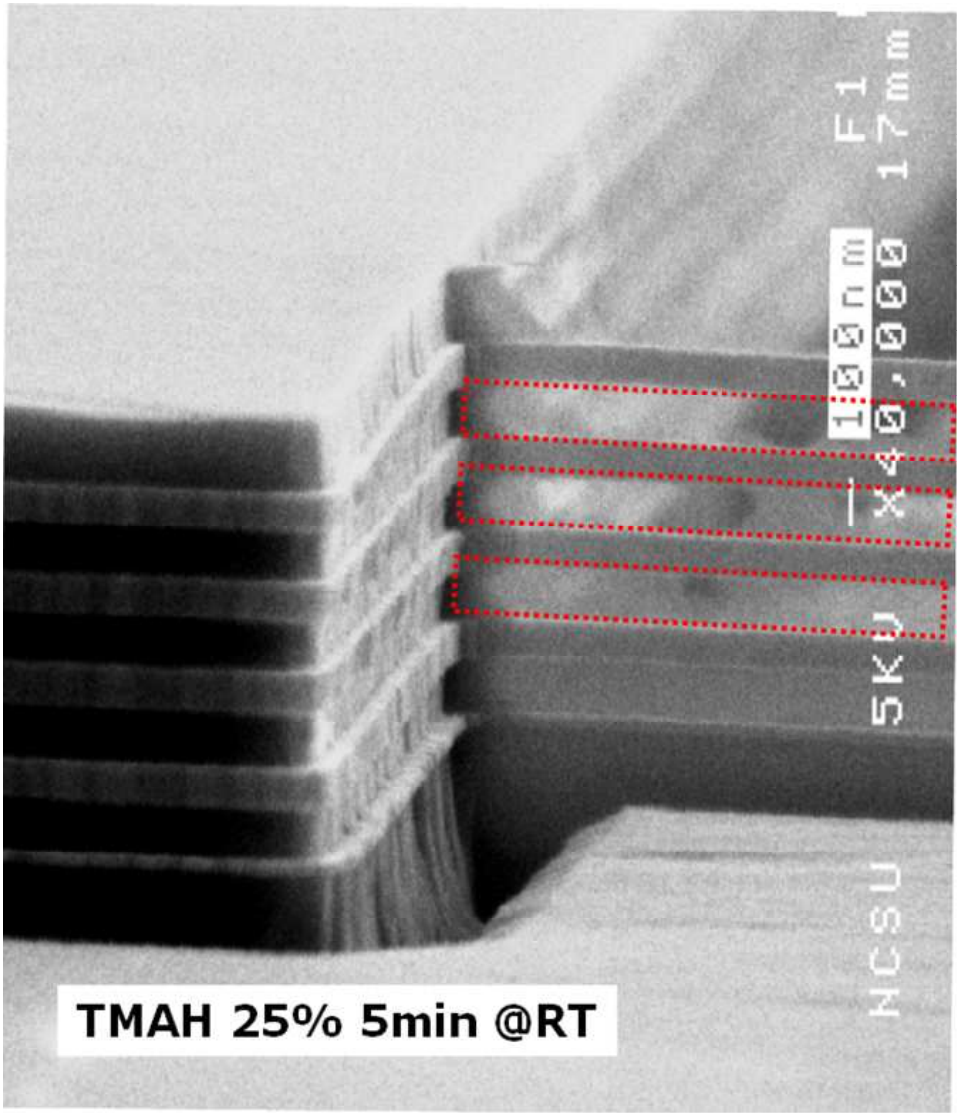

Figure 3.9: First $Si_{1-x}Ge_x$ nanowires formed by selective Si etching.

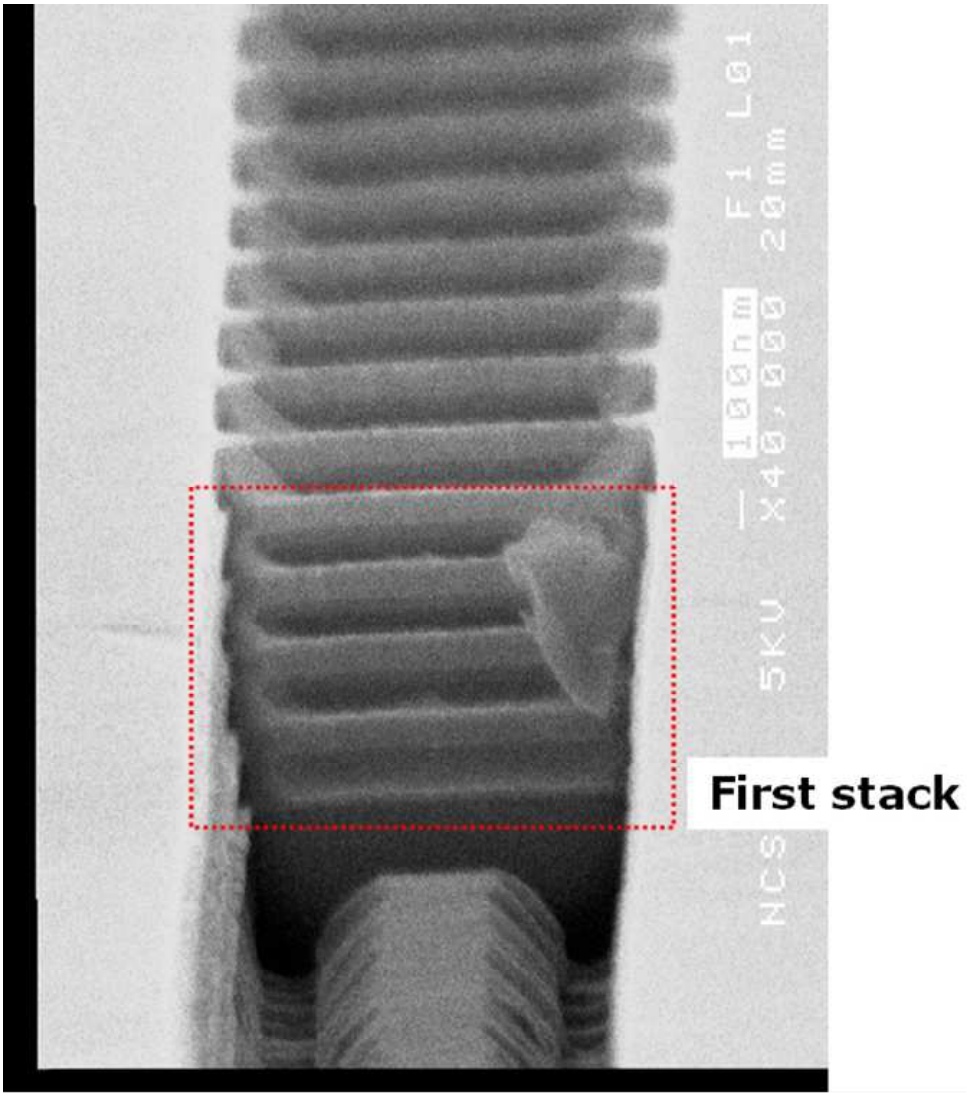

Figure 3.10: $Si_{1-x}Ge_x$ nanowires obtained by selective Si etching in TMAH.

force the nanowires to bend if they are below a certain diameter.

A similar idea was recently proposed by another group [67]. In their approach, the researchers grew an epitaxial stack of Si and Ge, patterned and etched the nanowires, and then oxidized them. Since germanium oxidizes much faster than silicon, germanium could be fully oxidized while silicon survived. Also, during oxidation germanium diffuses into the adjacent silicon layers converting Si into $Si_{1-x}Ge_x$. The fully oxidized germanium can then be etched in dilute HF, leading to suspended $Si_{1-x}Ge_x$ nanowires. Unfortunately, the $Si_{1-x}Ge_x$ nanowires formed using this approach do not have the same Ge concentration across the cross-section of the nanowires. They have shown that the Ge composition varied from 16.6% near the surface to 0.3% in the center of nanowire, which we believe is a major disadvantage of the technique compared to the method proposed in this study.

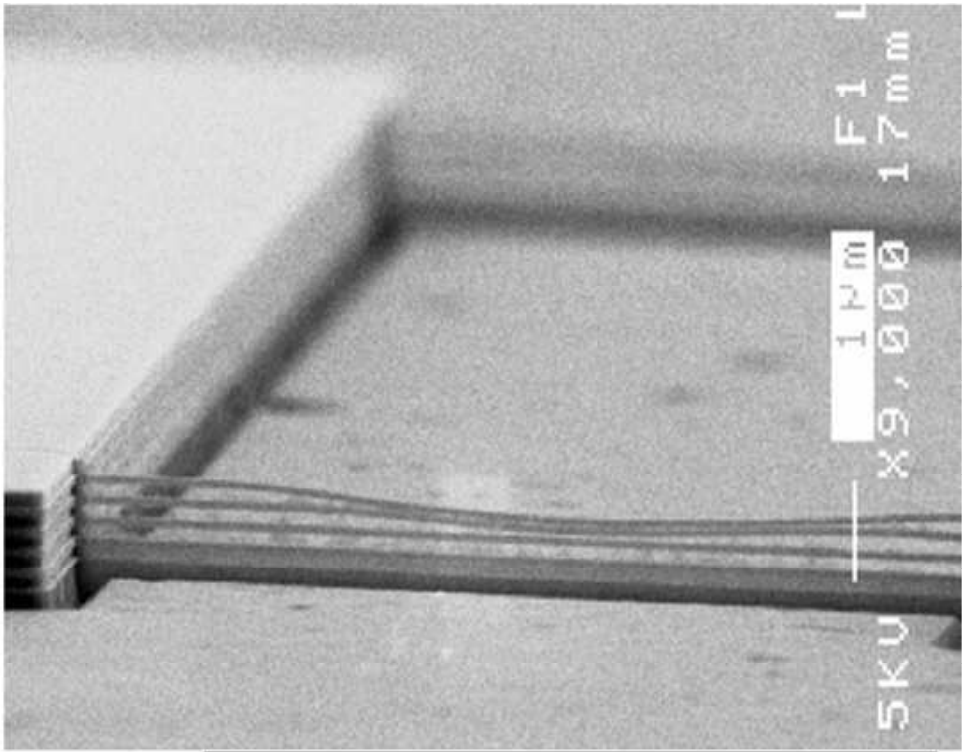

Figure 3.11: Deformation observed in 10 μm nanowires.

Chapter 4

Nanowire Characterization

4.1 New Lithographic Mask

For measurements of the electrical and thermal conductivity of the nanowires, a new mask set was designed and manufactured. The mask set shown in Figure 4.1 was designed for the ASML 193 Scanner and it consists of two levels both written on the same reticle. The first level is used to define the nanowires as described in this report. The second level is used to form the metal contact pads for electrical measurements. Using the precise coordinates of the two levels, alignment can be readily achieved.

A simple, four-point probe structure shown in Figure 4.2.a was designed to measure the resistance of the nanowires. An enlarged section of the test structure showing the metal pad and the individual nanowires is shown in Figure 4.2.b.

The reticle includes 24 test patterns, which varies in width, length, and the number of nanowires per structure. The exact dimensions of the nanowires are tabulated in Table 4.1.

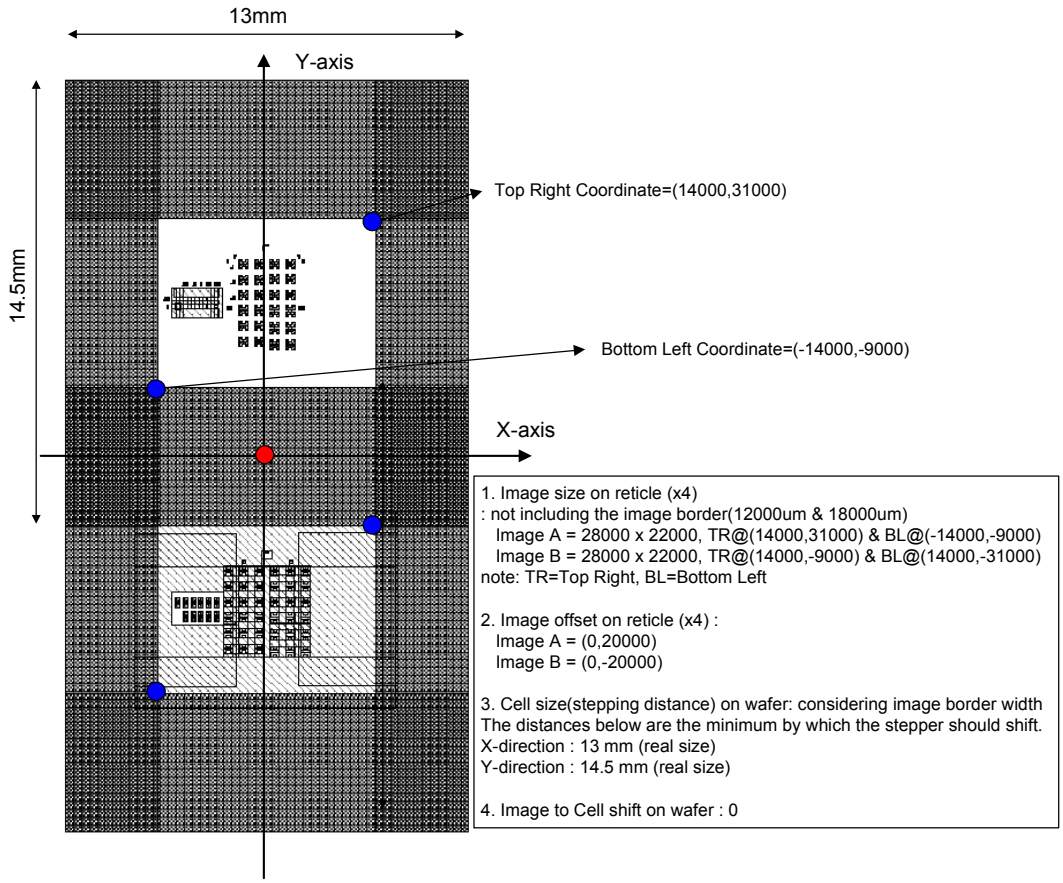

Figure 4.1: The layout of reticle with information for generation of the scanner job file.

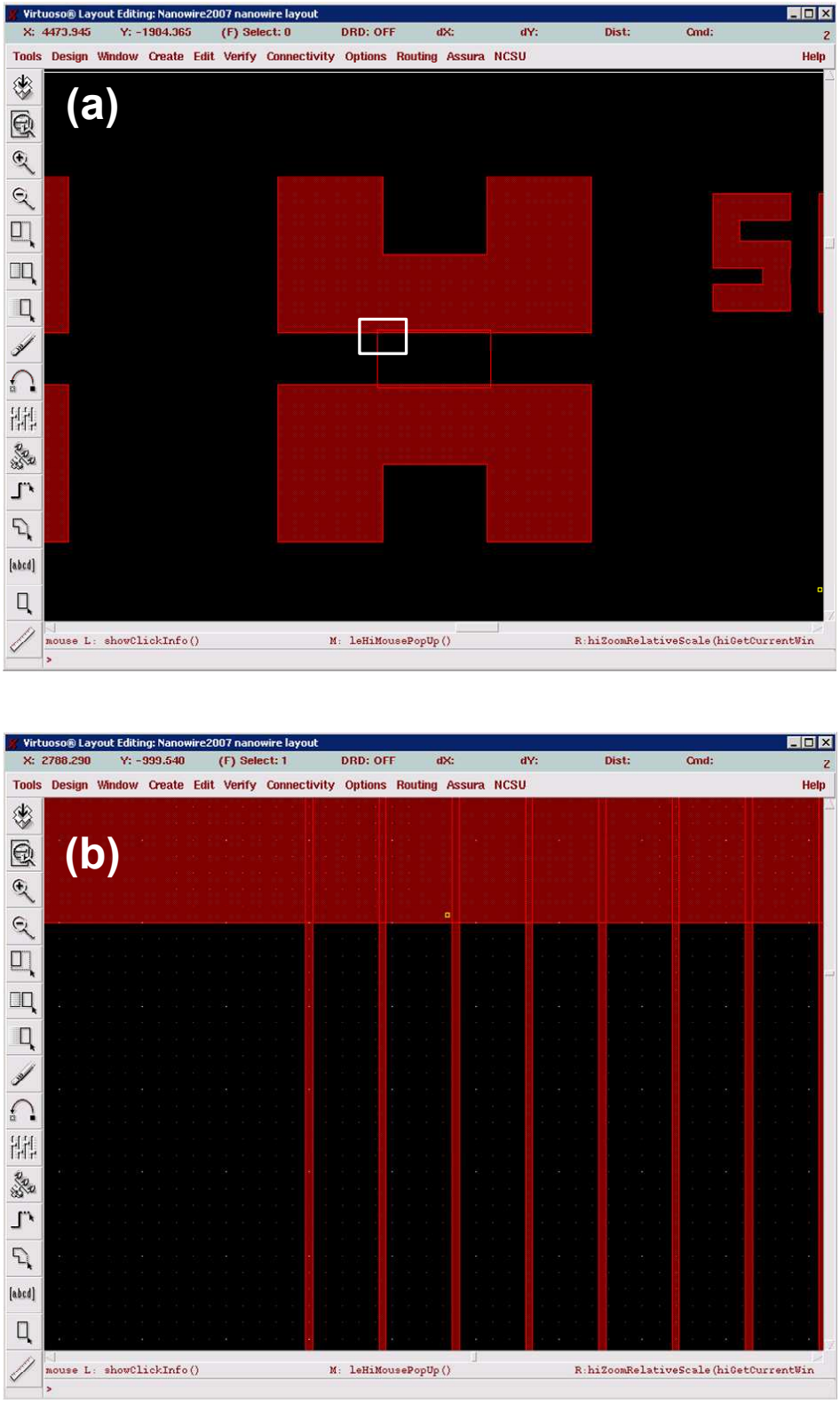

Figure 4.2: The simplified four-point probe test structure:(b) is the enlargement of the white box in (a).

Table 4.1: Critical dimensions of the test patterns available on the new mask

width [nm]	# of nanowires	length [μm]
100	1	1, 5, 10, 50
	100	1, 5, 10, 50
200	1	1, 5, 10, 50
	100	1, 5, 10, 50
500	1	1, 5, 10, 50
	100	1, 5, 10, 50

4.2 Fabrication of the Test Structures

Experiments were carried out to design and optimize a process flow to fabricate the test structures employing only two lithographic steps.

The detailed process flow is included in Table 4.2. According to this flow, after the standard surface preparation steps, the Si/SiGe superlattice is epitaxially grown on Si. An 80 nm thick oxide layer is deposited on the superlattice to serve as the hard mask during reactive etching. The nanowires are then defined using the first lithographic mask and then anisotropically etched in Cl_2 by reactive ion etching. After etching of the oxide in dilute hydrofluoric acid, wafers are again coated with photoresist for the second and the final lithographic step. This step leaves windows in the photoresist where the metal pads will be formed.

After evaporation of the metal, the pads are formed by the lift-off method. Finally, the Si layers in between the $Si_{1-x}Ge_x$ nanowires are etched in TMAH. The selective etching was performed in the last step so that the possible breakage of the nanowires could be avoided during the formation of the metal pads. For

successful lift-off, the photo-resist thickness has to be at least twice the thickness of the deposited metal. The standard Al thickness used in our laboratory is 200 nm, which provides a metal layer relatively resistance to scratching during probing. Therefore, we had to increase the thickness of the photoresist from 300 to 500 nm by decreasing the rotational speed to 1000 rpm during spin coating of the wafers. It is important to note that the BARC remaining in the openings for the metal pads should be removed before Al evaporation to form good, ohmic contacts to Si. After the lift-off, any remaining BARC on the wafer - especially on the nanowires - should be removed since it prevents TMAH from etching silicon.

Another challenge is to prevent TMAH from attacking the Al pads. To avoid this, a protective a 30 nm thick Ni layer was deposited on Aluminum. Pictures taken after Ni/Al deposition and lift-off are shown in Figure 4.3. SEM micrographs after Ni/Al lift-off and selective etching are shown in Figure 4.4 and Figure 4.5, respectively. The images show that nanowires can be successfully fabricated with metal pads using the process described in Table 4.2. While Ni provides some immunity to TMAH, experiments are underway to replace it with Pt to improve the protection of the metal pads. The preliminary experiments indicate that Pt is completely resistant to TMAH.

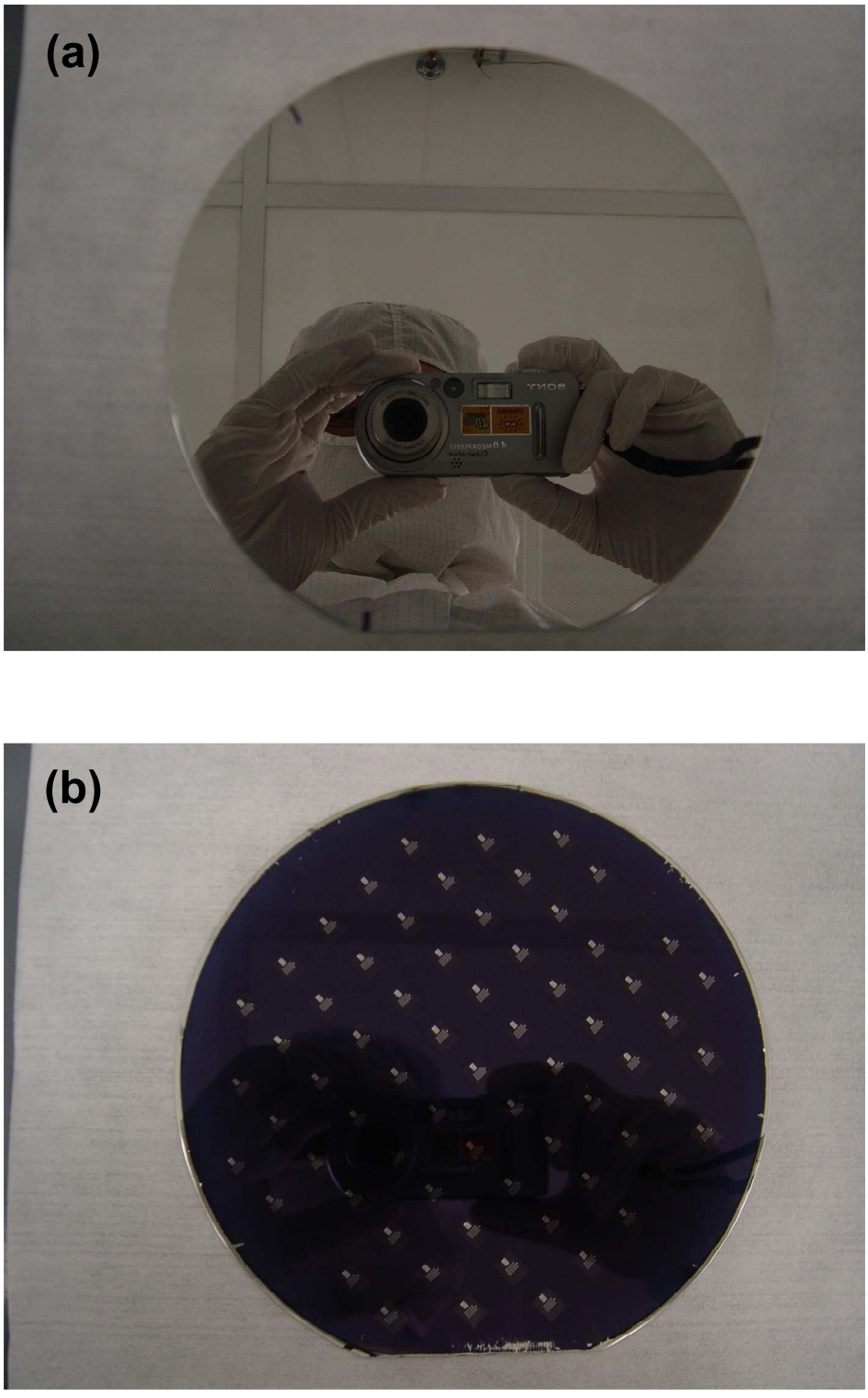

Figure 4.3: Pictures taken after Ni/Al deposition (a) and after lift-off (b).

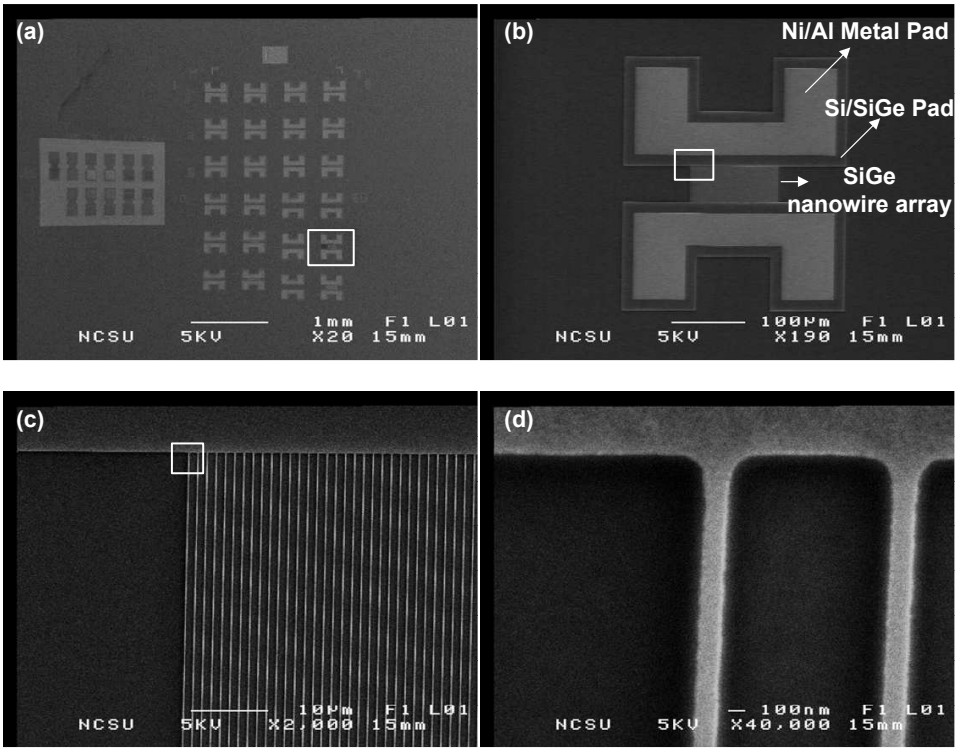

Figure 4.4: SEM micrographs obtained after Ni/Al lift-off:(a) the complete layout,(b) a 200 nm-wide nanowire array, (c) enlarged view of (b), (d) enlarged view of (c).

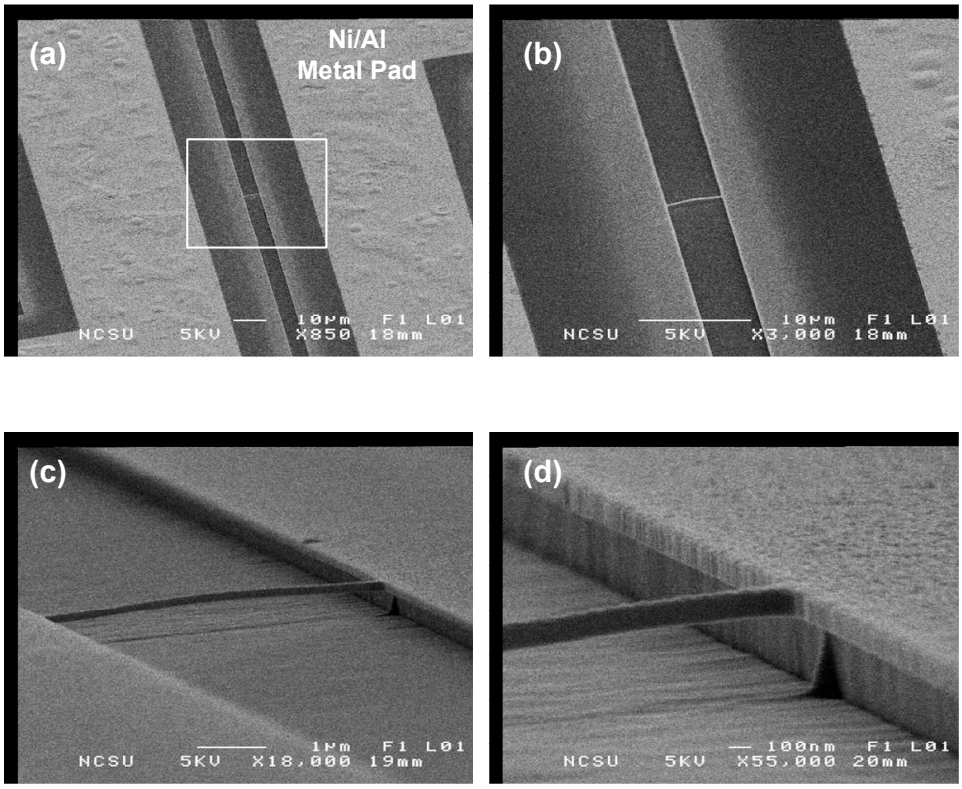

Figure 4.5: SEM micrographs after selective etching:(a) a 200nm-wide nanowire, (b) enlarged view of the nanowire shown in (a), (c) 74°tilted view, (d) 86°tilted view.

4.3 Measurement Results

Electrical measurements were performed on nanowires with four different lengths of 1 , 5, 10 and 50 μm before and after selective etching using an HP4145 parametric analizer. Scanning electron microscopy (SEM) was employed to determine the cross-sectional area of the nanowires. From the top view SEM micrographs, the width of the nanowires after all processing steps was measured as $\sim 130\ nm$. The thickness of the $Si_{1-x}Ge_x$ layer used to form the nanowire was also $\sim 130\ nm$. Figure 4.6 shows the results obtained from two and four point probe measurements prior to selective etching of the Si layer above and below the $Si_{1-x}Ge_x$ layer. It can be seen that the two measurements are in agreement with each other within 1%. The 2-probe measurements employed the internal source monitoring unit (SMU) voltmeters of the instrument. For the 4-probe measurements the voltage monitoring unit (VMU) was used, which provides a much higher input resistance. The fact that the two measurements are in agreement implies that the parasitic resistances included in the circuit are well below the input resistance of both voltmeters. As shown in Figure 4.6, the resistance of a 10 μm long nanowire is 0.95 $k\Omega$. It is important to note that this resistance includes the effect of the p-type Si layer on top of the $Si_{1-x}Ge_x$ nanowire. Finally, the measured resistance did not change with time, which was originally considered as a potential measurement challenge due to self-heating of the nanowires.

After selective etching, the resistance increased by approximately 2.5 times as shown in Figure 4.7, which is expected considering the fact that the silicon layer

on top, which was selectively removed was just as thick as the $Si_{1-x}Ge_x$ nanowire underneath. As expected, the resistance of the nanowires increases with increasing length of the nanowires as shown in Figure 4.8. Using a cross-sectional area of 130 $nm \times 130$ nm, we have found the resistivity of the $Si_{1-x}Ge_x$ nanowire to be $\approx 8\times10^{-4}$ $\Omega \cdot cm$, which is within the expected range for heavily boron doped $Si_{1-x}Ge_x$ layers grown in this reactor.

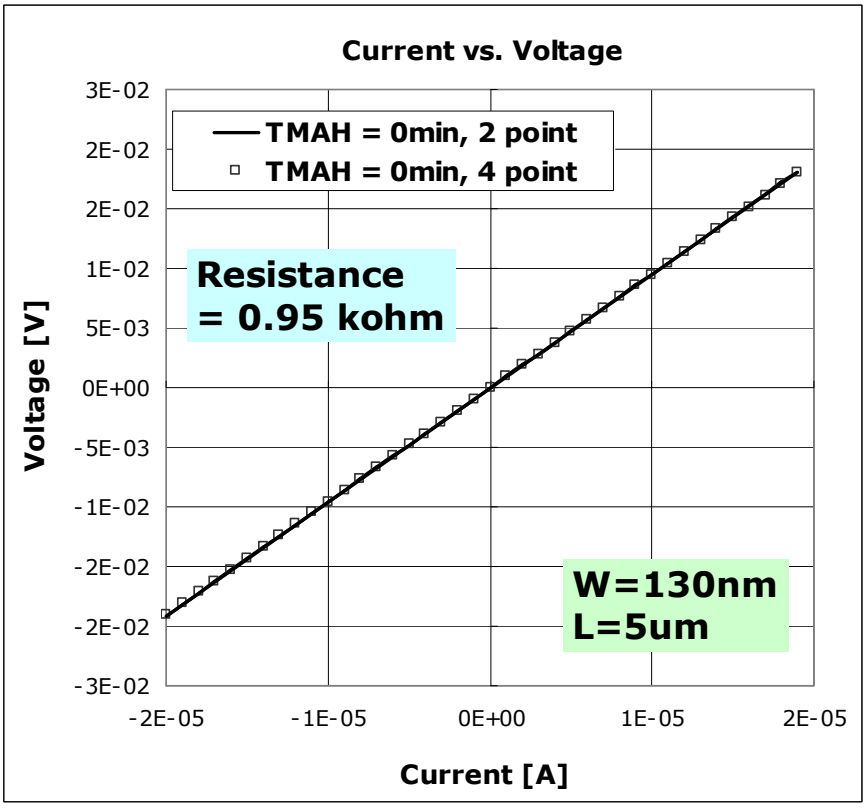

Figure 4.6: The current versus voltage graph showing the results of the two and four point probe measurements prior to selective etching of the Si layer above and below the $Si_{1-x}Ge_x$ layer.

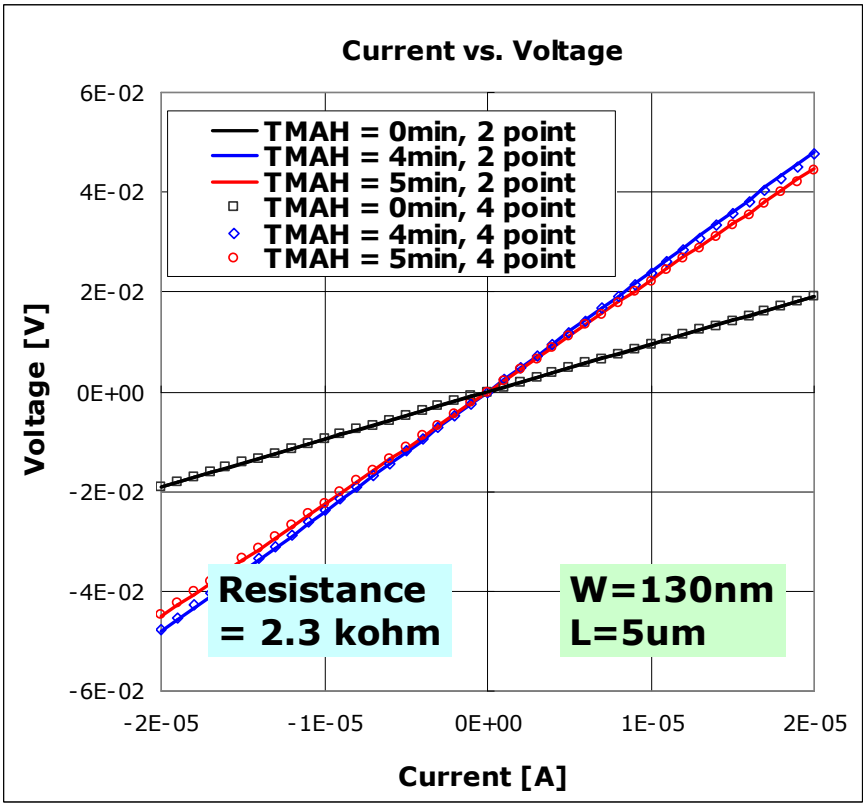

Figure 4.7: The current versus voltage graph of samples before and after selective etching.

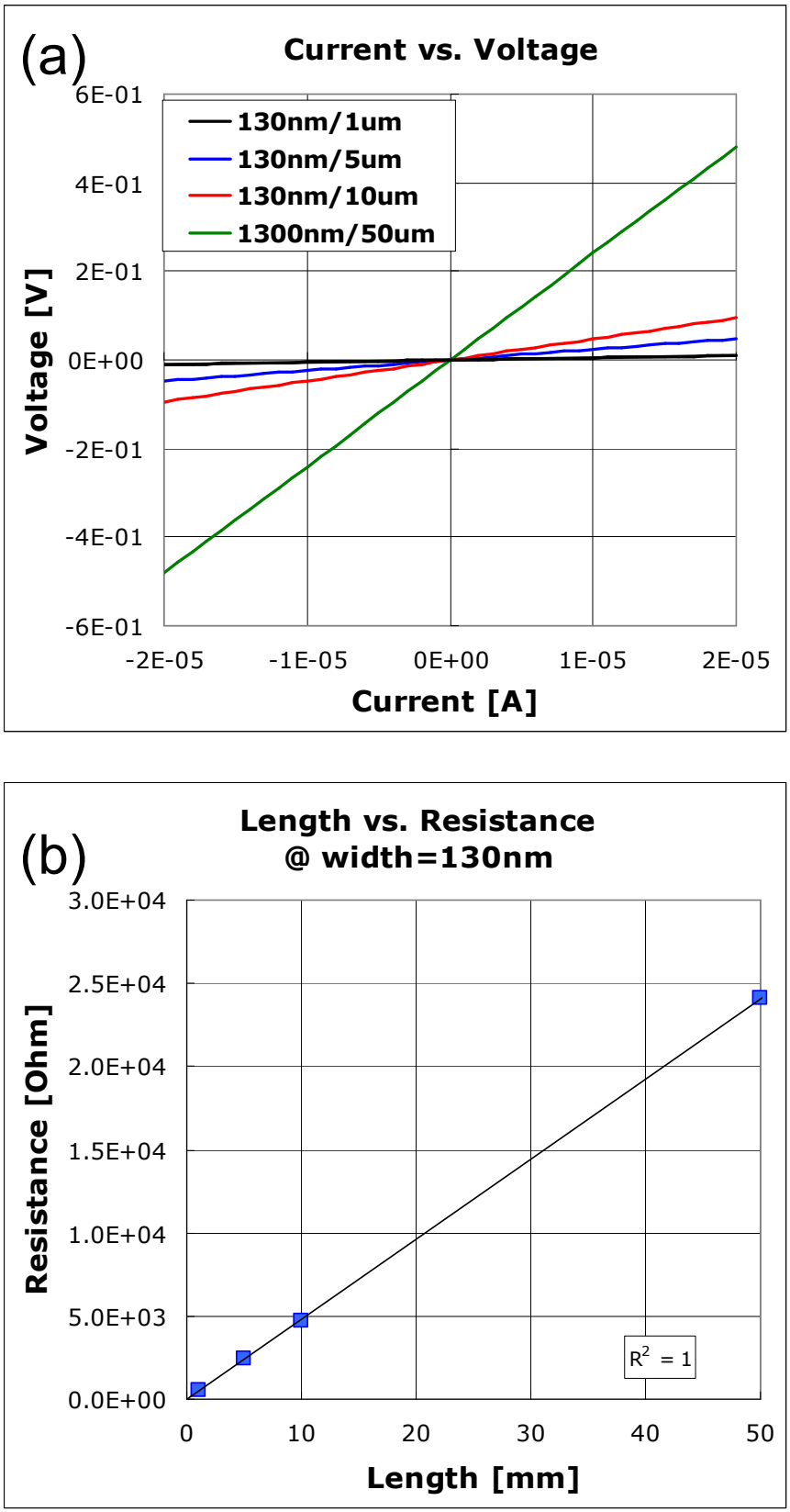

Figure 4.8: The current versus voltage graph of 1, 5, 10, and 50 μm long nanowires: (a) the four point probe measurement, (b) the length versus resistance plot.

Table 4.2: Process Flow for the Electrical and Thermal test structures.

step	process name	description
1	Surface Preparation	RCA cleaning Spin Drying 1% HF dip for 30 sec Blow-Drying by N_2
2	Si/SiGe Epitaxy	800°C, 500°C
3	LTO Deposition	410 °C, 800 Å
4	Nanowire Mask	Resist Coating Exposure(focus= ,energy=18 mJ) Development
5	BARC/LTO Etch	BARC E/T LTO E/T measure the remaining oxide
6	Si/SiGe Etch	Oxide-Through Etch with Cl_2 Si etch with Cl_2/O_2 PR strip with O_2
7	LTO Removal	BOE for 2 min
8	Metal Pad Mask	Resist Coating Exposure(focus= ,energy=23 mJ) Development
9	BARC Removal	40 mT, 50 W, 8 sccm O_2, 90 sec Inspection by microscope
10	Al Evaporation	200 nm
11	Ni Sputtering	30 nm
12	Lift-off	Soaking in acetone for 40min Cleaning with acetone Cleaning with methanol Rinsing with D.I. Water
13	BARC Removal	50 mT, 50 W, 8 sccm O_2, 60 sec Inspection by microscope
14	Selective Etch	1% HF dip for 30 sec TMAH Etching Rinsing with D.I. Water

Chapter 5

Summary and Future Work

We have successfully demonstrated a novel method to form a three-dimensional array of Si or $Si_{1-x}Ge_x$ nanowires that are horizontally aligned to the Si substrate. Unlike previous attempts, the nanowires of desired diameters and lengths can be readily formed at desired locations on a standard Si substrate. Also, this process does not need any catalyst metals such as gold used in other growth techniques.

The process relies on epitaxial growth of Si and $Si_{1-x}Ge_x$ layers, conventional lithography, reactive ion etching and selective etching of Si with respect to $Si_{1-x}Ge_x$ or selective $Si_{1-x}Ge_x$ etching with respect to Si. All of these processes exist in state-of-the-art silicon IC manufacturing; therefore, the proposed method can be readily implemented on Si chips for the integration of sensors and thermoelectric devices. Furthermore, the nanowires themselves can serve as the channels of MOSFETs allowing three dimensional integration of MOSFETs for increased current drive.

Selective etching was achieved with TMAH, which is an anisotropic etchant and does not contain any alkali metals. It has been shown that the Si vertical etch rate is at least 300 times faster than the etch rate of $Si_{1-x}Ge_x$ at 73 °C. This was true for even 17% Ge, which was the lowest Ge concentration used in this study. For lateral etching it was found that by aligning the patterns along the [110] direction which is horizontal or perpendicular to the major flat of the (100) wafer, the etching proceeds only until two (111) planes meet at the center of silicon layer sandwiched between the top and bottom $Si_{1-x}Ge_x$ layers. After this, etching continues very slowly because of the very slow etch rate of the {111} planes. On the other hand, when the patterns aligned along the [100] direction, the {110} planes are exposed and their etch rate is faster than that of the {100} planes. Therefore, the desired etch rate and the selectivity to $Si_{1-x}Ge_x$ nanowires can be obtained.

The $Si_{1-x}Ge_x$ nanowire has the resistivity of $\approx 8\times10^{-4}\ \Omega \cdot cm$, which is within the expected range for heavily boron doped $Si_{1-x}Ge_x$ layers grown in this reactor.

Table 5.1 lists the features of three different methods proposed by Hewlett Packard, Institute of Microelectronics at Singapore, and NCSU. The simple 'pick and place' method is omitted here. The method proposed by Institute of Microelectronics at Singapore is very similar to our method in that all the process steps are compatible with CMOS manufacturing. However, in the Singapore method, it is difficult to obtain a uniform germanium concentration within the cross-section

of the nanowire. The Ge concentration is maximum at the surface ($\approx 17\%$) and decreases toward the center of the nanowire ($\approx 0.3\%$). In the NCSU method, the Ge concentration is uniform since it is determined by epitaxy.

SEM images of the nanowires indicated some bending when the nanowires were too long. Future work must focus on the mechanical properties of these nanowires to understand the effects of the diameter/length ratio on the mechanical stability of the nanowires. Furthermore, the thermal properties of the nanowires should be studied.

Table 5.1: Comparison of the HP, Singapore and NCSU methods

	Hewlett-Packard	Singapore	NCSU
CMOS compatibility	moderate	good	good
Contact resistance	good	good	good
Three dimensionality	limited	good	good
Dimensional Control	limited	good	good
SiGe composition	bad	bad	good

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