Abstract

PARK, KIE JIN. Charge defects in low temperature Silicon Nitride/Silicon Interfaces for Applications in Computational Clothing and Electronic Textiles. (Under the direction of Dr. Gregory N. Parsons.)

The purpose of this research has been to 1) explore materials prepared using plasma enhanced chemical vapor deposition (PECVD) for amorphous silicon thin film transistors (TFTs) fabricated on large area flexible polyimide substrates, and 2) develop new concepts to make smart fabrics for computational clothing using the flexible TFTs.

For item 1), silicon nitride films, as gate dielectric of TFTs, were deposited using various processing gases having different NH_3/SiH_4 gas ratio with constant temperature and various temperature at constant processing gas ratio. It was shown that as NH_3/SH_4 ratio increases, NH/SiH ratio increases. Apparent leakage current decreased but the flat band voltage was shifted with increasing NH/SiH in the films. It was proposed that the decrease in apparent leakage current with increasing NH/SiH ratio was related to charge screening effect as well as film improved insulating quality. The interface charge and bulk charge densities for SiN_x films with different processing gas composition have been calculated. The interface charge density increases with increasing NH/SiH causing flatband shift and increasing total charge density. It was believed that the interface charge is generated by stress build up at Si/SiN_x interface and increases with NH/SiH ratio. We found that as substrate temperature increases the NH/SiH ratio remains constant, the apparent leakage current increases and the flat band voltage shifts. Because the net total charge is compensated as substrate temperature changes, charge screening

effects were believed to be less important than effects of composition change under the conditions studied. Interface charge density increased also with temperature. This was consistent with flat band voltage shift with temperature.

For item 2), amorphous silicon TFTs were formed successfully on large area polyimide substrate using back channel inverted staggered structure and novel masks design. Linear and saturation mobility are 0.026 and 0.059 $cm^2/V•s$, respectively. To address TFTs into clothing, conductive thread contact was investigated. Finally, using novel method, we attempted to form an electronic NOR gate using thin film transistors on polyimide, woven directly into a cotton fabric.

Charge Defects in Low temperature Silicon Nitride/Silicon Interfaces for Applications in Computational Clothing and Electronic Textiles

by

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Biography

The author was born on February 28, 1967 in Pusan, South Korea. He received his B.S. and M.S. degrees in Chemical Engineering in 1991 and 1993 from Pusan National University. He worked for Kolon Research and Development Center as a senior researcher from the January 1993 to the December 1999.

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Chapter I.

Introduction

1.1 Background

Conventional metal-oxide-silicon (MOS) field effect transistors are fabricated on crystalline wafers of silicon cut from a crystal boule grown from a melt. Metal-oxide-silicon field effect transistors thus fabricated have high mobility (~1000 $cm^2/V•s$) and relatively small feature size (~0.18) micrometers. In many applications, electronic devices have to be made on substrate rather than on single crystal silicon[1] MOS transistors thus fabricated are usually called thin film transistors (TFTs). Thin-film transistors (TFTs) were proposed by Weimer[2, 3] in 1961. For the application in the integrated circuits (IC's), thin film transistors are used as load devices of static random access memory[4]. For the application in large area circuits, thin film transistors are used as switches of pixel elements of active matrix liquid crystal displays (AMLCD's). For the sake of manufacturing cost and ease of fabrication, amorphous silicon thin film transistors (a-Si TFTs) are adopted currently in industry for the manufacturing of active matrix liquid crystal displays. The carrier mobility of amorphous silicon thin film transistors is much lower (0.5 ~1.0 $cm^2/V•s$).

1.2 Hydrogenated Amorphous Silicon TFTs

Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) were first reported in 1979[5]. A-Si:H TFTs have been used as the switching devices for the active matrix liquid crystal display[5, 6]. Three-terminal devices (like TFTs) are more flexible in their operation and have fewer limitations than two-terminal devices (i.e. diode). Hydrogenated amorphous silicon is a material with well-balanced features for electronic

applications. There are some advantages of a-Si:H[7]. A-Si:H is usually deposited by plasma enhanced chemical vapor deposition (PECVD) in which silane gas (SiH_4) is decomposed in a plasma excited by rf power. A typical rf frequency is 13.56 MHz, although much lower frequencies (e.g. 100Hz) can also be used. Using this technique, films can be deposited with thickness variations of only a few percent over the entire surface area. A-Si:H film can be deposited at low temperature. Low temperature deposition is essential in the fabrication of active matrix liquid crystal displays because glass or plastics are used as the transparent substrate materials[8-11] . The deposition rate must be low because good-quality a-Si:H films can only be formed if hydrogen is incorporated into the amorphous network; hydrogen will not be retained in the film if the substrate temperature is higher than 450 °C. a-Si:H is an amorphous material, so it can easily form hetero-interfaces while maintaining good interface properties. It is possible to deposit amorphous silicon on various substrates such as insulators (including glass, oxides, and nitrides), metal and semiconductors. The interface properties between the a-Si:H and the SiN_x gate insulator play a critical role in TFT characteristics. The a-Si:H forms good interface with all these materials, making the processing of TFTs very flexible and allowing a variety of processing schemes to be devised and used in the process line. Amorphous silicon is a hard scratch-resistant material (Vickers hardness HV = 1,500-2000 kg/mm^2) and finely patterned with photolithographic technology. Hydrogenated amorphous silicon has electrical resistivity in its undoped state and is highly conductive when doped.

1.3 TFT Structures

The structure of thin film transistors is usually categorized as co-planar type or staggered type[12-14] as illustrated in Figure 1. Staggered structure was usually adopted in the fabrication of amorphous silicon thin film transistors while co-planar structure was usually adopted in the polycrystalline silicon thin film transistors. In the staggered structure, there is normal staggered structure, which is usually called "top-gate thin film transistors" and is shown in Fig. 1.1(b), and there are inverted staggered structures, which are as usually called "bottom gate thin film transistors" and are shown in Fig. 1.1(c) and (d). The inverted staggered structure is further categorized as inverted staggered tri-layer configuration (Fig. 1.1(c)) or inverted staggered back channel cut configuration (Fig 1.1(d)). Inverted staggered thin film transistors usually achieve better performance than staggered thin film transistor[15]. It is generally believed that the sequence of plasma enhanced chemical vapor deposition determines the interfacial property between amorphous silicon and silicon nitride, which to a large extent determine the performance of the device. Plasma enhanced chemical vapor deposition of silicon nitride using silane and ammonia as the source gas mixture inherently needs high rf input power to generate NH_n radicals[16]. And, this partially explains the better device performance of inverted staggered thin film transistors.

1.4 Silicon Nitride

PECVD silicon nitride (SiN_x) has been exclusively used in the fabrication of commercial amorphous silicon (a-Si:H) thin film transistor arrays for large area liquid

crystal displays. SiN_x is the preferred gate dielectric material for a-Si:H TFTs because it gives better device performance than other dielectric such as silicon dioxide. Compared with a TFT with SiN_x gate dielectric layer, TFT with SiO_2 in the dielectric structure has inferior switching characteristics because SiN_x gives better interfacial qualities[17]. However the reason is still not clear. SiN_x can be characterized according to its chemical properties, such as Si/N ratio, Si-H and N-H concentrations, or its characteristics, such as reflective Index, energy gap, dangling bonds, charge density, and stress. They all affect the transistor's threshold voltage, reliability, on-current and off-current. Good quality, i.e., high breakdown voltages and low leakage current, silicon nitride films can be deposited using SiH_4 and NH_3 gases or with the addition of N_2. It is well known that silicon nitride films deposited using SiH_4, NH_3, and N_2 gases at high substrate temperature (>250 ^oC) have good electrical properties. It was not clear, however, how N_2 affects the deposition process. Yue Kuo[12] suggested that N_2 has the effect of shifting the electron energy to high energy, thus promoting the dissociation of NH_3.

1.5 TFTs on plastics

The use of thin (10 - 200μm) plastic films as substrates for large–area a-Si:H thin film transistors (TFTs) arrays has attracted considerable interest recently[18, 19], because of the need for cheap, light-weight, unbreakable, and foldable computer screens as well as for large-area sensor arrays for imaging of non-planar (curved) surfaces. There have been reports on TFT fabrication at 110 °C on polyethylene terephtalate (PET)[20]. However, poyimides are a suitable class of substrates for the development of flexible devices, because of their compatibility with the temperature and vacuum processing requirements

of amorphous silicon technology in which all processing steps can be routinely carried out at temperatures below 300 °C. Most common polyimides are stable to temperatures approaching 400 °C. So polyimide film or web is being used as a flexible substrate for amorphous silicon ultra thin electronics in a developing technology[21]. A class of channel length (L) equal to 2-50 μm minimum feature size inverted gate thin film transistor circuitry has been demonstrated, including individual ratio (W/L) from 1 to 1000, inverters, drivers and receivers, ring oscillators, logic circuits and SRAM cells on 5 and 75 μm polyimide substrates[22-24]. The technology developed is compatible with roll-to-roll processing and mass production and demonstrates the feasibility of TFT based circuits on polyimide comparable to those on rigid substrates.

1.6 Electronic fibers and Textiles

Current state of the art in integrating electronics with ubiquitous or wearable systems involves starting with packaged integrated electronic components (ICs), interconnected with each other on a rigid or flexible printed circuit board, the latter providing better conformity to the body. Enclosing these circuit boards for protection from environmental effects by a protective material or casing is a common process. Still, even state of the art packaging techniques developed by product designers for wearable computing, fail to pass beyond “bricks” attached to the body. Some components on the other hand may have to stay as rigid structures that need to be integrated comfortably with body. In the case of ubiquitous computing, taking the media cup as an example, a complete

integration is not achieved since the electronics and the cup are two separate entities and the electronics need to be removed for washing the cup. There are also novel approaches towards integration of passive electronic components into objects, such as Post and Orth's[25]. They integrated conductive stainless steel fibers into textiles for the purpose of connecting circuit boards and point in the direction of a higher-scale integration. D. De Rossi et al.[26] used conductive polymer and conductivity changes on this coating as a function of strain and temperature were observed. A glove prototype made from this coated textile showed sensing and actuation capabilities embedded into a piece of textile. At the micro-scale, Drury et al. reported all polymer microelectronics devices fabricated on the flexible substrates at a low cost using organic semiconductors[27]. Given today's technology, it is possible to group the possibilities of the integration of (micro) electronics into clothing at three levels.

1) Garment level integration is the first level. At this level, the fundamental design of clothing and electronics are accomplished independent from each other and are combined at a later stage. A good example of this type of integration is the Philips-Levi's ICD jacket[28].

2) As a second level, the electronics is integrated into the garment. A good example of this level is circuit boards attached onto the fabric connected to each other using conductive threads[29]. Integration of electronic components, such as sensors and integrated circuits are also examples that can be included in this group[30]. This provides a relatively unobtrusive way of integrating electronic components into clothing.

3) Third level is fiber level integration. Part or all the necessary electronics and sensors are directly integrated into the fibers that make up the yarns. "Fiber" is

generically defining the geometry of a material having very long length compared to its cross sectional dimensions, i.e. a very high aspect ratio. Fibers are used in many different areas of industry, from textile to optics to advanced composite materials. Simplest example is naturally the textile in the form of clothes, curtains, table clothes or textiles of that sort. Today, fibers in the everyday objects have basically structural and aesthetic functions with a certain macrostructure and appearance. However, "fibers" can also have added functions in the context of "wearable computing" as previously recognized by Post, and Orth[25, 30]. In terms of the integration of computing power into clothes or entities of that kind, we share the vision that "eventually, whole computers might be made from materials people are comfortable wearing"[31]. The main concept of "Fiber Computing" is to embed the basic unit of computation, transistor, into fibers that make up the clothes we wear. These transistors then may be connected to form inverters, gates and higher level circuits.

1.7 Application for computational clothing

We use the term "computational clothing" to refer to clothing that has the ability to process, store, retrieve, and send information. These capabilities will allow clothing and clothing accessories to function as stand alone computers, to react to sensors in the environment, or to link to the World Wide Web and other networked systems. Most importantly, computational clothing will allow users to access the functionality associated with modern computational devices while conforming to traditional fashion trends. Clothing is often referred to as a "portable environment" or as a "second skin".

Wearable computer have great potential for military use, and there is currently great interest in what this device can do. There are several aspects of wearable computers (WC) that relate to their use in the military. They must be rugged, and applicable military standards exist. They may have docking stations, cradles or holsters for recharging, uploading/downloading information, providing communication, or for securing the device and preventing damage. Weight and cost are important. Finally, other features that arise from their mobility requirements include wireless communication and knowledge of current location. One of the commander's main requirements is communications. That is, he must advise subordinates of changes in mission, support, and threat; also, he must inform superiors of changes in threat or timelines. The wearable computer can simplify this procedure because communication can be facilitated by antenna arrays sewn into clothing associated with the WC, using a WC to update information. Position determination and map functions could be performed by the WC. Medical support and tactical internet application would be effective one.

The WC can provide the solution to a number of needs over the entire spectrum of healthcare delivery, both for personal (or patient) and user (physician or healthcare provider) applications. As an example, for prevention, the wearing of smart clothing that contains noninvasive microsensors can continuously monitor and updated information of a person, the medication status of a patient, or the amount of physical stress of an athlete.

1.8 Technical Challenges

1.8.1 Electronic fibers

High speed, high performance computation will continue to be dominated by silicon-based microelectronics for the foreseeable future. However, there are many applications that would benefit from the development of large area, lower performance distributed electronics, especially if the substrate were rugged, flexible, and inexpensive. As an example, military applications include active camouflage, inflatable decoys, large area sensors, large area emitters, large area actuators, etc. Regardless of so many potential applications, electronic textiles are not pervasive because there has been little or no work on the development of the building blocks to build even single devices. There are several challenges for this field.

1) Fibers need to be made out of suitable materials that will host the transistors and be flexible. The magnitude and frequency stresses make our clothing suffer especially during maintenance (such as washing).

2) Material selection is important issue for satisfying both adequate electrical (e.g. insulator) and mechanical properties (e.g. compliant). Though transistor fabrication on curved surfaces is not entirely new and several examples already exist[32, 33], the basic question is handling of fibers during fabrication and interconnections between the transistors.

3) Packaging is one of the critical challenges as it meant because of protecting the fiber and its circuits electrically, optically, and mechanically as well as giving textile

characteristics to the fiber. Packaging also certainly plays a crucial role in minimizing the stresses that the core fiber carrying the electronics will experience.

4) Reliability refers to an estimate for the ability of a system to function properly over time. Packaging and reliability are closely related. As fibers will be exposed to maintenance of the garments they are on, time dependent effects will be more significant. Therefore for reliability viewpoint, packaging should be well engineered to protect the fibers while maintaining necessary mechanical properties.

5) Integration of the computing fibers into the textile material and scalability are the factors need to be considered. In a digital clothing application, at the higher level, one can imagine applications where sensors or the processing done on the sensors are not fixed at the specific locations but they need to change over time. Cell matrix or a cell matrix like architecture can facilitate the implementation of wiring between sensors, logic elements, as well as processing of sensor data for presentation or decision-making.

The principle component of any active semiconductor device is the transistor. As a method to make smart fabrics, transistors need to be fabricated on flat yarn ribbons. There are three different semiconductors as potential candidates for transistors on threads; nanocrystalline silicon, amorphous silicon, and organic materials[34-37] including pentacene[38] (and derivatives). Nanocrystalline silicon is a thin film silicon material grown by plasma enhanced chemical deposition (PECVD). This is the deposition technique used widely for making amorphous silicon films. When PECVD is run using silane (SiH_4) source gas diluted in excess hydrogen, the deposited film begins growing amorphous but then develops crystals that are up to ~50nm in size. There has been great interest in organic semiconductor materials composed of molecules such as sexithiophene

derivatives[34-36] and pentacene[37] for organic thin film transistors (TFTs), due to their high field effect mobilities observed in these materials and due to intermolecular interactions which lead to larger grain sizes and fewer grain boundaries, facilitating charge transport[37, 39, 40]. Pentacene films deposited from solution are polycrystalline with grains randomly oriented. The mobility in these films is limited by charge trapping at grain boundaries[41]. The basic distributed architecture of fabricating TFTs on strips and conductive threads can be driving materials for the circuit architecture by stacking them on each other. This device architecture impacts the circuit styles we use for implementation of logic primitives such as inverter, NOR and NAND gates. Other circuit primitives such as adders, latches, flip-flops, multiplexers and demultiplexers would be configurated using the basic NOR, NAND and inverter gates.

1.8.2 Challenges in TFTs

TFT on flexible substrates is a basic building block of our approach. There are several issues for TFT performance and addressing TFTs with conductive yarns. Two major performances of TFT are the threshold voltage and the mobility. The threshold voltage of a-Si:H TFT is related with the defect density of a-Si:H, the interface density around the Fermi level between SiN_x and a-Si:H, and the charge in the SiN_x. The mobility of a-Si:H TFT is related with the band tail states of a-Si:H, the n+ ohmic contact, the thickness of undoped a-Si:H layer and the SiN_x/a-Si:H interface. Among these, a-Si:H/gate dielectric interface, a-Si:H, and SiN_x bulk film qualities are key factors affecting TFT performance. Hydrogen is an important element in thin film transistor (TFT). Since a-Si:H and SiN_x films are usually prepared by the PECVD method using SiH_4 chemistry, a-Si:H and SiN_x

contain approximately 10 and 30 percent of hydrogen, respectively. In a-Si:H and SiN_x film process H_2 and NH_3 are included in the feed stream which is an additional hydrogen source for these films. The main function of hydrogen in TFT is to passivate silicon and nitrogen dangling bonds that are charge trapping centers. Plasma hydrogenation process can improve TFT characteristic by the interface hydrogen step. However, the mechanism of the hydrogenation isn't still well explained. Since a-Si:H is a field effect transistor, the transistor behavior is greatly influenced by a thin electron accumulation layer induced at the interface of gate SiN_x and a-Si:H. The interface morphology and electrical properties are critical to TFTs. A PECVD process contains particles of various forms and energy (e.g., atoms, molecules, radicals, and ions) and short wavelength light. These parameters affect the film's morphology, surface states, and band structure. In order to prepare a high performance TFT, properties including morphology, chemical structure, physical band energies, density of states, and stress mismatch have to be optimized. Films deposited by plasma enhanced chemical vapor deposition (PECVD) are affected by gas composition and deposition conditions such as RF power, temperature, and pressure. Though it was mentioned in Chapter 1.5 that polyimide film can be processed up to 400^{o}C, thermal responses of polyimide film and silicon nitride film are very different, i.e. polyimide film shrinks upon heating, for example 0.1% for 200ºC 30min and has a thermal expansion coefficient of 20 x 10^{-6}/ºC while the thermal coefficient of silicon nitride film is 1.5 x 10^{-6}/ºC. Also, the stress of silicon nitride film varies with nitride film deposition composition and temperature[16, 42]. The total stress in the system is also influenced by the stress in the polyimide substrate. Upon heating, the polyimide film will tend to shrink due to release of built-in tension during film fabrication. The changes in substrate size

result in a net compressive stress at the substrate/SiNx interface. The stress difference between polyimide film and the silicon nitride will likely lead to defects at the interface, and could lead to film delamination (as shown in Figure 2). So, the effect of temperature on the substrate, and on the deposited film composition, is a significant issue for TFT fabrication on plastic substrates.

Another important issue is the method of interconnecting TFT's on adjacent fibers within a woven network. To obtained reliable interconnection, issues related to thread/thread and thread/TFT contact resistance should be characterized and understood.

1.9 Summary

The demand for wearable or potable electronic circuits is growing but weaving approach in fabric level with TFTs on plastic film and conductive yarns has not been tried. In this work, a-Si:H TFTs were fabricated on 125 μm polyimide film using back channel cut inverted staggered TFT structure. The gate insulator of SiN_x has been studied with various deposition conditions. It was shown that the PECVD deposition temperatures are related to the bulk and interface charges of the films. NH/SiH ratio in silicon nitride film was characterized by charges in films. TFTs for smart fabric were made with low temperature SiN_x, and a-Si:H having acceptable mobility and threshold voltage. Finally, unique woven electronic circuits were demonstrated with TFTs on polyimide and conductive yarns.

Chapter II.

Experimental

2.1 Materials Preparation

2.1.1 Silicon nitride capacitors

A capacitively coupled rf (13.56 MHz) PECVD system was used for the deposition of various silicon nitride films. The electrode area is 30 x 35 cm^2 with a spacing of 3 cm. The system is capable of depositing uniform nitride films over 900 cm^2. The process gases were introduced through a showerhead array of 0.5 mm-diameter orifices in the rf-powered electrode. N-type silicon wafers were used as substrates, and their resistivities are about 1.0 Ohm·cm. Wafers were cleaned by the JTB Baker solution and 1% HF solution before being loaded into the reactor. For silicon nitride characterization experiments, 1) processing gases composition and 2) substrate temperature effects on the properties of the nitride films were studied. For 1) processing gas composition effect experiment, substrate temperature was kept at 150^oC or 250^oC, and processing pressure was kept at 0.4 Torr. RF power was also kept at 150W. Processing gases composition was controlled with changing NH_3/SiH_4 ratio while N_2 was constant at 575 standard cubic centimeters per minute (sccm). The summary of the deposition conditions for gas composition effect experiments is shown in Table I. For 2) substrate temperature effect experiment, processing gas composition was kept at $NH_3/SiH_4/N_2$=7.5/75/575. Both processing pressure and RF power were kept at 0.4 Torr and 150W, respectively. Substrate temperatures were 50, 150, 250, and 350^oC. The summary of deposition conditions for substrate temperature effect experiment son silicon nitride films is shown in Table II. For the characterization of the nitride films, Metal-Insulator-Semiconductor (MIS) structure was used. As the metal for the capacitor, Aluminum (Al) was deposited

by evaporation with thickness 2000 Å. For patterning Al, shadow masks whose area is ~7 x 10^{-4} cm^2 were used during evaporation of Al.

2.1.2 TFTs fabrication

The fabrication steps for TFT for woven circuits with conductive yarns are shown in Figure 3. Parallel plate rf (13.56 MHz) PECVD reactor (Figure 4) was used to deposit intrinsic amorphous silicon, doped a-Si:H, and silicon nitride layers at 250 ºC to form good quality TFT devices on polyimide film substrate. In the TFT structure, the n+ doped contact layer was formed using 1% phosphine in silane, also with hydrogen dilution. Silane/nitrogen/ammonia mixtures were used to form the insulating silicon nitride layers. TFTs were prepared on 4 x 4-inch 125 μm VN type Kapton® substrates. 2000 Å of aluminum was deposited first and patterned to form the gate. Before aluminum deposition, ultrasonic pre-cleanings with 10 minutes acetone were done. To assure the adhesion of aluminum to the Kapton® substrates, a base pressure of $2x10^{-6}$ Torr is necessary in the evaporator chamber before the aluminum deposition. The gates were patterned by conventional photolithography using printed emulsion mask, and wet etched. Then, trilayer including gate nitride, amorphous silicon, and top n+ doped silicon (3000Å/1000Å/500Å) were deposited by PECVD in a single reactor with a large electrode area (30cm x 35cm) capable of processing up to two 4x4 inch simultaneously without breaking vacuum. The chamber pressure < $2x10^{-6}$ Torr was achieved before the deposition of each layer. Substrate temperature was held at 250 ^oC and processing pressure was held at 0.4, 0.4, 1.5 Torr, respectively for gate nitride, amorphous silicon, and doped silicon layer. RF power was 150 W for SiN_x and 50 W for a-Si:H, doped n+

Si:H. Silane with a flow rate of 50 standard cubic centimeters per minute (sccm) and 500, 1500 sccm of hydrogen were used for a-Si:H and n+Si depositions, while a combination of 575 sccm nitrogen, 5 sccm silane, and 75 sccm ammonia was used for SiN_x deposition. The dielectric constant of SiN_x was calculated from the characteristic curve of displacement current versus applied voltage in MIS structures. Processing parameters for doped n+ a-Si:H are same as intrinsic a-Si:H deposition except the silane gas used for processing contained 1 percent of phosphine. After n+ deposition, positive photoresist of one micrometer is applied on top of the trilayer, and ultraviolet light of 275 W is then shined through the printed emulsion mask. After developing the photoresist, reactive ion etch (RIE) was used to form active transistor island area. The RIE process included SF_6 and O_2 gases. For RIE etching, operating pressure was 60mTorr, RF power was 100W and Temperature was 20 °C. Etching time for a-Si islands using first mask was 2 min 15 second and 27second for a-Si channel patterning. The following step is contact metal deposition (Al). Deposition conditions are same as those of gate Al but evaporation time. A base pressure of $2x10^{-6}$ Torr is necessary in the evaporator chamber before the aluminum deposition. The contact Al having fin patterns was patterned by conventional photolithography using printed emulsion mask, and wet etched by H_3PO_4, HNO_3 and CH_3COOH mixed aqueous solution. Without removing photoresist, n+Si:H was etched by reactive ion etch (RIE) processed with SF_6 and O_2 gases in order to make source/drain of transistors. An oven anneal under nitrogen gas ambient was applied. In order to inhibit the effusion of hydrogen, the annealing was performed at a lower temperature that that of tri-layer deposition. Two hours annealing at 150 ºC was found to be suitable to remove moisture that effects device testing.

2.2 Materials Characterization

To charaterize silicon nitride layer, FT-IR (Foulier Transform-Infrared) spectra absorption, Capacitance-Voltage, and Current-Voltage measurement were performed.

2.2.1FTIR measurement

Samples deposited on high resistivity (> 10 Ohm ·cm), double-side polished Si (100) substrates were used to perform infrared spectroscopy analysis. The spectra were collected in the transmission mode with a 4 cm^{-1} resolution using a Nicolet Magma 750. Absorption coefficients can be calculated from absorbance values after subtracting the baseline. No spectral deconvolution was performed.

2.2.2 Electrical characterization

For Capacitance-Voltage (CV) and Current-Voltage (IV) measurement, MIS (Metal Insulator Semiconductor) structures were used. For IV measurement, the gate biased positively, and the ramp rate was 5V/s. For CV measurements, the samples are initially biased to –3 MV/cm and illuminated for 1-2s to create an inversion layer at the substrate/silicon nitride interface. The creation of the inversion layer eliminates deep depletion in the substrate and insures that majority of the applied voltage is dropped across the insulator. Dielectric constants of silicon nitride films can be extracted using an equation as follows:

$$C_{nitride} = \frac{\varepsilon_o \varepsilon A}{d} \quad (1)$$

$C_{nitride}$ is the capacitance read from the capacitance meter, A is the area of the test dot, d is the thickness of the silicon nitride film, ε_o is the permittivity of vacuum, and ε is the dielectric constant. The dielectric constants for silicon nitride films deposited at 150 ^oC, 250 ^oC using SiH_4, NH_3, N_2 gases was calculated from C_{ox} obtained by CV measurement. The dielectric constants for the films deposited at 150 ^oC ranged 3.0 to 5.0. The dielectric constants for the films deposited at 250 ^oC ranged 6.0 to 8.0.

2.3 TFT Characterization

Thin film transistors were characterized using an HP 4145A analyzer by 1) drain current versus gate voltage (I_d-V_g), which is usually plotted as log (I_d) vs. V_g; and 2) drain current versus gate voltage (I_d-V_d). TFT's parameters, i.e., threshold voltage, effective linear mobility, saturation mobility, and subthreshold slope are extracted from I_d-V_g measurement. Effective linear mobilities are extracted using the following equation:

$$\mu_{eff} = \frac{L}{W} \cdot \frac{1}{C_i} \cdot \frac{1}{V_d} \cdot \left(\frac{dI_d}{dV_g} \right) \tag{2}$$

where μ_{eff} is the effective linear mobility, L is the channel length, W is the channel width, and C_i is the capacitance of the gate insulator per unit square (cm^2). V_d is kept at 0.1V in measuring the effective linear mobility. To determine the threshold voltage of a thin film transistor, we draw a straight line with the maximum slope on the I_d-V_g curve, where the drain voltage axis is the threshold voltage of the measured thin film transistor. The saturation mobility of a thin film transistor can be extracted from I_d-V_d

curves while keeping V_g=V_d. The expression used to calculate the saturation mobility is as follows:

$$\mu_{sat} = \frac{2L}{W} \cdot \frac{1}{C_i} \cdot \left(\frac{d\sqrt{I_d}}{dV_g} \right)^2_{V_g=V_d} \quad (3)$$

μ_{sat} is the saturation mobility of the measured thin film transistor. The subthreshold slope of a thin film transistor can be extracted from log (I_d) vs. V_g plots. To measure the subthreshold slope (equation 4), draw a straight line on log (I_d)-V_g curves for Vg=0~5V. The inverse of the slope of this straight is the subthreshold slope, and the unit of the subthreshold slope is V/decade.

$$S = \frac{dVg}{d(\log I_D)} \quad (4)$$

The threshold voltage and the subthreshold slope are an indication of the density of states around Fermi-level in the interface between the a-Si:H and a-SiN_x layers.

2.4 Weaving TFTs and Conductive yarns

Contact resistance was measured as the deviation from this behavior when two strips are contacted. Materials for contact experiment are aluminum (Al), gold (Au) and carbon fiber. Al film is 8% thinner than the Au Film. To compare contact resistance, resistance

was measured by distance variation with various metal contact. General volt-meter was used for measuring device. Pressure was applied at Al strip contact point. Contact resistance was extracted from equation (4).

$$R_T = \frac{\rho d}{A} + R_C \tag{5}$$

R_T, R_C, ρ, A and d are total measured resistance, contact resistance, resistivity of metal, area of contact and distance.

TFTs prepared on Kapton® film was weaved with conductive thread. Fin areas in the top view of TFTs were prepared for sewing TFT and threads (Figure 5), while maintaining contact for source and drain. By designing unique masks design (Figure 6) and processing (Figure 3), TFT structure can prevent from short with contact and gate. To apply TFT on Kapton® to general electronic circuits, by using sewing method, Inverter and NOR gate were prepared. The Inverter and NOR gate are shown in Figure 7.

Material analysis was done in collaboration with the TFT processing team in Prof. Parsons Lab. Specifically, Leonard Nelson performed contact resistance experiment, Kevin bray performed conductive thread interconnection experiment, mask design, and Dr. Laura smith designed circuits using conductive threads and TFTs. My primary work involved film deposition, MOS fabrication and characterization, and TFT processing and characterization. I also independently developed the primary focus of this thesis, which includes numerical characterization of the thickness dependent CV data to independently analyze bulk and interface charge defects in SiN_x/Si structures.

Chapter III.

Results and discussion

of TFT materials and devices

3.1 Effects of deposition conditions on the properties of SiN_x

3.1.1 Infrared absorption results

The effects of substrate temperature and source gas composition were investigated in relation to silicon nitride film structure. The infrared absorption spectra of silicon nitride film deposited with various NH_3/SiH_4 ratios at 150°C and 250°C are shown in Figure 8 and 9, respectively, and Figure 10 shows the infrared absorption spectra for various temperatures when NH_3/SiH_4 ratio is fixed at 10/1. Peaks of infrared absorption are assigned as follows, 1) N-H stretching mode at 3300 cm^{-1}, 2) Si-H stretching mode at 2140 cm^{-1}, and 3) N-H_2 scissors at 1550 cm^{-1}. The integrated absorption of N-H and Si-H stretching bands are correlated with the atomic concentration of hydrogen, which were calculated using the method proposed by Lanford and Rand[43]. Figure 11 shows the NH/SiH ratio obtained from the spectra in Figures 8, 9 and 10 plotted vs. NH_3/SiH_4 gas phase ratio. The figure shows that the NH/SiH ratio increases with increasing NH_3/SiH_4 ratio, and the trend is similar for films deposited at 150 and 250°C. This trend is consistent with other group's work[44, 45]. Figure 11 also shows that NH/SiH ratio increases with increasing N_2 flow rate. This suggests that nitrogen dilution has an 'extra' effect of enhancing the NH/SiH ratio of nitride film. Yue Kuo[46] concluded that nitrogen acts as an energy booster, which enhances dissociation of both SiH_4 and NH_3 Figure 12 (a) shows NH/SiH ratio and total hydrogen concentration, [H], calculated from the data in Figures 9 plotted vs. NH_3/SiH_4 flow ratio, and Figure 12(b) shows a similar plot of NH/SiH and [H], calculated from the data in Figures 10 plotted vs.

substrate temperature. We note that the total hydrogen content is sensitive to temperature but independent of flow ratio, whereas the NH/SiH ratio is sensitive to flow ratio but not temperature. The decrease [H] with temperature is likely linked to the fact that the deposition rate tends to decrease with increasing temperature, as shown in Figure 13.

3.1.2 Electrical results

The silicon nitride films described above were also electrically characterized. Figure 14 and 15 are logarithmic plots of current density versus electric field measured at room temperature for nitride films deposited at 150°C and 250°C, respectively, with different NH/SiH ratios. Figure 14 and 15 show that leakage current generally decreases with increasing NH/SiH ratio for films deposited at 150 and 250°C. Figure 16 is current vs. voltage for silicon nitride films deposited with different temperature for a fixed NH_3/SiH_4 ratio (ratio = 10), corresponding to a fixed NH/SiH ratio in the films (NH/Si-H ≈ 1). It is interesting to note that the leakage current between 4 and 10 MV/cm appears to improve with decreasing substrate temperature. Capacitance-Voltage analysis was also performed on these films, and results are shown in Figures 17-20. Figure 17 and 18 show the effect of NH/SiH ratio on flatband voltage for films deposited at 150 and 250°C respectively. We find that the flatband voltage is shifted negative from the expected V_{FB} (-0.04 V for Al gate electrodes) for both 150 and 250°C films, the negative shift generally increases with an increase in NH/SiH ratio. One exception is the curve for NH/SiH = 3.54 in Figure 17, where the flatband shift is less

than for the film with NH/SiH = 1.0. Figure 19 is capacitance versus voltage for different temperatures at NH_3/SiH_4 =10. All films show negative shift, consistent with positive fixed charge, but the magnitude of the shift decreases with decreasing film deposition temperature. Figure 20 (a) and (b) show CV curves for films deposited at 150 and 250°C. The hysteresis sweep direction (negative ΔV_{FB}) indicates that holes were injected into the nitride from the substrate and trapped during the CV cycle. The total trapped charge in the dielectric layer can be estimated from the CV flatband voltage shift using equations (6) and (7)[47].

$$\frac{C_{FB}}{C_{OX}} = \frac{1}{1+\frac{136\sqrt{T/300}}{t_{OX}\sqrt{N_A}}} \tag{6}$$

In equation (6), C_{FB} is flatband capacitance, and N_A is the substrate doping concentration. Equation (6) gives us the point on the CV curve (relative to C_{ox}) that corresponds to flatband. We then use the value of C_{FB}/C_{OX} to read V_{FB} from the CV curve, and input V_{FB} into equation (7) to obtain Q_T.

$$Q_T = \frac{(\phi_{MS} - V_{FB})K_{OX}\varepsilon_o}{t_{OX}} \tag{7}$$

In equation (7) V_{FB} is flatband voltage, Φ_{MS} is work function difference between metal and the semiconductor, K_{ox} is nitride dielectric constant obtained by C_{ox} from CV measurement, and t_{ox} is the nitride physical thickness. Note that Q_T is the net charge

density in the film, corresponding to a sum of the positive and negative fixed and bulk charge. If positive and negative charges are present in equal amounts (i.e. negative at the interface and positive in the film bulk), then the net charge density, Q_T, will be zero. Bulk and interface charges can be deduced by measuring the thickness dependence of V_{fb}, as discussed below.

Results of total net charge density obtained from the CV data in Figures 17 and 18 are shown in Figures 21. Figure 21 shows the total charge density plotted vs. NH/SiH ratio. The smallest charge densities are observed at low NH/SiH, but these films show high leakage in the IV traces (Figures 14 and 15). The highest charge densities are observed for NH/SiH near 1.0, with decreasing net charge as NH/SiH increases above 1. Note that the net charge density increases somewhat with increasing substrate temperature.

By characterizing the thickness dependence of CV curves and flatband voltage shifts, the total charge distribution (i.e. interface vs. bulk charge) can be determined. For a fixed charge density in a film, increasing the film thickness leads to an increase in the total charge, and therefore an increase in the V_{FB} shift. However, if the charge density is located primarily at or near the silicon/dielectric interface, increasing film thickness will not change the total charge density. However, we still expect a change in V_{FB} with thickness because C_{ox} changes as film thickness changes. Therefore, considering bulk (Q_{BC}) and interface (Q_{IC}) charges, the measured flatband voltage will change with thickness as given in equation (8)[47].

$$V_{FB} = \phi_{MS} - \frac{Q_{IC}}{K_S \varepsilon_o} t_{OX} - \frac{Q_{BC}}{2K_S \varepsilon_o} t_{OX}^2 \qquad (8)$$

This relationship holds only for Q_{BC} distributed uniformly through the film bulk. Figure 22 and 23 show CV curves measured at various film thicknesses ranging from 400 to 1500 Å. Figure 24 (a) shows the effect of film thickness on V_{FB} obtained from CV analysis for films deposited with various NH/SiH ratios at 150°C. Figure 24 (b) is a similar set of plots for films with NH_3/SiH_4 = 10 (i.e. NH/SiH ≈ 1.0) deposited at temperatures between 50 and 250°C. The flatband voltage changes with thickness in both plots, and the resulting numerical fits of the data to equation (8) are shown in Figures 24 (a) and (b). Values for Q_{IC} and $Q_{BC} \cdot t_{ox}$ are extracted from the fits and results are shown in Figures 25 and 26. To make the units consistent, Figures 25 and 26 show plot of Q_{IC} and $Q_{BC} \bullet t_{ox}$ assuming t_{ox}=1000Å. This value of thickness was chosen to be consistent with the data in Figure 21. Error bars obtained from the quality of the fits are also included.

Figure 25 shows Q_{IC} and Q_{BC} vs. NH/SiH ratio for films deposited at 150°C. At the lowest NH/SiH ratio measured, Q_{IC} and $Q_{BC} \bullet t_{ox}$ have a similar magnitude, but interface charge is negative, whereas the bulk charge is positive. This is consistent with the small total net charge observed in films with small NH/SiH (shown in Figure 21). Increasing NH/SiH results in a change in sign for both bulk and interface charge. At NH/SiH near 1.0, bulk and interface charge are both positive, but increasing NH/SiH leads to less positive and more negative charge in the film bulk, and more positive charge at the film interface. This leads to a decrease in the net total fixed charge, even

though the interface charge is becoming more positive and the bulk charge is becoming more negative with increasing NH/SiH. Figure 26 shows the effect of temperature on Q_{IC} and Q_{BC}•t_{ox} for films with NH/SiH ≈ 1. At this bonded hydrogen ratio, increasing deposition temperature leads to more positive interface charge density, and more negative bulk charge density. The net charge density is relatively insensitive to temperature, consistent with Q_T at different temperatures in Figure 21.

From a comparison of equations (7) and (8), we expect that the net charge density Q_T will correlate with the sum of Q_{IC} and Q_{BC}: $Q_T = (Q_{IC} + Q_{BC}•t_{ox}/2)$. Using this relation, Q_T values can be obtained from the data in Figures 25 and 26. From Figure 25, Q_T is found to increase upto NH/Si-H ≈ 1, then decrease. The trend is the same as the data for Q_T shown in Figure 21, measured directly from the CV curves for the 1000Å thick films. At NH/Si-H =1, the magnitude of Q_T from Figure 25 is approximately ½ of that found in Figure 21. The consistency of these results is good, considering that these two analyses came from different sets of data and different analysis approaches.

3.1.3 Discussion

3.1.3.1 Effect of Deposition Conditions on Film Composition

As shown in Figure 10, increasing substrate temperature results in a decrease in NH and SiH peak height, and an increase in Si-N peak intensity, consistent with a thermally driven release of hydrogen from the growth surface. Figure 12 (b) shows that NH/SiH ratio remains constant while total hydrogen concentration decreases with increasing

temperature. Even though the NH/SiH ratio stays constant it is likely that the N/Si ratio changes with deposition temperature. Increasing temperature is expected to enhance NH_3 evolution from the growth surface (see Figure 27 and discussion below), leading to a decrease in N/Si ratio in the film. The decrease in N may account for the increase leakage current with increasing temperature seen in Figure 16. Deposition rate decreases with increasing temperature as shown in Figure 13. We believe that deposition rate decreases because more ammonia is released with increasing temperature (Precursor sticking coefficient with increasing substrate temperature decreases and it may contribute to decrease the deposition rate). However, exact mechanism for deposition rate decreasing is still not well understood.

3.1.3.2 Bulk and Interface Charge, and Effect of Film Stress

The data in Figures 14 and 15 indicate that at 150 or 250°C, increasing the NH/SiH ratio decreases the apparent leakage current in the films. Charge transport in silicon nitride follows the Frenkel-Pool mechanism[48], where charge hops between defect sites in the bulk film. Therefore, we expect the bulk and interface charges in the films to have a pronounced effect on apparent leakage current. From the data in Figure 25, increasing NH/SiH leads to more positive interface charge and more negative bulk charge. Therefore, it is likely that the decreased apparent leakage current observed for large NH/SiH films is related to charge screening effects, where the charge in the film decreases the field dropped across the dielectric, and is not only due to an improvement in film insulating quality.

It has been reported[49] that as NH/SiH or N/Si ratio increases, the SiN_x film structure changes and converts from a more tetrahedral network (Si rich) to a Si_3N_4-like network. Films with a Si_3N_4-like network structure shows improved insulating properties over the Si-rich tetrahedral network, and SiN_x lattice distortion decreases as nitrogen content increases in the nitride film[49]. This is consistent with the data in Figures 14 and 15, which show a decrease in leakage with increasing NH/SiH.

It is important to note that the decrease in apparent leakage with increasing NH/SiH likely results from two mechanisms: 1) a improvement in film structure as the film becomes less Si-rich; and 2) an increase in fixed charge leading to an increase in the field screening effect. The field screening effect results from charge in the dielectric layer that effectively reduces the voltage drop across part of the dielectric layer, leading to a decrease in current leakage. The data in Figure 17, for example, where the flat band voltage is shifted more positive for NH/SiH = 3.54 can be understood in terms of compensation of positive interface and negative bulk charge in the film. Also, the bulk charges switch from positive to negative when NH/SiH is above 2.0 (shown in Figure 25). We believe that as NH/SiH increases, the larger electronegativity of N over Si may lead to the increase in negative charge centers.

Generally, higher temperatures are associated with improved transport properties. However, Figure 16 show that leakage current increases as substrate temperature is increased, and Figure 19 shows that the flatband voltage shifts more negative with increasing temperature, indicating an increase in the total charge density (shown in Figure 21). Data in Figure 26 shows that as the substrate temperature increases, the interface charge becomes more positive, and the bulk charge becomes more negative.

The increase in the number of charge states may relate to an increase in defect states for hopping, leading to an increase in charge leakage consistent with a decrease in N/Si ratio as discussed above. The fact that the increased charge is compensated (bulk charge is negative, interface charge is positive) suggests that as substrate temperature changes charge screening effects are less important than the effects of composition change under the conditions studied. We believe that the tensile stress increases with substrate temperature, resulting in increasing the interface charge density. Interface stress is expected to depend on details of the interface formation reactions, as discussed below.

Optimum dielectrics for transistor applications should minimize Q_{IC} and Q_{BC} to decrease charge scattering during transport along the semiconductor/dielectric interface. Therefore, the effects of film structure and bulk and interface charge need to be balanced to determine the optimum material processing conditions for devices. If we consider conditions that minimize the sum of the absolute magnitudes of positive and negative charge (as shown in Figure 25 (b)) then at 150°C, films with composition near NH/SiH ~1 may show the best device results.

We believe that the interface charge density observed in these materials is related to film stress at the Si/SiN_x interface built in during film deposition. The stress is believed to develop because the nitride film densification occurs in a chemical "condensation zone" which extends below the surface as illustrated in Figure 27[44]. Elimination of volatile species (ammonia) from the heated substrate creates dangling Si and N bonds separated by voids within which stretched Si-N bonds then form. These bonds cannot be relaxed as they would at the surface because they are constrained by the surrounding

structure, so the stress is frozen in. Results in the literature indicate that the stress in SiN_x:H films changes monotonically from strong compressive to strong tensile with increasing N/Si ratio (Figure 28)[42], resulting in a bigger stress mismatch, consistent with the data in Figure 25. Results presented here were measured for films deposited on crystalline silicon, whereas actual devices will utilize amorphous silicon or other semiconductors. The a-Si:H films is expected to have built-in compressive stress[50-53] which will enhance the effect of interface stress in actual devices. It is clear that a better understanding of interface stress, charge scattering, and flatband voltage shifts will be needed to improve TFT device performance.

3.2 TFT Performance

Thin film transistors were characterized using an HP 4145b device analyzer. The results of the analysis of a single "typical" device are shown in Figure 29-31. The channel width and length were 100 and 100μm, respectively. Figure 29 shows the log of the drain current versus gate voltage. The subthreshold voltage swing is ~ 5.5 V/decade. Figure 30 is a linear plot of the drain current versus drain voltage, and no evidence for current crowing is observed at low drain voltages. Linear best fits to the data in Figure 31 (a) and (b) give the linear and saturation mobilities, respectively. In Figure 31 (a), the source-drain voltage is held 10 V and the linear mobility is 0.026 $cm^2/V•s$ with 7-V threshold voltage. In Figure 31 (b), the gate voltage and drain are help at the same potential, and the saturation mobility is 0.059 $cm^2/V•s$ with 2.5-V threshold voltage. A total 12 devices on the on array were probed at random and

analyzed. All devices showed similar behavior, with saturation mobility of an average $0.059 cm^2/V•s$. A similar distribution with slightly lower values was found for the linear mobility.

Chapter IV.

Application to woven electronics

-Woven circuits with TFTs and Conductive yarns

TFTs made on Kapton® having special contact pad structure is the building block for integrated circuit on clothing. Metal contact during weaving is a significant issue. We did some experiments to understand the interconnection issues. Gold, Aluminum, and Carbon Fibers exhibit linear resistance vs. distance behavior. Kapton® strips with gold film exhibit the lowest contact resistance (Figure 32~33). Aluminum coated Kapton® and carbon fibers have high contact resistances unless pressure is applied at the contact point. 3-Dimensional weaving did not provide sufficient contact pressure for reliable conduction at contacts between carbon fibers and aluminum coated Kapton®. Poor contacts exhibited a large amount of data scatter as well as high resistance. Figure 34 shows that resistance vs. distance for two contacted Kapton® strips, i.e. gold films and Kapton® films. The data of resistance of aluminum coated Kapton® without any pressure was scattered, which means high resistance. We believe that this is because aluminum has thin natural Al_2O_3 layer which has very poor conductivity, while gold film doesn't have oxide layer. So without pressure the thin oxide layer played a critical role for conductivity. Once films have pressure on contact point, it seems that the oxide layer can't prevent electron moving between two aluminum layers. Resistances measured from materials sewed with aluminum coated Kapton® and various conductive threads which are silver impregnated nylon, single strand steel yarn, two ply steel yarn, gauge copper yarn and polypyrrole coated PET (polyethylene terephthalate) are shown in Figure 35. Steel yarns have excellent conductivity, when conductive polymer showed the worst conductivity. Figure 36 is the logic application of the inverter

circuit logic from TFT's and conductive threads. Figure 37 is actual inverter woven with TFT's and silver impregnated nylon yarns. Figure 38 shows masks design set #2 with contact pads for sewing TFT's and conductive threads. We found that mask design #2 set have a large area (~0.5 cm^2) overlap of gate aluminum and source/drain aluminum and that area is separated by silicon nitride layer only. Current-Voltage testing of Metal-Insulator-Metal structure capacitor having same area with our TFT fabricated with mask design #2 structure showed large current leakage current as seen in Figure 39 (b). Figure 39 is a plot for electric field versus current density for Metal-Insulator-Metal (MIM) structure. Figure 39 (a) is a plot for electric filed versus current density for MIM structure capacitor having ~$7x10^{-4}$ cm^2. For small area overlap of gate metal and contact metal, leakage current increases as the nitride thickness decreases seen in Figure 39 (a). However, Figure 39 (b) shows a large area (~0.5 cm^2) MIM structure causes a large leakage current in even 6500 Å nitride. To reduce gate/contact overlap, we redesigned our mask set. The redesigned mask set #3 is shown in Figure 40.

Chapter V.

Conclusion

An extensive study of silicon nitride deposited using plasma enhanced chemical vapor deposition (PECVD) with various substrate temperatures and processing gas compositions was presented. By Infrared absorption analysis, we have shown that NH/SiH ratio increases at 150^{o}C and 250^{o}C as processing gas ratio NH_3/SiH_4 increases. Also, we have shown apparent leakage current decreases as NH/SiH ratio increases. It was proposed that the decrease in apparent leakage current with increasing NH/SiH ratio was related to charge screening effect as well as film improved insulating quality. It was shown that increasing NH/SiH leads to more positive interface charge and more negative bulk charge. The interface charge and bulk charge densities for SiN_x films with different processing gas composition have been calculated. The interface charge density increases with increasing NH/SiH causing flatband shift and increasing total charge density. It was believed that the interface charge is mainly generated by stress build up at Si/SiN_x interface and increases with NH/SiH ratio.

To study substrate temperature effects on the SiN_x structure and charges variation, Infrared absorption analysis, Current-Voltage analysis, and Capacitance-Voltage analysis were performed. We found that as substrate temperature increases the NH/SiH ratio remains constant, the apparent leakage current increases and the flat band voltage shifts. Because the net total charge is compensated as substrate temperature changes, charge screening effects were believed to be less important than effects of composition change under the conditions studied.

From silicon nitride characterization, we selected proper silicon nitride film composition and temperature having low leakage current and relatively low shift in flat band voltage for thin film transistor (TFT). TFTs are fabricated successfully on

polyimide film substrate using silicon nitride, a-Si and n+Si layer with a back channel cut inverted staggered structure. Contact resistances with several conductive materials for weaving were compared. A unique method of using TFT on plastic film and conductive yarns for smart fabric was demonstrated. Although a need for improvement, we show a new approach in computational clothing field.

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Table I. Deposition conditions for processing gas composition effect experiments on silicon nitride films

(a) 150 ^{o}C

	N_2 (sccm)	NH_3 (sccm)	SiH_4 (Sccm)	Temperature (^{o}C)	RF Power (W)	Pressure (Torr)
TF23	575	75	20	150	150	0.4
TF24	575	75	10	150	150	0.4
TF26	575	75	7.5	150	150	0.4
TF27	575	75	5	150	150	0.4

(b) 250 ^{o}C

	N_2 (sccm)	NH_3 (sccm)	SiH_4 (Sccm)	Temperature (^{o}C)	RF Power	Pressure (Torr)
TF1	575	75	20	250	150	0.4
TF2	575	75	10	250	150	0.4
TF3	575	90	10	250	150	0.4
TF4	800	90	10	250	150	0.4

Table II. Deposition conditions for substrate temperature effect experiments on silicon nitride films

	N_2 (sccm)	NH_3 (sccm)	SiH_4 (Sccm)	Temperature (^oC)	RF Power (W)	Pressure (Torr)
TF39	575	75	7.5	50	150	0.4
TF26	575	75	7.5	150	150	0.4
TF46	575	75	7.5	250	150	0.4
TF49	575	75	7.5	350	150	0.4

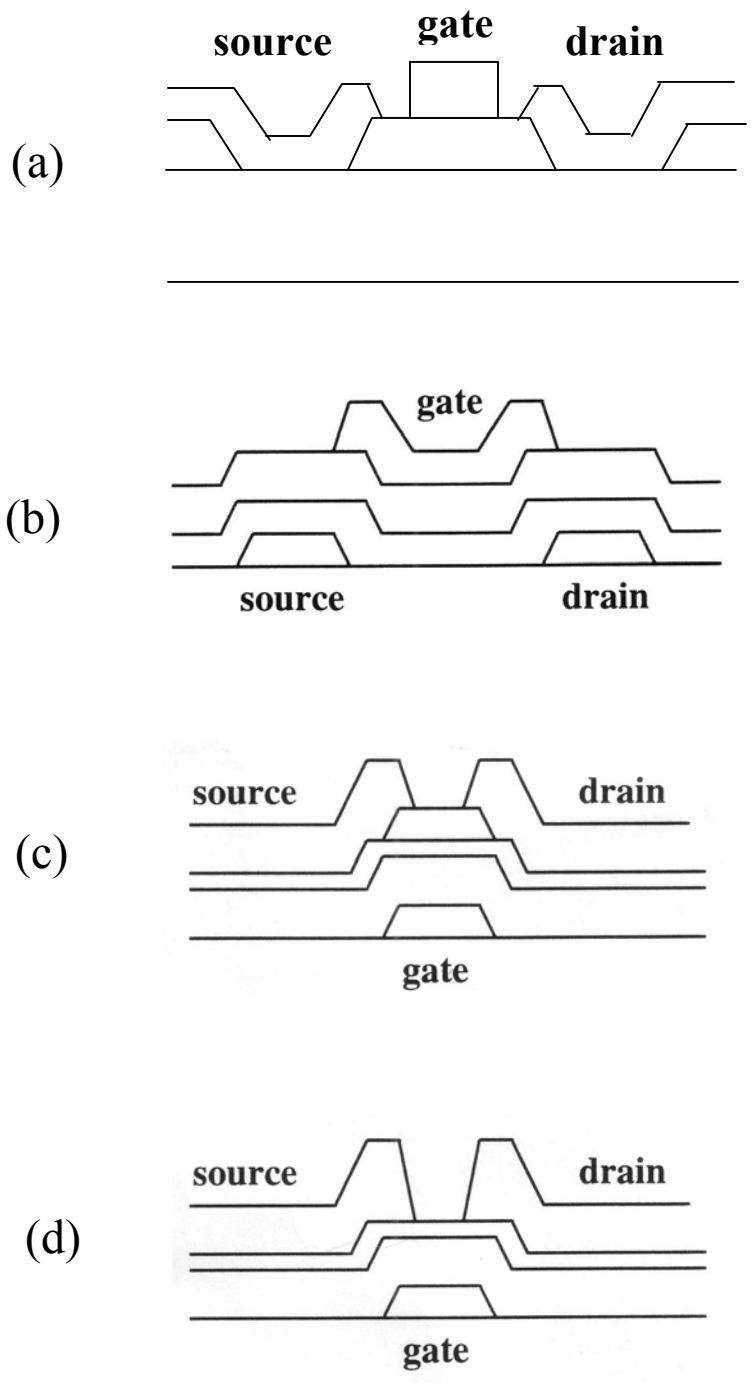


Figure 1. Conventional TFT structures

(a) Coplanar type TFT
(b) Staggered TFT
(c) Inverted Staggered TFT (tri-layer)
(d) Inverted Staggered TFT (back channel cut)

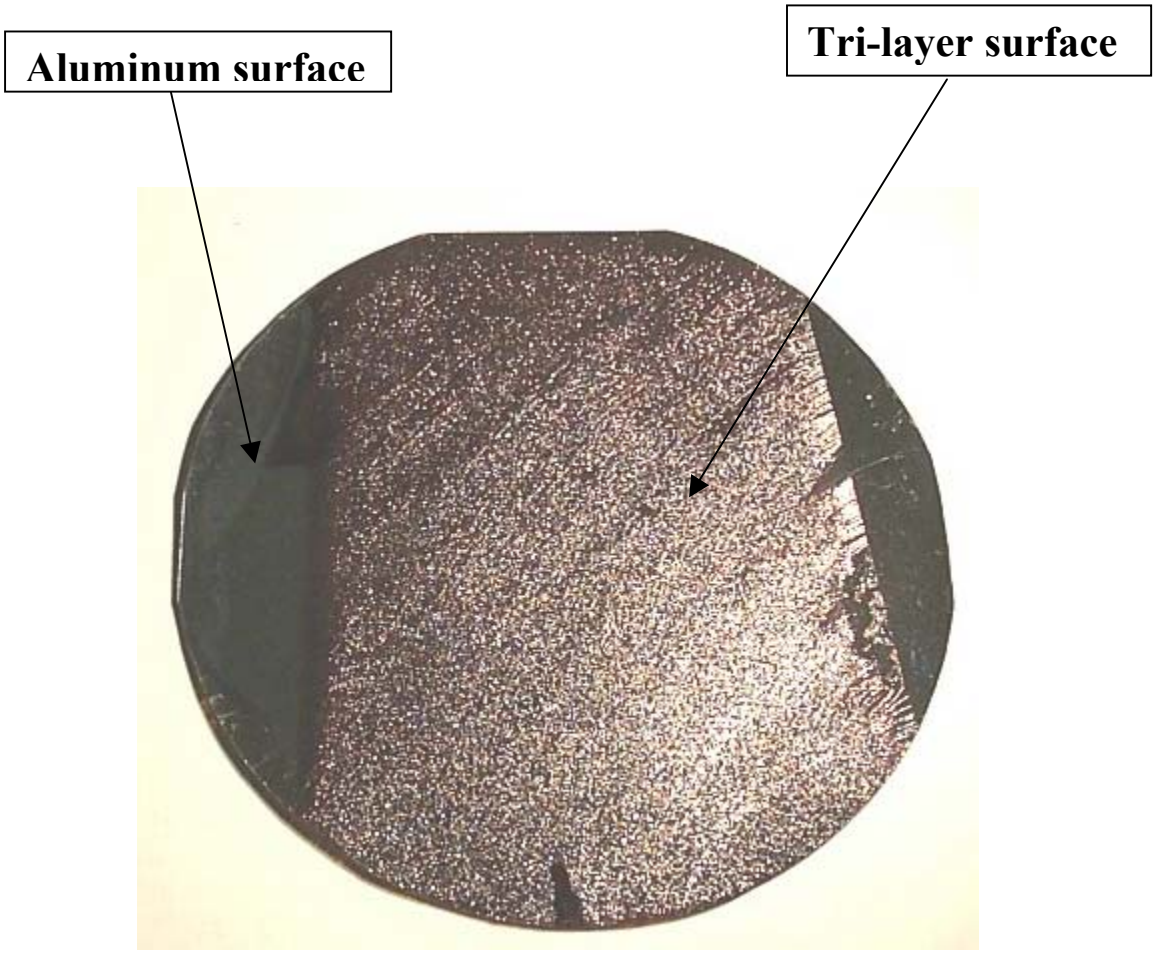


Figure 2. Tri-layer surface on Kapton® after development (Tri-layer deposited at 250 °C)

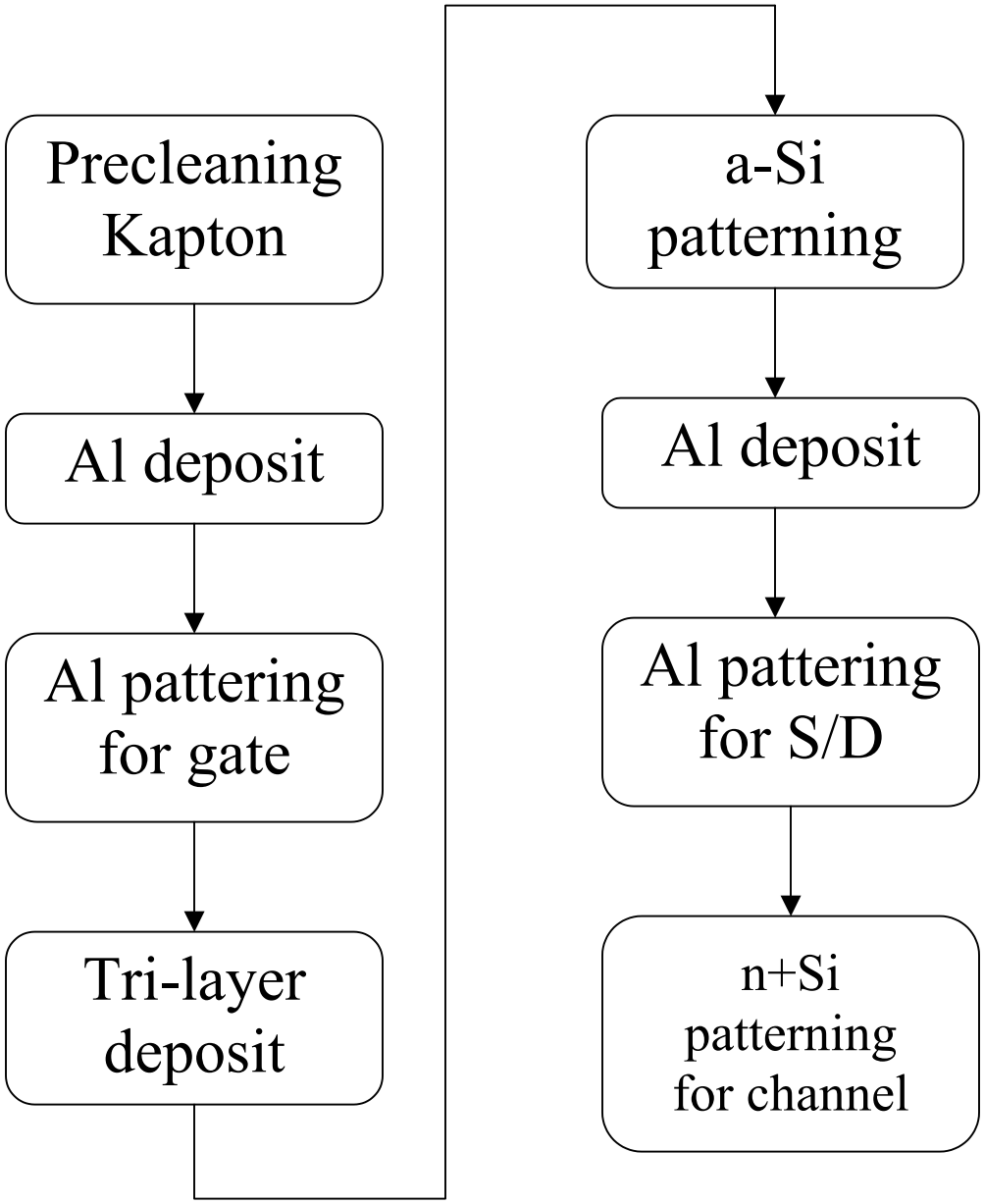
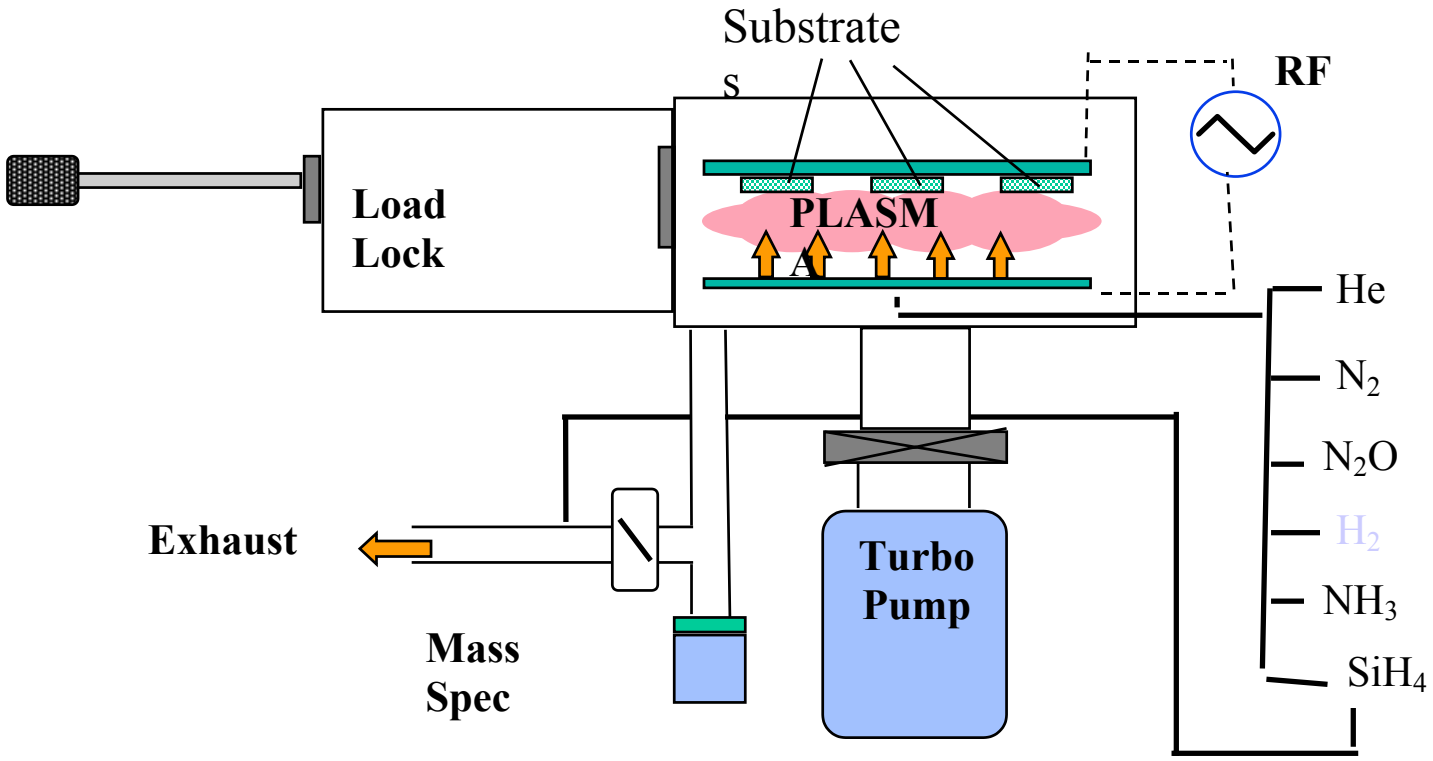
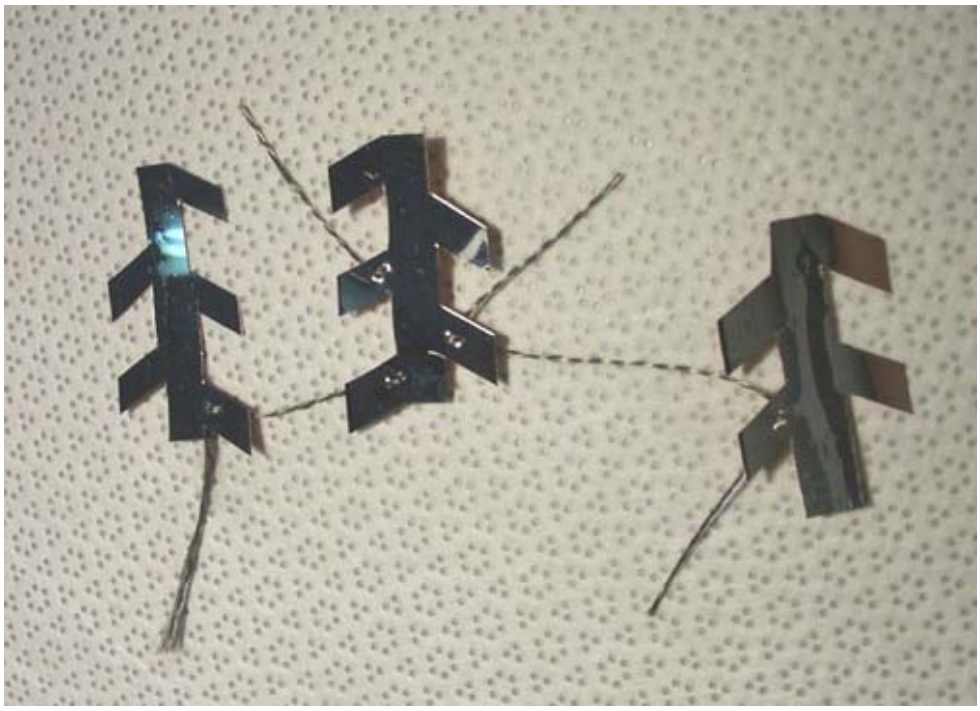


Figure 3. The fabrication process of TFT on Kapton®



- Electrode Area: 30 x 35 cm
- Base Pressure $1x10^{-7}$ Torr

Figure 4. Large Area Showerhead Reactor



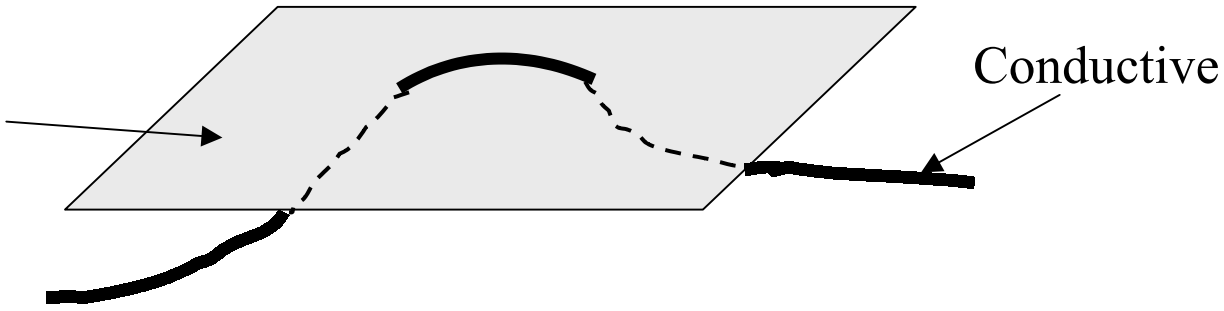
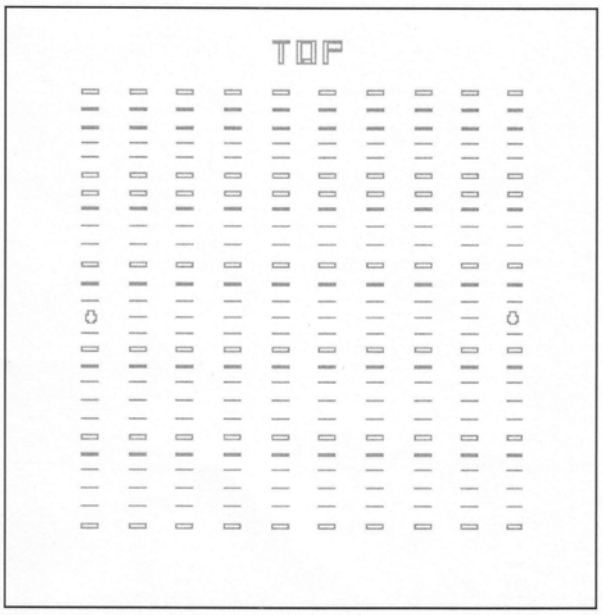
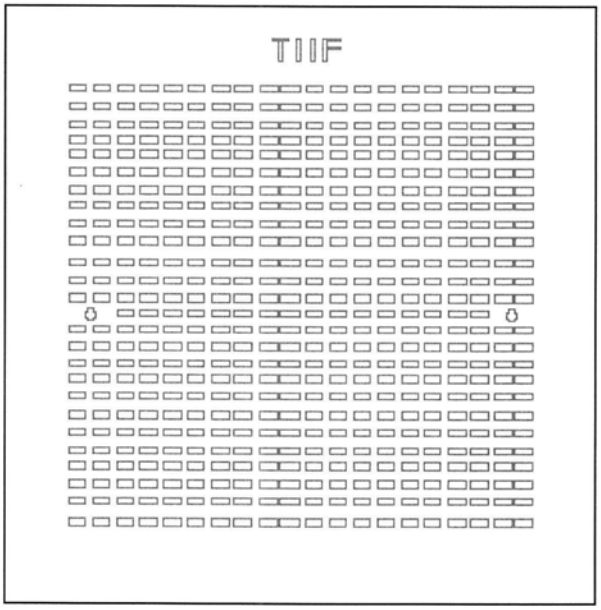


Figure 5. Sewing Diagram for active woven circuits



(a)



(b)

Figure 6. Mask design set #1 for TFT
(a) a-Si island (b) contact

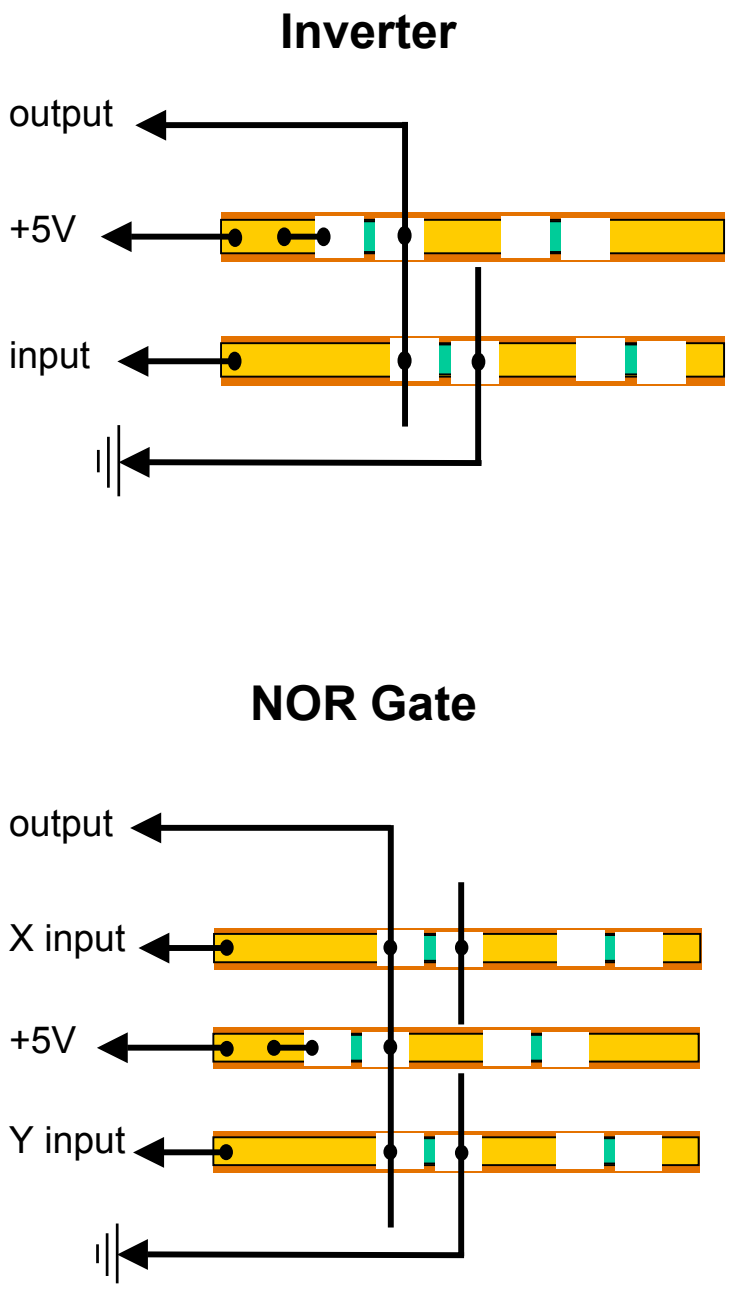


Figure 7. Inverter and NOR gate from TFTs on Kapton® and conductive threads

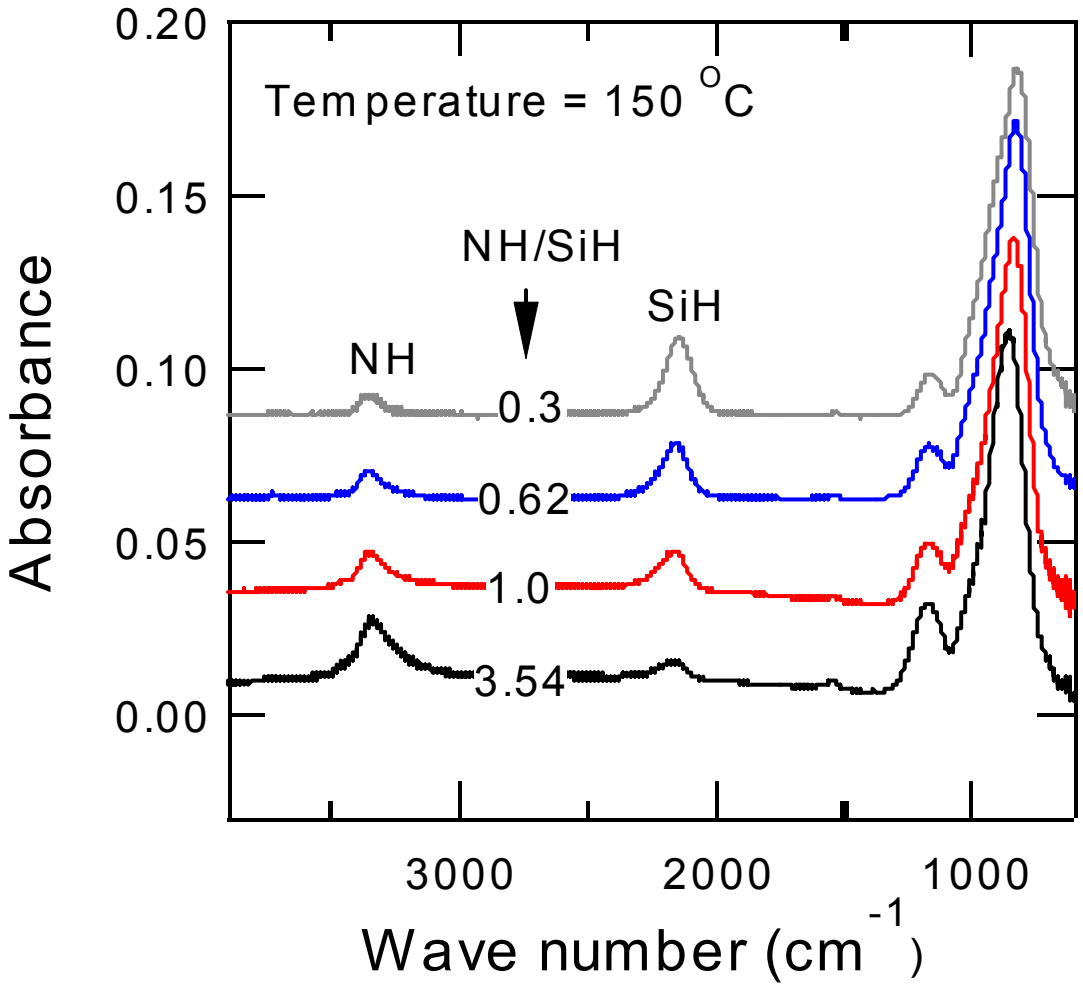


Figure 8. Infrared absorption spectra for PECVD SiN_x films with different NH/SiH ratio at T = 150 °C

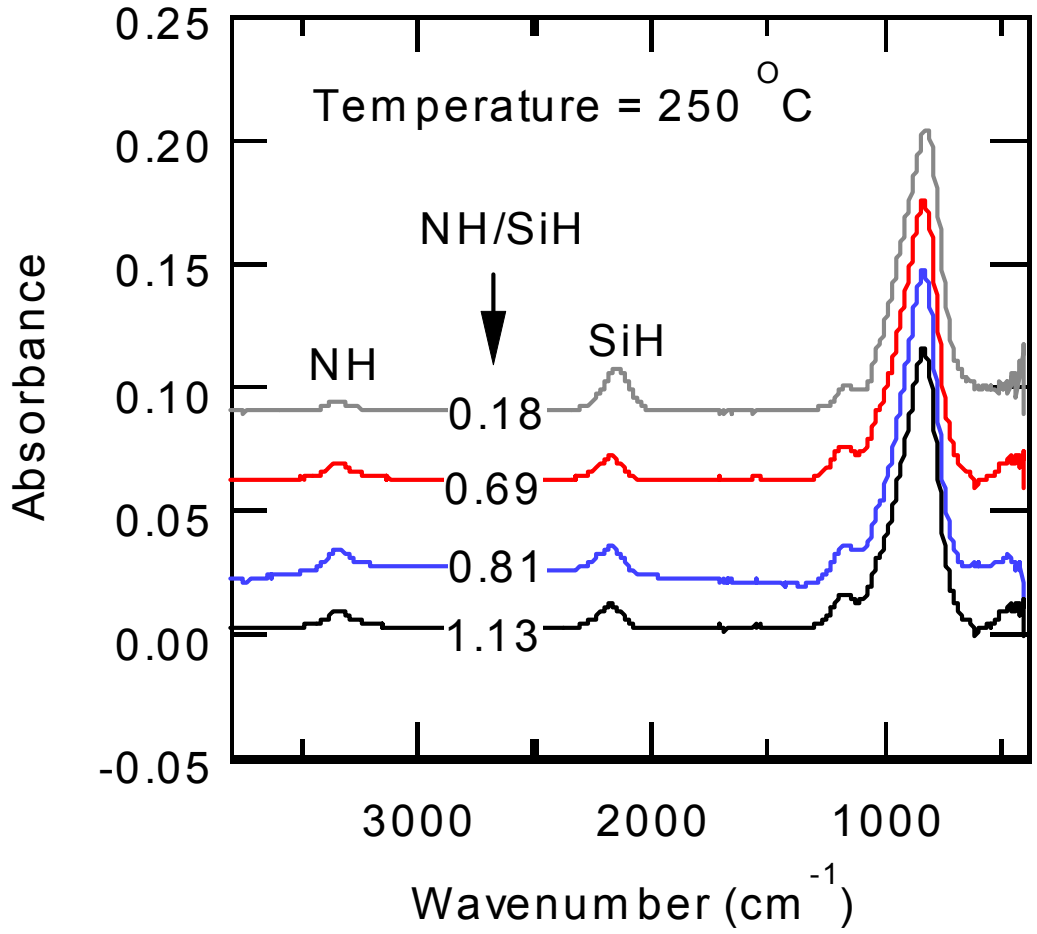


Figure 9. Infrared absorption spectra for PECVD SiN_x films with different NH/SiH ratio at T = 250 °C

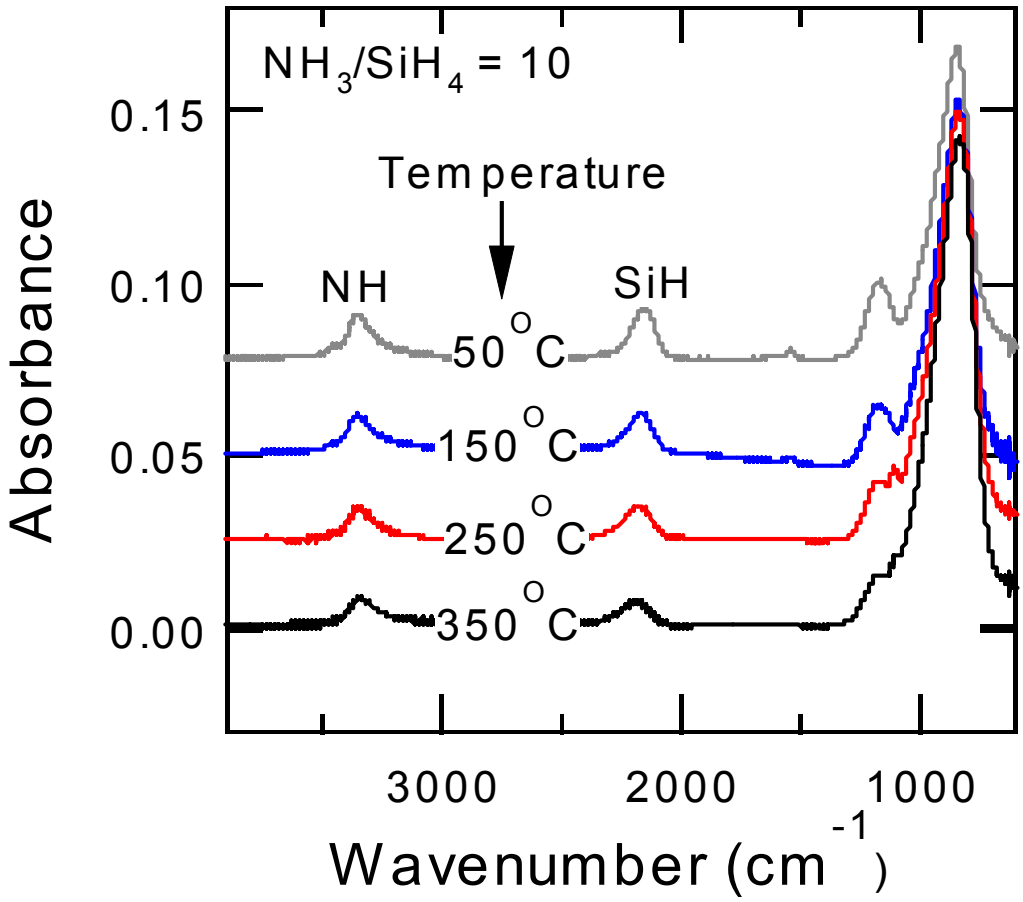


Figure 10. Infrared absorption spectra for PECVD SiN_x films with different temperature at $NH_3/SiH_4 = 10$

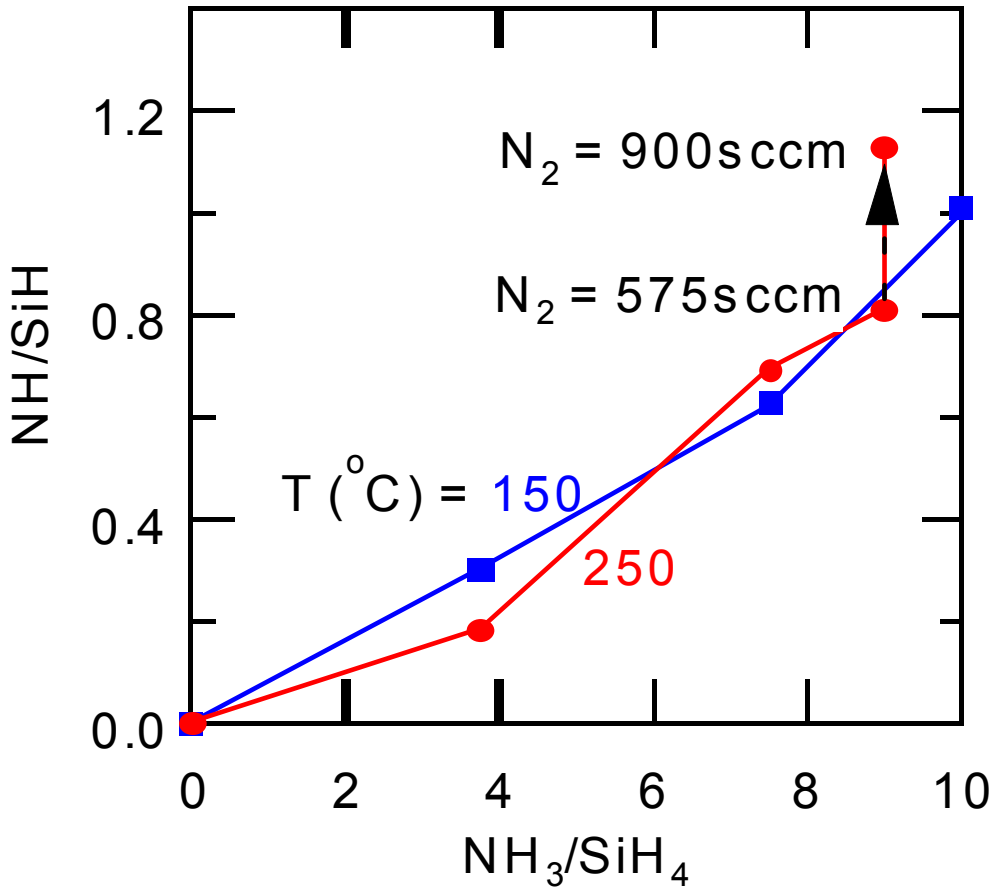
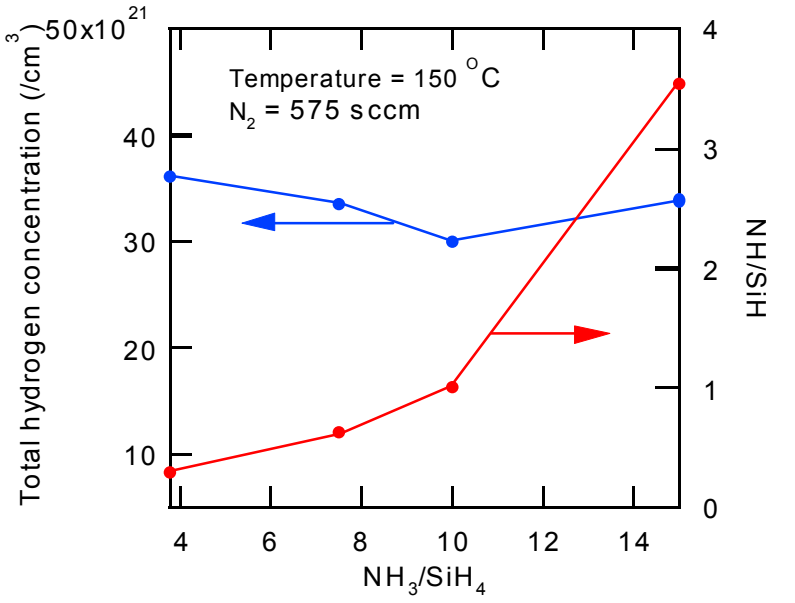
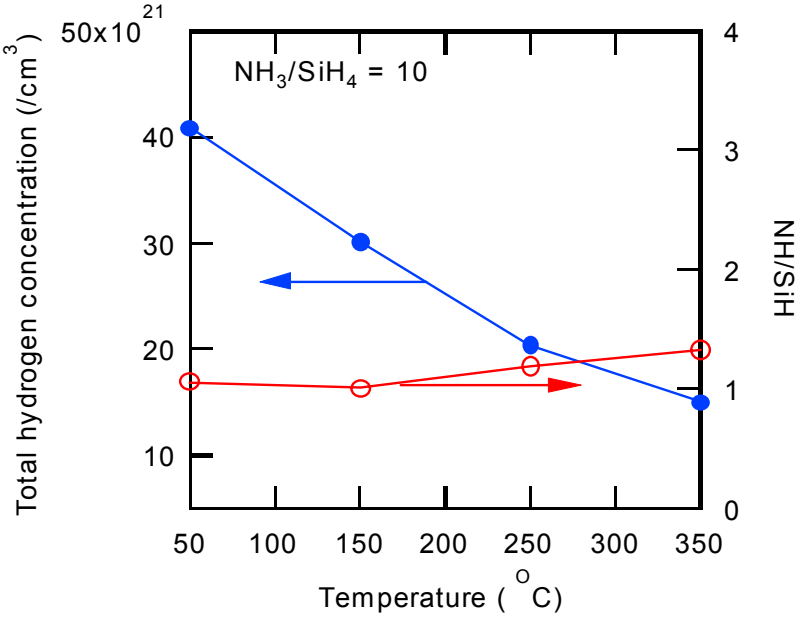


Figure 11. Processing gas composition effect on NH/SiH



(a)



(b)

Figure 12. Total hydrogen concentrations with (a) NH/SiH at 150 ^{o}C and (b) temperature at NH_3/SiH_4 = 10

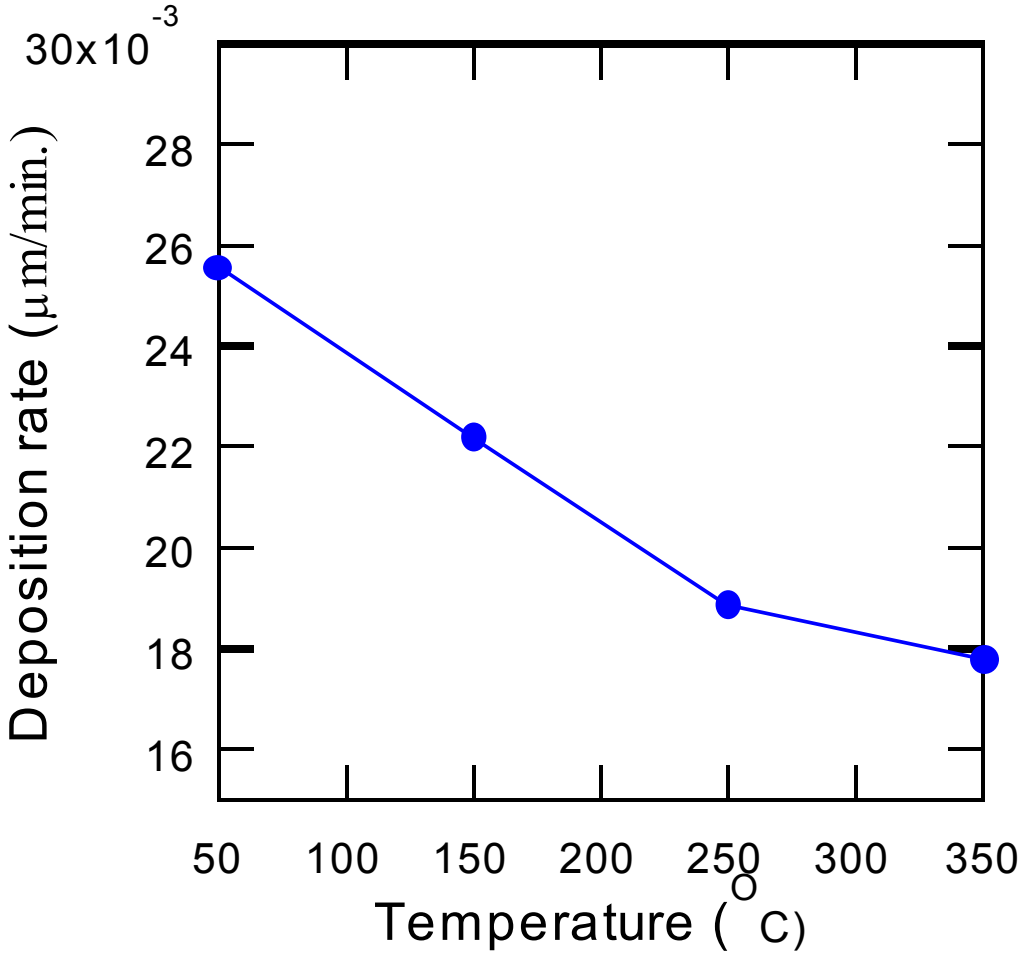


Figure 13. The deposition rate variation with temperature at $NH_3/SiH_4 = 10$

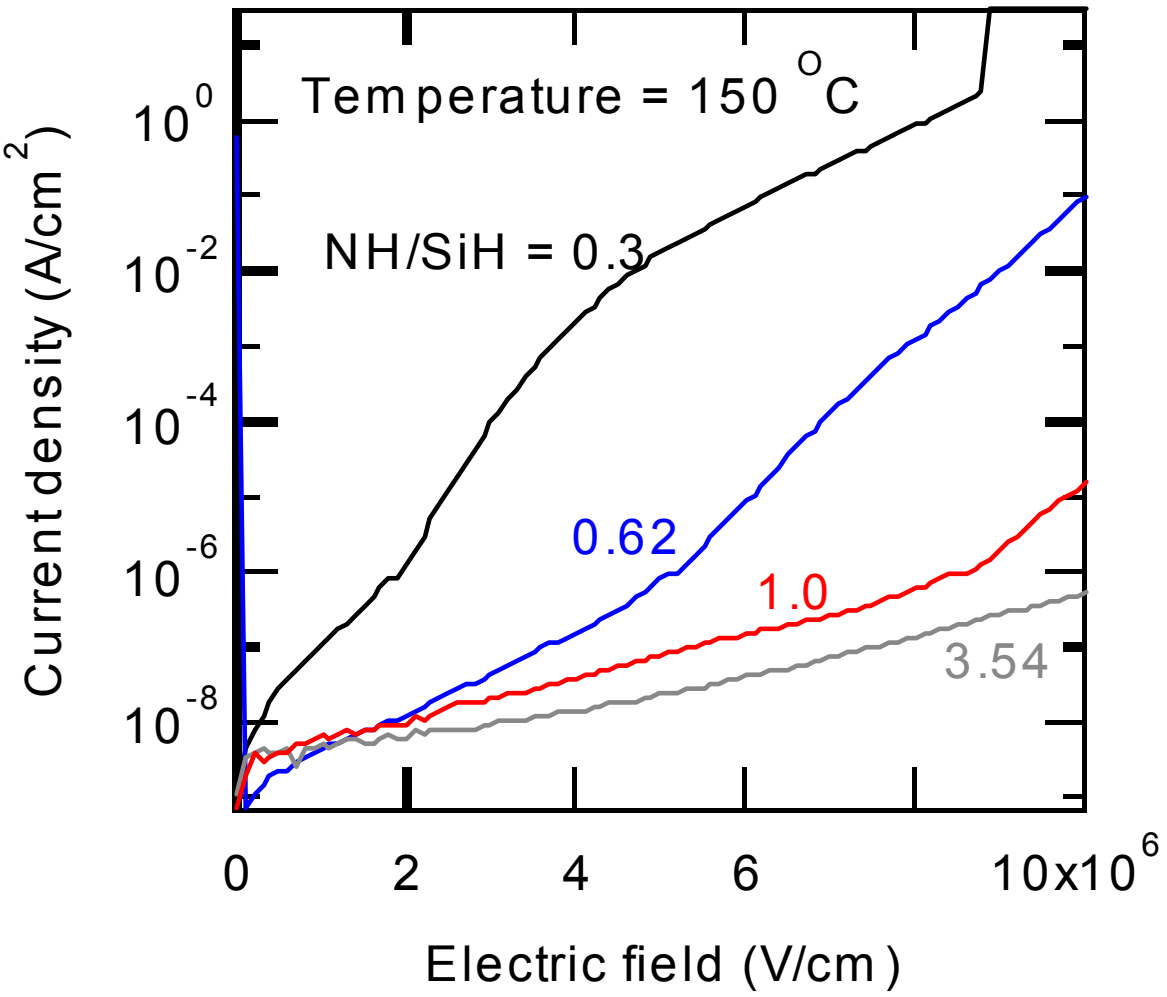


Figure 14. Current density vs. electric field for SiN_x with different NH/SiH ratio at 150 °C

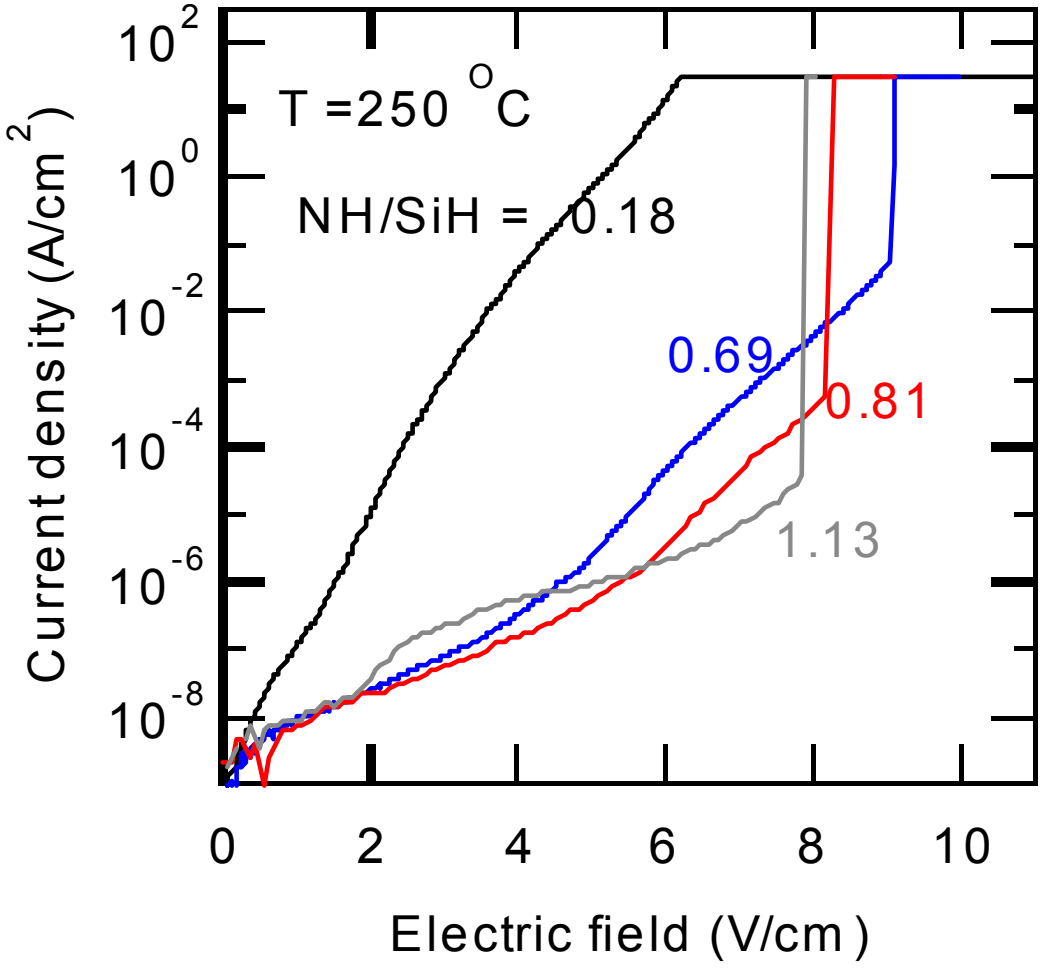


Figure 15. Current density vs. electric field for SiN_x with different NH/SiH ratio at 250 °C

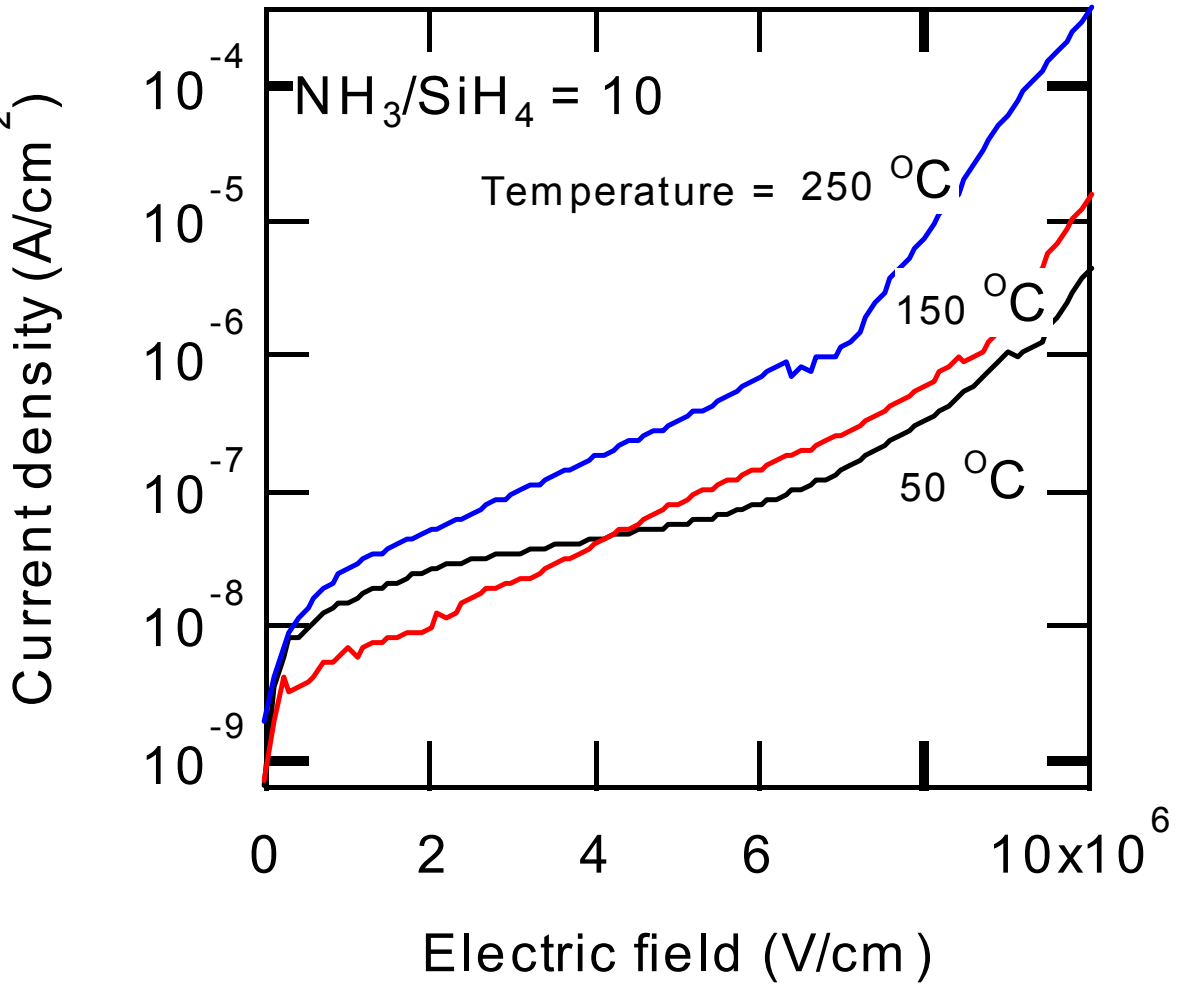


Figure 16. Current density vs. electric field for SiN_x with different temperature at NH_3/SiH_4=10

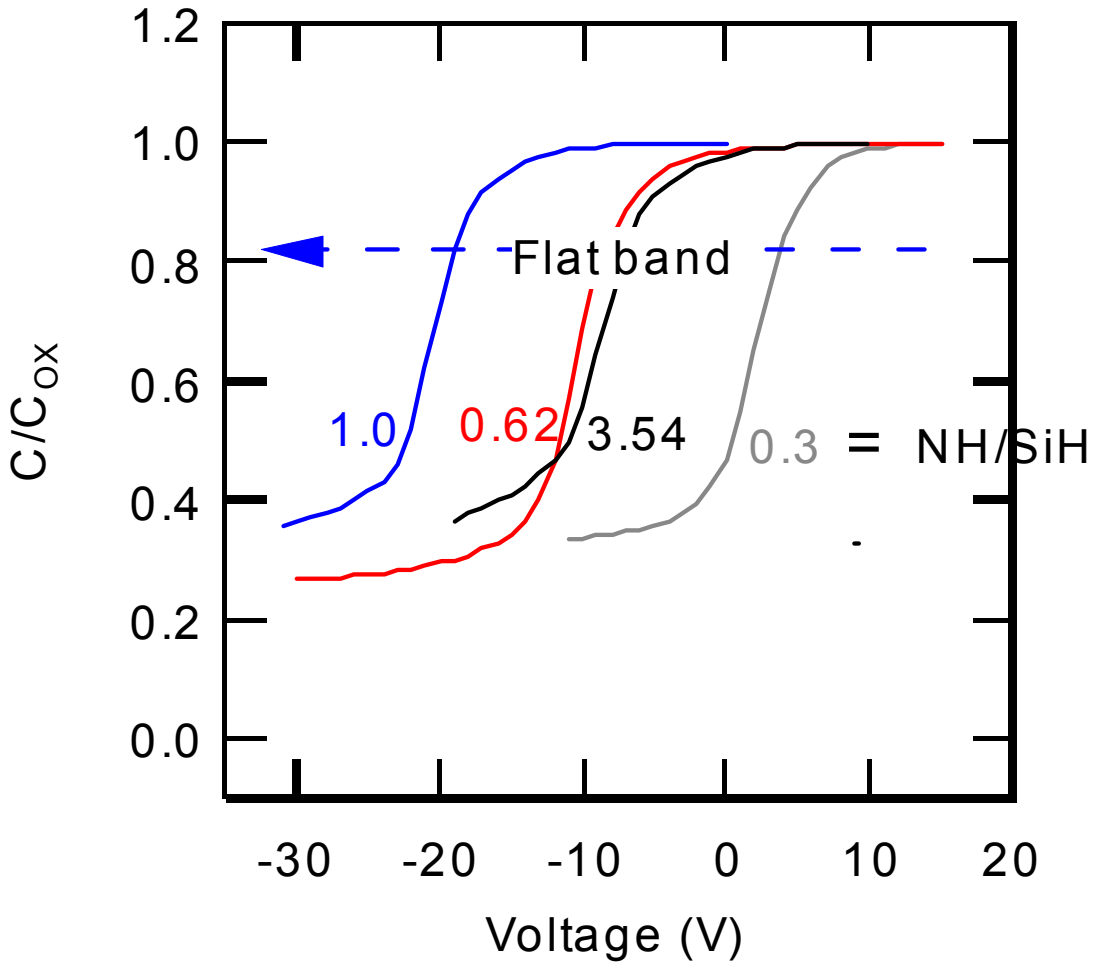


Figure 17. C/C_{ox} vs. voltage plots for nitride films with different NH/SiH ratio at 150 ^{o}C

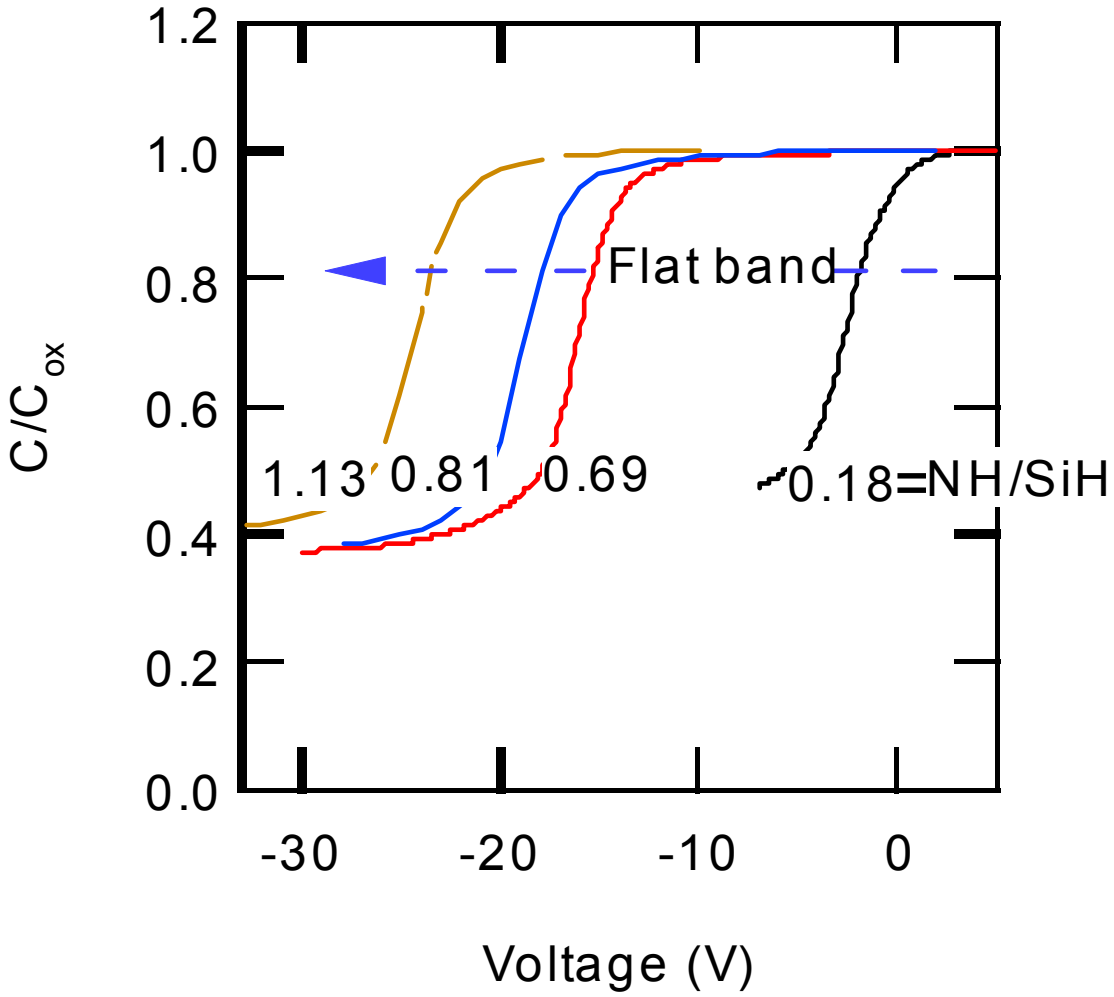


Figure 18. C/C_{ox} vs. voltage plots for nitride films with different NH/SiH ratio at 250 ^{o}C

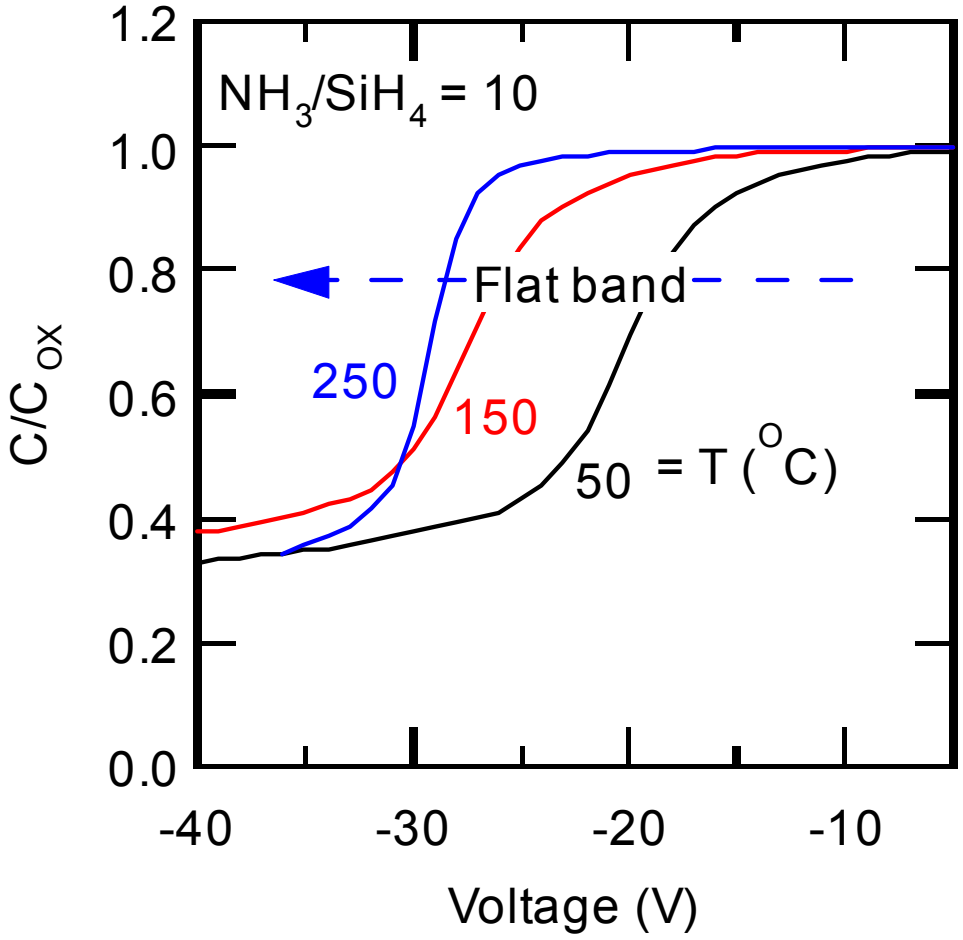
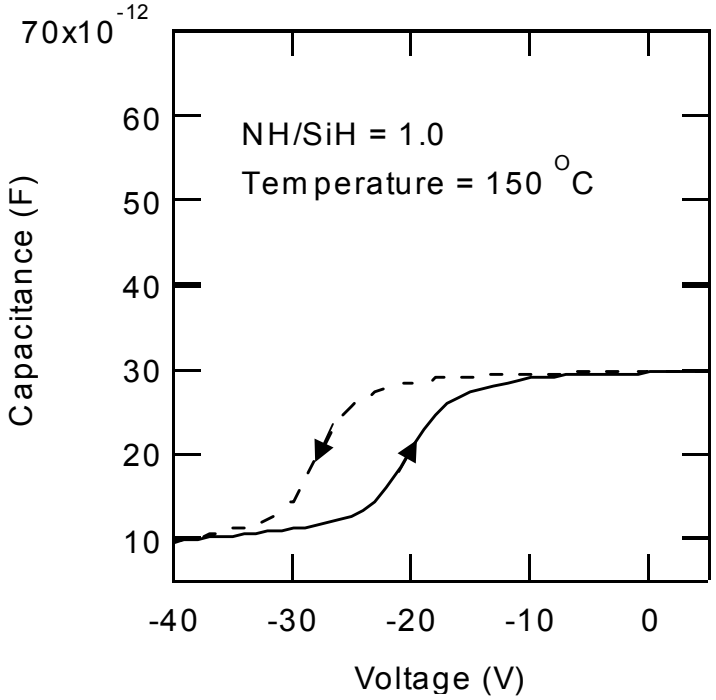
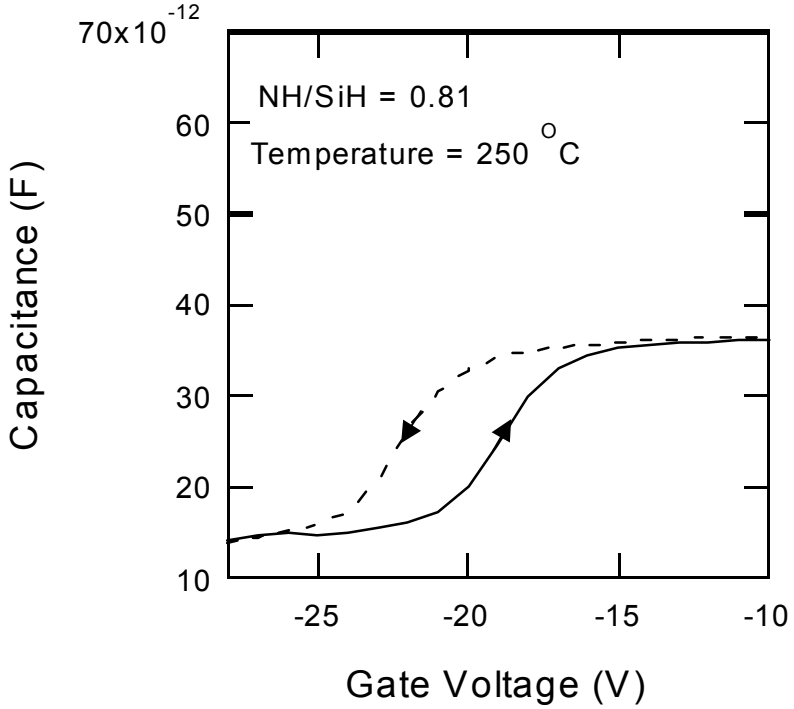


Figure 19. C/C_{ox} vs. voltage plots for nitride films with different temperature at NH_3/SiH_4 =10



(a)



(b)

Figure 20. The hysteresis loop for capacitance vs. voltage for SiN_x at (a) 150 °C and (b) 250 °C

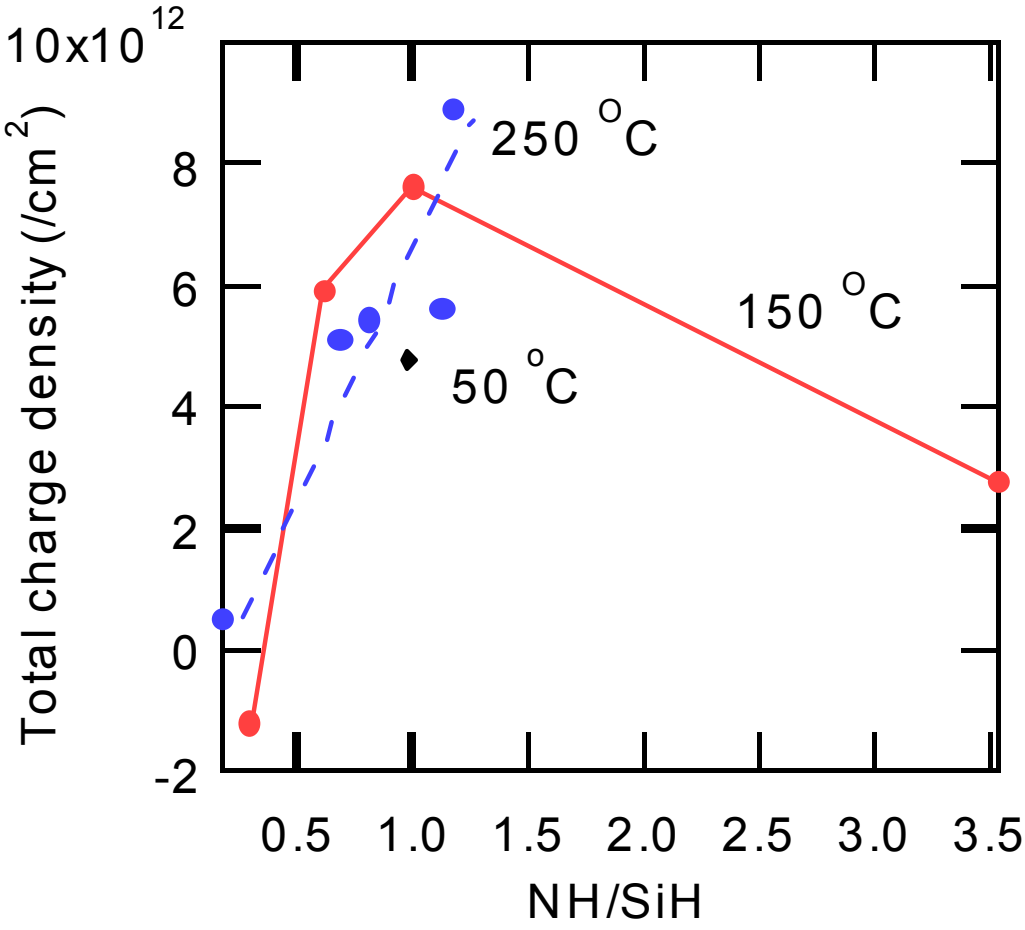


Figure 21. Total charge density variation with NH/SiH for film with t_{ox} = 1000 Å

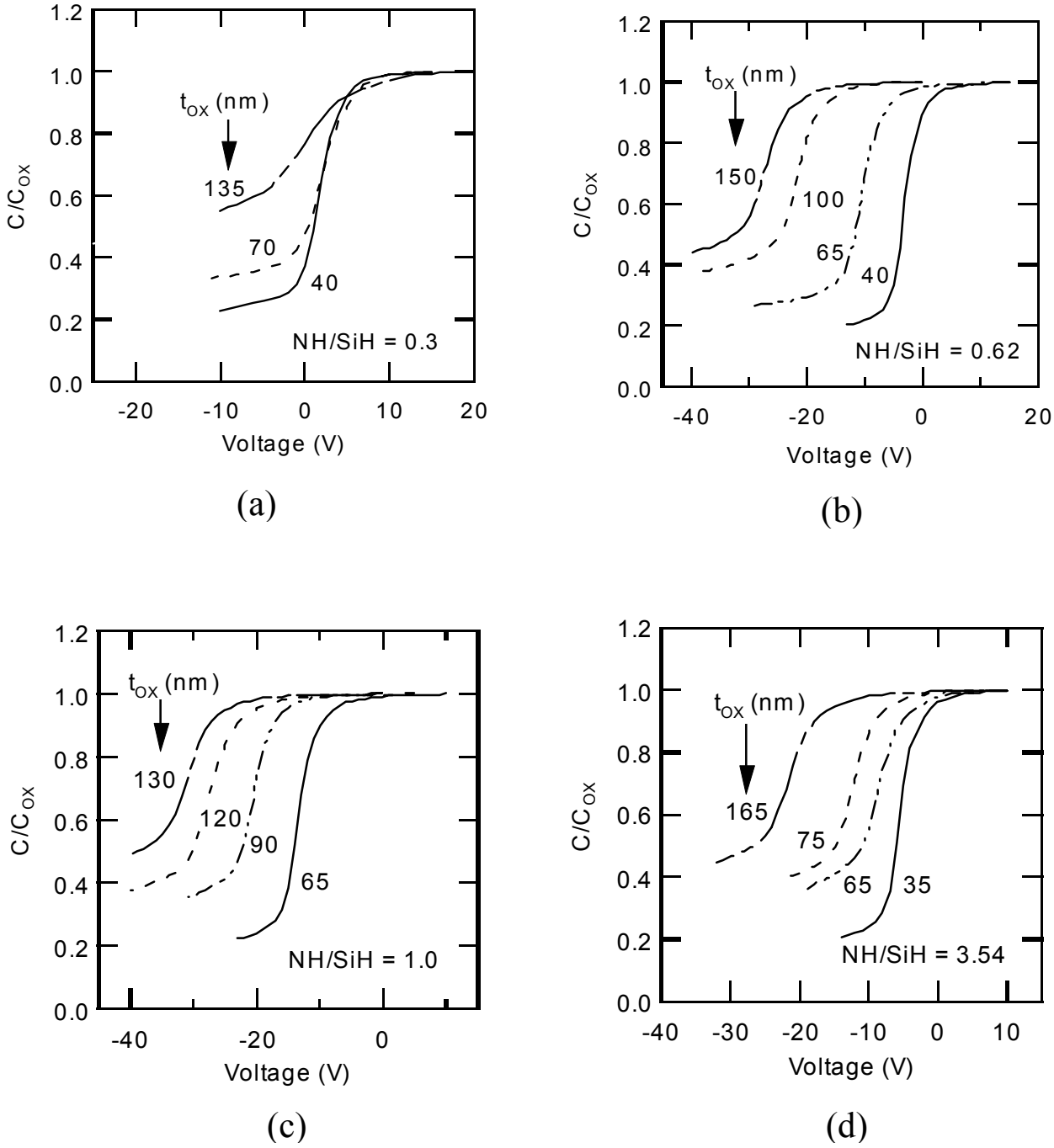


Figure 22. C/C_{ox} vs. Voltage with nitride thickness for various NH/SiH ratio at T = 150°C

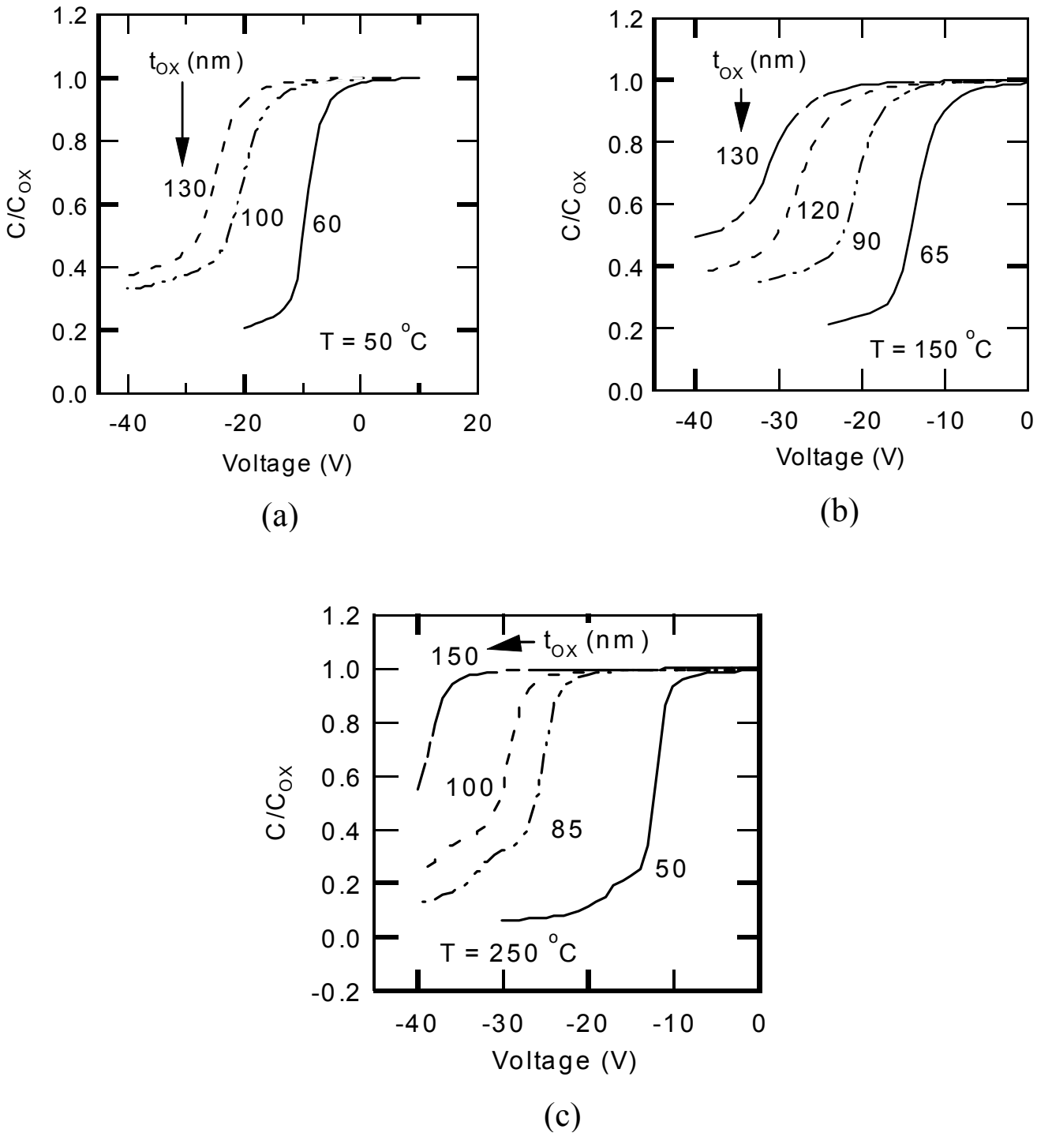
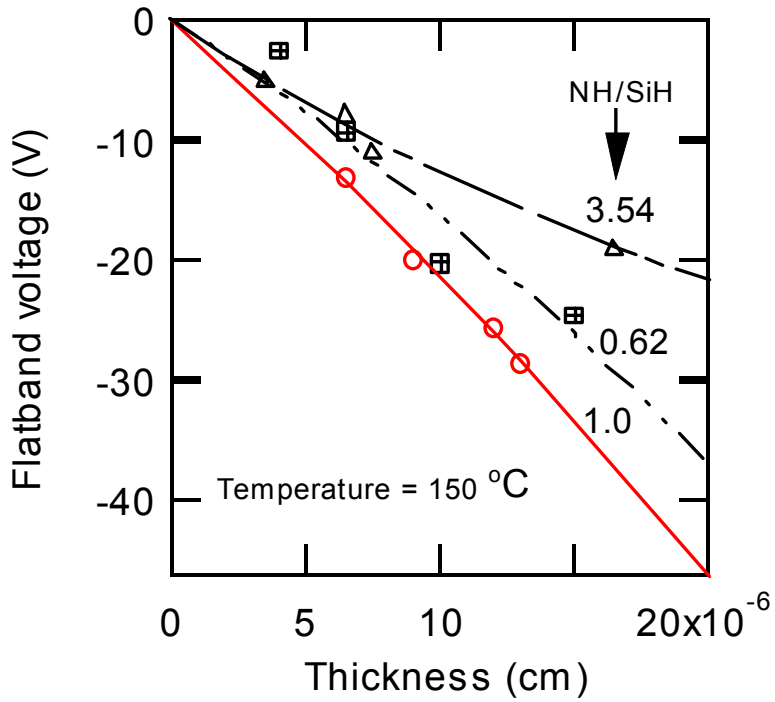
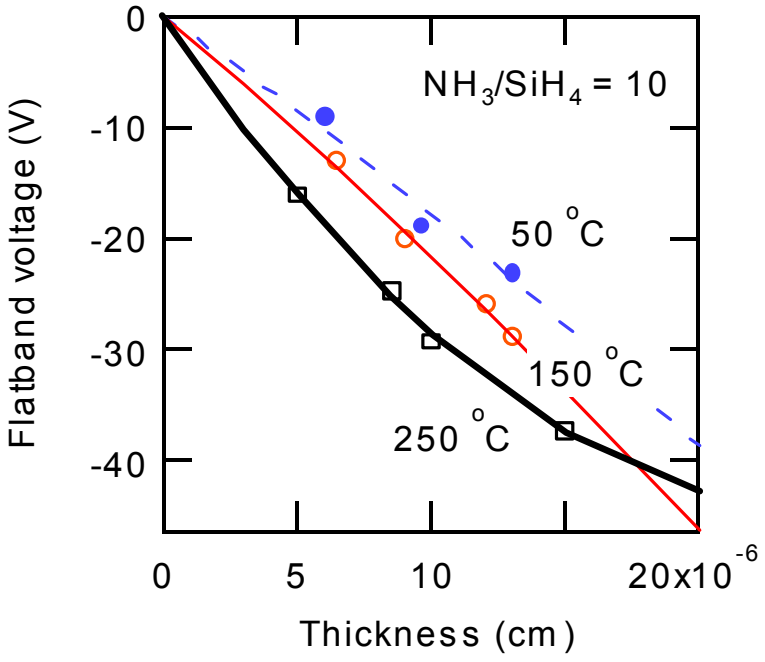


Figure 23. C/C_{ox} vs. Voltage with nitride thickness for various temperatures at NH/SiH = 1

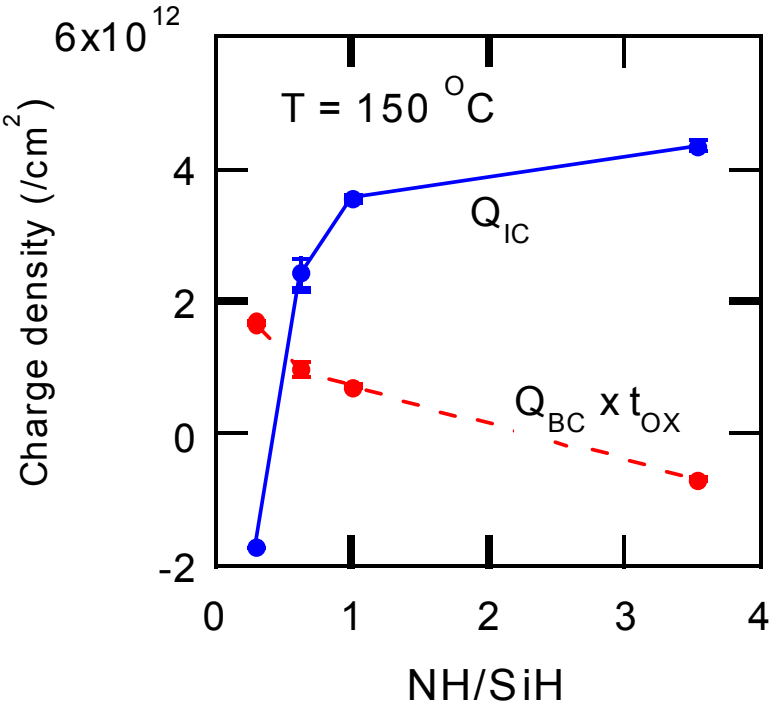


(a)

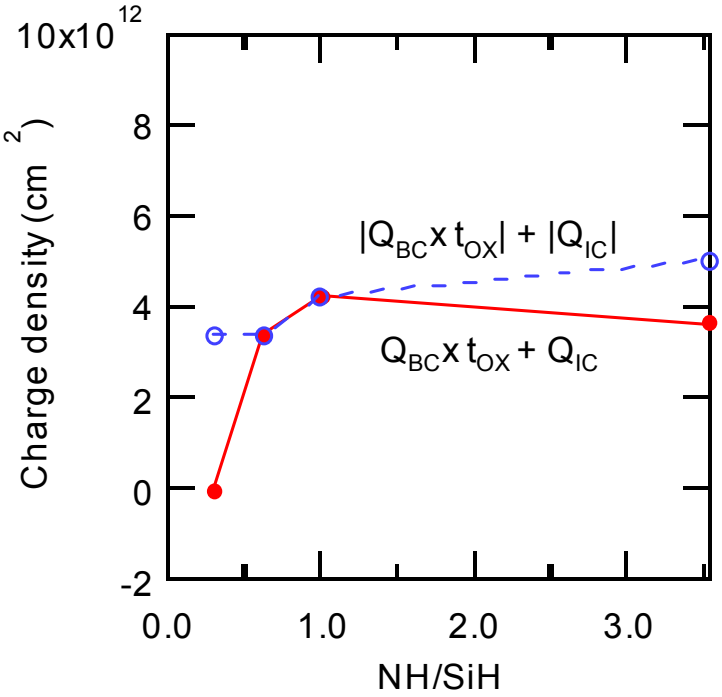


(b)

Figure 24. Plots of flat band voltage versus the nitride thickness at (a) 150 and (b) $NH_3/SiH_4 = 10$



(a)



(b)

Figure 25. (a) The charge variation in the interface and bulk film (b) net charge density variation with NH/SiH ratio at 150 °C

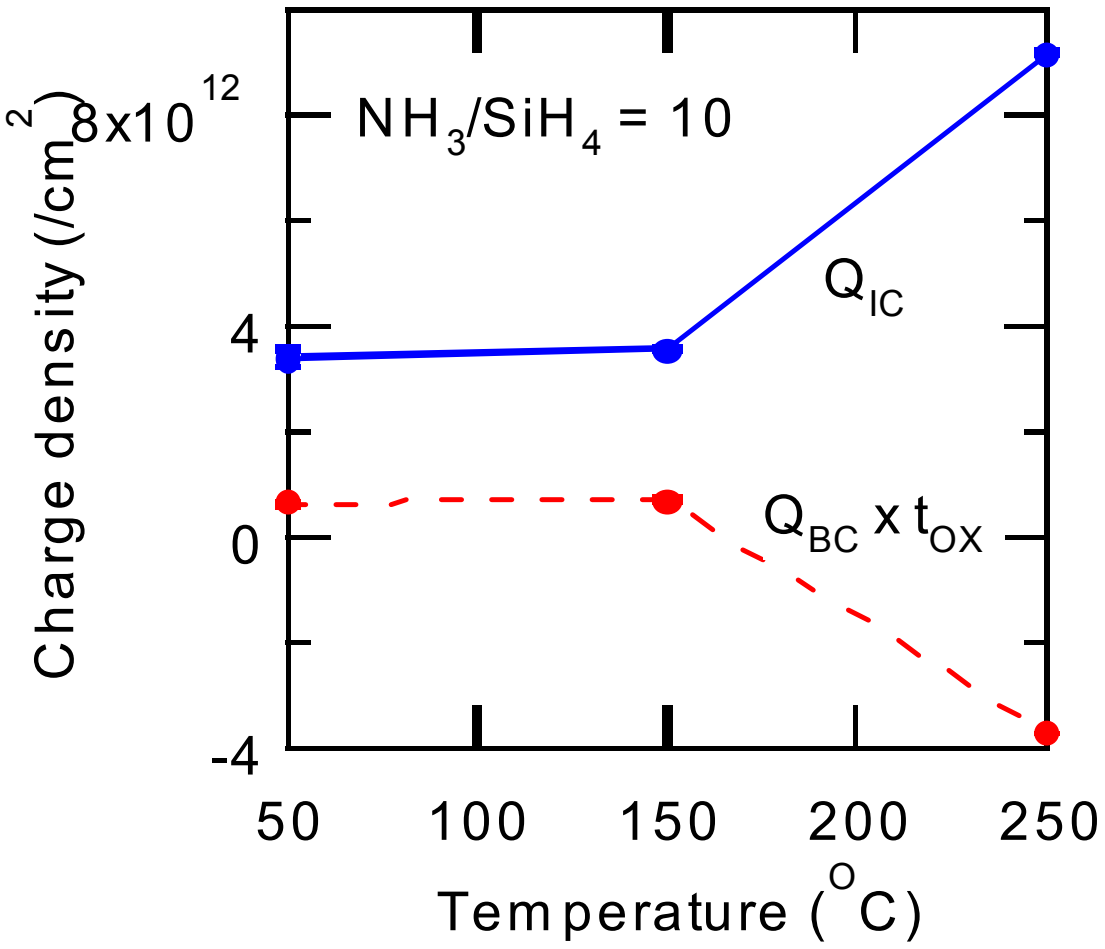


Figure 26. The charge variation in the interface and bulk film with temperature at $NH_3/SiH_4 = 10$

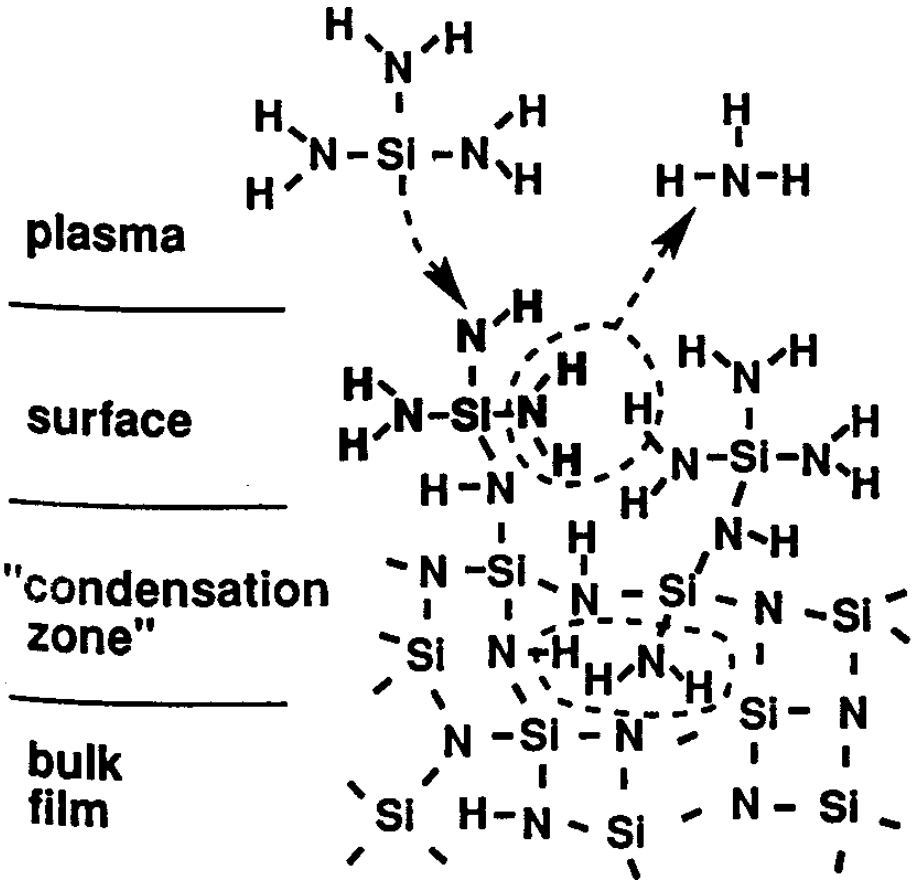


Figure 27. Cross-sectional structure model of the condensation of absorbed $Si(NH_2)_3$ toward on Si-N network with the evolution of NH_3
[Reference 44]

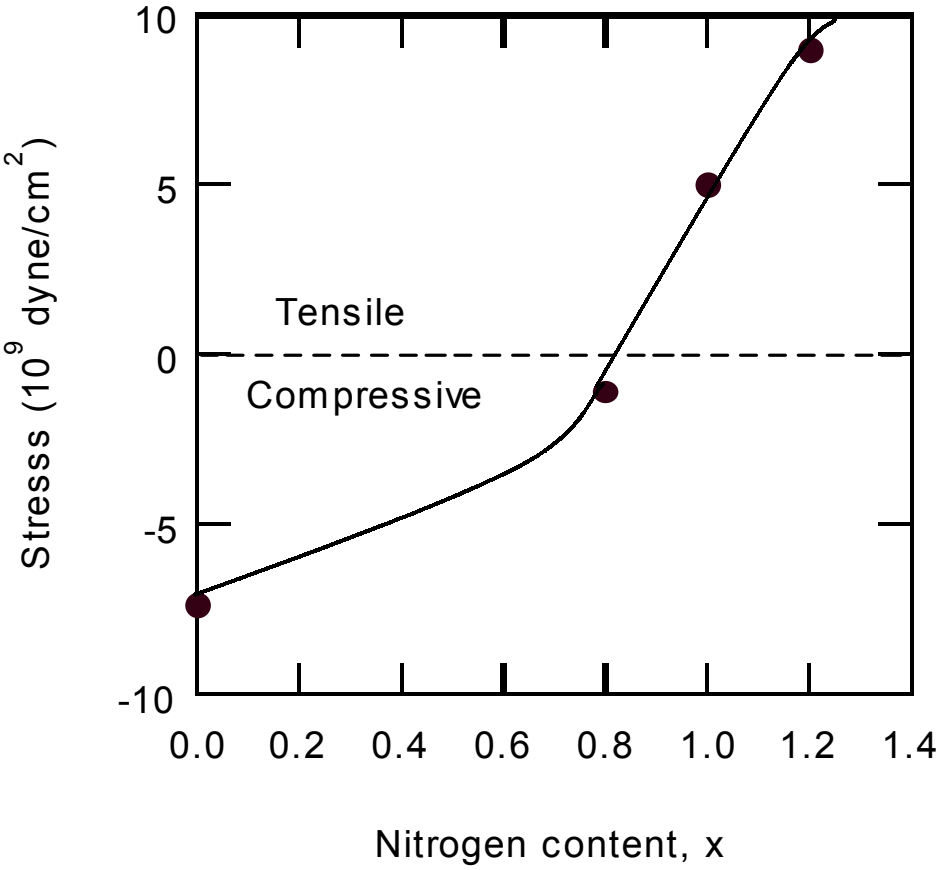


Figure 28. Stress in the SiN_x layer with nitrogen content

[Reference 42]

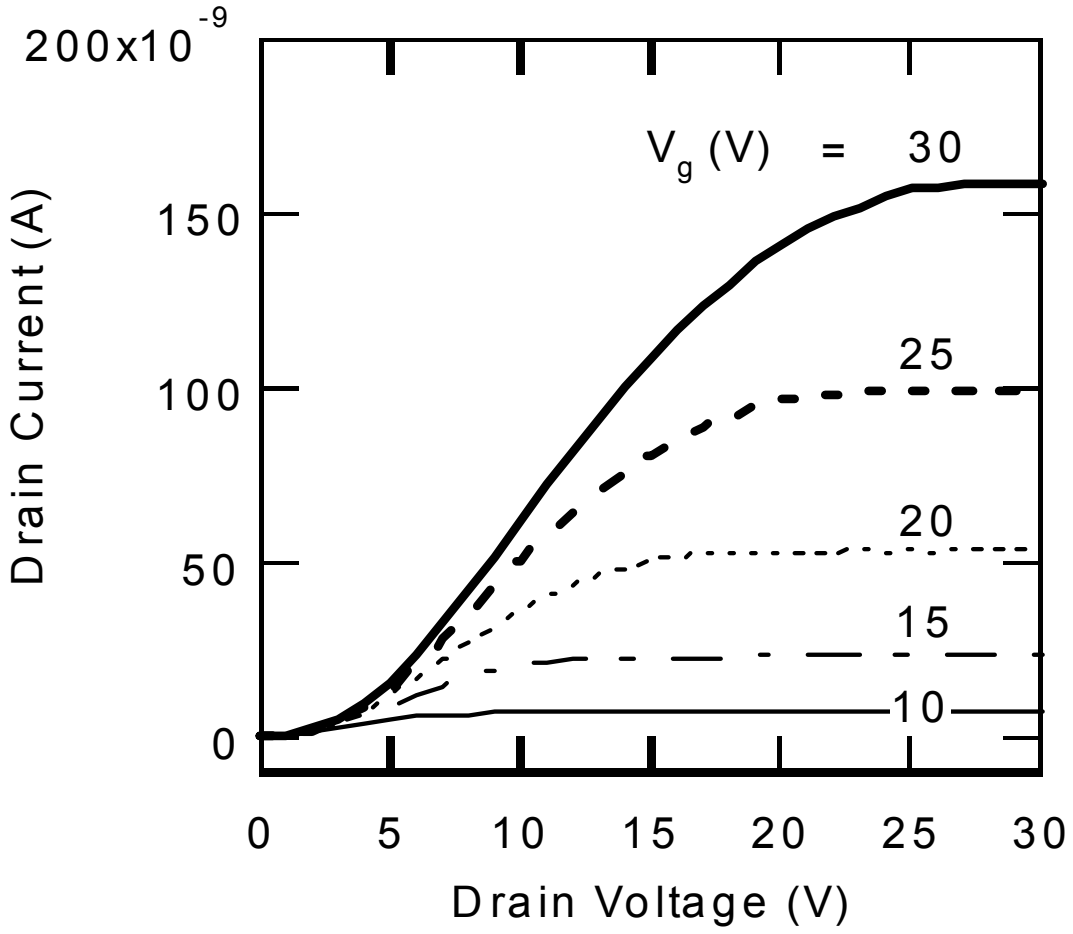


Figure 29. Drain current versus drain voltage for the TFT on plastic

V_g: gate voltage

Transistor channel width/length=0.1/0.1mm

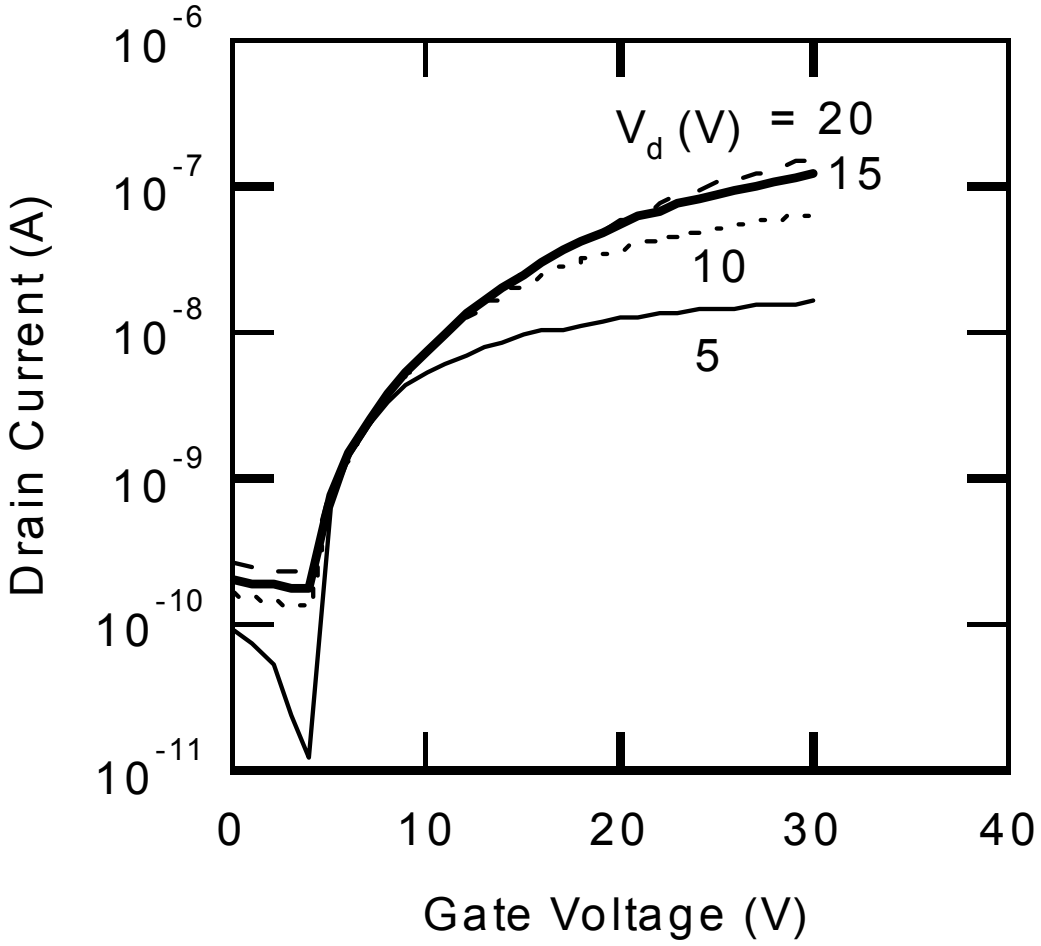


Figure 30. Log of drain current versus gate voltage for the TFT on plastic

V_d: drain voltage
Transistor channel width/length=0.1/0.1mm
linear mobility = 0.026 cm^2/Vs
saturation mobility = 0.059 cm^2/Vs

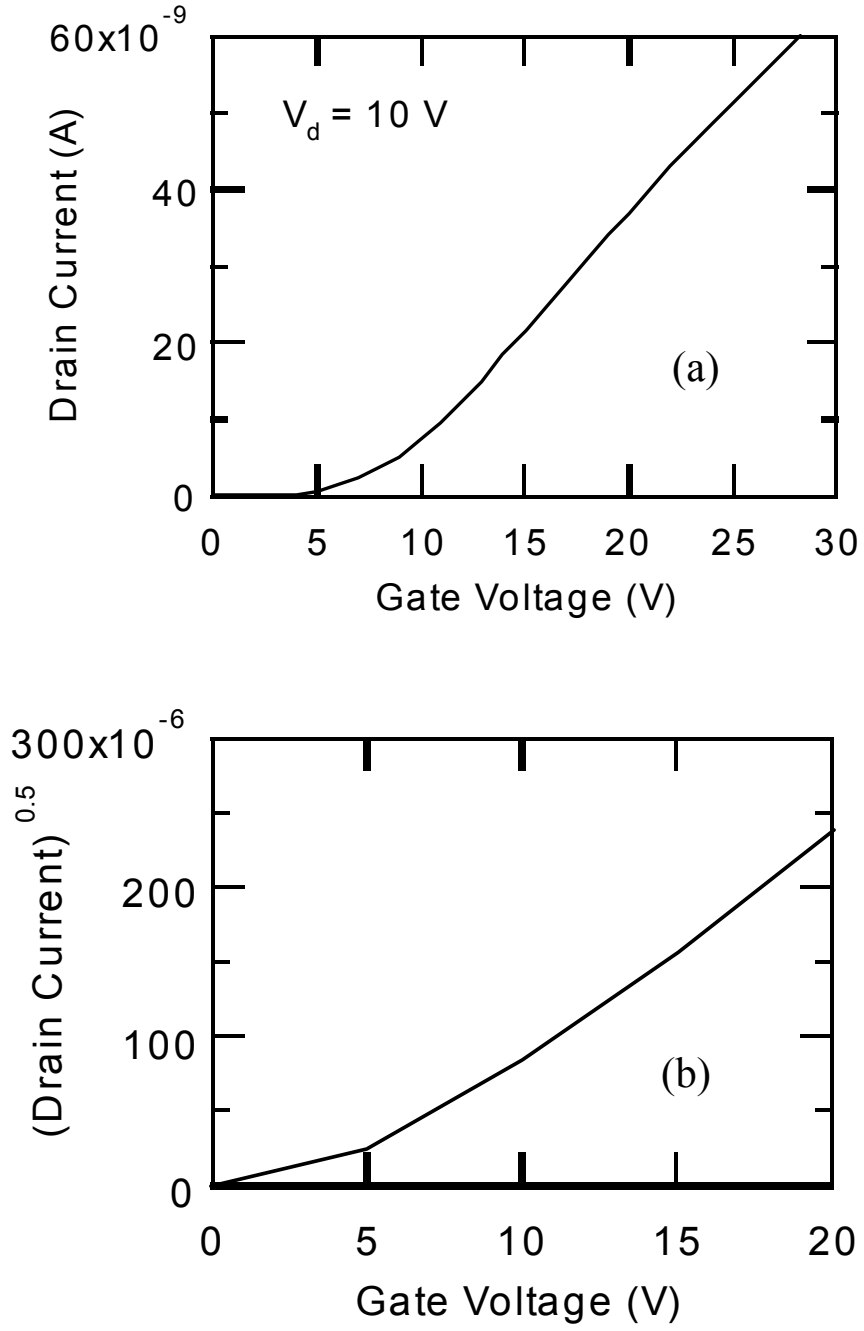


Figure 31. (a) Linear and (b) saturation mobility plots for TFT on plastic

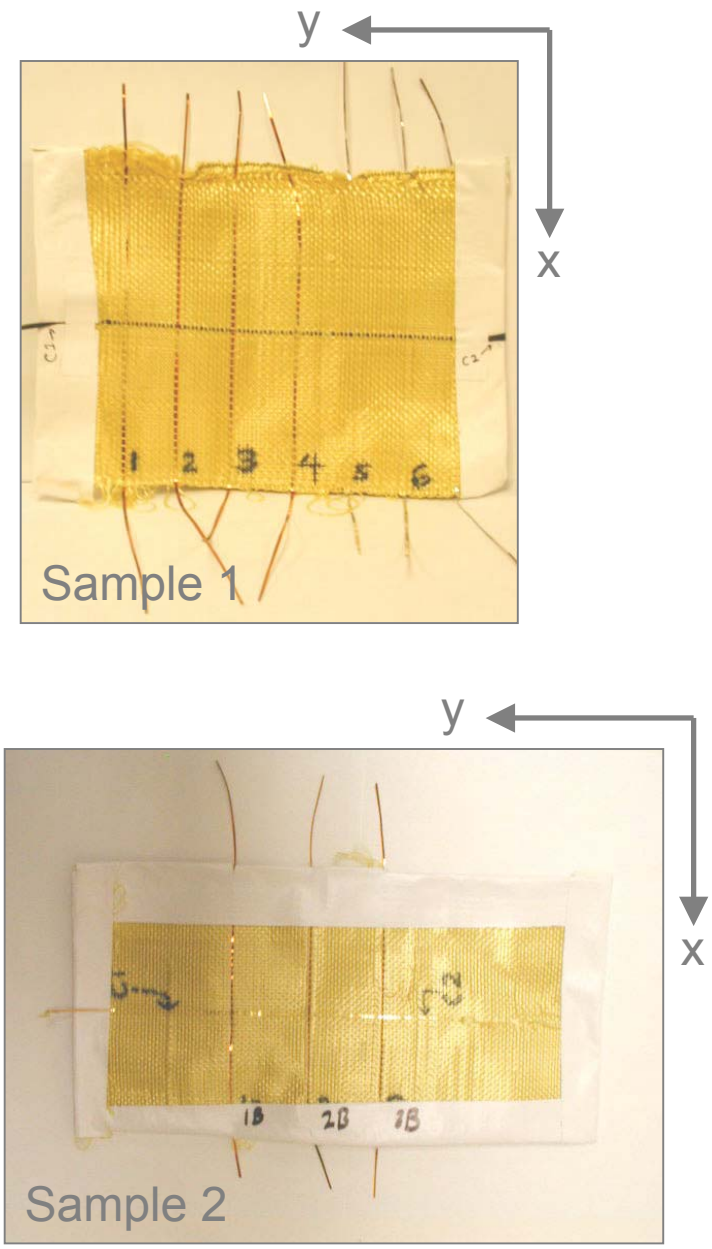


Figure 32. Woven circuits for contact measurement

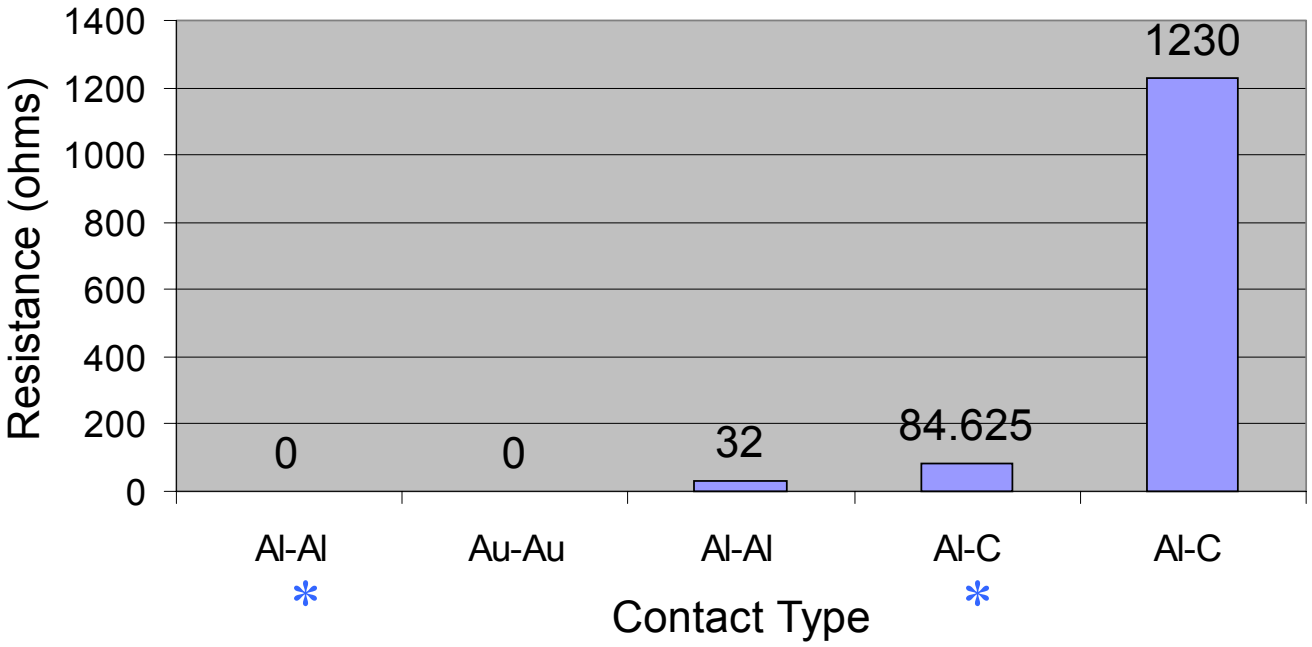


Figure 33. Contact resistance with different materials contact (Al: aluminum, Au: gold, C: carbon fiber)

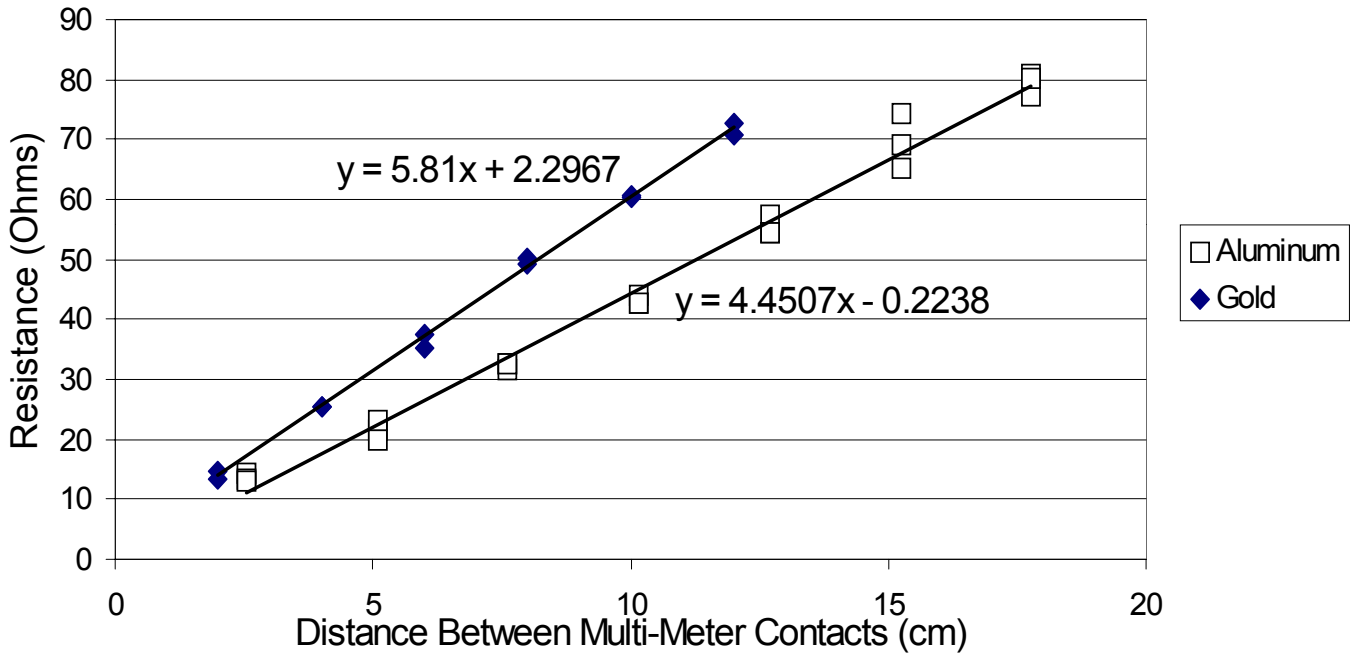


Figure 34. Resistance vs. distance for two contacted Kapton® strips: Gold Films and Kapton® Films

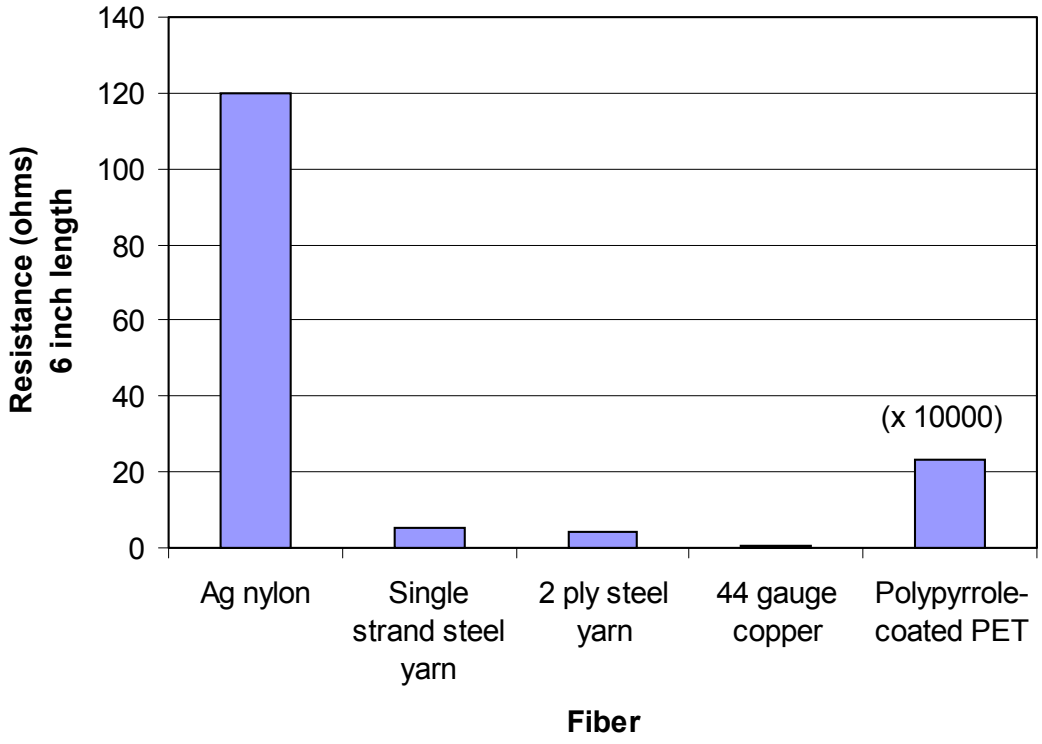
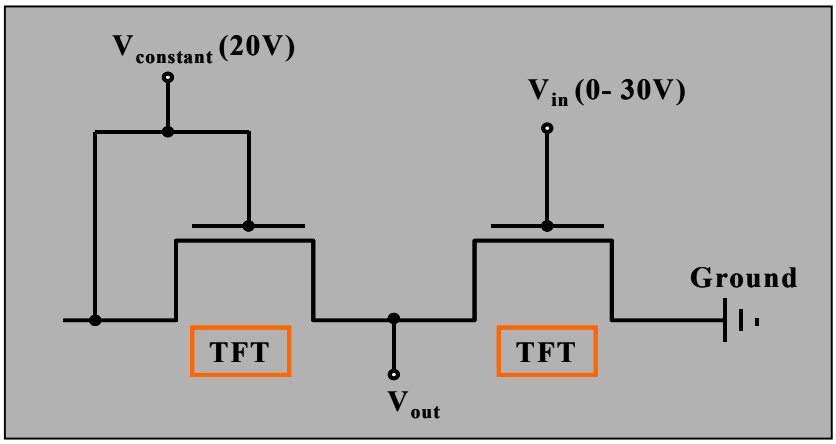


Figure 35. A comparison of the respective electrical resistances of five different conductive fibers



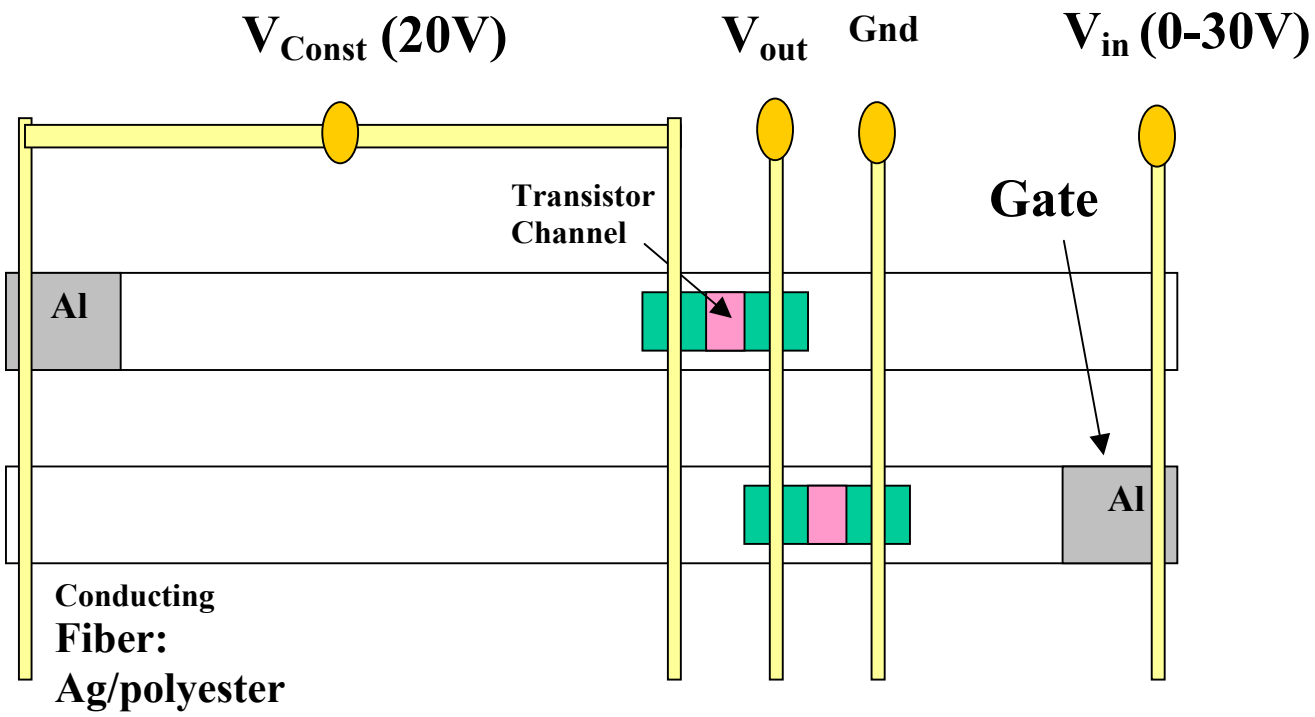


Figure 36. Simple inverter application with TFTs and conductive yarns

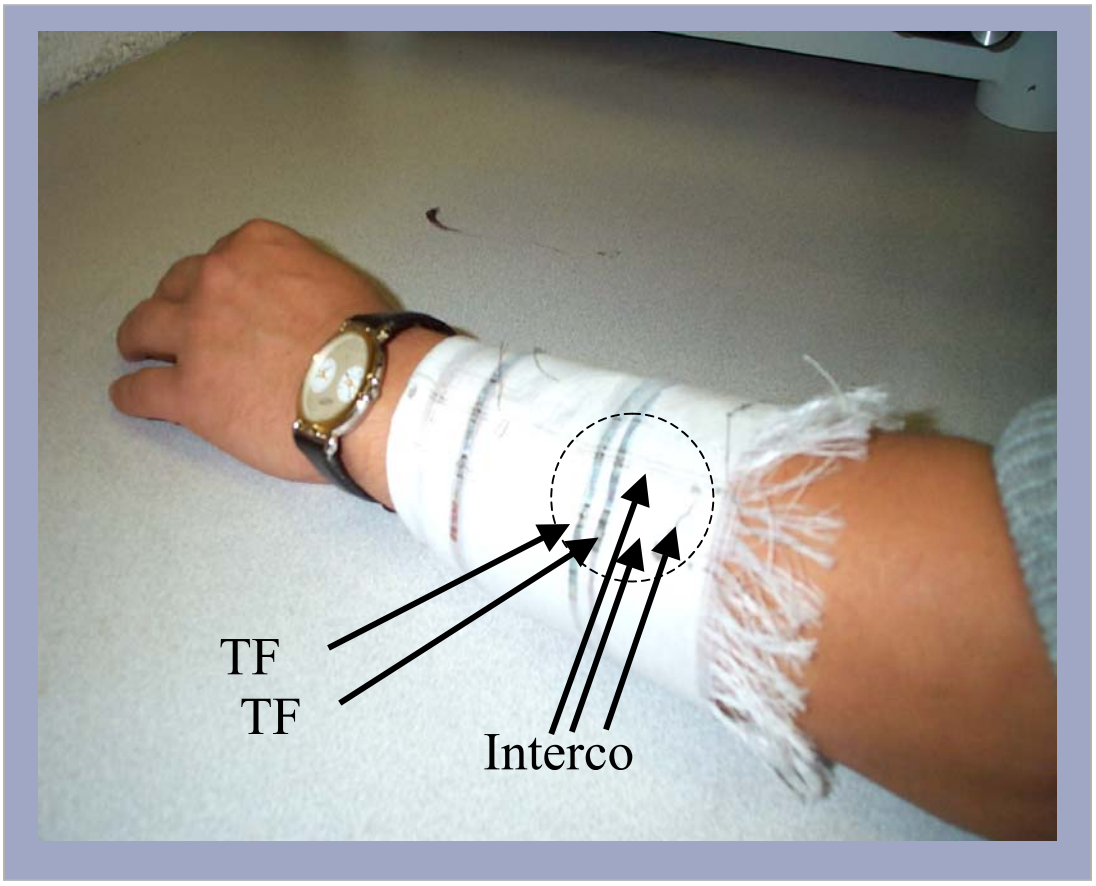


Figure 37. Wearable integrated Circuit: inverter structure

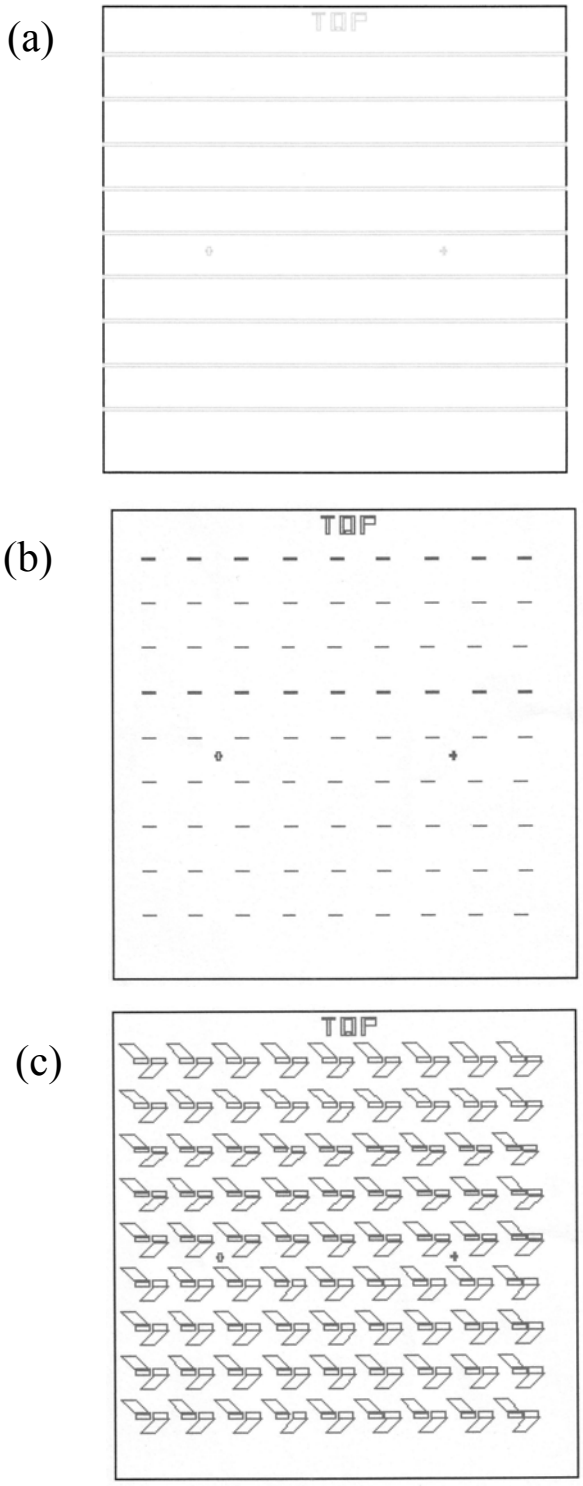
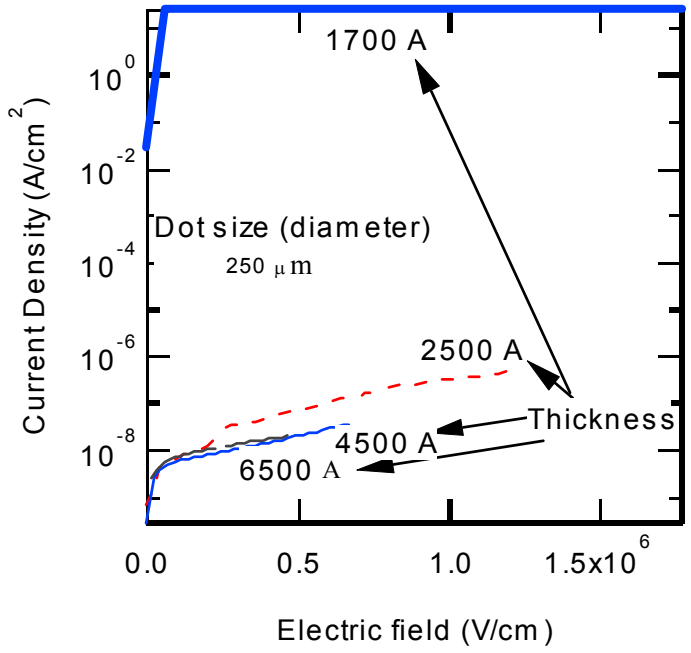


Figure 38. Mask design set #2 for TFTs
(a) gate (b) a-Si island (c) contact

(a)



(b)

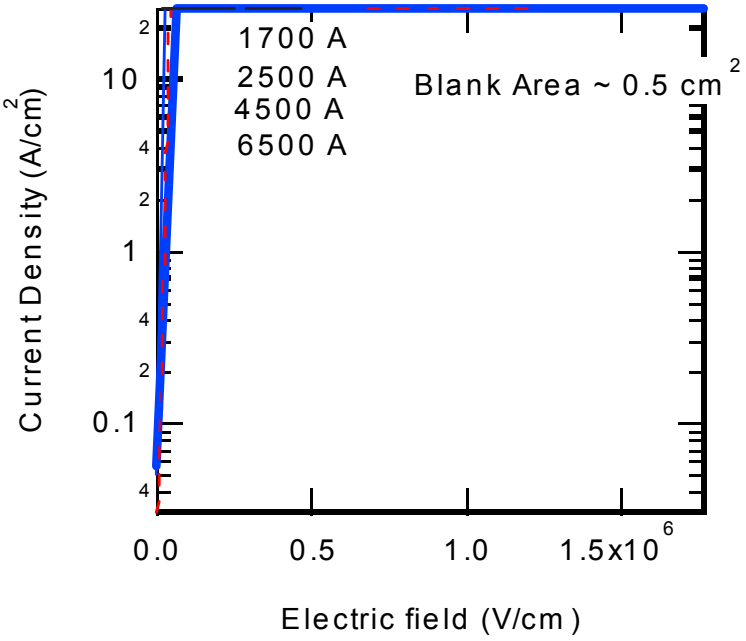
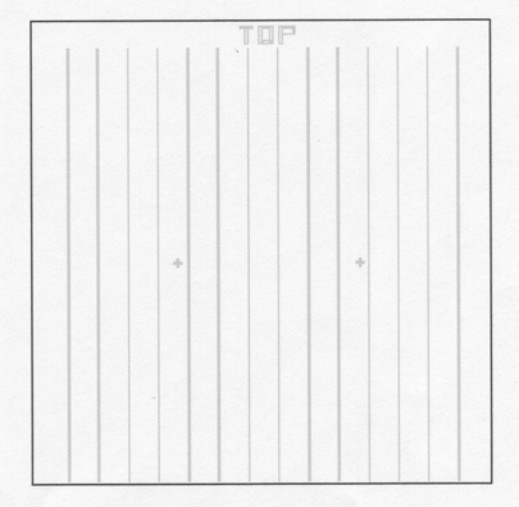
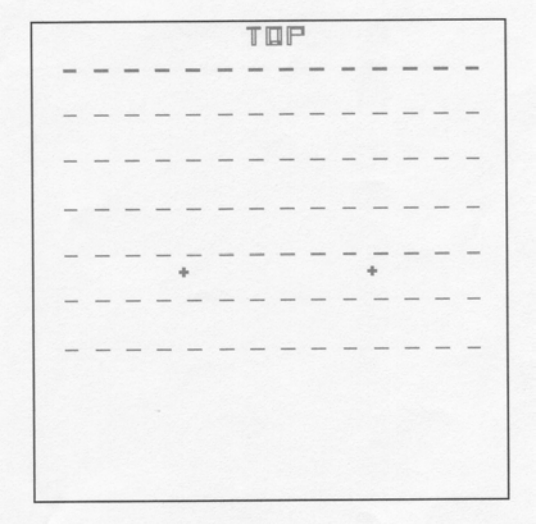


Figure 39. Electric field vs. Current density for Metal-Insulator-Metal structure with various nitride thickness
(a) Area: ~7x10^{-4} cm^2 (b) ~0.5 cm^2

(a)



(b)



(c)

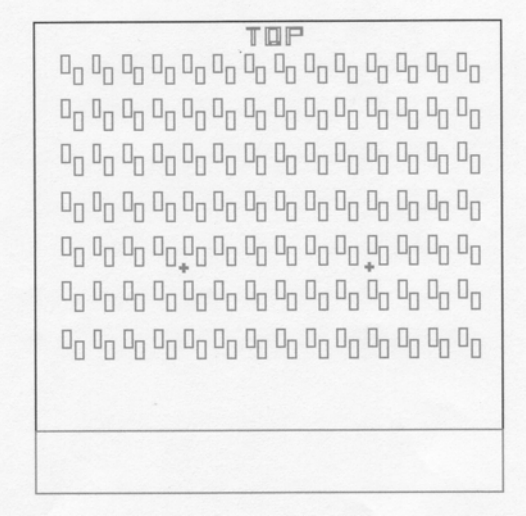


Figure 40. Mask design set #3 for future TFTs
(a) gate (b) a-Si island (c) contact