ABSTRACT

OZBEK, AYSE M. Schottky Barrier GaN FET Model Creation and Verification using TCAD for Technology Evaluation and Design. (Under the direction of Assistant Professor Doug W. Barlage).

Practical realization of low-power, high-speed transistor technologies for future generation nano-electronics can be achieved with novel structure logic devices such as ultra-thin body SOI MOSFET, double-gate MOSFET, tri-gate, FinFet or using novel materials instead of silicon such as Gallium Nitride (GaN). Novel Structures are the most promising candidates for logic devices with sub-20nm gate length. These novel structures can increase gate control and suppress short channel effects. To compare the feasibility of these different structures and to project the device performance, technology CAD (TCAD) simulation is a reasonable method.

With advantages from GaN channel material and heterogeneous source drain Schottky barrier FET structure, it is expect to see a novel device with promising performance in low power high speed digital application, and possibility for high power high frequency application.

This research focuses on the modeling of Nickel Schottky Barrier Source GaN MOSFET and the modeling of Vertically Insulated Gate AlGaN/GaN HFET by using TCAD. Schottky Barrier IGBT on GaN structure is also demonstrated for future power applications.

Schottky Barrier GaN FET Model Creation and Verification using TCAD for Technology Evaluation and Design

by

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DEDICATION

To

My Mother Inci Ozbek

and

My Father Emin Ozbek

BIOGRAPHY

Ayse M. Ozbek was born in Elazig, Turkey in February 1983. She joined Bilkent University in Ankara, Turkey in 2001. She graduated with a Bachelor of Science in Electrical and Electronics Engineering in 2006. In August 2006, she began her graduate studies in Electrical Engineering at North Carolina State University. Her focus has been on IC Fabrication and Nanotechnology. While working towards her Masters degree, she worked on her thesis under the guidance of Dr. Douglas W. Barlage. During this work she performed research on device simulation and modeling of III-nitride semiconductor based devices alternative to silicon based traditional MOSFET.

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Chapter 1

Introduction

1.1 Overview

Power semiconductor devices are a key component of all power electronic systems. It is estimated that as much as 50 percent of the electricity used in the world is controlled by power devices. Power devices have a major impact on the economy, because they determine cost and efficiency of systems. Power semiconductor devices have taken a dominant role with silicon serving as the base material after replacing vacuum tubes by solid state devices [1]. Bipolar power devices, such as bipolar transistors and tyristors, were first developed in the 1950s. Their power ratings and switching operating frequencies increased with better understanding of the operating physics and availability of more advanced lithography capability [1]. The power MOSFET has become the device of choice due to its inherent high switching speed and its high input impedance under steady state conditions [2]. However in order to minimize the power losses in power MOSFET, the on resistance value should be reduced, which can be achieved by increasing the device die area and by reducing the specific on resistance.Therefore, other semiconductor materials are considered to have further improvements in device performance.In the early 1980s, replacing silicon with wide band-gap semiconductors was suggested. The basis of this approach is based on the Figure of Merit equations. The physical properties of Gallium Nitride (GaN), high saturation velocity, high breakdown fields, high electron mobility, wide bandgap energy and high thermal conductivity make it a promising material for field effect transistor (FETs) devices for high speed, high power, and small channel length applications [3].

1.2 Motivation for GaN based FET Transistors

Gallium Nitride is a promising material for high-voltage and high temperature devices due to its remarkable material properties like wide bandgap (3.4 eV), large critical electric field (3 MV/cm) and a high saturation velocity (1.9x10^7 cms^{-1}) [4]. In addition to its good characteristics, alloys of GaN are also utilized in device engineering. InGaN and AlGaN materials offer a wide range of band gap 0.8 eV to 6.2 eV. This enables the design and fabrication of novel devices.

As the Si CMOS scaling keeps down, the short channel effect is getting more pronounced. However GaN is also a potential candidate for very short channel devices due to its material properties such as its large band gap, high saturation velocity and high thermal conductivity [5]. GaN also has an advantage over Si, because it suppress the source/drain leakage, supporting larger drive current, and eases the restriction of the device cooling [6].

Comparison of semiconductor materials' figures of merit is an efficient way to find out their device characteristics. Power handling, power loss and RF performance of a semiconductor material can be estimated from its figure of merits. The Johnson's figure of merit, JFOM= $(v_{sat}\ E_B/2\pi)^2$ is a merit for RF performances like cut-off frequency (f_c) and maximum power handling capacity. Since it relates saturation velocity and breakdown voltage, it demonstrates the high power and high performance capability of material. Keye's figure of merit, KFM= $K^*(v_{sat}\ E_B/4\pi\ \epsilon)^{0.5}$ is a merit for considering thermal limitation. Baliga's figure of merit, BFM= $\epsilon^*\mu^*(E_G)^3$ is a merit for power switching. BFM defines material parameters to minimize the conduction losses in power FETs [7].Baliga's figure of merit, BHFM= $\mu^*(E_B)^2$ is a merit for high frequency power switching.In Table 1.1, normalized FOMs for different materials are given and normalization is done by setting FOM of Si to 1. It is seen that in high power and high frequency applications GaN based devices capability is much better than Si, 4H-SiC and GaAs.

Table 1.1: Figures of merit for different materials

	JFM	KFM	BFM	BHFM
Si	1	1	1	1
GaAs	11	0.45	28	16
4H-SiC	410	5.1	290	34
GaN	790	1.8	910	100

High power handling of GaN power transistors have already been demonstrated by fabrication of GaN high electron mobility transistor (HEMT) and field effect transistor (FET) devices. Even though GaN based HEMTs have high power handling, they have several drawbacks. The leakage from the Schottky gate of such devices is a major concern for operating at elevated temperatures. However as an alternative, the use of an insulated gate metal oxide semiconductor (MOS) structure has some advantages. MOSFET reduces both the gate leakage and power consumption and it has better temperature sensitivity, because it does not suffer from the severe leakage of Schottky based devices. MOSFET also can use high temperature implantation to form highly doped source and drain without compromising the gate contact [8]. The use of MOSFET also allows the use of complementary devices and therefore it consumes less power and it will have a simpler circuit design. GaN based MOSFET is possible to achieve competitive performance comparing with GaN HEMT in high power and high frequency applications by using the recently available techniques to achieve low density of GaN insulator interface states in GaN MOSFET devices [9]. Using Schottky barrier metal source/drain MOSFET (SB-MOSFET) on GaN have been extended beyond the Si Schottky barrier MOSFET, because manufacturing process for GaN SB-CMOS is simpler than conventional bulk CMOS, requiring fewer process and photolithography steps and also the Schottky metal can be used as the carrier rich source/drain, which excludes the ion implantation and thermal diffusion from the manufacturing [8]. Metal source/drain also mitigates the scaling limitation of S/D doping profile control, sheet resistance and contact resistivity.

The most interesting feature of GaN and its alloys is their highly piezoelectric structure offering devices not possible with other III-V material systems like GaAs and InP. A two dimensional electron gas (2DEG) region forms at AlGaN/GaN hetero-junction with enhanced electron mobility. Due to its material properties, AlGaN/GaN heterojunction field-effect transistors have been developed for high power and high frequency amplifiers. AlGaN/GaN HFET is a promising candidate for post-Si high power switching devices.

Therefore GaN based Schottky barrier source/drain MOS structure and AlGaN/GaN HFET structure is explored in this research. With advantages from GaN channel material and heterogeneous source drain Schottky barrier FET structure, it is expected to see a novel device with promising performance in low power high speed digital application, and possibility for high power high frequency application.

1.3 Outline of the thesis

The thesis consists of 5 chapters.

Chapter 1 contains the introduction for the thesis and the motivation for using GaN MOSFET and GaN HFET devices. In Chapter 2, the theory of Schottky Barrier Metal Semiconductor Junctions, material properties of different semiconductor materials and polarization effect are described.

Chapter 3 explains the modeling of Schottky Barrier Source/Drain GaN MOSFET and the comparison of simulation and experimental data. Vertically Insulated Gate AlGaN/GaN HFET device model is explained in Chapter 4. Also in chapter 4, the new Vertically Insulated Gate Schotkky Barrier GaN MOSFET is demonstrated.

Finally, Chapter 5 contains the discussions regarding this work and future research directions are explained in this chapter.

Chapter 2

Theory and Design

This chapter starts with the some information about GaN. It is followed by the basics of metal semiconductor contacts. Then some information about Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and some information about High Field Effect Transistors (HFETs) are given.

2.1 Material Properties

Silicon (Si) and Germanium (Ge) are group IV elements in the periodic table. Gallium (Ga), Indium (In), Aluminum (Al) are all group III elements. Nitrogen (N), Arsenic (As), Antimony (Sb), Phosphorus (P) are all group V elements. By combining group III elements with group V elements, III-V compound semiconductors can be formed. The electron configuration of Gallium Nitride (GaN) is [Ar] $4s^2 4p^1$ for Gallium (Ga) and [He] $2s^2 2p^3$ for Nitrogen (N). By sharing 4p and 2p electrons through the covalent bond, the compound Gallium Nitride (GaN) forms. Also other III-V compound semiconductors such as GaAs and InP can be formed in the same way. In Table 2.1, the bulk material properties are summarized for Si, GaAs, GaN and InSb [8]. As can be seen from the Table 2.1, GaN has superior transport properties for high temperature and high power applications, if compared with the others [10].

Table 2.1: Material Properties of Si, GaAs, GaN, 4H-SiC and InSb

	Silicon	GaAs	GaN	4H-SiC	InSb
Bandgap energy (E_g eV)	1.12	1.42	3.41	3.26	0.17
Dielectric constant (ϵ_r)	11.8	12.8	9	9.7	17.7
Thermal conductivity (k_{th} W/cm/K)	1.5	0.46	1.3	3.7	0.18
Breakdown field (E_B V/cm	$3x10^5$	$5x10^5$	$3.3x10^6$	$3x10^6$	$1x10^3$
Saturation velocity (v_{sat} cm/s)	$1x10^7$	$2x10^7$	$3x10^7$	$2x10^7$	$6x10^7$
Electron mobility (μ_e cm^2/Vs)	1350	8500	1200	900	7800
Hole mobility (μ_h cm^2/Vs)	450	400	200	120	850

2.2 Metal-Semiconductor Contacts

The contact theory described below is taken from the standard metal-semiconductor contact model listed in books either by Streetman [11]. There are two types of contacts between metals and semiconductors. The first one is Ohmic contact and the second one is Schottky (rectifiying) contact [12].

2.2.1 Schottky Contacts

Rectifying metal-semiconductor contact is named as Schottky after W.Schottky proposed a model for barrier formation in 1931 [13]. An energy of $q\phi_m$ is required to remove an electron at the Fermi level to the vacuum outside the metal. When a metal with work function $q\phi_m$ is contacted with a semiconductor with work function $q\phi_s$,a potential barrier is formed due to the separation of charges at the metal-semiconductor interface [14]. The potential barrier height ϕ_B for electron injection from the metal into the semiconductor conduction band is ϕ_m - ξ, where $q\xi$ (called the electron affinity) is measured from the vacuum level to the semiconductor conduction band edge.Energy band diagrams of Schottky contacts on n- and p- type contact under thermal equilibrium are shown in Figure 2.1.

When a forward bias voltage V is applied to the Schottky barrier shown in Figure 2.1.a. , the contact potential reduces from V_i to V_i - V and as a result of that, electrons in the semiconductor conduction band can diffuse across the depletion region to the metal. This gives rise to a forward current (Metal to semiconductor) through the junction. A reverse bias increases the junction barrier to V_i + V and because of that electron flow from semiconductor to metal becomes negligible. The resulting current voltage characteristics is

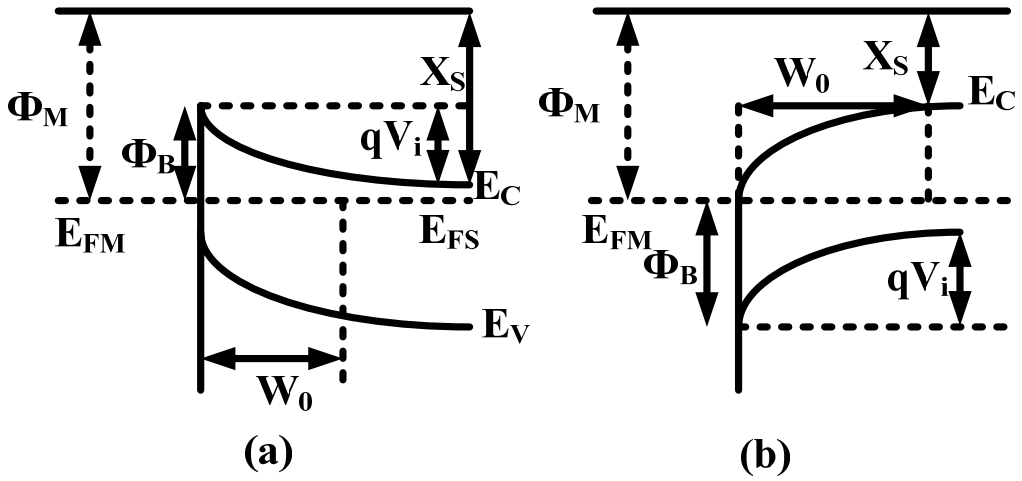

Figure 2.1: Energy band diagrams of metal contact to n-type (a) and p-type (b)

given by the relationship,

$$I = I_S(exp(\frac{qV}{nkT}) - 1), \tag{2.1}$$

where I_S, n and A* are the reverse saturation current, ideality factor and the modified Richardson constant, respectively. The formula implies that the reverse current saturates, however the forward current increases exponentially with the applied bias. The metal source drain Schottky barrier MOSFET (SB-MOS) was first investigated by Nishi in 1966 when he submitted a Japanese patent on the idea [15]. Several metal properties are given in the Table 2.2.

GaN Schottky junctions have been fabricated and studied recently. The following tables summarize several metals for GaN Schottky contact and the Schottky barrier height. Among all the metals which have being investigated so far on GaN, titanium (Ti), nickel (Ni), and Chromium (Cr) are the most promising candidates for their low Schottky barrier on GaN [16] [17].

2.3 Polarization in GaN

The polarization in GaN is described by Morkoc et al. in detail [17]. The wurtzite crystal structure of III nitrides are tetrahedrally coordinated and lack the inversion symmetry in the unit cell. Due to this non-centro symmetric structure and large ionicity

Table 2.2: Several Metal Properties

	Work function	Resistivity	Thermal conductivity
	(eV)	(10^{-6} Ohm-cm)	W/cm K
Platinum (Pt)	5.65	9.6	0.716
Nickel (Ni)	5.15	6.16	0.907
Pladdium (Pd)	5.12	9.78	0.715
Gold (Au)	5.10	2.05	3.17
Tungsten (W)	4.55	4.82	1.74
Chromium (Cr)	4.50	11.8	0.937
Titanium (Ti)	4.33	39	0.219
Niobium (Nb)	4.30	15.20	0.537
Aluminum (Al)	4.28	2.42	2.370
Tantalum (Ta)	4.25	12.20	0.575
Magnesium (Mg)	3.66	4.05	1.56

Table 2.3: Metal p-GaN Schottky contact properties

Metal	Ideality factor (n)	Barrier Height (eV)
Platinum (Pt)	1.15	0.5
Nickel (Ni)	1.44	0.50
Gold (Au)	1.27	0.57
Titanium (Ti)	1.36	0.65

associated with the covalent metal nitrogen bond, a spontaneous polarization occurs along the hexagonal c-axis [18]. Group III nitride materials have also large piezopolarization (PE) coefficients. Misfit strain and the thermal strain, which are caused by the thermal expansion coefficient difference between the substrate and the epitaxial layer, causes the strain related piezoelectric effect in heterostructures. The effect of strain induced polarization on band structures can have a significant effect when there are hetero-interfaces in a structure. Heterojunction devices such as HFETs are based on control of free carriers and band structures at hetero-interfaces [18]. Polarization is due to piezoelectric effects and the difference in spontaneous polarization between AlGaN and GaN in GaN/AlGaN based FETs. The effect of strain induced polarization is lowered when the strain is reduced by misfit dislocations [18]. Polarization has an important effect on III-N electronic devices, because piezoelectric field is superimposed to the band energies. If the modulation charge is the basis of operation for the device, polarization charge and the strain management of the thin film layers can result in increasing the sheet carrier density at the interface, which

Table 2.4: Metal n-GaN Schottky contact properties

Metal	Ideality factor	Barrier Height	Richardson Constant
	(n)	(eV)	A* ($Acm^{-2}K^{-2}$)
Platinum (Pt)	1.05	1.08	64.7
Nickel (Ni)	1.04	0.99	11.2
Gold (Au)	1.03	0.844	0.006
Titanium (Ti)	1.29	0.25	0.02

forms a two dimensional electron gas (2DEG) [19].

2.4 Design

Technology CAD(TCAD) refers to using computer simulations to develop and optimize semiconductor processing technologies and devices. TCAD simulation tools are designed to solve fundamental, physical partial differential equations, such as diffusion and transport equations for discretized geometries, representing the silicon wafer or the layer system in a semiconductor device. TCAD consists of 2 main branches: process simulation and device simulation. The family tree view, as shown in Figure 2.2,shows the simulations in Sentaurus Workbench. It defines the squence of tools and parameters that are used in the simulation.

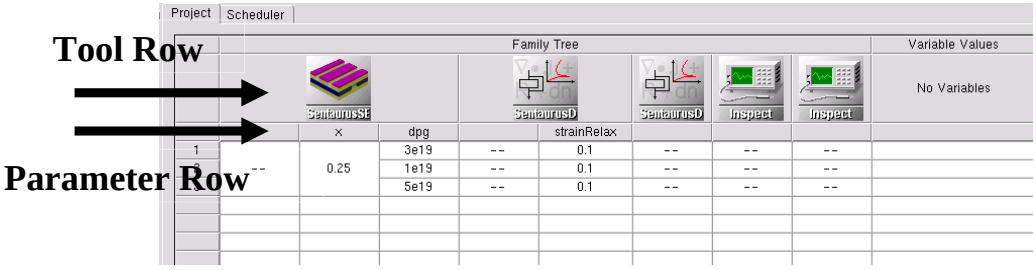

Figure 2.2: The family tree view

Sentaurus Process is an advanced 1D, 2D and 3D simulator for developing and optimizing silicon and compound semiconductor process technologies. In process simulation, processing steps such as etching,ion implantation,thermal annealing and oxidation are simulated based on physical equations. The simulated part is meshed and represented as a

finite element structure, as shown in Figure 2.3.

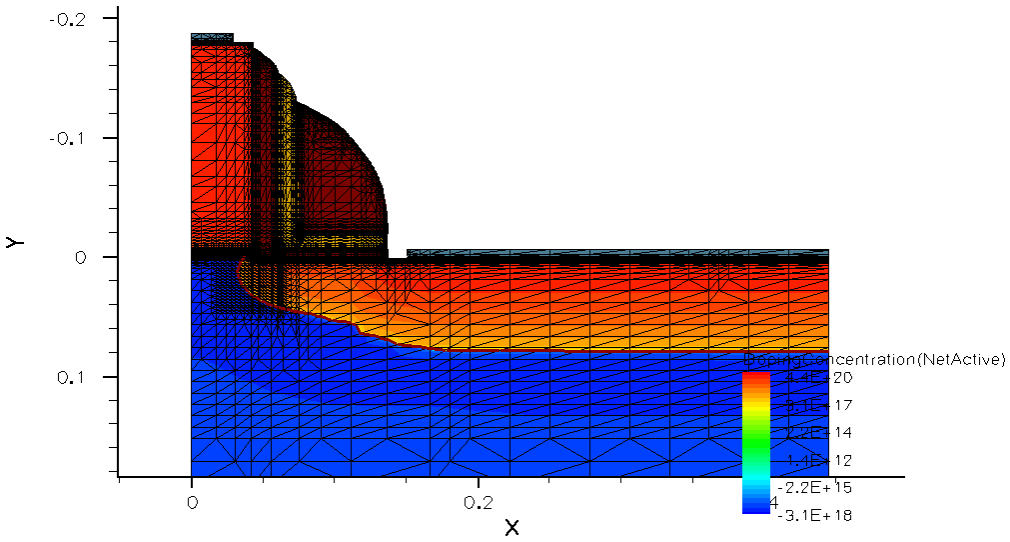

Figure 2.3: Cross Section of NMOS

Sentaurus Structure Editor is a 2D and 3D device editor, and 3D process emulator. It has three distinct operational modes: 2D structure editing, 3D structure editing, and 3D process emulation [20]. Geometric and process emulation operations can be mixed freely. From the graphical user interface (GUI), 2D and 3D device models are created geometrically using 2D or 3D primitives such as rectangles, polygons, cuboids, cylinders, and spheres. Three-dimensional regions can also be created by simple extrusion of 2D objects or by sweeping 2D objects along a path.

Doping profiles and meshing strategies are defined interactively. Placements are visualized as semitransparent boxes for easy verification. All doping and meshing options of the mesh generation tools Mesh and Noffset3D are supported. Synopsys provides two state-of-the-art approaches for the automatic generation of meshes. The quadtree/octree-based method Mesh creates meshes with an axis-aligned structure that is fitted to the boundary.

Sentaurus Device simulates the electrical, thermal, and optical characteristics of semiconductor devices. It is the leading device simulator and handles 1D, 2D, and 3D geometries, mixed-mode circuit simulation with compact models, and numeric devices [21]. It contains a comprehensive set of physical models that can be applied to all relevant

semiconductor devices and operation conditions. Sentaurus Device is used to evaluate and understand how a device works, to optimize devices, and to extract SPICE models and statistical data early in the development cycle. Applications of Sentaurus Device include VDSM silicon, where Sentaurus Device has proven accuracy to well below 100 nm technology; silicon-on-insulator (SOI) devices, where Sentaurus Device is known for its robust convergence and accuracy; double-gate and FinFET devices, where quantum transport is a reality; SiGe; thin-film transistors; optoelectronics; heterojunction HEMTs and HBTs; and power and RF semiconductor devices.

Synopsys has integrated and customized Tecplot, a dedicated software for scientific visualization. Tecplot, Inc. is a company with a long history of providing high-quality engineering and scientific visualization tools. Tecplot SV is a plotting software with extensive 2D and 3D capabilities for visualizing data from simulations and experiments [21]. It represents state-of-the-art scientific visualization. In addition, it is used to explore and analyze data, to produce informative 2D and 3D views, to create presentation-quality plots and animations, and to share results on the Web. The versatility and high-quality output of Tecplot SV gives users total control in order to obtain all types of required plot.

Inspect is a plotting and analysis tool for x-y data, such as doping profiles and electrical characteristics of semiconductor devices. The graphical user interface allows for quick access to the appropriate curve data. A script language and a library of mathematical functions allow users to compute with curves, and to manipulate and extract data from simulations. The extracted values can be returned to Sentaurus Workbench for further applications.

Chapter 3

Schottky Barrier GaN MOSFET

3.1 Introduction

Gallium Nitride (GaN) is currently a strong research area with its potential for use as a Radio Frequency (RF) and power device due to high breakdown voltage and thermal capacity [22]. The GaN p-HEMT has specifically been added to the ITRS roadmap in recent years as a device for RF Wireless applications. In an effort to decrease gate leakage and off-state current, an enhancement mode MOSFET structure is an attractive alternative to these depletion mode devices. Several methods for source-drain formation have been investigated previously for GaN FETs, such as ion implantation and selective area regrowth [23]. Past research and recent developments in silicon have provided another option, Schottky source-drain. The Schottky Barrier MOSFET (SB-MOSFET) allows for shallower junctions and decreased drain induced barrier lowering (DIBL), both of which are critical for device performance and scaling. This method also has the possibility for decreased source-to-drain leakage due to the potential barrier created by the Schottky interface (Figure 3.1). In GaN, a Schottky source-drain also offers an increase in mobile carriers over other methods.

GaN SB-MOSFET with Nickel source and drain was investigated by fabrication by L. Ma [8] and measured. Devices that were fabricated on 0.50 μm unintentionally doped GaN grown on c plane sapphire substrates by Metal-Organic Chemical Vapor Deposition (MOCVD). Schottky source and drain regions were formed through a BCl_3 Reactive Ion Etch (RIE) before Nickel electron beam deposition and lift-off. Silicon Nitride (100nm) was used as the gate dielectric with a Nickel/Gold (100nm/100nm) metal gate stack. The device measured is shown in Figure 3.2 with gate length Lg = 0.7 μm.

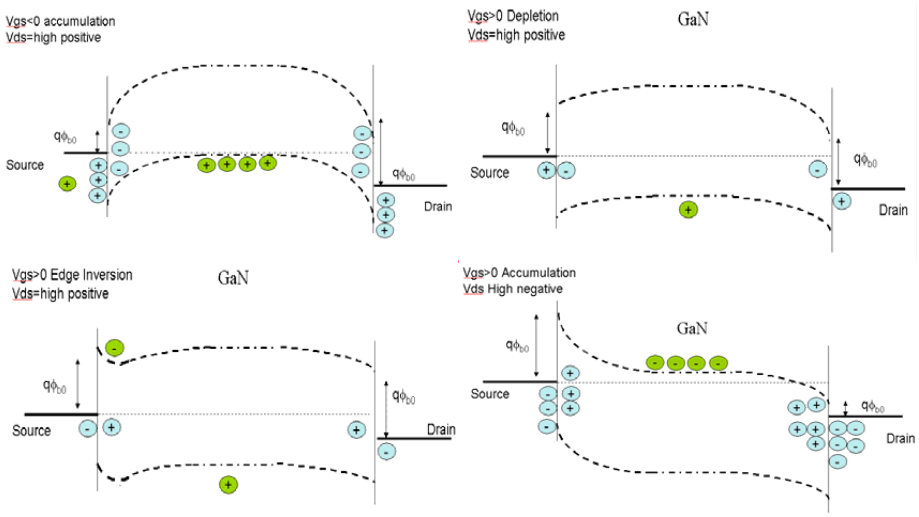

Figure 3.1: Energy Band diagrams of an n-type GaN Schottky barrier MOSFET channel in (a) Accumulation (b) Depletion (c) Edge Inversion and (d) Inversion

Figure 3.2: SB-MOSFET fabricated on GaN with nickel source-drain

DC characteristics of several one-finger i-GaN MOSFETs with metal source/drain were measured. V_{DS} was swept from 1 to 3.5V and V_{GS} from -8 to 3V. I_{DS}-V_{DS} and I_{DS}-V_{GS} plots are shown in Figure 3.3.

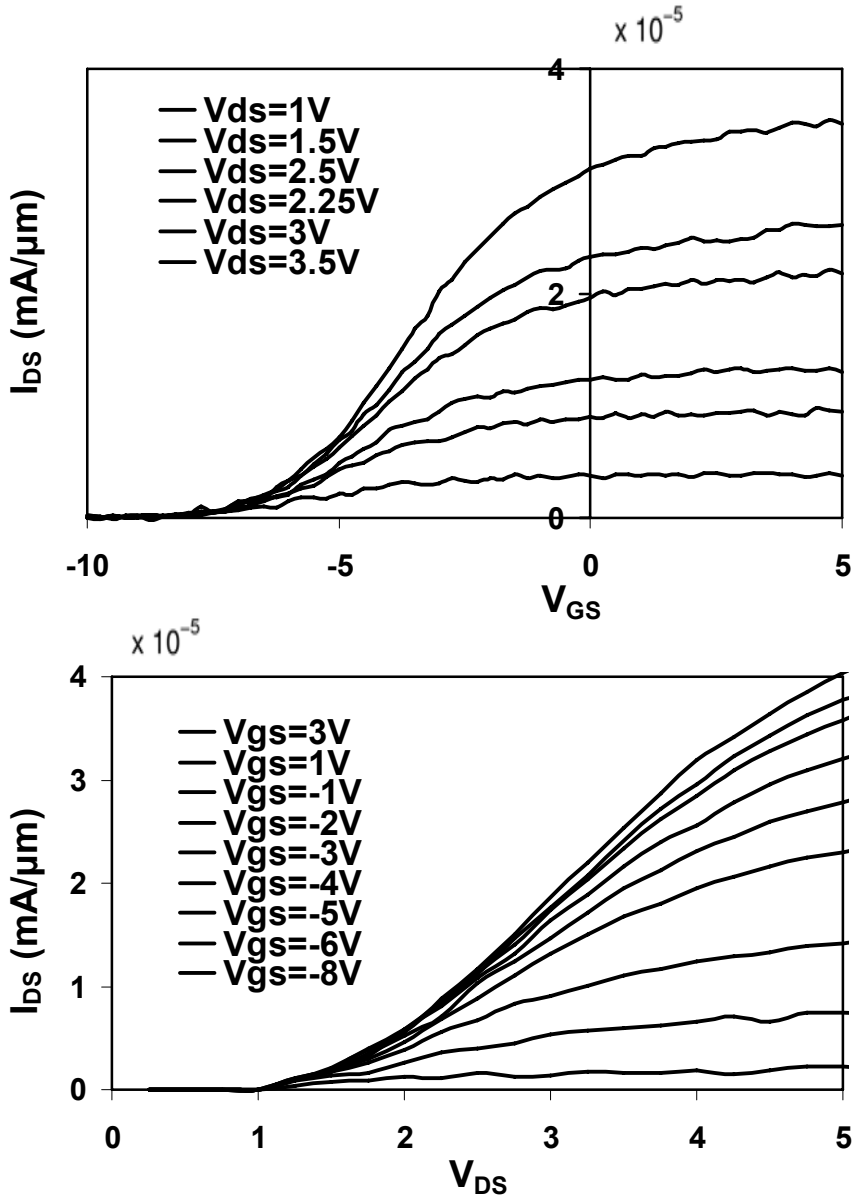

Figure 3.3: (a) V_{GS} from -8V to 3V (b) V_{DS} from 1 to 3.5V

GaN SB-MOSFET with Nickel source and drain is modeled by using ISE TCAD to optimize and project performance. The model is designed on the experimental device that is fabricated by L. Ma to obtain accurate results. Electrical characterization data of the experimental device was known and some of the device dimensions of the experimental device were known. The aim is to model the fabricated device by using the known device

dimensions and the electrical characterization data and fit the data that is obtained from the TCAD simulation to the experimental data. To model the device a strategy flow chart was followed. The strategy flow chart that was followed to fit the data is shown in Figure 3.4. First the device structure is designed by using Structure Editor and then the model was verified by using Techplot. If the structure of the device was correct, device module was defined. Device module includes the electrode section and the physics section. After running the simulation, simulation results were compared with the experimental data.

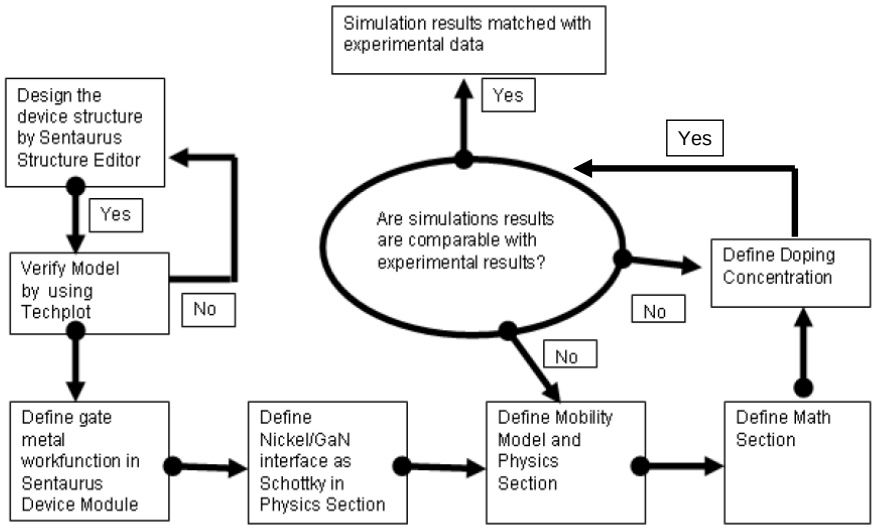

Figure 3.4: The strategy flow chart

3.2 Simulation Process

The SB-MOSFET with Nickel Schottky barriers as the source and drain are simulated by using Synopsys TCAD with Sentaurus Structure Editor, Sentaurus Device and Inspect modules. Sentaurus Structure Editor is used to define the GaN MOSFET structure and the meshing criteria. The structure of the simulated device is shown in Figure 3.5.

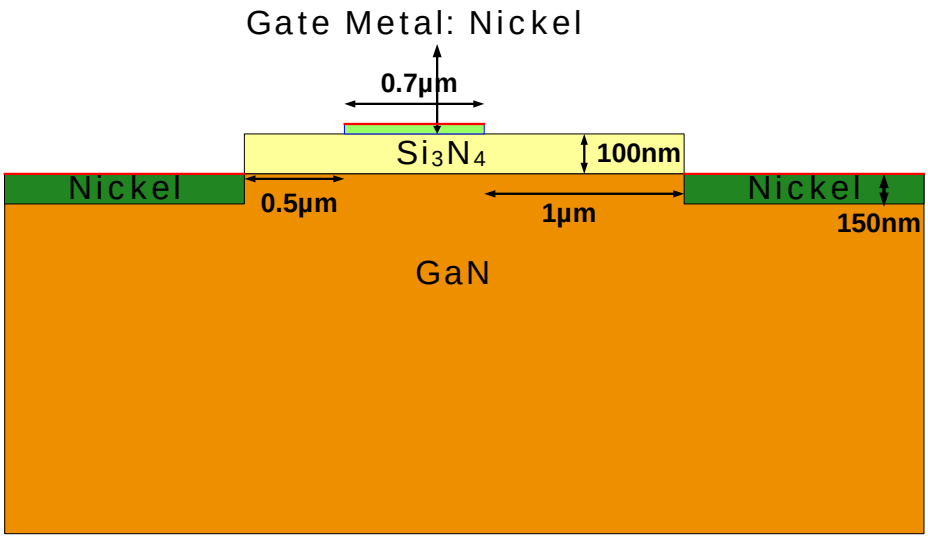

Figure 3.5: Structure of Schottky Barrier GaN Mosfet

The simulated device structure includes a GaN bulk layer, 150 nm thick Nickel source and drain regions, 100 nm thick Si_3N_4 gate dielectric region and Nickel gate metal. The device has a gate length of 0.7 μm, source is 0.5 μm and drain is 1.0 μm away from the gate. Si_3N_4 gate dielectric region has a length of 2.2 μm from the source to the drain region.

Sentaurus Device module simulates the electrical behavior of a semiconductor device. Contact potentials and the barrier height of the gate contact are defined in the Electrode section. Contact potentials for the source, drain and gate are defined as 0 Volts.Gate contact is also defined as Nickel by defining its work function, which is 5.15 eV, in the Electrode section.

Sentaurus Device allows different physical models to simulate semiconductor devices. Mobility model, generation-recombination rate, material-dependent parameters, interface and contact boundary conditions can be described in the Physics section. The first model that is described in this section is the mobility model. In doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility. The model for the mobility degradation due to impurity scattering is activated by specifying the 'DopingDependence' term in the Mobility section. In high electric fields, the carrier drift velocity is no longer proportional to the electric field, instead, the velocity

saturates to a finite speed v_{sat}. The high-field saturation models comprise three submodels: the actual mobility model, the velocity saturation model, and the driving force model. The driving force model is selected by the term 'eHighFieldSaturation (CarrierTempDrive)' in the Mobility section. The term CarrierTempDrive requires hydrodynamic simulation. Also, the default driving force model is chosen by specifying the term 'hHighFieldSaturation (GradQuasiFermi)'.

The second model that is defined in this section is the band gap model. The bandgap model is selected by using the 'EffectiveIntrinsicDensity' statement in the Physics section. The third model that is defined in this section is the recombination model. Generation-recombination processes are processes that exchange carriers between the conduction band and the valence band. Sentaurus Device has different parameters to describe generation-recombination model. Shockley-Read-Hall recombination, which is the recombination through deep defect levels in the gap, with doping dependence is used by specifying 'SRH (DopingDep)' term.

For metal-semiconductor interfaces, by default, there is an ohmic boundary condition. Therefore, Nickel/GaN interface is defined as Schottky in the Physics Section by using the syntax '(MaterialInterface = "Nickel/GaN") Schottky eRecVelocity= 2.573e6 hRecVelocity= 1.93e6'. The default values for eRecVelocity and hRecVelocity are used. The term 'Fermi' is also defined in the Physics section due to simulating a heterostructure device. For high values of carrier densities, the Fermi (Fermi-Dirac) should be used to have appropriate results. To activate the hydrodynamic model, the keyword Hydrodynamic (or Hydro) is specified in the Physics section. Because only one carrier temperature equation is to be solved, Hydro is specified as 'Hydro(eTemp)'. Also by default, the energy conservation equations of Sentaurus Device do not include generation-recombination heat sources. To activate them, the keyword RecGenHeat is specified in the Physics section. Anisotropic electrical permittivity is switched on by using the keyword Poisson in the Physics section. Sentaurus Device performs an I_{DS}-V_{DS} sweep with V_{DS} values ranging from 0 V to +4 V at a fixed V_G of 5 V, followed by an I_{DS}-V_{GS} sweep at V_D of 5 V and V_{GS} ranging from - 3 V to 2 V. I_{DS} versus V_{DS} curve and I_{DS} versus V_{GS} curve were plotted by Inspect module.

3.3 Comparison of Simulation and Experimental Data

After running the simulation, simulation results were compared with the experimental electrical characterization results. First the comparison was done when V_G equals 5 V and V_D equals 3V case. After observing the fitted data for that case, the total I-V curves were compared and it was observed that they also matched. By that way, it was determined that Schottky Barrier GaN MOSFET is modeled correctly.

Simulation and experimental results were compared for different V_{GS} values on the I_{DS}-V_{DS} curve and different V_{DS} values on the I_{DS}-V_{DS} curve. The pinch-off voltage was found to be approximately V_{GS} = -7.5V for both simulation and experimental data and also their maximum current values are the same. I_{DS}-V_{DS} and I_{DS}-V_{GS} curves that compare simulated and experimental data are shown in Figure 3.6 and Figure 3.7 respectively.

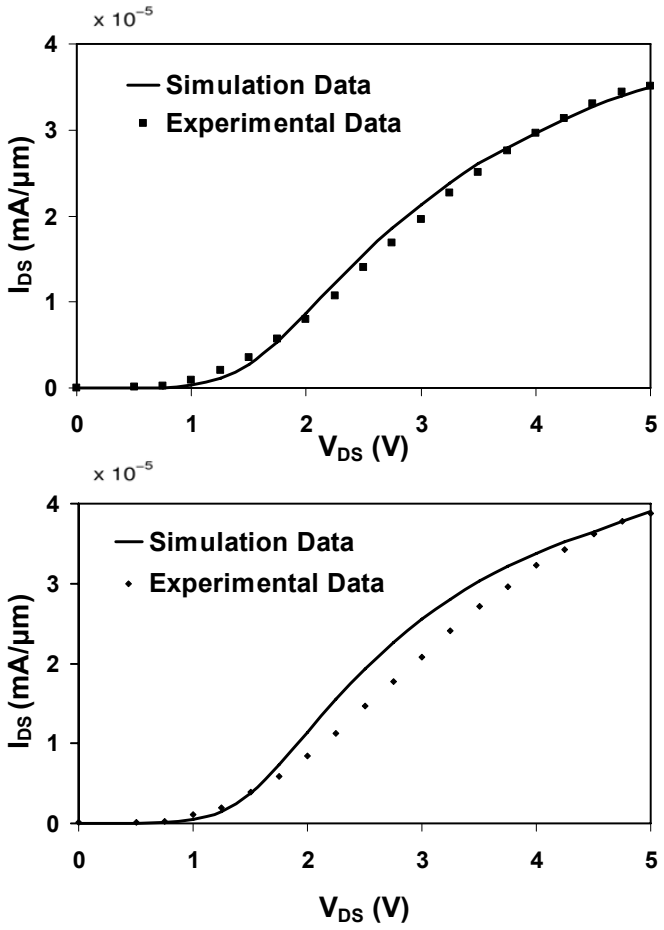

Figure 3.6: Comparison of I_{DS}-V_{DS} Curve for Experimental and Simulated Data when (a) V_G=-2V (b) V_G=0V

As can be seen from the plots, the experimental and simulated results are matched. They have the same pinch-off values and maximum drain current values. By comparing, their I-V curves, it is concluded that the Schottky Barrier GaN MOSFET is modeled correctly. However, there is a slight difference between the two curves. The first reason for this difference can be due to the defects. The simulation has no defects, however the actual device might have defects. Also, the modeling is done with 2 dimensional simulation. 3 dimensional simulation can give more accurate result, which can be fitted with the experimental result better than the 2 dimensional simulation.

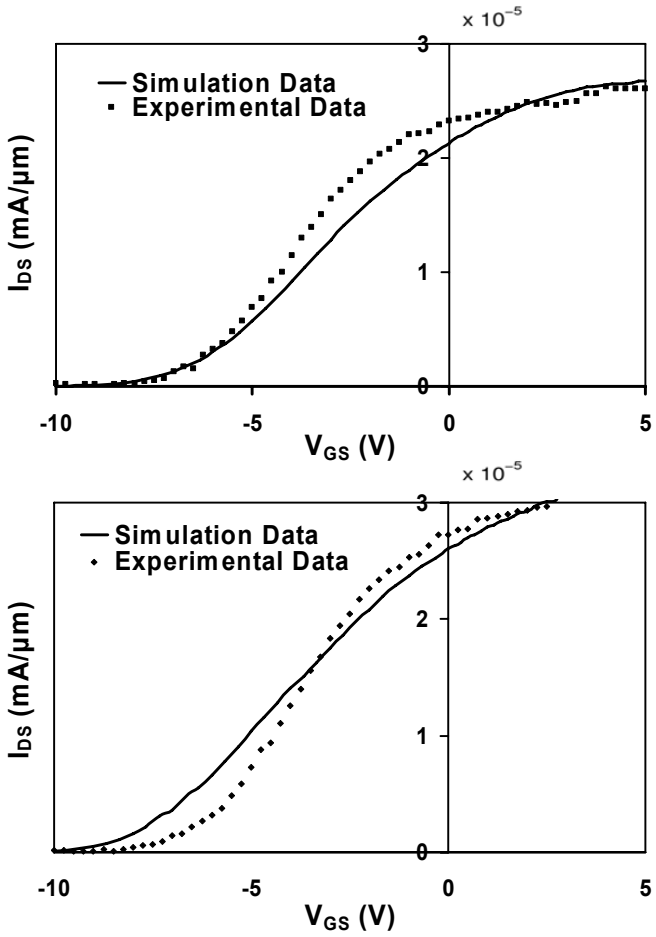

Figure 3.7: Comparison of I_{DS}-V_{GS} Curve for Experimental and Simulated Data when (a) V_D=3V (b)V_D=3.5V

3.4 Simulation Results

The general electrical characterization data of the simulated device also fits with the electrical characterization data of the experimental device. DC characteristics of Schottky Barrier GaN MOSFET that is defined by Structure Editor were plotted by using Inspect module. V_{DS} was swept from 0 V to +4 V at a fixed V_G of 5 V, followed by V_{GS} ranging from 3 V to -8 V at a fixed V_D of 5 V. I_{DS}-V_{DS} and I_{DS}-V_{GS} plots are shown in Figure 3.8 respectively.

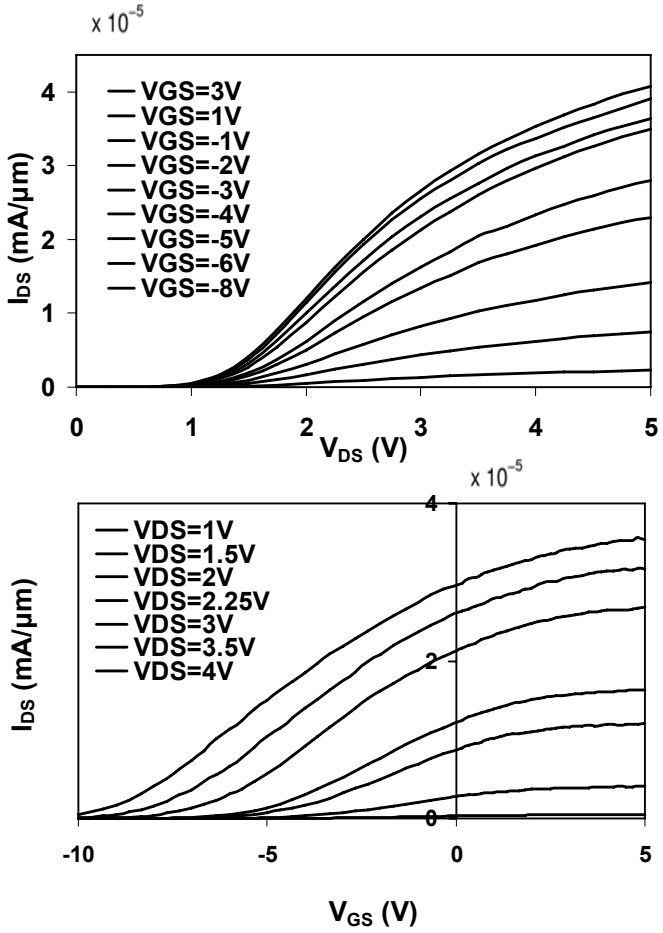

Figure 3.8: Drain current as a function of (a) drain potential for different gate voltages (b) gate potential for different drain voltages

3.5 Source-Drain Overlap Effect

The effect of source and drain spacing is examined to obtain the highest current. The Sentaurus Workbench parameter x is used by Sentaurus Structure Editor and defines the gate and source/drain overlap. Doping concentration of $2\text{x}10^{16}$ cm^{-3} is used for all device structures. Asymmetric device with source/drain spacing, symmetric device with no source/drain spacing and symmetric device with source/drain-gate overlap are simulated and the effect of overlap is examined. The structure of symmetric device at which source/drain overlaps 0.1 μm with gate is shown in Figure 3.9.

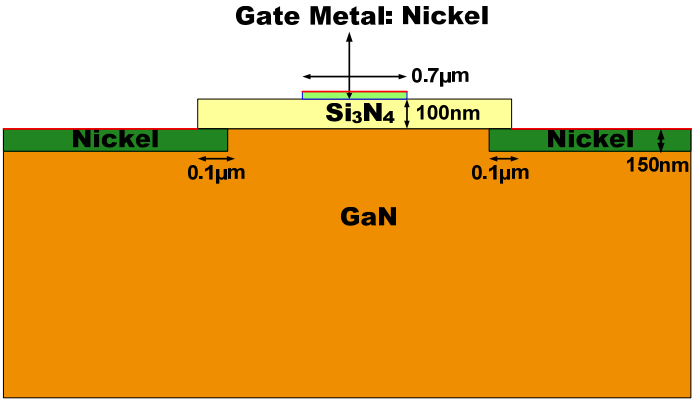

Figure 3.9: Structure of Schottky Barrier GaN Mosfet with 0.1 m source/drain-gate overlap

For V_{DS}=V_{GS}=4V, I_{ON} (mA/μm) versus distance and V_{th}(V) versus distance curve are shown in Figure 3.10. Spacing between source and gate is defined by d(μm). When d=-0.5 μm, spacing between drain and gate is 1 μm and spacing between source and gate is 0.5 μm. When d=-0.3 μm, spacing between drain and gate is 0.7 μm and spacing between source and gate is d=0.3 μm. When d=-0.1 μm, spacing between drain and gate is 0.5 μm and spacing between source and gate is d=0.1 μm. For positive values of d, the device is symmetric and the distance between source and drain to gate is the same as d.

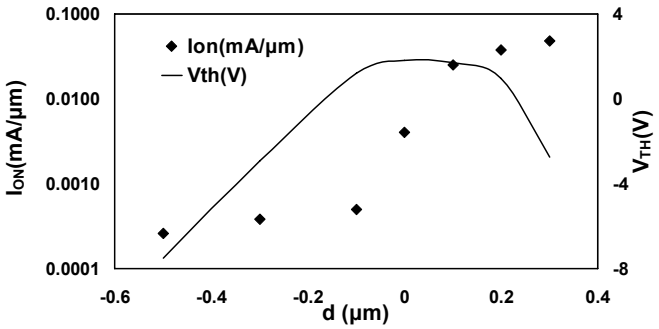

Figure 3.10: I_{ON} (mA/m) V_{th} (V) versus d(m)

As the source/drain spacing decreases and when source/drain overlaps with gate, the value of the drain current increases. The threshold value increases as distance between source/drain and gate decreases, but it will start decreasing as source/drain overlaps with the gate.

Chapter 4

Modeling of Vertical AlGaN/GaN Heterojunction Field-Effect Transistor

4.1 Introduction

The material properties of Gallium Nitride (GaN) make it an ideal candidate for high frequency, high temperature and high power electronic devices. AlGaN/GaN heterojunction contain high two dimensional electron gas (2DEG) with enhanced electron mobility [9]. Due to those material properties, AlGaN/GaN heterojunction field-effect transistors have been developed for high power and high frequency amplifiers. AlGaN/GaN HFET is a promising candidate for post-Si high power switching devices. This chapter details the modeling of vertically insulated gate AlGaN/GaN heterojunction field effect transistor (HFET) by using Synopsys TCAD.

The Vertically insulated gate HFET has apertures through which the electron current flows vertically. The reason of simulating vertical devices is their high-power switching capability, because they are more area efficient for both higher breakdown voltage and lower specific on resistance [24].

Vertically insulated gate AlGaN/GaN HFET was fabricated and measured by Kanechika et al [24]. The device was also modeled by Synopsys TCAD and the experimental and simulated data are compared within this chapter. The knowledge that is obtained from

the modeling of Schottky Barrier GaN MOSFET is also used in that modeling. The physics section, which is the most important part of the sentaurus device module, of the Schottky Barrier GaN MOSFET model is directly used for this simulation also. The physics section is important, because all physical models are defined in that section such as mobility model or band-gap model. Also the material files that are used for Schottky Barrier GaN MOSFET modeling is again used for the HFET modeling.

4.2 Simulation Process

The Vertically insulated gate AlGaN/GaN HFET was simulated by using Synopsys TCAD with Sentaurus Structure Editor, Sentaurus Device and Inspect modules. As it is mentioned in the introduction part, some of the parts that are used for the Schottky Barrier GaN MOSFET model is also used for that modeling too. However the most important concept for this simulation is the polarization and the polarization is defined in the sentaurus device module.

Sentaurus Structure Editor is used to define the GaN HFET and the meshing criteria. The structure of the device is shown in Figure 4.1. There are two important workbench parameters used for that simulation. The first one is the Sentaurus Workbench parameter x, which is used by Sentaurus Structure Editor and defines the mole fraction of the AlGaN barrier layer.

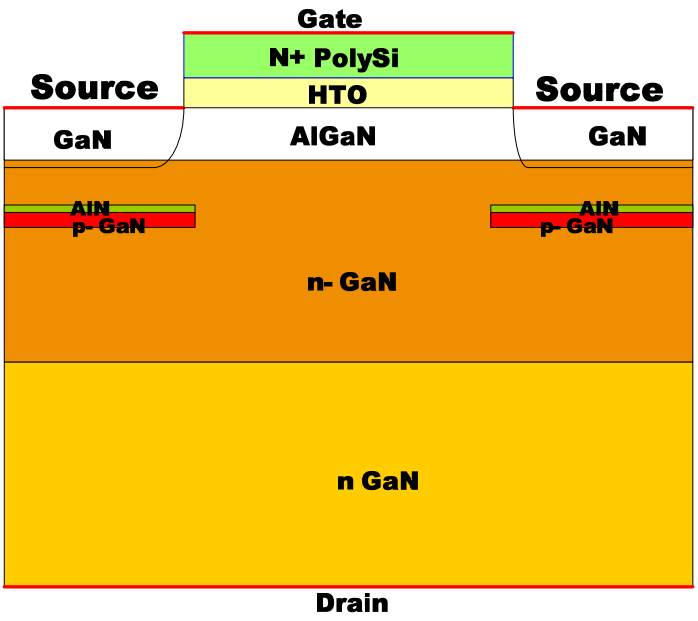

Figure 4.1: The structure of the vertically insulated gate AlGaN/GaN heterojunction field effect transistor (HFET)

The HFET structure, shown in Figure 4.1, has an n-type GaN substrate. On top of the substrate, there is a 3 μm thick n^- - GaN layer with a doping concentration of 1x10^{16} cm^{-3}. The p-GaN layer is 0.1 μm thick with a doping concentration of 3x10^{19} cm^{-3} and this layer blocks the current during the off-state. There is a 10-nm thick AlN layer on top of p-GaN layer to suppress the upward diffusion of the atoms in the p-GaN region and also to suppress the mass transport from the surface to the aperture region. The AlGaN layer is 15-nm thick and the source regions are n-GaN. SiO_2 layer is used as the gate insulator and there is a 250-nm thick n^+ doped poly-Si layer on top of it. The insulated gate allows higher voltage to be applied to the gate electrode and the gate leakage current to be reduced.

The mesh for the GaN HFET device is generated by Mesh, which is called from within Sentaurus Structure Editor with '(sde :build-mesh "mesh" "-s" "n@node@_msh")' to generate and save the mesh and '(system :command "mesh -F tdr n@node@_msh")' to build the mesh. The command-line option -F tdr instructs Mesh to use the TDR file format for the device structure file. Mesh also should be tight around hetero interfaces, especially where large variations in carrier concentration is observed, such as 2DEG Gas to obtain accurate results, therefore MultiBoxes are used at those areas.

Sentaurus Device module simulates the electrical behavior of a semiconductor device. One of the main characteristics of III-nitride materials is the presence of polarization vectors, with spontaneous and piezoelectric components. The primary effect of polarization is an interface charge due to abrupt variations in the polarization at the AlGaN-GaN hetero interface and at the AlGaN surface. The resulting values were automatically computed during the preprocessing phase in Sentaurus Workbench.

AlGaN and GaN has polarized wurtzite crystal structures, which have dipoles across the crystal in the [0001] direction. This macroscopic polarization includes spontaneous (pyroelectric) and strain induced (piepolarization) contributions, when there is no external field. Interface charge due to the abrupt divergence at the AlGaN-GaN heterointerface is the primary effect of polarization [25]. Sentaurus Device includes the divergence of polarization fields in the Poisson equation, however polarization effects were taken into account by using explicit charges at the heterointerfaces, where large polarization divergence are present, while modeling the GaN HFET device. The values of charges are computed while running the Sentaurus Device module. The computation follows the formulation by Ambacher, et al. [25]. Sentaurus Device module uses the Sentaurus Workbench parameter 'strainrelax' to compute a possible strain relaxation that leads to smaller piezopolarization charges. Acceptable values are from 0 to 1. In this simulation, it is assumed that GaN is fully relaxed and therefore its polarization vector only contains the spontaneous component, Psp(GaN). However for AlGaN, its polarization vector contains both the spontaneous and the piezopolarization component due to the strained AlGaN layer. The strain is computed using the in-plane lattice constant, a, of GaN and AlGaN:

$$\epsilon = (1 - r)\frac{(a_{AlGaN} - a_{GaN})}{a_{AlGaN}}, \tag{4.1}$$

where r is the amount of strain relaxation controlled by 'strainrelax'. The piezopolarization component of AlGaN is given by:

$$P_{pz}(AlGaN) = 2\epsilon(e_{31} - e_{33}\frac{c_{13}}{c_{33}}), \tag{4.2}$$

It is also assumed that only the vertical component of the polarization vectors is dominant. Therefore, the polarization vectors for GaN and AlGaN are given as

$$P_{Tz}(GaN) = P_{Sp}(GaN), \tag{4.3}$$

$$P_{Tz}(AlGaN) = P_{Sp}(AlGaN) + P_{pz}(AlGaN), \tag{4.4}$$

Heterointerface charges are computed from AlGaN surface and GaN-AlGaN interface as:

$$\sigma_{surf} = -[0 - P_{Tz}(AlGaN)], \tag{4.5}$$

$$\sigma_{AlGaN/GaN} = -[P_{Tz}(AlGaN) - P_{Tz}(GaN)], \tag{4.6}$$

The piezoelectric constants and mechanical constants that are used in the Sentaurus Device is given in the Table 4.1.

Table 4.1: The piezoelectric and mechanical constants for GaN and AlGaN

Constants	GaN	AlGaN
P_{sp}	-2.9x10^{-6}	-8.1x10^{-6}
e_{31}	-0.49x10^{-4}	-0.6x10^{-4}
e_{33}	0.73x10^{-4}	1.46x10^{-4}
c_{13}	103	108
c_{33}	405	373

Contact potentials for the source, drain and gate are defined as 0 Volts in the Electrode section of the Sentaurus Device. 'Hydro(eTemp)' is used in the Physics section, because hot electrons play an important role in the vertical charge transfer and subsequent capture in bulk traps. Anisotropic electrical permittivity is switched on by using the keyword 'Poisson' in the Physics section. The model for the mobility degradation due to impurity scattering is activated by specifying the 'DopingDependence' term in the Mobility model. The driving force model is also selected by the term 'eHighFieldSaturation (CarrierTempDrive)' in the Mobility model. The other models that are used for the Physics section of GaN HFET is same as the models that are used in the Physics section of the SB-MOSFET.

Sentaurus Device performs an I_{DS}-V_{GS} sweep at $V_D = 1$ V and V_{GS} ranging from -20 V to 0 V. I_{DS} versus V_{GS} curve were plotted by the Inspect module.

4.3 Simulation Results

The value of the 'strainrelax' is used as 0.1 and the value of the 'x', which is the mole fraction of the AlGaN barrier layer, is given as 0.25. The same values that are given by Kanechika et al [24] are used to compare experimental results with simulation results. The total current density figure of the vertically insulated gate GaN HFET is

shown in Figure 4.2. High two dimensional electron gas (2DEG) that is contained in the AlGaN/GaN heterojunction with enhanced electron mobility is shown in the Figure 4.3.

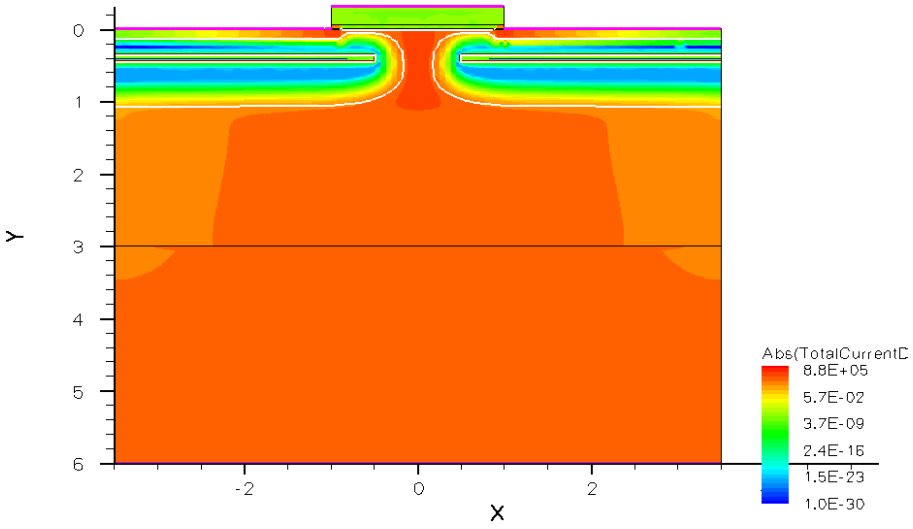

Figure 4.2: The Total Current Density Figure of Vertically Insulated GaN HFET

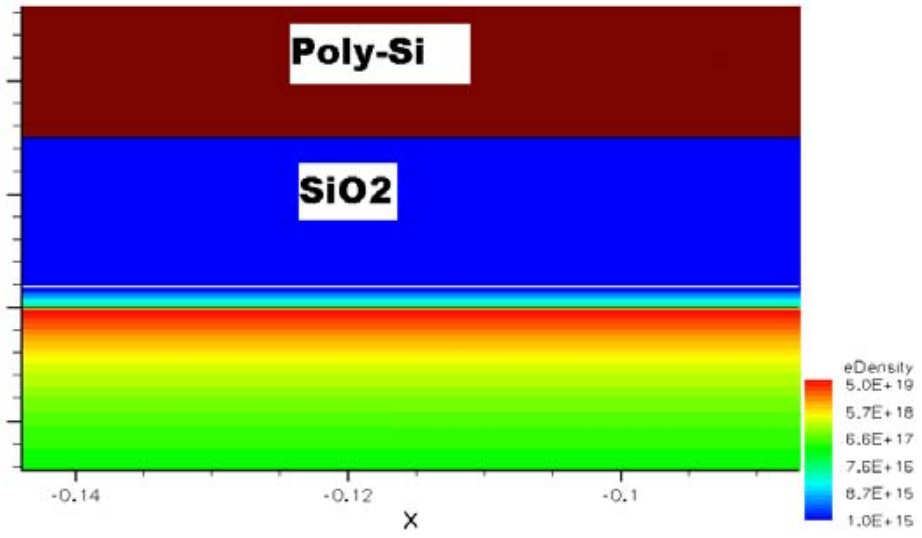

Figure 4.3: 2DEG Gas formed at the AlGaN/GaN interface

The I_{DS}-V_{GS} curve that is obtained from the simulation data is compared with the I_{DS}-V_{GS} curve obtained by experimental data given by Kanechika et al. in Figure 4.4

[24]. As can be seen from the figure, the value of maximum current and the threshold voltage are the same. P-type region dopant energy level and the defects inherent in the structure are the source of the difference in current. As explained before, mesh is one of the most important parts of this modeling. To obtain accurate results, mesh was increased and checked with the previous mesh result. If they were the same, that means that the results were accurate. If they were not the same, the mesh increased and checked again until the I-V curve becomes stable.

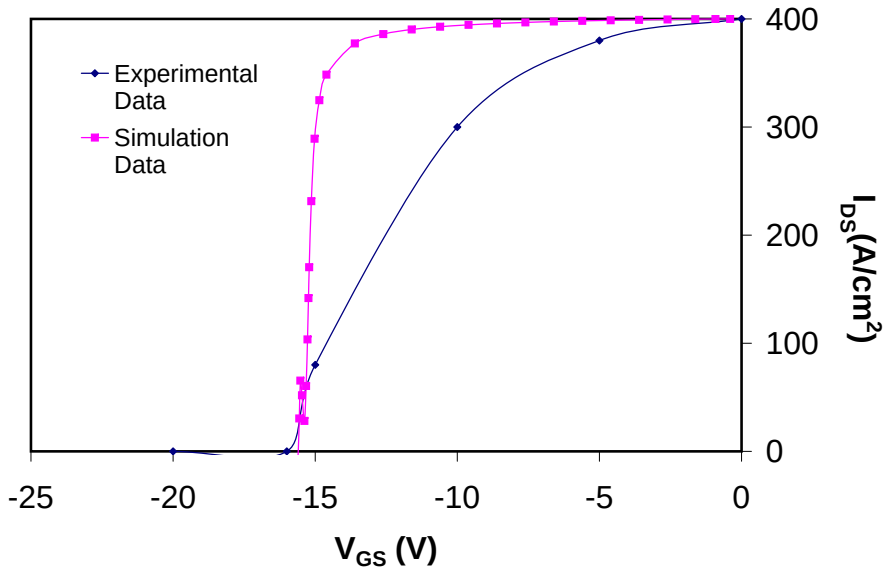

Figure 4.4: The comparison of experimental and simulated data

Device dimensions and workbench parameters are changed to observe their effect on pinch-off voltage value and the drain current value. Therefore oxide thickness and the length of p-GaN region are varied to observe the effect of device dimensions. Also mole fraction and strain relaxation values are varied to observe the effect of workbench parameters. The effect of the oxide thickness as shown in Figure 4.5, the effect of the length of the p-GaN region as shown in Figure 4.6, the effect of mole fraction as shown in Figure 4.7 and the effect of strain relax as shown in Figure 4.8 are analyzed.

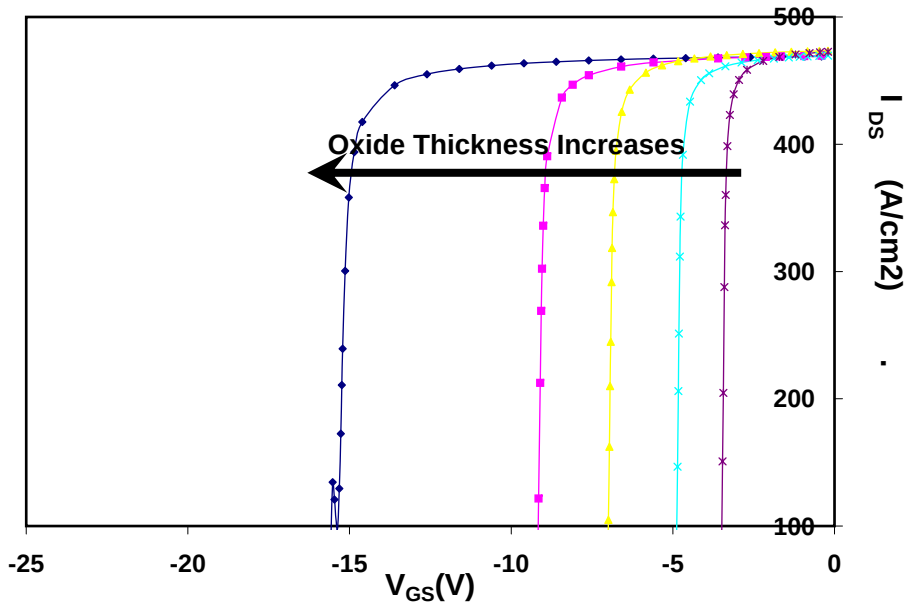

Figure 4.5: The effect of oxide thickness

The threshold voltage depends strongly on the gate oxide thickness (t_{OX}). The formula for the threshold voltage is [26],

$$V_{th} = Q_{MS} - \frac{Q_0}{C_{OX}} + Q_0 - \frac{Q_B}{C_{OX}}, \tag{4.7}$$

As the oxide thickness increases, the value of the threshold voltage decreases as can be seen from the equation. Also another explanation can be as the oxide thickness increases, the channel control becomes difficult and as a result of that pinch-off voltage decreases.

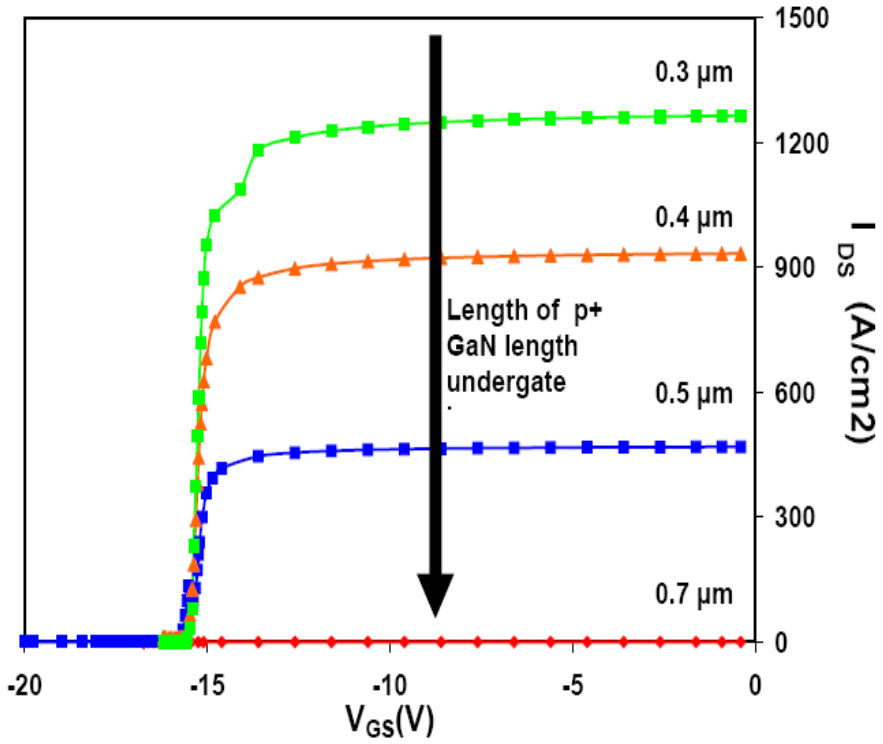

Figure 4.6: The effect of length of p-GaN region

The second device dimension that is observed is the length of p-GaN region. As can be seen from the plot, as the length of the p-GaN region increases, the value of the drain current decreases. However the threshold value does not change. Electrons flow through the channel between the p-GaN regions. As the length of the p-GaN region increases, the channel that electrons flow gets smaller. As the electron current flow through the channel decreases, the drain current value decreases.

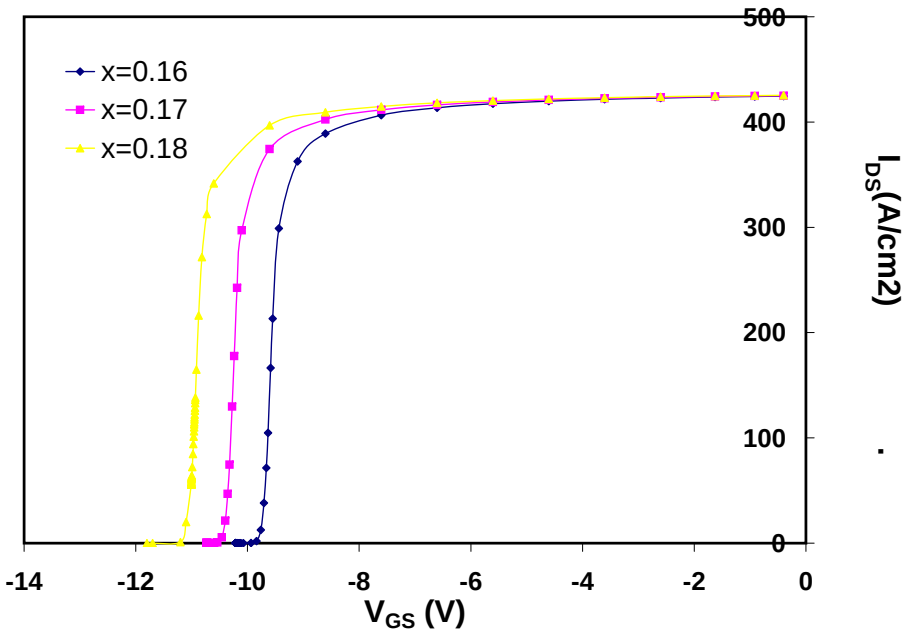

Figure 4.7: The effect of mole fraction

As a sentaurus workbench parameter, the effect of mole fraction is observed first of all. Mole fraction is defined as the amount of Al in the AlGaN layer. It can be defined as the;

$$x = \frac{[Al]}{[Al] + [Ga]}, \tag{4.8}$$

As can seen from the plot, as mole fraction value changes the threshold value changes. However it does not have any effect on maximum drain current value. That can be explained by the carrier density amount in 2-DEG. As the mole fraction value increases, the carrier density in 2-DEG increases and in order to deplete that region, higher voltage should be applied.

The second workbench parameter that is observed is strain relaxation value. Strain relaxation describes how polymers relieve stress under constant strain. Strain relax has an effect on threshold value and it has a slight effect on maximum drain current. If strain relaxation value increases, strain decreases and as the strain decreases, carrier density in 2-DEG decreases. Therefore the channel can be depleted with less reverse bias.

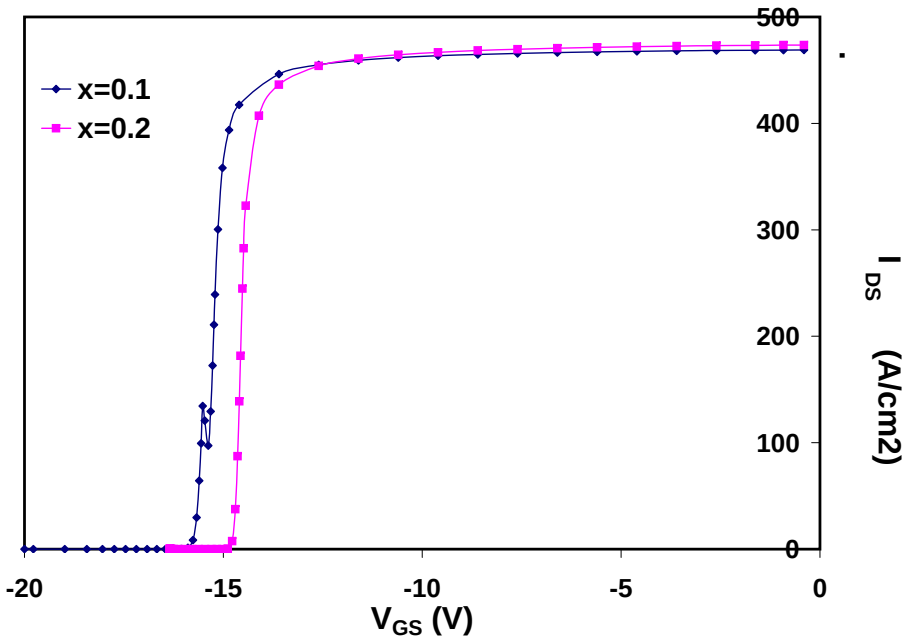

Figure 4.8: The effect of strain relax

Nickel Schottky Barrier is used as a source region material for Vertically Insulated Gate GaN HFET. The I_{DS}-V_{GS} curve of the Nickel Schottky Barrier Source GaN HFET and the GaN source HFET are compared. The comparison is done on two cases, at the first case there is no source-gate overlap for both of the devices and at the second case, there is source-gate overlap for both of the devices. The simulation result of the total current density for Nickel Schottky barrier Source GaN HFET with no source-gate overlap is given in Figure 4.9.a. The structure of the Nickel Schottky Barrier Source HFET and the structure of the GaN Source HFET is shown in Figure 4.9.b and Figure 4.9.c respectively.

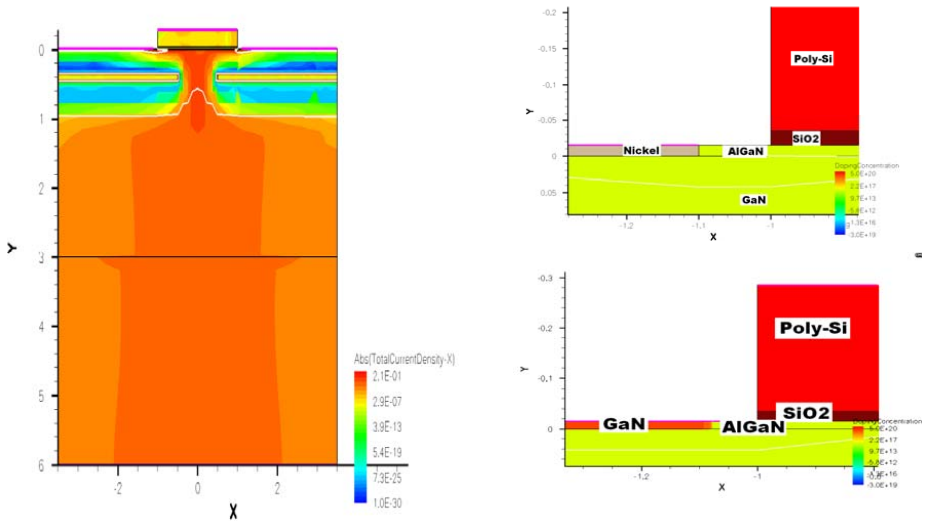

Figure 4.9: (a) The simulation result of Nickel Schottky Barrier Source GaN HFET, (b) Structure of Nickel source HFET (c) Structure of GaN source HFET

The I_{DS}-V_{GS} curve that is obtained from the Vertically Insulated Gate GaN HFET with nickel schottky barrier source, shown in Figure 4.9.b, and GaN source, shown in Figure 4.9.c, are compared. The comparison curve is shown in Figure 4.10. The values of threshold voltage and the values of drain current are same for those devices.

The simulation result of the total current density for nickel Schottky barrier source GaN HFET with source-gate overlap is given in Figure 4.11.a. The structure of the nickel Schottky barrier source HFET with source-gate overlap and the structure of the GaN source HFET with source-gate overlap is shown in Figure 4.11.b and Figure 4.11.c respectively.

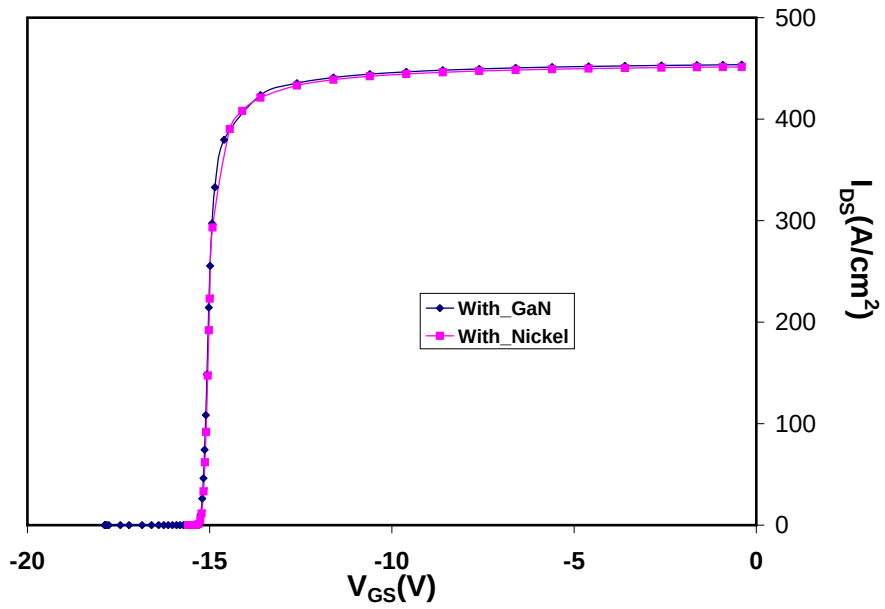

Figure 4.10: Comparison of Nickel Schottky Barrier Source GaN HFET without source gate overlap and GaN Source GaN HFET without source gate overlap

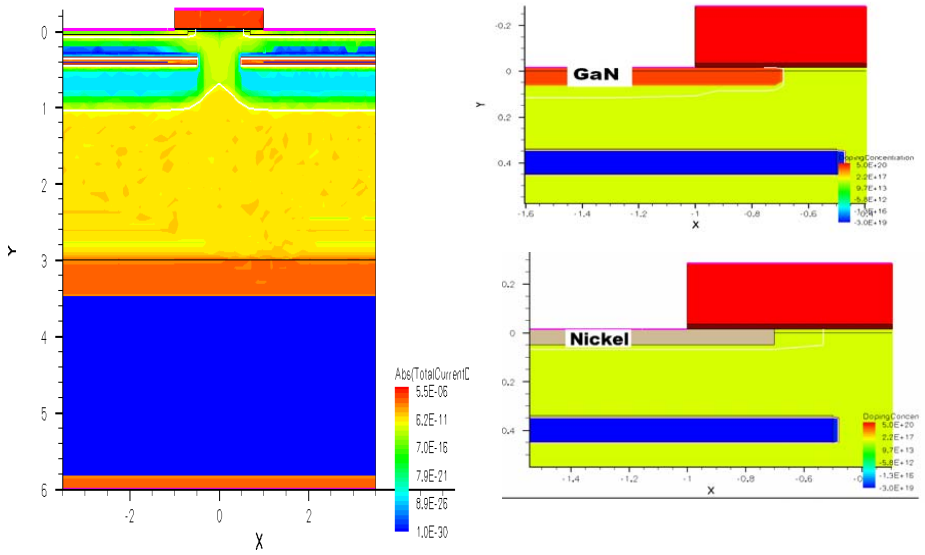

Figure 4.11: (a) The simulation result of Nickel Schottky Barrier Source GaN HFET, (b) Structure of Nickel source HFET (c) Structure of GaN source HFET

The I_{DS}-V_{GS} curve that is obtained from the Vertically Insulated Gate GaN HFET with nickel schottky barrier source, shown in Figure 4.11.b, and GaN source, shown in Figure

4.11.c, are compared. The comparison curve is shown in Figure 4.12. The threshold voltage value is approximately the same for the two cases. However the value of I_{DS} is higher for HFET with GaN source region that HFET with Nickel source region.

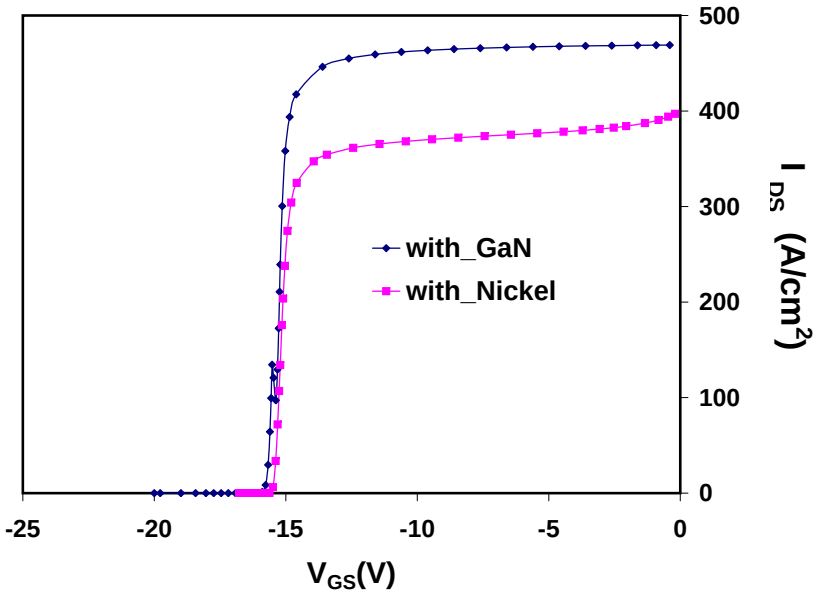

Figure 4.12: Comparison of Nickel Schottky Barrier Source GaN HFET and GaN Source GaN HFET with source gate overlap

Schottky Barrier IGBT on GaN is modeled by using Synopsys TCAD. The device structure that is shown in Figure 4.13 has an n-type GaN substrate. On top of the substrate, there is a 3 μm thick n^- - GaN layer with a doping concentration of $1x10^{16}$ cm^{-3}. The p-GaN layer is 0.1 μm thick with a doping concentration of $3x10^{19}$ cm^{-3} and this layer blocks the current during the off-state. There is a 10-nm thick AlN layer on top of p-GaN layer to suppress the upward diffusion of the atoms in the p-GaN region and also to suppress the mass transport from the surface to the aperture region. SiO_2 layer is used as the gate insulator and there is a 250-nm thick n^+ doped poly-Si layer on top of it. The insulated gate allows higher voltage to be applied to the gate electrode and the gate leakage current to be reduced. Therefore, the device is again vertical and has an insulated gate. However Nickel Schotkky Barrier is used as the source and there is no AlGaN layer. Therefore the device has no 2DEG gas. The comparison of I_{DS}-V_{GS} curve of Schottky Barrier IGBT on GaN, Vertically Insulated Gate GaN HFET with nickel schottky barrier source and Vertically Insulated Gate GaN HFET are shown in Figure 4.14.

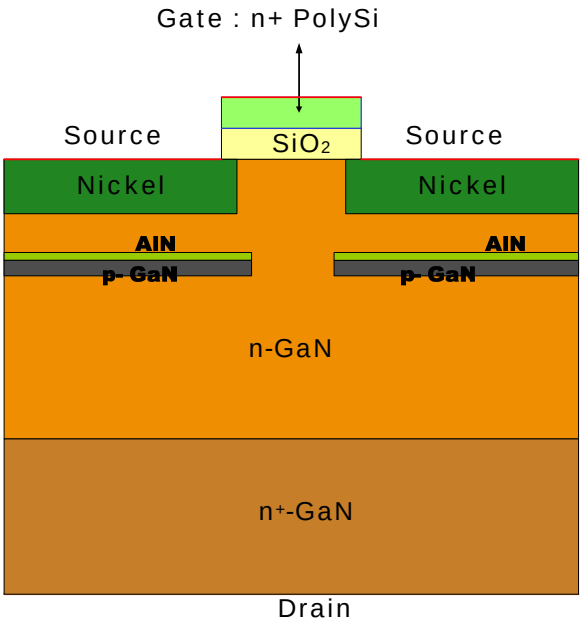

Figure 4.13: Structure of Schottky Barrier IGBT on GaN

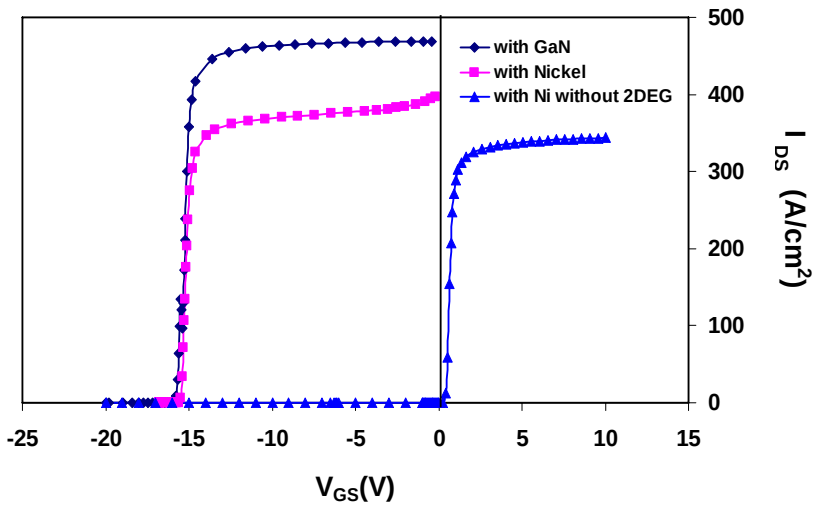

Figure 4.14: Comparison of 3 structures

As can be seen from the Figure 4.15, the Schottky Barrier IGBT on GaN has approximately the same I_D value, if compared with the other two structures. The new device structure is also an enhancement mode device. Because the device has metal on source regions, the fabrication process is much easier and it can be used for high power applications.

Chapter 5

Conclusion and Future Works

We have successfully demonstrated a novel method to model the Nickel Schottky Barrier Source/ Drain GaN MOSFET by using Synopsys TCAD. The modeled device shows similar I-V characteristics with the experimental data. The source/drain spacing is also examined by changing the source/drain spacing with respect to gate. It is concluded that as source/drain overlaps with the gate, there is an increase in drain current.

Vertically Insulated Gate AlGaN/GaN HFET is modeled successfully by using Synopsys TCAD. The simulated device shows similar I-V characteristics with the experimental device data. Also the effects of the oxide thickness, strain relax, mole fraction and the length of the p region are examined. Length of p-GaN region has an effect on I_D value. As the length of the p-GaN region increases, the I_D value decreases. Mole fraction, strain relaxation and oxide thickness have an effect on the value of threshold voltage. As the value of mole fraction and oxide thickness increases, the value of threshold voltage decreases. However as the value of strain relaxation increases, the value of threshold voltage increases. Nickel Schottky Barrier is used as the source for the same device and Schottky Barrier GaN HFET device and GaN source HFET device are compared according to the source to gate spacing.

As a future power device, Schottky Barrier IGBT on GaN is demonstrated. The enhancement mode device has approximately the same drain current value without the 2DEG gas formed at AlGaN and GaN interface,if compared with the AlGaN/GaN HFET structure.

Future work must focus on the enhancement mode Schottky Barrier GaN MOSFET and also different metals should be tried instead of Nickel, such as Platinum or Tita-

nium. Also, the thickness of the gate oxide should be decreased to obtain higher I_D value. Furthermore, Schottky Barrier IGBT on GaN structure should be studied more. Different gate oxide materials and different gate metals should be tried to obtain higher I_D value.

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Appendices

Appendix A

Visualization Tools

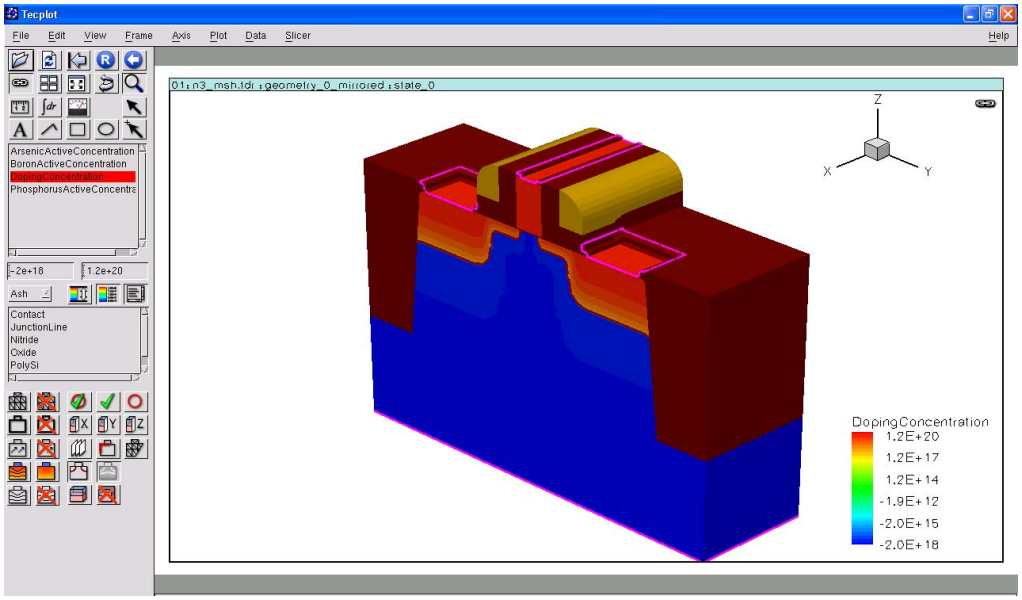

Figure A.1: Graphical user interface of Techplot

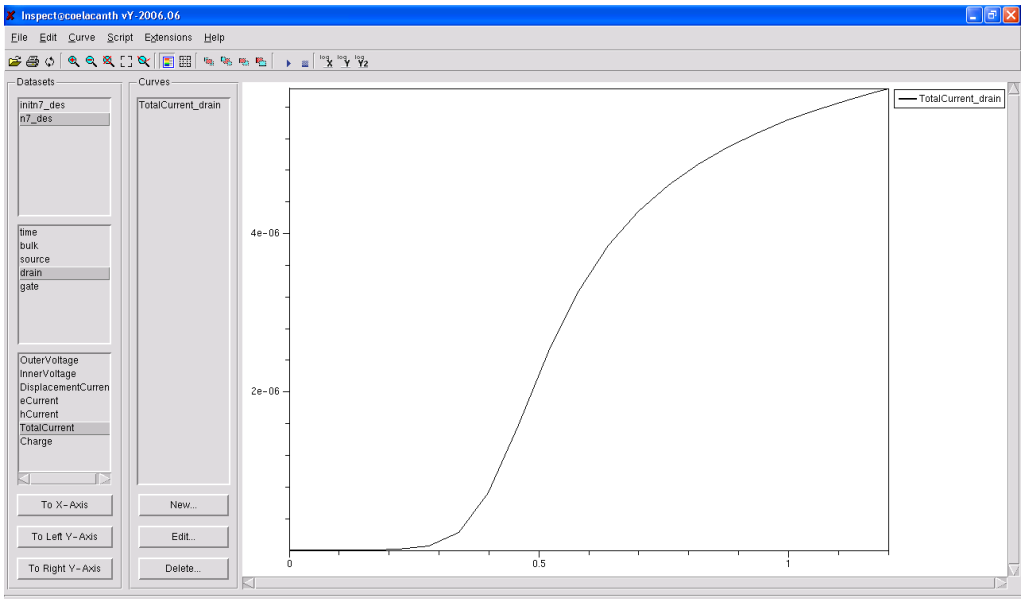

Figure A.2: Graphical user interface of Inspect