ABSTRACT

GUPTA, ABHEEK. Inductor Geometries and Inductance Calculations for Power Transfer in Biomedical Implants. (Under the direction of Dr. Gianluca Lazzi.)

Biomedical implants used as neural prostheses are often powered by low frequency wireless inductive systems. Such an inductive coil system consists of the primary coil outside the body and the secondary coil implanted on-chip with the prosthesis. This thesis proposes novel designs for the geometry of the on-chip coil and computes the inductive coupling obtained by using the proposed geometries. Traditional inductance calculation methods involve the use of computationally expensive field solvers or complicated analytical methods. A computational method employing the partial inductance concept is used to calculate the self and mutual inductances at low frequencies of certain regular 2-D and 3-D geometries (spirals, rectangular helices, pyramidal inductors etc.). These inductor geometries are fabricated and the measurement results match closely with the values predicted by the simulations. This provides an analytically simple, cost-efficient and computationally fast method of finding the self and mutual inductances of regular 2-D and 3-D geometries which can be used to reliably compute the coupling of the proposed on-chip inductor geometries. The inductor geometry for optimal power transfer can be chosen on the basis of these inductance calculations.

Inductor Geometries and Inductance Calculations for Power Transfer in Biomedical Implants

by

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Biography

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His research is in the areas of on-chip 3-D inductors for implantable biomedical chips, inductance calculations, inductor geometries and fabrication, and wireless inductive power coupling applicable to biomedical prosthesis development. The project which he represents is a joint research effort between ophthalmologists and surgeons at the University of Southern California and electrical engineers at North Carolina State University. The goal is the development of a chronic retinal prosthesis implant to recover limited vision to people who are blind due to outer retinal degeneration caused primarily by the diseases Retinitis Pigmentosa and Age-Related Macular degeneration.

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The proposals of inductor geometries contained in this thesis have primarily been the contributions of Dr. Mehmet Ozturk. Their inclusion in my thesis is the result of my research group's collaboration with him. Further, the preliminary investigations into the cleanroom fabrication process for the on-chip inductors have been conducted under his direct guidance. For sharing his innovative research ideas and providing me with the knowledge and resources for the fabrication, I thank Dr. Ozturk profusely.

I thank Dr. Bilbro and Dr. Barlage for serving on my thesis advisory committee and providing me with invaluable advice.

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Contents

List of Figures **vi**

List of Tables **viii**

1 Introduction **1**
1.1 Inductance Coupling and Geometries . . . 3
1.1.1 Importance of Coil Geometry . . . 4
1.1.2 Prior Research on Coil Coupling and Geometries . . . 4
1.2 Inductance Extraction Methodology . . . 6
1.3 Inductance Calculation . . . 7
1.4 Inductance Fabrication and Measurement . . . 8
1.5 Organization of Thesis . . . 9

2 Inductor Geometries for Power Transfer **10**
2.1 Proposed Inductor Geometries . . . 11
2.2 Investigation into Proposed Cleanroom Fabrication . . . 14

3 The Partial Inductance Method **25**
3.1 Inductive Interaction between Conductors . . . 26
3.1.1 Ampere's Law . . . 26
3.1.2 Faraday's Law . . . 28
3.1.3 Electric Potential . . . 28
3.1.4 Loop Inductance . . . 29
3.2 The Partial Inductance Concept . . . 30
3.3 Useful Partial Inductance Formulae . . . 33
3.4 The Computational Method . . . 37
3.4.1 Algorithm for Self-Inductance Calculation . . . 37
3.4.2 Algorithm for Mutual-Inductance Calculation . . . 39
3.5 Justification for Non-Filamentisation of Segments . . . 40
3.5.1 Mutual Inductance Case . . . 42
3.5.2 Self Inductance Case . . . 45

4 Inductor Fabrication and Measurements **49**
4.1 Inductor Fabrication 50
4.2 Inductor Measurement 51

5 Analysis of Inductor Geometries and Results **55**
5.1 Test Structures and Results 55
5.1.1 Self Inductance 55
5.1.2 Mutual Inductance 62
5.2 Error Analysis 67
5.3 Optimal Geometry Analysis 69
5.3.1 Varying the value of N 71
5.3.2 Varying the value of Track Separation 76

6 Conclusion **80**
6.1 Contributions 80
6.2 Future Work 81

Bibliography **83**

List of Figures

2.1 Basic Geometry for Backside On-chip Pyramidal Inductor 12
2.2 Geometry for Recessed Backside Pyramidal Inductor 12
2.3 Cross Sectional Geometry for Backside Trench Pyramidal Inductor 13
2.4 Process Flow Diagram(contd.) 20
2.5 Process Flow Diagram (contd.) 21
2.6 Process Flow Diagram (contd.) 22
2.7 Process Flow Diagram (contd.) 23
2.8 Process Flow Diagram 24

3.1 Magnetic Field created by time-variant current flowing through conductor loop 27
3.2 Electric Voltage created by time-variant magnetic field passing through a conductor loop 29
3.3 Magnetic Field created by the time-variant current in loop j induces voltage in loop i, since some of the magnetic field passes through i 29
3.4 Partitioning of Loops into Segments 31
3.5 Partitioning of Segments into Filaments 32
3.6 Two Equal Parallel Filaments 35
3.7 Unequal Parallel Offset Filaments 35
3.8 Unequal Parallel Overlapping Filaments 35
3.9 Unequal Parallel Filaments with complete Overlap 36
3.10 Unequal Parallel Filaments with Ends on same side of Common Perpendicular 36
3.11 Unequal Parallel Filaments with Ends on opposite sides of Common Perpendicular 36
3.12 Special Case of Unequal Coaxial Filaments 37
3.13 Partitioning of Segments into Filaments 41

5.1 Square Loop 56
5.2 Predicted and Measured Results Plot for Square Loop 56
5.3 Square Loop with Leads 58
5.4 Predicted and Measured Results Plot for Square Loop with Leads 58
5.5 Spiral Inductor 59
5.6 Predicted and Measured Results Plot for Spiral Inductor 59

5.7 Rectangular Helical Inductor 60
5.8 Predicted and Measured Results Plot for Rectangular Helical Inductor . . . 60
5.9 Side View of Pyramidal Inductor 61
5.10 Top View of Pyramidal Inductor 61
5.11 Predicted and Measured Results Plot for Pyramidal Inductor 62
5.12 Mutual Inductance between Coaxial Square Loops 63
5.13 Predicted and Numerical Simulation Results Plot for 2 Square Loops 63
5.14 Mutual Inductance between Spiral Inductors 64
5.15 Predicted and Measured Results Plot for 2 Spiral Inductors, D=1.8 cm . . . 64
5.16 Predicted and Measured Results Plot for 2 Spiral Inductors, D=2.5 cm . . . 65
5.17 Predicted and Measured Results Plot for 2 Spiral Inductors, D=3.0cm . . . 66
5.18 Mutual Inductance between Pyramidal Inductor and Square Loop 66
5.19 Predicted and Measured Results Plot for Pyramidal Inductor and Square Loop 67
5.20 Error Percentages for Predicted Self Inductance Values 68
5.21 Error Percentages for Predicted Mutual Inductance Values 69
5.22 Basic Pyramidal Inductor Geometry 70
5.23 Recessed Pyramidal Inductor Geometry 70
5.24 Double Recessed Pyramidal Inductor Geometry 71
5.25 Mutual Inductance between Pyramidal Inductor and Square Loop 71
5.26 Normalized Coupling Coefficient variation with N for $2-N-2$ Pyramid . 72
5.27 Normalized Coupling Coefficient variation with N for On-Chip $3-N-3$ Pyramid 73
5.28 Normalized Coupling Coefficient variation with N for On-Chip $2-N-2-N-2$ Pyramid 74
5.29 Normalized Coupling Coefficient variation with N for On-Chip $2-N-2$ Pyramid 75
5.30 Normalized Coupling Coefficient variation with Track Separation for On-Chip Basic Pyramid 77
5.31 Normalized Coupling Coefficient variation with Track Separation for On-Chip $2-2-2$ Pyramid 78
5.32 Normalized Coupling Coefficient variation with Track Separation for On-Chip $2-2-2-2-2$ Pyramid 79

List of Tables

3.1 Inductance values with & without Filamentisation(Test Dimensions) 43
3.2 Inductance values with & without Filamentisation(On-Chip Dimensions) . . 44
3.3 Inductance values with & without Filamentisation(Test Dimensions) 46
3.4 Inductance values with & without Filamentisation(On-Chip Dimensions) . . 48

Chapter 1

Introduction

Biomedical implants used as neural prostheses typically do not reside fully inside the body, but rather consist of an implantable stimulation unit linked to an external unit. This is motivated by the desire to have a simpler implant with ease of upgrading signal processing and other aspects of the exterior unit without incurring re-entrant surgery. Although percutaneous (wired) connections between external and internal units have been used in earlier developments, the transcutaneous (wireless) link is the method of choice due to reduced mechanical tethering on the implant and lower risk of infection. A successful biomedical implant needs a sophisticated electronic system to provide the necessary power and data transmission between the external and internal implant units. The primary concerns for the development of these microelectronics are efficiency, small size, low power dissipation and minimal heat generation. Biomedical implants used as prostheses are often powered by low frequency wireless inductive systems.
The use of transcutaneous, or wireless, connections is justified due to the following complications which are typical for alternative schemes [1]:

- Risk of infection: Percutaneous connectors (physically wired links between implanted and exterior prosthesis components) raise the risk of infections due to a perpetual breach of the body, through which wires must pass.

- Adverse reaction to excessive movement: Depending on mechanical anchoring, such as to bone, percutaneous connectors may restrict movement of a prosthesis in the tissues

in which it is implanted and with which it interfaces electrically. These tissues may be free to move with respect to a percutaneous connector with obvious complications.

- Breakage of leads or device dislodging: For example, in the case of ocular prostheses, rapid eye movement can break any penetrating wires passing through the scleral wall, which might otherwise be used to connect an intraocular prosthesis to external electronics. Furthermore, dislodging of the implant due to external tethering on the wires could occur.

- Battery replacement: In the case of most prostheses, implantable batteries are undesirable because of the associated replacement surgery (except where charging can be initiated from outside of the body, as from coils, for example). Even renewable cells have limited recharge cycles. Furthermore, as a consequence of the biological environment, implanted batteries must be enclosed in the implant encapsulant, which would complicate replacement.

Magnetically coupled coils have been the traditional means of wireless connection to implanted devices [2]. Although there are many ways to transmit data to the implant, it has been the primary way to transfer a significant amount of power to the implant. Because the magnetic field strength over the coil axis falls as a third power of distance, this type of link is suitable only for very small distances. The primary coil radiates energy widely in many directions. This is primarily the case when the magnetic field may not be directed due to the absence of magnetic material. The use of magnetic material should be avoided as it may lead to adverse effects if the individual with the implant were to come under the influence of an unwanted magnetic field. Due to discontinuity at the body surface and the absence of magnetic material for reasons explained above, the coils are air-coupled. Depending on the space between coils, air-coupling may result in very poor coupling coefficient between the coils. Several studies have been conducted to measure the mutual inductance between two air-coupled coils [3] [4] [5]. Coupling strength is dependent on coil loading, excitation frequency, coil separation, coil geometry, coaxial alignment and angular alignment. Most of these are subject to variation in prostheses. Typical values for coil-coupling coefficients are between 0.01 and 0.1. To receive the required power at low coupling, high field strengths are used. Because the low frequency at which the coils operate does not have much absorption in the tissue, this can generally be used safely. However, for high power implantable

devices, electromagnetic absorption in the human body must be determined to ensure that international safety standards are met.

1.1 Inductance Coupling and Geometries

Inductive telemetry has been the standard means of wireless connection to implanted devices for years. It is based on the mutual magnetic coupling of two proximal inductive coils. The secondary coil in this arrangement is implanted along with the stimulator/neuro-recorder which it services, while the primary coil remains exterior. A low frequency carrier (i.e. usually 1-10 MHz) is driven onto the primary coil which can then be coupled onto the secondary coil for transfer of power. Transcutaneous power transfer for medical applications via inductively coupled coils was first demonstrated by Schuder [6]. Since then, several papers have reported various advancements on the theme of inductive wireless power transfer. However, the basic concept behind the transfer theme remains the same. For power transfer, the two implant units are connected by a wireless inductive link, allowing the internal implant unit to derive power from the external implant unit. The primary inductor coil which is located on the external implant unit is driven by an external transmitter circuit and transmits power. The secondary coil is located on the internal implant along with a receiver circuit to receive power for the internal device electronics.

Two major disadvantages are noted here regarding magnetic coupling, which are simply a characteristic of the coils.

- Direction of Radiation: It is obviously desirable to radiate energy only towards the secondary coil. In reality, the primary coil radiates energy widely in many directions, particularly with no ferrous core to concentrate the magnetic flux, as in a transformer. This omni-directional radiation pattern imposes an unnecessary drain on the system batteries.

- Poor Coupling: Due to the implantation, the coils must be disjoint and subsequently cannot be coupled, or linked, by a common ferrous material, but are rather air-cored. Therefore, the mutual-inductance, or coupling-coefficient, is quite low. This requires high magnetic field strength in the primary coil in order to induce sufficient energy in the secondary coil to power the implant. The coupling coefficient of the coils may be enhanced by careful design of their geometries and relative orientation.

1.1.1 Importance of Coil Geometry

From magnetic flux considerations, it is known that the inductive coupling between the two coils is determined by their geometries and relative orientation for a given separation. The constraints on the dimensions of the coils are based on the environments in which they are placed. Though the primary coil does not have very small area requirements since it is outside the body, the secondary coil has to be miniaturized to satisfy the stringent space constraints within the body. The secondary coil is often located on-chip to increase integration density of the system which further reduces the space available to construct the inductor. The geometry of the secondary on-chip inductor is thus seen to be of significant importance since it needs to maximize coupling with the external inductor while being integrated on-chip and complying with the space constraints.

1.1.2 Prior Research on Coil Coupling and Geometries

The optimization of the coil coupling depends on various factors. Research has been conducted on various geometries in 2-D and 3-D coils as well as other geometric coupling enhancement techniques.

Zierhofer et al. demonstrated that the coupling coefficient between coils can be considerably enhanced if the turns of the coils are not concentrated at the circumferences, but distributed across the diameters [5]. However, such a distribution of turns results in a reduction of the unloaded quality factors of the coils. The same authors showed that an optimum number of turns can be achieved for maximum net efficiency improvement [7].

Due to anatomical requirements of the implant, the coils may be frequently misaligned, therefore reducing coupling efficiency. The possibility of coil misalignment is considered by Flack et al. [8] who also provide calculations and graphs for the lateral misalignment case between two coils whose planes are parallel, for a variety of spacings between the planes and displacements between the axes of the coils. Soma et al. derive inductance formulae for the lateral and angular misalignment of coils as well as for a combination of the two kinds of misalignments [9].

From a fabrication point of view, various 2-D and 3-D inductors have been fabricated on-chip. Neagu et al. optimize the design of the receiver coil by focusing on different configurations of planar receiver coils made with the use of micromachining technologies

such as thin-film deposition and electroplating [10]. Mokwa et al. improved the power transfer of coils by developing a new fabrication process for the realization of multiple layer coils by using a folding technique to manufacture single, double and 4-layer coils [11].

Tang et al. proposed and fabricated a miniature stacked 3-D inductor using standard digital one-poly four-metal technology which led to a significant reduction in area compared to conventional spiral inductors [12].

An on-chip 3-D inductor is fabricated by Young et al. [13] by electroplating copper traces around an alumina insulating core, deposition of conformal photoresist by electroplating, and using a 3-D maskless direct-write laser lithography tool to expose the resist. Chomnawang et al. designed, fabricated and characterized 3-D on-chip air core solenoid inductors and 3-D on-chip suspended dome shaped spiral inductors using deformed sacrificial polymer core and conformal photoresist electroplating techniques [14].

Yoon et al. fabricated arbitrary 3-D metal microstructures including suspended spiral inductors, solenoid inductors and transformers using a new, thick-metal surface micromachining technology [15].

A new 3-D assembly process called plastic deformation magnetic assembly was developed by Zou et al. to fabricate vertical spiral inductors and solenoid inductors by first fabricating the inductors on the substrate and then assembling them into the vertical position using magnetic fields and plastic deformation materials [16].

Since planar inductors involve substantial substrate losses and parasitics [17] [18], thereby reducing coupling efficiency, we choose to focus on 3-D on-chip inductors to obtain better coupling with the external coil. Although a good deal of research has been published in the areas of coil coupling as well as design and fabrication of 3-D inductors, this work differs significantly from prior work in this field. In this research, we formulate a computational method which can directly calculate the mutual coupling between the external coil and various geometries and structures for the internal coil. We propose some novel and unique inductor geometries which may possibly provide good coupling. These geometries are analyzed by our computational method once the method has been tested and validated for simpler structures. The proposed 3-D geometries may be fabricated concurrently using standard IC processes to establish the fabrication procedure to be used in their construction. Having obtained the information from the computational method regarding the on-chip inductor geometry with optimal coupling characteristics, we may proceed to fabricate the chosen geometry on-chip and integrate it with the biomedical implant.

1.2 Inductance Extraction Methodology

The problem statement for this research has been described in the previous couple of sections. In short, it is desired to find out which inductor geometries give us the highest coupling coefficient values to enable efficient power coupling. There are various methods by which this question may be answered. One possible route is to actually fabricate the structures in question, measure the inductance values and compare the values to select the best possible geometry. However, given the small size of the inductor structures and the technology required to fabricate such devices, the prohibitive cost of this approach makes it impractical. We would need to compare many possible structures which differ from each other by small deviations in a few parameters. It would be economically unfeasible to fabricate the required number of approximately similar structures to isolate the optimal inductor structure. Another possible method would be to use an analytical approach to solve the problem. The difficulty with this approach is that precise analytical formulae do not exist for the pyramidal inductor structures being proposed, and thus we cannot directly analyze these structures using simple formulae.

However, it is possible to find a close approximation to the inductance values for these structures by meshing the original structure into smaller segments and using quasi-analytical methods. Such an approach would be tedious and labor-intensive in terms of attempting to calculate the overall inductance by hand. The nature of the problem seems to suggest that a computational approach may be tenable. The required meshing and computations could be carried out by a computer code written specifically for the purpose. The code should ideally be able to tackle any inductor structure of a certain geometry type. Different codes could be written in order to handle inductors with different geometries. Thus, given the dimensions, geometry and configuration of the inductors, the computer simulations would generate the inductance value for the configuration. This approach is a time and cost-efficient way of tackling the problem. It also allows us the flexibility of making dimensional and geometric changes and observing, via simulations, how these changes affect the inductance value of the structures.

The approach followed in researching this problem is to write computer codes in the C programming language which incorporate the inductance extraction method for analyzing a variety of inductor geometries. A code for a certain geometry essentially divides the original structure into a number of segments which comprise the inductor and analyzes

their interactions to find the total value of inductance. The results from the computer simulations are then used to determine which inductor structure is most suited for our purpose.

1.3 Inductance Calculation

Traditional inductance calculation methods [19] involve the use of electromagnetic field solvers or complicated analytical methods. They may also require the use of approximate lumped or distributed models and experimentally fitted parameters. However, these methods are both tedious and computationally expensive and may not easily analyze the self and mutual inductance of certain inductor geometries of interest.

Although accurate, electromagnetic simulators are slow and computationally intensive, both in memory and time. Thus, while these field solvers are suitable for accurately simulating simple structures, they are not suitable for simulating large three dimensional structures with multiple segments. On-chip inductors require long simulation times, access to fast processors and availability of substantial memory, factors that are aggravated by commonly encountered situations where the spacing between conductors is small compared to their width. Furthermore, since these simulators require both the lateral and vertical geometries to be specified, considerable experience is required on the part of the user to simulate on-chip inductors. These field solvers also do not provide any insight into the engineering trade-offs involved in the design of on-chip inductors and transformers. Although the better field solvers are excellent for verification, they are inconvenient at the initial design and optimization stages. For the reasons noted above, full fledged field solvers are not a practical option for on-chip inductance calculations.

Some analytical methods like the Greenhouse method [20] are often used in conjunction with lumped models for calculation of the inductance value. This method is based on a segmented summation approach which increases in complexity as the square of the number of segments in the inductor and thus lacks a simple expression. Although the Greenhouse method offers sufficient accuracy and adequate speed, it cannot provide an inductor design directly from specifications. Thus the absence of a simple accurate expression for the inductance diminishes the versatility of the lumped model and makes it inconvenient for circuit design and optimization. Further, lumped models may not model some effects

that affect the value of the inductance.

In this work, a low frequency method is investigated which uses the Partial Inductance formulation [21] to compute the self and mutual inductance values for a variety of 2-D and 3-D geometries. The Partial Inductance formulation allows the evaluation of inductances for a variety of arbitrary microcircuit geometries. In general, the inductance of open loops is not a defined quantity since we typically require the flux linkage with the area enclosed by a loop to calculate inductance and the area enclosed by an open loop is not a meaningful concept [22]. The main contribution of this formulation is the establishment of a relationship between incomplete loops and closed loops, thus allowing the definition and computation of the inductance of incomplete loops. Further, it provides simplifications which allow complicated geometries to be treated with ease under certain conditions. Since accuracy, time and cost are the main factors that we are trying to optimize, we need to make sure that neither complicated analytical methods, nor time or cost-intensive computational methods are involved, and that the method developed gives predicted inductance values within reasonable bounds of error for the required applications. For low frequencies and for regular geometries, the Partial Inductance formulation allows the self and mutual inductance of the inductor to be calculated with relative ease. A computationally efficient and inexpensive method is developed for calculating the self and mutual inductances at low frequencies of certain regular 2-D and 3-D geometries (spirals, rectangular helices, pyramidal inductors etc.), using the Partial Inductance method.

1.4 Inductance Fabrication and Measurement

In carrying out this computational analysis, it is extremely important to validate the values determined by the simulations. The computer analysis should be able to predict the inductance of the given structures with a relatively high degree of accuracy and it is important to know how the simulation values compare with the actual inductance values. Possible sources of validation are measured inductance values of fabricated inductors and results obtained for simple geometries using existing numerical simulation methods.
In order to provide independent verification sources for the inductance values predicted by the computational analysis, several test structures were fabricated and then measured. These structures were also simulated and the results predicted by the computational method

were compared with the measurement results. If the computational results are in good agreement with the measurement results, the validity of the computational method is established and it may be used to confidently predict the inductance values of various structures with reasonable accuracy and speed.

1.5 Organization of Thesis

The remainder of this thesis is organized in the following manner. Chapter 2 contains a description of the inductor geometries which have been proposed for optimal power transfer. The explanation of the partial inductance method and the development of the algorithm for the computational method are presented in Chapter 3. Inductor fabrication details and the measurement process is described in Chapter 4. Chapter 5 contains the analysis of the results for the various test structures. Finally, Chapter 6 presents the conclusions of the work.

Chapter 2

Inductor Geometries for Power Transfer

In order to achieve optimal power transfer, we need to integrate inductors on chip which maximize electromagnetic coupling with the external inductor. From magnetic flux considerations, it is known that the inductive coupling between two coils is determined by their geometries and relative orientation. The geometry of the secondary on-chip inductor is thus seen to be of significant importance since it needs to maximize coupling with the external inductor while being integrated on-chip and complying with the space constraints. The purpose of this work is to examine a few novel inductor geometries which may be fabricated on-chip and then compare the various options based on calculations of mutual coupling with the external coil.

Traditionally, spiral inductors have been the preferred geometry for on-chip inductors primarily due to the difficulties associated with the fabrication of 3-D inductors. For example, previously fabricated 3-D inductors typically involve sacrificial cores [14], electroplating of metal traces, electrodeposition of photoresist and maskless direct-write laser lithography [13] - all of which are expensive and process-intensive methods. Whereas this expense and effort to integrate inductors along with the chip electronics may be justified for the fabrication of integrated high-Q inductors to be used as inductive circuit elements, we recognize

that the on-chip inductor we intend to fabricate is part of a transformer unit to enable wireless power transfer. This means that the space and geometry constraints involved in the fabrication of this inductor are different from the typical case - specifically, our on-chip inductor need not be located on the same side of the wafer as the chip electronics.
By allowing the inductor to be located on the opposite side of the wafer, we buy increased flexibility with regard to the inductor dimensions, geometry and process techniques. Since a 3-D coil geometry takes up less comparable surface area and does not involve as much substrate losses and inter-metal capacitive coupling as a planar arrangement, we shall investigate a pyramidal geometry using the backside of the chip as the inductor base area. Also, we shall try to use as much of the backside chip surface area to form the base of the 3-D inductor because large inductors lead to better coupling.

2.1 Proposed Inductor Geometries

The inductor geometries proposed in this section are a result of a collaborative work with Dr. Mehmet Ozturk, ECE Dept., NCSU, Raleigh. Dr. Ozturk's innovative ideas on inductor geometries for maximal power coupling which would be compatible with current IC fabrication processes comprise the core of this section of the thesis. The research carried out in this area investigating different geometries and formulating the fabrication process was done under his guidance.

- **Pyramidal Geometry**

  A 3-D pyramidal geometry like the one shown in Fig. 2.1 is the basic design for the backside on-chip inductor. This geometry provides us with the possibility of several turns in the inductor, therefore increasing the magnetic flux generated by the coil while still not taking up as much base surface area as a spiral inductor with a comparable number of turns. In this configuration, the inductor metal lines are patterned on the sides of a pyramid of dielectric material such as silicon oxide. The dielectric pyramid may be formed via deposition or oxidation on the silicon wafer followed by selective etching. The reverse side of the silicon wafer contains the chip electronics which function as the control circuitry for the data and power transfer mechanism. The flat portion on the top of the dielectric pyramid may accommodate some other

component used by the implant - in this case, an antenna for transcutaneous wireless data transfer.

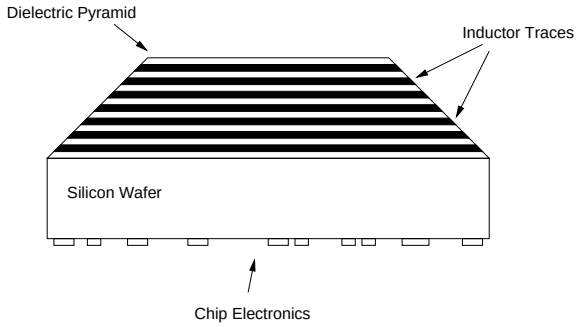


Figure 2.1: Basic Geometry for Backside On-chip Pyramidal Inductor

- **Recessed Pyramidal Geometry**

  A variant of the basic pyramidal geometry is a recessed pyramid as shown in Fig. 2.2. This geometry can be further modified by providing a number of recesses along the height of the pyramid.

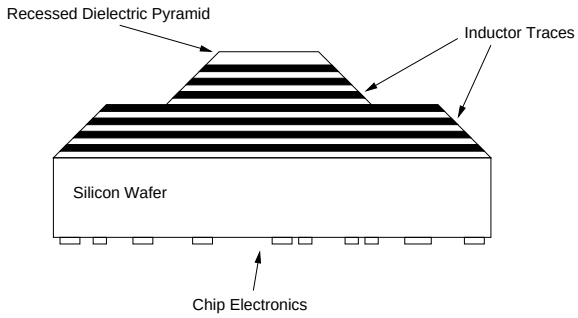


Figure 2.2: Geometry for Recessed Backside Pyramidal Inductor

However, both the above inductor geometries are beset with fabrication and process issues. Process runs to fabricate these inductors involve the electrodeposition of photoresist for conformal coverage of the 3-D pyramidal surface in order to pattern the metal lines. Electrodepositable photoresist technology is labor intensive, tedious and error-prone. Since EDPs are still in the research and development stage in the industry, several anaphoretic/cataphoretic photoresists have to be tried out to obtain

a satisfactory exposure of the metal lines. EDPs also have a short shelf life which is highly unsuitable for research purposes. Another issue which arises with the exposure is that offset photolithographic masks may be required to achieve satisfactory exposure of the slanted pyramid sides due to diffraction effects.

- **Trench Pyramidal Inductor**

  In view of the process issues described above, another pyramidal design, the backside trench inductor is proposed (Fig. 3) which can be fabricated using standard photoresists and photolithography techniques. Since a pyramidal trench needs to be conformally covered with photoresist in this case, a traditional spin-on photoresist is considered viable. During the spin-on process, the photoresist will be spread outward from the bottom of the trench, thus providing conformal coverage of the entire surface. This allows us to use standard photoresists and photoresist spin-on processes coupled with photolithographic exposure with a standard mask-set. Etching a deep trench in the silicon wafer is the time consuming step in this process. The standard silicon etch comprising Hydrofluoric Acid, Nitric Acid and Acetic Acid is an isotropic etch which is unsuitable for our purpose since we need sharply defined trench pyramid slopes. Therefore, an anisotropic etch comprising alkaline KOH and water may be used to etch the silicon wafer in the required trench shape. This process takes a few hours and needs to be carefully monitored.

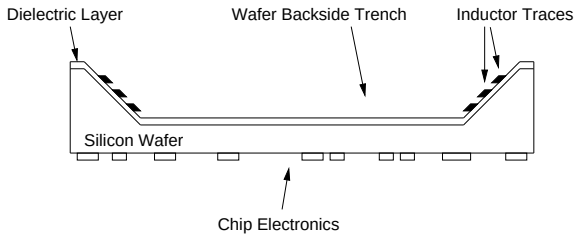


Figure 2.3: Cross Sectional Geometry for Backside Trench Pyramidal Inductor

The inductor geometries described above will be investigated for optimal power transfer from the external inductor to the implant. We use the partial inductance concept to develop a computational method which can analyze the self and mutual inductances of these structures so as to reliably predict the inductive coupling achieved by each geometry. These results will help us choose a specific inductor geometry for our

biomedical implant. The next section explains the issues involved in fabricating the inductors described above.

2.2 Investigation into Proposed Cleanroom Fabrication

The inductors that will be fabricated as described in Section 4.2 are scaled up versions of the intended on-chip inductors. Since the partial inductance method is a scalable method of computing inductances, a close match of predicted and measured results at these dimensions validates the method for the actual inductor dimensions of interest as well. The scalability of this method is borne out by the fact that the partial inductance method is used at very small dimensions, eg. for calculating the inductance matrix of on-chip and off-chip interconnects [23]. However, in order to verify and validate the method without doubt for the inductor geometries of interest, we propose to fabricate some on-chip inductor geometries using standard IC processing methods and then measure the inductance values obtained. A good match for these inductors would validate the method for on-chip inductor dimensions. The issues involved in fabricating the on-chip inductors and the factors motivating the choice of the trench pyramidal inductor as the favored geometry for fabrication are explained below.

- **Conformal Photoresist Deposition:** The inductor metal traces in the first two inductor geometries mentioned above - the pyramidal geometry and the recessed pyramidal geometry - are patterned on sloping surfaces, specifically, surfaces sloping downward. This means that we need to have conformal coverage of the dielectric surface by the sputtered metal as well as conformal coverage of the photoresist. Conformal coverage of metal by sputtering or evaporation may be obtained since the metal vapor or atoms may be expected to cover all surfaces in a relatively conformal manner. However, conformal coverage of the surface by the photoresist is a very major problem. A useful comparison of techniques for conformal coverage of sloped surfaces is supplied by Pham in [24], which surveys spin, spray and ED resists. For spin coating, positive photoresist Hoechst AZ4562 is used; the spray coating is done using the EVG 101 system dispensing photoresist AZ4652 diluted with a solvent for good coverage and a uniform layer; the electrodeposition is carried out using Eagle 2400ED positive resist and Eagle 2100ED negative resist. Conventional spin coating of the photoresist will not allow for fabrication of such continuous lines over that topography due to

severe resist trends to accumulate [25]. The main obstacle is caused by the centrifugal force when spinning. The deeply etched features cause a physical obstruction to the solution flow, preventing coverage and often causing striation or resist thickness variation such as the variation on the near and far sides of a cavity. With positive photoresists this will prohibit opening of the exposed area. This will result in shorted and/or interrupted lines. Modified spin coating techniques have been proposed [26], but these can only be used for certain specific MEMS applications with modifications of the equipment, the spinning method or the coating program. Another new coating technique called direct spray coating of photoresist [27] has been introduced as a new method for MEMS applications. However, this technique, apart from being in the early stages of exploration, is best suited for wafers with moderate topography. There exists a flow of the resist due to its gravity, resulting in a thicker resist layer at the bottom corner and a thinner one at the top corner of the same cavity. Wafers with extreme topography can be produced best by using a coating process with high shape conformality. The capabilities and characteristics of electrodepositable photoresists (EDPs) are best suited for this purpose. This coating process is based on the electrodeposition of a negative tone organic photoresist onto a cathodic polarised conductive substrate in a bath. However, a major disadvantage of this method is that it requires a conductive (metal) surface. Therefore, it cannot be used at all stages of a process. The equipment required, setup and handling are more complicated than other techniques and the coating bath should be checked and maintained frequently to remove free acid by ultrafiltration in order to get a reproducible process. Thus, electrodepositable photoresist technology is labor intensive, tedious and error-prone. Further, EDPs also have a short shelf life which is highly unsuitable for research purposes.

The above descriptions of the resists available for conformal coverage of a variable topography in silicon makes it obvious that they are process intensive and specialised techniques. Our effort in this work has been to develop an inductor design which may be fabricated by available IC processing technology with standard spin-on photoresists. To this end, we explored the option of changing the pyramidal geometry to make it more process friendly, especially in terms of photoresist coverage. This led to the proposed trench inductor geometry. The hypothesis in this scenario is that since

the sloped surfaces of the trench incline upward, the spin-on resist process will still provide relatively conformal coverage. The reason for this is that the same centrifugal force which spun the resist off the pyramidal surface in the previous cases, will cause the resist to move upward from the bottom of the pit along the sloping sidewalls, thus providing the required conformal coverage. This means that traditional spin-on photoresists may be used for the patterning of metal traces onto the trench sidewalls.

- **Photolithography Issues:** The strong topography of the substrate to be patterned constrains the choice of exposure tools [28]. Because of their small depth of focus, wafer steppers cannot be used. For best image quality, a focused beam writing equipment (eg. laser) should be used. However, high resolution images are rarely required in 3-D structures; therefore, the economic shadow mask printing delivers a sufficiently good quality for most applications. Two important issue that must be considered in the photolithography step are (a) diffraction, and (b) reflections on tilted sidewalls. Toward the bottom of the etch pits, the distance between the shadow mask and the photoresist can be fairly large and diffraction therefore plays an important role. Very little can be done concerning loss of resolution. However, the image quality may be improved by choice of proper development parameters. Definitely the most severe complication of lithography in 3-D structures is that the incidence of radiation may not be perpendicular everywhere in the system. Light may be reflected from tilted planes and may, at worst, cross-expose masked parts of the structure. This effect may be countered by choosing resists that have a relatively strong absorption of the specific wavelength of light being used for the exposure - strong enough to almost completely suppress reflections from the resist-metal surface. Further, the radiation exposure dose may be controlled to control this phenomenon.

- **Silicon Etch:** Having decided upon the trench pyramidal geometry for the reasons cited above, we are faced with the task of etching a deep $200\mu m - 500\mu m$ trench into the silicon wafer which will hold the inductor metal traces on its sidewalls. Silicon etch is traditionally carried out by a 20% Hydrofluoric Acid, 45% Nitric Acid and 35% Acetic Acid mixture at about 25^oC. This mixture has a rather rapid etch rate and is suitable for creating deep trenches in a relatively short span of time. For eg., the etch rate of the above etch is $\approx 5\mu m/min$ which means that a $500\mu m$ deep pit would take about 1.5 hours. However, the acidic mixture etches isotropically into the

wafer which translates into a slight curvature in the sidewalls of the etched pit, which is undesirable for our purposes.

An anisotropic etch is desired which is capable of creating sharply defined inclined sidewalls as required by the inductor geometry defined earlier. Heated alkaline KOH (with isopropyl alcohol) solutions at about 85^oC can be used for preferential etching of silicon along crystal planes. The etch rate will depend on the doping and crystal orientation and the type of KOH solution used, but is typically on the order of about $1\mu m/min$. We see that this is a rather slow etch in comparison since a a $500\mu m$ deep pit would take about 8 hours. This rate may be enhanced to about $1.4\mu m/min$ by increasing the temperature. However, to prevent boiling of the mixture, the temperature should not exceed 90^oC. Typically, a test wafer is etched to determine the exact etch rate since the rate depends on the current solution concentration which keeps changing as the etch proceeds. Readings from this test etch may be used to etch the wafers by the required amount. Since photoresist is susceptible to etching by KOH, we need to use another layer to mask the silicon wafer. Typically, Silicon Nitride, Si_3N_4 is used for this purpose. Further, since phosphoric acid H_3PO_4 is used to etch the nitride, silicon oxide SiO_2 is used to mask the nitride. Another important issue with the KOH etch is that potassium (K+) is an extremely fast-diffusing alkali metal ion and a lifetime killer for MOS devices. Thus, KOH etching is limited to designated areas of the cleanroom. Cleanroom users of KOH must observe proper procedures to avoid contaminating any metal-ion sensitive processes and equipment elsewhere in the lab. KOH-etched substrates, however, may be later processed in clean equipment, providing the procedures for decontamination are strictly followed.

- **Process Summary:** The formulation of the process flow for this specific process to construct on-chip inductors was conducted under the guidance of Dr. Mehmet Ozturk. The basic process to be followed in order to create the trench inductor is as follows:

  - RCA Clean: This preliminary step removes surface particles and impurities from the wafer and ensures that we have a clean wafer surface for subsequent processing.
  - Nitride CVD: A Si_3N_4 layer is deposited onto the bare silicon wafer using chem-

ical vapor deposition for purposes of masking the silicon wafer for the KOH etch.

- Oxide CVD: An SiO_2 layer is then deposited over the nitride layer for the purpose of masking the nitride layer during the H_3PO_4 etch.
- Photoresist Spin-On: Photoresist is then spun onto the oxide surface to mask the oxide etch.
- Photolithography: The photoresist is exposed using a mask defining the rectangular shape of trench. Developer solution is then used to wash away the developed resist.
- Oxide Etch: The SiO_2 layer is etched in hydrofluoric acid, HF. The photoresist mask is washed away with photoresist remover.
- Nitride Etch: The Si_3N_4 layer is etched with hot H_3PO_4 using the oxide layer as a mask for the process.
- Silicon Etch: The alkaline KOH etch is used to etch the silicon wafer using the nitride as a mask. This process also removes the oxide mask left over from the previous step.
- Nitride Removal: The nitride mask from the previous step is then stripped using the H_3PO_4 etch. Thus, we have now obtained the trench in the silicon wafer. We must now obtain the aluminum inductor traces along the sidewalls.
- Oxide CVD: An SiO_2 layer is then deposited over the trench for the purpose of acting as the base on which the inductor is formed.
- Aluminum CVD: An Al layer is then deposited over the oxide to form the metallic inductor traces.
- Photoresist Spin-On: Photoresist is dropped into the trench and the wafer is spun to obtain conformal coverage over the sidewalls of the trench.
- Photolithography: The photoresist is exposed using a mask defining the inductor geometry. Developer solution is then used to wash away the developed resist.
- Aluminum Etch: The metal is now etched using an aluminum etch containing phosphoric acid, H_3PO_4, nitric acid, HNO_3, water, H_2O, and acetic acid, CH_3COOH as a buffer. The photoresist mask is washed away with photoresist remover. Thus, the inductor metal traces now lie along the sidewalls of the trench.

This completes the process definition for the fabrication of the trench pyramidal inductor. Inductors fabricated by this process may now be measured to validate that the inductance values match those predicted by the computational method. A good match of the values will verify the validity of the method for on-chip inductor dimensions. A cleanroom process flow diagram for the inductor fabrication is illustrated on the subsequent pages.

- **Cleanroom Process Flow Diagram:**
  (Formulated under the guidance of Dr. Mehmet Ozturk)

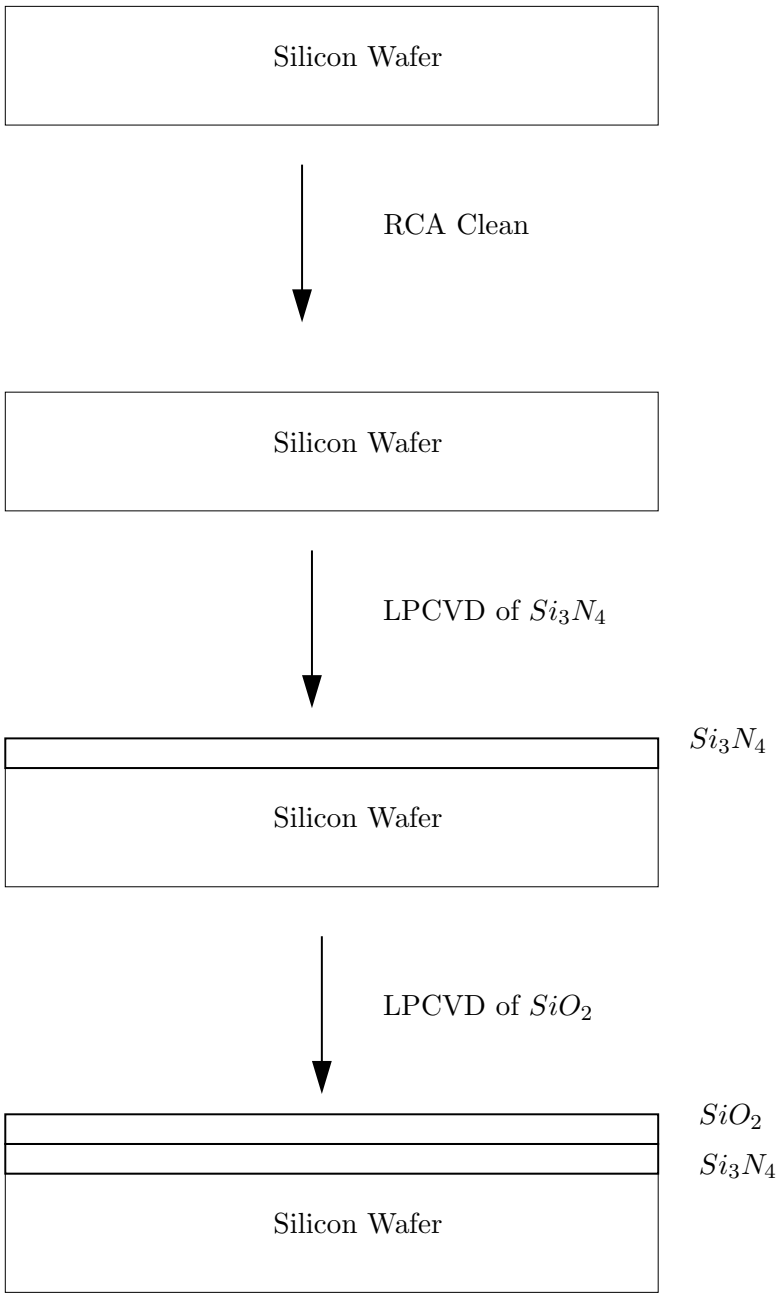


Figure 2.4: Process Flow Diagram(contd.)

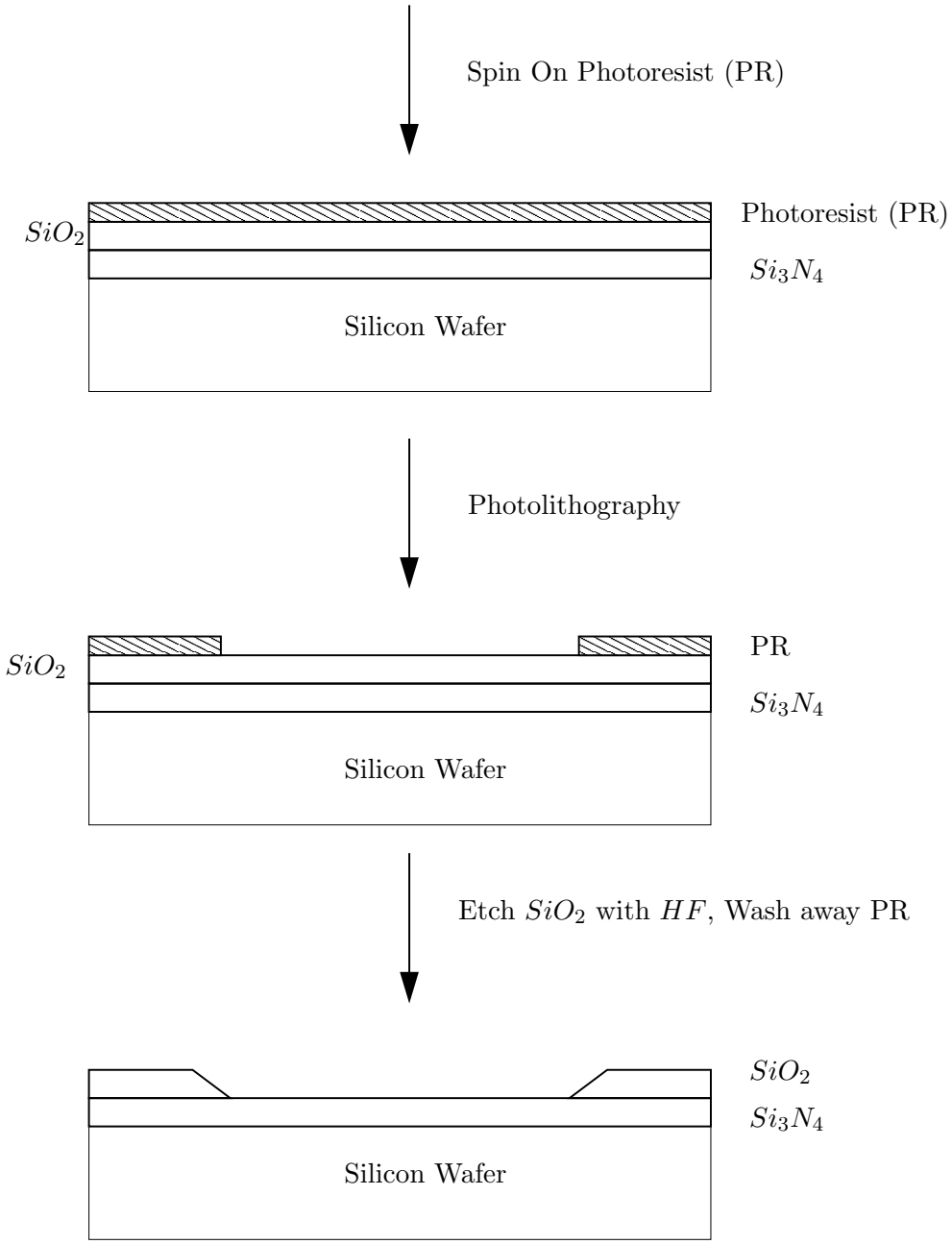


Figure 2.5: Process Flow Diagram (contd.)

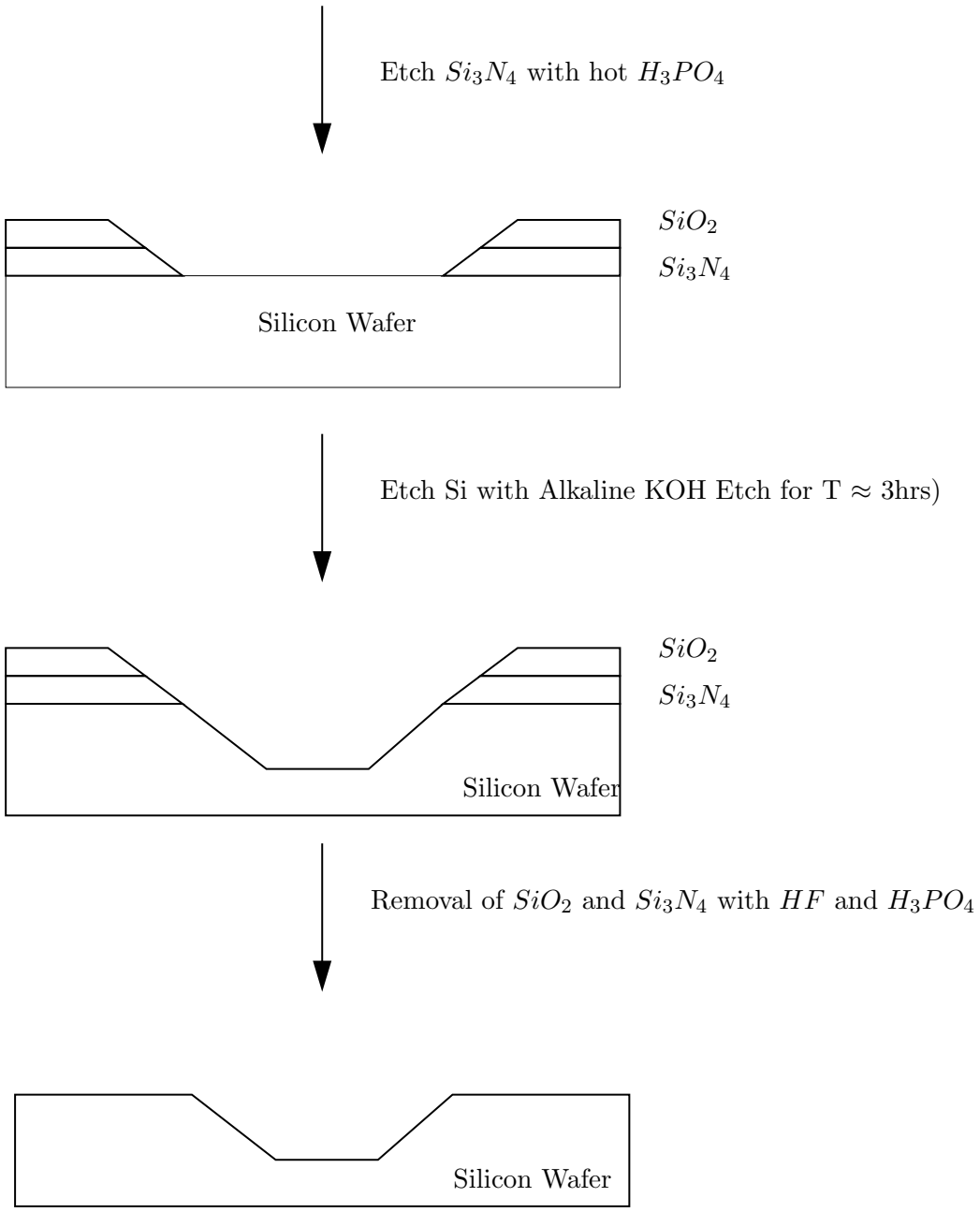


Figure 2.6: Process Flow Diagram (contd.)

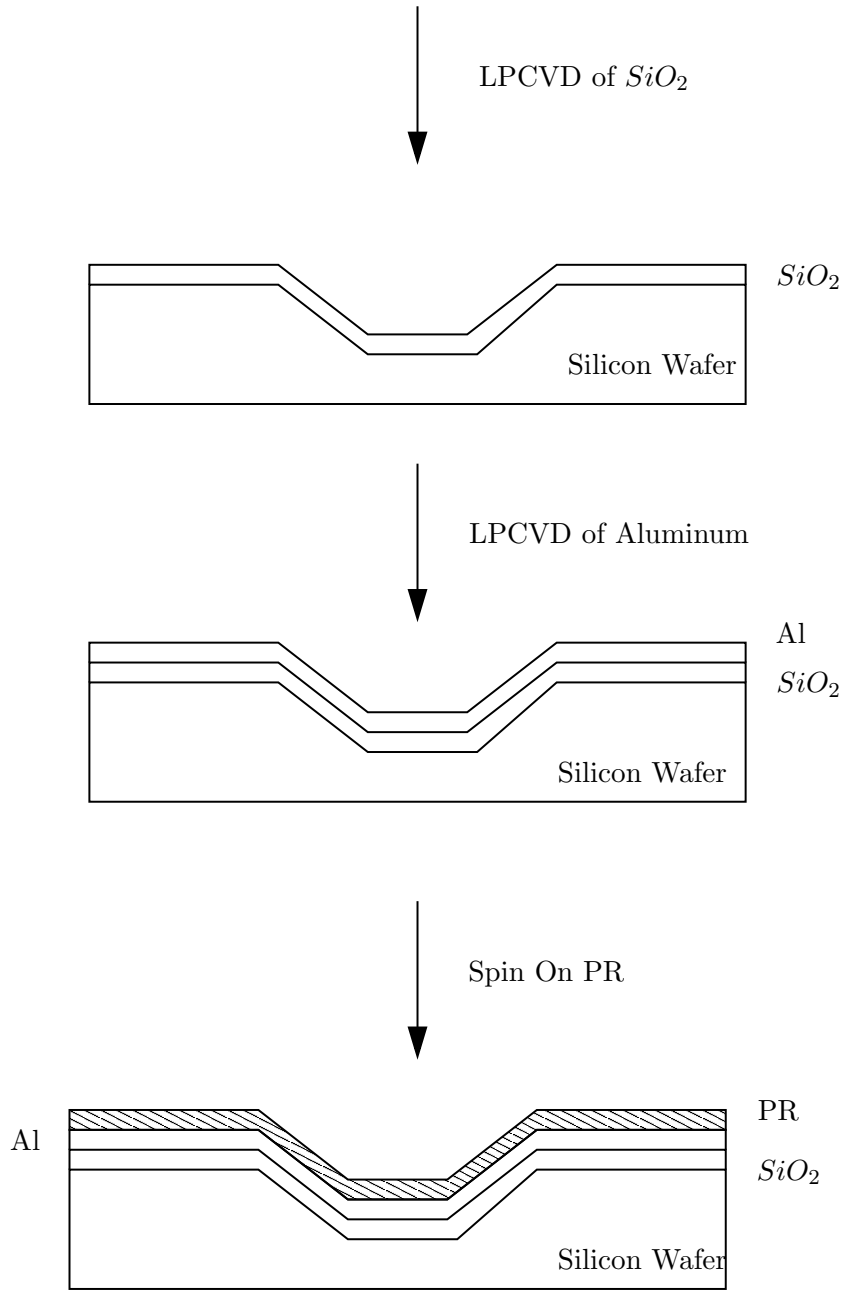


Figure 2.7: Process Flow Diagram (contd.)

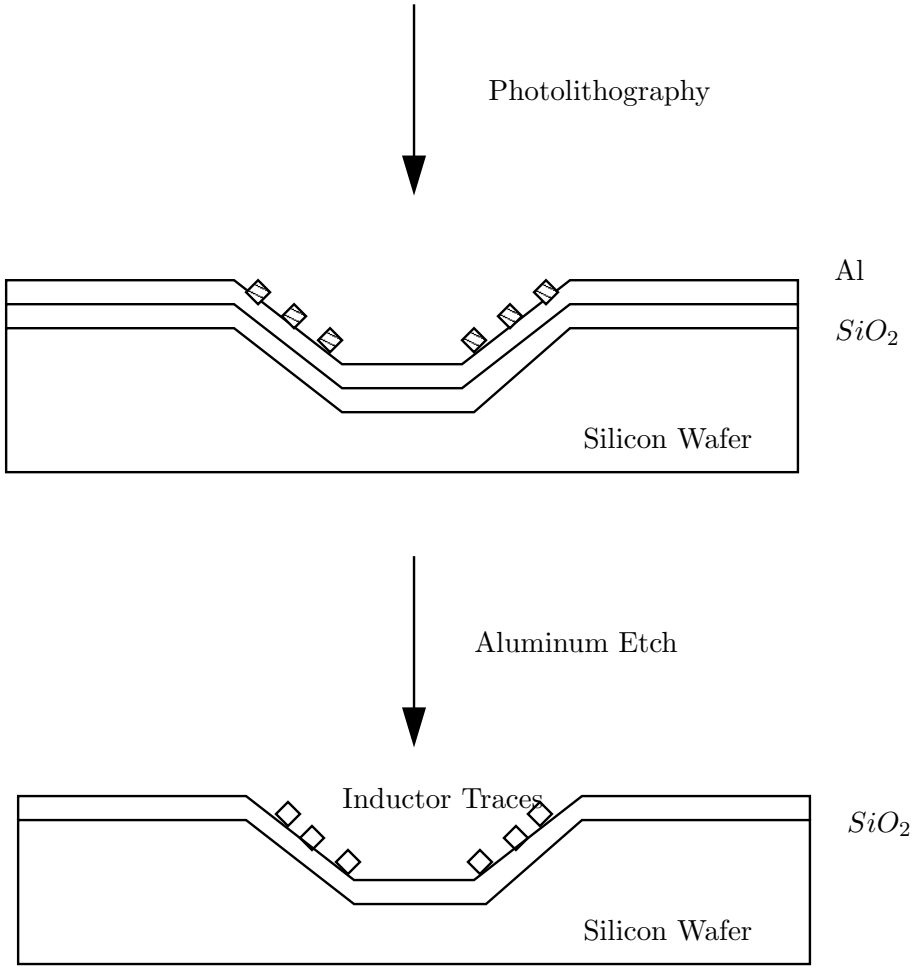


Figure 2.8: Process Flow Diagram

Chapter 3

The Partial Inductance Method

The objective of this work is to develop a computational method which can predict the self and mutual inductance values of certain inductor geometries with reasonable accuracy and speed in order to be able to decide the optimal inductor geometry to be used for power transfer to the transcutaneous biomedical implant. Several methods were explored to decide which approach would solve the problem reliably and elegantly. The primary factors considered were efficiency, simplicity and computational speed. The partial inductance method satisfied all three criteria and seemed to be the best way to proceed for a variety of reasons. As it turns out, the partial inductance method, like most other inductance calculation methods, can theoretically find out the inductance values of any given structure. However, for the specific structures we are interested in, the partial inductance method simplifies the problem greatly due to the symmetry and regularity of the geometries under investigation. This greatly reduces the complexity of the problem. Further, since this method does not depend on full electromagnetic field solving techniques which require iterative simulation of the entire problem space, the computational time required is on the order of seconds instead of hours. Finally, the inherent accuracy of partial inductance method is borne out by the fact that it is used widely for the purposes of on-chip interconnect inductance matrix calculations in which the accuracy of inductance values is very important [29] [30].

In essence, the partial inductance method partitions a structure into various *parts* which can then be used to calculate partial inductances with respect to other parts of

the same or different structure. These values of partial inductance comprise the partial inductance matrix and the self or mutual inductance values desired may be calculated by summing over the elements of the inductance matrix.

3.1 Inductive Interaction between Conductors

The process of inductive interaction between conductors carrying currents can be decomposed into three effects which take place concurrently [22]:

- Currents flowing through conductors create magnetic fields (Ampere's Law)
- Magnetic fields varying with time create induced electric fields (Faraday's Law)
- Induced electric fields exert forces upon the electrons in the conductors and cause electric voltage (Electric Potential) drops.

3.1.1 Ampere's Law

Currents flowing through conductor loops and time- varying electric fields create magnetic fields. This relationship between current density j, the electric field E and the resulting magnetic field B is Ampere's Law:

$$\nabla \times \mathbf{B} = \mu \mathbf{j} + \mu\epsilon \frac{\partial \mathbf{E}}{\partial t} \tag{3.1.1}$$

The first term on the right hand side of (3.1.1) represents the contribution of the current density to the magnetic field on the left hand side. μ is the magnetic permeability of the insulator surrounding the wires and ϵ its electric permittivity. The curl operator on the left hand side causes the resulting magnetic field to be wrapped around the existing current flow patterns (see Fig. 3.1). The integral form, which can be derived from (1) via Stokes' Law, is

$$\oint_S \mathbf{B} \cdot \mathbf{dl} = \mu \int_S \left(\mathbf{j} + \epsilon \frac{\partial \mathbf{E}}{\partial t} \right) \cdot \mathbf{dS} \tag{3.1.2}$$

where S is a surface which intersects the wire (see Fig. 3.1). The current through the wire creates a magnetic field around the wire. For a general, three-dimensional current flow this

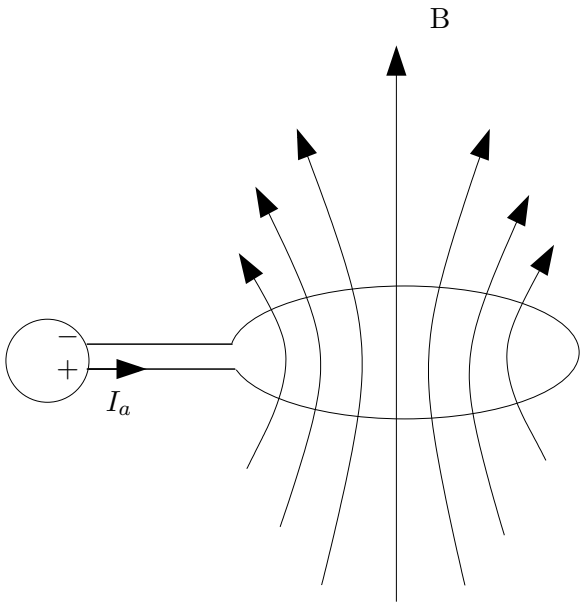


Figure 3.1: Magnetic Field created by time-variant current flowing through conductor loop

field is difficult to predict intuitively, but for one-dimensional wires the field direction can be predicted with the right- hand rule: if the thumb of the right hand points in current direction, the other fingers point in direction of the magnetic field.

The second term in the right-hand side integral of (3.1.2) is referred to as the displacement current density, since it has the dimension of a current density and represents the ac current flowing between two conductors due to their capacitive couplings. Time-varying electric fields can create magnetic fields. Usually, however, this term is neglected in Ampere's Law for integrated circuits since the magnetic field created directly by the currents flowing within the conductors is larger than the magnetic field created by the displacement currents - even with dominant lateral capacitance coupling - by at least one order of magnitude.

Discarding the displacement current term in (3.1.2) decouples the inductive and capacitive effects within the circuit; therefore this step is referred to as a quasistatic approximation, since the capacitive electric fields are assumed to be roughly (quasi) static and variations of the potential differences between conductors are sufficiently slow such that the displacement term is negligible compared with the current term. The quasi-static (differential and integral) form of Ampere's Law is:

$$\nabla \times \mathbf{B} = \mu \mathbf{j} \tag{3.1.3}$$

or

$$\oint_S \mathbf{B} \cdot \mathbf{dl} = \mu \int_S \mathbf{j} \cdot \mathbf{dS} \tag{3.1.4}$$

Though the displacement current contribution to the magnetic field is usually negligible, the displacement current itself, however, is not negligible. It may be shown that the contribution of the displacement currents to the magnetic field is negligible.

3.1.2 Faraday's Law

Ampere's Law gives us the first part of the inductive process: the creation of the magnetic field. Only if these magnetic fields vary with time do these fields create induced electric fields. Therefore, time-variant currents are required for induction, the relationship of which is Faraday's Law:

$$\oint_j \mathbf{E_{ind}} \cdot \mathbf{dl} = -\frac{\partial \phi}{\partial t} \tag{3.1.5}$$

where $\phi = \int \mathbf{B} \cdot \mathbf{dS}$ is the magnetic flux with the integral taken over the area of the primary loop and E_{ind} is the induced electric field in the secondary loop. The induced electric field wraps around the magnetic field lines (see Fig. 3.2). The portion of the induced electric field which is parallel to the wire of the loop in Fig. 3.2 exerts force on the charges and creates voltage in the loop. The induced E-field is caused by the time-variant magnetic field in Eq.(3.1.4). The orientation of the loop with respect to the induced electric field determines the amount of induced voltage. If the loop is orthogonal to the induced E-field the total effect of the magnetic field on it will be zero (As we will see later in a more detailed derivation, this causes partial inductive couplings between orthogonal wires to become zero).

3.1.3 Electric Potential

The induced electric field can be integrated along the victim loop and results in an induced voltage which adds to the already existing voltage due to the resistance of the loop:

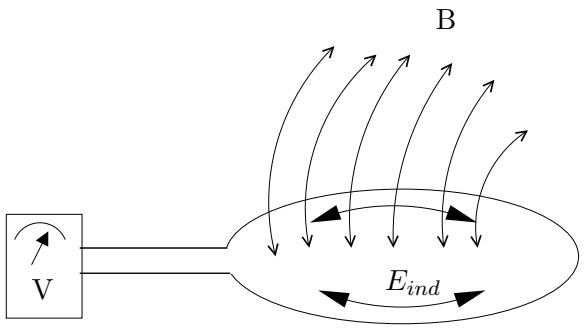


Figure 3.2: Electric Voltage created by time-variant magnetic field passing through a conductor loop

$$V_i^{ind} = -\oint_i \mathbf{E_{ind}} \cdot \mathbf{dl} \tag{3.1.6}$$

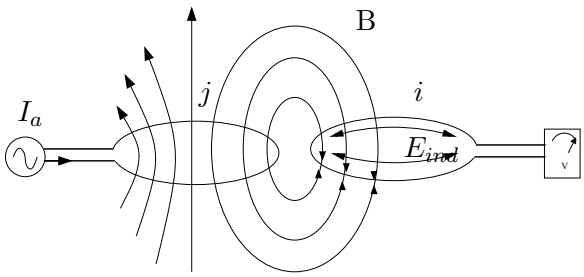


Figure 3.3: Magnetic Field created by the time-variant current in loop j induces voltage in loop i, since some of the magnetic field passes through i

3.1.4 Loop Inductance

Fig. 3.3 summarizes the combination of these three effects which combine to generate a voltage drop in the victim loop i due to a time-variant current in loop j. All three relationships involved in the preceding equations are linear. Therefore, the resulting combined relationship between time-derivatives of currents in the loops and the resulting induced voltage drop is linear as well:

$$V_i^{ind} = L_{ij} \frac{\partial I_j}{\partial t} \tag{3.1.7}$$

where $I_j = \int \mathbf{j} \cdot \mathbf{dS}$ and the integral is taken over the cross sectional area of conductor j.

L_{ij} is the mutual inductance of loop j upon loop i and I_j is the current flowing through the loop j. V_i^{ind} is the voltage induced in the victim loop i. For the special case where loops i and j are the same, the coefficient L_{ii} is the self inductance of loop i.

3.2 The Partial Inductance Concept

Inductance is defined as the ratio of the total magnetic flux that couples a closed path to the current that is the source of the magnetic flux,

$$L_{ij} \equiv \frac{\phi_{ij}}{I_j} \tag{3.2.1}$$

where the current I_j flows in loop j and causes flux ϕ_{ij} to be set up in closed loop i.

Clearly, the concept of inductance is defined only for closed loops. The need for partial inductances arises because we often deal with open loops or single linear conductors for which the associated magnetic flux coupling cannot be readily defined. The concept of a partial inductance was first developed by Rosa [31] in 1908 in application to linear conductors and Grover [32] provided a comprehensive summary of partial inductances in 1946. A rigorous theoretical treatment of the subject was provided by Ruehli in [21], where the general definition of the partial inductance of an arbitrarily shaped conductor is given in terms of the magnetic vector potential. Ruehli formulated the partial inductance concept for calculating multiloop inductances by dividing conductor loops into segments for which the partial inductances were calculated. The partial inductance is intended to represent the inductance that a circuit segment contributes as part of a closed loop circuit. A brief review of the concept is given below.

If there exist two closed loops i and j with a current I_j flowing in loop j, the mutual inductance between loops i and j is given by (3.2.1). The flux ϕ_{ij} developed in loop i is related to the magnetic vector potential $\mathbf{A}_{ij}$, generated by the current I_j flowing in loop j, as

$$\phi_{ij} = \frac{1}{a_i} \oint_i \int_{a_i} \mathbf{A}_{ij} \cdot \mathbf{dl}_i \, da_i \tag{3.2.2}$$

where $d\mathbf{l}_i$ is an element of conductor i with direction along the axis of the conductor and a_i represents the cross sectional area of conductor i.

The expression for the magnetic vector potential generated by the current I_j is given by

$$\mathbf{A}_{ij} = \frac{\mu}{4\pi}\frac{I_j}{a_j}\oint_j \int_{a_j} \frac{d\mathbf{l}_j\, da_j}{r_{ij}} \tag{3.2.3}$$

where $r_{ij} = \mid \mathbf{r}_i - \mathbf{r}_j \mid$.
Inserting (3.2.3) in (3.2.2) and using the result in (3.2.1) yields

$$L_{ij} = \frac{\mu}{4\pi}\frac{1}{a_i a_j}\oint_i \int_{a_i} \oint_j \int_{a_j} \frac{d\mathbf{l}_i \cdot d\mathbf{l}_j}{r_{ij}}\, da_i da_j \tag{3.2.4}$$

To develop relations for the inductances of the segments of the loops, we partition each loop into a number of segments and re-write the integrations over the lengths as summations over the straight loop segments

$$L_{ij} = \sum_{k=1}^{K}\sum_{m=1}^{M} \frac{\mu}{4\pi}\frac{1}{a_k a_m} \int_{a_k}\int_{a_m}\int_{b_k}^{c_k}\int_{b_m}^{c_m} \frac{d\mathbf{l}_k \cdot d\mathbf{l}_m}{r_{ij}}\, da_k da_m \tag{3.2.5}$$

where loop i is divided into K segments and loop j into M segments, a_k and a_m are the cross sectional areas of the k^{th} and m^{th} segments, b_k and b_m are the starting points of the k^{th} and m^{th} segments and c_k and c_m are the end points of the k^{th} and m^{th} segments respectively.

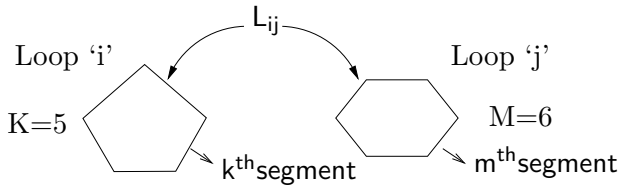


Figure 3.4: Partitioning of Loops into Segments

From this expression, we see that the argument of the double summation can be defined as the partial inductance of the loop segments as

$$L_{p_{km}} = \frac{\mu}{4\pi}\frac{1}{a_k a_m} \int_{a_k}\int_{a_m}\int_{b_k}^{c_k}\int_{b_m}^{c_m} \frac{\mid d\mathbf{l}_k \cdot d\mathbf{l}_m \mid}{r_{ij}}\, da_k da_m \tag{3.2.6}$$

leading to a more compact representation of the loop inductance in terms of the partial inductance of the loop segments as

$$L_{ij} = \sum_{k=1}^{K}\sum_{m=1}^{M} S_{km} L_{p_{km}} \tag{3.2.7}$$

Here S_{km} is a sign term which is determined by the scalar product between the current vectors i and j and is zero for the case of orthogonal current segments. Further, it is evident that the derived partial mutual inductance formula (3.2.6) can be transformed into a partial self inductance formula by making both the indices the same, i.e $L_{p_{kk}}$ is obtained by performing both sets of integrations over the same conductor.

From (3.2.6), we observe that the line integrals within the area integration can be identified as the inductance between any two filaments r and s belonging to the two conductor segments k and m

$$L_{pf_{rs}} = \frac{\mu}{4\pi} \int_{b_r}^{c_r} \int_{b_s}^{c_s} \frac{\mid d\mathbf{l}_r \cdot d\mathbf{l}_s \mid}{r_{rs}} \tag{3.2.8}$$

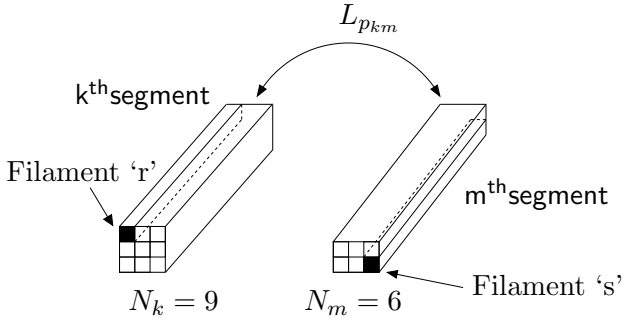


Figure 3.5: Partitioning of Segments into Filaments

The partial inductance formula given by (3.2.6) takes into account finite conductor cross sectional area. To facilitate computations, the integral over each segment's cross sectional area in the partial inductance formula is transformed into a summation by partitioning it into a large (ideally infinite) number of rectangular cross sectional areas representing filamentary cross sections. If the cross sectional areas of the k^{th} and m^{th} segments are divided into N_k and N_m rectangles respectively, (3.2.6) could be re-written as the normalized summation of the partial inductances of $N_k \times N_m$ filaments

$$L_{p_{km}} = \lim_{N_k, N_m \to \infty} \frac{1}{N_k N_m} \sum_{r=1}^{N_k} \sum_{s=1}^{N_m} L_{pf_{rs}} \tag{3.2.9}$$

Though N_k and N_m should ideally be very large, it will be seen that in practical computations where the distance between the segments is much larger than the cross sectional dimensions of the conductor, few or no filaments are needed per segment for accurate results.

Hence, the process of calculating the inductance based on this partial inductance concept is as follows. The loop to be analyzed is broken into smaller segments, each of which does not by itself form a closed circuit. Typically, the loop is partitioned into elements of simple shape, such as straight wire elements of constant cross section for which precise and convenient analytical partial inductance formulae are available. Each of these segments is assigned a partial self inductance and each pair of these segments is assigned a partial mutual inductance. The partial self and mutual inductances of the loop segments and the topology of the segment connections are all the information required to calculate the total self and mutual inductance of the circuit. The partial inductance matrix for a set of n conductors is an $n \times n$ real symmetric matrix. The diagonal terms of this matrix are the partial self inductances while the off-diagonal terms are partial mutual inductances. The inductance of the loop can be calculated from this matrix by using (3.2.7) in which the summation terms shown are precisely the partial inductance matrix elements.

3.3 Useful Partial Inductance Formulae

In order to calculate the elements of a partial inductance matrix of a standard inductive coil geometry consisting of linear segments of rectangular cross section, we need the partial self inductance formula for a linear conductor of rectangular cross section. The closed form expression of this formula is given in [21] and involves the length, width and thickness of the conductor segment. A different mathematical form of the same formula which is easier for computations is given by Kundu [33] and is used for the calculation of all partial self inductances in this paper.

Let the length of the k^{th} segment be $l[k]$ and the width and thickness be $W[k]$ and T respectively. Defining the normalized width and thickness as $w = W[k]/l[k]$ and $t = T/l[k]$ and some other parameters $r = \sqrt{w^2 + t^2}$, $a_w = \sqrt{w^2 + 1}$, $a_t = \sqrt{t^2 + 1}$ and $a_r = \sqrt{w^2 + t^2 + 1}$, the partial self inductance of the segment k can be written as:

$$
\begin{aligned}
L_{p_{kk}} = \frac{2\mu l_k}{\pi}\Bigg\{ & \frac{1}{4}\left[\frac{1}{w}S\left(\frac{w}{a_t}\right)+\frac{1}{t}S\left(\frac{t}{a_w}\right)+S\left(\frac{1}{r}\right)\right] \\
& +\frac{1}{24}\left[\frac{t^2}{w}S\left(\frac{w}{ta_t(r+a_r)}\right)+\frac{w^2}{t}S\left(\frac{t}{wa_w(r+a_r)}\right)\right] \\
& +\frac{1}{24}\left[\frac{t^2}{w^2}S\left(\frac{w^2}{tr(a_t+a_r)}\right)+\frac{w^2}{t^2}S\left(\frac{t^2}{wr(a_w+a_r)}\right)\right] \\
& +\frac{1}{24}\left[\frac{1}{wt^2}S\left(\frac{wt^2}{a_t(a_w+a_r)}\right)+\frac{1}{tw^2}S\left(\frac{tw^2}{a_w(a_t+a_r)}\right)\right] \\
& -\frac{1}{6}\left[\frac{1}{wt}T\left(\frac{wt}{a_r}\right)+\frac{t}{w}T\left(\frac{w}{ta_r}\right)+\frac{w}{t}T\left(\frac{t}{wa_r}\right)\right] \\
& -\frac{1}{60}\left[\frac{(a_r+r+t+a_t)t^2}{(a_r+r)(r+t)(t+a_t)(a_t+a_r)}\right] \\
& -\frac{1}{60}\left[\frac{(a_r+r+w+a_w)w^2}{(a_r+r)(r+w)(w+a_w)(a_w+a_r)}\right] \\
& -\frac{1}{60}\left[\frac{(a_r+a_w+a_t+1)w^2}{(a_r+a_w)(a_w+1)(a_t+1)(a_t+a_r)}\right] \\
& -\frac{1}{20}\left[\frac{1}{(r+a_r)}+\frac{1}{(a_w+a_r)}+\frac{1}{(a_t+a_r)}\right]\Bigg\} \qquad (3.3.1)
\end{aligned}
$$

where $S(x) = \log_e\left(x+\sqrt{1+x^2}\right)$ and $T(x) = \arctan(x)$

For the partial mutual inductances, it will be shown in Section 3.5 that partitioning of the cross section of the segments into a number of filaments is not required for the current work since the segment separation dimensions are larger than the cross sectional dimensions for all geometries considered. Simulations comparing the partial mutual inductance values obtained with and without the partitioning of each segment into filaments prove that the differences are negligible. Thus, the loop segments are treated as single filaments for the purposes of partial mutual inductance calculations and the formulae provided by Grover [32] for various configurations of parallel filaments are used in this work.

For the case of two equal parallel straight filaments of length l and distance of separation d, the partial mutual inductance is given by

$$
M = \frac{\mu l}{2\pi}\left[\log_e\left(\frac{l}{d}+\sqrt{1+\frac{l^2}{d^2}}\right)-\sqrt{1+\frac{d^2}{l^2}}+\frac{d}{l}\right] \qquad (3.3.2)
$$

For the case of unequal parallel filaments with varying degrees of overlap, a combination of sum and difference terms based on the above formula gives the expression for the partial

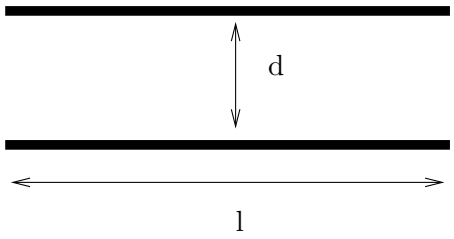


Figure 3.6: Two Equal Parallel Filaments

mutual inductance. If M_l is used as the notation to represent the mutual inductance of 2 equal parallel filaments spaced at a distance d for the given configuration, the mutual inductance formulae for the different cases are given by:

- *Unequal Parallel Offset Filaments*

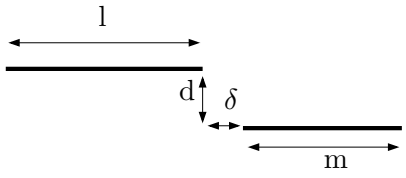


Figure 3.7: Unequal Parallel Offset Filaments

$$M = \frac{1}{2}\left[(M_{l+m+\delta} + M_{\delta}) - (M_{l+\delta} + M_{m+\delta})\right] \tag{3.3.3}$$

- *Unequal Parallel Overlapping Filaments*

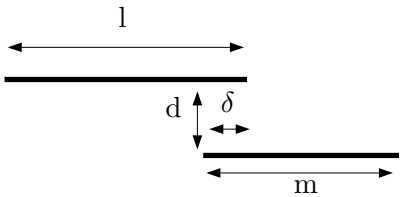


Figure 3.8: Unequal Parallel Overlapping Filaments

$$M = \frac{1}{2}\left[(M_{l+m-\delta} + M_{\delta}) - (M_{l-\delta} + M_{m-\delta})\right] \tag{3.3.4}$$

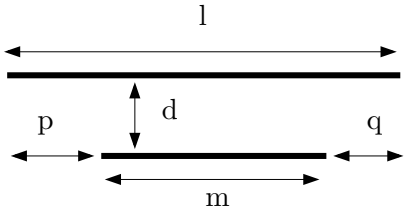


Figure 3.9: Unequal Parallel Filaments with complete Overlap

- *Unequal Parallel Filaments with complete Overlap*

$$M = \frac{1}{2}\big[(M_{m+p} + M_{m+q}) - (M_p + M_q)\big] \tag{3.3.5}$$

- *Unequal Parallel Filaments with Ends on Common Perpendicular*

  - On Same Side of Perpendicular

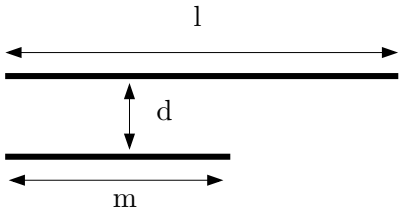


Figure 3.10: Unequal Parallel Filaments with Ends on same side of Common Perpendicular

$$M = \frac{1}{2}\big[(M_l + M_m) - (M_{l-m})\big] \tag{3.3.6}$$

  - On Opposite Sides of Perpendicular

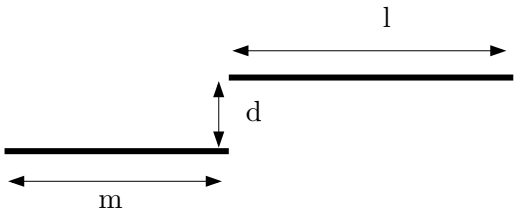


Figure 3.11: Unequal Parallel Filaments with Ends on opposite sides of Common Perpendicular

$$M = \frac{1}{2}\big[(M_{l+m}) - (M_l + M_m)\big] \tag{3.3.7}$$

- *Special Case of Unequal Coaxial Filaments*

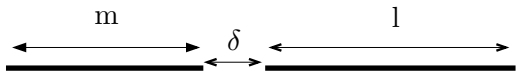


Figure 3.12: Special Case of Unequal Coaxial Filaments

$$M = \frac{\mu}{4\pi}\left[l\log_e\frac{l+m}{l} + m\log_e\frac{l+m}{m}\right] \tag{3.3.8}$$

3.4 The Computational Method

The Partial Inductance concept is used to calculate the self and mutual inductances of various 2-D and 3-D geometries. The computational method developed uses the symmetry and/or regularity of the inductor geometries to facilitate rapid calculation of the partial mutual inductances. A step-by-step algorithm is described below for the process of calculating the inductance values of the geometries. This algorithm is coded in C for each different type of geometry i.e separate C programs are written for loops, spirals, helices, pyramids etc. The program for a certain geometry can be used to evaluate various different variations of that geometry - with different dimensions, track spacing, metal width, thickness etc. This serves as a useful tool for the rapid comparison of inductances of various geometries and variations of a certain geometry.

3.4.1 Algorithm for Self-Inductance Calculation

The following algorithm describes the process of entering a specific inductor geometry into the code and calculating its self inductance value from its partial inductance matrix.

- *Segment Partitioning:* The inductor geometry is partitioned into a number of segments depending on the geometric symmetry and regularity of the structure and specified in the code as an array of numbered segments. This essentially performs the important step of dividing the inductor into a finite number of partial elements for the partial

inductance analysis. Each of the segments is a partial element and will have its own partial inductance value $L_{p_{kk}}$.

- *Dimensional Parameter Specification:* The initialization of the segment lengths, widths and thicknesses are performed and stored in array variables. Variable conductor widths over the inductor geometry are facilitated by allowing each segment's width to be specified separately. The thickness is assumed constant over the entire inductor since it is usually not possible to vary metallization thickness over different segments. By a suitable choice of segment partitions for the geometry, variable inductor widths may be accommodated.

- *Coordinate Calculation:* The coordinates of the various segments and their endpoints are calculated based on the geometry of the structure. The calculation and storage of the coordinate positions of each segment's endpoints and its axial location facilitates the determination of the distances between segments.

- *Sign Allocation:* The geometric regularity of the structure is exploited in handling the sign assignment for parallel segments and in determining the positions of the zeros in the inductance matrix. The sign assigned to a partial inductance term arises from the relative current direction in each pair of segments in the inductor. This will decide the sign term S_{km} for each pair of segments k and m. Thus, parallel loop segments are assigned a value of either $+1$ or -1 based on the relative direction of current while perpendicular loop segments are assigned a value of 0, since their partial mutual inductance is evidently zero. We also expect the diagonal elements of the partial self inductance matrix to be positive.

- *Partial Self Inductance Calculation:*The partial self inductance calculations of all segments are based on the self inductance formula for a conductor with rectangular cross-section, Eqn. 3.3.1. The formula uses the length, width and thickness of each conductor segment to calculate the partial self inductance of that segment. These values of partial self inductances $L_{p_{kk}}$ form the diagonal elements of the partial self inductance matrix $[L_{p_{km}}]$.

- *Partial Mutual Inductance Calculation:* The partial mutual inductances between the segments of the same inductor are calculated using Grover's formulae for mutual

inductances of filaments in various parallel configurations, Eqns. 3.3.2 - 3.3.8. These calculations utilize the lengths and coordinate locations of the segments calculated earlier. The partial mutual inductance values $L_{p_{km}}$ populate the off-diagonal elements in the partial self inductance matrix. The appropriate signs S_{km} calculated earlier are associated with the off-diagonal values.

- *Matrix Summation:* The summation of the partial inductance matrix of the inductor 'i' gives the value of the self inductance L_{ii}.

3.4.2 Algorithm for Mutual-Inductance Calculation

The algorithm for mutual inductance calculation is similar to the previous algorithm. In this case, there are two different inductor geometries, both of which are partitioned into segments and the segments are then used to compute the elements of the partial inductance matrix; and hence the mutual inductance of the inductor configuration.

- *Segment Partitioning:* The two inductor geometries are both partitioned into a number of segments depending on the geometric symmetry and regularity of each structure and specified in the code as two separate arrays of numbered segments. This essentially performs the important step of dividing both inductors into a finite number of partial elements for the partial inductance analysis. Each segment of an inductor is a partial element and will have a mutual inductance with each segment of the other inductor, leading to the partial inductance matrix elements $[L_{p_{km}}]$. A diagonal element in this matrix is simply the mutual inductance of two segments with the same segment numbers in the two inductors. Hence, there is no intrinsic difference between the diagonal and off-diagonal elements of this matrix.

- *Dimensional Parameter Specification:* The initialization of the segment lengths, widths and thicknesses are performed and stored in array variables. Variable conductor widths over the inductor geometry are facilitated by allowing each segment's width to be specified separately. The thickness is assumed constant over the entire inductor since it is usually not possible to vary metallization thickness over different segments. By a suitable choice of segment partitions for the geometry, variable inductor widths may be accommodated.

- *Coordinate Calculation:* The coordinates of the various segments of both inductors and their endpoints are calculated based on the geometry of the structure. The calculation and storage of the coordinate positions of each segment's endpoints and its axial location facilitates the determination of the distances between segments.

- *Sign Allocation:* The geometric regularity of the structures is exploited in handling the sign assignment for parallel segments and in determining the positions of the zeros in the inductance matrix. The sign assigned to a partial mutual inductance term arises from the relative current direction in the pair of segments. This will decide the sign term S_{km} for a pair of segments k and m, which belong to loops i and j respectively. Thus, parallel segments are assigned a value of either $+1$ or -1 based on the relative direction of current while perpendicular segments are assigned a value of 0, since their partial mutual inductance is evidently zero.

- *Partial Mutual Inductance Calculation:* The partial mutual inductances between the segments of the two inductors are calculated using Grover's formulae for mutual inductances of filaments in various parallel configurations, Eqns. 3.3.2 - 3.3.8. These calculations utilize the lengths and coordinate locations of the segments calculated earlier. The partial mutual inductance values $L_{p_{km}}$ populate both the diagonal and off-diagonal elements in the partial mutual inductance matrix. The appropriate sign S_{km} calculated earlier is associated with each matrix element.

- *Matrix Summation:* The summation of the partial inductance matrix of the inductor pair i and j gives us the value of the mutual inductance L_{ij}.

3.5 Justification for Non-Filamentisation of Segments

As mentioned in a preceding section, the partial inductance method allows us to partition the cross section of a given segment into a number of elements, which are then treated as filaments for purposes of inductance calculations. We term the process of partitioning the cross section of a given segment as 'filamentisation'. However, we shall prove here that the error due to non-filamentisation of segments in this work is negligible due to the dimensions of the segments and the separations between them. This implies that we can treat segments as filaments for the purposes of partial mutual inductance calculations,

thus greatly reducing the complexity of the computational algorithm without sacrificing the accuracy of the predicted result.

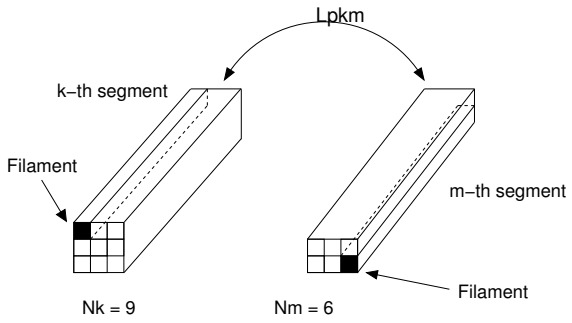


Figure 3.13: Partitioning of Segments into Filaments

Without filamentisation, the partial mutual inductance between two segments k and m would be calculated by treating each of them as a single filament. With filamentisation, each segment is partitioned into a number of filaments and the inductance is calculated as the interaction of the filaments of one conductor with those of the other. For example, in Fig. 3.13, we see that the k^{th} segment has been partitioned into 9 filaments while the m^{th} segment has been partitioned into 6 filaments. The partial mutual inductance in this case would be obtained by calculating the weighted sum of the inductances of the filaments which comprise the two segments.

$$L_{p_{km}} = \frac{1}{9 \times 6} \sum_{r=1}^{9} \sum_{s=1}^{6} L_{pf_{rs}} \tag{3.5.1}$$

To gain a quantitative idea of whether this filamentisation is required in our work, we analyze the the different cases of interest for inductance calculations. We then compare the inductance values computed by utilizing filamentisation to the values obtained without filamentisation. We may differentiate the various possible inductance calculation scenarios into the cases of (a) mutual inductance between two inductor structures, and (b) self inductance of an inductor structure. Further, it should be mentioned that the test structures fabricated to validate the computational method are actually dimensionally scaled versions of the intended on-chip inductor structures. Therefore, for each of the cases above, we are required to justify the validity of our assumption for (i) test structure dimensions, and (ii) on-chip inductor dimensions. If the error observed is negligible, we may safely treat

each segment of our inductors as a filament for the purposes of partial mutual inductance calculations and thereby reduce the complexity of the computational algorithm.

3.5.1 Mutual Inductance Case

The calculation of the mutual inductance matrix for a two-inductor configuration consists of finding the partial mutual inductances between the segments of one inductor with respect to the other. Thus, it is clear that any two segments being considered for purposes of partial mutual inductance calculation are separated approximately by the distance of separation between the two inductors. The distance of separation between the two inductor structures of a biomedical implant depends on how deep the implant is embedded within the body and how close to the body the external unit is located. Since this distance is typically large compared to the dimensions of the inductors, we expect that the segments may be approximated as filaments and the error introduced should be negligible. We consider two cases for the order of dimensions.

- **Test Structure Dimensions:** As we shall see later in Chapter 4, the dimensions of the test structures are scaled up with respect to the actual dimensions of the proposed on-chip inductors. For purposes of this calculation, we take a range of values for the various dimensional parameters - linewidth W, metallization thickness T, distance of separation D and length of segments L - approximated over the various test structures that were fabricated. The specific case we shall consider for our calculations is that of two straight equal parallel segments as shown in Fig. 3.13 and compare the values of partial mutual inductance obtained for varying values of the above parameters with and without filamentisation.

  From the test structures fabricated, we see that the values of the dimensional parameters are in the following range:

  $D \approx 25mm; W \approx 0.5mm; T \approx 50\mu m; L \approx 5mm \rightarrow 42.5mm$

  We thus take L as the independent variable and filamentise each segment into $N_k = N_m = 125$ filaments widthwise. We construct a table of the inductance values and error percentages between the two sets of values as shown in Table 3.1 where L is the length of the two segments whose mutual inductance is being calculated, M_F is the partial mutual inductance with filamentisation, M_S is the partial mutual inductance

without filamentisation (or inductance considering the segments as filaments) and the percentage error is calculated from the fractional difference relative to M_S.

Table 3.1: Inductance values with & without Filamentisation(Test Dimensions)

Length of Segments, L (m)	M_F (Henry)	M_S(Henry)	% Error = $\frac{M_F - M_S}{M_S} \times 100$
5.00e-03	9.773483554e-11	9.772867025e-11	0.006309
7.50e-03	2.190513729e-10	2.190378113e-10	0.006191
1.00e-02	3.873717064e-10	3.873483106e-10	0.006040
1.25e-02	6.013109862e-10	6.012757284e-10	0.005864
1.50e-02	8.592556673e-10	8.592069311e-10	0.005672
1.75e-02	1.159447471e-09	1.159384016e-09	0.005473
2.00e-02	1.500056604e-09	1.499977510e-09	0.005273
2.25e-02	1.879240333e-09	1.879144939e-09	0.005076
2.50e-02	2.295186433e-09	2.295074280e-09	0.004887
2.75e-02	2.746143109e-09	2.746013892e-09	0.004706
3.00e-02	3.230437900e-09	3.230291425e-09	0.004534
3.25e-02	3.746488174e-09	3.746324328e-09	0.004374
3.50e-02	4.292805569e-09	4.292624298e-09	0.004223
3.75e-02	4.867996256e-09	4.867797547e-09	0.004082
4.00e-02	5.470758484e-09	5.470542349e-09	0.003951
4.25e-02	6.099878440e-09	6.099644912e-09	0.003829

This calculation was repeated with $N_k = N_m = 500$ and no difference was observed in the error percentage, indicating that the number of filaments is sufficient. From the inductance and error percentage values, it is evident that the change in results obtained by utilizing filamentisation is minimal. Since other sources of error exist which are greater in magnitude than the error observed here, we may safely neglect this error.

- **On-Chip Inductor Dimensions:** To test the validity of our assumption for the dimensions of on-chip inductors, we repeat the previous calculations for the approximate on-chip range of values for the dimensional parameters - linewidth W, metallization thickness T, distance of separation D and length of segments L. Yet again, we consider the case of two straight equal parallel segments as shown in Fig. 3.13 and compare the values of partial mutual inductance obtained for varying values of the above parameters with and without filamentisation.

For the on-chip inductors, the values of the dimensional parameters are approximated to be in the following range:

$D \approx 25mm; W \approx 25\mu m; T \approx 0.3\mu m; L \approx 1.25mm \rightarrow 5mm$

As in the previous calculation, we take L as the independent variable and filamentise each segment into $N_k = N_m = 125$ filaments widthwise. We construct a table of the inductance values and error percentages between the two sets of values as shown in Table 3.2 where L is the length of the two segments whose mutual inductance is being calculated, M_F is the partial mutual inductance with filamentisation, M_S is the partial mutual inductance without filamentisation (or inductance considering the segments as filaments) and the percentage error is calculated from the fractional difference relative to M_S.

Table 3.2: Inductance values with & without Filamentisation(On-Chip Dimensions)

Length of Segments, L (m)	M_F (Henry)	M_S(Henry)	% Error = $\frac{M_F - M_S}{M_S} \times 100$
1.25e-03	6.242460067e-12	6.242459029e-12	0.000017
1.50e-03	8.988321464e-12	8.988319972e-12	0.000017
1.75e-03	1.223278446e-11	1.223278243e-11	0.000017
2.00e-03	1.597552711e-11	1.597552446e-11	0.000017
2.25e-03	2.021617869e-11	2.021617533e-11	0.000017
2.50e-03	2.495432006e-11	2.495431593e-11	0.000017
2.75e-03	3.018948404e-11	3.018947904e-11	0.000017
3.00e-03	3.592115576e-11	3.592114982e-11	0.000017
3.25e-03	4.214877317e-11	4.214876621e-11	0.000017
3.50e-03	4.887172751e-11	4.887171944e-11	0.000016
3.75e-03	5.608936381e-11	5.608935457e-11	0.000016
4.00e-03	6.380098150e-11	6.380097100e-11	0.000016
4.25e-03	7.200583494e-11	7.200582311e-11	0.000016
4.50e-03	8.070313412e-11	8.070312087e-11	0.000016
4.75e-03	8.989204525e-11	8.989203051e-11	0.000016
5.00e-03	9.957169150e-11	9.957167520e-11	0.000016

As before, this calculation was repeated with $N_k = N_m = 500$ and no difference was observed in the error percentage, indicating that the number of filaments is sufficient. From the inductance and error percentage values, it is evident that the change in results obtained by utilizing filamentisation is negligible and we may safely neglect

this error.

Thus, for the calculation of mutual inductances between inductors, it is observed that partitioning of the cross section of the segments into filaments is not required for the current work since the segment separation dimensions are much larger than the cross sectional dimensions for all geometries considered. Simulations comparing the partial mutual inductance values obtained with and without the partitioning of each segment into filaments prove that the differences are negligible. Thus, the segments are treated as single filaments for the purposes of mutual inductance calculations and the formulae provided by Grover [32] for various configurations of parallel filaments are used in this work.

3.5.2 Self Inductance Case

The calculation of the self inductance matrix for an inductor structure consists of two parts - finding the partial self inductances of the inductor segments (diagonal matrix elements) and then finding the partial mutual inductances between the inductor segments (off-diagonal matrix elements). We are currently concerned with the partial mutual inductance calculation. Any two segments being considered for purposes of partial mutual inductance calculation are separated by variable distances - ranging between the track separation between the neighboring segments to the largest dimension of the inductor. Since these distances are comparable to the dimensions of the segments, we must check that the error introduced by non-filamentisation is not considerable. We must also consider the fact that the self inductance of the inductor is dominated by the partial self inductances of the segments i.e. the diagonal elements. Thus, an error introduced in the off-diagonal elements may not contribute significant error to the final inductance value since the off-diagonal elements are smaller than the diagonal elements. To quantify this relative error, we consider two cases for the order of dimensions as before.

- **Test Structure Dimensions:** For purposes of this calculation, we take a range of values for the various dimensional parameters - linewidth W, metallization thickness T, distance of separation D and length of segments L - approximated over the various test structures that were fabricated. In the above approximation, we consider the worst case scenario for estimating the value of D. Since smaller values of D will lead to larger error, we take the smallest value of D expected in the test structure, which

is the track separation between inductor segments. The specific case we shall consider for our calculations is that of two straight equal parallel segments as shown in Fig. 3.13 and compare the values of partial mutual inductance obtained for varying values of the above parameters with and without filamentisation.

From the test structures fabricated, we see that the values of the dimensional parameters are in the following range:

$D \approx 1mm; W \approx 0.5mm; T \approx 50\mu m; L \approx 5mm \rightarrow 42.5mm$

Table 3.3: Inductance values with & without Filamentisation(Test Dimensions)

Length (m)	M_F (Henry)	M_S(Henry)	L_S (Henry)	% Error = $\frac{M_F - M_S}{L_S} \times 100$
5.00e-03	1.183948488e-09	1.174865821e-09	3.448131458e-09	0.263408
7.50e-03	2.252891525e-09	2.238951658e-09	5.764060076e-09	0.241841
1.00e-02	3.488056908e-09	3.469315737e-09	8.249770104e-09	0.227172
1.25e-02	4.848060571e-09	4.824542915e-09	1.086176860e-08	0.216518
1.50e-02	6.307987350e-09	6.279706165e-09	1.357442095e-08	0.208342
1.75e-02	7.851204801e-09	7.818167655e-09	1.637078323e-08	0.201806
2.00e-02	9.465824646e-09	9.428036332e-09	1.923881056e-08	0.196417
2.25e-02	1.114292725e-08	1.110039099e-08	2.216949601e-08	0.191868
2.50e-02	1.287557345e-08	1.282829151e-08	2.515584795e-08	0.187956
2.75e-02	1.465821100e-08	1.460618503e-08	2.819228067e-08	0.184540
3.00e-02	1.648629664e-08	1.642952790e-08	3.127422859e-08	0.181519
3.25e-02	1.835604399e-08	1.829453343e-08	3.439788987e-08	0.178821
3.50e-02	2.026424901e-08	2.019799739e-08	3.756004941e-08	0.176389
3.75e-02	2.220816522e-08	2.213717314e-08	4.075795262e-08	0.174180
4.00e-02	2.418541225e-08	2.410968021e-08	4.398921304e-08	0.172160
4.25e-02	2.619390722e-08	2.611343561e-08	4.725174315e-08	0.170304

We thus take L as the independent variable and filamentise each segment into $N_k = N_m = 125$ filaments widthwise. We construct a table of the inductance values and error percentages between the two sets of values as shown in Table 3.3 where L is the length of the two segments whose mutual inductance is being calculated, M_F is the partial mutual inductance with filamentisation, M_S is the partial mutual inductance without filamentisation (or inductance considering the segments as filaments), L_S is the partial self inductance of the segment, and the worst case percentage relative error is calculated from the fractional difference of M_F and M_S relative to L_S. It is

to be noted that the error is calculated relative to L_S and not relative to M_S. This is because the value of the self inductance of the inductor is dominated by the partial self inductance L_S and thus the error contributed due to filamentisation to the overall inductance should be calculated relative to this quantity.

This calculation was repeated with $N_k = N_m = 500$ and no significant difference was observed in the error percentage, indicating that the number of filaments is sufficient. Since the relative worst case error percentage values in Table 3.3 are uniformly $< 0.3\%$, the non-filamentisation of the inductor segments is justified.

- **On-Chip Dimensions:** To test the validity of our assumption for the dimensions of on-chip inductors, we repeat the previous calculations for the approximate range of values for the various on-chip dimensional parameters - linewidth W, metallization thickness T, distance of separation D and length of segments L. This data was obtained from previous on-chip inductor fabrication efforts and the estimated dimensions for our on-chip inductors. In the above approximation, we consider the worst case scenario for estimating the value of D. Since smaller values of D will lead to larger error, we take the smallest value of D expected, which is the track separation between on-chip inductor segments. The track separation is assumed to be equal to the linewidth, which is generally the case. The specific case we shall consider for our calculations is that of two straight equal parallel segments as shown in Fig. 3.13 and compare the values of partial mutual inductance obtained for varying values of the above parameters with and without filamentisation.

  For the on-chip inductors, the values of the dimensional parameters are approximated to be in the following range:

  $D \approx 25\mu m; W \approx 25\mu m; T \approx 0.3\mu m; L \approx 1.25mm \rightarrow 5mm$

  As before, we take L as the independent variable and filamentise each segment into $N_k = N_m = 125$ filaments widthwise. We construct a table of the inductance values and error percentages between the two sets of values as shown in Table 3.4 where L is the length of the two segments whose mutual inductance is being calculated, M_F is the partial mutual inductance with filamentisation, M_S is the partial mutual inductance without filamentisation (or inductance considering the segments as filaments), L_S is the partial self inductance of the segment, and the worst case percentage relative error

Table 3.4: Inductance values with & without Filamentisation(On-Chip Dimensions)

Length (m)	M_F (Henry)	M_S(Henry)	L_S (Henry)	% Error = $\frac{M_F - M_S}{L_S} \times 100$
1.25e-03	7.433963774e-10	7.379057713e-10	1.279016869e-09	0.429283
1.50e-03	9.448102987e-10	9.382200469e-10	1.589185838e-09	0.414694
1.75e-03	1.154591614e-09	1.146901913e-09	1.907726849e-09	0.403082
2.00e-03	1.371537184e-09	1.362748159e-09	2.233434957e-09	0.393521
2.25e-03	1.594747067e-09	1.584858800e-09	2.565409381e-09	0.385446
2.50e-03	1.823522548e-09	1.812535095e-09	2.902950660e-09	0.378493
2.75e-03	2.057305343e-09	2.045218749e-09	3.245500333e-09	0.372411
3.00e-03	2.295639087e-09	2.282453380e-09	3.592601435e-09	0.367024
3.25e-03	2.538143725e-09	2.523858932e-09	3.943874157e-09	0.362202
3.50e-03	2.784497843e-09	2.769113982e-09	4.298996876e-09	0.357848
3.75e-03	3.034426051e-09	3.017943138e-09	4.657694339e-09	0.353886
4.00e-03	3.287689757e-09	3.270107803e-09	5.019726780e-09	0.350257
4.25e-03	3.544080244e-09	3.525399260e-09	5.384886855e-09	0.346915
4.50e-03	3.803413394e-09	3.783633388e-09	5.752989572e-09	0.343821
4.75e-03	4.065525573e-09	4.044646553e-09	6.123871177e-09	0.340945
5.00e-03	4.330270395e-09	4.308292367e-09	6.497386729e-09	0.338260

is calculated from the fractional difference of M_F and M_S relative to L_S.

This calculation was repeated with $N_k = N_m = 500$ and no significant difference was observed in the error percentage, indicating that the number of filaments is sufficient. Since the relative worst case error percentage values in Table 3.3 are uniformly $< 0.5\%$, the non-filamentisation of the inductor segments is justified.

Therefore, for the calculation of self inductances of inductors, it is observed that partitioning of the cross section of the segments into filaments is not required for the current work. Simulations comparing the partial mutual inductance values obtained with and without the partitioning of each segment into filaments prove that the relative error is negligible. Thus, the segments are treated as single filaments for the purposes of self inductance calculations and the formulae provided by Grover [32] for various configurations of parallel filaments are used in this work.

Chapter 4

Inductor Fabrication and Measurements

The computational method developed on the basis of the partial inductance method calculates the self and mutual inductances of several simple and complex inductor geometries. It is possible to validate the results for some structures by using analytical formulae from the literature or numerical methods to calculate the inductance of the structures. This is a good source of verification for the results of the simpler structures, eg. square loops. However, for more complex structures, accurate and reliable analytical formulae do not exist. Most of the formulae found in literature are approximate and empirical in nature and do not provide very accurate results. Numerical methods are not able to handle complex structures or take inordinate amounts of computational time. This indicates that we need to have an independent and reliable source for cross-checking the inductance values generated by the computational method. An obvious solution is to fabricate the inductor geometries being simulated and measure the self and mutual inductance values. Though there are various issues involved in the fabrication and measurements, this seems to be the most suitable approach in order to obtain reliable validation of the predicted inductance values. If the computational results are in good agreement with the measurement results, the validity of the computational method will be established and it may be used to confidently predict the

inductance values of various structures with reasonable accuracy and speed.

4.1 Inductor Fabrication

While the actual dimensions of the secondary on-chip inductor would be determined by the precise function of the biomedical implant and its position in the human body, we make the conservative assumption that most implants would be able to accommodate approximately a 5 mm $\times$ 5 mm inductor with a possible height of a few hundred microns.

Test structures were fabricated using PCB prototype machines on dielectric laminate boards and by other methods. The test structures fabricated using PCB technology were scaled up in size and were around 15mm on the side and higher. Since the partial inductance method is a scalable method of computing inductances, a close match of predicted and measured results at these dimensions validates the method for the actual inductor dimensions of interest as well. The scalability of this method is borne out by the fact that the partial inductance method is used at very small dimensions, eg. for calculating the inductance matrix of on-chip and off-chip interconnects [23]. The test inductors were fabricated with copper on a laminate with high dielectric constant, using the LPKF Protomat PCB Prototyping system (also called the milling machine) which was interfaced with Agilent ADS, LPKF CircuitCam and BoardMaster.

The first step in the fabrication process was to design the layout of the inductor geometry by hand with the appropriate dimensions. While deciding the dimensions of the inductor, the fabrication restrictions and measurement apparatus had to be taken into consideration. For instance, since the inductors were to be measured using the HP8510 Network Analyzer, they would have to be connected to the cables of the HP8510 using an SMA connector. The SMA connector's connection holes are 6 mm apart and this translates into a dimensional constraint for the leads of the inductor. Further, for a spiral inductor, the track separation had a lower bound decided by the pitch of the milling machine's drill bit. Once a hand layout had been completed, the layout design was entered into Agilent ADS, which allowed the required layout to be made on several layers, - vias, metal, dielectric etc. Once this design entry was completed, the layout was converted into the Gerber file format and output to the LPKF CircuitCam. The Gerber data which was input to LPKF

CircuitCam was isolated ready for milling. Isolation is the process of computing the tool paths to remove copper as the negative of the Gerber data. Data from the PCB design software was imported into CircuitCam, modified, isolated and finally output to the LPKF BoardMaster graphical machine control program. BoardMaster offers a user friendly system for controlling the LPKF circuit board plotters. The graphical user interface displays the cutting data generated by CircuitCam. The WYSIWYG (what you see is what you get) display of the cutting data and material size enabled easy placement of different boards to be processed. The data for drilling, milling and routing a board was contained in one file with tool assignments. The machine then drilled the holes and milled the tracks on the laminate board. The milled board was removed from the Milling Machine and the excess Copper was peeled away from its surface. The board was cut to the size of the inductor geometry. Finally, the SMA connector was soldered onto the board to form the contacts required for the measurement setup. This was the summary of the technology and process flow for the fabrication of most of the inductor geometries made in the course of this project.

Since the above method allows only the fabrication of planar inductors, the 3-D test structures were constructed by hand. This involved the construction of test structures using coils of copper wire. To construct a a rectangular helical inductor, the process involved the use of regular insulated solid copper wire wound around a core of rectangular cross section to form a rigid inductor in the shape of a helix. Leads were extended from the inductor geometry in order to facilitate measurements. Similarly, a pyramidal inductor was formed by wrapping turns of thin wire around a non-conducting pyramidal base, which was especially fabricated and machined for this purpose.

4.2 Inductor Measurement

The fabricated inductors were measured with the Hewlett-Packard HP8510 Network Analyzer. The S-parameters of the structure were measured by the Network Analyzer and the inductances of the inductor geometries were extracted from the S-parameters. It is to be noted that measurement associated errors are inevitable, but there is no definite way of identifying and quantifying these errors for our structures. Thus, the measurement error is lumped with the prediction error and error plots presented in a subsequent section include the composite error from all possible sources.

In order to measure the self inductance on an inductor, it was connected to the Network Analyzer cables using the SMA connector which had been soldered onto the board. Next, a frequency sweep was performed from 50 MHz to 2 GHz and the S parameters of the 1 port network were measured by the Network Analyzer. The data gathered by the Network Analyzer could be seen in the form of a Smith Chart on the display on the instrument. This would give a fair idea of whether the structure was behaving inductive at the frequencies of interest.

For mutual inductance measurements, the two inductors of interest were connected to separate ports of the HP8510. To ensure that the two inductors were positioned correctly relative to each other, they were mounted on a non-conductive strip which passed through the central axis of each inductor and held the inductors together in a stable configuration a certain distance apart.

The S parameter data measured by the HP8510 for either setup was transferred to a computer and was analyzed using MATLAB to find out the inductance values from the S parameter measurements. The following relationships easily extract the Inductance from the Real and Imaginary parts of the S parameters which is the data provided by the Network Analyzer.

For self inductance calculations,

$$S_{11} = Re(S_{11}) + i * Img(S_{11}) \tag{4.2.1}$$

which calculates the complex S11 parameter from the measurement data,

$$Z = 50 \left(\frac{1 + S_{11}}{1 - S_{11}} \right) \Omega \tag{4.2.2}$$

which calculates impedance of the inductor structure, where 50 Ω is the impedance of the connecting cables of the Network Analyzer,

$$X = Img(Z) \tag{4.2.3}$$

which extracts the reactance as the imaginary part of the impedance, and finally,

$$L = \left(\frac{X}{2\pi f} \right) Henry \tag{4.2.4}$$

which gives the value of the Inductance L from the frequency f and reactance X.

Thus, in four simple steps, the self inductance of the fabricated inductor can be extracted from the data provided by the Network Analyzer measurements. This procedure was followed for each fabricated device: measuring its S parameters using the Network Analyzer, analyzing the data using MATLAB and finding out the inductance values using the given relations. The result was a set of inductance values for each frequency point of the frequency sweep, which could be plotted against frequency.

For mutual inductance calculations,

$$S_{ij} = Re(S_{ij}) + i * Img(S_{ij}) \tag{4.2.5}$$

which calculates the complex S_{ij} parameter of the 2-port network from the measurement data, where $i = 1, 2$ and $j = 1, 2$ to form the four S_{ij} parameters.

$$Z_{12} = 50 \left(\frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right) \Omega \tag{4.2.6}$$

$$Z_{21} = 50 \left(\frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{21}S_{12}} \right) \Omega \tag{4.2.7}$$

which calculate the impedance matrix values of the mutual inductor configuration, where 50 Ω is the impedance of the connecting cables of the Network Analyzer,

$$X_{12} = Img(Z_{12}) \tag{4.2.8}$$

$$X_{21} = Img(Z_{21}) \tag{4.2.9}$$

which extract the elements of the reactance matrix as the imaginary parts of the impedance matrix elements, and finally,

$$M_{12} = \left(\frac{X_{12}}{2\pi f} \right) Henry \tag{4.2.10}$$

$$M_{21} = \left(\frac{X_{21}}{2\pi f} \right) Henry \tag{4.2.11}$$

which give the values of the mutual inductance M_{12} and M_{21} from the frequency f and reactance X. Ideally, $M_{12} = M_{21}$, but due to inevitable measurement errors, the mutual inductance values differ minutely over the entire measurement range and $M_{12} \simeq M_{21}$.

The mutual inductance of the fabricated inductor can thus be extracted from the data provided by the Network Analyzer measurements. This procedure was followed for each

fabricated device: measuring its S parameters using the Network Analyzer, analyzing the data using MATLAB and finding out the mutual inductance values using the given relations. The result was a set of mutual inductance values for each frequency point of the frequency sweep, which could be plotted against frequency.

The partial inductance method calculates a frequency-independent value of the inductance. Therefore, though the measured results are frequency dependent, the low frequency range of values of the measured results are generally taken as the accurate measurement range for comparison.

Another instrument used to measure inductance values was a simple RLC meter, which gives the Inductance values of any device when its leads are shorted to the input terminals of the RLC meter. However, a drawback with this method was that additional leads were required to be attached to the inductor, and these leads had to be simulated separately, after the fabrication was complete. In practice, the device was fabricated, an SMA was attached and the Network Analyzer readings were taken. After this, the SMA was removed and solder leads were attached to the ends of the inductor. These leads were measured for purposes of entering their dimensions into the computer simulation. Then, the device was measured using the RLC meter. Thus, this alternate measurement scheme provided another independent source of validation for the inductance values of the fabricated geometries.

These two methods of measurement and the Thin-Strut Formalism method [34], an extension of the numerical FDTD method, were the three sources of comparison used for validation of the predicted inductance values.

Chapter 5

Analysis of Inductor Geometries and Results

The purpose of this work is to examine inductor geometries which may be fabricated on-chip and find the best option based on calculations of mutual coupling with the external coil. However, in order that these coupling calculations may be considered reliable, we need to first validate the results obtained for simpler structures via measurements or known calculation methods. If the computational results are in good agreement with the measurement results, the validity of the computational method will be established and it may be used to confidently predict the inductance values of various structures with reasonable accuracy and speed. A number of test structures were analyzed to test the validity of the inductance prediction code.

5.1 Test Structures and Results

5.1.1 Self Inductance

- **Square Loop:**

  A 10 mm square loop was fabricated on a PCB substrate as shown in Fig. 5.1 and the

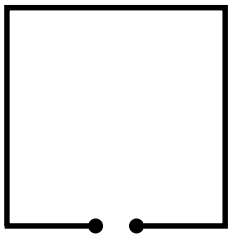


Figure 5.1: Square Loop

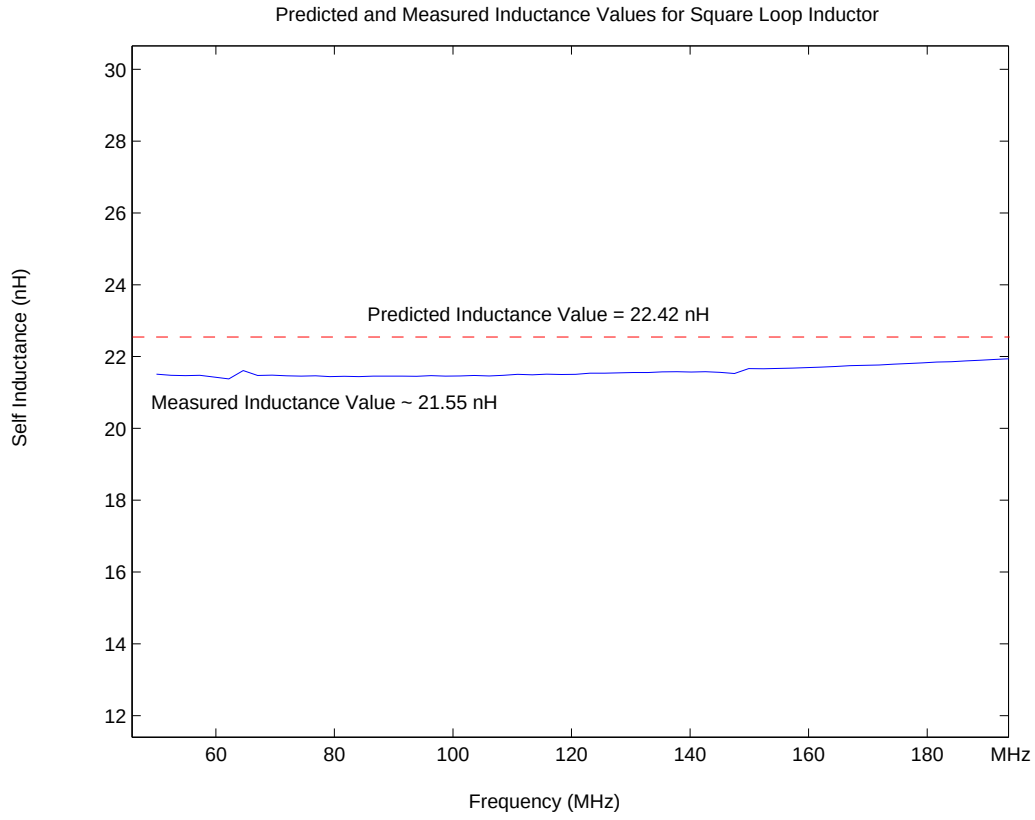


Figure 5.2: Predicted and Measured Results Plot for Square Loop

measurement results were compared with the predicted results (Fig. 5.2). Measurements were performed by connecting the square loop via an SMA connector located directly underneath the loop to a Network Analyzer. We observe that the predicted value for the self inductance of the loop matches the experimental values closely for low frequencies. It is to be noted that the comparison between predicted and observed values should indeed be performed in the low frequency range since the code predicts the low frequency inductance of a structure.

- **Square Loop with Leads:**

  Since the SMA connector lies directly beneath the square loop in the previous structure, there is the possibility that the inductance measurements are affected by it. This issue can be circumvented by fabricating a 10 mm square loop with long leads which then connect to the SMA connector. The SMA connector would not be under the square loop anymore, minimizing the effect it might have on the structure. The square loop is fabricated as shown in Fig. 5.3 and the measurement results are shown in Fig. 5.4. We observe that the inductance values are greater as expected, due to the extra length of the leads. Once again, there is a reasonably good match between the predicted and measured results.

- **Spiral Inductor:**

  A spiral inductor with 4 turns and an outer side length of 15 mm is fabricated on a PCB substrate with leads attached for measurement purposes as shown in Fig. 5.5. In Fig. 5.6, the comparison results for the spiral inductor suggest that the computational method predicts the inductance of relatively complicated inductor geometries with good accuracy. The good match between the expected value and measurement results for 2-D structures encourages us to extend the method to predict the inductances of 3-D structures.

- **Rectangular Helical Inductor:**

  To test the validity of the results predicted by the method for 3-D structures, a rectangular helical inductor 45 mm $\times$30 mm was constructed using several turns of electrical wire wrapped around a non-conducting core as shown in Fig. 5.7. The measurement method in this instance utilized a simple RLC meter since the Network Analyzer could not be used due to the larger size and radius of the inductor leads.

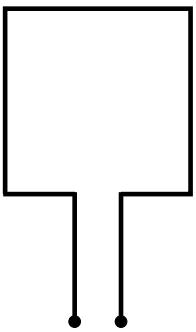


Figure 5.3: Square Loop with Leads

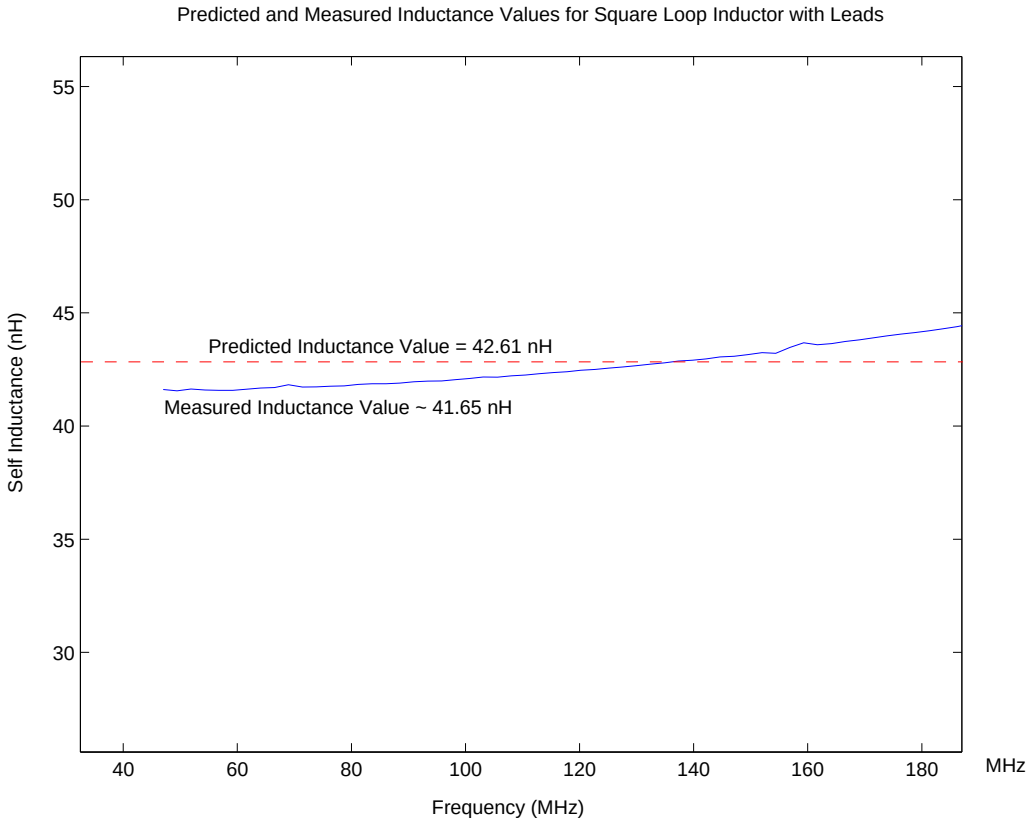


Figure 5.4: Predicted and Measured Results Plot for Square Loop with Leads

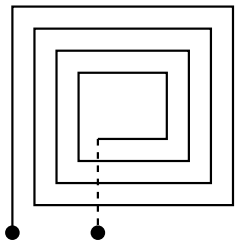


Figure 5.5: Spiral Inductor

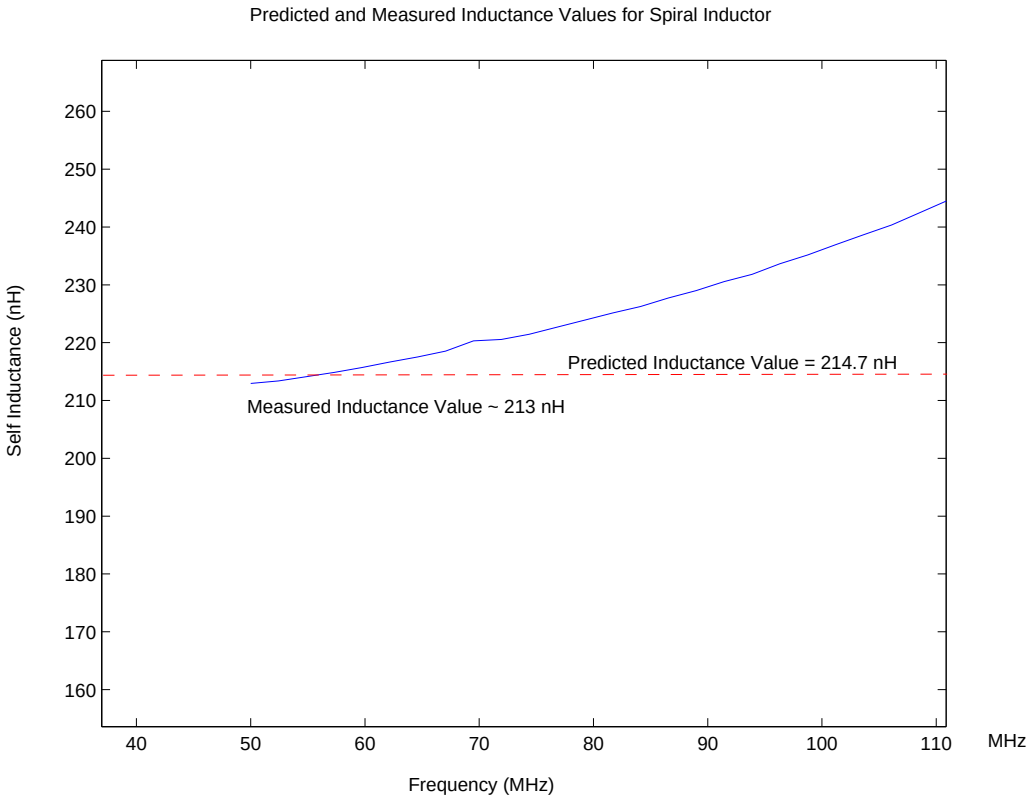


Figure 5.6: Predicted and Measured Results Plot for Spiral Inductor

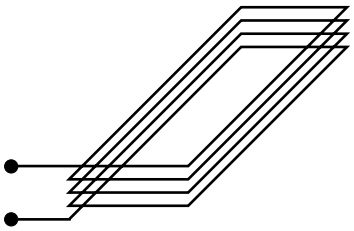


Figure 5.7: Rectangular Helical Inductor

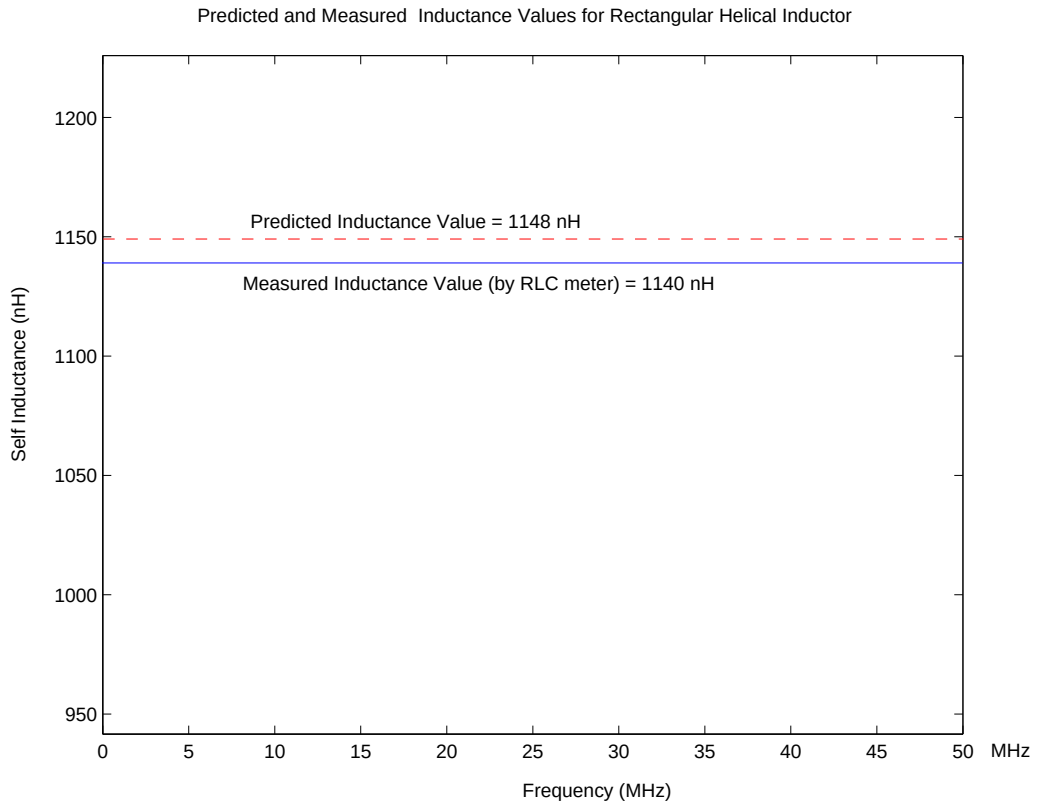


Figure 5.8: Predicted and Measured Results Plot for Rectangular Helical Inductor

As we see in Fig. 5.8, the results shown prove that a good match is obtained for the helical inductor.

- **Pyramidal Inductor:**

  Finally, a 3-D pyramidal inductor (50 mm ×50 mm base dimensions) is constructed on a non-conducting pyramidal base as shown in Fig. 5.9 and Fig. 5.10, and the results are plotted in Fig. 5.11. Two predicted results are obtained depending on slightly differing definition of the segment heights. The good match between the results for this pyramidal structure and for all previous structures validates the prediction of self inductances with a high degree of accuracy. This is also a big step toward the prediction of mutual inductance for coupled coils since the partial inductance concept uses the same basic principle for the calculation of self and mutual inductances of various structures.

Figure 5.9: Side View of Pyramidal Inductor

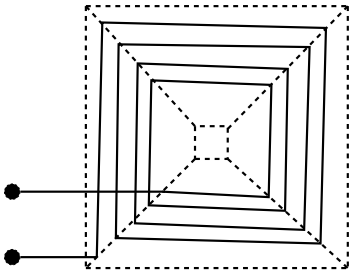


Figure 5.10: Top View of Pyramidal Inductor

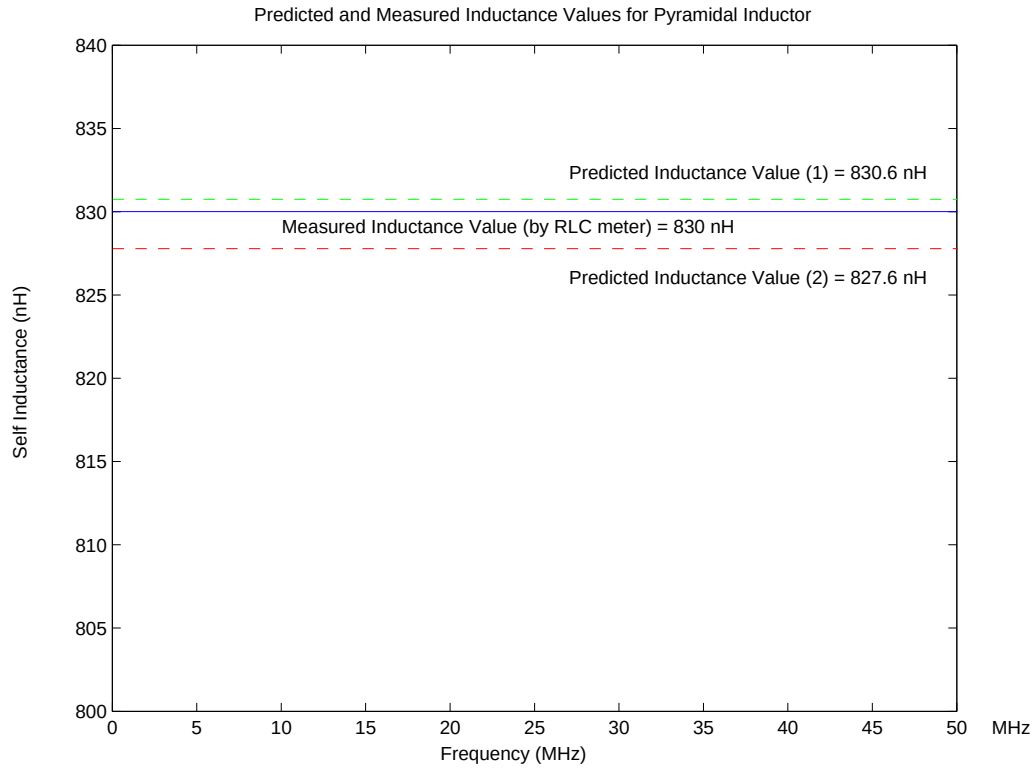


Figure 5.11: Predicted and Measured Results Plot for Pyramidal Inductor

5.1.2 Mutual Inductance

- **Coaxial Square Loops:** To test the validity of the method for simple mutual inductance calculations, we calculate the values of mutual inductance for 2 square coaxial loops (Fig. 5.12). Simulation results from the Thin-Strut Formalism (a numerical FDTD based method) [34] for an identical configuration were used for comparison purposes. The results, plotted in Fig. 5.13, show the comparison of mutual inductance to self inductance ratios when the length of one square loop is varied while holding the axial distance constant and when the axial distance between the loops is varied while holding the square lengths constant. The plots indicate a very close match in mutual inductance values obtained by two methods which employ totally different approaches.

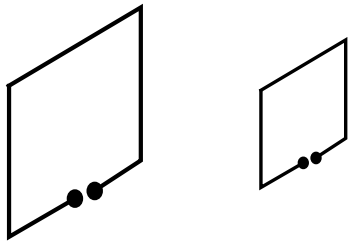
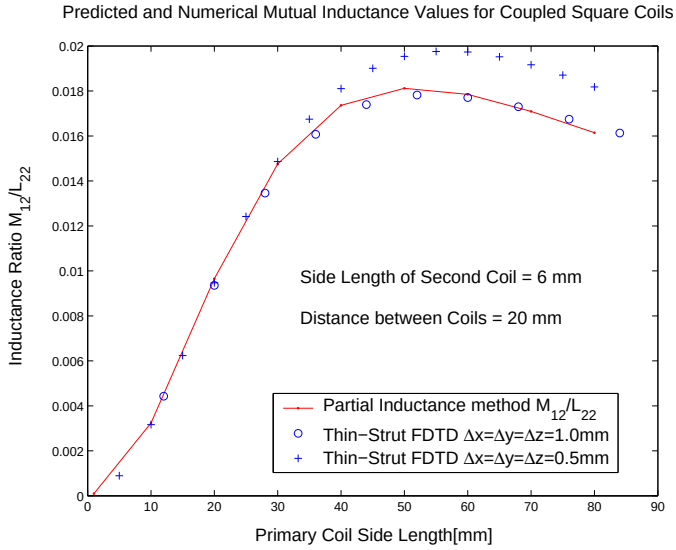
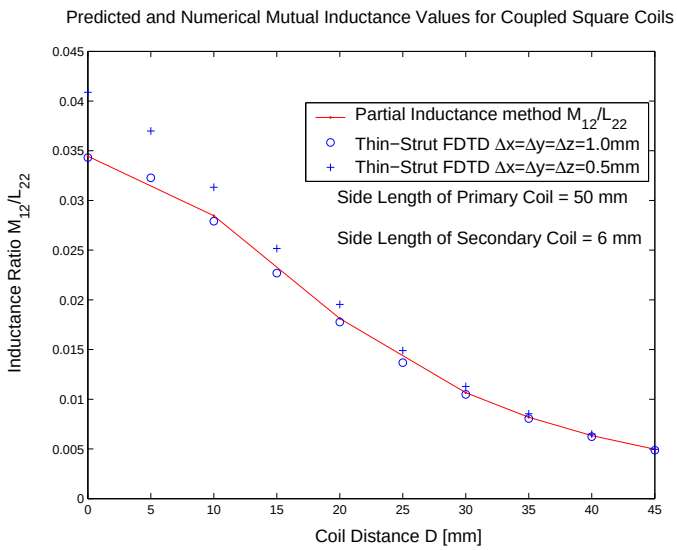


Figure 5.12: Mutual Inductance between Coaxial Square Loops



(a) D = 20 mm, L2= 6mm, L1 = 10 - 80 mm



(b) D = 0 - 45 mm, L2= 6mm, L1 = 50 mm

Figure 5.13: Predicted and Numerical Simulation Results Plot for 2 Square Loops

- **Coaxial Spiral Loops:**

  The previous result encourages us to fabricate 2 identical spiral inductors 15 mm on the outer side, arrange them in a coaxial configuration (Fig. 5.14) and compare the inductance results. The measurement results for this coupling configuration are shown in Fig. 5.15, Fig. 5.16 and Fig. 5.17 for different values of separation, D = 1.8 cm, 2.5 cm, 3.0 cm. These are the M_{12} and M_{21} values obtained from the S_{12} and S_{21} measurements respectively, which are nominally equal to each other. The results are an excellent match and show that the method predicts mutual inductances accurately

for relatively complex coupled structures. This also validates the mutual inductance method for distances of separation generally used for biomedical implants.

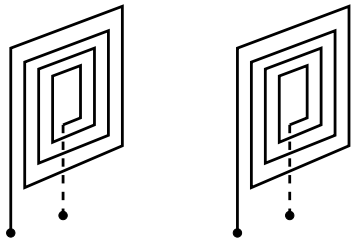


Figure 5.14: Mutual Inductance between Spiral Inductors

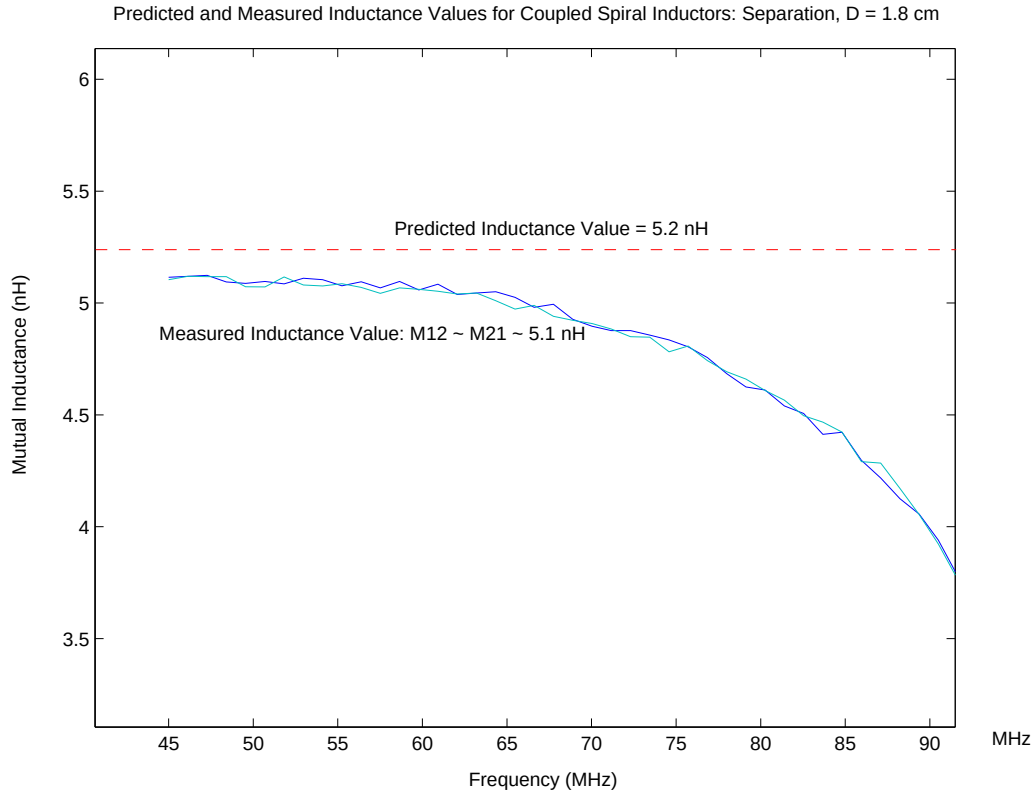


Figure 5.15: Predicted and Measured Results Plot for 2 Spiral Inductors, D=1.8 cm

- **Pyramidal Inductor and Square Loop:**

  Finally, we construct the inductor coupling structure intended to couple the power to

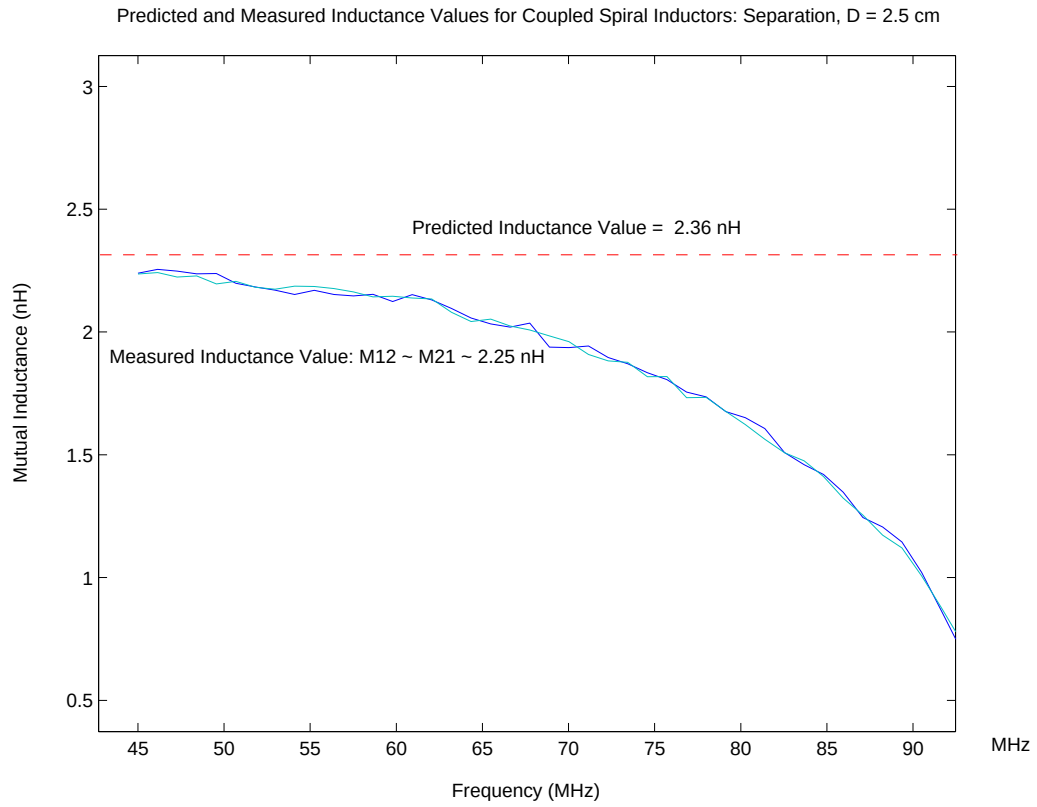


Figure 5.16: Predicted and Measured Results Plot for 2 Spiral Inductors, D=2.5 cm

the biomedical implant. A 3-D pyramidal inductor (50 mm $\times$50 mm base dimensions) is placed coaxially with a large 145 mm $\times$115 mm square loop (Fig. 5.18). The reason a large loop is used is because it is intended to represent the external inductor which typically has a high inductance value. Further, since the dimensional constraints on the external inductor are not strict, a relatively large inductor may be built for good coupling. The axial distance of separation between the inductors is $D \approx 45$ mm and their coupling is measured and compared to the predicted results in Fig. 5.19. Yet again, the low frequency values of the measured results are to be compared with the predicted inductance value from the code. In this plot, we observe that the match between the measured and predicted value is relatively close. In conjunction with all the previous results, this result for the coupling between a 3-D inductor and a rectangular loop indicates that this method can be used to predict the self and mutual inductances of various regular 2-D and 3-D structures with a high degree of acuracy.

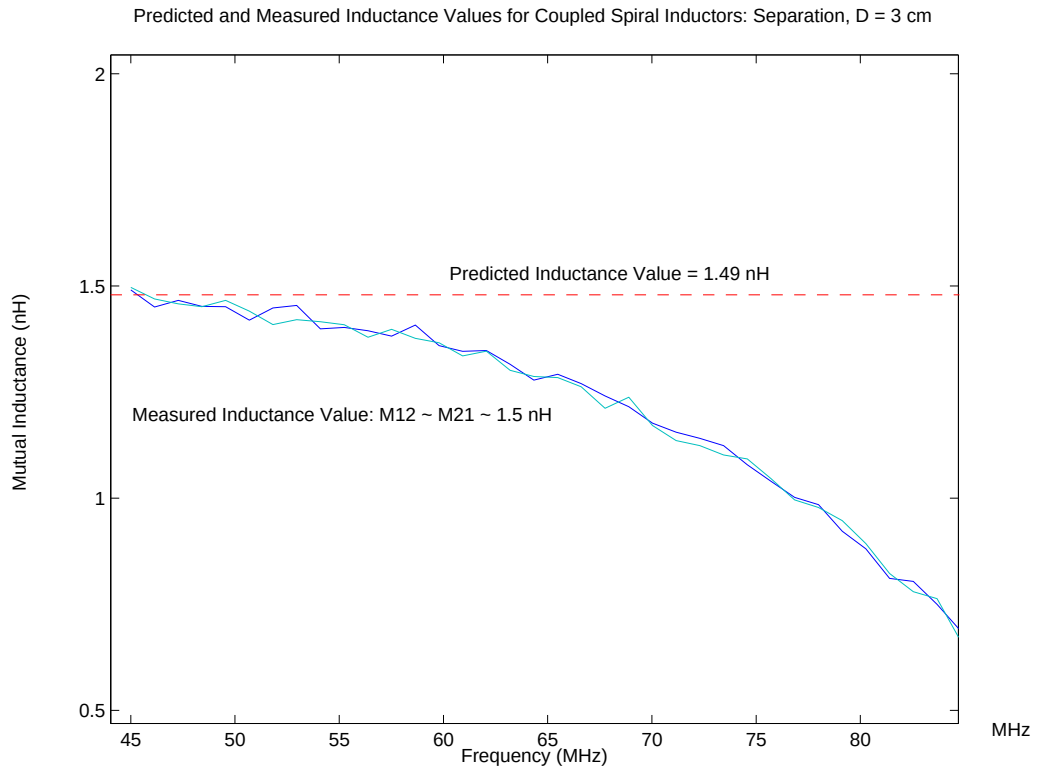


Figure 5.17: Predicted and Measured Results Plot for 2 Spiral Inductors, D=3.0cm

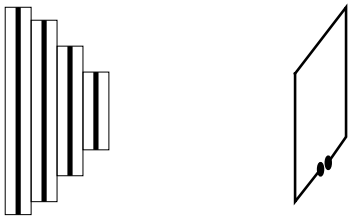


Figure 5.18: Mutual Inductance between Pyramidal Inductor and Square Loop

In this section, we have seen plots comparing the predicted inductance values with the measured or numerically simulated inductance values for both the self inductance and mutual inductance cases. The results indicate a good match for the structures and thus validate the computational method for the purposes of predicting inductance values of different inductor geometries. These inductance predictions can be used for deciding the optimal inductor geometry for coupling power to biomedical implants.

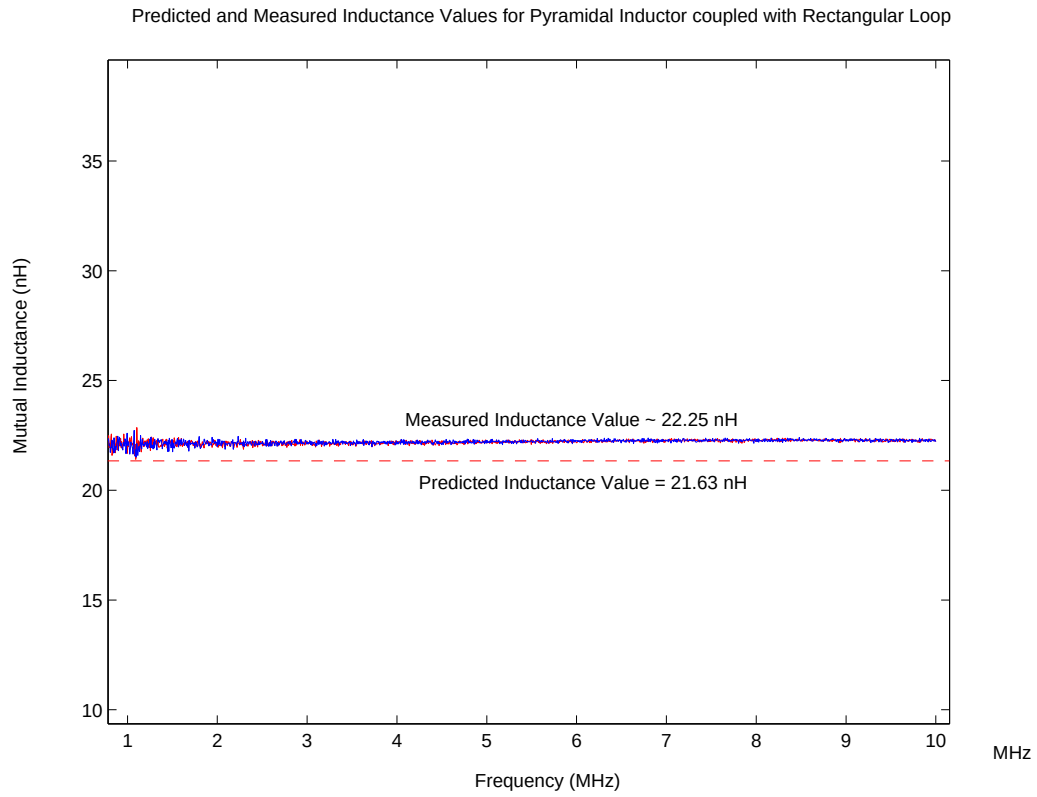


Figure 5.19: Predicted and Measured Results Plot for Pyramidal Inductor and Square Loop

5.2 Error Analysis

The comparison of the predicted and measured/numerical results for the test structures indicate that the validity of the computational method has been firmly established. However, an idea of the error involved in prediction is required before using the method for inductance prediction. To get a quantitative estimate of the approximate error involved in the prediction of inductances, we plot the error percentages for the various self and mutual inductance structures. These error percentages essentially quantify the fractional difference in predicted and measured/numerical inductance values as a percentage of the measured/numerical value. In cases where there is more than one predicted value from different methods, or in cases where the comparison is performed over a range of different values of the independent variable, the average value of error is considered. It is to be noted that since the measured/numerical values have an error associated with them as well, the error we plot is the combined error associated with the predicted and the measured/numerical

values.

$$\text{Error Percentage} = \frac{\text{Predicted Value} - \text{Measured or Numerical Value}}{\text{Measured or Numerical Value}} \times 100 \qquad (5.2.1)$$

For the case of self inductance values, the error percentage graph is shown in Fig. 5.20 for the different test structures.

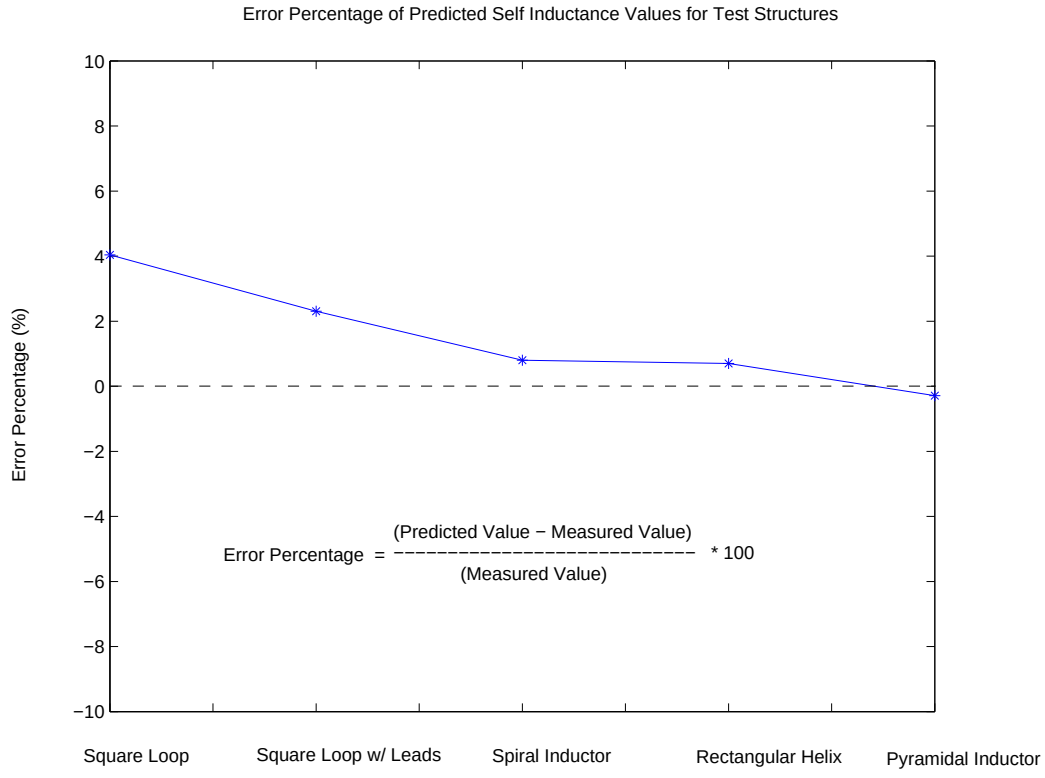


Figure 5.20: Error Percentages for Predicted Self Inductance Values

From the error percentages plotted in Fig. 5.20, we see that the self inductances are calculated by our method with a small relative error within ±4%, thereby verifying the method for self inductance calculations.

Next, we plot the error percentages for the mutual inductance values of the various configurations in Fig. 5.21. All the error percentages are well within ±6% and so we are justified in stating that the method predicts the mutual inductance coupling with reasonable accuracy for various geometrical structures.

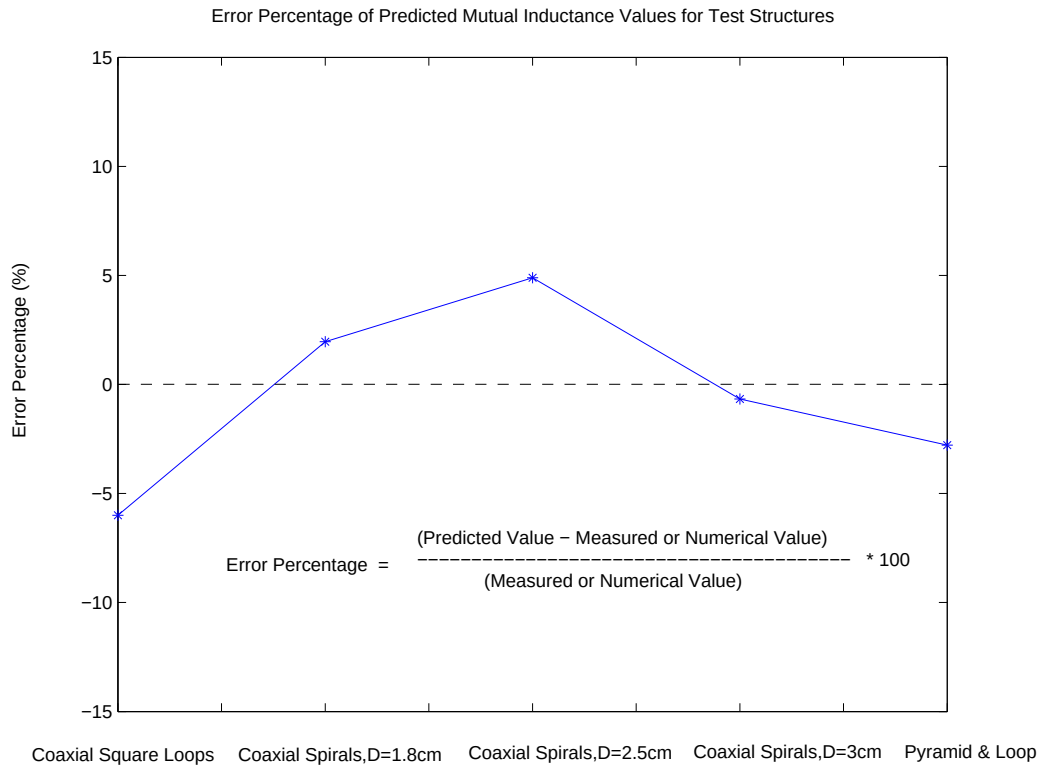


Figure 5.21: Error Percentages for Predicted Mutual Inductance Values

5.3 Optimal Geometry Analysis

The main object of this thesis so far has been to develop a computational method which can accurately and quickly predict the self and mutual inductance of various inductor geometries and configurations. The method has been validated by comparison with measurement results for certain fabricated test structures. The results indicate that the computational method predicts the self and mutual inductance values with a good degree of accuracy for the structures of our interest. This computational method is now applied to the problem of choosing an optimal inductor geometry for power coupling to the implant. The coupling coefficient k, defined by:

$$k = \frac{M}{\sqrt{(L_1 L_2)}} \tag{5.3.1}$$

is the standard measure of coupling between coils. This quantity is used to compare and choose between the coil geometries.

We analyze three different variations of the same basic inductor geometry - the pyramidal inductor - as shown in Figs. 5.22, 5.23 and 5.24. Figs. 5.23 and 5.24 show single and double recessed pyramids with one and two recessed plateaus in their geometries respectively. These plateaus may contain a variable number of turns which leads to different values of the coupling coefficient. For each of these three geometries, we vary two parameters - the number of turns on the plateaus and track separation between segments, both of which are typically within our control as designers, and observe the change in coupling predicted by our method. To make a fair comparison possible, we ensure that the following parameters are kept the same for a given comparison - total height of the entire structure, base length and width, and total number of tracks on inclined surfaces. The external inductor coupled with these inductor geometries is a simple rectangular loop inductor, giving rise to the configuration shown in Fig. 5.25.

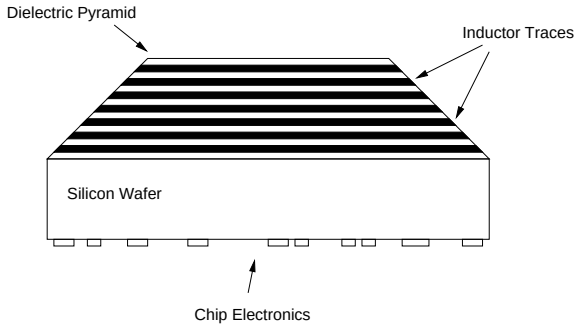


Figure 5.22: Basic Pyramidal Inductor Geometry

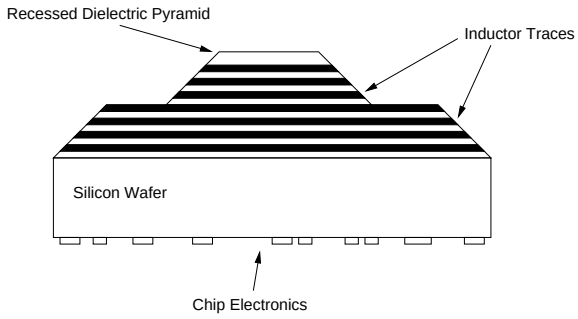


Figure 5.23: Recessed Pyramidal Inductor Geometry

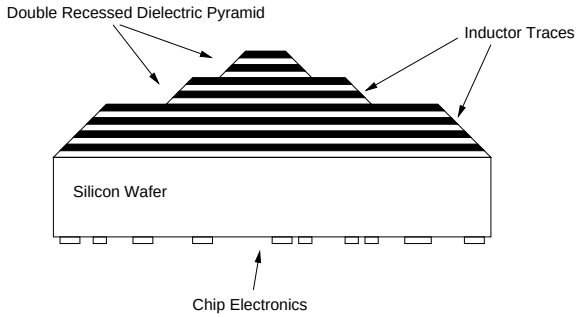


Figure 5.24: Double Recessed Pyramidal Inductor Geometry

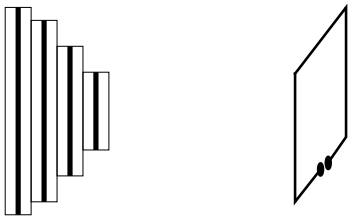


Figure 5.25: Mutual Inductance between Pyramidal Inductor and Square Loop

5.3.1 Varying the value of N

To observe the variation of the coupling coefficient k with respect to the first of the two variable parameters, we introduce a notation to denote the precise structure of a basic or recessed pyramidal structure for simplicity of description. For example, a $2-N-2$ pyramid is a recessed pyramid structure with a single plateau along the incline of the pyramid. The lower sloped surface has 2 turns on it, the plateau has N turns, and the upper sloped surface has 2 turns. Similarly, a $2-N-2-N-2$ pyramid is a double recessed pyramid with two plateaus along the incline of the pyramid, each of which has N turns while the three sloped surfaces all have 2 turns each. It is evident that for the case of a basic pyramid, $N = 0$. We compare the coupling coefficients of the single and double recessed pyramid with the basic pyramid by examining different pyramidal structures and varying the value of N, where the coupling coefficient for the basic pyramid is given by the y-axis value on the graph for $N = 0$. We now take a look at the variation in the coupling coefficient, normalized to the value of coupling coefficient for $N = 0$ and seek the optimal coupling configuration for a variety of situations.

- **Test Structure, $2-N-2$ Pyramid:** We first analyze the case of a single recessed pyramid for test structure dimensions. The dimensions of the pyramidal inductor and rectangular loop are approximately the same as those used in the mutual inductance calculation in Section. 5.1. The plot of the normalized coupling coefficient is shown in Fig. 5.26.

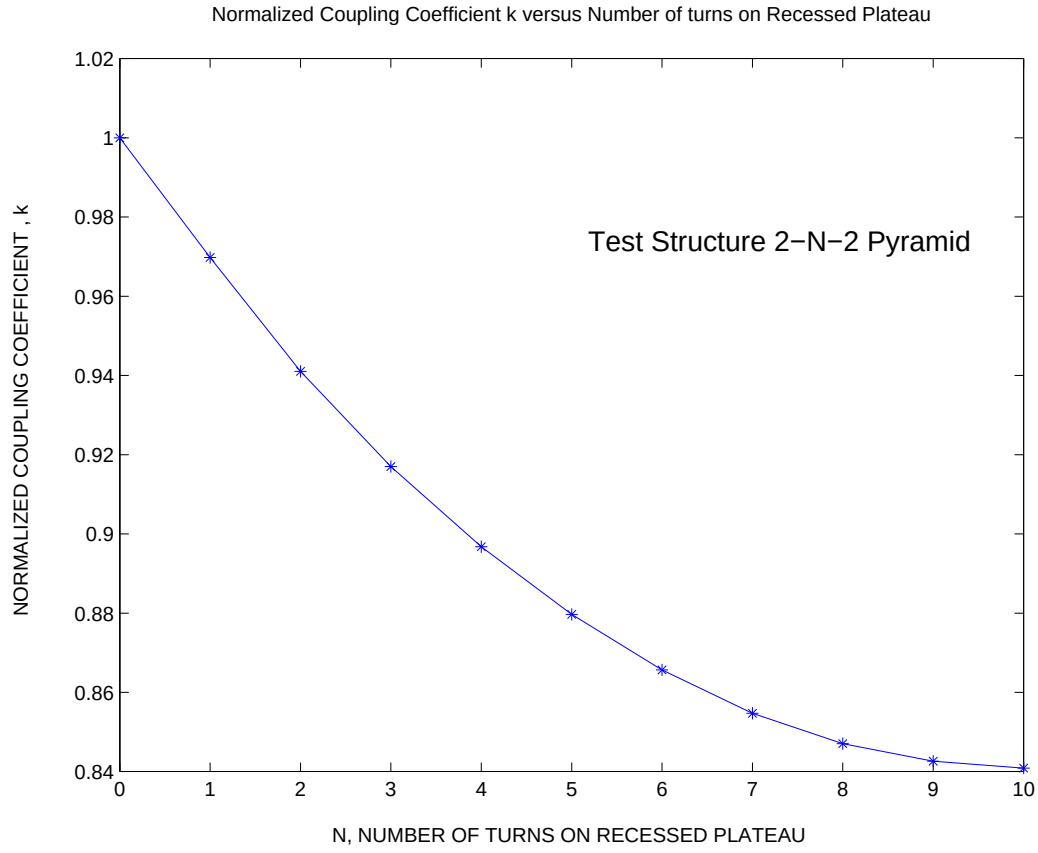


Figure 5.26: Normalized Coupling Coefficient variation with N for $2-N-2$ Pyramid

It is evident that the coupling coefficient of the Basic Pyramidal geometry is the highest and it is thus the optimal geometry to couple power to the implant. There is no advantage in building recessed pyramids for this situation. We see that our inductance calculation analysis has thus provided us with an optimal pyramidal geometry to couple with the external rectangular loop coil based on the value of the coupling coefficient k.

- **On-Chip Dimensions, $3-N-3$ Pyramid:** To get an idea of the coupling coefficient values we should obtain when we fabricate such inductor geometries on-chip, we compute and compare the coupling coefficients for the single recessed pyramidal inductor geometries with on-chip inductor dimensions, assuming a 7 mm $\times$7 mm backside chip surface area available for the pyramidal inductor (Fig. 5.27).

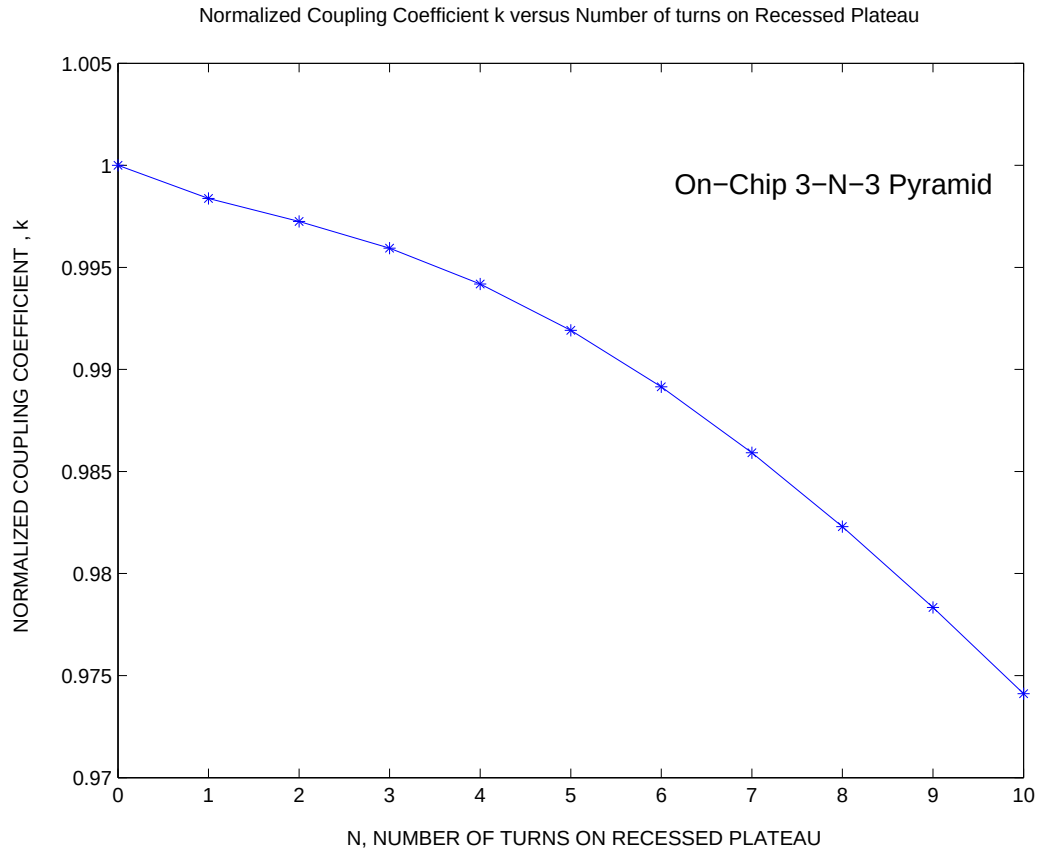


Figure 5.27: Normalized Coupling Coefficient variation with N for On-Chip $3-N-3$ Pyramid

Yet again, we observe that the coupling coefficient of the Basic Pyramidal geometry is the highest and it is thus the optimal geometry to couple power to the implant. There is no advantage in building recessed pyramids for this situation. Our inductance calculation analysis has thus provided us with an optimal on-chip pyramidal geometry to couple with the external rectangular loop coil based on the value of the coupling coefficient k.

- **On-Chip Dimensions,** $2-N-2-N-2$ **Pyramid:** We now analyze the case of a double recessed on-chip pyramidal geometry with a number of turns on each plateau, the number of turns N being the same on each plateau. As before, the $N = 0$ case represents the basic pyramidal geometry and the coupling coefficients are normalized to that value. We also note that the total height of the double recessed structure is the same as that of the comparable basic pyramid. The comparison of the normalized coupling coefficients is shown in Fig. 5.28.

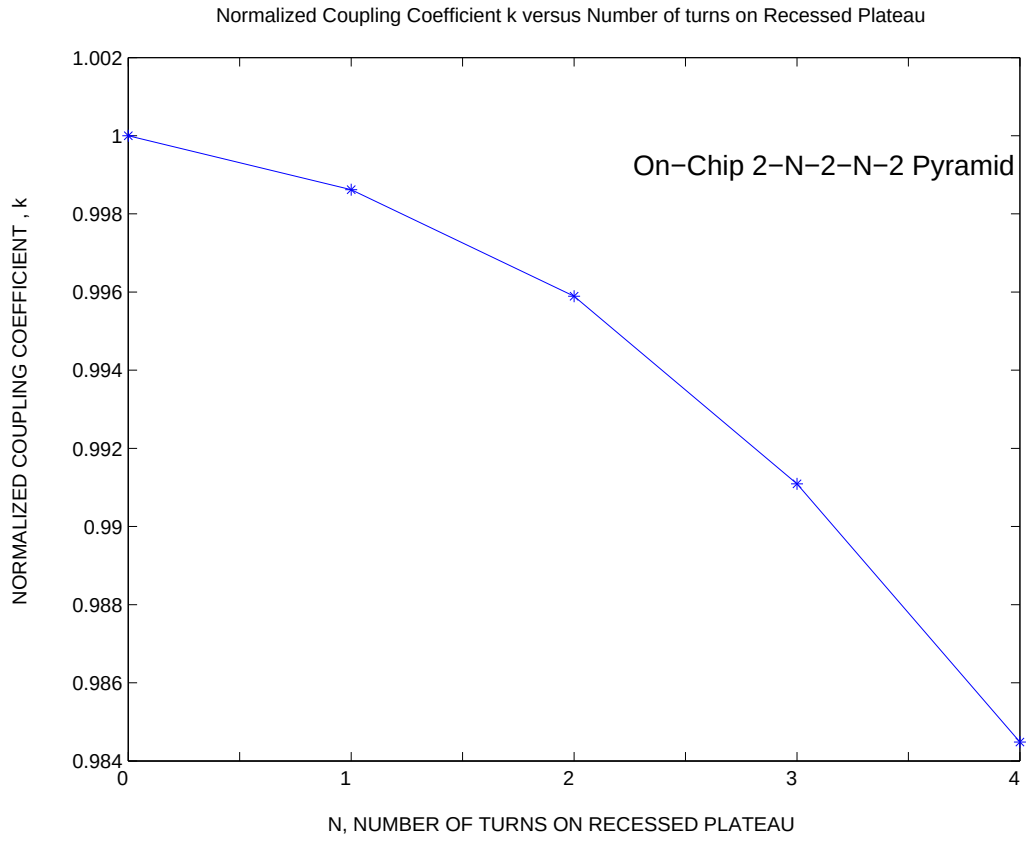


Figure 5.28: Normalized Coupling Coefficient variation with N for On-Chip $2-N-2-N-2$ Pyramid

We observe from the plot that the Basic Pyramid is the optimal geometry yet again and is advantageous as compared to the double recessed pyramidal geometry for this situation. Given the previous plots, we may be tempted to discern a trend in this dependence of coupling coefficients on N. However, that such a hypothesis would be erroneous is proven by the subsequent analysis.

- **On-Chip Dimensions, $2-N-2$ Pyramid:** We analyze the case of a single recessed on-chip pyramid with a $2-N-2$ configuration in Fig. 5.29.

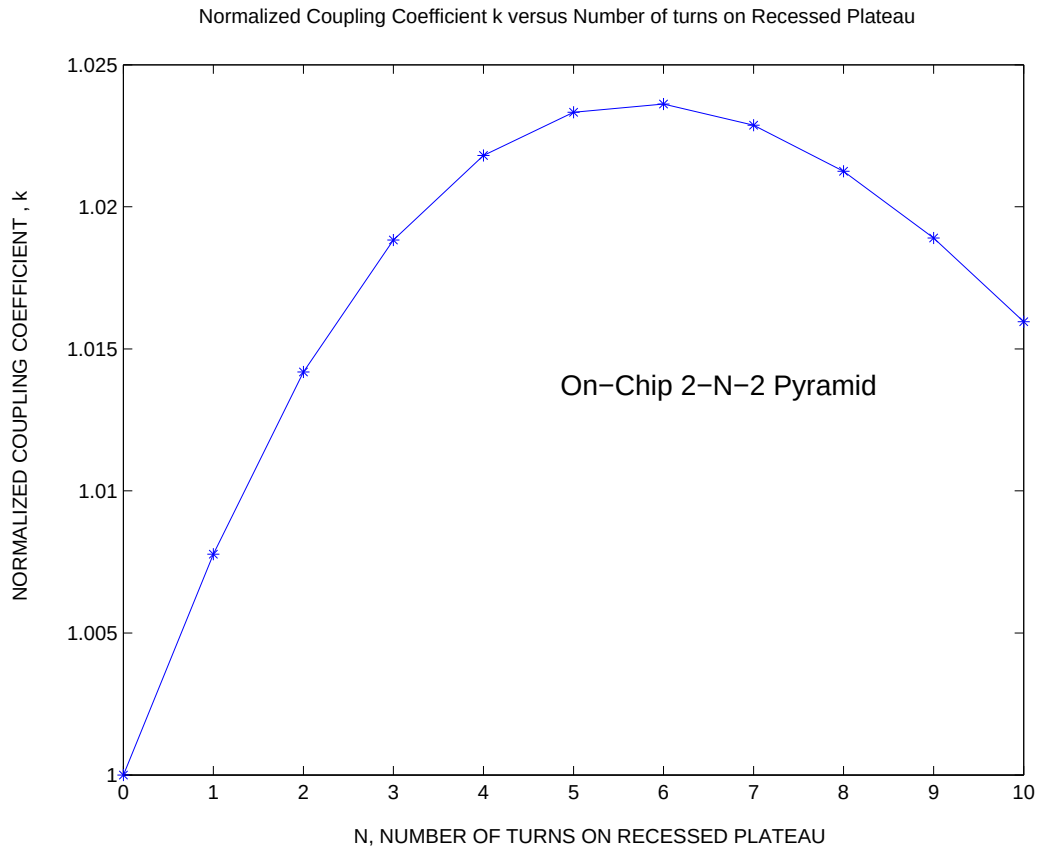


Figure 5.29: Normalized Coupling Coefficient variation with N for On-Chip $2-N-2$ Pyramid

From the figure, we observe that the maximal coupling is obtained when there are 6 turns on the plateau of the recessed pyramid. Therefore, the optimal pyramidal structure for power coupling in this situation is a $2-6-2$ recessed pyramid. Thus, we see that the actual optimal inductor structure is dependent heavily on the precise coupling situation in terms of configuration, dimensions and other factors. We may not formulate any general rules to determine the optimal inductor geometry for all situations. However, for a particular situation, it is possible to use our method to compute inductances and hence coupling coefficients, plot comparative graphs and thus determine the optimal coupling structure for the situation.

5.3.2 Varying the value of Track Separation

We wish to observe the variation of coupling coefficient k with geometric dimensions. It becomes evident that the horizontal track separation between the segments of the inductor is a dimension over which we have some degree of control. The metal linewidth and metallization thickness of the inductor traces are typically determined by available fabrication technology and other factors like electromigration etc. Electromigration considerations may act as a constraint on the lower bound on the width and thickness since these inductor traces may need to carry large currents over extended periods of time and thus need to be wide and thick enough to handle sufficient current densities. The base dimensions of the pyramid itself are constrained by the amount of on-chip space we have on the implant. The height of the pyramid is also constrained by the depth of the trench we are able to etch in the silicon wafer in a reasonable amount of time.

We must keep in mind that the coupling coefficient k is directly proportional to the mutual inductance and inversely proportional to the square root of the self inductances and is thus, in general dominated by the mutual inductance variation. So, changing some dimensions may increase the mutual inductance but may simultaneously increase self inductance of the structure by such an amount that it offsets the increase in the mutual inductance and actually reduces the coupling coefficient. Thus, it is important to observe the relative values of the coupling coefficient when changing the dimensions of the inductor geometry.

Working with the dimensional constraint that the inductor is around 400μm high, we choose a vertical turn separation z value of 100μm. This means that we may have 4 turns in the basic pyramidal inductor geometry. The linewidth chosen is 25μm and the metallization thickness is 0.5μm. The three pyramidal inductor geometries - basic, single recessed and double recessed - are assumed to be coupled with a large external rectangular loop inductor with dimensions 14 mm $\times$12mm. Since the size constraint on the external inductor is not strict, we could possibly build a larger inductor with a bigger inductance value for larger coupling. However, for demonstration purposes, we work with the current loop size. The coaxial distance of separation is 25 mm as was assumed to be the separation distance for most biomedical implants.

- **On-Chip Dimensions, Basic Pyramid, 4 Turns:** We analyze the case of a basic on-chip pyramid with 4 turns and observe how the coupling coefficient varies with changing track separation in Fig. 5.30. In this case, the track separation is varied between $50\mu m$ and $550\mu m$ and the values of the coupling coefficient are normalized to the value of the coupling coefficient for a track separation of $50\mu m$.

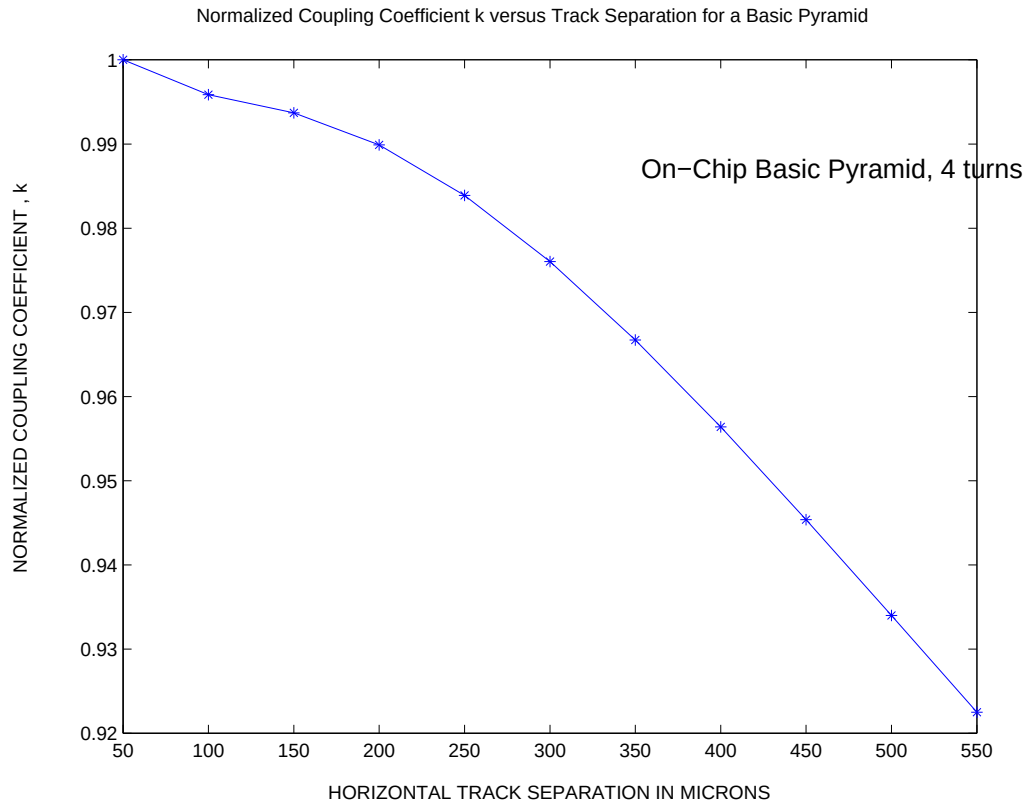


Figure 5.30: Normalized Coupling Coefficient variation with Track Separation for On-Chip Basic Pyramid

From the plot, it is evident that the coupling coefficient decreases with increasing track separation. Thus, it appears that we must try to decrease tr in order to maximize k. This may be achieved by placing the inductor segments close together. We note that our method has allowed us to optimize our inductor geometry for maximal power transfer by a comparison of relative coupling coefficients.

- **On-Chip Dimensions, 2-2-2 Pyramid:** Next, we analyze the case of a single recessed on-chip pyramid with $2-2-2$ turns. This means that there are 2 turns on the lower sloping surface, 2 turns on the plateau and 2 turns on the upper sloping surface. We wish to observe how the coupling coefficient varies with changing track separation in Fig. 5.31. Yet again, the track separation is varied between $50\mu m$ and $550\mu m$ and the values of the coupling coefficient are normalized to the value of the coupling coefficient for a track separation of $50\mu m$.

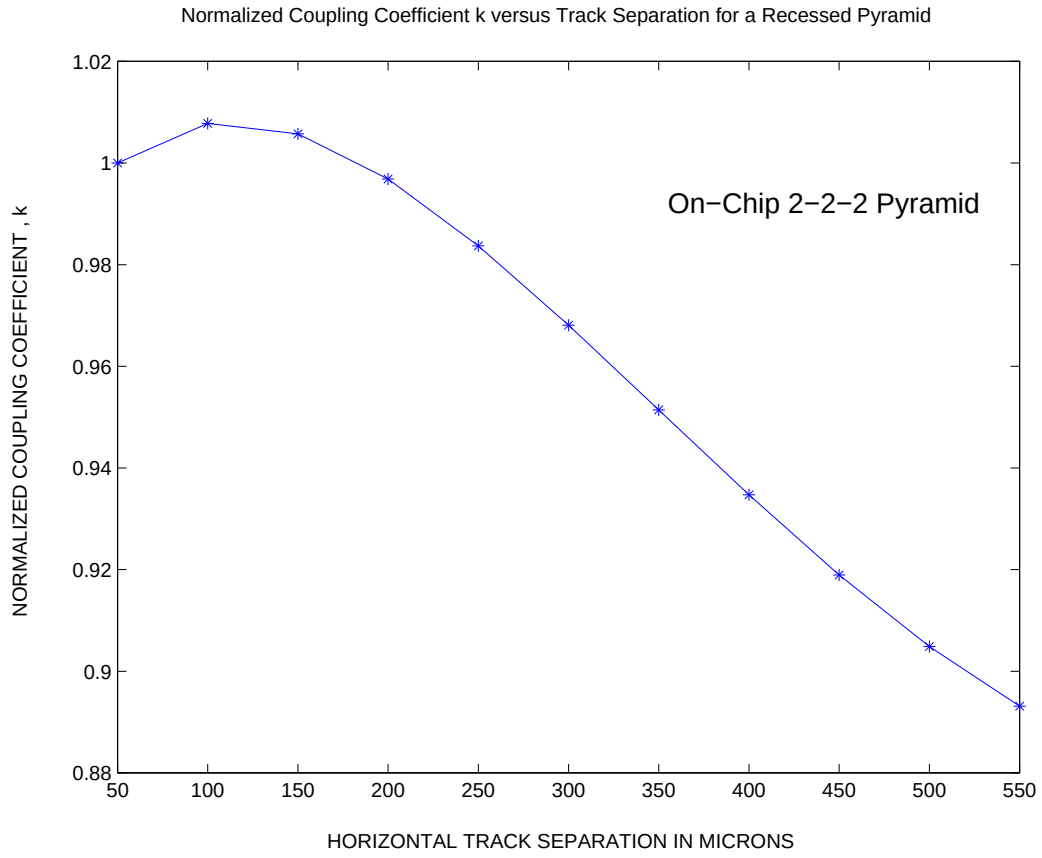


Figure 5.31: Normalized Coupling Coefficient variation with Track Separation for On-Chip $2-2-2$ Pyramid

In this case, we note that the normalized coupling coefficient actually rises to a maximum value before falling down again. The value of track separation for which the maximal k is obtained is found to be $100\mu m$. Therefore, we see that the optimal single-recessed pyramidal geometry for power coupling in this situation will have a track separation of $100\mu m$.

- **On-Chip Dimensions, 2-2-2-2 Pyramid:** Finally, we analyze the case of a double recessed on-chip pyramid with $2-2-2-2$ turns to observe how the coupling coefficient varies with changing track separation in Fig. 5.32.

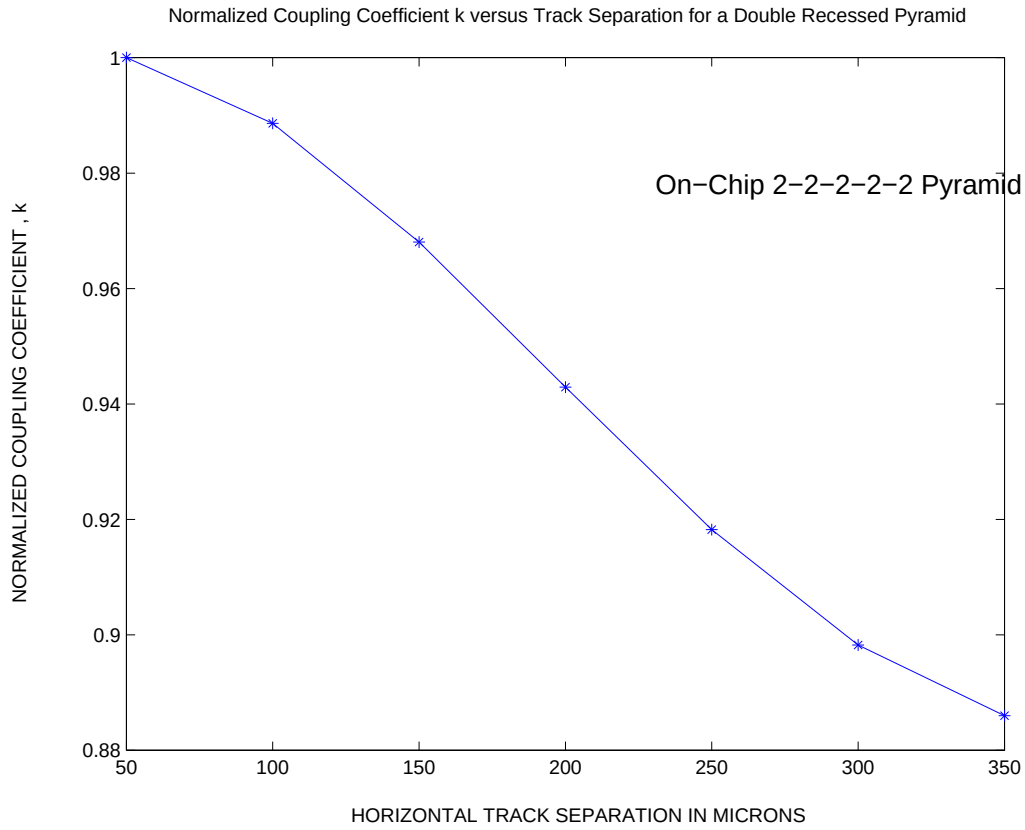


Figure 5.32: Normalized Coupling Coefficient variation with Track Separation for On-Chip $2-2-2-2-2$ Pyramid

This case is observed to be similar to the first case since the optimal case for coupling is given by the case of minimum track separation. Thus, our method has successfully optimized the track separation of the inductor geometry for maximal power transfer by a comparison of relative coupling coefficients.

Chapter 6

Conclusion

This thesis has developed a computational method for inductance predictions of inductors and investigated novel geometries for inductors used for power coupling to implants. This chapter summarizes the major contributions of this work and identifies areas that merit future study.

6.1 Contributions

- A computational method is developed from the partial inductance concept which is used to predict the inductance values - self and mutual - of various different inductor geometries and inductor configurations. Since power coupling to the implant depends on the mutual inductance obtained between the on-chip and external inductors, the predicted values of inductance may be used to choose an inductor geometry which can maximize the power transfer.

- Several test inductor structures are fabricated and their inductance values are measured. These measurements serve as a comparison for the values predicted by the computational code in order to prove the validity of the method. From the comparisons, it is evident that the computational method predicts the inductance values of the test structures quite accurately, within acceptable limits of error.

- Novel inductor geometries are proposed which are expected to enhance the coupling of power into the implant. These geometries may be fabricated on-chip using standard IC processing methods. Though on-chip 3-D inductors typically involve expensive and tedious processes, the proposed geometries for the inductors are distinguished by their ease of fabrication and cost-efficiency. A preliminary investigation is conducted into the process flow for the fabrication of the on-chip inductors.

6.2 Future Work

This sections identifies topics covered in this thesis which merit more detailed study.

- The fabrication of on-chip inductor test structures is a work currently in progress. Once the fabrication of these inductors has been completed, the inductance values obtained from measurements can be compared with the inductance values predicted by the computational code for the on-chip structures. This comparison will provide a definite confirmation regarding the validity of the computational method for the on-chip inductor geometries.

- The computational code may be enhanced and extended in a variety of ways. It can be expanded to include a larger variety of geometries. Currently, the code can handle 2-D geometries such as square & rectangular loops and spirals as well as 3-D geometries such as rectangular helices and pyramids. Some geometries that the code may be expanded to handle are polygonal 2-D and 3-D geometries such as spirals and pyramids of hexagonal or octagonal shapes.

- Another possibility for the enhancement of the code is for it to be able to handle segments inclined to each other at an angle. Currently, all segments are assumed to be parallel or perpendicular to each other. While this assumption is approximately valid for spirals, it may be violated for helices or pyramids which have a large vertical track separation.

- Further, even though the current code does not implement filamentisation of the segments since it is not required for the current dimensions, future work may implement this since it would lead to a more generalized and accurate code over a large range of dimensions.

- Finally, the current code can also be enhanced in its ability to handle the current geometries. For instance, a good degree of knowledge of the code is required for a user to be able to analyze a certain inductor geometry. This may be addressed by making the code capable of handling the geometric specifications with just the required dimensional parameters as inputs from the user. An interactive user interface may be included to make the procedure fast, efficient and user-friendly.

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