U.S. DEPARTMENT OF ENERGY
SMALL BUSINESS INNOVATION RESEARCH
Phase I SBIR Final Report
Grant DE-FG03-99ER82806
PROJECT SUMMARY

(All information provided on this page is subject to release to the public.)

Applicant Name: International Power Group, Inc.
Project Title: Innovative, New and Advanced High Voltage Power Supply for Capacitor Charging at Linear Collider
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Purpose of SBIR Phase I Research

The DOE requires a power supply for capacitor charging for a new linear accelerator. The supply must be over 90% efficient, reliable and cost effective to manufacture and maintain. A frequent difficulty with high voltage equipment is its cost, size and performance, especially in terms of efficiency. The market now demands decreased size with increased efficiency at a competitive price.

Brief Description of the Research Carried Out

The feasibility of the new cellular power supply design was examined using computer modeling, simulation and test results from a scaled down brass board prototype. The results show that the cellular design is a high efficiency (93 – 95%) supply and produces a more efficient capacitor charging profile when compared to conventional power supplies. The Phase I data also suggest a possible design for internal redundancy allowing continued operation with a component failure.

Research Findings

While not all results achieved were consistent with original prediction, it is clear from the study that the IPG power supply can meet the NLC requirement utilizing more than a single cell design and switching topology. The study results did make clear certain conclusions respecting cell size as it relates to component cost and reliability. The modeling made clear that the MTBF of the cellular supply is at least equal to a conventional supply, but that the ability to utilize internal redundancy creates a form of reliability not previously available in power supply design. The versatility of the cellular approach was made clear from the research performed.

Potential Applications of the Research

The cellular power supply design is well suited to numerous commercial, industrial and governmental program applications such as capacitor charging, high power vacuum tubes, electrostatic precipitators, and others where size, weight, efficiency and high reliability are critical. The power supply possesses inherently low stored energy, high efficiency, and is capable of rapid interactivity with a load. In many applications, cost to produce is equal to or less than for conventional supplies.

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INTRODUCTION: Report Contents

The purpose of the Phase I grant from the DOE was to address the following problem:

> The proposed electron-positron linear collider will be 10 times larger than present generation linear accelerators. The components required for this collider must enhance performance and reliability while reducing the high costs associated with both procurement and operation. In particular, the solicitation is for a 100kW (average) HVPS to charge a pulse-forming network with a total capacitance of 200nF to a maximum voltage of 80kV with an electrical efficiency > 90%. The HVPS must be compact in size, highly reliable (MTBF > 50,000 hours), and cost effective to manufacture and maintain. The HVPS required for the HV capacitor charging of the dual klystron modulator is one of the key components for the proposed collider.

As a solution to the above, IPG proposed to develop a HVPS (Phase I and II) based on the evolutionary patented cellular power supply technology.

This report will proceed with the following Sections:

I) A brief summary of the Tasks proposed and general results obtained from the study;

II) An in depth analysis of the study or research results;

III) Proof of feasibility, success and recommendations for the conduct of the Phase II grant.

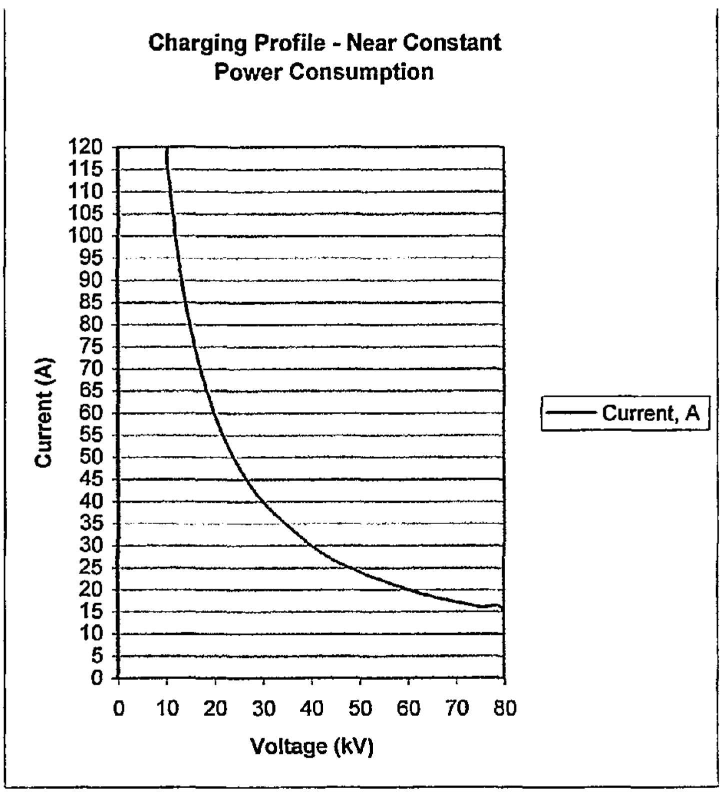
Section I Summary of the Study and General Results

Task I – Computer Modeling of a Real Capacitor

Capacitor data was collected from the capacitor manufacture (Maxwell) for the 10 nF capacitors used in the PFN. PFN data was collected from SLAC. A SPICE model of the PFN and simplified charging circuit were developed. Simulations of the charging process were run using Spice. The model was adjusted to represent the real PFN and simulations were again run to verify the model. A schematic of the model is contained in the final Phase I report, and it possesses sufficient data to be representative of the actual PFN. The task was completed and this data then used in the tasks that followed.

Task II – Determine Capacitor Charging Profile

A theoretical curve depicting an ideal charging profile for near constant power consumption was generated prior to actual computer modeling and is presented below as CHART I. This was subsequently modified in modeling to produce a practical and efficient charging profile that meets the requirements of the NLC for repetition rate and minimum charge time based on reasonable de-rating of components and reasonable number of parallel cells. This task was completed and the results provided appropriate data to be used in the tasks that follow.



Task III – Draft Design of HVPS Topology

The method of switching affects many other HVPS design and component issues. Consequently, two topology draft designs were developed: a hard switch and a series resonant switch. Based upon evaluation of the charging profile developed in Task II, and the maximum reasonable efficiency obtainable, a draft design of the HVPS was generated depicting both the theoretical maximum and minimum total number of cells. These numbers were 78 and 40, respectively, and using a hard switch circuit topology. Theoretical models were developed with calculations generated showing both a 78 and 60 cell hard switch. Although the task was completed, later studies in the Phase I portion of the research indicate that both the above theoretical cell size(s) and switching topology are unlikely to be the preferred embodiment. Subsequent computer analysis revealed that the range of possible acceptable configurations supported a smaller number of cells of higher voltage and current, and slightly favoring a series resonant switch. Also, the data suggests that a smaller number of higher voltage and current cells may be more appropriate in terms of total cost even though the originally proposed sixty cell design may have slightly higher theoretical efficiency. Consequently, further and the final comparative analysis, done in collaboration with SLAC team members, will be completed in Phase II.

Task IV – Computer Modeling of HVPS

Both of the topologies drafted in Task III were modeled in SPICE, and a simulation of the PFN charging process was performed for each. The models were modified as necessary to simulate reality as much as possible within the limitations of the software. Given the relatively complex modeling and number of variables considered, computer processing time was extreme, which necessitated use of computer using triple Pentium (750) processors. In order to ensure that the best circuit topology for the application is determinable, SPICE models of a hard switch and a series resonant circuit were developed. A simulation was run of each circuit topology in a multi-cellular format as each charged the PFN SPICE model. The HVPS models were modified as necessary until the simulation results were representative of reasonably expected results. The task was completed and the results provide appropriate data for comparison to further circuit modeling and testing of multiple cell structures as will be set forth in the Phase II application. In general terms, the results of the Phase I study showed that smaller cells are more appropriate than larger cells for maximum performance and efficiency. Additionally, the soft switch appears more robust and reliable for this application and specification.

Task V – Refined Design of the HVPS

A Comparison Matrix, shown below, was developed to consider such issues as power consumption, performance/efficiency/cost and relative size of the HVPS.

Review of the matrix indicates certain trends that need to be considered for the final HVPS design. Phase II will expand upon this matrix to further assure that the best design possible for the application requirements will be realized. Based on the simulation of the SPICE models of each circuit topology and cell size (voltage output) as the modeled capacitor is charged, modifications to the HVPS model were made. The task was completed and the results were incorporated in the final design decisions in Task VIII.

General Comparison Matrix (Non-Weighted)

Large = 20kV (2)
Small = 5kV

cell circuit topology	(input) Power Consumption (1)	Performance (1) (Controllability)		Efficiency (1)		Comparative Cost	Estimated HVPS Size
		Apparent	Reactive	Apparent	Reactive		
Small Hard	Medium	Med	Med	Med	Med	Med	Small
Small Soft	Very High	Very High	High (3)	Very High	Very High	Med	Med
Large Hard	Low	Low	High (4)	Low	Low	High	Med
Large Soft	High	High	Med High	High	High	Very High	Large

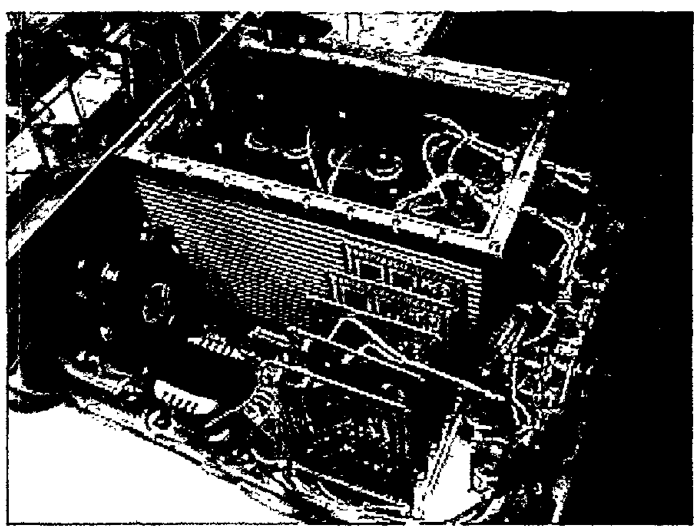
Notes:
(1) Additional graphs contained in Section II
(2) Phase II should examine a matrix of "small" cells of 5kV and lower together with a "large" cell of 10kV and 35kV
(3) At end of charging cycle
(4) At beginning of charging cycle

Task VI – Enhance the HVPS Reliability

The reliability of a single cell was calculated and extrapolated to include the entire power supply. Additionally, research was performed to evaluate enhancement of the HVPS reliability through the utilization of "redundant" cells in each Level (column) of the charging power supply (n+1). Phase II will expand this research to evaluate the use of hot swappable "cross-over" cells that can literally be operationally moved from and to any location in the cellular matrix. The task was completed. However, as a result of the investigation, it was determined that any method of implementing redundancy could significantly enhance reliability at a minimal overall cost when compared to an untimely failure and the likely need for backup or reserve HVPSs. Therefore, we will expand this research in Phase II to evaluate the use of in-line hot swappable single use replacement and "cross-over" cells that can be functionally moved from and to any location in the cellular matrix.

Task VII – Develop and Construct a Scaled Down Brass Board

Given the brevity of the Phase I study in terms of development of hardware, the decision as to the brass board prototype was determined based upon the theoretical model and during the early stages of computer modeling. A seven-cell series-parallel brass board prototype HVPS was developed to demonstrate the basic feasibility of performing constant power charging utilizing the IPG cellular technology. However, it was determined that despite the added cost, it was necessary to develop the prototype beyond the "brass board" type originally depicted. The below Photo 1 shows the final prototype, case opened with Plexiglas HV section top for viewing, which was completed and tested with positive results supplied to the SLAC design team(s). The supply operates from the 117Vac line to facilitate ease of movement and connection for demonstrations where there is limited available power, has a maximum output capability of –30kV at approximately 1800W, and adjustability and control of current in each stack or "column" of cells. The task was completed, and it was successfully demonstrated by performing the constant power charging through activation of parallel cells at the beginning of the charging process, then deactivating parallel cells while activating series cells as the charging process advanced to full charge. A video tape of the demonstration was submitted to the modulator design team at SLAC.

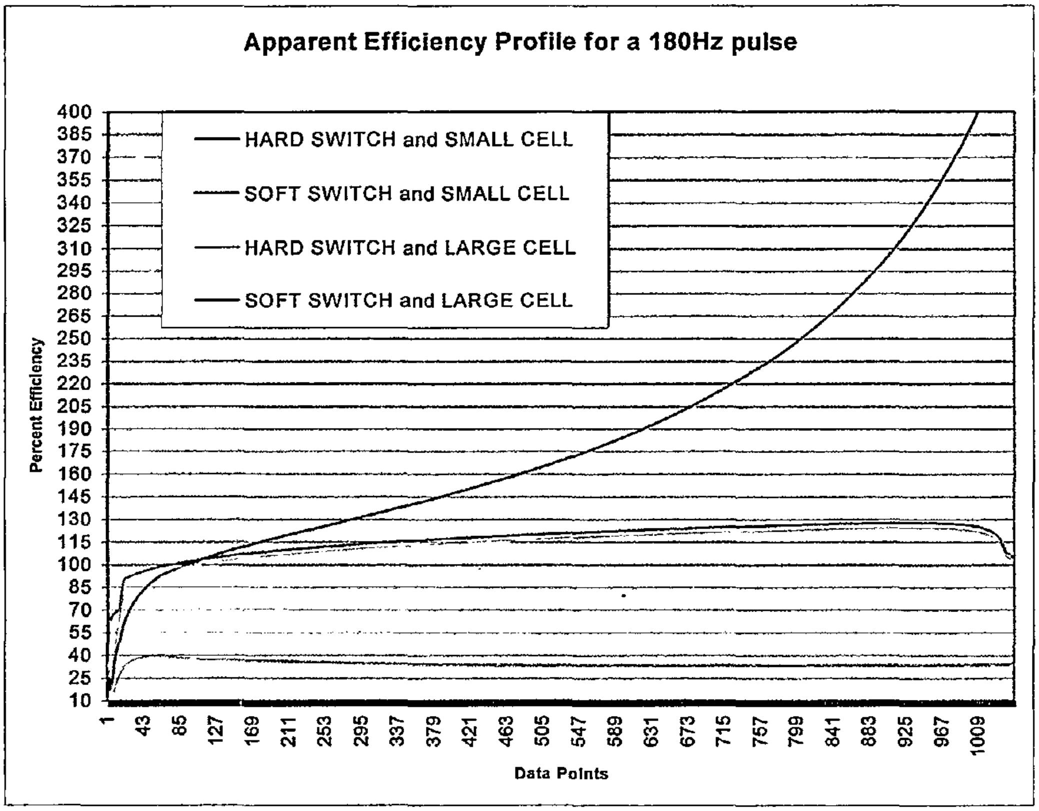


Task VIII – Final HVPS Design

Based on the research of Phase I, more than one solution to the question of cell and switching topology was derived. However, a range and trend for cell size was also established. In order to ensure the best combination of topology and cell size in consideration of efficiency, performance, reliability, and cost, a refinement and final analysis and selection is proposed for Phase II.

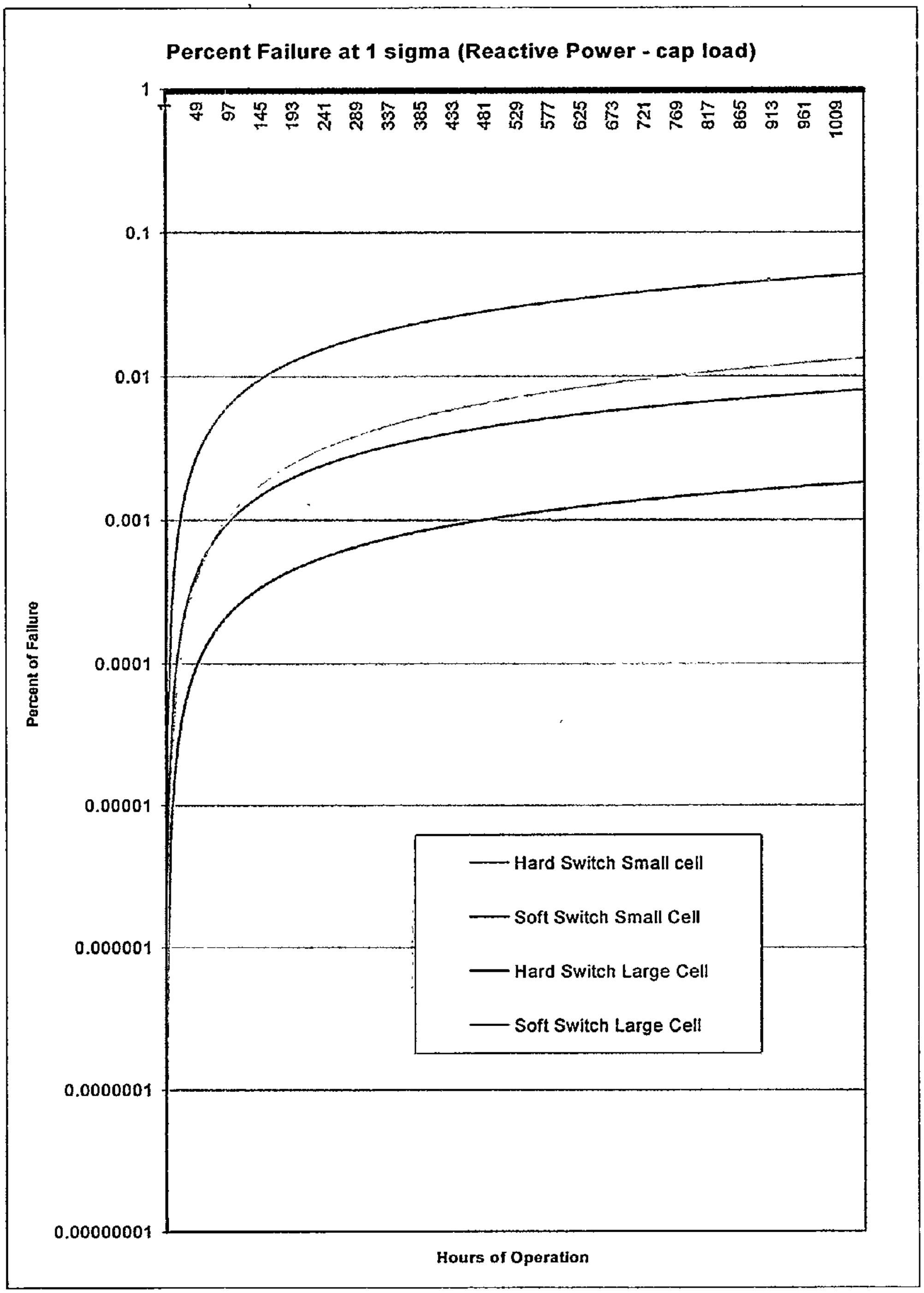
To portray a portion of the Phase I research results, the following graphs depict a number of key variables that answer two important questions raised in Phase I regarding cell size and topology: (1) what is the maximum relative efficiency, and (2) what is the input power consumption of the various topologies?

GRAPH 1 compares relative apparent efficiency of each of four combinations of cell size and topology as annotated on the graph. It is important to note that the graph depicts an anomaly with respect to the hard switch small cell data. This is explained very simply as follows: The most accurate portion of the graph is at the far left at approximately data point 43. Moving to the right, the back electromotive force (EMF) from the HV transformer begins to add to the apparent efficiency in the computer model. More detailed graphs for efficiency appear in Section II.



GRAPH 1 – Apparent Efficiency Profiles for a 180Hz Pulse

Graph 2 on the next page compares the relative percent failure of the power inverter over the charging cycle.



GRAPH 2: Percent Failure at 1 sigma (Reactive Power – cap load)

Results of the studies tend to indicate that contrary to what might be expected, there is not a strong correlation between cell size and overall HVPS cost.

However, other variables more significantly affect the selection of cell size, but these relationships do require further study as now proposed in this application through the development of a matrix of cell sizes and topologies.

Task IX – Hardware Design

The basic construction, layout and topology of the modeled HVPS were researched in Phase I. In particular, the criteria for the design of the HV transformer and rectifier assembly were established. These criteria included high voltage isolation, relative physical location of high voltage and low voltage components, assembly methods and techniques to allow for easy repair, etc. Calculations estimating the total volume of liquid dielectric and its maximum temperature and expansion characteristics were completed. The overall packaging scheme was also examined. The overall size of the HVPS was determined to be such that it would fit into a 72" tall standard 19" rack enclosure. A layout drawing of a sixty-cell and a forty cell HVPS that depict the relative locations of the low voltage and high voltage circuits and transitions between were generated. As mentioned previously, the sixty-cell configuration is unlikely to be the final embodiment unless some improvement occurs in component efficiency cost. The forty-cell configuration (approximate) appears more cost effective without any significant loss of efficiency or reliability. The task was completed, however the final cell size, among several that appear viable, and detailed mechanical design will be formulated upon completion of the research described in the Phase II application.

Section II Theory, Computations and Modeling Analysis

Consistent with the Tasks laid out in the Phase I application and described in Section I, the research team immediately embarked upon collecting data necessary to model the PFN (Pulse Forming Network) or modulator proposed for the NLC. Data was collected from two primary sources. One was obviously the modulator design team at SLAC who provided the overall modulator design criteria and characteristics necessary for a correct PFN model. The other major source of data was the manufacturer of one of capacitors being considered for use in the modulator circuit and a prior supplier to SLAC. Since an actual supplier is not yet identified, no other source was appropriate. Then both the theoretical design and modeling tasks were commenced. Data from the manufacturer's (Maxwell Technology) data sheet, and from special testing performed by the capacitor manufacturer, was combined with the pertinent data from the SLAC team to create a SPICE model of the PFN. Also modeled in SPICE was a basic charging circuit. Also, a simulation of the charging of the PFN model was performed. It should be noted that the following described data is presented in a logical manner, but does not necessarily follow the precise sequence of the numbered tasks in the application.

The HVPS should be able to charge 0.2Uf capacitor to the maximum voltage of 80,000V in 5ms or less. Assuming the capacitor's efficiency to be 100%, the average current needed is equal 3.2A.

One conceptual approach is to use what is equivalent to a single cell. This single cell or a conventional HVPS would need to be able to develop 3.2 A max and 80kV max. This would require that the HVPS should be designed for minimum power of 3.2 x 80 = 256kW plus factors for efficiency. Such a HVPS will provide linear (saw-tooth) energy consumption and a linear voltage increase. The maximum energy consumed from the primary network will be approximately 256kW (See Figure 1). In the original NLC modulator concept, some 3,000 HVPSs were required. This would result in a minimum total power requirement for the HVPSs of greater than 256 x 3,000 = 768MW. The efficiency of the charging process using such a HVPS would be comparatively low due to low energy to the HV capacitor when the output voltage is low.

Another approach is to use a theoretical maximum number of cells to make the power consumption in the charging process as uniform as possible (also see Figure 1). In the hypothetical case of virtually unlimited current from the HVPS, the power consumption would be about 128kW during a charging period (with 100% efficiency). This number sets up a limit for the "ideal" HVPS.

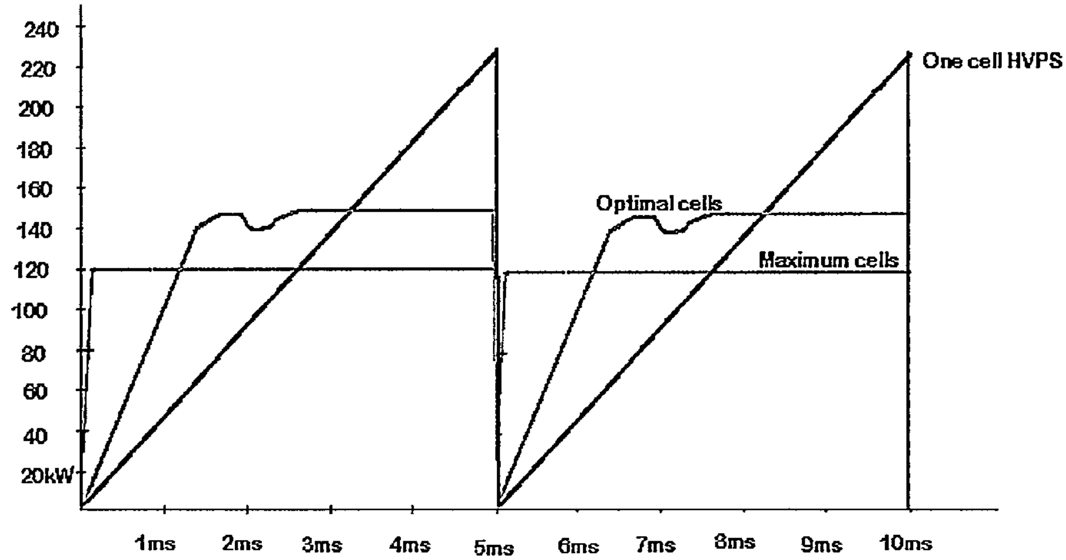


FIGURE 1: Power Consumption Comparison

Before proceeding, it is important to note that throughout the study, certain matters were consistently considered:

- Cost
- Losses (efficiency over charging process)
- Reliability
- Total volume of HVPS
- Manufacturability
- Design flexibility (in the event of a modification in design)

Theoretical Modeling

The initial theoretical model(s) considered the following:

Number of cells assumed: 60 cells at 3.333kV and 1.5A each, and in the alternative, 79 cells at 3.333kV and 1.7A each arranged in a different matrix. As indicated, *cells in the IPG HVPS may vary by output voltage and by output current. This, of course, defines the number of cells connected in series (voltage) and in parallel (current) for a given HVPS requirement.* The 60 cell model has three (3) "control" cells and appear as shown in Figure 2.

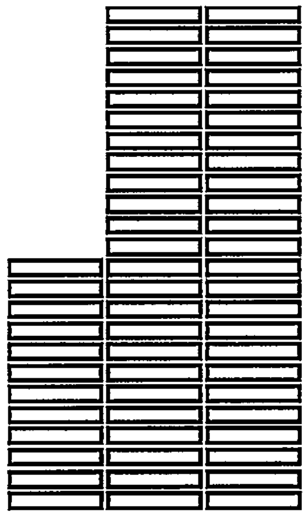


FIGURE 2: A 60 Cell Embodiment

One of the feasible variants is to use a 79 cell HVPS as shown in Figure 3. This HVPS is capable of transferring to the HV capacitor as much as 136kW. Each cell is capable of generating 3.333kV and current up to 1.7A. The maximum number of cells operating at a time is 44 (22 in series and 2 in parallel). The design for maximum output power of this HVPS is, therefore, 79 x 136/44 = 244kW. This is still much less than the one cell HVPS and results in lesser volume. Eight cells would be current controlled.

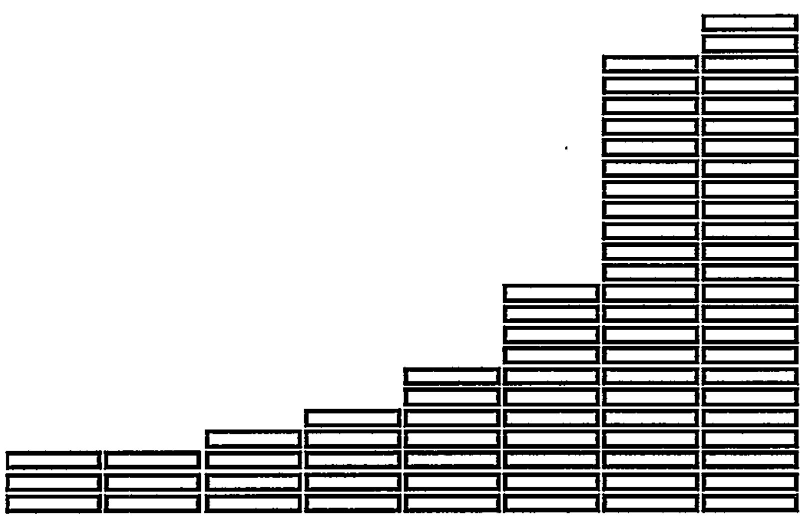


FIGURE 3: A 79 Cell Embodiment

At the beginning of the Phase I program, the intended power conversion circuit topology of cells of the HVPS was consistent with the IPG patents with the preferred embodiment envisioned by the inventor, i.e. a hard switched high frequency inverter. From this conception and for comparison, a schematic of a single cell was developed that included a high frequency dc-ac inverter operating at approximately 30kHz, the ac output of which is used to drive the primary of a high voltage transformer. The multiple secondaries of the HV transformer are rectified and connected in series to provide the dc output voltage of the cell.

Capacitor charging process

The real value of the IPG technology is the flexibility and tight control of current, voltage and power. This makes it possible to develop a charging curve as close to ideal as practical with a **minimum capital cost and maximum efficiency.** The IPG technology utilization of cells in series and in parallel ensure optimal current and voltage values during the HV capacitor charging process with virtually equal voltage and current stresses in power components.

It should be noted, that the efficiency stated in the data sheet for any HVPS differs from the actual efficiency of the HVPS during HV capacitor charging. This is especially important when a capacitor is fully discharged. The power delivered to the HV capacitor is equal to the voltage (V) across the capacitor at any given instant of time multiplied by the current (I) flowing into the capacitor at that same instant. At the beginning of each charging process the power delivered to the capacitor is close to zero. This is because the voltage is very low at this time. However, the losses in the HVPS are not small. As follows from the calculations to follow, static losses that depend on current are greater than switching losses and outnumber the latter by at least a factor of four. A HVPS's efficiency is the ratio of the power delivered to the capacitor (P_c) to the power being consumed from the primary source (P_p). The latter is the sum of power delivered (P_c) and the HVPS's losses (P_L). Efficiency (E) at any given moment is therefore equal:

$$E = P_c/P_p = P_c/(P_c + P_L) = I \times V/(I \times V + P_L)$$

It is obvious that at zero voltage (V) across a capacitor, the efficiency is equal to zero because power to the capacitor P_c is close to zero. At low voltages the efficiency is also very low. The average efficiency over the charging process is never equal to the HVPS's maximum efficiency capability such as with a pure resistive load or *during the partial discharge process.* **The key to greater average efficiency for the fully discharged HV capacitor is to increase voltage at the beginning of the charging process as fast as possible.** This means that the current flowing into the HV capacitor must be of greater value at the beginning of the charging process and gradually decrease toward the end of this process.

The IPG cellular HVPS is more capable of being able to perform the charging process than conventional single inverter devices. Detailed calculations were made for the 60 and 79 cell embodiments, which show that the IPG HVPS is capable of generating a near constant power consumption (see Tables 1 & 2).

The following calculations and discussion refer to the 60 cell embodiment. In order to calculate overall efficiency, the charging process has been divided into 24 periods. During each period, a specific predetermined current is delivered to the capacitor. The time duration of each period (T_P) is determined by the time necessary to charge the HV capacitor to the next predetermined voltage.

$$T_P = C / I \times (V_N - V_{N-1})$$

During the first period, for instance, the HV capacitor is charged to the maximum voltage of a single inverter, i.e. 3,333V. During this period the current flowing to the HV capacitor is equal 4.5A. Therefore,

$$T_P = 0.2 \times 10^{-6}/4.5\ (3{,}333 - 0) = 148\mu s.$$

As shown in the table, during the next period the current remains at the same value as does the duration of the period. During the periods from 13 to 15, the current is equal to 3A and the duration of these periods is equal 240µs. Losses for each period are the sum of the losses of each cell (active or inactive) through which electric current is flowing. All losses are calculated in accordance with above calculations for the hard switching cells taking into account necessary current deviations. For instance, losses during the first period consist of losses in

- Three PWM converters
- Three activated inverter cells
- 57 inactive inverter cells.

Voltage across the power components of an inverter cell increases from zero to a maximum value 650V during each period. It is assumed, therefore, that switching losses during each that are proportional to that voltage and are about one half of that at the maximum voltage. Losses in the magnetic core are proportional to $V^{2.6}$ and are $0.5^{2.6} = 0.165$ of those under the maximum voltage. Thus during the first stage losses in three PWM converters are equal to 3 x 59.5W = 178.5W. Losses in three inverter cells are equal to 3 x (29.3 + 10.0/2 + 27.5 + 22.5 x 0.165 + 48 + 9.2 + 25) = 3 x 147.7W = 443.1W. Losses in inactive cells are equal to 57 x 24W = 1,368W. Total losses in the HVPS are equal to 178.5 + 443.1 + 1,368 = 1989.6W. This same method is applied to each period. During last several periods it is reasonable to maintain the output current of each cell at the level that is less than the cell's maximum current, I_{MAX}. This maintains the consumed energy at approximately the same level, i.e. 150kW. The losses in active cells were assumed lower than those at the maximum current. The ratio of the actual losses to the maximum losses is therefore equal $(I/I_{MAX})^2$. Thus, if the maximum losses in the inverter cell are equal to 137.9W at 1.5A of output current, the same cell losses at 1.3A are equal to $137.9 \times (1.3/1.5)^2 = 103.6$W. Energy lost during the first period is equal to the period duration times power losses, i.e. $148 \times 10^{-6} \times 1952.1 = 289 \times 10^{-3}$J. The ratio of total energy loss over the charging period to the electric energy stored in the capacitor defines capacitor charging process efficiency. As it follows from Table 1, total energy loss is equal to 23.434J during the charging process. At the same time, electric energy accumulated in the HV capacitor is equal to $0.2 \times 10^{-6}\ 80{,}000^2/2 = 640$J. Therefore, the total efficiency of the charging process is equal to 640/(640 + 23.434) = 96.47%.

Cumm. Time	Maximum voltage at the end of period kV	Maximum power delivered to the HV capacitor kW	Current flowing into the HV capacitor A	Number of cells connected in series	Number of cells connected in parallel	Losses in PWMs (active) W	Losses in active cells W	Losses in inactive cells W	Period duration ms	Losses during period W	Energy loss during the period J
1.48E-04	3.333	15	4.5	1	3	178.5	514.5	1368.0	1.48E-04	2061.0	0.305
2.96E-04	6.666	30	4.5	2	3	178.5	1029.0	1296.0	1.48E-04	2503.5	0.371
4.44E-04	10	45	4.5	3	3	178.5	1543.5	1224.0	1.48E-04	2946.0	0.437
5.92E-04	13.33	60	4.5	4	3	178.5	2058.0	1152.0	1.48E-04	3388.5	0.501
7.41E-04	16.67	75	4.5	5	3	178.5	2572.5	1080.0	1.48E-04	3831.0	0.569
8.89E-04	20	90	4.5	6	3	178.5	3087.0	1008.0	1.48E-04	4273.5	0.632
1.04E-03	23.33	105	4.5	7	3	178.5	3601.5	936.0	1.48E-04	4716.0	0.698
1.19E-03	26.666	120	4.5	8	3	178.5	4116.0	864.0	1.48E-04	5158.5	0.765
1.33E-03	30	135	4.5	9	3	178.5	4630.5	792.0	1.48E-04	5601.0	0.830
1.48E-03	33.333	150	4.5	10	3	178.5	5145.0	720.0	1.48E-04	6043.5	0.895
1.63E-03	36.666	165	4.5	11	3	178.5	5659.5	648.0	1.48E-04	6486.0	0.961
1.78E-03	40	180	4.5	12	3	178.5	6174.0	576.0	1.48E-04	6928.5	1.027
2.00E-03	43.333	130	3	13	2	119.0	4459.0	528.0	2.22E-04	5106.0	1.135
2.22E-03	46.666	140	3	14	2	119.0	4802.0	480.0	2.22E-04	5401.0	1.200
2.44E-03	50	150	3	15	2	119.0	5145.0	432.0	2.22E-04	5696.0	1.266
2.68E-03	53.333	150	2.81	16	2	104.4	4814.9	359.7	2.37E-04	5279.0	1.252
2.93E-03	56.666	150	2.65	17	2	92.9	4549.8	296.8	2.52E-04	4939.5	1.243
3.20E-03	60	150	2.5	18	2	82.6	4287.5	240.0	2.67E-04	4610.1	1.230
3.48E-03	63.333	150	2.37	19	2	74.3	4067.3	189.6	2.81E-04	4331.1	1.218
3.78E-03	66.666	150	2.25	20	2	66.9	3858.8	144.0	2.96E-04	4069.7	1.206
4.09E-03	70	150	2.14	21	2	60.6	3665.2	102.7	3.12E-04	3828.5	1.193
4.42E-03	73.333	150	2.04	22	2	55.0	3489.3	65.3	3.27E-04	3609.6	1.179
4.76E-03	76.666	150	1.96	23	2	50.8	3367.4	31.4	3.40E-04	3449.5	1.173
5.11E-03	80	152	1.9	24	2	47.7	3301.9	0.0	3.51E-04	3349.7	1.176
										Total	22.461

TABLE 1 – 60 Cell Model

Similar calculations were performed to verify the 79 cell configuration. The results are summarized in Table 2 and clearly show that the actual charging profile is slightly superior to the 60 cell configuration and, therefore, is closer to the preferred optimal design. However, the apparent cost and physical size are greater. Consequently, the 60 cell design does represent a more effective over all embodiment.

Cumm. Time	Maximum voltage at the end of period, kV	Maximum power delivered to the HV capacitor kW	Current flowing into the HV capacitor A	Number of cells connected in series	Number of cells connected in parallel	Losses in PWMs (active) W	Losses in active cells W	Losses in inactive cells W	Period duration sec	Losses during period W	Energy loss during the period J
4.90E-05	3.333	45	13.6	1	8	611.4	1762.3	1931.2	4.90E-05	4304.9	0.211
9.80E-05	6.666	91	13.6	2	8	611.4	3524.5	1713.6	4.90E-05	5849.5	0.287
1.47E-04	10	136	13.6	3	8	611.4	5286.8	1496.0	4.90E-05	7394.2	0.363
2.12E-04	13.33	136	10.2	4	6	458.5	5286.8	1496.0	6.53E-05	7241.3	0.473
2.94E-04	16.67	136	8.15	5	5	351.3	5062.9	1408.3	8.20E-05	6822.5	0.559
3.92E-04	20	136	6.8	6	4	305.7	5286.8	1496.0	9.79E-05	7088.5	0.694
5.06E-04	23.33	136	5.83	7	4	224.7	4533.7	1189.3	1.14E-04	5947.8	0.679
6.37E-04	26.666	136	5.1	8	3	229.3	5286.8	1496.0	1.31E-04	7012.0	0.917
7.85E-04	30	136	4.53	9	3	180.9	4692.4	1256.3	1.47E-04	6129.7	0.902
9.48E-04	33.333	136	4.08	10	3	146.7	4229.4	1066.2	1.63E-04	5442.4	0.889
1.13E-03	36.666	136	3.71	11	3	121.3	3846.8	910.2	1.80E-04	4878.3	0.877
1.32E-03	40	136	3.4	12	2	152.8	5286.8	1496.0	1.96E-04	6935.6	1.360
1.54E-03	43.333	136	3.14	13	2	130.4	4884.9	1331.4	2.12E-04	6346.6	1.347
1.77E-03	46.666	136	2.91	14	2	112.0	4518.2	1187.3	2.29E-04	5817.4	1.333
2.01E-03	50	136	2.72	15	2	97.8	4229.4	1066.2	2.45E-04	5393.5	1.322
2.27E-03	53.333	136	2.55	16	2	86.0	3965.1	958.8	2.61E-04	5009.9	1.310
2.55E-03	56.666	136	2.4	17	2	76.2	3731.8	864.0	2.78E-04	4672.0	1.298
2.84E-03	60	136	2.27	18	2	68.1	3534.9	780.9	2.94E-04	4383.9	1.288
3.15E-03	63.333	136	2.15	19	2	61.1	3347.2	705.2	3.10E-04	4113.5	1.275
3.48E-03	66.666	136	2.04	20	2	55.0	3172.1	636.5	3.27E-04	3863.6	1.262
3.82E-03	70	136	1.94	21	2	49.8	3012.1	574.2	3.44E-04	3636.1	1.250
4.18E-03	73.333	136	1.85	22	2	45.3	2869.6	518.0	3.60E-04	3432.8	1.237
4.58E-03	76.666	130	1.7	23	1	76.4	5066.5	1523.2	3.92E-04	6666.1	2.614
4.97E-03	80	136	1.7	24	1	76.4	5286.8	1496.0	3.92E-04	6859.2	2.690
										Total	26.438

TABLE 2 – 79 Cell Model

A Comparison Between Hard Switching and Soft Switching Circuit Topologies for Power Converters for Capacitor Charging Application.

A matter worthy of note before the analysis. We have examined the available literature from various HVPS suppliers who could potentially supply a single transformer resonant switcher for capacitor charging. We can find no evidence or documented cases in this information of resonant HVPSs connected in series for capacitor charging applications. Therefore, some skepticism regarding the feasibility of such connection is understandable. Unlike the IPG cellular approach, it is not clear how different HVPSs would "negotiate" voltage and current distribution between themselves while connected in series to the common capacitive load. It may seem that only one of either current or voltage may be able to be controlled using a resonant format. The virtual lack of available information of documented use of series connected resonant inverters makes it very difficult to determine the charging process of such a possible device.

A review of hard switching and soft switching power conversion

Hard switching of power transistors occurs when the ON or OFF transition of the current through the transistor and the voltage across the transistor's collector-emitter (source-drain for MOSFET) takes place nearly simultaneously. The initial moment of switching often coincides with the maximum magnitude of one of those values and the final moment of switching often ends with the maximum magnitude of the other value. If, for instant, a transistor was in an ON state before switching, the current flowing through it is at the maximum possible magnitude while the voltage is near zero. At the end of the switching process, when the transistor is OFF, no current flows; however, the voltage is close to maximum magnitude.

During a transition period three things occur:

1) The rapid change of voltage and current from zero to maximum creates large magnitudes of both magnetic and electric field first derivatives. That, in accordance with laws of electrodynamics, induces electromotive and magnetomotive forces in nearby conductors. The voltage change leads to EMF induction through capacitive links between conductors. The current change induces MMF through the magnetic field common between two or more conductors [18]. The influence is proportional either to dV/dt (electric field) or dI/dt (magnetic field) in the conductors connected to the switching transistor. Depending on power, frequency and proximity to the sensitive equipment it may cause some disturbances in the equipment operation if the forces exceed FCC or VDE standards [3]. This issue is eliminated in this specific HV application. "Most of the concerns ... surround AC-DC supplies that are connected directly to the DC mains. These products will typically contain input filtering designed to suppress conducted emissions to a level below one of the FCC or VDE standards. Radiated emissions... are typically limited by careful magnetics design and shielded packaging."[3].

2) The switching transistor is subjected to current and voltage simultaneously. The transition period is, therefore, characterized by power dissipation that is many times greater than in the ON state when voltage across the transistor is very small. Despite the short duration of a transition period, average losses are comparable to the losses during ON stage and often may exceed the latter. Switching losses are approximately proportional to the switching frequency and, according to [11] are

$$P_{SW} = 1/8\, f\, (I_{min} V_{DS} t_{on} + I_{max} V_{DS} t_{off})$$

Therefore, there is a practical limit to the frequency of operation of hard switched devices in certain applications.

Substantially similar results are shown in [19], where

$$P_{SW} = 1/6\, f\, (I_{max} V_{DS} (t_{on} + t_{off}))$$

From another view, $t_{on} + t_{off}$ is proportional to V_{DS} at the same voltage change rate (dV/dt) and, as shown in [19],

$$P_{SW} = 1/6\, f\, (I\, V_{DS}{}^2 (t_{on} + t_{off})$$

In order to minimize switching losses one should consider the above illustrated inverse proportionality of the frequency and $V_{DS}{}^2$. This consideration leads to the fact that for low voltage applications, such as battery powered power supplies, high frequency switching up to the megahertz region is justified. However, for high voltage applications, such a frequency range should be considered as an exotic feature that leads to no real advantages [20].

3) The voltage and current may go beyond the SOA (Safe Operating Area) of the transistor's capabilities [17].

These concerns have led to the development of soft switching techniques that slow the transition of the current and/or voltage during the switching time by addition of capacitors and inductors in series with the transformers primary winding. Therefore, the current through and voltage across the transistor during the transition period do not change simultaneously and switching losses are drastically reduced. Also, when the current and voltage waveforms are of a sinusoidal shape, both dV/dt and dI/dt are within reasonable limits and are less likely to induce disturbances in nearby circuits.

The below study makes a comparison between the two techniques: hard switching and series-resonant switching, which is becoming more popular in modern state-of-the-art power supplies. It should be noted that resonant and quasi-resonant topologies, although new to many designers, have been a consideration for quite some time. As long as two decades ago the concept of a "bell" shape of a current through transistors was proposed. However, due to the obvious complication of such wave-form generation, the approach has not been in common use until more recently. It should also be noted that soft switching techniques are not without significant potential problems or limitations. "The use of resonant converter topologies would help to reduce the switching losses in

DC-DC converters and enable the operation at switching frequencies in the megahertz range. The major disadvantage of resonant converters is increased peak current (or voltage) stress [15]."

In summation, it should be stated that both hard switching and soft switching converters are on today's market and both have advantages and disadvantages of which some may be crucial depending on the application. **The below comparison does not claim a to be of universal character, but rather is applicable to the specified purpose: the charging of the HV capacitor needed for NLC.**

To make a practical comparison between the two topologies, one should take into account the following:

1. The general efficiency of the power converter. This includes losses in all the components, such as power transistors (both static and dynamic losses), conductors including transformer and inductor windings, diodes and magnetic cores. The losses in those components depend on input and output voltage, operating frequency, magnetic materials and actual design topology.
2. The power converter's efficiency for the particular HV capacitor charging application. The efficiency of the converter is quite different for different load characteristics of capacitance, resistance, inductance or any combination thereof.
3. Circuit complexity and capital cost. That includes the design cost and cost of the components.
4. The power converter's reliability. More component count may mean lesser reliability while simple circuitry promises the greatest MTBF.
5. Components' safe operating area.
6. Converter's enclosure. When a converter is enclosed into a conductive enclosure that is properly grounded, virtually no EMF or MMF is generated to the outside world.
7. Industry trends. Since we are looking into year 2003-2004, or beyond, for the actual project start, it would be wise to consider industry trends in semiconductors' development rather than solely deal with today's components.

Circuit description

The initial preferred embodiment of the IPG HVPS as envisioned by the inventor consists of 60 separate uniform hard switched inverter cells arranged in three columns. At the bottom of each column is a voltage-to-current converter for regulation of each column's voltage and current over the charging process. This preferred embodiment of the IPG power inverter is designed for the input voltage 480V 3Ph AC 650VDC and maximum output power 5,000W. Output voltage of each inverter is 3,333V while maximum output current is 1.5A. The power inverter (Figure 4) is a full bridge inverter connected to HV transformer.

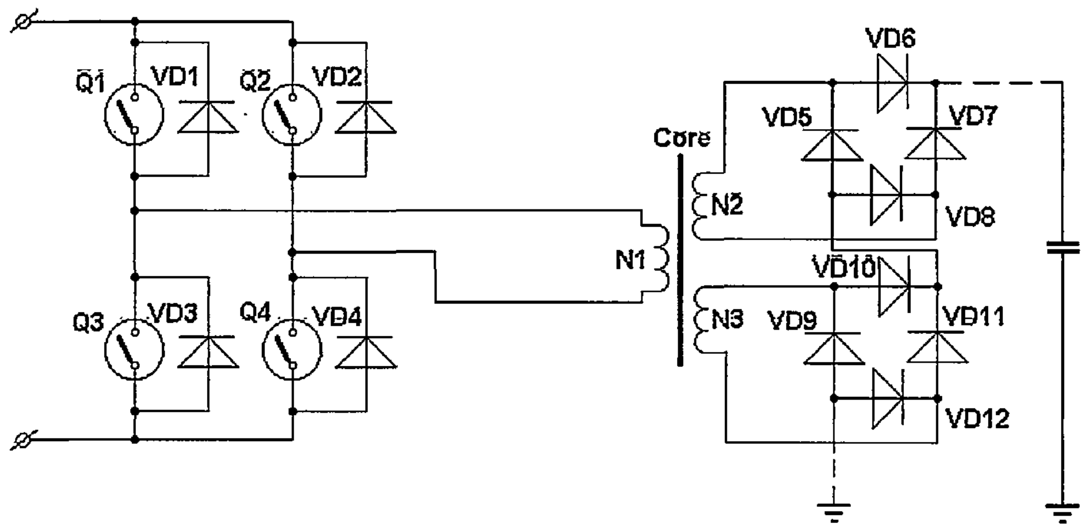


FIGURE 4

The latter has two secondary windings, each of which is connected to a full bridge arrangement of HV rectifiers. The outputs of the bridge rectifiers are connected in series to generate the output of the inverter cell. Due to IPG's patented conversion process, current through power transistors Q1-Q4 is of the substantially constant value during each half of the switching period and does not exceed 8.0A. Average current value is 7.70A. Due to direct conversion and parallel diodes D1-D4 across the power transistors, no excessive voltage is anticipated and use of 1,200V IGBTs is justified. Modern IGBTs have a saturation voltage about 1.9V [6]. Switching (transient) time ON and OFF of the IGBTs is 0.1μs each. Diodes D1-D4 serve to conduct current during short period of dead time when none of the power transistors are ON. HV diodes D5-D12 are Voltage Multiplier PN 1N6517 with maximum average current 2.0A and maximum forward voltage 8.0V. Maximum reverse recovery time is 70ns [32]. The HV transformer is custom made and consists of a pair of magnetic U-core and three windings - one primary and two secondaries. Leakage inductance does not play a significant role in the conversion process due to IPG's patented conversion process that largely overcomes the leakage inductance by applying excessive voltage to the transformer primary during first 1-1.5μs each half of period. However, the short delay caused by the leakage inductance does separate transient current and transient voltage resulting in virtually no switching losses during the ON transition. Switching losses occur only during the OFF transition time. The chosen operating frequency is 30kHz based on the initial discussion of this comparison.

The power losses for each inverter cell are as follows:

1. Static losses (P_s) in power transistors. In the bridge configuration, two transistors conduct simultaneously during each half cycle of the inversion process.

   Total voltage drop is 2 x 1.9V = 3.8V. Static losses, P_s = 7.7A x 3.8V = 29.3W.

2. Switching losses (P_{SW}) during OFF time.

   $P_{SW} = 1/6\ f\ I_{max}\ V_{DS}\ t_{off}$ = 1/6 x 30,000Hz x 650V x 7.7A x 10^{-7}s= 2.5 W per transistor.

   Total P_{SW} value for all 4 transistors is 4 x 2.5 = 10.0W.

3. HV transformer losses. Typical efficiency of HV transformer of similar output power and output voltage is about 99% and power losses are about 50W (industry practice and IPG's experience). This figure is valid for square wave input voltage and current. Of this 1% losses, about 55% are attributed to the windings (both secondary and primary) and the remaining 45% are attributable to the magnetic ferrite core. That constitutes 27.5W for windings and 22.5W for a magnetic core.

4. Output HV rectifier. When a cell is active, i.e. power transistors switch ON and OFF at a frequency 30kHz, four HV diodes per cell conduct current simultaneously.

   Total voltage drop is 4 x 8.0V = 32V.

   Static losses (P_S) are, therefore, equal P_S = 1.5A x 32V = 48W.

   Switching losses are negligible. This is due to the leakage inductance which creates a time delay between voltage across a diode and current through the diode that is much greater than HV diode (1N6517) recovery time. When a cell is passive and all transistors are OFF current still flows from adjacent cells through HV diodes. To decrease these static losses additional diodes may be installed in diagonals of each HV diode bridge (not shown). In this case static losses will constitute only a half of 48W when cell is active, i.e. 24W per cell.

5. Total losses (P_t) in power inversion are, therefore, equal

   P_t = 29.3 + 10.0 + 50 + 48 = 137.3W

   when the cell is active and 24W when the cell is OFF.

Efficiency (E) of the inversion circuitry is about E = 5,000/(5,000 + 137.3) = 97.3%.

6. In addition to the inversion circuitry, each cell includes a 3 phase input rectifier. Based on Voltage Multipliers PN 3310 [32], the forward voltage drop of each diode is equal to 1.2V. Two diodes conduct current simultaneously. Therefore, rectifier losses (P_r) are equal to

$$P_r = 1.2V \times 7.7A = 9.2W.$$

7. Losses in buses, control circuitry, etc. are assumed at the level 25W, of which buses' losses are about a half of this value, i.e. 12.5W.

8. Overall losses (P_o) in a cell, therefore, equal

$$P_o = 137.3 + 9.2 + 25 = 171.5W$$

and the overall maximum efficiency of an active cell is

$$E = 5000/(5000 + 171.5) = 96.68\%$$

A simplified schematic of the voltage-to-current converters is shown in Figure 5.

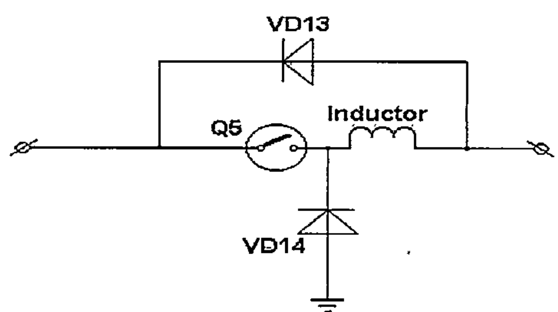


FIGURE 5

The converter consists of a power IGBT (Q5), two diodes (VD 13 and VD14) and an inductor. The circuit converts input voltage to output current of a preset value.

Power losses for the converter are as follows:

1. The losses in the power transistor, Q5, depend on the duty cycle and are of a maximum value when duty cycle is at its maximum. Let us assume that

average duty cycle is equal to 50% and that the mode of operation is continuous. Average current is equal to 7.7A while maximum current, I_{max} = 8.47A and I_{min} = 6.93A (+/- 10% input line). The transistor's static losses (P_S) are

$$P_S = 0.5 \times 7.7A \times 1.9V = 7.3W.$$

Switching losses (P_{SW}) are

$$P_{SW} = 1/6\ f\ [(I_{min} \times V_{DS} \times t_{on}) + (I_{max} \times V_{DS} \times t_{off})] = 1/6 \times 30{,}000Hz \times [(6.93A \times 650V \times 10^{-7}s) + (6.47A \times 650V \times 10^{-7}s)] = 5.0W.$$

2. Static losses (P_S) in the diode D14 are equal to

$$P_S = 0.5 \times 7.7A \times 0.7V = 2.7W$$

Switching losses P_{SW} are equal to

$$1/6\ f\ (I_{max} \times V_{DS} \times t_{on} + I_{min} \times V_{DS} \times t_{on}) =$$
$$= 1/6 \times 30{,}000\ [(8.47 \times 650 \times 70 \times 10^{-9}) + (6.93 \times 650 \times 70 \times 10^{-9})] = 3.5W.$$

3. Inductor's losses (P_i) are assumed as a half of those in HV transformer. This is because inductor has just one winding and the magnetic core operates at a lower maximum flux density. Therefore, P_i = 25W.

4. Static losses in the diode D13 are negligible because it conducts current during very short time (about 2% of a period) while switching losses are approximately of the same value as those in the diode D14.

$$P_{SW} = 3.5W$$

5. Losses in buses, control circuitry, etc. are assumed at the level 12.5W.

6. Total losses (P_t) in a PWM are, therefore, equal to

$$P_t = 7.3 + 5.0 + 2.7 + 3.5 + 25 + 3.5 + 12.5 = 59.5W$$

and overall maximum efficiency of a PWM is about 5,000/(5,000 + 59.5) = 98.8%.

A simplified schematic of a resonant inverter [21] is shown in Figure 6, and consists of nearly the same components as the above IPG inverter.

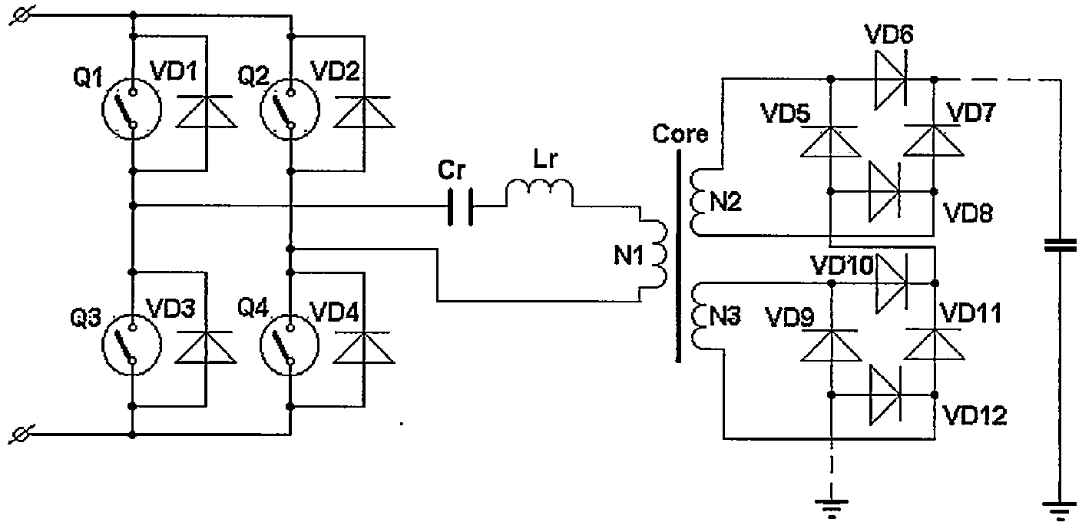


FIGURE 6

In addition to the components of the hard switched IPG inverter, a resonant capacitor, Cr, and a resonant inductor, Lr, are included. All sources indicate that switching losses in such a resonant inverter are essentially equal to zero. On the other hand, the resonant peak voltages and currents cause an estimated 10% increase in transformer winding and core losses, and power buss losses. The operating frequency for the soft switch circuitry is assumed to be the same as that of the hard switch, i.e. about 30kHz.

1. Static losses in power transistors. Two transistors conduct at a time. Total voltage drop is 2 x 1.9V = 3.8V. Static losses are,

$$P_s = 7.7A \times 3.8V = 29.3W$$

2. Switching losses $P_{SW} = 0$.

3. Resonant capacitor losses P_{RC} = approximately 6.5W, based on an ESR of 0.1Ω, and a peak current of 18A over 20% of the cycle.

4. Resonant inductor losses P_{LR} = approximately 5W, based on use of an EE55 ferrite core using 3F3 material.

5. HV transformer losses. Assuming again a typical efficiency of HV transformer of similar output power and output voltage is about 99% and power losses are about 50W. Of this 1% losses about 55% consume windings (both secondary and primary) and the rest 45% consumes magnetic ferrite core. This is 27.5 x 1.1 = 30.25W for windings and 22.5 x 1.1 = 24.75W for a magnetic core. Total losses in HV transformer are, therefore,

$$P_t = 30.25 + 24.75 = 55W.$$

6. Output HV rectifier. Four HV diodes conduct current. Total voltage drop is 4 x 8.0V = 32V. Static losses P_S are, therefore,

$$P_S = 1.5A \times 32V = 48W$$

   Switching losses are negligible.

7. Losses in busses are approximately 10% higher than for hard switch inverter, i.e. 12.5W x 1.1 = 13.75W.

8. Losses in control circuitry are assumed the same as in IPG inverter despite of more complex control circuitry required [16], i.e. 12.5W.

9. Total losses P_t in resonant converter are, therefore, equal

$$P_t = 29.3 + 6.5 + 5 + 55 + 48 + 13.75 + 12.5 = 170.0W$$

   Efficiency E of the inverter cell is

$$E = 5{,}000/(5{,}000 + 170.0) = 96.7\%$$

10. In addition each cell comprises of input 3Ph rectifier of the same design. Rectifier losses P_r are equal $P_r = 7.8W$.

11. Total losses in inverter cell are, therefore, equal

$$P_o = 170.0 + 7.8 = 177.8W$$

and overall maximum efficiency of a active cell is

$$E = 5000/(5000 + 177.8) = 96.57\%.$$

Use of a PWM buck regulator, not unlike that described above as the voltage to current converter, assumes that the losses here will be the same as previously described.

A comparison of the results of the above calculations appear in Table 3. As can be seen, the theoretical difference in efficiency between the two topologies is nearly insignificant.

	Hard Switch	Soft Switch
Inverter Efficiency	96.68%	96.57%
PWM Converter Efficiency	98.8%	98.8%

TABLE 3

Practical design, however, should consider the possible higher I_{RMS}/I_{AVG} ratio and other possible losses, including switching ones, utilizing a resonant power conversion technique. Other HVPS manufacturers report the efficiency of power resonant converter no higher than 92% [33] with a typical value about 85% [24]. It has also [15] been stated that ". . . the major disadvantage of resonant converters is increased peak current (or voltage) stress." The preceding is evidence that resonant power conversion requires careful design consideration to maximize it's full potential. "Today, quasi-resonant technology is just one of many possible design options the power supply designer can select. Other path such as PWM phase modulation of full-bridge converters... are reasonable design option... Quasi-resonant switching power supplies require about 30% more development time and cost about 10% more in the bill of materials over a comparable PWM switching power supply. The major applications in which quasi-resonant technology finds acceptance today are those that require a very low radiated RFI level" [16].

Trends in Component Development

Since our goal is to create a HVPS that will be perfect at the year 2004 or later, power electronics industry trends are taken into consideration. IGBT power transistors are chosen due to considerable progress made and additional expected changes in the future. Fourth generation of IGBT voltage drop [1 and 3] is decreased while switching frequency is increased. It is expected that a 1,200V IGBT will reach 1.9V voltage ON drop this year [6]. At the same time "...for high voltage MOSFET it is impossible to change the well established law $R_{DS(on)} * kV^{2.6}$. IGBT technology is progressing more rapidly than any other power switching device. The IGBT has one essential major economic advantage over the MOSFET: a higher switchable power/silicon ratio. IGBTs are now mature turn-off components adapted from very low power (1A) to very high power (3.3kV at 1.2kA)[8]. "When done correctly, using an IGBT instead of a MOSFET provides lower system cost and higher system reliability. Switching losses for a 600W, 90Vac Gen 4 IGBT (size 3) are about half of that for a comparable MOSFET (2SK899, 2 devices, size 5) operating at a frequency of 50kHz

Comparison of Standard Single Transformer Design with the IPG Cellular Design

A comparison of the maximum efficiency expected from the IPG cellular HVPS and a conventional single transformer HVPS was done.

The conventional HVPS consists of a voltage-to-current regulator circuit (buck converter) and power inverter, which is consistent with the previously described inverter and buck regulator of the preferred embodiment of the IPG cell design.

An assumption is made that all losses in a conventional HVPS consisting of one or more modules is proportional to the maximum power of any one module. This is true, for example, of the modular approach of Spellman (23, 24) where multiple modules are connected in parallel to generate greater power.

Losses in conventional HVPS may be placed in five categories.

1. Ohmic losses (P_o) in wires, buses, windings, etc. are $P_o = I^2 \times R$.
2. Static losses (P_s) in IGBTs and diodes are $P_s = I \times V_{ON}$.
3. Switching losses (P_{sw}) in IGBTs and diodes are $P_{sw} = 1/6\ f\ (I_{max}\ V_{DS}\ (t_{on} + t_{off}))$.
4. Losses in magnetic core of the HV transformers (P_{MT}) and inductors (P_{MI}) are proportional to $V^{2.6}$, where V = AC voltage across winding.
5. Losses in control circuitry that are assumed unchanged.

Using previous calculations, the following losses for a single transformer 5kW HVPS would result while working on static load.

1. Ohmic losses P_o in wires, buses, windings, etc. are equal to 27.5 + 12.5 + 13.75 + 6.25 = 60W.
2. Static losses P_s in IGBTs and diodes that are equal to 22.9 + 48 + 7.8 + 6.2 + 3.1 = 88W.
3. Switching losses P_{sw} in IGBTs and diodes are equal to 8.4 + 5.4 + 2.9 + 2.9 = 19.6W.
4. Losses in magnetic core in HV transformer P_{MT} and inductor P_{MI} are equal to 22.5 + 11.25 = 33.75W
5. Losses in control circuitry are equal to 12.5 + 6.25 = 18.75W.

This gives total losses of 220.1W for the 5,000W HVPS. The **maximum potential efficiency** of such a HVPS is, therefore, equal to 5,000/(5,000 + 220.1) = 95.8%.

The **efficiency of a HVPS for charging** of a HV capacitor is the ratio of energy spent during each charging cycle to the energy actually accumulated by the HV capacitor. In order to charge a HV capacitor 200nF to 80kV in 5ms with constant current mode as suggested in the Maxwell data sheets, the HVPS should be able to generate 80kV and 3.2A; **i.e. it should be designed for output power of**

256kW, which is substantially larger than any likely IPG HVPS design. Since current remains the same during this charging process, the voltage across the HV capacitor and some of the power components increases in a linear fashion. Extrapolating the losses for the 5kW HVPS above, the losses for a 256kW HVPS are as follows:

1. Ohmic losses P_o do not depend on voltage and are equal to 60 x 256kW/5 = 3,072W.
2. Static losses P_s in IGBTs and diodes that are equal to 88 x 256/5 = 4.505.6W.
3. Switching losses P_{swt} in IGBTs of power inverter are proportional to the voltage. They change from zero (at the beginning of charging process) to 8.4 x 256/5 = 430.08W at the end of the charging process. During the voltage V grow losses are equal to P_{swt} = 1,218.56 x V x t/5 10^{-3}. Voltage across the components of the buck converter is the same. Switching losses in IGBTs of buck converter and diodes P_{swb} are therefore equal to 13.0 x 256/5 = 665.6W.
4. Losses in magnetic core P_{MT} in HV transformer and inductor P_{MT} change from zero (at the beginning of charging process) and 22.5 x 256/5 = 1,152W. During the voltage V grow losses are equal to
$P_{sw} = 1{,}152 \times (V/V_{max})^{2.6} = 1{,}152 \times (t/5 \times 10^{-3})^{2.6}$
Losses P_{MI} in magnetic core of inductor are equal to 11.25 x 256/5 = 576W.
5. Losses in control circuitry P_{cc} are equal to 18.75 x 256/5 = 960W.

Energy wasted during one cycle (5 x 10^{-3} s) of the charging process is a sum of the integrals of all the losses above during this cycle.

a. Ohmic losses energy E_o is equal to 3,072 x 5 x 10^{-3} = 15.36J.
b. Static losses E_s is equal to 4.505.6 x 5 x 10^{-3} = 22.528J.
c. Switching losses E_{swt} in IGBTs are equal to $\int_0^{5 \times 10^{-3}} 552.96\,(t/5 \times 10^{-3})\,dt$ =

= $552.96 \times (5 \times 10^{-3})^2/(5 \times 10^{-3} \times 2) = 1.38$J.
Switching losses in IGBTs of the buck converter and diodes E_{swb} are equal to 665.6 x 5 x 10^{-3} = 3.328J.

d. Losses E_{MT} in HV transformer are equal to $\int_0^{5 \times 10^{-3}} 1{,}152\,(t/5 \times 10^{-3})\,2.6\,dt$ =

= $1.152/(3.6 \times 5 \times 10^{-3})^{2.6} \times (5 \times 10^{-3})^{3.6} = 1.6$J. Losses in inductor E_{MI} are equal to 576 x 5 x 10^{-3} = 2.88J.

e. Losses in control circuitry E_{cc} are equal to 960 x 5 x 10^{-3} = 4.8J.

Total energy loss E_{Total} during one cycle of charging process is equal to the sum of all the above losses, i.e.:
$E_{Total} = \sum E_o + E_s + E_{swt} + E_{swb} + E_{MT} + E_{MI} + E_{cc}$ = 15.36 + 22.528 + 1.38 +3.328 + 1.6 + 2.88 + 4.8 = 51.876J.

A ratio of total energy E_{spent} spent over the charging period to the electric energy stored in the capacitor E_{stored} defines capacitor charging process efficiency $\tilde{\eta}$
$\tilde{\eta} = E_{stored} / E_{spent} = E_{stored} / (E_{stored} + E_{Total})$.
During the charging process electric energy accumulated in the HV capacitor is equal to
$E_{stored} = 0.2 \times 10^{-6} \times 80{,}000^2/2 = 640J.$

Total efficiency of the charging process is equal to 640/(640 + 51.876) = 92.5%. This constitutes more than twice the losses than with the 60 cell IPG HVPS as shown in Table (1). **Therefore, the conventional HVPS is greater capital and operating cost of equipment, a more complex design for cooling, potentially greater component stress and consumes more energy.**

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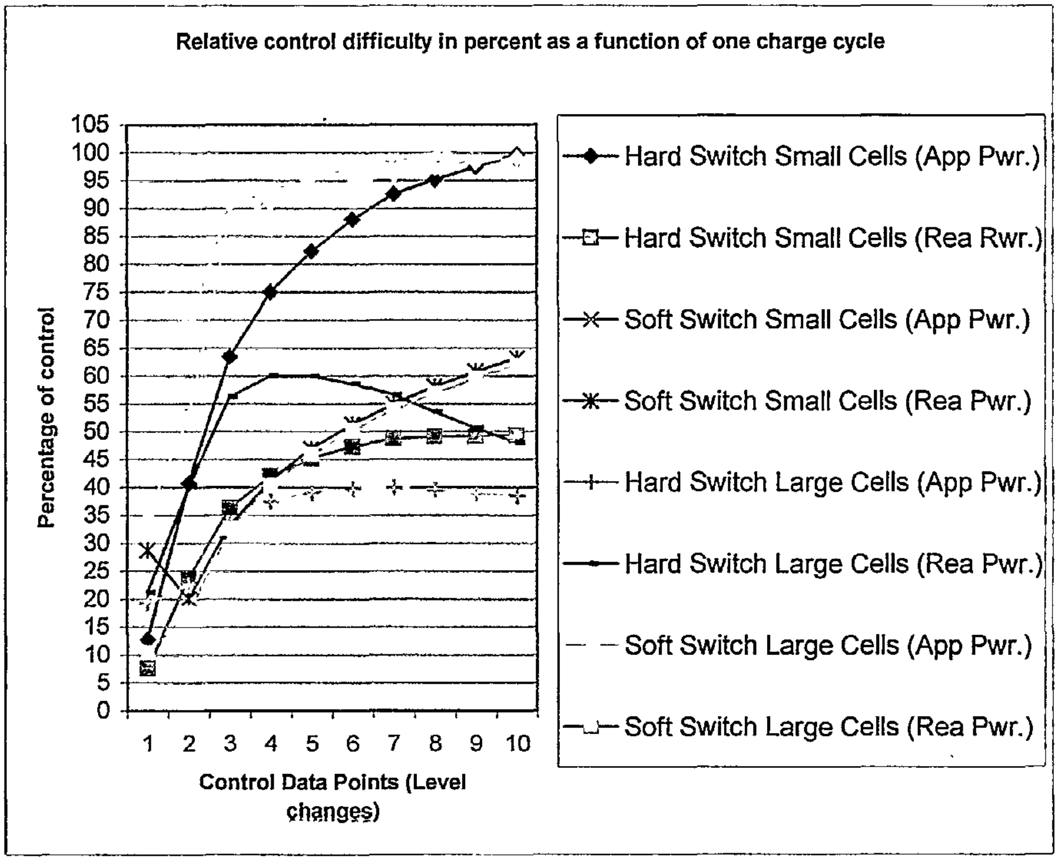
Computer Modeling

Following the extensive theoretical and mathematical analysis performed, the IPG research team performed extensive computer modeling of the PFN, cell types and the previously described cell configurations. The resulting IPG cellular HVPSs were also analyzed based on [and several cellular charging supplies based on] multiple cells of varying output voltage and circuit topology. These models were created using the latest software available, PSPICE in ORCAD v9.1 and Ansoft v5.0 (a very powerful complex analysis program used for such tasks as magnetic and electric field simulation). Multiple computer simulations of the charging process were run using the different modeled cell configurations to charge the PFN model.

Additional modeling of the HV transformer and rectifiers was performed using Ansoft to verify the relationship between the I^2R losses of the secondary windings vs. the V_f losses of the HV diodes. The models compared 10kV windings to 3kV windings over varying loads. The wire guage and diode type, and diode deratings were held constant for all models. The resulting data clearly shows that *combined losses of the windings and diodes may be reduced by using multiples of smaller windings vs fewer larger windings*. This has a direct effect on the overall efficiency of the power supply. The transformer study also included models using one large core vs. three smaller cores with the same power handling capabilities to produce power to the load. The investigation sought to compare the core heating and related core losses in the two models. The results, here, clearly show that the use of multiple smaller cores reduces the overall core losses of the power supply. This also has a direct effect on the overall efficiency of the power supply. It is also obvious that cost of manufacture and materials may either decrease or increase with the increased complexity of maximized number of cores and secondaries. As the volume rises, the price per piece decreases, sometimes very dramatically. This is a significant consideration when considering a higher piece count. Additionally, "smaller" component often means or leads to derating or a lower production cost component. Since cost of the NLC system component (HVPS) is extremely important, further in depth study of cost vs. efficiency has been proposed for the Phase II research.

The following graphical results provide a substantial overview of the research data. Graph 3 is the result of a great deal of complex data analysis and shows the relative difficulty of control of the charging profile comparing 2 topologies, 2 cell sizes (by output voltage), and both reactive power (at the capacitor) and apparent power (at the transformer). The simulation was run for one charging cycle at 180Hz.

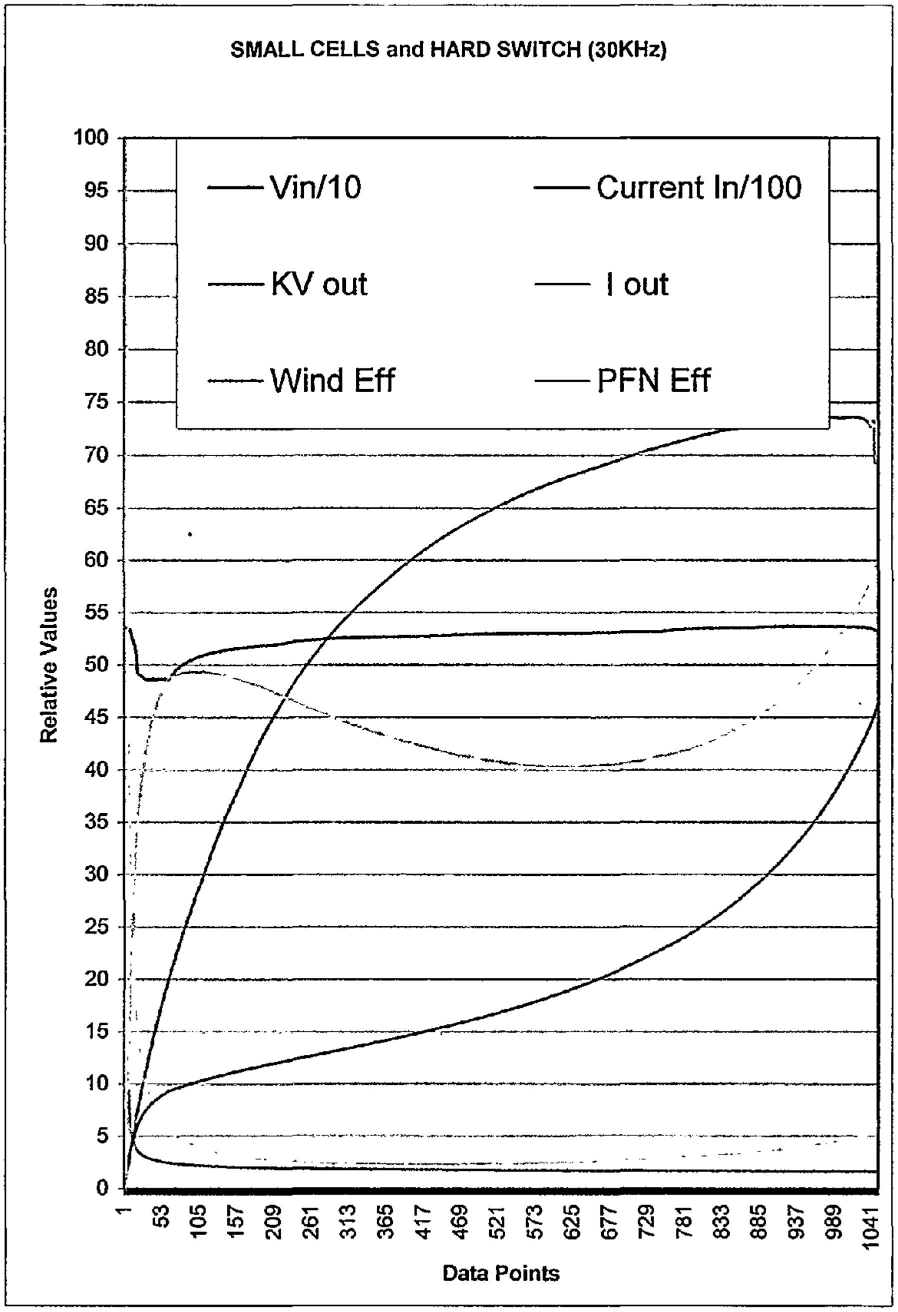


Graph 3: Relative Control Difficulty

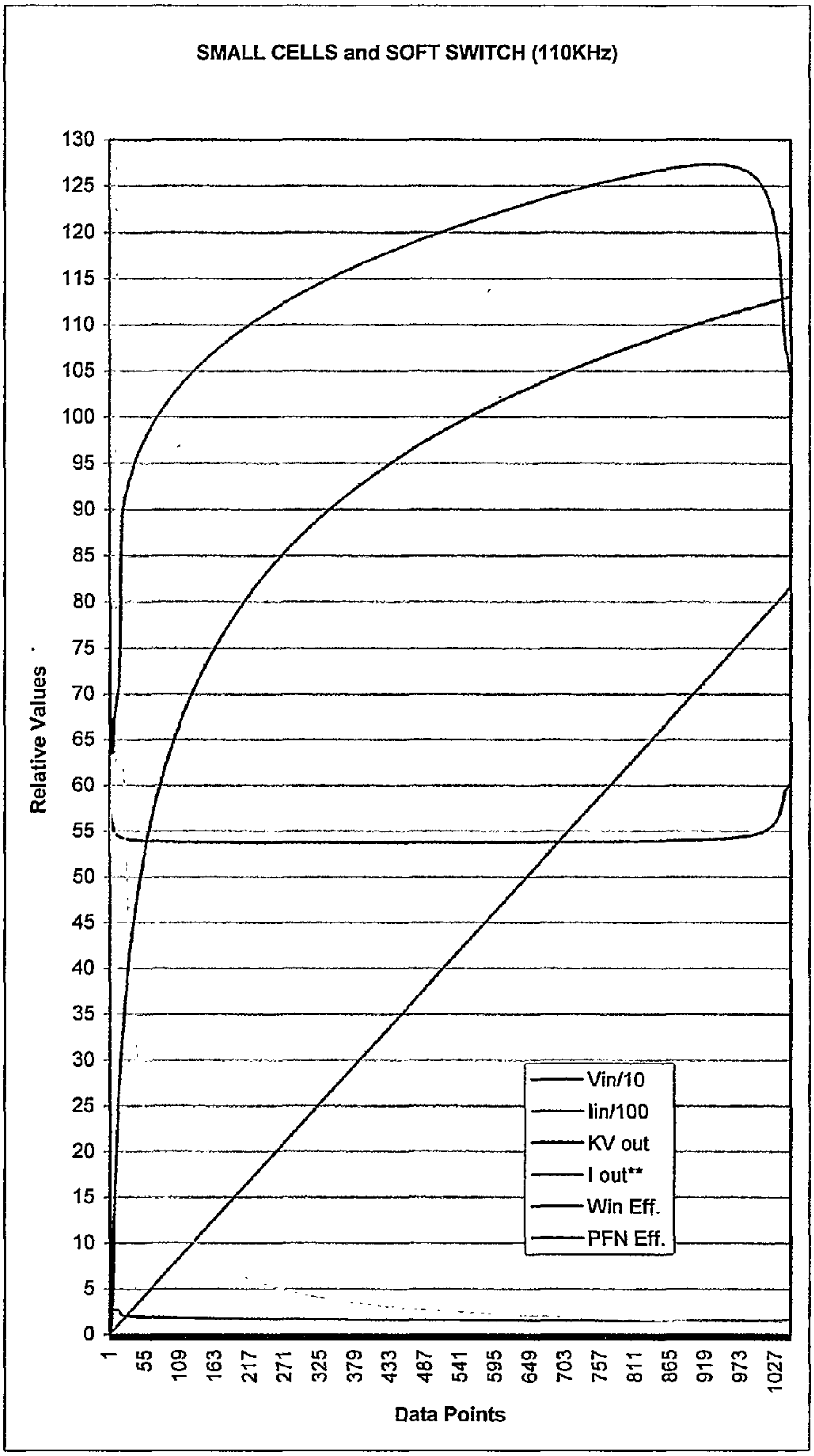
As can be seen, the data suggests that in general, all combinations, except the hard switch large cell, have improved control as the charging cycle progresses. Also, suggested is that the resonant topologies have the best "potential" control (although marginally in some cases), and the hard switch large cell is the least controllable for either the reactive or apparent power. The term "potential" is used because the resonant or soft switch, when compared to the hard switch, has certain inherent limitations that necessitate very careful design of cores and winding for each specific overall HVPS design. For example, the parasitic elements of the transformer play a significant role in the precise operation of the resonant circuit. Control of the phase angle of current and voltage are of particular concern for optimized delivery of power to the load. Designed control of leakage inductances and coupling factors are very critical, perhaps leading to specialized core design. All of these factors will be closely scrutinized in Phase II as stated in that application.

Graphs 4 thru 7 show the simulation of four different cellular HVPSs as they charge the PFN model over a single charging cycle at 180z. The small cells have a 5kVoutput and the large cells a 20kV output. The PFN is modeled as two banks of 10 each 10nF, 80kV Maxwell Technologies capacitors in parallel with

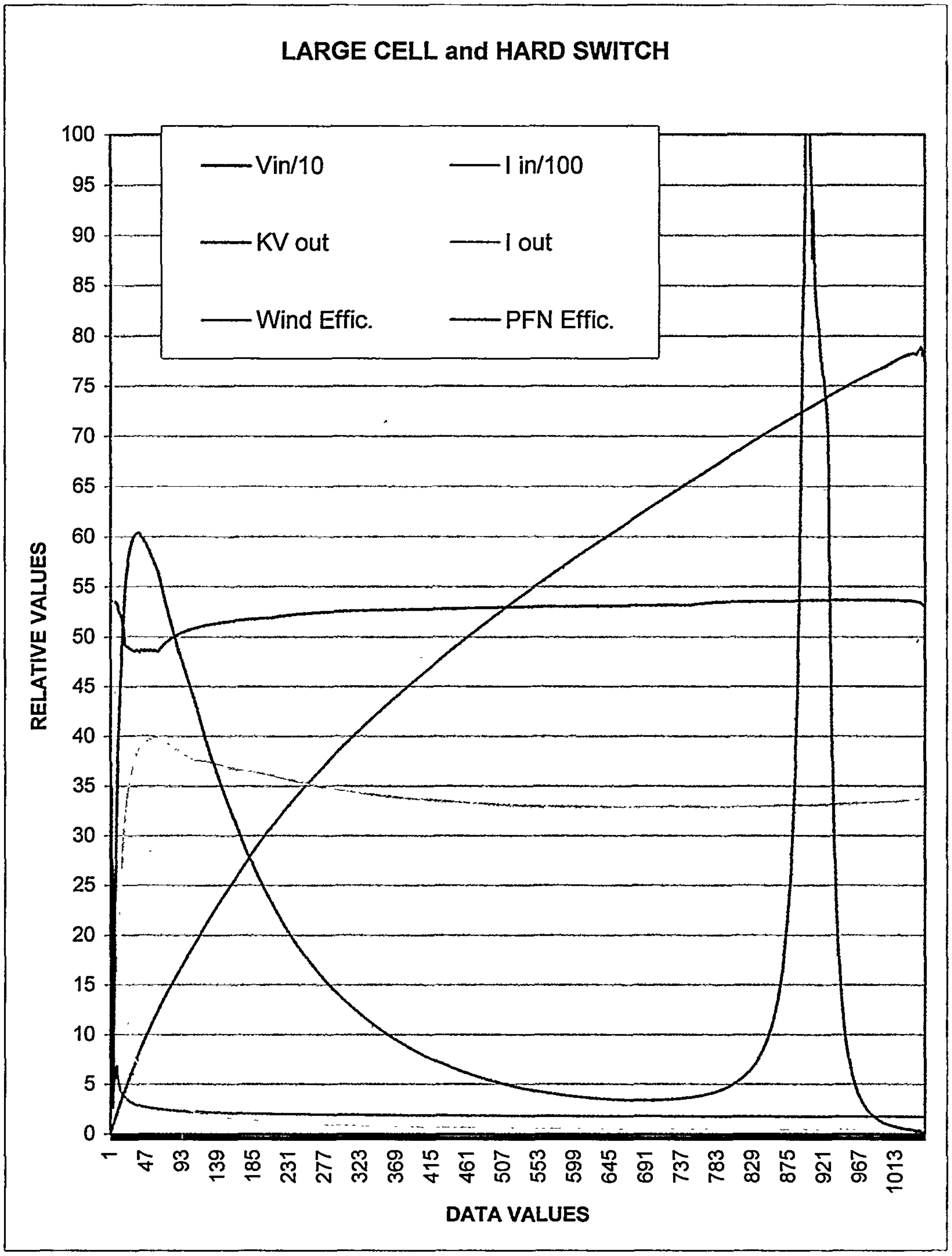
40nH of inductance in series with each bank and 1.47MΩ of resistance across each bank. The two banks are then connected in parallel.



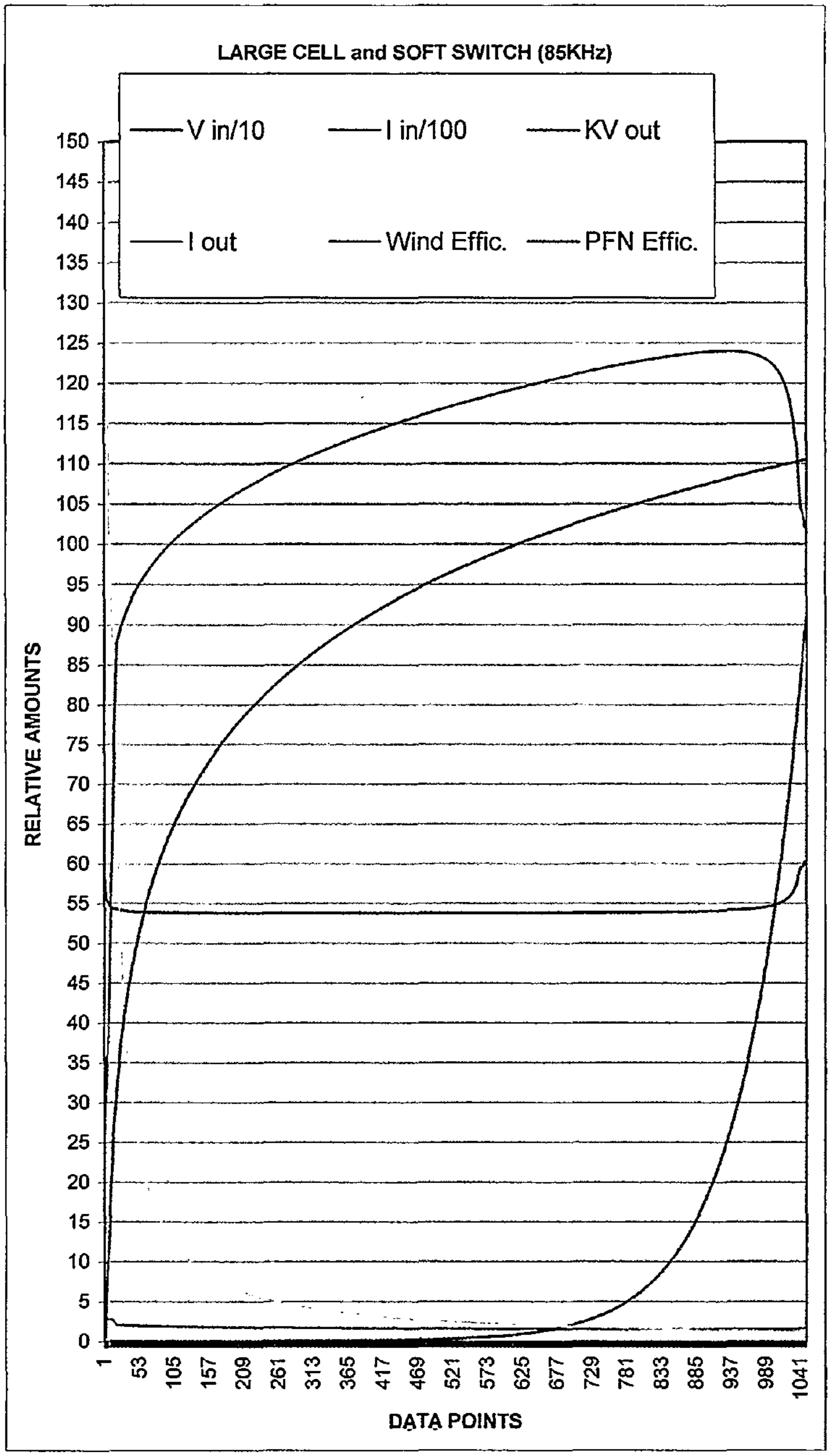
Graph 4: Small Cells and Hard Switch



Graph 5: Small Cells and Soft Switch



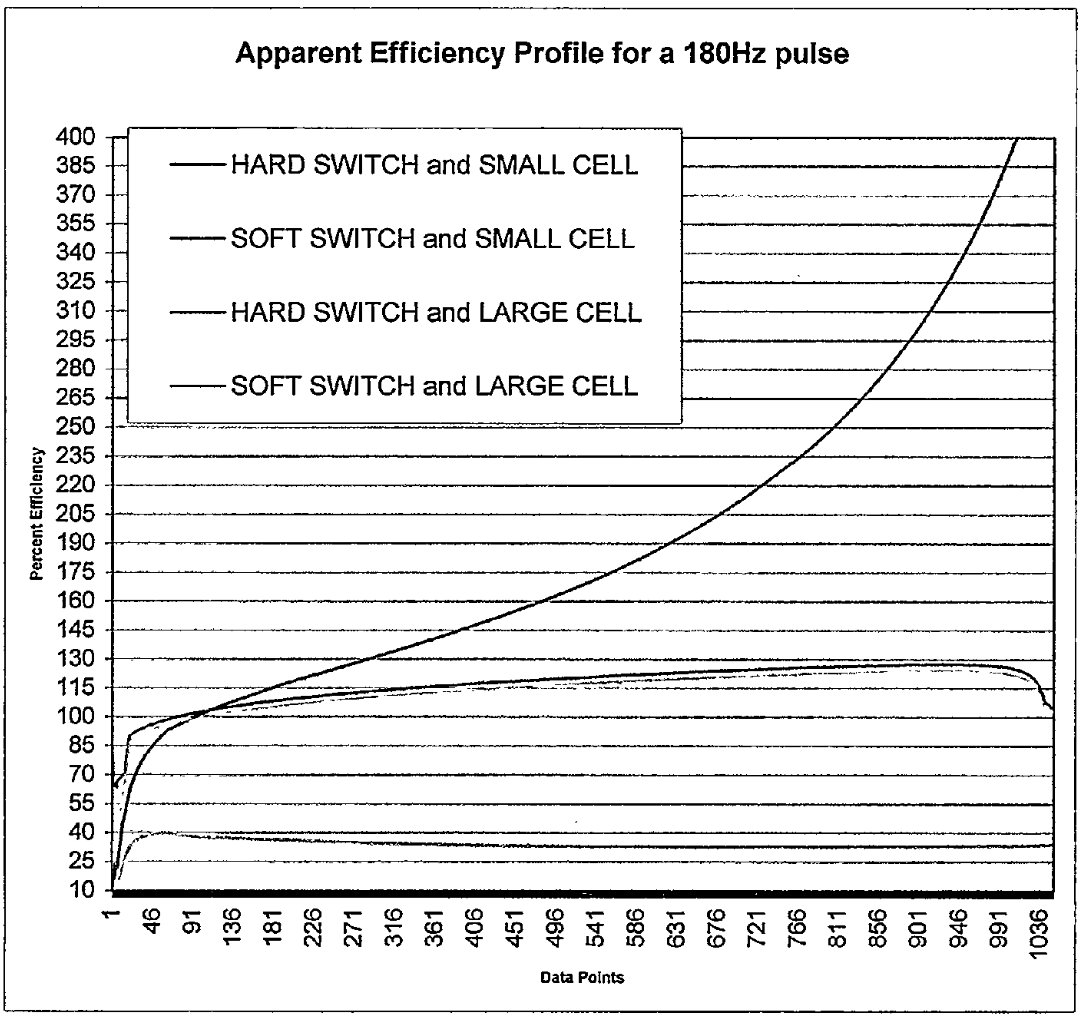
Graph 6: Large Cells and Hard Switch



Graph 7: Large Cells and Soft Switch

The resultant data of interest in each graph is the Input power efficiency, P_{in} Eff., and the efficiency of the PFN, PFN Eff. The data clearly indicates that small cells and soft switch have the highest efficiency in both categories with the small cell hard switch very close, while the large cell and hard switch appears to have the worst efficiency characteristics. The fastest charging rate, based on the "kV out" and "I out", appears to be demonstrated by the large cells and soft switch. Clearly, further research as suggested in the Phase II application is required to fully understand the affects of cell circuit topology and size based on voltage and power on the charging process.

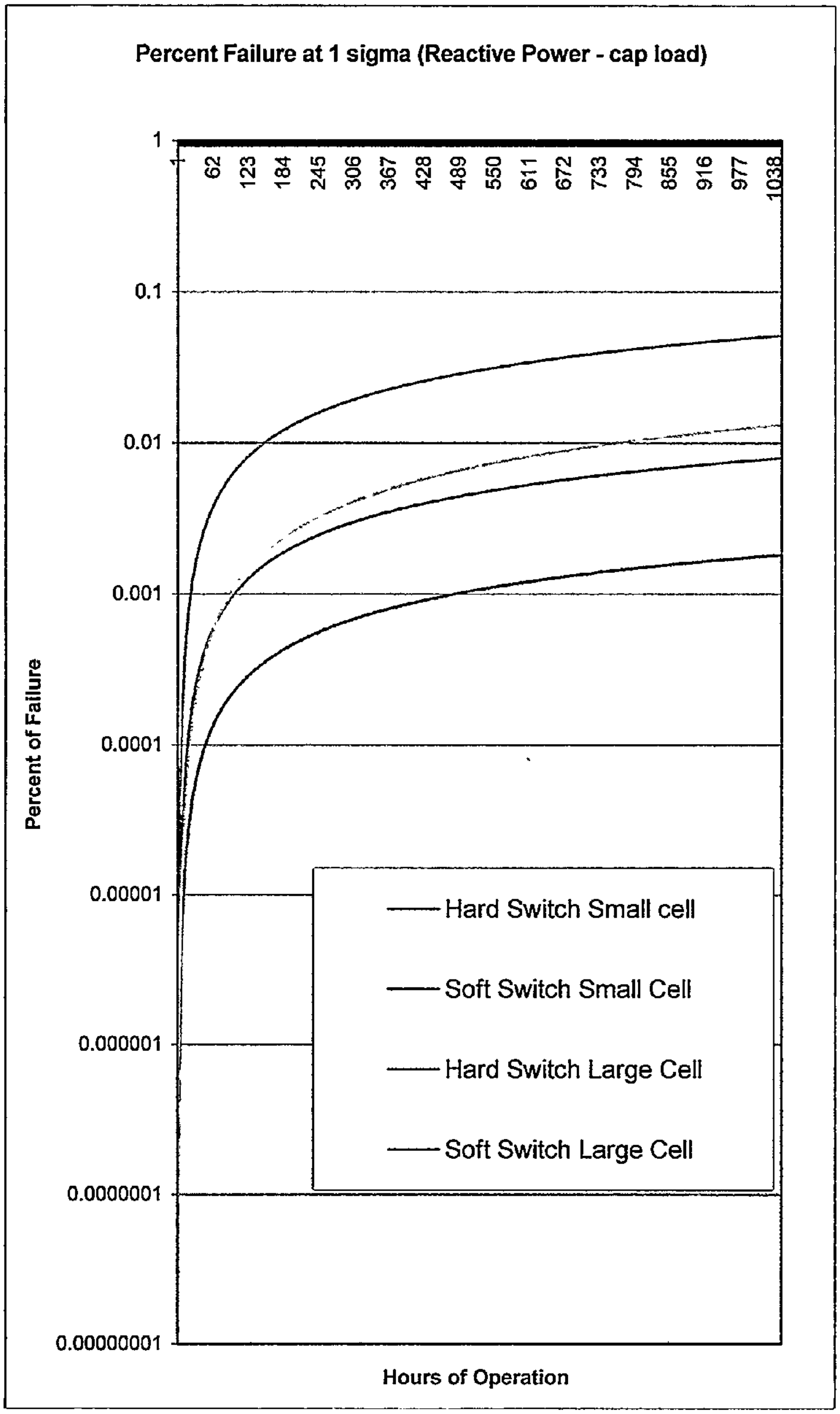
Apparent efficiency over the period of one charging cycle of the four models is shown in Graph 8. It should be noted that the effects of transformer design specifics that tend to vary greatly, have been minimized in the models depicted. The leakage inductance has been held to less than 10% of the total inductance and the coupling factor has been set at 0.95.



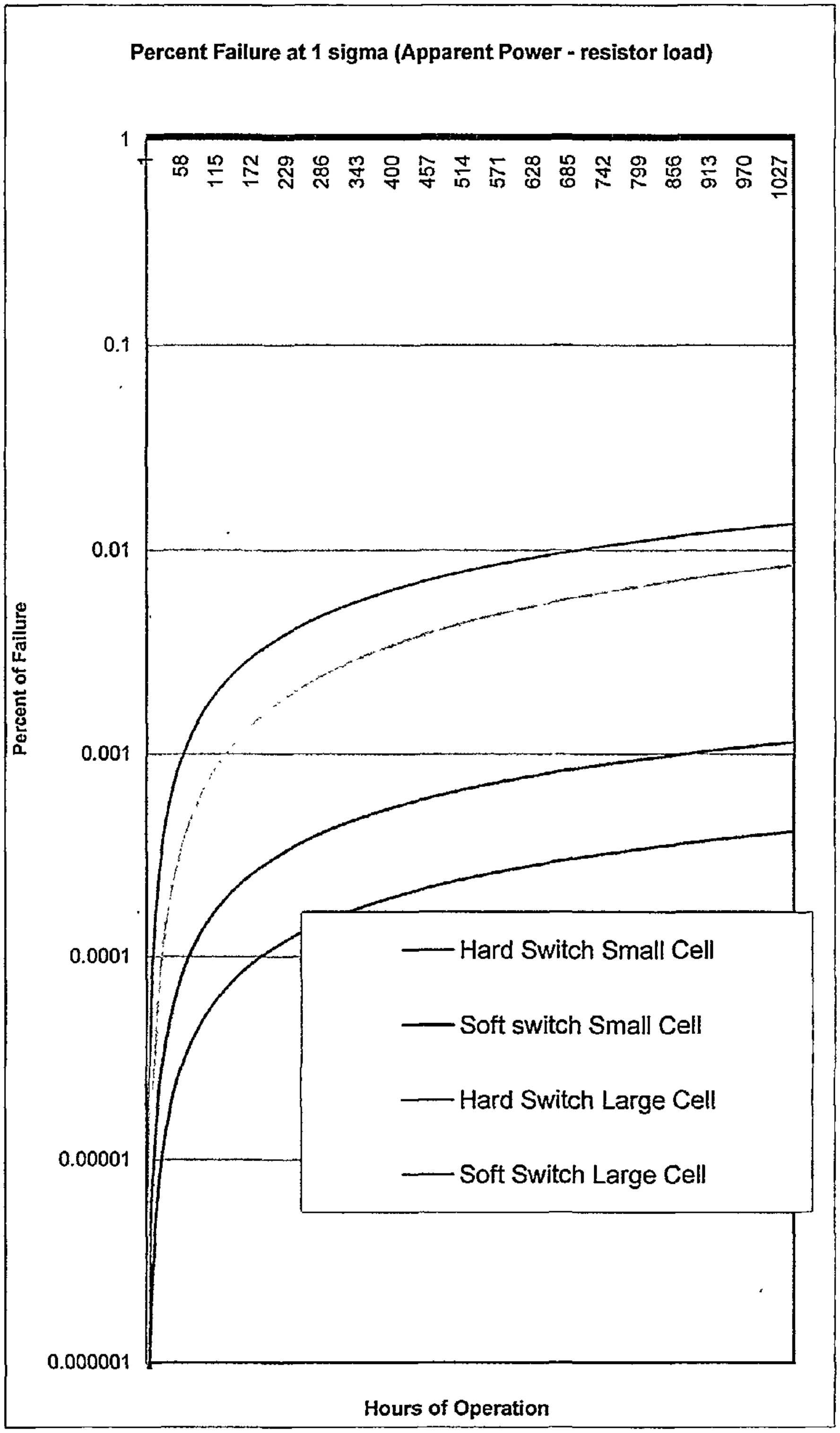
Graph 8: Apparent Efficiency Profile for a 180Hz pulse

It should be noted that all four models appear to be more than 100% efficient after the initial part of the charging cycle. This anomaly is a reflection of the back EMF that occurs as the phase angle between the voltage and current change over the period. The model is limited by the software in that the back EMF cannot be subtracted out and, therefore, actually appears to push the efficiency over 100%. This is particularly true of the small cells and hard switch model in which the phase angles of current and voltage remain fairly constant and in-phase over the period. The best true evaluation of the efficiencies of each of the models is seen at the beginning of the period, to the left of the second data point annotation. The actual efficiencies of the modeled circuits will be greatly affected by the transformer design in terms of core geometry and winding method. The most straight-forward transformer design would be for the small cell and hard switch case. In other words, the core geometry is less critical due to the natural phase angle relationships of the driving topology. However, the small cell and soft switch would likely produce the best results if special care were taken to provide an optimized core geometry and winding methods. This would likely require a special designed core. Therefore, research of these issues and their relative cost of implementation into a production mode are proposed for the Phase II project.

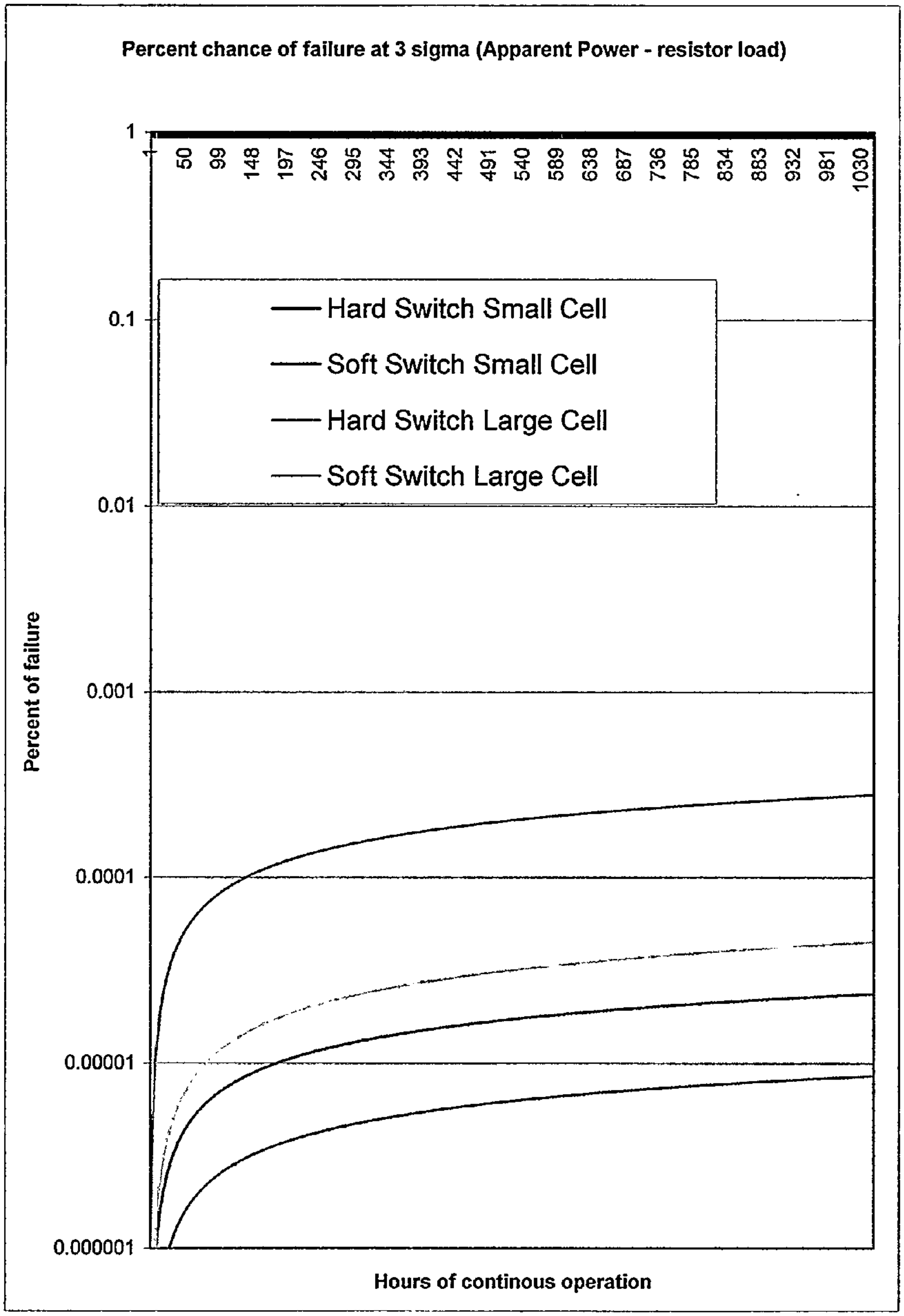
Graphs 9 thru 11 compares failure rates of the four modeled cellular HVPSs. The plots do not take into consideration derating variables for environmental change, power line interruptions and transients, etc. The plots do represent the failure modes of those components that are operating at high levels of constant electrical stress. This is not a reflection of the entire HVPS, as the final design for the NLC application has not yet been identified. Failure rate data was collected from the manufacturers of components considered appropriate for the application.



Graph 9: Percent Failure at 1 Sigma (Reactive Power)

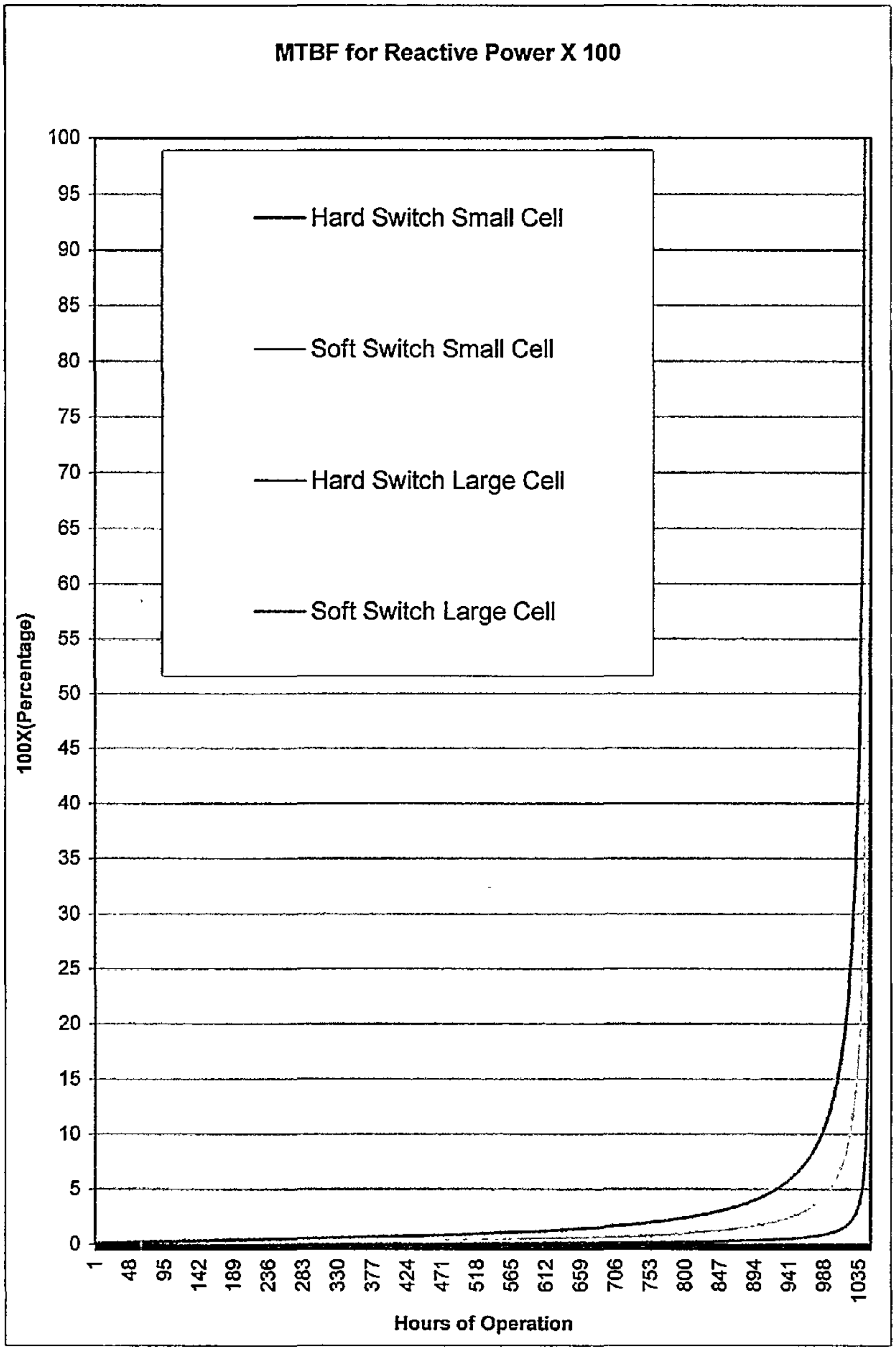


Graph 10: Percent Failure at 1 Sigma (Apparent Power)

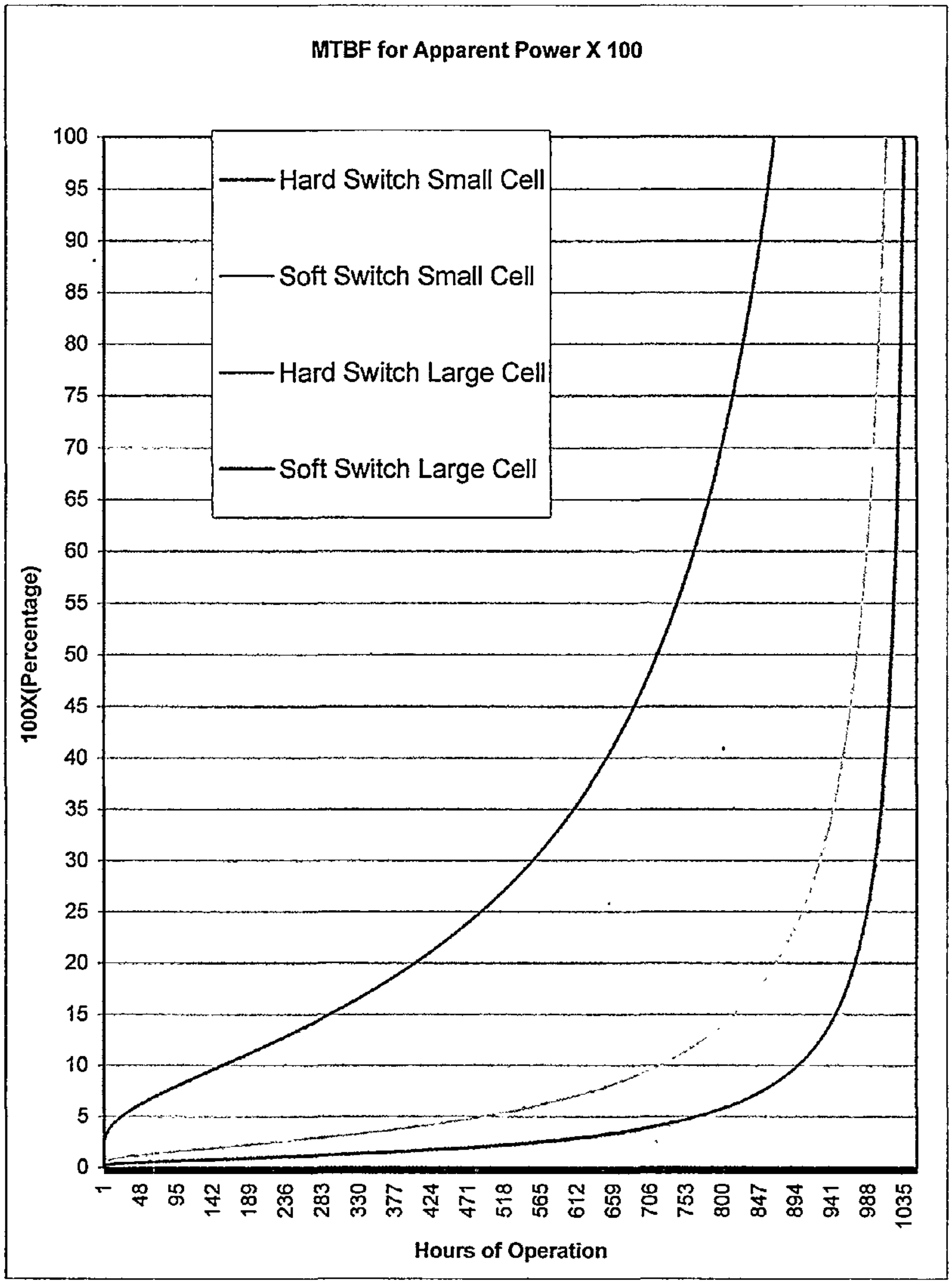


Graph 11: Percent Failure at 3 Sigma (apparent Power)

Graphs 12 and 13 show relative MTBF of the four modeled HVPSs.



Graph 12: MTBF for Reactive Power X100



Graph 13: MTBF for Apparent Power X100

The previous five graphs consistently indicate that the smaller cell size tends to produce lower failure rates and higher MTBF numbers. However, there is likely to be a point at which further reduction of cell size and increased quantity of cells in a given supply may prove to be cost sensitive. This, along with the wide variation of requirements in the marketplace, suggests that more in depth analysis of these relationships needs to be pursued as proposed in the Phase II application.

Section III Proof of Feasibility, Success and Recommendations for the Conduct of Phase II

Applicant has determined that actual development of an appropriate IPG HVPS is feasible and can meet the requirements for the new NLC. In the performance in the previously described tasks, **all objectives were met.** The technical objectives, which focused upon the development of an ideal HVPS for the NLC resulted in the conclusion that **more than one configuration and topology will meet the stated needs.** The questions posed and the answers derived through the Phase I research are basically as follows:

1. What is the ideal charging ramp? It is a constant power charge, which can be achieved efficiently through more than a single cellular configuration and circuit topology.
2. How many cells are responsibly required? Based on the research to date, the number of cells is likely to be between forty (40) and sixty (60) depending upon the switching topology and cost. The data, from an efficiency point of view, suggest a resonant "small cell" design of approximately forty (40) cells configured as follows: Each cell of a nominal 5kV output voltage with four columns or Levels. Level 1, the column that provides current throughout the charging process, contains sixteen (16) cells in series. Level 2 contains twelve (12) cells in series, Level 3 contains eight (8) cells in series, and Level four, which provides current only during the first stage of the charging process, would contain 4 cells in series. This does not include redundant cells to address the n+1 method for improving the HVPS reliability. This issue will be resolved based on the further study in Phase II of a potential "cross-over" cell.

3. What are the most reliable and cost effective components? In general, a wide range of reliable components is available with component selection likely to improve given the length of time before the NLC project actually commences. The cost effective strategy in component selection is a function of a power supply design that reduces component stress and avoids high performance and high cost components particularly with respect to diodes, IGBT's and/or FETs. Additionally, the transformer core design and core material are critical.

4. What is the best cell efficiency over the charging time? Extensive modeling demonstrated that the best cell efficiency over the typical operating period of the charging cycle ranged between 93% and 96%. However, testing of actual varying cell sizes/outputs, as proposed in the application for Phase II, will produce precise efficiency numbers, which are not expected to vary greatly from the modeled numbers assuming high quality materials and precision design.

5. What are the transformer losses? For the transformers selected, the exact quantitative losses for the high voltage transformer are a function of the final design chosen based upon the final decision of cell size and circuit topology. Based upon the results of the studies performed in Phase I, it is apparent that the transformer losses will be no greater than 1% of the transformer output power. The data also suggests that there is a direct relationship between cell size and such losses.

6. What is the best trade-off position regarding efficiency, uniform power consumption, cost and size? Simply stated, more than a single sized cell will produce a "best" position. Much depends on how these factors are weighted by the NLC. In general terms, it appears that a cell size ranging from 3.3 kV to 5 kV produces results, considering all these variables, that are far superior to cell sizes which are either smaller or larger.

7. What is the most efficient number of "redundant" cells to use for HVPS reliability versus cost? A redundant cell at the top of each parallel stack of cells is the minimum according to the studies performed. However, another method of creating redundancy is purposed in Phase II with that method potentially further reducing the number of redundant cells.

8. What is the most reasonable HVPS topology for the linear colliders most efficient performance? Initial findings suggested the hard switch approach to the HVPS design, and the brass board prototype utilized a hard switch topology. However, subsequent data suggests that a series resonant switch method may prove more reliable and cost effective with only a very slight difference in charging performance and overall operating efficiency.

While not all results achieved were consistent with original estimates as to the particular topology, it is clear from the study that the IPG power supply can meet the NLC requirement utilizing several possible configurations and either hard or soft (resonant) switching topology. The study results did make clear certain conclusions respecting cell size and circuit topology as they relate to over all efficiency, component cost and reliability. The modeling and simulations of the charging process made clear that the IPG cellular concept for a capacitor charging HVPS is far superior to the typical or conventional single transformer, single inverter designs in providing the most efficient charging process possible. The modeling also made clear that the MTBF of the cellular supply is at least equal to a conventional supply, but the ability to utilize internal redundancy creates a form of reliability not previously available in power supply design.

Further design research into alternative methods of redundancy may prove important and are proposed in the Phase II application. The transformer modeling and analysis confirmed that multiples of small transformers with multiple small secondary windings is potentially the most efficient and effective design. Truly, the versatility, applicability and superiority of the cellular approach has been made very evident from the research performed.