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Direct-Cooled Power Electronics Substrate

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Direct-Cooled Power Electronics Substrate

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LIST OF ACRONYMS

°C	degrees Celsius
°C/W	degrees Celsius per Watt
µm	micro-meter
AlN	aluminum nitride
Al_2O_3	aluminum oxide or alumina
BeO	beryllium oxide
CARES	Ceramic Analysis and Reliability Evaluation of Structures
DBC	direct bonded copper
EG	ethylene glycol
FEA	finite element analysis
GPM	gallons per minute
HEV	hybrid electric vehicle
ICE	internal combustion engine
IGBT	insulated gate bipolar transistor
kg	kilogram
kg/m^3	kilogram per cubic meter
kW	kilowatt
MPa	mega Pascal
OEMs	original equipment manufacturers
PHEV	plug-in hybrid electric vehicles
psig	pounds per square inch gauge
POS	probability of survival
Si_3N_4	silicon nitride
SiC	silicon carbide
TIM	thermal interface material
W	Watt
W/mK	Watts per meter Kelvin
WEG	water-ethylene glycol

ABSTRACT

The goal of the Direct-Cooled Power Electronics Substrate project is to reduce the size and weight of the heat sink for power electronics used in hybrid electric vehicles (HEVs) and plug-in hybrid electric vehicles (PHEVs). The concept proposed in this project was to develop an innovative power electronics mounting structure, model it, and perform both thermal and mechanical finite-element analysis (FEA). This concept involved integrating cooling channels within the direct-bonded copper (DBC) substrate and strategically locating these channels underneath the power electronic devices. This arrangement would then be directly cooled by water-ethylene glycol (WEG), essentially eliminating the conventional heat sink and associated heat flow path.

The concept was evaluated to determine its manufacturability, its compatibility with WEG, and the potential to reduce size and weight while directly cooling the DBC and associated electronics with a coolant temperature of 105ºC. This concept does not provide direct cooling to the electronics, only direct cooling inside the DBC substrate itself. These designs will take into account issues such as containment of the fluid (separation from the electronics) and synergy with the whole power inverter design architecture.

In FY 2008, mechanical modeling of substrate and inverter core designs as well as thermal and mechanical stress FEA modeling of the substrate designs was performed, along with research into manufacturing capabilities and methods that will support the substrate designs. In FY 2009, a preferred design(s) will be fabricated and laboratory validation testing will be completed. In FY 2010, based on the previous years laboratory testing, the mechanical design will be modified and the next generation will be built and tested in an operating inverter prototype.

1.0 INTRODUCTION

As consumer interest grows in hybrid electric vehicles (HEVs) and plug-in hybrid electric vehicles (PHEVs), original equipment manufacturers (OEMs) are challenged to offer these technologies at reduced costs. The automotive manufacturer's goal is to reduce the price of these vehicles relative to the cost of traditional internal combustion engine (ICE) powered vehicles. Thermal management of the power electronic systems that must be implemented into these products constitutes a large cost to both manufacturers and consumers. Currently, HEVs utilize two cooling loops. One cooling loop is for the ICE, which operates at approximately 105°C, and a second is for the power electronics modules, which operates near 70°C. One way to significantly reduce the cost to both manufacturers and consumers is to only use a single coolant loop for both the ICE and power electronics using 105°C coolant as the primary means of heat dissipation.

Current HEV products containing power modules and state-of-the-art inverters are based on chip and wire assembly and direct-bonded copper (DBC) on flat ceramic substrates. The unidirectional heat flow path for this type of packaging includes the power electronics (silicon die), solder joint, DBC, base plate, thermal paste or grease, and final heat sink. These are traditionally packaged within a housing and then commonly encapsulated with silicone gels for protection. The many layers involved in the typical package contribute to a large overall thermal resistance between the chip junction and the heat sink, but the major thermal conduction limiter is the thermal grease or other thermal interface material (TIM).

The purpose of this research and development project is to design a direct-cooled power electronics substrate that would enable automotive manufacturers to use solely 105°C coolant thus eliminating the secondary coolant loop. Thermal performance and mechanical stress finite-element analyses (FEAs) were performed on design concepts to ensure they satisfied the design criteria for material strength and thermal heat dissipation. Surveys were also performed on manufacturer's capabilities and methods supporting the substrate design and fabrication.

2.0 CANDIDATE PROCESSING METHODS AND MATERIALS FOR A DIRECT-COOLED POWER ELECTRONICS SUBSTRATE

A need for sufficient cooling of automotive power electronics using 105°C water-ethylene glycol (WEG) is becoming a reality. This creates a small window for successful cooling because the junction temperature of the silicon insulated gate bipolar transistors (IGBTs) and diodes cannot exceed a peak value of 175°C or a continuous temperature of 150°C. Alternative cooling strategies must be considered to enable cooling of the inverter with 105°C WEG. One involves positioning the 105°C cooling as close to the IGBT and diode as possible through the use of a (electrically insulating) ceramic heat exchanger.

A heat exchanger concept involving the use of a ceramic is the focus of this research effort. An illustration of this concept is shown in Fig. 1, along with a computer rendering of one of the heat exchangers and a machined prototype shown in Fig. 2. Additional concepts involve the use of foam inserted into the coolant channel to act as a thermal conductivity enhancer. Note that the concept shown (in Fig. 1) also uses a metal foam insert in the four flow channels. In any design case, the ceramic in the heat exchanger would serve the same primary role as a ceramic in a conventional DBC, namely an electrical insulator. The substrate would then be metalized with copper to facilitate bonding (e.g., soldering or sintering) to a silicon IGBT and diode.

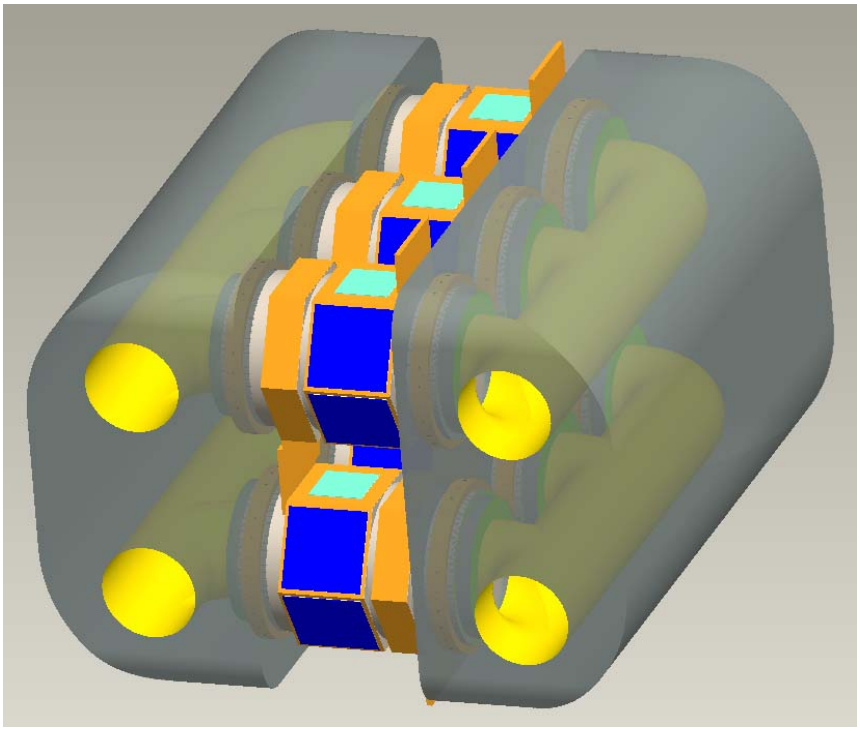

Fig. 1. Conceptual rendering of a direct-cooled power electronic substrate. Six ceramic heat exchangers would provide sustained cooling to 24 IGBTs and 12 diodes.

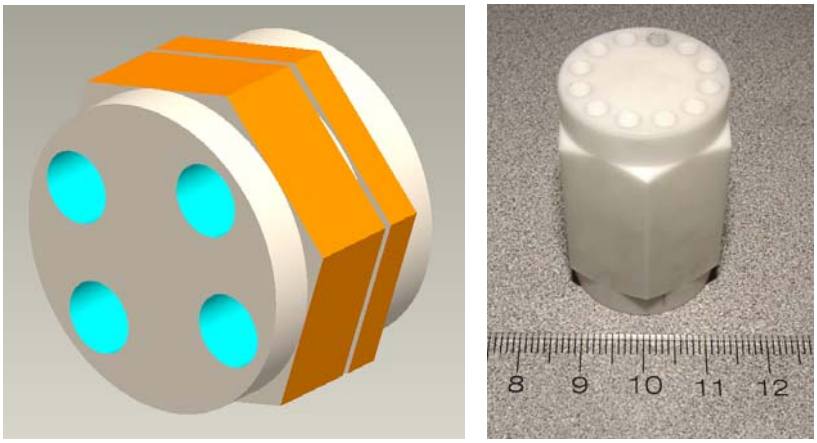

Fig. 2. Conceptual rendering of the hexagonally shaped substrate (left) and photograph of a machined prototype (right).

The following sections describe current state-of-the-art processing methods that satisfy the fabrication requirements as well as candidate ceramic materials.

2.1 CERAMIC PROCESSING METHODS

Ceramic processing methods were identified that could be used to produce a direct-cooled DBC. The manufacturing techniques should combine two characteristics: they should be capable of producing small-scale features (e.g., hole diameters of 1 mm [0.040 in.] or less) in a structure up to 50 mm in length and be mature processes capable of large-scale manufacturing applicable to the automotive industry. Four identified ceramic processing methods described in the following sections are considered to be "green-state" fabrication techniques; that is, they are methods that form processed ceramic powder into some desired shape at or near ambient temperature. Their attributes are compared in Table 1.

Table 1. Comparison of candidate ceramic processing methods for a direct-cooled power electronic substrate

Method	Mature	Mass production capability	Many companies use?	Complex shapes and fine features?
Dry pressing	X	X	X	
Extrusion	X	X	X	
Injection molding	X	X		X
"Ceramatec process" tape casting + laser machining + lamination	X			X

The "green-processed" component is ultimately sintered (i.e., a solid-state densification process) to final density at elevated temperatures. For ceramics under consideration for this heat exchanger application, sintering temperatures of 1300°C (2300°F) or higher probably would be required. The sintering stage and method are largely independent of the green-state processing method, so their details are not discussed here.

2.1.1 Dry Pressing

Dry pressing is one of the most traditional ceramic processing methods. Its advantages are that most ceramic manufacturers are adept at it, it is a mature technology, it is relatively inexpensive, and it is amenable for mass production. Ceramic powder is blended with organics; a die is filled with the powder blend and then uniaxially pressed. Dry pressing by itself could not produce the shape shown in Fig. 2, so manufacturers would perform green-state machining of the dry pressed billet to promote that hexagonal shape and to incorporate the flow channels. Green-state machining is attractive because conventional grinding and machining tools can be used whereas (expensive) diamond tooling is required for machining after a ceramic has been sintered. The sintering process reduces the size of the green-state shape, but manufacturers can accurately take that into account because they are aware of how much reduction occurs for a given ceramic material. The disadvantage of this method is that the architecture may be limited by what can be accomplished during green-state machining; for example, very small thru-hole diameters (e.g., 1 mm [0.040 in.]) may be difficult to produce in the ceramic's green-state and maintain through the sintering process.

2.1.2 Extrusion

Extrusion is another traditional ceramic processing method. Like dry pressing, its advantages are that many ceramic manufacturers are experienced with it, it is a mature technology, it is relatively inexpensive, and it is amenable for mass production. Ceramic powder is blended with organics to make a plastic body that is then pressurized and forced to pass through a die of the desired cross-section. Like dry pressing, extrusion by itself would not be able to produce the shape shown in Fig. 2; green-state machining would be needed, so fine-scale-features of the final architecture could be limited.

2.1.3 Injection Molding

Injection molding can achieve high precision ceramic parts (e.g., ± 25 μm = ± 0.001 in.) having small or large size, high production volumes (tens of thousands to millions), an almost infinite variety of designs, low labor requirements, and low costs. Another advantage to injection molding is that machining costs can often be eliminated (certainly minimized) once dies and tooling have been optimized. It does not have the limitations inherent to green-state machining of dry-pressed or extruded billets; internal features are not limited by symmetry and can be very complex if desired. For example, a helical pattern can be incorporated in a channel to better promote turbulent flow of a WEG. Examples of the fine architectures achievable with ceramic injection molding are shown in Fig. 3.

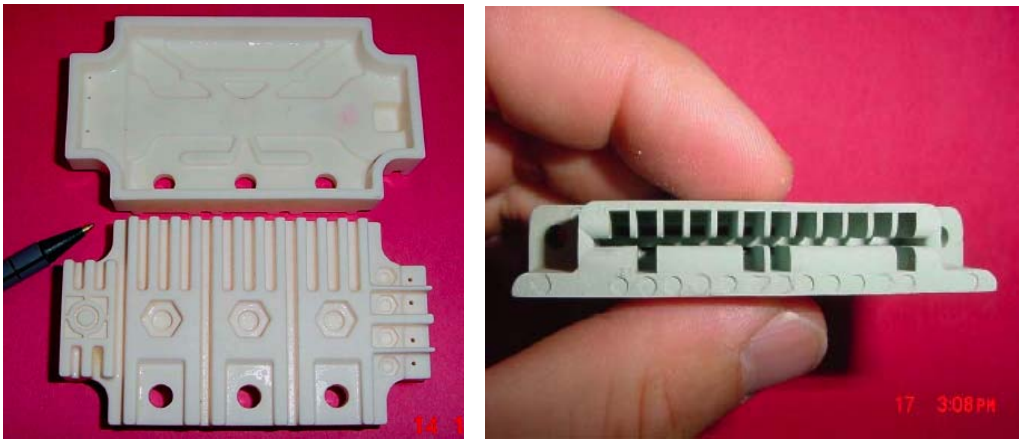

Fig. 3. Examples of ceramic injection molded parts and the fine features that can be achieved. Aluminum oxide IGBT cover (left) and silicon carbide (SiC) electronic part (right). [Images provided by Springboard Ceramic Injection Molding, Pittsfield, MA].

2.1.4 Ceramatec Process

The Ceramatec process combines tape casting, laser machining of the green tapes, and lamination to produce ceramic components with complex internal channels. Fine tolerances can be achieved, and the process is mature and under consideration for a wide range of ion transport membrane technologies. Large dimensions are achievable in two of the three dimensions. The mass production capabilities of this process are not as good as for dry pressing, extrusion, or injection molding (Fig. 4).

Fig. 4. Examples of fine-scale ceramic architectures fabricated by the Ceramatec process. Laminated ion transport membrane (left) and laminated ceramic solid oxide fuel cell structure (right). [Images provided by M. Ferber, Ceramatec, Salt Lake City, UT].

3.0 DETERMINE THE OPTIMUM CERAMIC MATERIAL FOR MAXIMUM HEAT TRANSFER

Ceramic materials were sought that combined: electrical insulation (> 10^9 ohm•cm), the potential to be chemically compatible with WEG, good thermal conductivity (> 50 W/mK), modest tensile strength (> 200 MPa), and minimum cost and that could be processed by any of the four methods described earlier. A summary of several candidate ceramics is shown in Table 2.

Table 2. Comparison of candidate ceramic materials for a direct-cooled power electronic substrate

Candidate ceramic	Electrical insulation	Thermal conductivity	Cost	Chemical Compatibility with WEG
Aluminum oxide or alumina (Al_2O_3)	Excellent	Fair	Low	Unknown but probably good
Aluminum nitride (AlN)	Excellent	Excellent	High	Unknown
Silicon Nitride (Si_3N_4)	Excellent	Fair to good	High	Unknown
High resistivity polycrystalline SiC	Potentially excellent	Good to excellent	Medium to high	Unknown
Beryllium oxide (BeO)	Excellent	Excellent	Medium	Unknown

Some of the candidate ceramic materials are documented [1,2] as being unstable in contact with moisture. The thermal cycling of the material may introduce fatigue when it is in contact with WEG, so a series of strength and fatigue tests were begun on AlN, Al_2O_3, Si_3N_4, and SiC after they were immersed in and impinged with WEG. Preliminary indications were that none of the materials had a dramatic decrease in strength from contact with WEG; however, scanning electron microscopy of ceramic surfaces subjected to WEG impingement for 590 hours showed that erosion was occurring probably because of a chemical reaction between the AlN and WEG (see Fig. 5). Longer-term studies are continuing. Additionally, electrical resistivity tests were completed on the designated ceramic candidates at 25, 200, and 325°C. The results of the electrical resistivity tests are shown in Figs. 6–9.

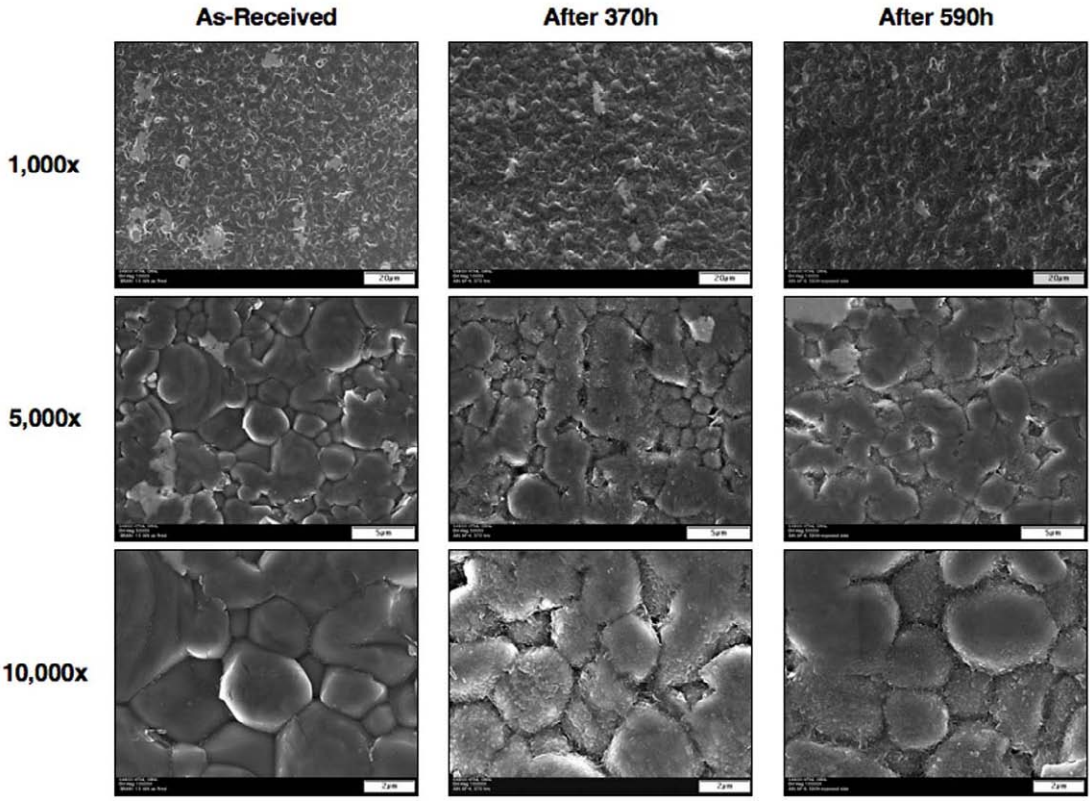

Fig. 5. WEG impingement on AlN surface shows evidence of chemical reaction. Such a reaction can enable erosion.

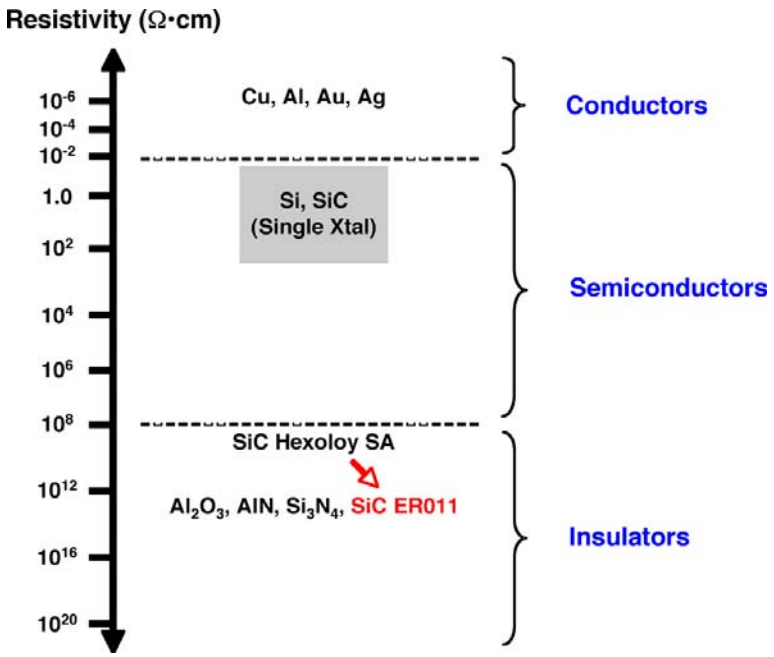

Fig. 6. Electrical resistivity domains.

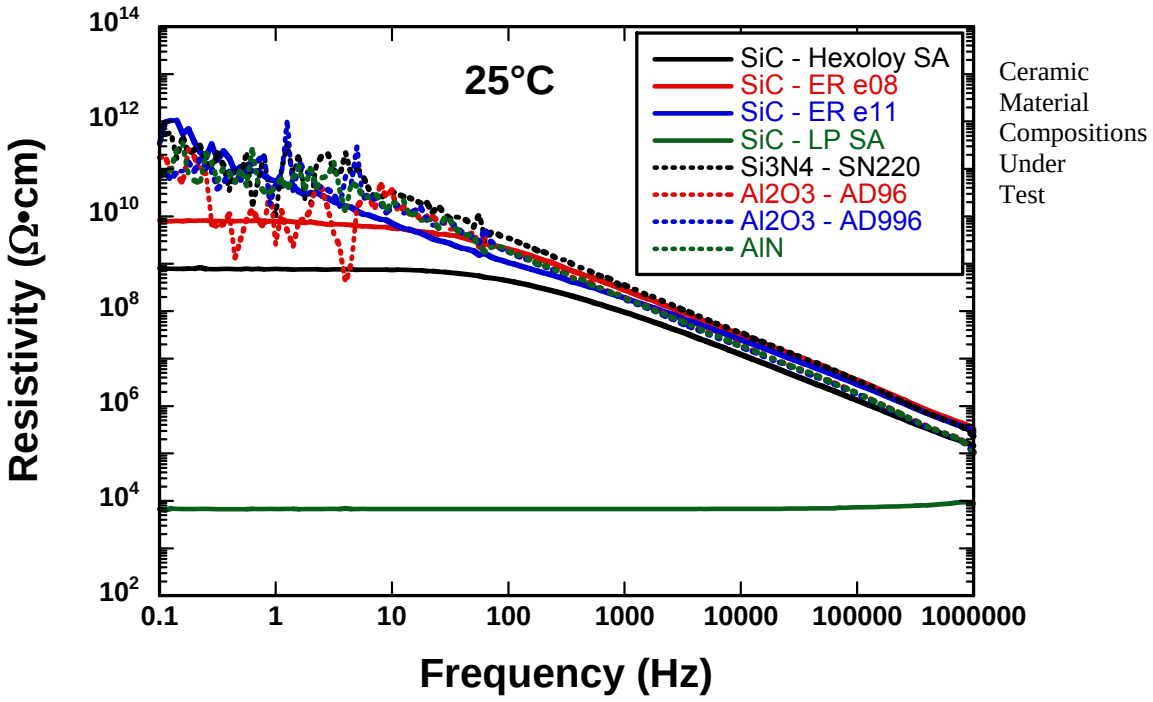

Fig. 7. Electrical resistivity of candidate ceramic materials at 25°C.

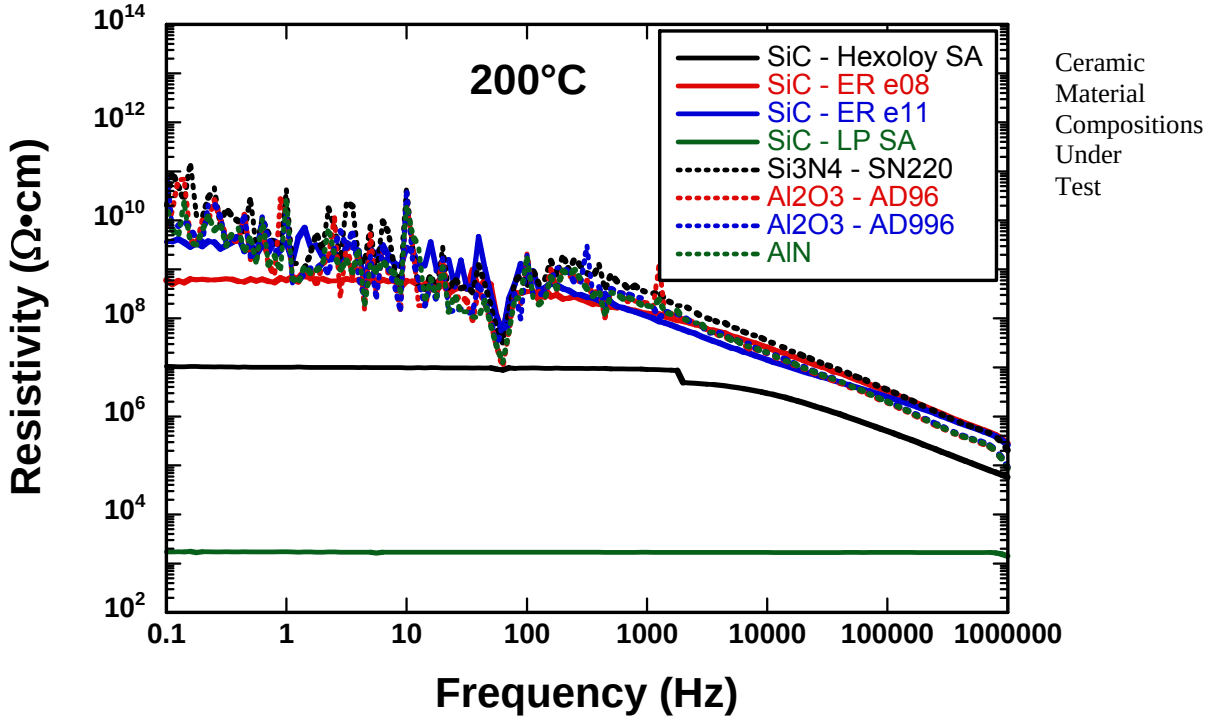

Fig. 8. Electrical resistivity of candidate ceramic materials at 200°C.

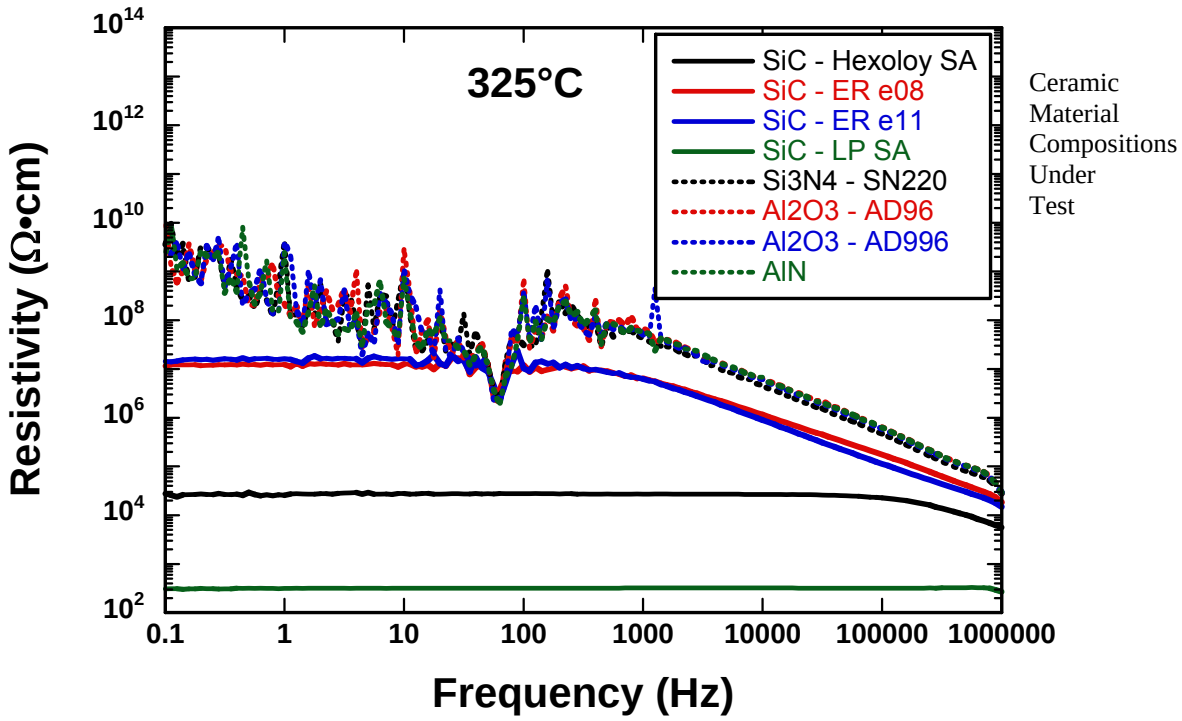

Fig. 9. Electrical resistivity of candidate ceramic materials at 325°C.

A list of candidate ceramic manufacturers is provided in Table 3. All have large-scale ceramic manufacturing capabilities, presently have sizeable ceramic markets, and could satisfactorily manufacture a heat exchanger like that shown in Fig. 2. All were contacted about the heat exchanger concept, and its manufacturability was discussed.

Table 3. Candidate ceramic manufacturers for the direct-cooled power electronic substrate

Company	Where located?	Ceramics
ACR	Tucson, AZ	Al_2O_3, AlN, Si_3N_4
Brush Ceramic Products	Tucson, AZ	BeO
BAE Ceramics (Cercom)	Vista, CA	Al_2O_3, AlN, SiC
Ceradyne	Costa Mesa, CA	Al_2O_3, AlN, Si_3N_4, SiC
Ceramatec	Salt Lake City, UT	Al_2O_3, AlN, Si_3N_4
CoorsTek	Golden, CO	Al_2O_3
Kennametal	Latrobe, PA	Si_3N_4
Kyocera	Japan	Si_3N_4
Saint-Gobain	Niagara Falls, NY	SiC
Springboard CIM	Pittsfield, MA	Al_2O_3, AlN, Si_3N_4, SiC

4.0 DESIGN SELECTION

4.1 SELECT CHIP SETS THAT WILL MEET THE INVERTER POWER REQUIREMENT

A silicon device's primary rating is its current-voltage (I-V) characteristics that dictate how much current the device can conduct at the expense of a forward voltage drop. For IGBTs, these curves depend on the applied gate voltage and junction temperature. For diodes, the characteristic curves are temperature dependent. Likewise the junction temperature of the device is dependent on the packaging and the heat removal rate.

It was determined that a device can conduct rated current up to its maximum rated junction temperature as long as the waste heat being produced is consistently removed. The typical junction-to-case resistance noted in the device literature can involve many internal layers. The thermal efficiency of a multilayered structure is only as good as that of the poorest thermal conductor in that multilayer, and that is usually the TIM. Our liquid-cooled DBC design dramatically reduces the number of thermal resistances including omitting the TIM. Furthermore, using bare chips instead of prepackaged chips allows for more control over the junction temperature.

Typical thermal resistances are 0.3–0.4ºC/W when a prepackaged IGBT is used. For a waste heat of approximately 50 W, this would imply a 15–20ºC rise from case to junction. For our designs, the solder layer and the intrinsic resistance of the silicon are the only contributors to the thermal resistance beyond the bonded copper. For a 100 µm thick chip with a cross-sectional area of 121 mm^2, the thermal resistance would be 0.0056ºC/W corresponding to a 0.3ºC rise to junction. Lead-tin solder could have a resistance of around 0.02ºC/W, which would give a 1ºC rise across the solder joint. The total increase from the interface temperature would be about 1.5ºC which is an order of magnitude lower than in the prepackaged chip. The lower temperature difference between the junction and interface allows for the maximum amount of current to conduct at much higher "case" temperatures.

IGBTs selected for use in modeling were Infineon Technologies "trench type" IGBTs. This chip has maximum ratings of 600 V and 200 A. It possesses low $V_{CE(sat)}$, low turn-off losses, short tail current, and positive temperature coefficient and is easily paralleled. Diodes selected for use were Infineon Technologies fast-switching diode chips in EMCON 3-Technology. This chip has maximum ratings of 600 V and 200 A. It possesses soft, fast switching, a low reverse recovery charge and a small temperature coefficient. Both have temperature operating ranges of -40°C to 175°C.

4.2 ESTABLISH DESIGN PARAMETERS FOR FEA ON 3-DIMENSIONAL (3-D) MODELS FOR HEAT TRANSFER OPTIMIZATION

4.2.1 Determine Appropriate Thermal Load for 3-D Models

In previous research and development efforts, two inverter ratings were used in thermal models: 55 kW peak and 30 kW continuous. A constant efficiency in the inverter over the entire operational range was also assumed in these previous efforts. Thus the thermal load could be determined for continuous and peak loading. However, these assumptions are not entirely valid. Data from Oak Ridge National Laboratory's (ORNL) Semikron [3] testing shown in Fig. 10 show that waste heat magnitudes can approach maximum values while the output is below the peak power rating. This is due to decreases in efficiencies based on running conditions.

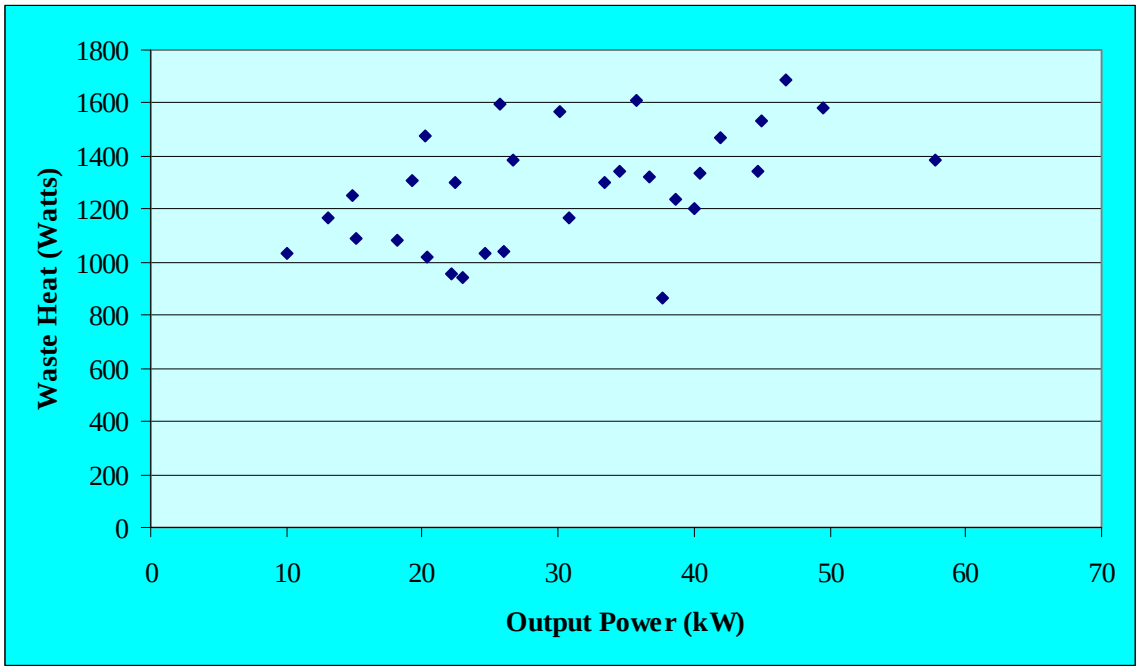

Fig. 10. Waste heat produced by Semikron inverter for different output powers.

An approximate waste heat distribution for this architecture can be found using Semikron testing evaluation results and a maximum waste heat of 1746 W. Assuming that the upper and lower leg of each phase will dissipate equal amounts of energy over an operational period, the heat loss per hexagonal section is 291 W. Each section will have two diodes and three or four IGBTs. It is assumed that the diode losses are about a third of the switch losses. This approximation is based on an application note that Semikron published for an inverter to control electric forklifts [4]. The power range was smaller than for full-size vehicles but the loss ratio should give a good estimate of the loss distribution.

Using this ratio and four IGBTs per section implies that 75% of the loss will come from the switches and 25% from the diodes or 54.6 W per switch and 36.4 W per diode. If three switches were used, the losses would be 72.75 W per switch and 36.4 W per diode. No attempt will be made to justify a continuous operating loss because of the efficiency dependency of the heat losses. Furthermore, using the maximum losses allows the design to be configured for the worst case scenario. The design should then provide more than adequate cooling for transient power fluctuations and continuous load.

4.2.2 Justification of Number of Chips to Use for Specific Designs

In this study the heat load for the IGBT was varied to simulate the number of switches used for each half electrical phase. A minimum of three switches is required to achieve the current rating necessary for the inverter. Because the devices are being run at the upper end of their operational range, four switches may be used to spread the losses of the inverter out over a wider area and to add a margin of safety. The computer models will predict the maximum temperatures to determine if the selected chip population is a viable option.

Using the power ratings in the previous discussion, computer models were run using 55 W and 73 W per chip for all devices. These heat loads will represent the worst-case scenario for their respective chip population per section. The hexagonal design of the half electrical phase section allows for various placements of the switches and diodes as depicted in Fig. 11. The hexagonal structure was desired

because it allows for a compact chip layout, provides excellent sealing surfaces, and provides adequate space to incorporate coolant channels. In high-thermal-conductivity materials, the flat of the hexagonal structure was designed to be 12 mm. This provided enough surface area for the switches to be sintered or soldered. When using a lower thermal conductivity material, such as Al_2O_3, the flat of the hexagonal structure has to increase. Models showed that it must increase to 24 mm. This was necessary for heat dissipation within the structure. In either case, the length of the entire ceramic structure is 30 mm. This length provides enough surface area for the switches, wire bonds, electrical connections, and sealing surfaces. Substrate sealing issues were another concern. The rounded ends of the hexagonal structure will provide an excellent sealing surface as opposed to the traditional flat plate design currently used. Because of manufacturing restrictions and automotive manufacturer guidelines, typical thin, flat plate DBC substrates are not feasible for this concept of direct cooling. More cross-sectional area had to be created to incorporate flow channels to remove the heat.

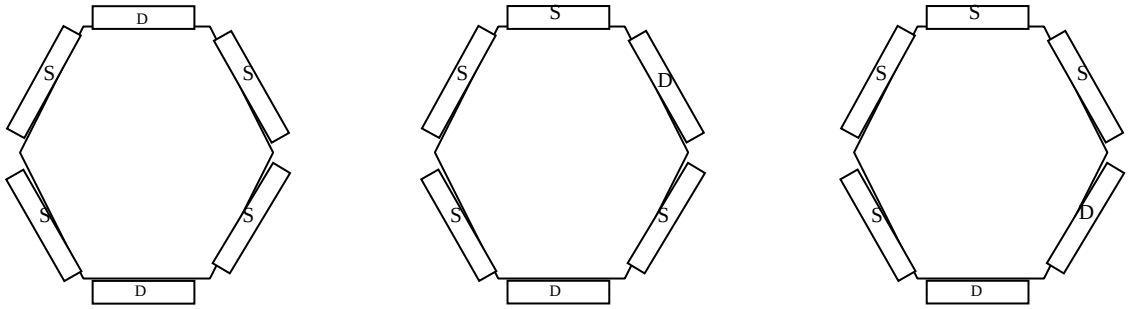

Fig. 11. Possible diode placements on hexagonal substructure.

Various layout options may suggest that full-geometry thermal models are required. However, two switches will always be on adjoining faces. This observation, along with the proximity of the flow channels to the heat source, leads to little variation in maximum temperatures that occur under the IGBTs. The effects of a lower heat loss for one face will result in local cooler regions but should not significantly affect flow channel temperatures under other devices. Furthermore, modeling the temperature distribution for higher losses, where the diodes would be present, adds to the robustness of the design.

4.2.3 Method of Determining a Successful Chip Layout

For a design to be considered successful, the thermal models must predict junction temperatures below 175ºC or even below 150ºC. Also, the coolant temperatures must be maintained below the boiling point of a 50/50 WEG mixture so that OEMs do not have to alter system pressure ratings. Table 4 shows the boiling point for 50/50 mixes of WEG for various system pressures. Typical automotive radiator caps are rated at 12–18 psig (15–16 is psig more common). Pressure ratings above 18 psig are typically indicative of high-performance parts. The coolant temperature performance criterion used in developing the models was limited to 130°C, which corresponds to 16 psig.

Table 4. Boiling point for 50/50 mixtures of WEG

Coolant pressure (psig)	WEG boiling point ºC
0	107.1
12	125.4
13	126.6
14.7	128.6
16	130.0
20	134.1

4.2.4 Analysis Parameters

The fluid inlet velocity varied depending on fluid channel size. Initial inlet velocity was consistent with a total inverter flow rate set at 2.5 gallons per minute (GPM). Velocities were then increased for various designs to determine at what flow rate the design met the design intent. This increase in velocity was helpful in determining the preferred designs. Each of the five designs should be able to pass a 1-mm particle through the flow channels; however, filtering of the coolant may be necessary. This will be determined during component testing. Fluid inlet temperature was specified as 105ºC. All other boundaries were modeled as thermally insulated. This assumption allows for a conservative design, and the actual thermal performance should result in lower junction and fluid temperatures because of other minor heat losses. The material properties used in the FEA modeling are listed in Table 5. Thermal conductivity and specific heat are dependent on temperature; however, room-temperature values are shown in Table 5 and were used in the analysis.

Table 5. Material properties used in FEA analysis modeling parameters

Material	Thermal conductivity W/m-K	Density kg/m3	Specific heat J/kg-K	Viscosity Pa-s
AlN	160	3260	740	n/a
Al_2O_3	25	3700	800	n/a
BeO	146	2850	1046	n/a
Si_3N_4	40	3200	700	n/a
SiC sintered polycrystalline	130	3100	720	n/a
50/50 **EG water**	0.4	1006	3750	0.0006

5.0 THERMAL FEA ANALYSIS RESULTS OF 3-D DESIGNS

5.1 THERMAL PERFORMANCE OF DESIGN 1 WITH OPEN FLOW THROUGH 24 FLOW CHANNELS, 1.27 MM DIAMETER

In Design 1 shown in Fig. 12, 24 flow channels are placed through the ceramic subsection. They are equally spaced on a bolt circle that maintains a minimum distance of 1.27 mm [0.050 in.] between surfaces. The minimum distance is maintained to provide structural integrity and is based on ceramic manufacturing limitations. The inlet velocity of the fluid was 0.85 m/s which translated to a total inverter flow rate of 2.50 GPM. The inlet temperature of the fluid was specified as 105ºC. The darkened triangle represents a thermally symmetric unit cell that was modeled for simplicity.

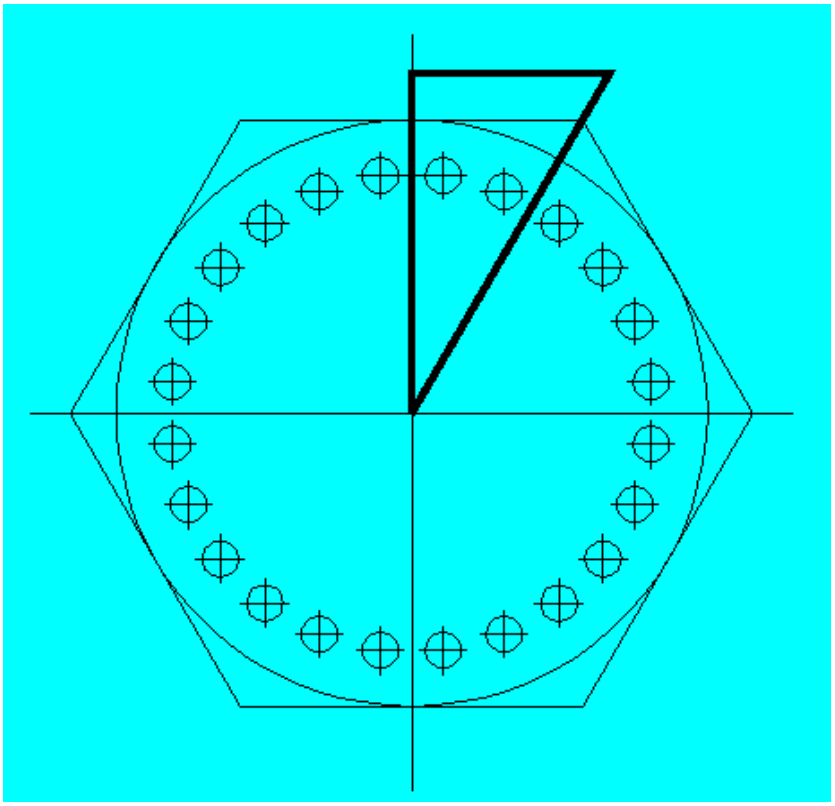

Fig. 12. Sketch of flow channel geometry relative to hexagon subsection with symmetric geometry noted.

In Fig. 13, the open-flow configuration represents the coolest temperature distribution for a load of 55 W per chip. The maximum projected junction temperature is 141.7ºC, and the maximum fluid temperature is 136.5ºC. The junction temperature represented in the graphical representation is representative of AlN. When Al_2O_3 is used, the projected junction temperature is 182.9ºC and the maximum fluid temperature is 163.0ºC. With SiC, the projected junction temperature is 144.7ºC, and the maximum fluid temperature is 138.8ºC. If BeO is used, the projected junction temperature is 143.0ºC, and the maximum fluid temperature is 137.5ºC.

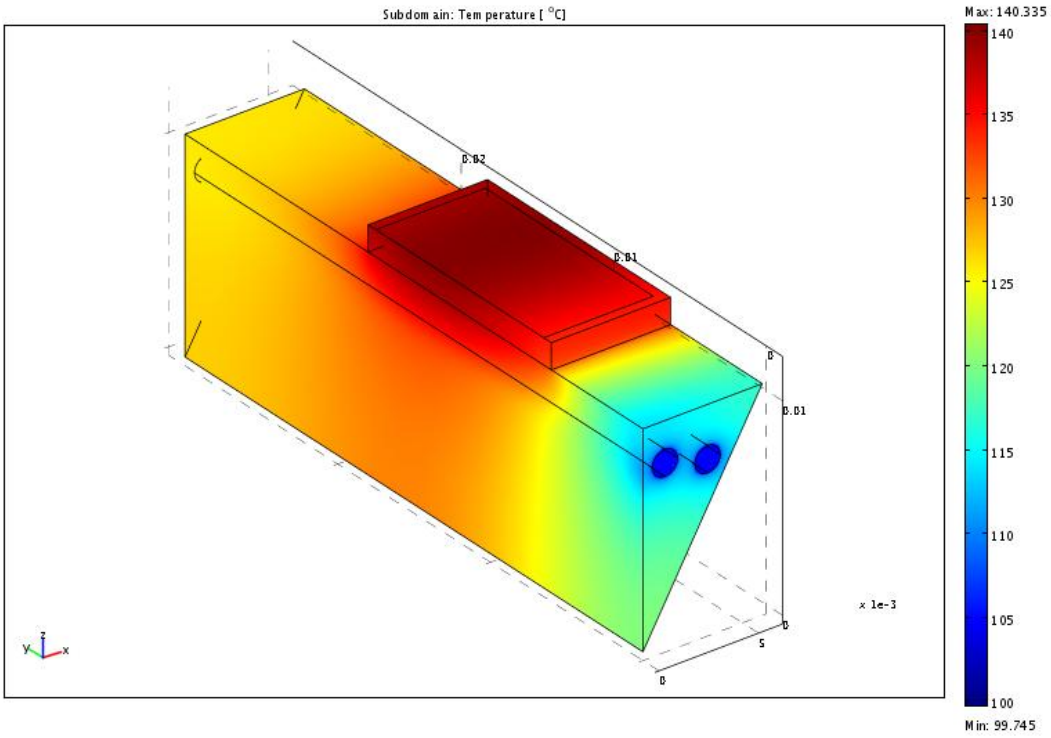

Fig. 13. Temperature distributions for Design 1 with a load of 55 W.

In each case using different ceramic materials, the maximum fluid temperature exceeded the boiling point with the load resulting from four switches. Therefore, no FEA was run using three switches, as the increased load would increase both maximum junction temperature and fluid temperature.

Variations in the WEG mixture were investigated briefly to see if a temperature decrease would result from increasing the thermal conductivity of the solution. Solutions of 60/40 and 70/30 WEG were modeled. The maximum fluid temperatures did decrease but only by about a degree Celsius for each 10% reduction in EG. Unfortunately the boiling points also readjusted for the new mix ratios. The boiling points also dropped by about a degree Celsius for each 10% reduction in EG; therefore, the relative difference between maximum fluid temperature and allowable boiling points was constant. Thus, no noticeable benefit was obtained by altering the fluid mixture from 50/50 WEG.

5.2 THERMAL PERFORMANCE OF DESIGN 2 WITH FLOW THROUGH FOUR HOLES FILLED WITH A POROUS METALLIC FOAM INSERT, 5.4 MM DIAMETER

Other options were explored because Design 1 resulted in a maximum fluid temperature that exceeded the boiling point of WEG. In order to enhance the thermal conductivity of the fluid, metal foam additions to the flow section were explored. The addition of a thermal enhancer, such as aluminum foam or copper foam, into the flow channels provided a greater surface area within the flow channel to remove the waste heat more efficiently. This material has a much higher structural integrity than other types of microstructures and provided a simple means of manufacture. Figure 14 shows the design geometry with four holes; each would be filled with either a copper foam or aluminum foam insert. The section in the rectangle is the symmetric section that is modeled. Fewer holes are required because more heat can be removed with the addition of the foam.

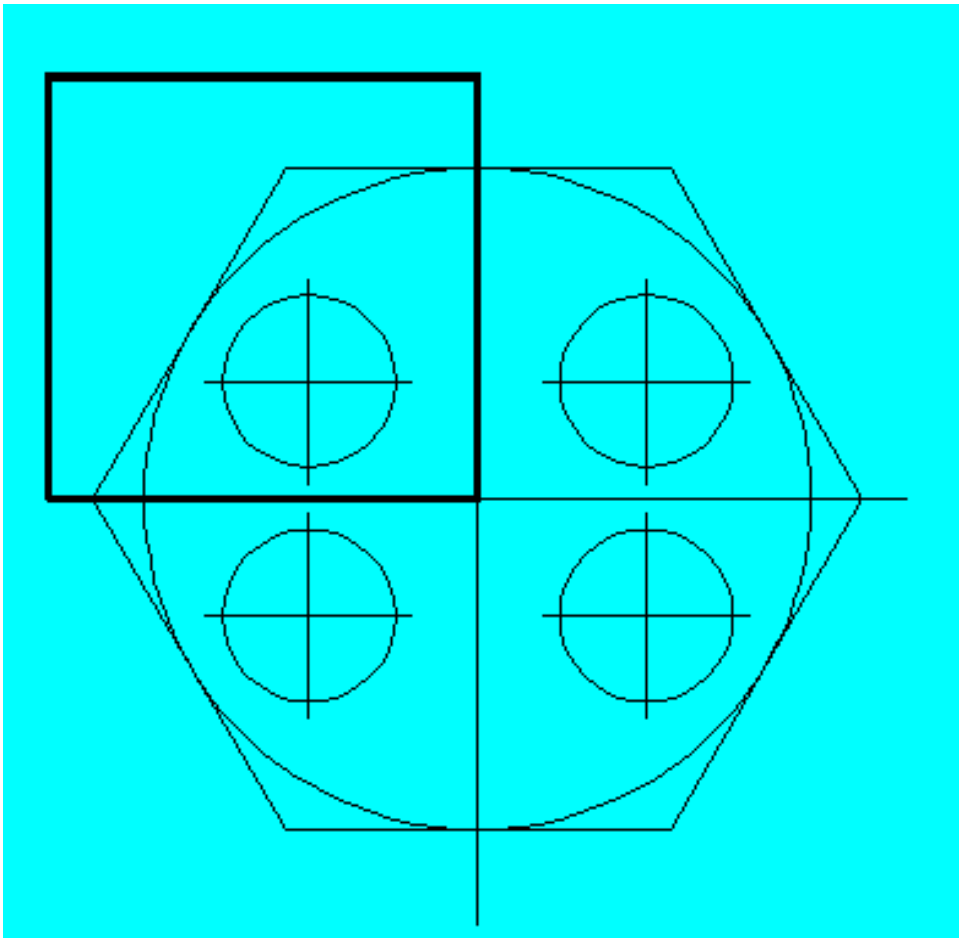

Fig. 14. Sketch of Design 2 with four flow channels.

The properties for the flow channel must be adjusted to reflect the addition of the metallic foam. Also, the velocity of the inlet must be calculated for an effective area because the metal foam matrix blocks some of the inlet area. Table 6 shows the parameters used for the both the copper foam and aluminum foam inserts. The inlet conditions correspond to an inverter flow rate of 2.5 GPM at a temperature of 105ºC.

Table 6. Properties of flow channel with copper foam and aluminum foam insert

Material	Thermal conductivity	Density	Specific hHeat	Porosity
	W/m, K	kg/m3	J/kg, K	
50/50 mixture with copper foam	14	1775	2101	0.9
50/50 mixture with aluminum foam	7.2	1175	3095	0.89

The thermal conductivity is an effective thermal conductivity based on correlations by Calmidi and Mahajan [5]. Note that no viscosity was used because the flow field was assumed to be plug flow. This

assumption is valid based on Darcy's Law for flow through porous media. In short, the metal matrix prohibits boundary layer formation along the walls of the channel which results in plug-type flow.

In Fig. 15, the maximum fluid temperature is 119°C and the maximum projected junction is 126.5°C when AlN is used with copper foam added to the flow channel and four switches.

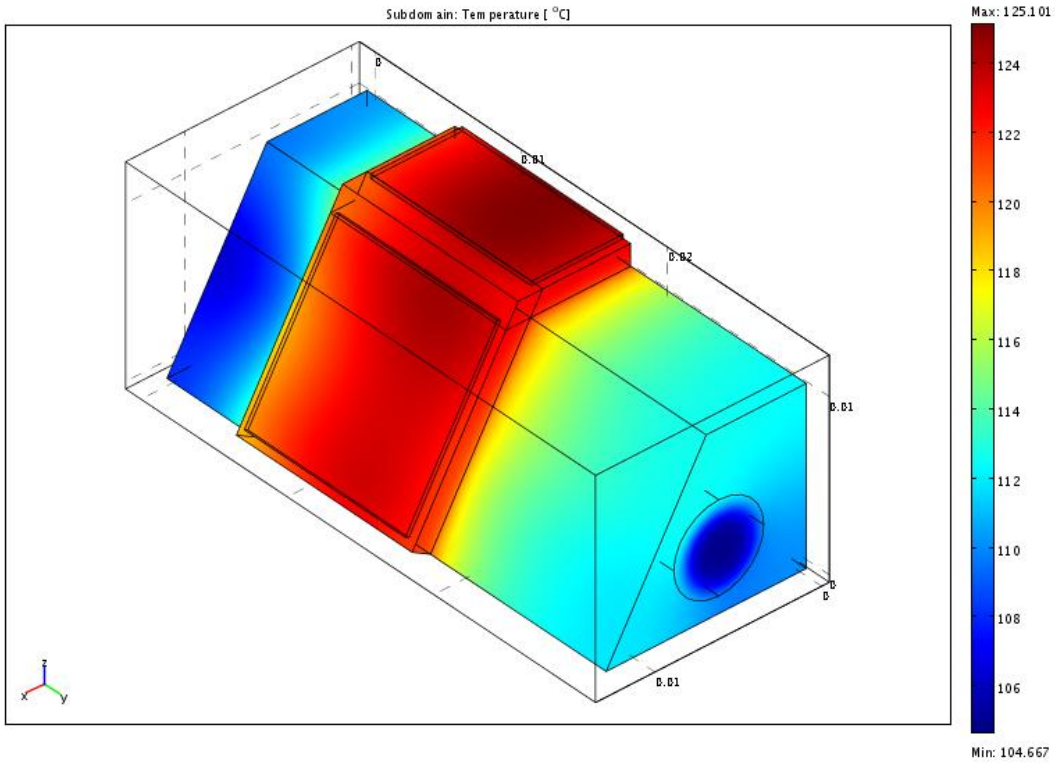

Fig. 15. Temperature distributions in Design 2 with copper foam insert.

If BeO is used, the maximum junction temperature is 127.6ºC and the maximum fluid temperature is 119.4ºC. When Al_2O_3 is used, the maximum junction temperature is 167.5ºC, and the maximum fluid temperature is 126.6ºC. If SiC is used, the maximum junction temperature is 128.2ºC and the maximum fluid temperature is 119.8ºC.

When the aluminum foam is added to the flow channel and four switches are used, the maximum projected junction temperature of AlN is 129.3ºC and the maximum fluid temperature is 122.7ºC. If BeO is used, the maximum junction temperature is 130.6ºC and the maximum fluid temperature is 123.1ºC. When Al_2O_3 is used, the maximum junction temperature is 171.5ºC and the maximum fluid temperature is 133.4ºC. If SiC is used, the maximum junction temperature is 131.9ºC and the maximum fluid temperature is 123.7ºC.

For a design with three chips using AlN, the maximum projected junction temperature is 133.8ºC and the maximum fluid temperature is 123.7ºC. This design could use three or four switches based on the thermal analysis for the higher-thermal-conductivity ceramics. If three switches were used, the minimum radiator pressure should be 15 psig to allow for a margin of safety.

5.3 THERMAL PERFORMANCE OF DESIGN 3 WITH FLOW THROUGH ONE FLOW CHANNEL FILLED WITH A POROUS METALLIC FOAM INSERT, 9 MM DIAMETER

Figure 16 shows the third design. The flow channel in the center is 9 mm in diameter and is filled with a metallic foam insert. The triangular section represents the modeled (one-twelfth) symmetric section. The material properties were the same as for the previous case. The inlet conditions corresponded to a flow rate of 2.5 GPM for the whole inverter at a temperature of 105ºC.

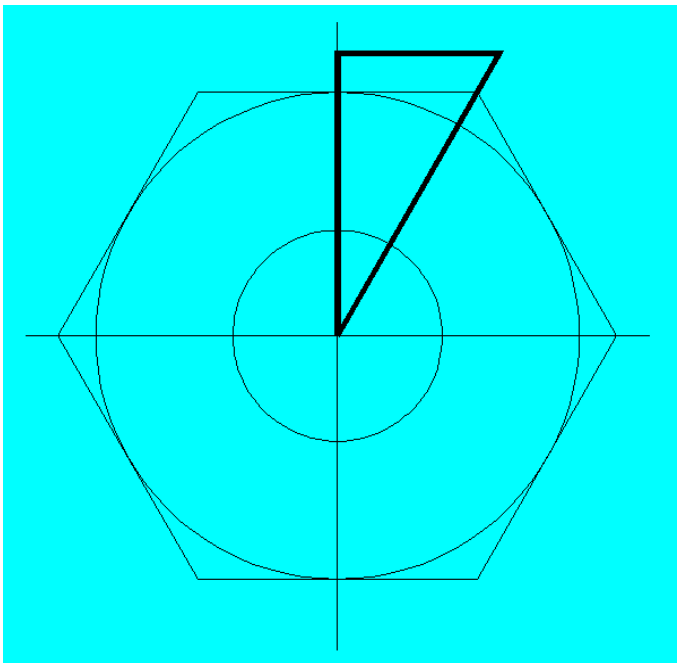

Fig. 16. Sketch of Design 3 with one flow channel.

Figure 17 shows the temperature distribution in Design 3 with a copper foam insert. Decreasing the number of flow channels to one allows for much simpler construction and manufacturing. Using a total of four switches, the maximum junction temperature for AlN is 137.3ºC and the maximum fluid temperature is 120.5ºC. When BeO is used, the maximum junction temperature is 138.8ºC and the maximum fluid temperature is 120.6ºC. If Al_2O_3 is used, the maximum junction temperature is 219.5ºC and the maximum fluid temperature is 121.4ºC. If SiC is used, the maximum junction temperature is 140.9ºC and the maximum fluid temperature is 120.7ºC. For three switches using AlN, the temperatures remain within the performance criteria with a maximum junction of 147.9ºC and a maximum fluid temperature of 125.6ºC.

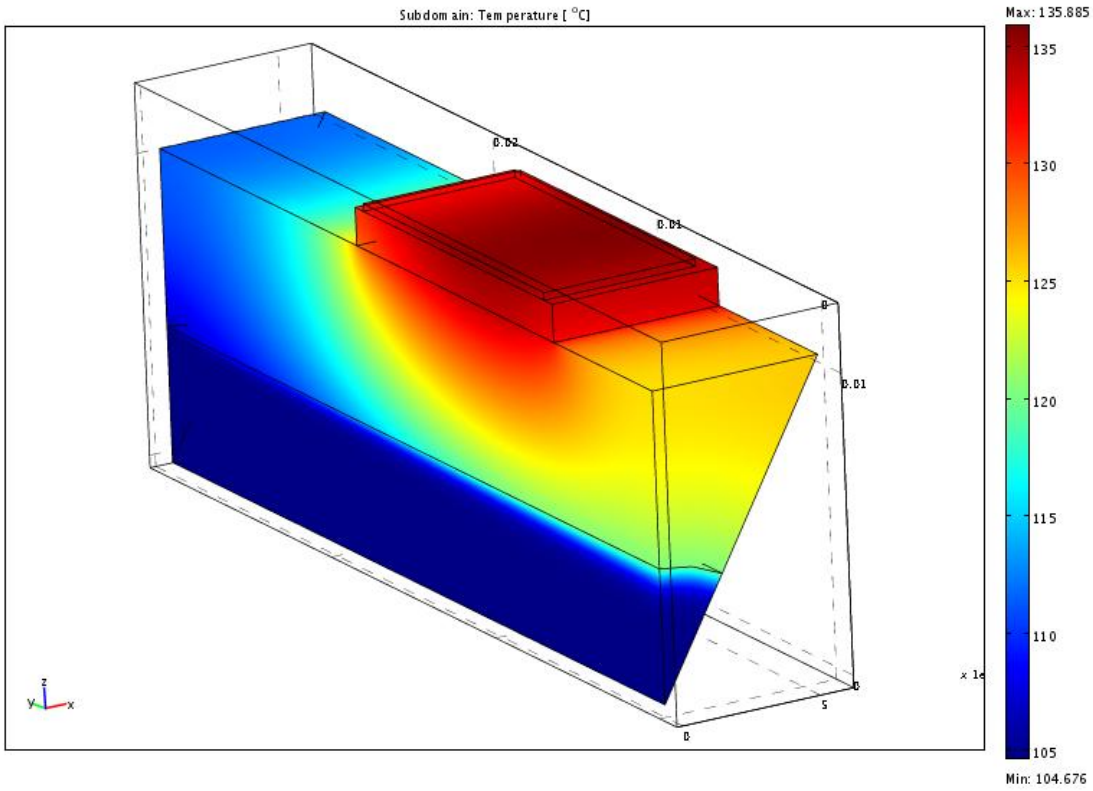

Fig. 17. Temperature distributions in Design 3 with copper foam insert.

Using a total of four switches and adding aluminum foam to the flow channel, the maximum junction temperature for AlN is 142.3ºC, and the maximum fluid temperature is 126.1ºC. When BeO is used, the maximum junction temperature is 143.8ºC and the maximum fluid temperature is 126.3ºC. If Al_2O_3 is used, the maximum junction temperature is 224.4ºC and the maximum fluid temperature is 127.9ºC. If SiC is used, the maximum junction temperature is 145.9ºC and the maximum fluid temperature is 126.4ºC.

Again, the maximum temperatures for this design would decrease as the diameter of the copper foam increased. This increase in diameter would need to be contrasted against the cost and structural integrity of the ceramic during thermal cycling. If fewer switches were used in either the copper or aluminum foam design containing a single flow channel, then the system pressure would need to be maintained at around 16 psig to ensure that boiling would not occur.

The foam structure adds another benefit in that it can restrict bubble growth in the event of boiling. In an open-channel design, bubbles can grow to the point of blocking flow. Furthermore, as a bubble develops on the wall it creates a local hot spot that could be detrimental to a chip. The foam limits the bubble growth size to roughly the pore size of the foam. Thus if boiling were to occur, which the models do not predict, it could neither significantly block the flow nor create a large hot spot near the wall.

5.4 THERMAL PERFORMANCE OF DESIGN 4 WITH FLOW THROUGH A ANNULAR FLOW CHANNEL FILLED WITH A POROUS METALLIC FOAM INSERT

Based on careful examination of the previous designs for all materials, a lower-cost option for the higher-thermal-conductivity materials (AlN, BeO, and SiC) needed to be explored. Even though the thermal performance of those ceramics is far superior to that of Al_2O_3, substrates made of these materials would cost almost as much as the whole inverter at the current OEM's cost target, so their consideration was discontinued. Additionally, concern was beginning to mount over the chemical compatibility of AlN with WEG (and therefore the potential for erosion of AlN) as shown in Fig. 5. That lent a further rationale for considering Al_2O_3 instead because it is chemically inert against WEG. In another design iteration to improve the thermal performance of a substrate made with Al_2O_3, an annular flow channel with aluminum foam was modeled. Figure 18 is a sketch of this geometry.

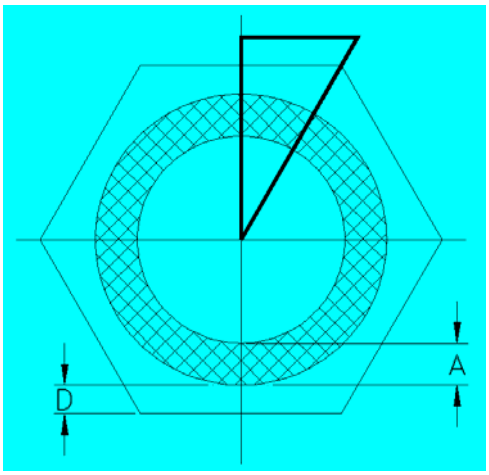

Fig. 18. Schematic of annular geometry.

In this geometry the minimum distance from the face to the flow channel D can be smaller than in the previous models. This smaller distance is a result of an increase in local velocities created by the annular shape. For the model, D was 3.4 mm and A, the annulus thickness, was 5 mm. Five millimeters was chosen based on the general dimensions of the aluminum foam matrix. If the annulus thickness was too thin, the foam would not have any structural integrity. The radii were determined based on these parameters and the hexagon face width. The inlet velocity was determined based on a constant inverter flow rate of 2.5 GPM. Figure 19 shows the maximum temperatures for this design.

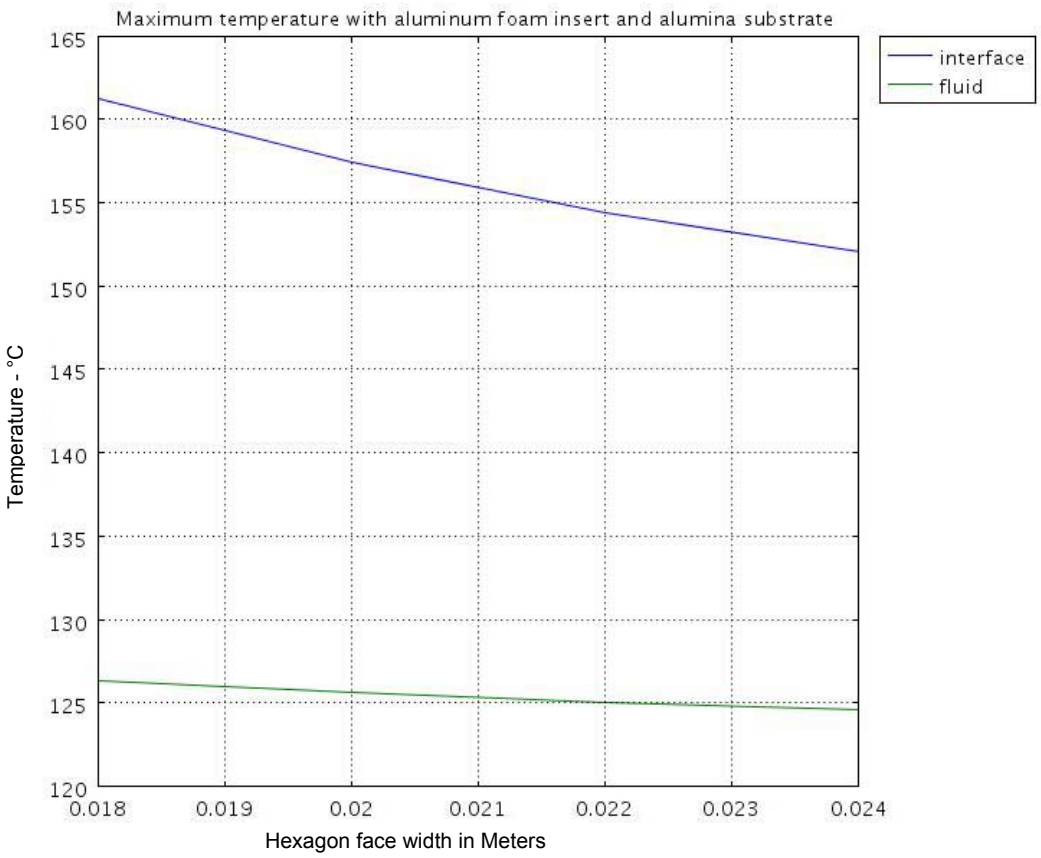

Fig. 19. Maximum interface and fluid temperatures for annular flow channel geometry with aluminum foam, D = 3.4 mm and A = 5 mm.

At a face width of 18 mm, the temperatures are within the maximum limits of the design. This performance is a considerable improvement over the Al_2O_3 single flow channel in Design 3. To increase the reliability of the power electronics, the hexagon face could be increased more.

The probability of survival (POS) of the Al_2O_3 substrate subjected to the conditions shown in Fig. 20 was determined by performing an established two-step analysis. First, the thermo-mechanical stress state within the Al_2O_3 substrate was determined using FEA (ANSYS, Canonsburg, PA). A one-twelfth symmetry was utilized, as shown in Fig. 21. The thermal conductivities, coefficients of thermal expansions, elastic moduli, and Poisson's ratios of the Al_2O_3, copper (directly bonded to the Al_2O_3), solder, and silicon chip were taken into account. The solder was allowed to yield but the other three materials in the model remained linearly elastic (see Fig. 22). Heat generation in the silicon chip (55 W) was accounted for. At a face width of 24 mm, which is twice the nominal width of 12 mm using higher-thermal-conductivity materials, the maximum interface temperature was around 152°C and the maximum fluid temperature was below 125°C (see Fig. 23). Again these temperatures meet the maximum limits of the design parameters.

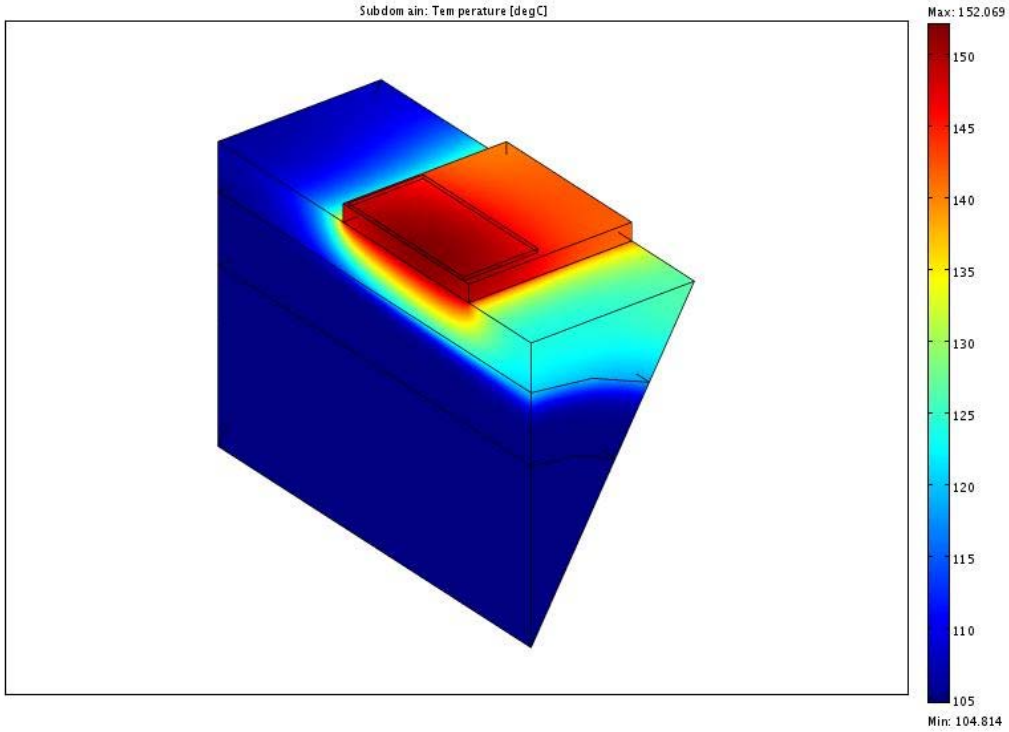

Fig. 20. Temperature distribution in Design 4, 24 mm face width alumina ceramic with annular flow channel geometry.

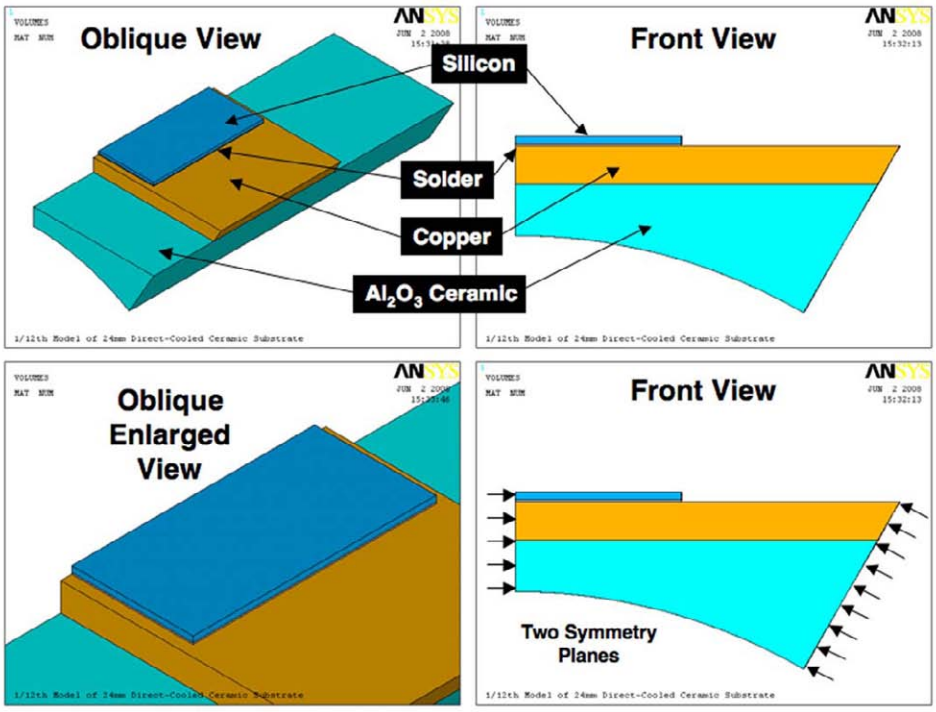

Fig. 21. One-twelfth thermo-mechanical FEA model of Design 4, 24 mm face width alumina ceramic with annular flow channel geometry.

Material	E (GPa)	Poisson's Ratio	CTE (ppm/°C)	κ (W/mK)	Yield Strength (MPa)
Al_2O_3	360	0.24	8	25	
Copper	117	0.30	17	400	138
Solder	12.5	0.36	26	15	22
Silicon	130	0.28	4	130	

Fig. 22. Material properties used in the thermo-mechanical FEA model.

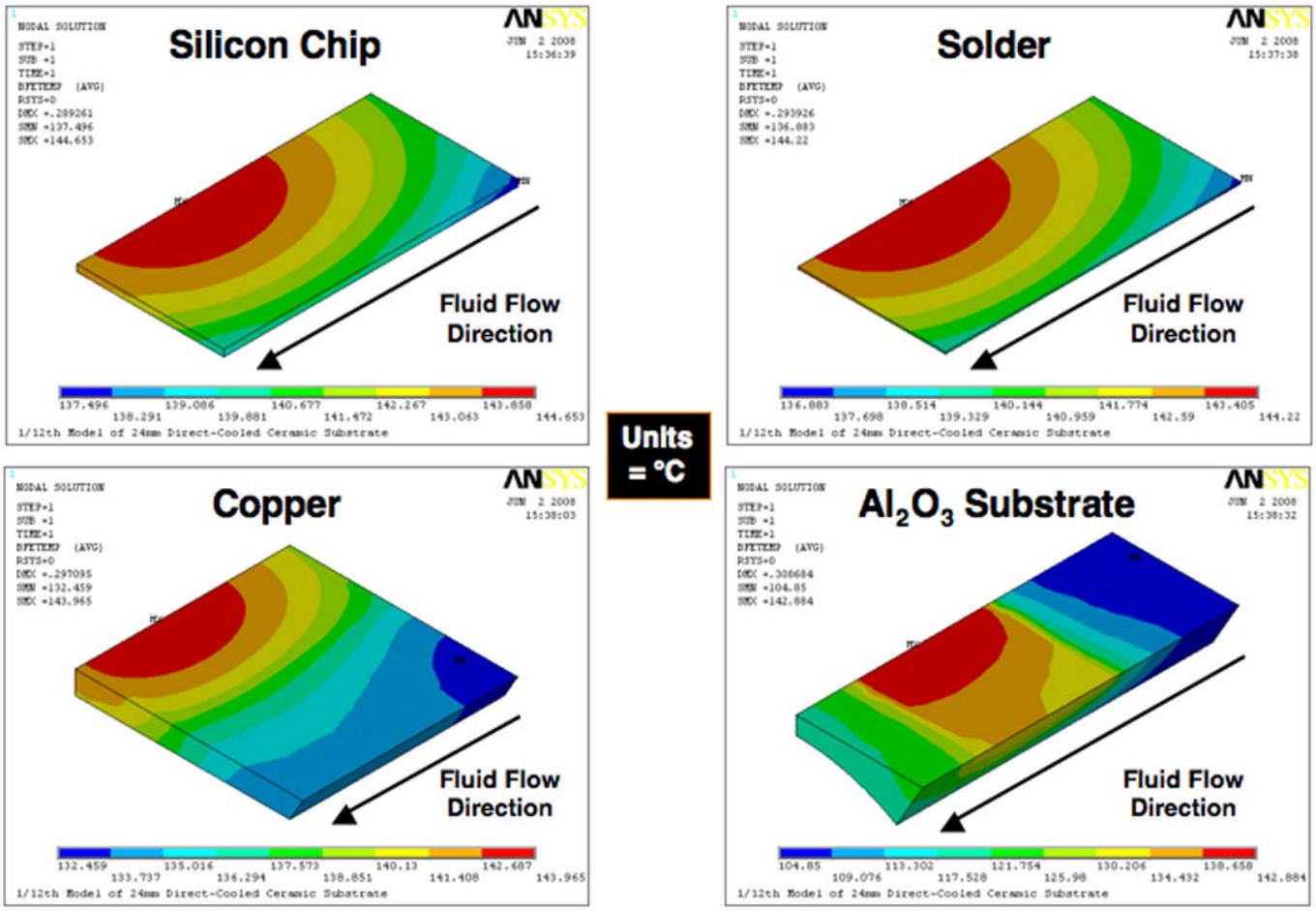

Fig. 23. Temperature profiles in each of the four subcomponents.

The magnitude of the first-principles tensile stresses and their field dictate the POS of a ceramic component, so that the (thermal-induced) stress field was determined and is shown in Fig. 24. The POS was determined by incorporating both of the two-parameter Weibull strength distributions for Al_2O_3 limited by both volume- and surface-type flaws. In this analysis, the Weibull moduli of both were taken to be 15, and the scaling parameters were 500 MPa•mm$^{3/m}$ for volume-based analysis and 500 MPa•mm$^{2/m}$ for surface-based analysis. The combination of the first-principles tensile stress field and those Weibull parameters occurred using a FEA post-processing software called Ceramic Analysis and Reliability Evaluation of Structures (CARES [Connecticut Reserve Technologies, Gates Mills, OH]).

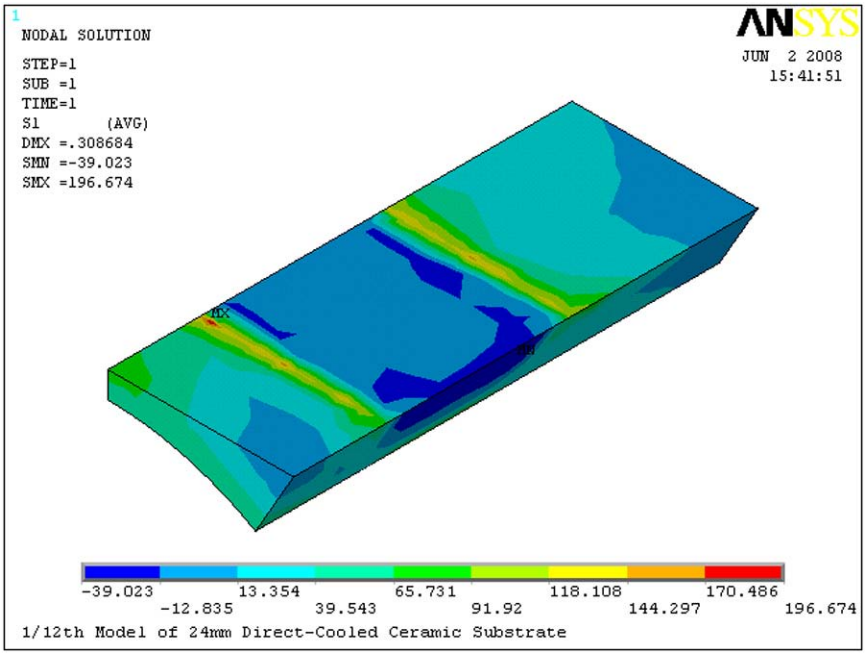

Fig. 24. First-principles stresses in the Al_2O_3 ceramic substrate (Design 4).

The CARES analysis showed that the maximum first-principles tensile stresses from thermal loading were low and easily within the mechanical capability of the Al_2O_3 ceramic. Its resulting POS analysis showed that 999,992 out of 1,000,000 hexagonal structures (99.9992%) of Design 4 should sustain the imposed thermo-mechanical stresses without mechanical failure. Further optimization of this geometry could be explored to decrease the face-to-radius distance and increase the POS, but this model shows that a candidate Al_2O_3 ceramic geometry is actually quite viable in Design 4.

This design adds some other benefits. A common product with aluminum foam is a pipe with foam bonded onto the outer surface. In Design 4, an aluminum pipe with foam could be pressed into a larger hole to form the annulus. The aluminum pipe ends would have to be brazed closed to prevent a fluid bypass. However, the overall effect would reduce the weight of the substrate and should keep the cost lower because less Al_2O_3 is needed to make the part compared with a solid core.

5.5 THERMAL PERFORMANCE OF DESIGN 5 WITH FLOW THROUGH FOUR HOLES FILLED WITH A POROUS METALLIC FOAM INSERT, 9.8 MM DIAMETER

To provide another design option with Al_2O_3, a four-hole design was explored. Again the face width had to be increased to reduce the operating temperatures to the design limits. In this design process, the size of the flow channel, which is filled with aluminum foam, and the hole center location were varied to find an optimum design. In the final design iteration, the center of the hole was offset from the center of the chip to provide the coolest chip temperatures. The resulting temperatures proved that the offset dimension was critical for this design to meet the performance criteria. The highlighted section in Fig. 25 represents the (one-fourth) symmetric section of the model used for FEA.

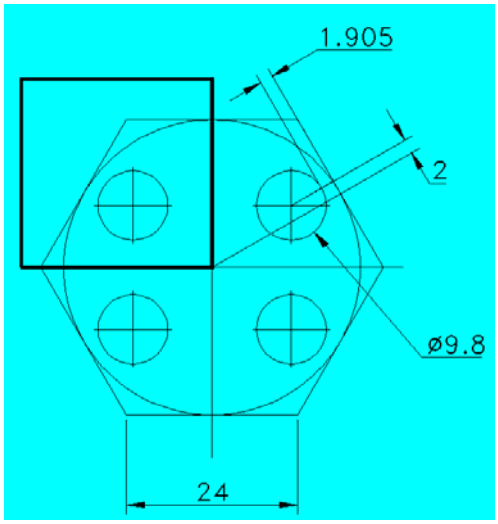

Fig. 25. Design 5 with four offset 9.8-mm-diameter flow channels.

The FEA run on this model used a top silicon chip heat generation of 37 W to represent a diode, and a side silicon chip heat generation of 55 W to represent an IGBT. Figure 26 represents the chip and fluid temperatures at various offset dimensions.

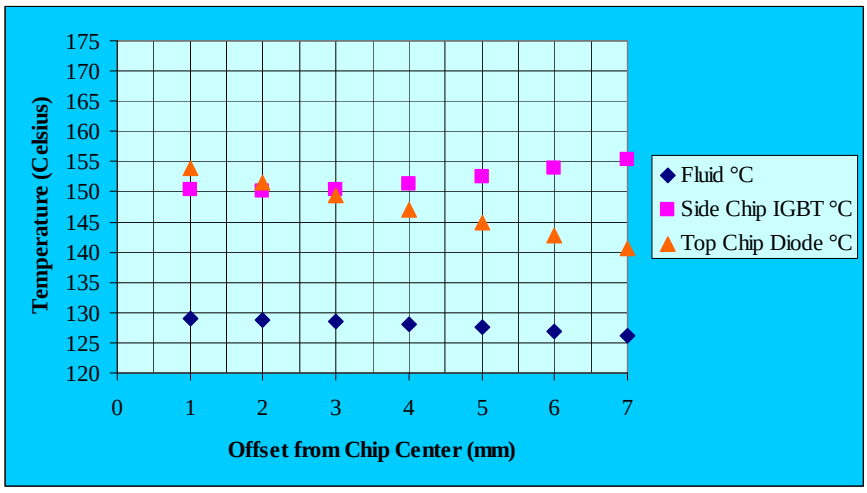

Fig. 26. Critical temperatures for 9.8-mm-diameter coolant channel.

Figure 27 represents the temperature distribution of Design 5. This design contains a 24-mm face with a Al_2O_3 ceramic containing aluminum foam with the flow channel offset 2 mm from the chip center.

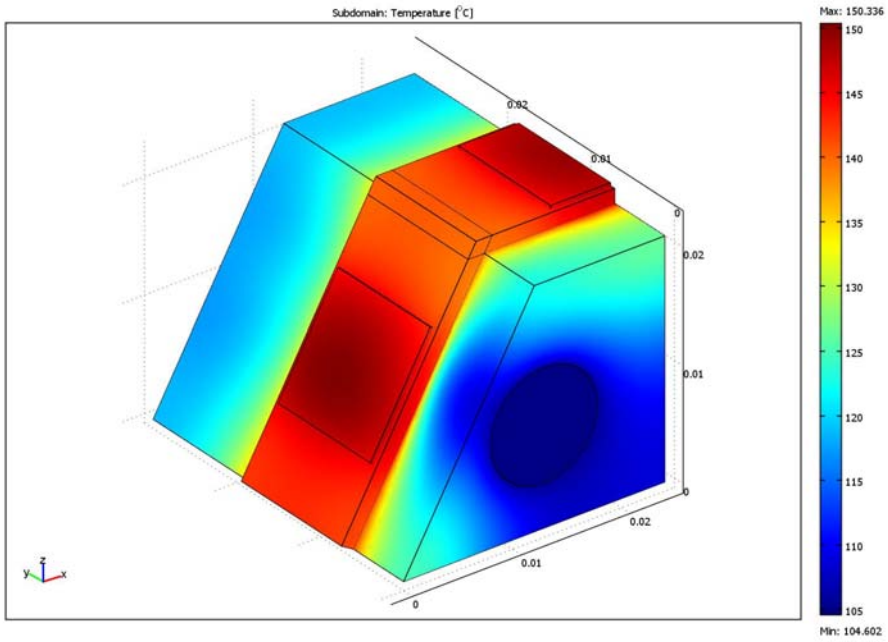

Fig. 27. Temperature distribution of Design 5 containing four coolant channels with each channel offset 2 mm from chip center.

Another ceramic POS analysis study was conducted using the information portrayed in Figs. 25–27. A one-fourth model of Design 5 was constructed in ANSYS and is shown in Fig. 28. Copper and solder dimensions were the same as those shown in Fig. 21 and are included in Fig. 28. The IGBT (left in Fig. 28) generated 55 W and the diode (top in Fig. 28) generated 37 W. The maximum chip temperature is 153°C and the maximum fluid temperature is below 125°C, and those meet the design temperature constraints (see Fig. 29). Again these temperatures met the maximum limits of the design parameters. The same properties shown in Fig. 22 were again used in this analysis of Design 5. The resulting first-principles tensile stress field within the ceramic substrate is shown in Fig. 30.

Using the same Weibull parameters as above, CARES analysis showed that the maximum first-principles tensile stresses from thermal loading were low and easily within the mechanical capability of the Al_2O_3 ceramic. The POS analysis showed that 999,906 out of 1,000,000 hexagonal structures (99.9906%) of Design 5 will sustain the imposed thermo-mechanical stresses without mechanical failure. Further optimization of this geometry could be explored to decrease the face-to-radius distance and increase the POS, but this model also shows that a candidate Al_2O_3 ceramic geometry is again quite viable in Design 5.

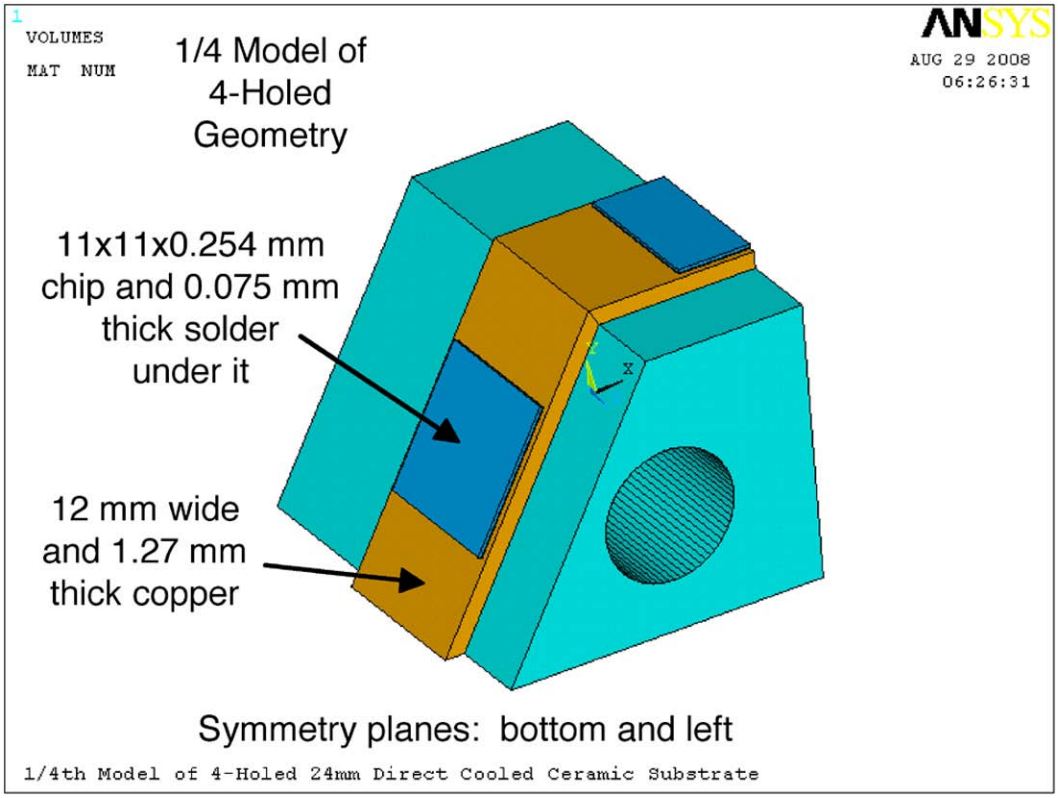

Fig. 28. One-fourth thermo-mechanical FEA model of Design 5 containing four coolant channels with each channel offset 2 mm from chip center.

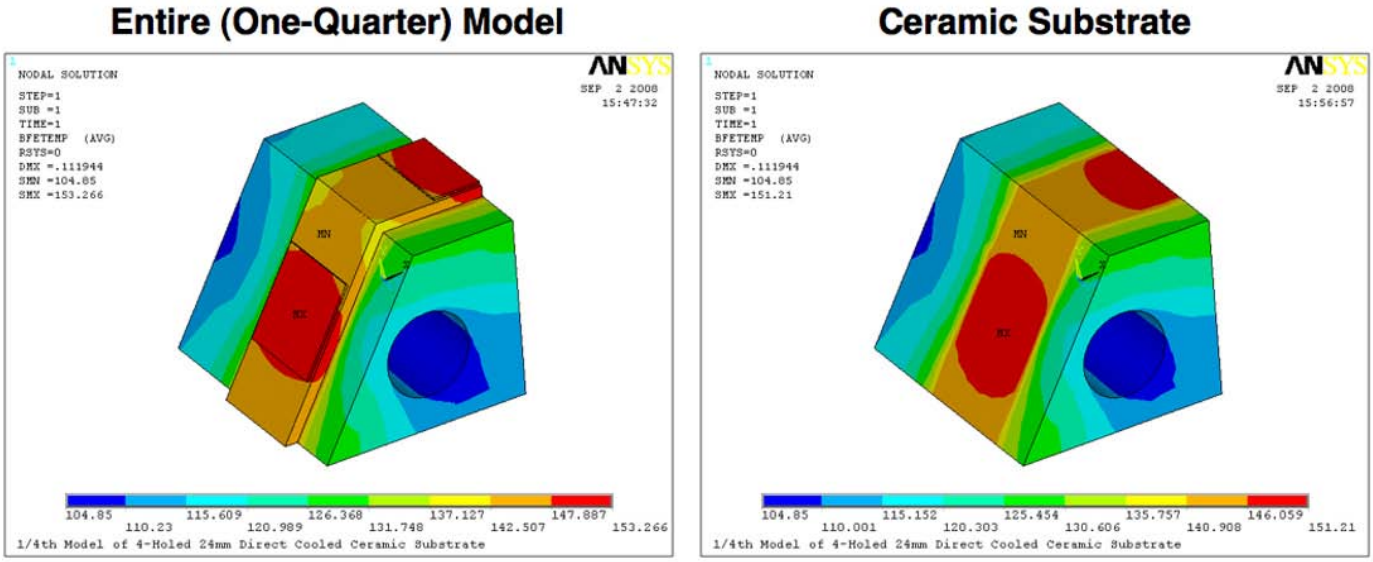

Fig. 29. Temperature profiles in Design 5.

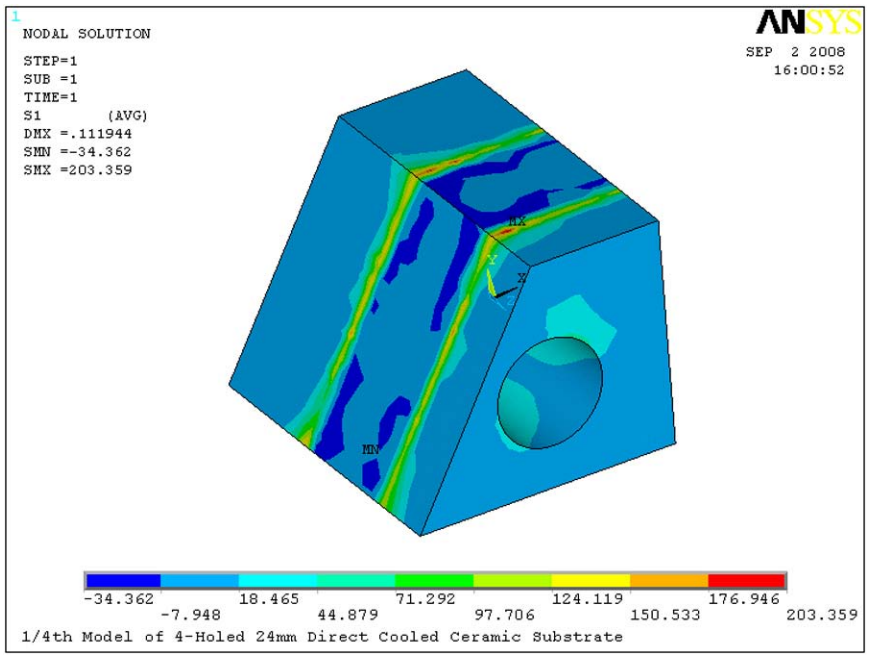

Fig. 30. First-principles stresses in the Al_2O_3 ceramic substrate (Design 5).

6.0 DESIGN CONCLUSION

6.1 DESIGN MATRIX SUMMARY

A performance matrix and weight system was developed to help evaluate the effectiveness of each design. These design matrix summaries are listed in Tables 7–13. They contain the loads, thermal data resulting from the use of three or four IGBTs, manufacturing variables and trade-offs, and cost to manufacture in quantities of 100,000 pieces. If the thermal results of some designs using four IGBTs were at or above the design criteria limitations, no FEAs were needed using fewer chips. In addition, velocities were determined for each design that exceeded the performance criteria to determine how much flow increase was required to meet the design intent. This increase in velocity was helpful in determining the preferred designs; however, OEMs recommended the volumetric flow rate be maintained at a maximum of 2.5 GPM.

Table 7. Design 1 matrix summary

Design	1			
Description	24 holes 1.27 mm diameter			
Ceramic insulator	AlN	BeO	Alumina	SiC
Copper foam (10 ppi, 8% ρ_{rel})				
Aluminum foam (10 ppi, 8% ρ_{rel})				
Load (W/switch)	55			
Performance at 2.5 GPM for entire inverter				
Max projected junction temperature	141.7	143.0	182.9	144.7
Max. fluid temperature	136.5	137.5	163.0	138.8
Pass 1-mm particle	√			
Compatible with WEG		√	√	√
Manufacturability				
Smallest feature size (mm)	1.27			
Post processing (assembly, machining…)				
Trade-offs to meet design criteria				
Required flow rate (GPM)	>7.25	>7.95	Large	>8.67
Filter	no			
Cost per ceramic rated from 100,000 pcs.	$45.87	$19.59	$2.97	$30.25
Optimization				
Load (W/switch)	n/a			
150 C – max. projected junction temperature	0	0	0	0
EG BP @ 16psig – max. fluid temperature	0	0	0	0

Table 8. Design 2 matrix summary using copper foam

Design	2			
Description	4 holes 5.7 mm diameter			
Ceramic insulator	AlN	BeO	Alumina	SiC
Copper foam (10 ppi, 8% ρ_{rel})	√			
Aluminum foam (10 ppi, 8% ρ_{rel})				
Load (W/switch)	55			
Performance at 2.5 GPM for entire inverter				
Max projected junction temperature	126.5	127.6	167.5	128.8
Max. fluid temperature	119.0	119.4	126.6	119.8
Pass 1-mm particle	Probably			
Compatible with WEG		√	√	√
Manufacturability				
Smallest feature size (mm)	5.7			
Post processing (assembly, machining…)	Foam insert			
Trade-offs to meet design criteria				
Required flow rate (GPM)	2.5	2.5	3.88	2.5
Filter	Possibly			
Cost per ceramic rated from 100,000 pcs.	$45.87	$19.59	$2.97	$30.25
Optimization				
Load (W/switch)	73			
150 C – max. projected junction temperature	133.8	135.0	0	136.7
EG BP @ 16psig – max. fluid temperature	123.7	124.1	124.7	0

Table 9. Design 2 matrix summary using aluminum foam

Design	2			
Description	4 holes 5.7 mm diameter			
Ceramic insulator	AlN	BeO	Alumina	SiC
Copper foam (10 ppi, 8% ρ_{rel})				
Aluminum foam (10 ppi, 8% ρ_{rel})	√			
Load (W/switch)	55			
Performance at 2.5 GPM for entire inverter				
Max projected junction temperature	129.3	130.6	171.5	131.9
Max. fluid temperature	122.7	123.1	133.4	123.7
Pass 1-mm particle	Probably			
Compatible with WEG		√	√	√
Manufacturability				
Smallest feature size (mm)	5.7			
Post processing (assembly, machining…)	Foam insert			
Trade-offs to meet design criteria				
Required flow rate (GPM)	2.5	2.5	3.88	2.5
Filter	Possibly			
Cost per ceramic rated from 100,000 pcs.	$45.87	$19.59	$2.97	$30.25
Optimization				
Load (W/switch)	73			
150 C – max. projected junction temperature	137.8	139.0	0	140.8
EG BP @ 16psig – max. fluid temperature	128.5	129.1	0	129.9

Table 10. Design 3 matrix summary using copper foam

Design	3			
Description	1 hole 9.0 mm diameter			
Ceramic insulator	AlN	BeO	Alumina	SiC
Copper foam (10 ppi, 8% ρ_{rel})	√			
Aluminum foam (10 ppi, 8% ρ_{rel})				
Load (W/switch)	55			
Performance at 2.5 GPM for entire inverter				
Max projected junction temperature	137.3	138.8	219.5	140.9
Max. fluid temperature	120.5	120.6	121.4	120.7
Pass 1-mm particle	Probably			
Compatible with WEG		√	√	√
Manufacturability				
Smallest feature size (mm)	9.0			
Post processing (assembly, machining…)	Foam insert			
Trade-offs to meet design criteria				
Required flow rate (GPM)	2.5	2.5	Large	2.5
Filter	Possibly			
Cost per ceramic rated from 100,000 pcs.	$45.87	$19.59	$2.97	$30.25
Optimization				
Load (W/switch)	73			
150 C – max. projected junction temperature	147.9	149.9	0	150.0
EG BP @ 16psig – max. fluid temperature	125.6	125.7	124.7	125.8

Table 11. Design 3 matrix summary using aluminum foam

Design	3			
Description	1 hole 9.0 mm diameter			
Ceramic insulator	AlN	BeO	Alumina	SiC
Copper foam (10 ppi, 8% ρ_{rel})				
Aluminum foam (10 ppi, 8% ρ_{rel})	√			
Load (W/switch)	55			
Performance at 2.5 GPM for entire inverter				
Max projected junction temperature	142.3	143.8	224.4	145.9
Max. fluid temperature	126.1	126.3	127.9	126.4
Pass 1-mm particle	Probably			
Compatible with WEG		√	√	√
Manufacturability				
Smallest feature size (mm)	9.0			
Post processing (assembly, machining…)	Foam insert			
Trade-offs to meet design criteria				
Required flow rate (GPM)	2.5	2.5	Large	2.5
Filter	Possibly			
Cost per ceramic rated from 100,000 pcs.	$45.87	$19.59	$2.97	$30.25
Optimization				
Load (W/switch)	73			
150 C – max. projected junction temperature	n/a	n/a	n/a	n/a
EG BP @ 16psig – max. fluid temperature	n/a	n/a	n/a	n/a

Table 12. Design 4 matrix summary using aluminum foam

Design	4			
Description	24 mm face, annular flow channel			
Ceramic insulator	AlN	BeO	Alumina	SiC
Copper foam (10 ppi, 8% ρ_{rel})				
Aluminum foam (10 ppi, 8% ρ_{rel})	√			
Load (W/switch)	55			
Performance at 2.5 GPM for entire inverter				
Max projected junction temperature	n/a	n/a	152.0	n/a
Max. fluid temperature	n/a	n/a	124.0	n/a
Pass 1-mm particle	Probably			
Compatible with WEG			√	
Manufacturability				
Smallest feature size (mm)	5.0			
Post processing (assembly, machining…)	Foam insert			
Trade-offs to meet design criteria				
Required flow rate (GPM)	2.5	2.5	2.5	2.5
Filter	Possibly			
Cost per ceramic rated from 100,000 pcs.	X	X	$2.97	X
Optimization				
Load (W/switch)	73			
150 C – max. projected junction temperature	n/a	n/a	n/a	n/a
EG BP @ 16psig – max. fluid temperature	n/a	n/a	n/a	n/a

Table 13. Design 5 matrix summary using aluminum foam

Design	5			
Description	24 mm face, 4 holes 9.8 mm diameter, offset 2 mm from center of chip			
Ceramic insulator	AlN	BeO	Alumina	SiC
Copper foam (10 ppi, 8% ρ_{rel})				
Aluminum foam (10 ppi, 8% ρ_{rel})	√			
Load (W/switch)	55 per IGBT, 37 per diode			
Performance at 2.5 GPM for entire inverter				
Max projected junction temperature	n/a	n/a	150.3	n/a
Max. fluid temperature	n/a	n/a	128.5	n/a
Pass 1-mm particle	Probably			
Compatible with WEG			√	
Manufacturability				
Smallest feature size (mm)	5.0			
Post processing (assembly, machining…)	Foam insert			
Trade-offs to meet design criteria				
Required flow rate (GPM)	2.5	2.5	2.5	2.5
Filter	Possibly			
Cost per ceramic rated from 100,000 pcs.	X	X	$2.97	X
Optimization				
Load (W/chip)	73			
150 C – max. projected junction temperature	n/a	n/a	n/a	n/a
EG BP @ 16psig – max. fluid temperature	n/a	n/a	n/a	n/a

FEAs of the minimum and maximum principal stresses induced by thermal cycling were run only on the preferred Designs 4 and 5. This was to determine if Al_2O_3, having a lower thermal conductivity, could

withstand the temperature-induced stress without failure. The higher-thermal-conductivity materials could inherently withstand higher stress values and not fail. All of the temperature values are close to that of the Al_2O_3 design, so stress should not be a factor in the higher-thermal-conductivity materials. The two designs (4 and 5) meet the OEM's cost and performance targets.

6.2 COST COMPARISON

The directly cooled power electronics substrate project is a new concept and therefore untried in industry. Costs can be quantified on conventional inverter architectures based on component purchase prices, material costs and manufacturing assembly costs. What can be determined in this research effort are material extrusion costs, fabrication costs for ceramic components, and estimated cost savings from the elimination of the conventional heat sink, the base plate/heat spreader, and the TIM. Each of the ceramic fabrication costs is listed in Table 14 and is based on material and tooling costs per 100,000 pieces.

Table 14. Cost summary for ceramic materials considered in the fabrication of a direct-cooled power electronics substrate

Description	Material extrusion cost	Copper plating	Purchase price	Total cost per inverter
AlN	$45.87	$3.12	$48.99	$293.94
Al_2O_3	$2.97	$3.12	$6.09	$36.54
SiC	$30.25	$3.12	$33.37	$200.22
BeO	$19.59	$3.12	$22.71	$136.26

If the ceramic of choice in the final inverter design was Al_2O_3, based on the information in Table 14, the cost to produce the copper-plated ceramic substrate in a quantity of 100,000 units would be approximately $36.54. The savings compared with a conventional inverter, such as Semikron, would be $64.02 from just the elimination of the heat sink and the base plate. Additional savings will be realized by the elimination of the TIM, and there would be a weight savings of ~3 kg per inverter in this research effort because the base plate and heat sink would not be required. These cost savings do not take into account the wire bonds, the cost of the IGBTs and diodes, or the capacitor since it is expected these costs will be comparable to the current Semikron inverter in mass production.

7.0 SUMMARY

Directly cooling an Al_2O_3 ceramic substrate with 105°C coolant while maintaining silicon temperatures below their maximum operation temperature is viable and cost-effective. The shape of the substrate, size and shape of the capacitor, coolant flow channels, metallic foam flow channel inserts, and chip population on the substrate all play a key role. Because of cost limitations, Designs 1–3 had to be modified in order to meet the design goals. These changes resulted in the development of Designs 4 and 5. The designs explored all have hexagonal cross-sections. This configuration was chosen because the required surface area could be obtained within the smallest package volume. These substrates would be joined by a manifold which is placed inside the inner diameter of a hollow capacitor. Additionally, the hexagonal shape, with round ends, is far easier to seal from the coolant than other types of planer structural shapes. This design layout is similar to that of the refrigerant-cooled inverter researched by ORNL [6].

The addition of a thermal enhancer, such as aluminum foam, into the flow channels provided a greater surface area within the flow channel to remove the waste heat more efficiently. This material has a much higher structural integrity than other types of microstructures and provides a simple means of manufacture. FEA results were run using both aluminum and copper foam; however, cost, availability, and environmental concerns due to the manufacturability of the copper foam steered this research effort towards aluminum foam.

The capacitor(s) necessary to complete the inverter design dictates the overall volume of the direct-cooled power electronics substrate. Since this component has a larger volume than many of the other required components, volume reduction can be limited by the physical size of the capacitor and the capacitance required for inverter operation. Based on capacitor designs obtained from the SBE, Inc. Power Ring division, the preferred design in this research and development effort has a power density approaching 14 kW/l. However, this preferred design uses a ceramic substrate with a high-thermal-conductivity capability, which comes at a higher cost. If the lower cost ceramic substrate such as Al_2O_3 is used, the cost is significantly reduced; but the power density approaches 7.5 kW/l because of the size of the substrate necessary to spread the thermal load.

Performance testing of Designs 4 and 5 will be performed to validate the FEA results. These designs meet the specified design criteria while providing a lower cost to the OEMs. Designs 2 and 3 also met the specified design criteria but at a higher cost. They could be constructed with three or four chips as long as the coolant system pressure is kept high enough to prevent boiling but low enough such that the OEMs do not have to alter conventional radiator components. For initial bench testing in FY 2009, diodes will be used on Designs 4 and 5 to generate the waste heat needed to validate the modeling. Fewer silicon switching devices could be implemented in the final architectures so long as the experimentation supports the modeling results.

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