2008 Solar Annual Review Meeting

Session: Process Development and Integration Lab (PDIL)
Organization: National Renewable Energy Laboratory
Funding Opportunity: PDIL Capital Equipment

Wafer Replacement Cluster Tool

Howard M. Branz
National Renewable Energy Laboratory
Golden, CO 80401
howard_branz@nrel.gov

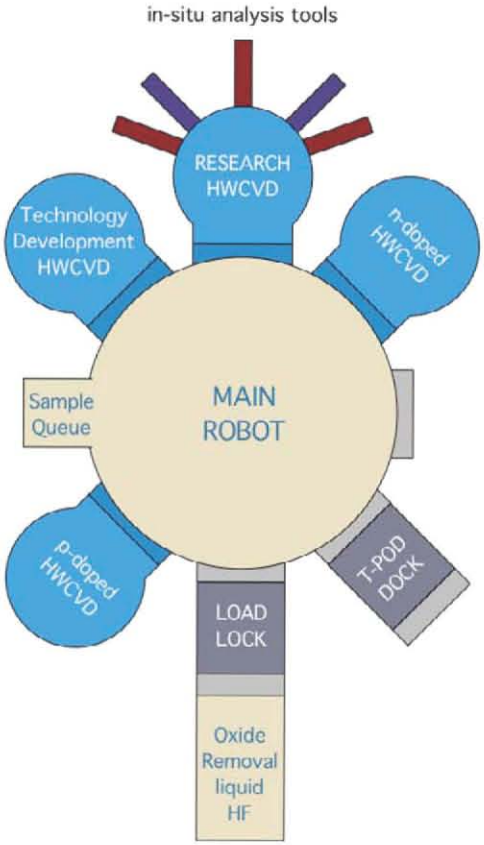
NREL/PR-520-43195
Presented at the Solar Energy Technologies Program (SETP) Annual Program Review Meeting held April 22-24, 2008 in Austin, Texas

Wafer Replacement Cluster Tool

- Platform for advanced R&D toward SAI 2015 Cost Goal
  - Crystal silicon PV at area costs closer to amorphous Si PV
    - 15% efficiency
    - Inexpensive substrate
    - Moderate temperature processing (<800°C)

- Why silicon?
  - Industrial and knowledge base
  - Abundant and environmentally benign
  - Market acceptance
  - Good efficiency

- Why replace wafers?
  - Expensive
  - High embedded energy content
  - Use 50-100 times more silicon than needed



Energy and Si-intensive wafers

Current process:

- 2 yr energy payback
- $0.60/W - $1.00/W for feedstock alone

Sand

Add Carbon & Heat Energy

CO_2

metallurgical grade Si

pure $SiHCl_3$ or SiH_4

Waste ~1/2 in sawing

Add more heat energy (1500°C)

Add Heat Energy (1000 °C)

silicon feedstock

Use 10X more than needed

Vision for wafer replacement Si

Film Si growth:

Sand

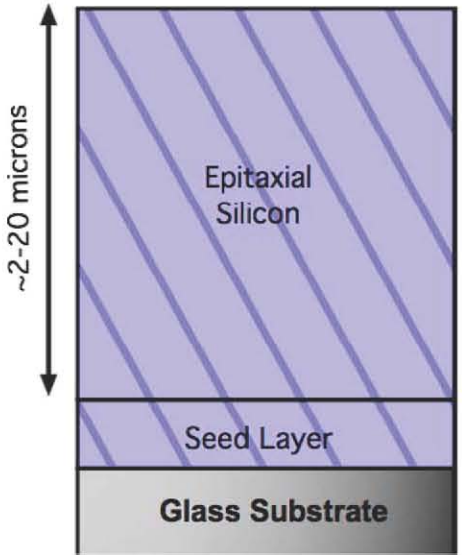
Add Carbon & Heat Energy

CO_2

metallurgical grade Si

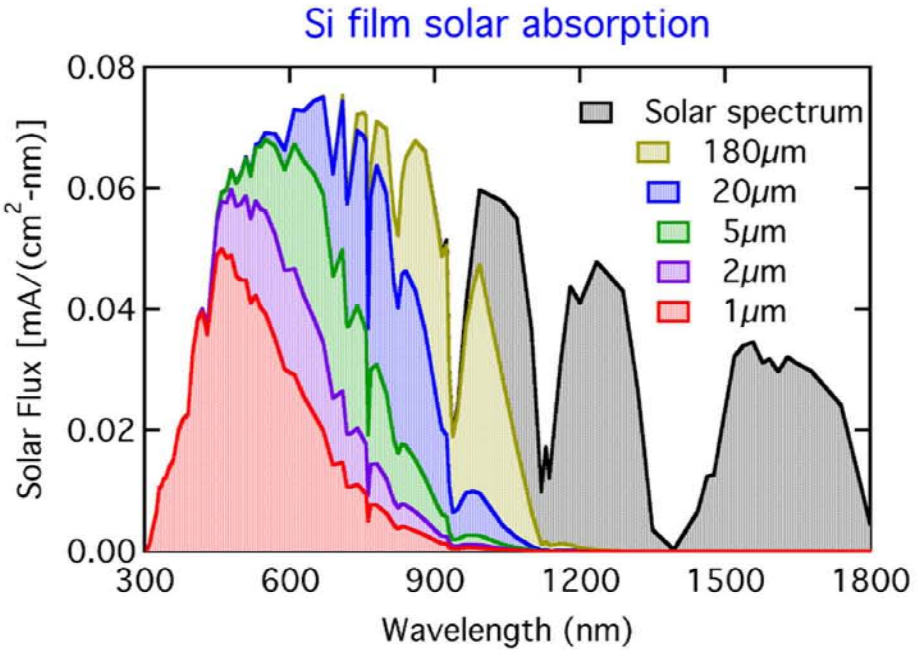
pure $SiHCl_3$ or SiH_4

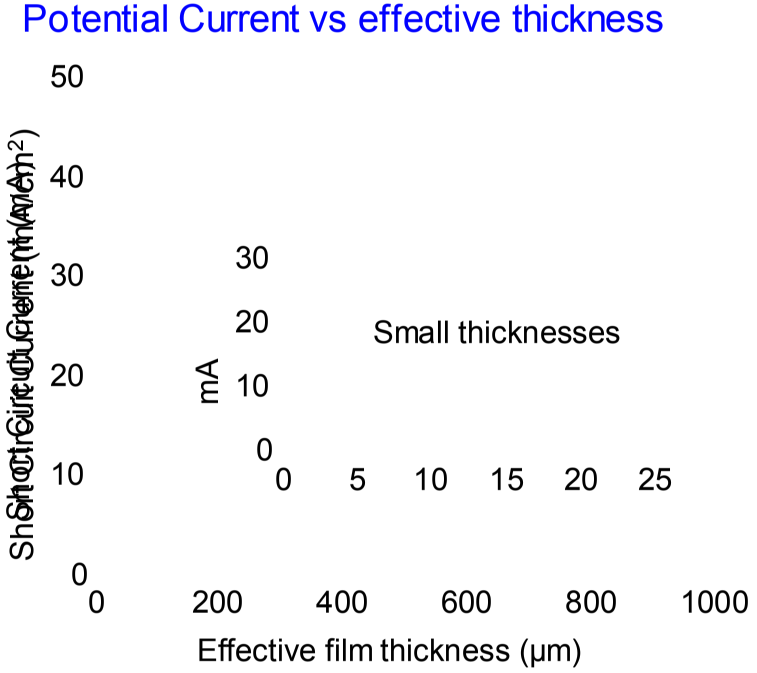
HWCVD is best low-T scalable technique



Directly deposit enough pure silicon for light absorption

Thick wafers not needed for c-Si PV



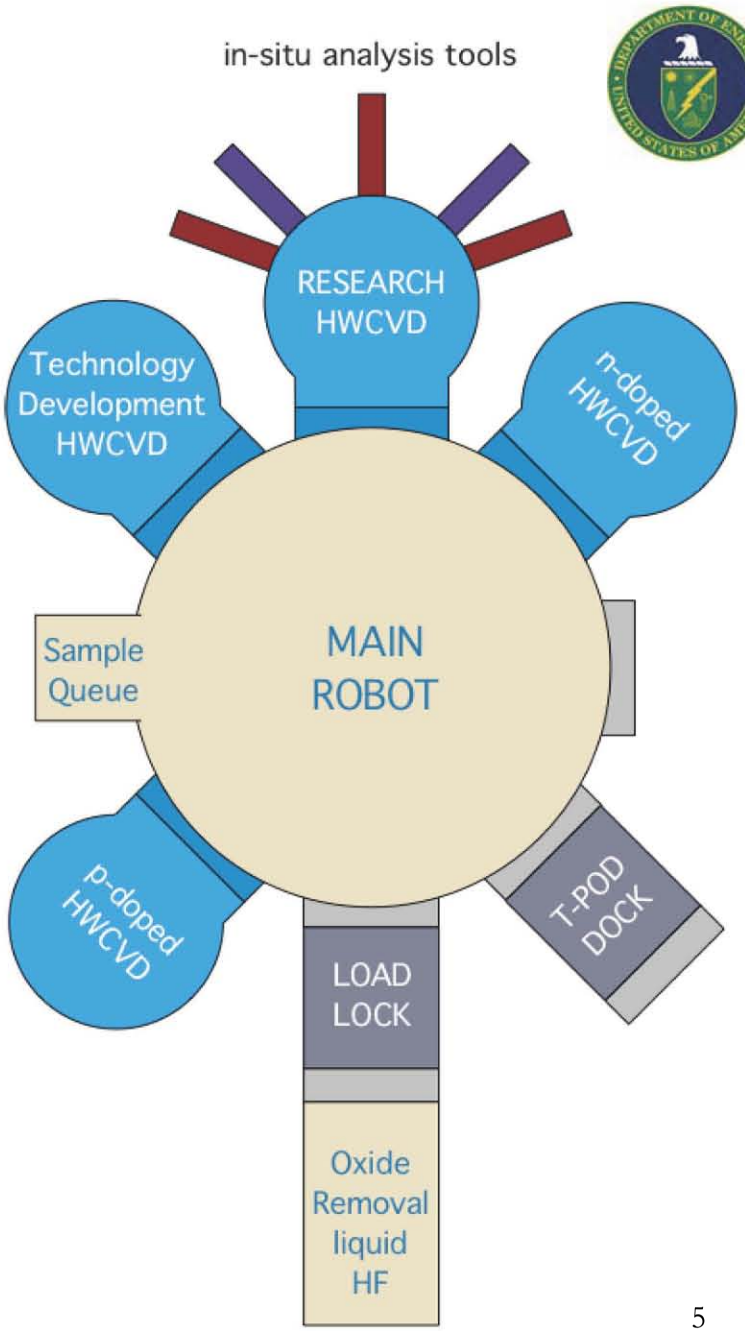


- Most current available at 20 μm effective thickness
- Over 30 mA attainable for 5-μm silicon with 5X light trapping
  - absorbs like 25 μm silicon layer

Tool and its capabilities

- Substrate to 800°C
- 156-mm samples queue in vacuum
- Automated liquid-based oxide removal
  - key last-minute step
- Doping control in separate chambers
  - n-type
  - p-type
- Research HWCVD
  - 10^{-8} Torr vacuum, low impurity
  - RTSE, RHEED, pyrometer, RGA
- Technology development HWCVD
  - Develop new filament and heater designs

- Load Lock
- Vacuum Transfer Pod to other PDIL Tools
- Spare port for alternatives and collaborations



Tool Alignment with Film c-Si Technology Roadmap

Roadmap

c-Si Film Technologies

Need	Significance
Develop inexpensive large-grain or single-crystal, high-quality c-Si film growth processes and materials for use with low-cost substrates	Higher efficiency than amorphous, but lower cost than wafer-based silicon
Develop seeding techniques for high-quality epitaxial c-Si film formation on low-cost substrates	Increased efficiency
Develop light-management strategies for weakly absorbing c-Si films	Increased efficiency
Develop inexpensive, high-temperature (>600°C) substrates for c-Si films	Reduced cost
Develop inexpensive, reduced-temperature processing for c-Si films	Reduced cost
Develop low-temperature passivation techniques for film-Si surfaces, interfaces, and grain boundaries	Increased efficiency
Develop, automate, and scale up deposition equipment for c-Si film fabrication	Reduced cost and increased yield

Wafer Replacement Tool

Scalable hot-wire (HWCVD) epitaxy
– 300 nm/min, 10 μm, with low dislocations
– Epitaxy on all orientations

Will enable us to evaluate seed layers

Will enable us to develop light-trapping at 6-inch scale

Will enable us to evaluate new substrates

Glass-compatible temperatures 600 - 700°C

Hot-wire hydrogenation possible, if needed

Technology development chamber and in-situ diagnostics

Status and schedule

- Conceptual design (chambers) complete
  - based on new test epitaxy chamber (1”)
- Detailed design work continuing
- Statement of work for RFQ in preparation
- Bids and vendor selection in FY08
- Delivery of robot and key chambers in FY09

Partnerships anticipated

- Seed layer candidates
  - semiconductor equipment companies
  - display companies
  - glass companies
  - start-ups
  - NREL R&D
  - university and national labs
- PV ventures testing low-T epitaxy step
- Equipment vendors
  - chamber to test HWCVD innovations

NREL Contacts

Chaz Teplin
charles_teplin@nrel.gov
303-384-6440

Paul Stradins
pauls_stradins@nrel.gov
303-384-6774

Howard Branz
howard_branz@nrel.gov
303-384-6694

CIGS Platform

Miguel Contreras

PV Technology Road Maps

Platform	Wafer Si	Film Si	CPV	CdTe	CIGS	OPV	DSPV
Thin Si							
Wafer Rep.							
CIGS							
CdTe							
Atm. Proc.							
M&C Ind.							
M&C Cluster							