Advanced Solid State Sensors for Vision 21 Systems
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ABSTRACT

Silicon carbide (SiC) is a high temperature semiconductor with the potential to meet the gas and temperature sensor needs in both present and future power generation systems. These devices have been and are currently being investigated for a variety of high temperature sensing applications. These include leak detection, fire detection, environmental control, and emissions monitoring. Electronically these sensors can be very simple Schottky diode structures that rely on gas-induced changes in electrical characteristics at the metal-semiconductor interface. In these devices, thermal stability of the interfaces has been shown to be an essential requirement for improving and maintaining sensor sensitivity and lifetime.

In this report, we describe device fabrication and characterization studies relevant to the development of SiC based gas and temperature sensors. Specifically, we have investigated the use of periodically stepped surfaces to improve the thermal stability of the metal semiconductor interface for simple Pd-SiC Schottky diodes. These periodically stepped surfaces have atomically flat terraces on the order of 200 nm wide separated by steps of 1.5 nm height. It should be noted that 1.5 nm is the unit cell height for the 6H-SiC (0001) substrates used in these studies. These surfaces contrast markedly with the "standard" SiC surfaces normally used in device fabrication. Obvious scratches and pots as well as subsurface defects characterize these standard surfaces. This research involved ultrahigh vacuum deposition and characterization studies to investigate the thermal stability of Pd-SiC Schottky diodes on both the stepped and standard surfaces, high temperature electrical characterization of these device structures, and high temperature electrical characterization of diodes under wet and dry oxidizing conditions. To our knowledge, these studies have yielded the first electrical characterization of actual sensor device structures fabricated under ultrahigh vacuum conditions.

The results demonstrate that the Pd-SiC interfaces formed on the stepped surface are remarkably stable at temperatures up to 670^{o}C and that there is a definite improvement in the electrical characteristics. This temperature, though lower than DOE target temperatures is still 100^{o}C higher than that used in reported field studies. The Pd films studied here ranged in thickness from the monolayer level (~0.4 nm) to actual device dimensions (~46.5 nm) and are deposited under ultrahigh vacuum conditions at ~50^{o}C. The films were characterized *in-situ* using Auger electron spectroscopy both before and after annealing at 670^{o}C. The Auger lineshapes were used to provide quantitative information on the chemistry of the reaction products. *Ex-situ* atomic force microscopy was used to characterize changes in surface morphology. Current-voltage (I-V) measurements were made as a function of temperature to further characterize the devices. Additional studies were performed to gain an understanding of the effects of wet and dry oxidizing environments on device performance. These measurements were performed for temperatures up to 325^{o}C, the highest temperature attainable with our current apparatus.

Our results clearly show a significant benefit in thermal stability and electrical characteristics associated with the stepped surface. These results are quite promising but much development and testing work remains to be done.

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Advanced Solid State Sensors for Vision 21 Systems

I. INTRODUCTION

a) Silicon Carbide Sensor Technology

Future power plants such as that illustrated in Figure 1 are envisioned as highly integrated, advanced technology modules operating at high efficiency with essentially zero environmental impact. Examples of the technologies that may be utilized in these systems include advanced coal gasification and combustion processes combined with turbines or fuel cells. To realize this ambitious goal, sophisticated computer algorithms will control the plant, and sensors will provide the real-time plant-computer interface.

Figure 1. Artist rendition of a future power plant. [From Vision 21 Technology Roadmap.]

At the present time, the needed sensor technologies are not available. Moreover, measurements of two of the most important process parameters, gas species concentrations and temperature, will be extremely challenging at the anticipated high temperatures in future coal-energy conversion processes. Despite these challenging conditions, there are emerging sensor technologies with the potential for performing the desired measurements. One of the most promising of these is based on presently emerging silicon carbide (SiC) technology.

SiC is wide band gap semiconductor that has exceptional high temperature properties and stability. SiC has two primary crystal forms, the cubic structure which has one polytype (β-SiC) and the hexagonal which has numerous polytypes (e.g., 4H- and 6H-SiC). Free standing, 2 and 3-inch diameter hexagonal type wafers of increasingly high quality are readily available today from and increasing number of vendors. These are grown by high temperature chemical vapor transport methods. Most cubic material is grown as thick films on commercial silicon (Si) substrates using chemical vapor deposition methods. The availability of high quality 4H- and 6H-SiC wafers represents a tremendous technology investment in hexagonal SiC wafer development by the Federal Government over the past 15 to 20 years.

The use of SiC as a high temperature electronics material has been the subject of study for many years.[1] Moreover, proof of principle measurements dating from the mid to late 1990's have been performed which demonstrate the materials potential for gas species measurements. One example of these is given in Figure 2 which shows CO measurements performed using a SiC sensor operating at 275 ^{o}C (left axis) and Fourier transformed infrared (FTIR) spectroscopy as a control (right axis) measurement.[2] Similar measurements have been obtained for H_2, NH_3, O_2, NO, CO, SO_2, and CH_4.[3,4] More recently, SiC gas sensor operation

has been demonstrated at temperatures of 425°C by NASA researchers[6] and 525°C in studies at General Electric.[7]

Current limitations on the use of SiC technology under harsh conditions are not due to the inherent materials properties of SiC but to thermal instability of the sensor structure and quite which are quite possibly due to defects produced in the chemo-mechanical polishing (finishing) of the SiC wafers themselves. To understand the origins of these limitations, it is helpful to have an understanding of the structure and operation of the devices themselves.

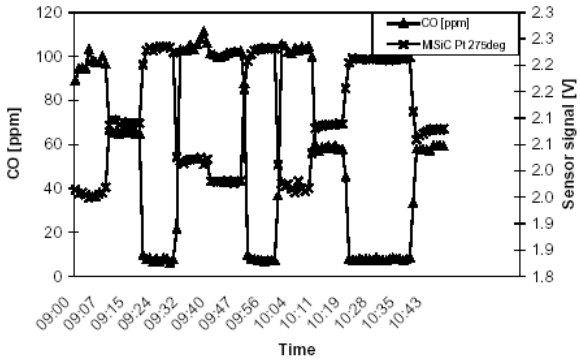


Figure 2. Experimental measurements of CO concentration versus time measured a SiC sensor operation at 275°C. [From Reference 2.]

An example of a metal-insulator-SiC (MISiC) type sensor structure is illustrated in Figure 3. It consists of thin SiO_2 and metal films deposited on a p-n junction. The junction itself is formed by the deposition of a thin n-type epitaxial SiC layer on a commercially available n-type 4H- or 6H-SiC substrate. The thickness of this epi-layer is in the range of 1-10 μm. Pt, Ir, Pd, or various alloys have been used for the metal film, which is frequently referred to as the catalyst.

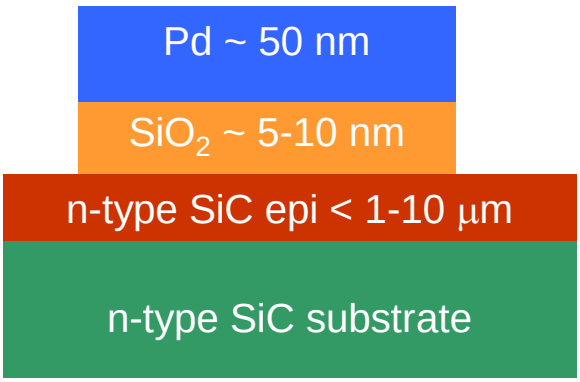


Figure 3. Schematic of MISiC type sensor structure used for gas and temperature sensing applications in harsh environments.

In operation, target molecules such as H_2 react with the metal surface to produce steady state concentration of surface intermediates. Due to charge transfer between the intermediates and the surface these species can be polarized, and the resulting polarization field shifts the electrical properties of the p-n junction.

The property of these structures that makes them useful as sensors is the fact that the shift in electrical characteristics is dependent on the target species. This is illustrated in Figure 4 where the shift in turn-on voltage for the p-n junction is shown for two different gases, H_2 and O_2.

The problem that arises is that over long term operation at high temperatures,[5] the sensitivity of the sensors degrades. Early sensors were simple Schottky diodes composed

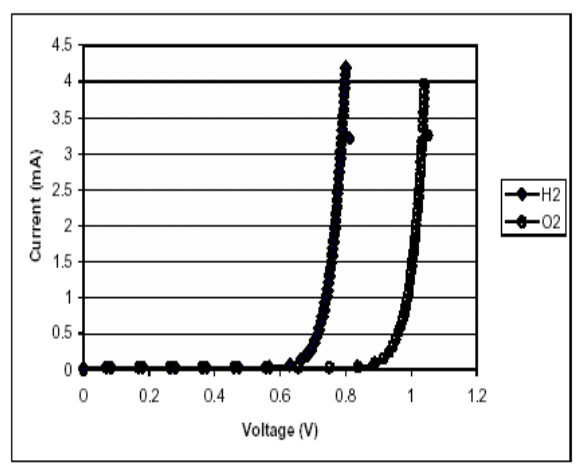


Figure 4. Experimental I-V curves for a SiC based sensor operating in the presence of H_2 and O_2. [From Reference 2.]

of a metal deposited directly on the SiC. It was observed, however, that annealing the devices for 140 hours at 425^{o}C reduced their sensitivity.[6] Auger depth profiling analyses of failed devices revealed that this was due to interdiffusion and reaction at the metal-semiconductor interface which produced various metal silicides and graphite. The device structure shown in Figure 3 was designed to circumvent this limitation. Specifically, the oxide layer was inserted to decrease the extent of interfacial diffusion and reaction between the metal and the substrate. It was found, however, that although the oxide layer stabilized the interface, the sensitivity rapidly decreased due to the formation of an SiO_x layer on the metal surface. This was thought to be due to the reduction in active gas dissociation sites on the metal and the formation of an electronic barrier.

b) <u>The Focus of This Research Program</u>

In order to produce SiC sensors with acceptable performance characteristics, research performed elsewhere has focused primarily device development aspects. For example, research at NASA Glenn Research Center has involved studies of relatively complex metal alloy systems for the catalyst layer.[8] While these studies have provided improvements in performance, they neglect a fundamental issue which may severely limit the thermal stability of all existing SiC device structures. Specifically, previous device studies have not investigated the role of surface and near surface substrate damage on thermal stability. When examined by a variety of non-destructive techniques, the best commercially available SiC wafers appear to have an excellent surface finish (i.e. average roughness less than 0.3 nm with no visible scratches). However, **<u>ALL</u>** commercially available wafer have varying levels of subsurface defects associated with the polishing process that are not benign with respect to device quality.[9]

During the device fabrication, surface and subsurface defects in the SiC substrate will propagate into the deposited films degrading the device performance and reducing device yield.[10,11] In addition, electrically active near surface defects have also been observed.[12] Finally, at operational temperatures the defects in the surface and near surface layers of the substrate will enhance interdiffusion processes and lead to accelerated failure rates.

Based on these considerations, **the research performed under this contract has focused on assessing the impact of improving the quality of the SiC substrate surface and near surface layers on the long term thermal stability of SiC sensors.** In these studies, we have used high temperature hydrogen (H_2) etching to remove several microns of material to yield surfaces with wide terraces (e.g., 200 nm) and unit cell step heights (i.e., 1.5 nm).[13,14] In this way, the surface and near surface damage associated with the polishing process is removed and high. This final report describes the results of studies to compare the thermal stability and electrical characteristics of Schottky diode sensors fabricated on these surfaces with those fabricated on standard SiC surfaces which have not had the polishing damage removed.

The thermal stability experiments were performed at West Virginia University and used a variety of surface and thin film methods to characterize changes in composition, structure, and surface morphology. The electrical characterization studies were performed at VA Tech. These studies included Schottky diodes on both standard and stepped surface that were fabricated at WVU and device structures that were fabricated at VA Tech.

II. EXPERIMENTAL

a) Thermal Stability Experiments

Commercially available n-type, 6H-SiC wafers were purchased from CREE Research Inc. and Sterling Semiconductor (now Dow Corning) and diced into 1 cm x 1 cm squares by American Precision Dicing. The wafers were production grade 1 with less than 100 micropipes/cm^2. The resistivity of the 50.8mm diameter, n-type wafers was between 0.09-0.12 W-cm. All wafers had vendor polished (0001)-Si faces. The Sterling wafers were cut on axis while CREE wafers were cut 3.5^o off axis. The electrical characteristics are described in more detail in the next subsection.

Prior to Pd deposition, the SiC surfaces were prepared using either of two methods. In the first, the sample was first degreased using tetrachloroethylene, acetone, and methanol. Then an HF based etch was used to remove the silicon oxide overlayer. This yielded the ***standard*** SiC surface typically used in device fabrication. In the second, an additional high temperature (1600 ^{o}C) H_2 etching step was used to create the ***stepped*** surface. The details of this preparation procedure will be discussed elsewhere [14].

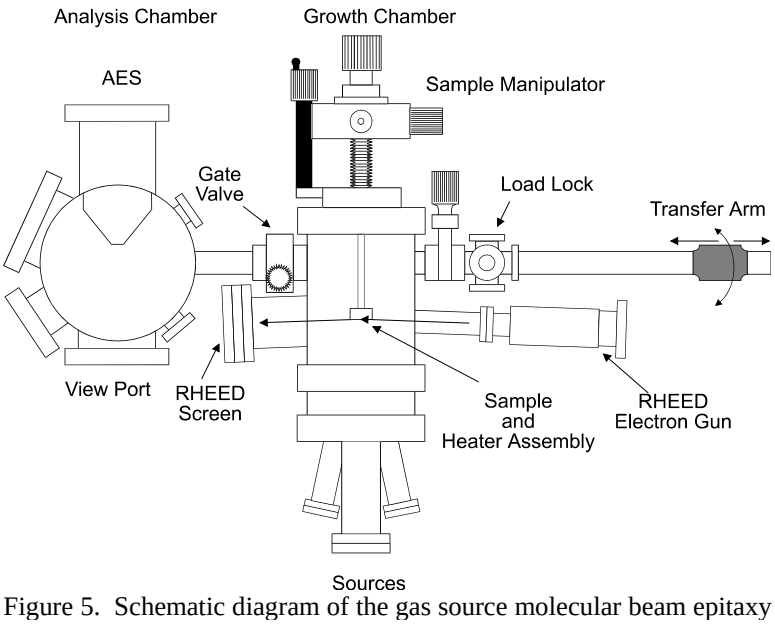


Figure 5. Schematic diagram of the gas source molecular beam epitaxy and surface characterization apparatus used in these studies.

Atomic force microscopy (AFM) analyses of the standard surfaces revealed random scratches and small pits left by the polishing process. It is thought that these observable surface features are associated with additional damage beneath the surface. Hydrogen etching of these substrates was used to remove material down to a depth of several microns, and this produced a periodically stepped surface with atomically flat terraces. Depending upon the angle at which the original surface was cut, the stepped surfaces had terraces of 25 nm – 200 nm wide and steps heights of on the order of 1.5 nm. That is, one unit cell high steps for 6H-SiC.

The pre-treated samples were mounted on a molybdenum puck and load-locked into the ultrahigh vacuum (UHV) growth and surface characterization apparatus shown in Figure 5. The growth chamber is pumped by two turbo molecular pumps and operates at a base pressure of $5x10^{-10}$ Torr. This sample manipulator allows precise positioning of the sample for both deposition and reflection high-energy electron diffraction (RHEED) analyses. In addition, the sample may be heated to temperatures on the order of 1000 ^{o}C. The metal for the deposition studies was provided using an EPI-10HT high temperature effusion cell located in a water-cooled source ports. The Pd source material used in the deposition studies was 99.99 % pure Pd supplied by (Electronic Source Products). Additional gas sources are available which allow thin

film growth using molecular and radical species. An Omega Model OS1562 fiber optic infrared sensor, also located on the source flange, was used for measuring substrate temperatures in the range of 400 to 1800 ^{o}C with an accuracy of ±1%. The size of the measurement spot at the substrate is ~1 mm in diameter so that substrates may be readily temperature profiled.

Once a deposition or growth sequence was completed, the sample was transferred to the analysis chamber for characterization using Auger electron spectroscopy (AES). This chamber was pumped by a 220 l/s ion pump and operates at a base pressure of $5x10^{-10}$ Torr.

Deposition rates for Pd were determined by weight gain. For both the standard and stepped surfaces, a series Pd films ranging in thickness from 0.4 to 46.5 nm were deposited at (nominally) 50 ^{o}C and then annealed at 670^{o}C. Based on a simple face centered cubic model for the Pd film and an atomic volume of 8.89 cm^3/mole [15], the thickness of the first monolayer is ~ 0.30 nm, while the addition of the second and third layers yield a film thickness of 0.52 nm and ~0.73 nm, respectively. The film thickness of 46.5 nm was chosen to match the nominal thickness of the metal layer used in the Schottky diode gas sensors [6].

At each step, before and after Pd deposition and after annealing, *in-situ* AES analyses were performed to determine the composition of the surface. *Ex-situ* AFM analyses (performed as terminal analyses of a selected samples) were used to characterize the surface morphology. The *in-situ* AES analyses were obtained using a PHI Model 545 scanning Auger microprobe. The *ex-situ* AFM analyses were obtained using a Joel Model 4210 located at the National Energy Technology Laboratory in Morgantown, WV.

AES peak intensities and known elemental sensitivity factors were used in a standard manner to determine the amount of each element present in the AES sampling volume [16]. In addition, the lineshape of AES transitions involving a valance band state are sensitive to the chemical bonding of the atoms in the solid. Thus, the Si-LMM, the C-KLL and, to a lesser extent, the Pd-MNN lineshapes were used to determine the chemical state of the surface. In particular, Bermudez [17] demonstrated that the stoichiometry of Pd_xSi films can be determined from the lineshape analysis of the Si-LMM AES peaks for silicide compounds.

b) <u>Electrical Characterization</u>

The 6H substrate wafers and die used in this portion of the experimental studies were the same as those used in the thermal stability studies. Following the removal of the die from the mounting tape, the die were soaked in acetone and then blown dry using dry nitrogen. Additional organics were removed from the surface of the SiC samples by placing the die in a Piranha etch for 5 minutes. The SiC samples were then transferred into a solution of 10:1 buffered oxide etch for 1 minute to remove the native oxide from the SiC surface. The samples were then rinsed in de-ionized water and blown dry. A second buffered oxide etch for 1 minute with DI water rinse and blow dry was performed immediately before the deposition of the metallization on the SiC surfaces.

A Thermionics e-beam system was used to deposit Pd and Ti/Au on to the SiC samples for form the Schottky and Ohmic contacts, respectively, at a base pressure of approximately

$4x10^{-9}$ Torr with a current between 150-250 mA. Two different thicknesses of Pd were used as the Schottky contact to the SiC, depending on the experiment to be run. A thin film of Pd, 25nm in thickness, was used on samples on which Auger emission spectroscopy was to be performed. Thicker Pd layers, 100nm in thickness, were deposited when electrical characterization of the Schottky contact was to be performed. The thinner layer of Pd reduced the time required to sputter through the Pd-SiC interface and improved the accuracy of the depth profile while the thicker layer of Pd eased the difficulties associated with making good mechanical contact of the electrical probe to the Pd on the SiC sample. To form uniformly sized, small area Schottky diodes, a shadow mask, a mesh formed by 16 mil wire with 34 x 34 mil holes, was placed on the surface of the SiC samples before the 100nm Pd layers were deposited. A broad area n-contact, composed of 10nm Ti followed by 100nm Au, was deposited on to the back surface of the SiC sample. Resistance measurements performed on patterned SiC samples indicated that the contacts were Ohmic as deposited.

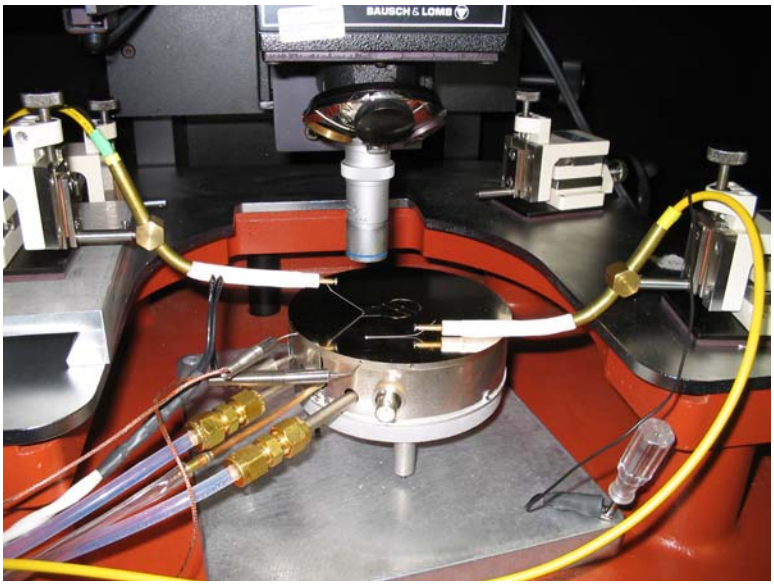


Figure 6. Signatone Probe Station with hot and cold chuck.

Electrical characteristics of the Schottky diodes fabricated in these studies were measured at room temperature before the diodes were annealed at 325°C under both dry and wet oxidizing conditions. The anneals were performed using a Quietemp S-1080R heated stage that was part of the Signatone probe station. This apparatus is shown in Figure 6. The heated stage was fitted with a custom-fabricated aluminum chamber in which the oxidations were performed. In the case of dry oxidations, the oxygen was simply allowed to flow at a rate of 100 sccm at 30 psi into the chamber while the Pd-SiC samples were held at 325°C. For the wet oxidations, the incoming oxygen was first bubbled through a flask containing water heated to 90 °C before flowing into the chamber. In the case of atmospheric oxidations, room air was allowed to enter the chamber while the Pd-SiC samples were at 325°C. The electrical characteristics of the Schottky diodes were measured during the anneals in the case of the atmospheric oxidations. For the Pd-SiC samples that underwent the dry and wet oxidations, the current versus voltage measurements were performed at 325°C immediately before the gas flow was initiated and again immediately after the gas flow was terminated. Electrical characterization of the Schottky diodes at room temperature was subsequently performed after the heated stage was allowed to cool to 25°C.

Depth profiling of the samples before and after thermal annealing was performed using a Perkin Elmer PHI610 Auger electron spectrometer (AES) with secondary ion mass spectrometry (SIMS) capabilities. A Perkin Elmer 5400 X-ray photoelectron spectrometer (XPS) with ion-

scattering spectrometry (ISS) capabilities was used to determine the chemical bonding of oxygen in several of the samples.

III. RESULTS AND DISCUSSION

a) Thermal Stability of Pd-SiC Schottky Diode Structures

Prior to annealing at 670°C, AFM analyses reveal that all deposited Pd films are conformal with the initial surface morphology. The AES lineshape analyses show that there are no surfaces reactions leading to silicide formation. After annealing at 670°C, however, the surface composition and morphology are found to be strong functions of the initial surface morphology and initial film thickness. In the subsequent discussion, all Pd film thickness values refer to the initial Pd film thickness prior to annealing.

Figure 7 shows the Si-LMM AES spectral region for a series of annealed Pd films on the standard SiC surface as well as reference spectra for the initial SiC surface and the 46.5 nm thick

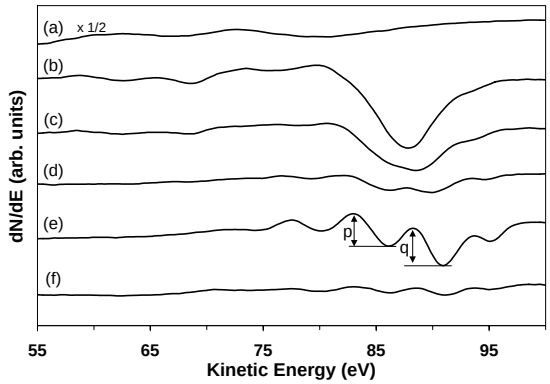


Figure 7. Si-LMM spectral region for a) a 46.5 nm thick Pd overlayer prior to annealing, b) the standard SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.7 nm, e) 8.5 nm, and f) 46.5 nm on the standard surface.

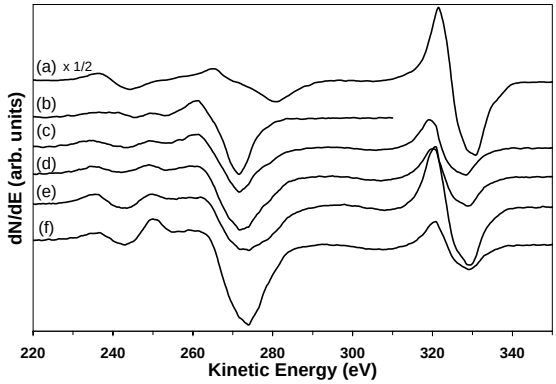


Figure 8. C-KLL and Pd-MNN spectral regions for a) the 46.5 nm thick Pd overlayer prior to annealing, b) the standard SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.7 nm, e) 8.5 nm, and f) 46.5 nm on the standard surface.

Pd overlayer prior to annealing. Figure 8 shows the corresponding C-KLL and Pd-MNN spectral regions. Compared with the reference spectrum for SiC (Figure 7b), the spectrum for the annealed 0.4 nm (~1 ML) film shown in Figure 7c shows evidence of attenuation. In addition, it provides evidence of broadening in the lower wing of the Si-LMM peak at 88 eV and the emergence of a weak shoulder at 94 eV. As seen in Figure 7a for the thick Pd overlayer, there are no elemental Pd features that can contribute to the Si-LMM lineshape in this region. Consequently the observed lineshape changes are indicative a reaction to form Pd_xSi. The spectra for the films of 0.7 nm (~3 ML) and 8.5 nm (~39 ML) thickness shown in Figures 1d and 1e, respectively, exhibit increasingly well-formed silicide peaks. Following Bermudez [17], the ratio of the peak-to-peak intensities identified as p and q in Figure 7e indicate that the composition of the silicide corresponds to $Pd_{x>4}Si$ for the 0.7 nm film and Pd_3Si for the 8.5 nm film. For the annealed 46.5 nm film (Figure 7f), the composition also corresponds to Pd_3Si, but the overall spectrum is significantly attenuated compared to Figure 7e.

Compared with the C-KLL reference spectrum for SiC shown in Figure 8b, the C-KLL lineshape for the 0.4 nm (~1 ML) film shown in Figure 8c provides evidence of broadening of the lower wing at 272 eV as well as a broadening and reduction in intensity of the upper wing at 255 eV. While there is no significant change in intensity of the feature at 250 eV, there is a sharpening of the plasmon feature at 236 eV. In the absence of Pd, these changes would be indicative of a conversion of carbon from the sp^3-C state in SiC to the sp^2-C state in graphite [9]. With Pd present, however, features in the Pd-MNN (Figure 8a) may also contribute to these changes. The situation is further complicated by the fact that Pd-MNN lineshape may change as Pd reacts with Si. Given the relative intensities of the Pd-MNN peaks, however, their main effect on the C-KLL peak in Figure 8c is simply to broaden the lower wing of the C-KLL peak. The lineshape changes associated with the upper wing of the C-KLL peak in Figure 8c are due primarily to graphite formation. As evidenced in Figures 2d – 2f, these changes continue with increasing initial Pd film thickness to the extent that the C-KLL lineshape in Figure 8f for the 46.5 nm film is representative of graphite rather than SiC.

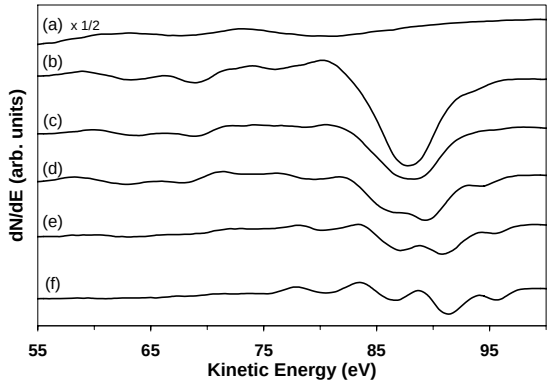


Figure 9. Si-LMM spectral region for a) a 46.5 nm thick Pd overlayer prior to annealing, b) the stepped SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.6 nm, e) 10.5 nm, and f) 46.5 nm on the stepped surface.

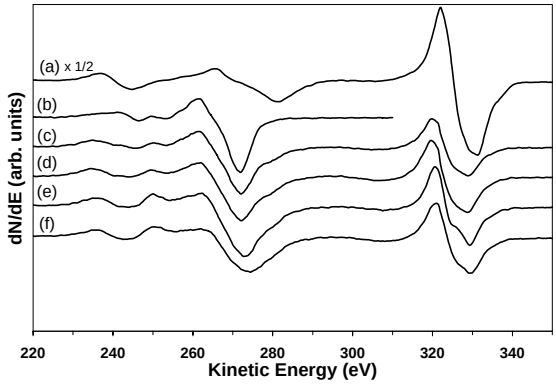


Figure 10. C-KLL and Pd-MNN spectral regions for a) the 46.5 nm thick Pd overlayer prior to annealing, b) the stepped SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.6 nm, e) 10.5 nm, and f) 46.5 nm on the stepped surface.

The Si-LMM spectra in Figure 7e and 1f both correspond to Pd_3Si. Consequently, we expect to see same amount of C (graphite) in the AES sampling volume because the stoichiometry is the same. In particular, since the lineshapes are not changing, the peak-to-peak C-KLL /Si-LMM intensity ratios should be the same. What is observed, however, is roughly ten-fold increase in this ratio on going from the 8.5 nm to the 46.5 nm film. For this to occur with no change in lineshape requires that the graphite overlay the silicide for the 46.5 nm film. Based on the attenuation of the Si-LMM peaks in Figure 8f relative to 2e, the thickness of the graphite layer is ~0.8 nm.

Figure 9 shows the Si-LMM AES spectral region for a series of annealed Pd films on the stepped SiC surface as well as reference spectra for the initial SiC surface and the 46.5 nm thick Pd overlayer prior to annealing. Figure 10 shows the corresponding C-KLL and Pd-MNN spectral regions. As before, there are no features in the Pd spectrum (Figure 9a) that can contribute to the Si-LMM lineshape. Compared with the spectrum for SiC (Figure 9b), the

spectrum for the 0.4 nm (~1 ML) film seen in Figure 9c is attenuated, as it should be, by the Pd overlayer, but otherwise shows no evidence of reaction to form the silicide. This contrasts with the standard surface where reaction to form Pd_xSi is observed, and it suggests that the stepped surface is more thermally stable than the standard surface. This is most likely due to improved crystal ordering for the stepped surface as compared to the standard surface that still has surface and near-surface damage associated with the polishing process. It is clear from this observation that reactant mobility plays a role in initiating reactions at the Pd-SiC interface.

The Si-LMM spectrum for the 0.6 nm film (~2 ML) shown in Figure 9d shows clear evidence of silicide formation, and the spectra for the 10.5 nm (Figure 9e) and 46.5 nm (Figure 9f) films exhibit increasingly well formed silicide peaks. Based on lineshape analyses, these films correspond, respectively, to $Pd_{x>4}Si$ and Pd_3Si.

The C-KLL spectra shown in Figure 10b to 4f are similar to those for the standard surface with respect to the conversion of sp^3-C to the sp^2-C. That is, we again observe lineshape changes

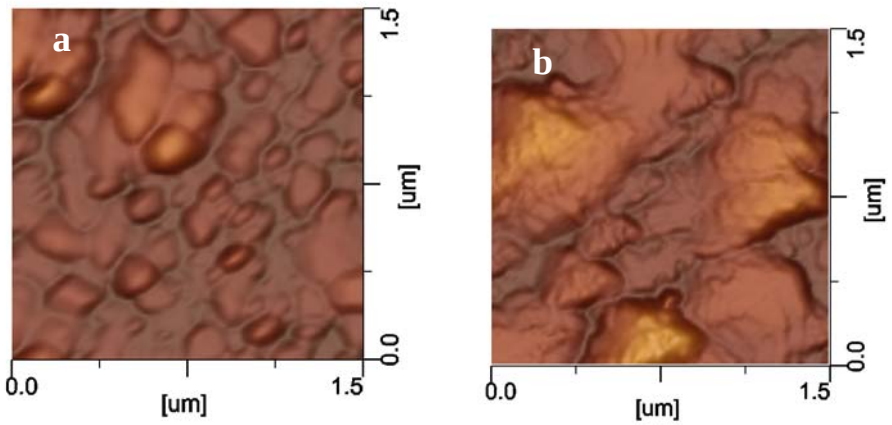


Figure 11 AFM images for a) an annealed 8.5 nm film on the standard SiC surface and b) an annealed 10.5 nm film on the stepped surface.

corresponding to graphite formation along with the reaction to form Pd_xSi. As just noted above, composition of the 10.5 nm and 46.5 nm films is $Pd_{x>4}Si$ and Pd_3Si, respectively. Thus, the graphitic contribution to the spectrum in Figure 10f should greater than that in Figure 10e. This, however, is not observed, and in fact, the overall intensity of the C-KLL in Figure 10f is slightly less than Figure 10e. This is consistent with the *silicide overlaying the graphite* on the stepped surface, which contrasts with a graphitic overlayer for the standard surface.

This behavior once again suggests possible differences in the reactant transport and mobility mechanisms for the stepped and standard surfaces. Specifically, the results are consistent with silicide growth by Si out diffusion and reaction on the stepped surface, while growth on the standard surface involves Pd in diffusion. In this case, it appears that the surface and near surface damage on the standard surfaces not only facilitates the initiation of the reaction but also helps to set the direction of reactant transport.

As mentioned previously the as deposited Pd films are conformal with the substrate surface. Annealing these films at 670^{o}C leads not only to silicide formation but also to characteristically different film morphologies that depend on the initial surface. Figure 11 shows AFM images of an annealed 8.5 nm film on the standard surface and a 10.5 nm film on the stepped surface. Here the different morphologies are evident. Hillock-like islands are formed on the standard surface (Figure 11a), while triangular crystallites are formed on the stepped surfaces (Figure 11b). AFM analyses of the thinner films reveal that the hillocks and triangular crystallites first appear as small, isolated features only after AES indicates the formation of Pd_xSi. This occurs for 0.4 nm films on the standard surface and 0.5 nm films on the stepped surface. As the initial film thickness increases, the hillocks and crystallites increase in size and extent of overlap. AFM line profiles show that the hillock-like features are columnar in structure, while the crystallites are relatively flat. For the 0.4 nm films on the stepped surface, we did not observe hillocks, crystallites, or Pd_xSi formation. This again suggests that the stepped surface is more thermally stable than the standard surface. The observed morphologies are consistent with the transport modes discussed above.

When a 46.5 nm Pd film on the standard surface was annealed at 670^{o}C, a hillock-like Pd_3Si structure was once again observed consistent with the morphology shown in Figure 11a. When a 46.5 nm Pd film on the stepped surface was annealed at 670^{o}C, hillock-like Pd_3Si features replaced the triangular crystallites observed for the thinner films. Thus, a different growth mode may exist for the thick Pd films on the stepped surface, or there may simply not be enough thermal energy in the system to allow the thicker film to crystallize at 670^{o}C.

b) Electrical Characterization

The purpose of this study was to correlate the changes in stability and sensitivity of SiC-based gas sensors with surface preparation and metal deposition technique. For simplicity and because there is a large body of operating experience, Pd-SiC Schottky diodes were the gas sensors studied in this work. In these devices, the current through the diode at a constant forward bias voltage increases with exposure to a gas such as hydrogen because the in-diffusion of the gas reduces the Schottky barrier height.[18] Due to equipment limitations, the Pd-SiC diodes fabricated in this study were tested up to a maximum temperature of 325^{o}C, which is below the temperatures at which other groups have tested the Pd-SiC gas sensors and is much lower than the desired operating temperature for a number of gas sensing applications.[18-20] None-the-less, we have been able to gain a fundamental understanding of the influence of surface preparation and metal deposition technique on stability and sensitivity of these devices.

Electrical Characterization of Stepped and Standard Surfaces

I-V measurements were carried out on a number of diode arrays formed on both standard and stepped surfaces under ultrahigh vacuum conditions. These were fabricated using either standard or stepped substrate and a shadow mask with openings that were on the approximately 0.8 mm x 0.8 mm. Figure 12 is a very low magnification scanning electron microscope image which shows a small portion of such an array. The magnification in this image is so low that circular lens aperture limits the area imaged (i.e., Note the four corners of the image). The light areas in the image are the 46 nm thick Pd film while the darker areas are the SiC substrate. The

slight distortion in the Pd squares is due to the non-uniformities in the mask. These could readily be eliminated but were of no consequence in the present work.

In addition to allowing multiple diodes to be formed on a single substrate, this approach also led to a reduction in device-device variations in characteristics. This is illustrated in Figure 13, which shows the forward I-C curves for four different diodes on the same substrate. The uniformity in these curves is remarkable given the current level of sophistication of the deposition and measurement schemes.

Figure 14 shows representative data for the forward and reverse I-V characteristics measured at 300 ^{o}C for diodes fabricated on both standard and stepped surfaces. If we assume that there are negligible surface states in the SiC following the high temperature hydrogen etching so that the that the Fermi level is unpinned at the surface, then the built-in voltage for a Pd-SiC Schottky diode at 300 ^{o}C is 0.77 V. Thus, the forward I-V curve in Figure 21a for the stepped SiC surface is clearly much closer to the ideal than that for the diode formed on the standard substrate surface. Furthermore, the reverse saturation current is lower and breakdown voltage is

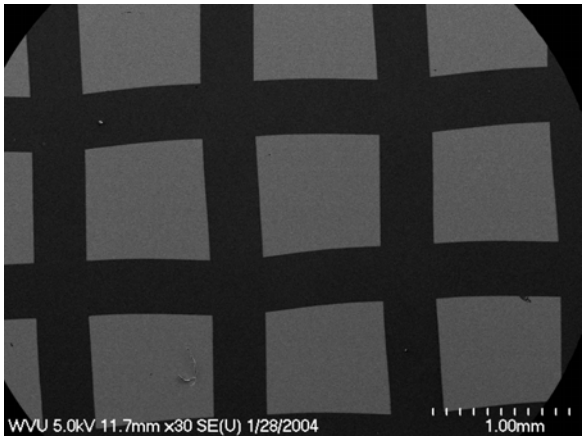


Figure 12. Patterned array (0.8 x 0.8 mm) of of Pd-SiC Schottky diodes deposited under ultrahigh vacuum conditions.

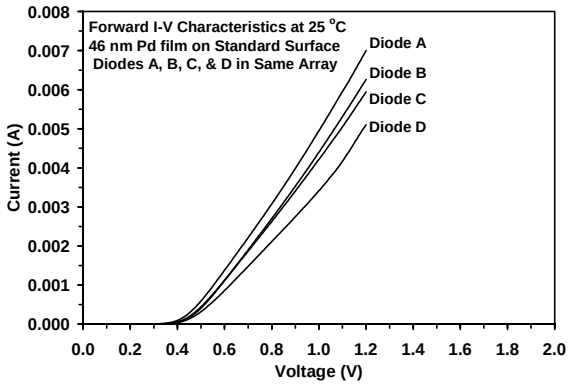
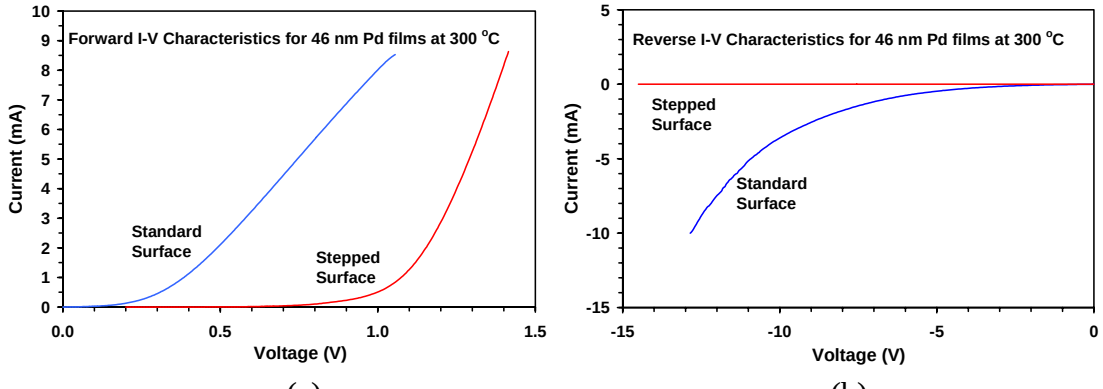


Figure 13. Forward I-V characteristics measured at 25^{o}C for four different diodes formed on the same substrate.



(a) (b)

Figure 14. a) Forward and b) reverse I-V characteristics measured at 300 ^{o}C for Pd-SiC Schottky diodes fabricated on both standard and stepped surfaces.

larger for the Schottky diode formed on the stepped surface. It is not known whether the hydrogen etch has altered the concentration of electrically active impurities near the surface of the SiC due to in-diffusion of hydrogen. C-V measurements performed in the future could be useful in resolving this issue.

Electrical Characterization in Oxidizing Environments

In the process of measuring the temperature dependence of the I-V characteristics of the Pd-SiC diodes, it was observed that the I-V characteristics were not stable while the devices were held at 325^{o}C in air. In fact, the I-V characteristics at 325^{o}C slowly improved with time until stabilizing. This time period for this stabilization to occur was 3 hours and was independent of Pd thickness for films ranging from 25nm to 100nm.

During the anneal, changes were observed in both the forward and reverse I-V characteristics. Specifically, the built-in voltage increased, the ideality factor improved, the reverse saturation current decreased, and the reverse breakdown voltage increased. Similar, but not identical, changes in the electrical characteristics of the diode at room temperature before and after the 325^{o}C anneal were observed. The exception was that the reverse breakdown voltage of the Pd-SiC diode at 25^{o}C decreased, rather than increased, after annealing.

Drift of the diode characteristics of Pd-SiC Schottky diodes, as well as a decrease in the gas sensor's sensitivity to hydrogen gas, has been noted previously by Hunter and co-workers.[19] A study was conducted on the effect of a 100^{o}C anneal on the electrical properties of a Pd-SiC Schottky diode.[20] The paper by Hunter and coworkers[19] demonstrated that the turn-on voltage of the diode increased as the temperature increased to 300^{o}C and then began to decrease at 400 ^{o}C. This was attributed to experimental error in measurement.

Our analysis of the forward I-V characteristics of some 20 diodes in prepared for this study indicates that this trend in the turn-on voltage as a function of anneal temperature is real. Some change in the I-V characteristics was expected due to increased activation of dopants in the n-type SiC, the formation of Pd_2Si during the anneal, and gettering of residual native oxides at the Pd-SiC interface. However, an increase in the electrically active donors does not explain the increase in the breakdown voltage. Nor does increased activation explain why changes were observed in the I-V characteristic at room temperature performed immediately following the 325^{o}C anneal. The formation of palladium silicide does not explain the magnitude of the changes in the I-V characteristics observed at 325^{o}C. A thin palladium silicide is known to form at room temperature at the interface of the Pd and SiC.[21] The work function of the silicide is similar to that of palladium, $\phi_m(Pd_2Si) = 5.0$ eV[22] versus $\phi_m(Pd) = 5.12$ eV. Therefore, there should be a minor difference in the turn-on voltage between a Pd-SiC and $Pd/Pd_2Si/SiC$ Schottky diode. None of these causes are adequate to explain the fact that the breakdown voltage of the diodes at 25^{o}C was degraded while other device parameters were improved following the anneal at 325^{o}C.

A series of experiments was conducted to identify the causes of the modification to the electrical characteristics of the Pd-SiC diodes. The Pd-SiC diodes were annealed in two different oxidizing environments, 100% O_2 anneal and O_2 saturated with water vapor. Electrical characterization of the diodes was conducted at 25^{o}C before and immediately following the

325°C and at the beginning and end of the 3 hour anneal. AES depth profiling analyses were performed on the as-deposited and annealed samples.

Dry Oxidative Environment

Following the initial electrical characterization at 25°C, the Pd-SiC diodes were placed in the test cell. The thickness of the Pd layer was 100nm to ease the formation of electrical contacts to the Pd by the stage probe. The flow of oxygen was initiated and then the temperature of the stage was increased to 325°C at a rate of ~ 0.25°C/s. When possible, I-V characteristics were collected during the anneal in addition to the ones taken at the beginning and end of the anneal. After completing the anneal, the temperature of the stage was ramped down to room temperature at a rate of 1 °C/m. Oxygen flow was maintained until the stage temperature reached 25°C.

There was some device-to-device variability in the initial device characteristics of the Pd-SiC as one would expect when testing large area diodes fabricated directly on SiC substrates. Multiple diodes were tested during these anneals. The trends in the changes of the device parameters, V_j, n, I_o, and V_{BR}, were consistent, though the magnitude of the changes and the final value of each device parameter were not. As can be noted from the electrical characteristics in Figure 15, significant changes in both the forward and reverse characteristic of the Pd-SiC diodes were observed. A comparison between these characteristics and those shown in Figure 16 which were obtained at 25°C demonstrates that the trends in the device parameters before and after anneal are not consistent. Specifically, the built-in voltage of the Schottky diode at 25°C has decreased following the anneal and the breakdown voltage has improved following the anneal.

AES depth profiling analyses were performed on Pd-SiC samples that were annealed under the same conditions. To facilitate the analysis, the thickness of the Pd was reduced to ~25nm. The results of these analyses are shown in Figures 17 and 18. Although there is a C-Pd peak overlap that enhances the carbon intensity, this has not been taken into account when calculating the carbon concentration. In Figure 17, it may be seen that there is some oxygen present at the air-Pd interface of the as-deposited Pd-SiC device. This is most likely due to adsorbed O_2 from the air.

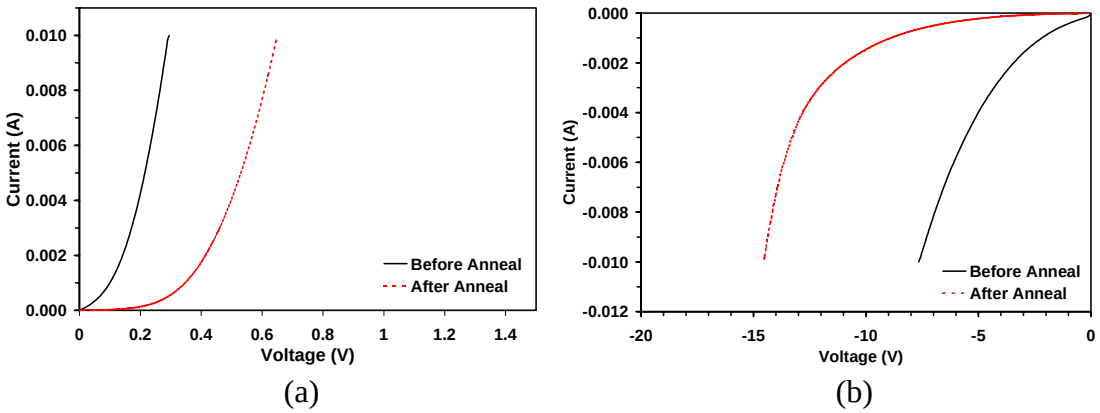


Figure 15. Electrical characteristics at 325°C of the Pd-SiC Schottky diode under a) forward and b) reverse bias before (solid line) and after (dotted line) a 3 hour, 325°C anneal in a dry oxidative environment.

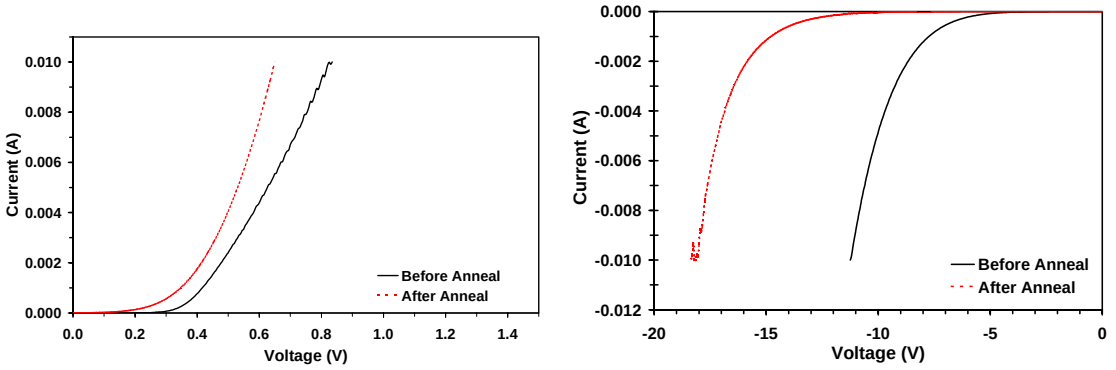


Figure 16. Electrical characteristics at 25°C of the same Pd-SiC Schottky diode under a) forward and b) reverse bias before (solid line) and after (dotted line) a 3 hour, 325°C anneal in a dry oxidative environment.

The Pd-SiC interface is relatively sharp. There is no observed oxygen signal at this interface, which demonstrates that the pre-clean used before Pd deposition was sufficient to remove any native oxide from the SiC substrate. As can be noted in Figure 18, oxygen is concentrated at the air-Pd interface and again at the Pd-SiC interface and a lower concentration of oxygen is present throughout the entire Pd layer following the anneal. This is consistent with the fact that oxygen in-diffuses into Pd at temperature greater than 200°C.[23] As a bulk oxide of palladium is not formed at these temperatures, the in-diffusing oxygen is free to move to the Pd-SiC interface.[24]

There is no evidence of decomposition of the SiC substrate or significant palladium silicide formation after the anneal is completed. Thus, we speculate that the changes in the I-V characteristic are a result of a formation of an interfacial layer of PdO and/or PdO_2, both of which are conducting oxides.[25,26] This interfacial layer will alter the positioning of the Fermi levels and influence the device parameters of the Schottky diode.

Wet Oxidative Environment

A similar testing procedure was used to determine the effects of water vapor on the electrical characteristics of the Pd-SiC diodes. For these experiments, the same protocol was

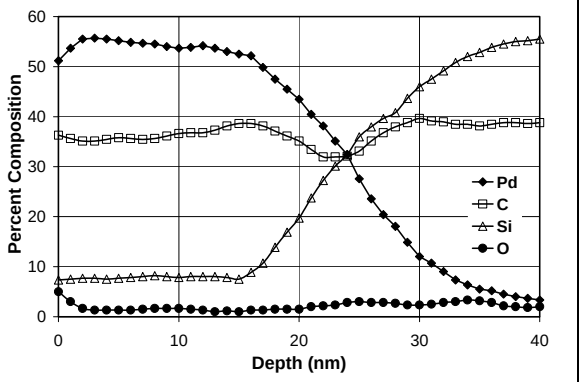


Figure 17. Auger depth profile of the as-deposited Pd-SiC diode.

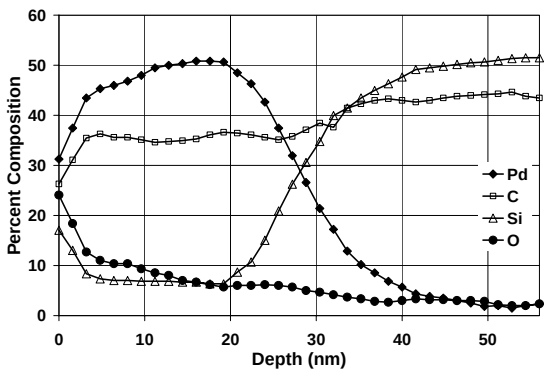


Figure 18. Auger depth profile of Pd-SiC diode following 3 hour, 325°C anneal in dry oxygen.

used with the exception that the oxygen flowed through 90°C water before entering the sample compartment. A difference between the two anneals was observed immediately following the completion of the anneal – the surface of the Pd was pink, rather than the gray metallic surface observed on the Pd-SiC samples before and after the dry oxidative anneal. Furthermore, electrical contacting of the Pd-SiC diodes was much more difficult during and following the anneal. A change in the I-V characteristics was again observed during the anneal. However, the I-V characteristics stabilized after 2 hours, rather than the 3 hours needed during the dry oxidative anneal.

The I-V characteristics measured at 325°C and 25°C following wet oxidation are shown in Figure 19 and 20, respectively. Due to device-to-device variability, as mentioned above, a direct comparison can not be made with the characteristics shown in Figures 15 and 16 for the dry oxidation. However, the reduction in the breakdown voltage at 25°C following the wet oxidative anneal was observed consistently from test to test. The degradation in breakdown voltage is consistent with that observed when the anneal was performed in air.

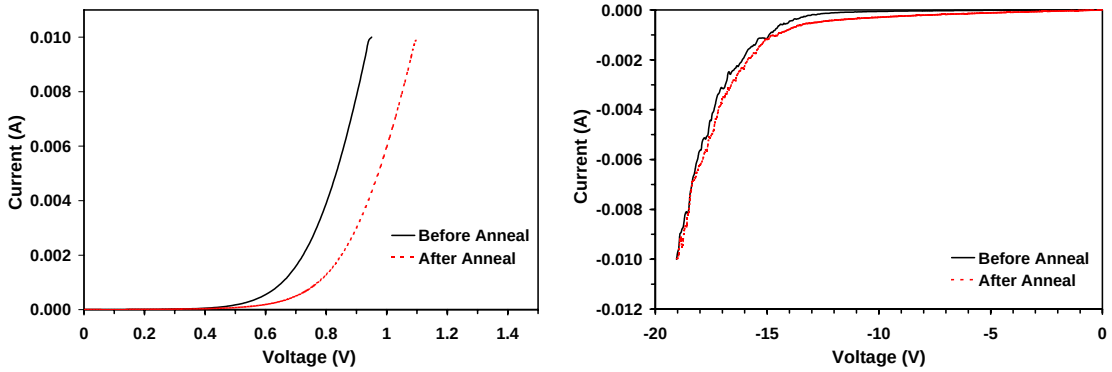


Figure 19. Electrical characteristics at 325°C of the Pd-SiC Schottky diode under a) forward and b) reverse bias before (solid line) and after (dotted line) a 3 hour, 325°C anneal in a wet oxidative environment.

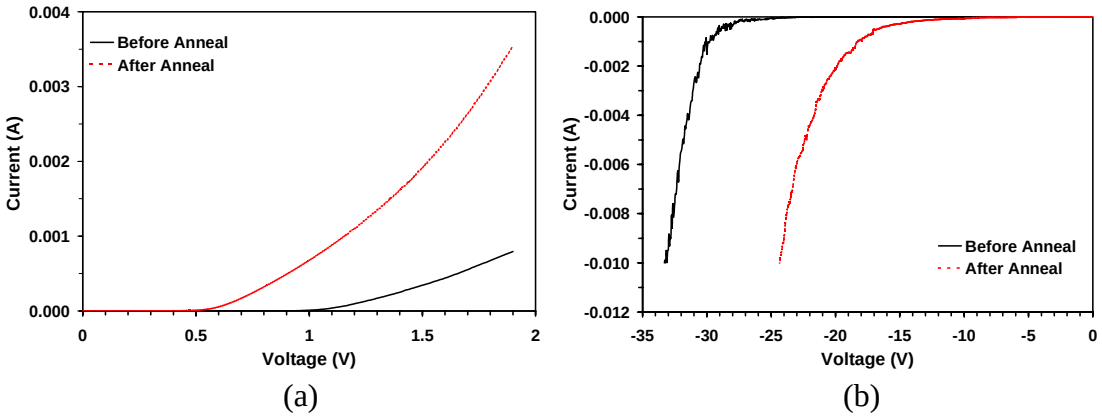


Figure 20. Electrical characteristics at 25°C of the Pd-SiC Schottky diode under a) forward and b) reverse bias before (solid line) and after (dotted line) a 3 hour, 325°C anneal in a wet oxidative environment.

Depth profiles on Pd-SiC samples that had undergone the wet oxidation are shown in Figure 21. Again, oxygen is observed throughout the Pd layer with significant concentrations found at the air-Pd and Pd-SiC interfaces. In contrast to the samples that underwent a dry oxidation, there is evidence of a reaction with the SiC substrates in these samples. There is a higher concentration of Si in the Pd layer and a peak associated with silicon at the Pd-air interface in addition to the oxygen peak. XPS analysis was performed on the surface of the sample, which confirmed that both SiO_2 and PdO_2 were present at the air-Pd interface, the latter contributed the reddish-pink tinge to the surface.

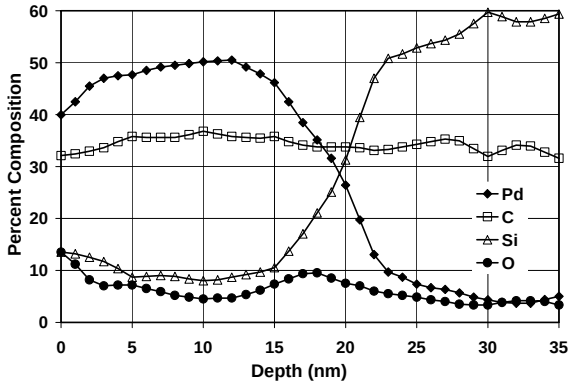


Figure 21. Auger depth profile of Pd-SiC diode following 3 hour, 325°C anneal in water vapor oxygen

Water has been shown to deactivate the catalytic activity of Pd and it is speculated that this deactivation is due to the formation of palladium hydroxide, $Pd(OH)_2$.[27] It is perhaps the deactivation of Pd which explains why PdO_2 is observed on the surface of the Pd following the anneal, rather than decomposition to PdO. The presence of $Pd(OH)_2$ along with the atomic Pd may then be responsible for the decomposition of the SiC substrate and the subsequent Si out-diffusion observed in the depth profiles obtained on the Pd-SiC samples following the wet oxidative anneal (Figure 18). Hydrous palladium oxide may have also formed at the Pd-SiC interface during the electrical testing of the Pd-SiC diodes, which was performed at regular intervals during the wet oxidization.[28] This non-conducting oxide is extremely stable and highly porous, which would enable water vapor to continue to in-diffuse to the SiC surface and to allow Si to easily out-diffuse. The formation of the silicon oxide at the surface of the Pd-SiC diode along with the formation of the various palladium oxides are likely the cause for the decrease in sensitivity of Pd-SiC gas sensors that has been observed by other.

An additional observation was that the electrical characteristics of the Pd-SiC diodes exposed to air or dry oxygen slowly reverted to the as-deposited electrical characteristics if left at room temperature for times greater than 24 hours. This implies that the modifications to the Schottky junction that occurred during the 325°C anneal were chemically unstable. That is, since palladium is a reactive metal, it acts as a catalyst for many reactions including the reduction of Pd_2Si to Si[29], the reduction of SiO_2 in the presence of Pd to Pd_2Si[30], the oxidation of Si in the presence of SiO_2 and Pd[31], and the reduction of PdO_2 and PdO to Pd by hydrogen[32]. While most of these reactions were documented at temperatures between 200-300°C, the temperature required to initiate the final reaction (PdO to Pd) was 20°C, room temperature. Furthermore, PdO_2 is unstable at high temperature and readily converts to PdO at temperatures greater than 200°C. Thus, these reactions supports our conclusions that a thin layer of palladium oxide, primarily composed of PdO, is formed at both the Pd-SiC and air-Pd interfaces during the 325°C anneal in a dry oxidizing environment.

During a 325^{o}C wet oxidative anneal, $Pd(OH^{-})_2$ is formed at the Pd-SiC interface during a anneal, which chemically attacks the SiC substrate to allow the out-diffusion of Si to the air-Pd surface. At the surface, both SiO_2 and PdO_2 are formed, which inhibit the in-diffusion of gases and reduce the catalytic activity of the Pd, leading to a reduction in sensitivity of the Pd-SiC gas sensors.

IV. ASSESSMENT AND CONCLUSIONS

SiC is a high temperature semiconductor with great potential for present and future power generation systems. It has been shown that simple SiC based sensors are responsive to gas species such as H_2, NH_3, O_2, NO, CO, SO_2, and CH_4 and other hydrocarbons which are of interest in energy systems. Beyond this however, DOE and other planners also need to know at what temperatures and in what environments these sensors can operate as well as what sensor lifetimes can be expected under these conditions.

Numerous groups, some funded by DOE, others sponsored by industry and other federal agencies, are addressing various aspects of this problem by looking at alternative device structures. The research performed under this DOE contract clearly demonstrates that there is yet one more parameter that has not been considered in any of the previous efforts. Specifically, this is the quality of the SiC wafer surface and near surface layers as provided by current SiC wafer polishing techniques. Our results, as well as the work of others, show these surfaces are highly defective. The studies performed here show that these defective layers are not removed by standard SiC wafer processing techniques and that they enhance the type of interdiffusion processes known to degrade sensors under operational conditions. Moreover, this work shows that when these defective layers are removed, the resulting substrates and device structures formed on these surfaces are more thermally stable.

In the present work, we have limited our attention to the simplest device structures, Pd-SiC Schottky diodes, to allow the most clear-cut and straightforward analysis of our results and their implications. Other types of device structures such as MISiC and MOSFET will be impacted by the similar degradation mechanism although on different temperature and time scales.

As deposited Pd films on both standard and stepped 6H-SiC surfaces are conformal with the initial surface morphology regardless of thickness for films ranging from 0.4 nm to 46.5 nm. That is, from monolayer to device dimensions. There is no apparent room temperature reaction to form Pd_xSi. When these films are annealed at 670^{o}C, however, the resulting morphology and composition are strong functions of the initial surface morphology and film thickness.

With respect to the formation of Pd_xSi, the stepped surface appears to be more thermally stable than the standard surface. This is most likely due to enhanced reactant mobility in the damaged surface and near surface layers of the standard surface. For annealed thin Pd films (0.4 nm to 10.5 nm) on the stepped surfaces, it appears that silicide growth occurs by out diffusion of Si accompanied by the conversion Si depleted SiC layers to graphite. For the standard surface Pd in diffusion may be play a role. Again, the stage appears to be set for this by the surface and near surface damage on the standard surfaces.

The morphology of the annealed films is quite dependent on the initial surface with triangular crystallites being formed on the stepped surfaces and hillock-like clusters being formed on the standard surface. For thick 46.5 nm films, the silicide morphology is hillock-like regardless of initial surface conditions. This may simply be insufficient thermal energy to crystallize thick Pd_xSi film on stepped surface. Another difference between the stepped and standard surfaces is the presence of a graphitic overlayer on the silicide grown on the standard surface. This may again be indicative of different transport mechanism for the two surfaces.

The electrical characteristics of Pd-SiC Schottky diodes as a function of time were measured at 325^{o}C in air. The device parameters characterized initially and after 3 hours at 325^{o}C at which time the I-V characteristics had stabilized and were significantly different with major increases in the built-in and breakdown voltages and reductions in the ideality factor and reverse saturation currents being observed. Subsequent anneals in dry and wet oxidative environments indicate that two different processes are initiated. In the case of the dry oxidative anneal, oxygen in-diffuses to the Pd-SiC interface and reacts with the Pd to form a palladium oxide primarily composed of PdO. This interfacial layer alters the I-V characteristics of the Pd-SiC diode. In the case of the wet oxidative anneal, both oxygen and water in-diffuse to the Pd-SiC interface. The water vapor reacts with Pd at the Pd-SiC interface to form $Pd(OH^-)_2$ and hydrous palladium oxide during electrical testing. The $Pd(OH^-)_2$ attacks the SiC, which allows the out-diffusion of Si from the SiC substrate to the air-Pd surface. The formation of SiO_2 and PdO_2 at this surface impedes the ability for form good electrical contacts to the Pd-SiC.

We theorize that the in-diffusion of water vapor is the dominant factor in the altered electrical characteristics of the Pd-SiC Schottky diodes annealed in air and that the oxide formation at the air-Pd interface is continually reduced by other gases present during the anneal. We speculate that the presence of these two oxides along with the palladium hydroxide may account for the observed decrease in sensitivity of Pd-SiC gas sensors.

Additional studies are necessary to understand the complex interactions between oxidizing and reducing gases, SiC, and the catalyst, Pd, on the characteristics of the SiC gas sensors. The stability of the interface between the Pd and SiC is clearly important to achieve predictable sensitivity and longevity of these sensors. Thus, characterization of the chemical profile of the gas sensor at higher temperatures, operated under a wider set of gaseous environments, and with known interfacial layers between the Pd and SiC must be performed.

Preliminary studies of the effect of hydrogen on the Pd-SiC diodes following the exposure to the oxidizing environments indicate that the surface oxide on the Pd is reduced. Long-term studies are needed to determine if the oxidation of the SiC at the Pd-SiC interface and the out-diffusion of Si results in a progressive migration of the physical location of the Pd-SiC junction and if there are gas sensitivity and device reliability issues that result from the oxidation processes.

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VI. PUBLICATIONS

Interdiffusion and Reaction of Pd on Atomically Stepped 6H-SiC Surfaces: Progress Toward Thermally Stable High Temperature Gas Sensors, C.D. Stinespring, C.Y. Peng, A.A. Woodworth, K. Meehan, M.J. Murdoch-Kitt, and C.L. Anderson, Mat. Res. Soc. Symp. Proc. (2004) (Accepted / To Appear / Attached).

Characterization of the Metal-Semiconductor Interface for Silicon Carbide Based Sensors, A.A. Woodworth, C.Y. Peng, C.D. Stinespring, and K. Meehan, NATO-Advanced Studies Institute, Nanostructured and Advanced Materials for Optoelectronic and Sensor Applications September 6-17 2004 Sozopol, Bulgaria (Accepteed / To Appear / Attached).

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Interdiffusion and Reaction of Pd on Atomically Stepped 6H-SiC Surfaces: Progress Toward Thermally Stable High Temperature Gas Sensors

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ABSTRACT

High temperature Pd-SiC Schottky diode gas sensors are known to thermally degrade due to interdiffusion and reaction at the metal-semiconductor interface. To understand and possibly eliminate this problem, detailed surface studies of thermally induced Pd-SiC surface interactions have been performed. These experiments compare ***standard*** 6H-SiC (0001) surfaces typical of those used in device fabrication with periodically ***stepped*** surfaces prepared by high temperature hydrogen etching. The Pd films range in thickness from the monolayer level (~0.4 nm) to actual device dimensions (~46.5 nm) and are deposited under ultrahigh vacuum conditions at ~50 ^{o}C. These films are characterized *in-situ* using Auger electron spectroscopy both before and after annealing at 670 ^{o}C. The Auger lineshapes provide quantitative information on the chemistry of the reaction products. *Ex-situ* atomic force microscopy is used to characterize changes in surface morphology.

INTRODUCTION

SiC is a robust, wide band gap semiconductor suitable for fabricating high temperature gas sensors [1]. One of the simplest sensor structures studied to date has been the Pd-SiC Schottky diode. These devices change their electrical characteristics when gases such as H_2, O_2, CO, NO, and hydrocarbons are adsorbed on the metal contact [2].

Sensor lifetime studies indicate that thermally induced compositional and structural changes at the Pd-SiC interface adversely impact sensor performance [3]. One factor that may contribute to this thermal instability is the quality of the SiC substrate surfaces on which the devices are fabricated. The vendor supplied 6H-SiC substrates have a varying number of surface and sub-surface defects associated with the polishing process. High temperature hydrogen etching can be used to remove several microns of this damaged material and yields periodically stepped surfaces with unit cell high steps and atomically flat terraces [4].

In this paper, we report studies that compare the thermally induced changes in Pd thin films deposited on stepped SiC surfaces with those observed on the standard surfaces commonly used in SiC sensor device fabrication. These results provide a basis for understanding the degradation mechanism and will ultimately be extended to more advanced sensor designs.

EXPERIMENTAL PROCEDURE

Commercially available n-type, 6H-SiC wafers were purchased from CREE Research Inc. and Sterling Semiconductor and diced into 1 cm x 1 cm squares. All wafers had vendor

polished (0001)-Si faces. Sterling samples were cut on axis while CREE wafers were cut 3.5^{o} off axis.

Prior to Pd deposition, the SiC surfaces were prepared using either of two methods. In the first, the sample was first degreased using tetrachloroethylene, acetone, and methanol. Then an HF based etch was used to remove the silicon oxide overlayer. This yielded the ***standard*** SiC surface typically used in device fabrication. In the second, an additional high temperature (1600 ^{o}C) H_2 etching step was used to create the ***stepped*** surface. The details of this preparation procedure will be discussed elsewhere [5].

Atomic force microscopy (AFM) analyses of the standard surfaces revealed random scratches and small pits left by the polishing process. It is thought that these observable surface features are associated with additional damage beneath the surface. Hydrogen etching of these substrates was used to remove material down to a depth of several microns, and this produced a periodically stepped surface with atomically flat terraces. Depending upon the angle at which the original surface was cut, the stepped surfaces had terraces of 25 nm – 200 nm wide and steps heights of on the order of 1.5 nm. That is, one unit cell high steps for 6H-SiC.

The pre-treated samples were mounted on a molybdenum puck and load-locked into the ultrahigh vacuum (UHV) growth system. The growth system was equipped with an effusion cell for Pd deposition, a resistance heater used in annealing the sample, an optical pyrometer to measure the front face temperature of the sample, and a thermocouple to measure rear face temperature. In an adjacent, interlocked UHV chamber, facilities were available for Auger electron spectroscopy (AES).

Deposition rates for Pd were determined by weight gain. For both the standard and stepped surfaces, a series Pd films ranging in thickness from 0.4 to 46.5 nm were deposited at (nominally) 50 ^{o}C and then annealed at 670 ^{o}C. Based on a simple face centered cubic model for the Pd film and an atomic volume of 8.89 cm^3/mole [6], the thickness of the first monolayer is ~ 0.30 nm, while the addition of the second and third layers yield a film thickness of 0.52 nm and ~0.73 nm, respectively. The film thickness of 46.5 nm was chosen to match the nominal thickness of the metal layer used in the Schottky diode gas sensors [3].

At each step, before and after Pd deposition and after annealing, *in-situ* AES analyses were performed to determine the composition of the surface. *Ex-situ* AFM analyses (performed as terminal analyses of a selected samples) were used to characterize the surface morphology. AES peak intensities and known elemental sensitivity factors were used in a standard manner to determine the amount of each element present in the AES sampling volume [7]. In addition, the lineshape of AES transitions involving a valance band state are sensitive to the chemical bonding of the atoms in the solid. Thus, the Si-LMM, the C-KLL and, to a lesser extent, the Pd-MNN lineshapes were used to determine the chemical state of the surface. In particular, Bermudez [8] demonstrated that the stoichiometry of Pd_xSi films can be determined from the lineshape analysis of the Si-LMM AES peaks for silicide compounds.

RESULTS AND DISCUSSION

Prior to annealing at 670 ^{o}C, AFM analyses reveal that all deposited Pd films are conformal with the initial surface morphology. The AES lineshape analyses show that there are no surfaces reactions leading to silicide formation. After annealing at 670 ^{o}C, however, the surface composition and morphology are found to be strong functions of the initial surface

morphology and initial film thickness. In the subsequent discussion, all Pd film thickness values refer to the initial Pd film thickness prior to annealing.

Figure 1 shows the Si-LMM AES spectral region for a series of annealed Pd films on the standard SiC surface as well as reference spectra for the initial SiC surface and the 46.5 nm thick Pd overlayer prior to annealing. Figure 2 shows the corresponding C-KLL and Pd-MNN spectral regions. Compared with the reference spectrum for SiC (Figure 1b), the spectrum for the annealed 0.4 nm (~1 ML) film shown in Figure 1c shows evidence of attenuation. In addition, it provides evidence of broadening in the lower wing of the Si-LMM peak at 88 eV and the emergence of a weak shoulder at 94 eV. As seen in Figure 1a for the thick Pd overlayer, there are no elemental Pd features that can contribute to the Si-LMM lineshape in this region. Consequently the observed lineshape changes are indicative a reaction to form Pd_xSi. The spectra for the films of 0.7 nm (~3 ML) and 8.5 nm (~39 ML) thickness shown in Figures 1d and 1e, respectively, exhibit increasingly well-formed silicide peaks. Following Bermudez [8], the ratio of the peak-to-peak intensities identified as p and q in Figure 1e indicate that the

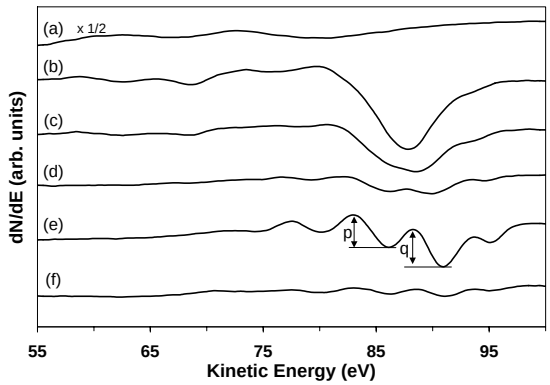

Figure 1. Si-LMM spectral region for a) a 46.5 nm thick Pd overlayer prior to annealing, b) the standard SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.7 nm, e) 8.5 nm, and f) 46.5 nm on the standard surface.

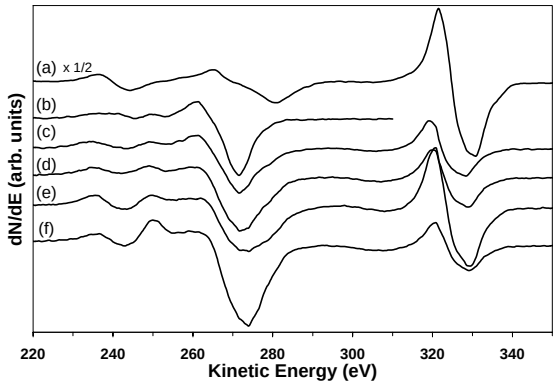

Figure 2. C-KLL and Pd-MNN spectral regions for a) the 46.5 nm thick Pd overlayer prior to annealing, b) the standard SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.7 nm, e) 8.5 nm, and f) 46.5 nm on the standard surface.

composition of the silicide corresponds to $Pd_{x>4}Si$ for the 0.7 nm film and Pd_3Si for the 8.5 nm film. For the annealed 46.5 nm film (Figure 1f), the composition also corresponds to Pd_3Si, but the overall spectrum is significantly attenuated compared to Figure 1e.

Compared with the C-KLL reference spectrum for SiC shown in Figure 2b, the C-KLL lineshape for the 0.4 nm (~1 ML) film shown in Figure 2c provides evidence of broadening of the lower wing at 272 eV as well as a broadening and reduction in intensity of the upper wing at 255 eV. While there is no significant change in intensity of the feature at 250 eV, there is a sharpening of the plasmon feature at 236 eV. In the absence of Pd, these changes would be indicative of a conversion of carbon from the sp^3-C state in SiC to the sp^2-C state in graphite [9]. With Pd present, however, features in the Pd-MNN (Figure 2a) may also contribute to these changes. The situation is further complicated by the fact that Pd-MNN lineshape may change as Pd reacts with Si. Given the relative intensities of the Pd-MNN peaks, however, their main effect on the C-KLL peak in Figure 2c is simply to broaden the lower wing of the C-KLL peak.

The lineshape changes associated with the upper wing of the C-KLL peak in Figure 2c are due primarily to graphite formation. As evidenced in Figures 2d – 2f, these changes continue with increasing initial Pd film thickness to the extent that the C-KLL lineshape in Figure 2f for the 46.5 nm film is representative of graphite rather than SiC.

The Si-LMM spectra in Figure 1e and 1f both correspond to Pd_3Si. Consequently, we expect to see same amount of C (graphite) in the AES sampling volume because the stoichiometry is the same. In particular, since the lineshapes are not changing, the peak-to-peak C-KLL /Si-LMM intensity ratios should be the same. What is observed, however, is roughly ten-fold increase in this ratio on going from the 8.5 nm to the 46.5 nm film. For this to occur with no change in lineshape requires that the graphite overlay the silicide for the 46.5 nm film. Based on the attenuation of the Si-LMM peaks in Figure 2f relative to 2e, the thickness of the graphite layer is ~0.8 nm.

Figure 3 shows the Si-LMM AES spectral region for a series of annealed Pd films on the stepped SiC surface as well as reference spectra for the initial SiC surface and the 46.5 nm thick

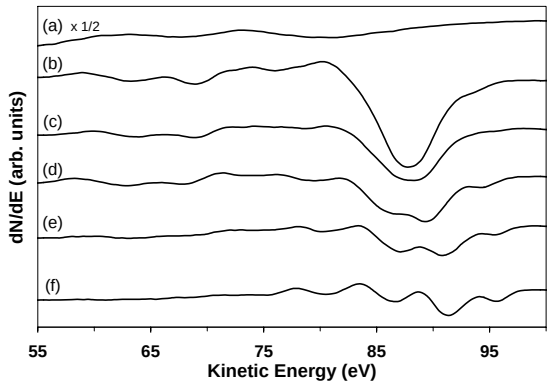

Figure 3. Si-LMM spectral region for a) a 46.5 nm thick Pd overlayer prior to annealing, b) the stepped SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.6 nm, e) 10.5 nm, and f) 46.5 nm on the stepped surface.

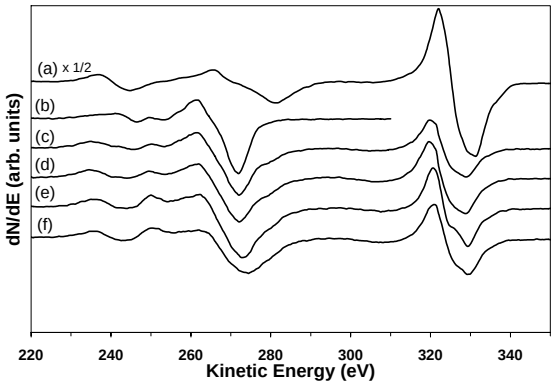

Figure 4. C-KLL and Pd-MNN spectral regions for a) the 46.5 nm thick Pd overlayer prior to annealing, b) the stepped SiC substrate, and annealed Pd films of thickness c) 0.4 nm, d) 0.6 nm, e) 10.5 nm, and f) 46.5 nm on the stepped surface.

Pd overlayer prior to annealing. Figure 4 shows the corresponding C-KLL and Pd-MNN spectral regions. As before, there are no features in the Pd spectrum (Figure 3a) that can contribute to the Si-LMM lineshape. Compared with the spectrum for SiC (Figure 3b), the spectrum for the 0.4 nm (~1 ML) film seen in Figure 3c is attenuated, as it should be, by the Pd overlayer, but otherwise shows no evidence of reaction to form the silicide. This contrasts with the standard surface where reaction to form Pd_xSi is observed, and it suggests that the stepped surface is more thermally stable than the standard surface. This is most likely due to improved crystal ordering for the stepped surface as compared to the standard surface that still has surface and near-surface damage associated with the polishing process. It is clear from this observation that reactant mobility plays a role in initiating reactions at the Pd-SiC interface.

The Si-LMM spectrum for the 0.6 nm film (~2 ML) shown in Figure 3d shows clear evidence of silicide formation, and the spectra for the 10.5 nm (Figure 3e) and 46.5 nm (Figure

3f) films exhibit increasingly well formed silicide peaks. Based on lineshape analyses, these films correspond, respectively, to $Pd_{x>4}Si$ and Pd_3Si.

The C-KLL spectra shown in Figure 4b to 4f are similar to those for the standard surface with respect to the conversion of sp^3-C to the sp^2-C. That is, we again observe lineshape changes corresponding to graphite formation along with the reaction to form Pd_xSi. As just noted above, composition of the 10.5 nm and 46.5 nm films is $Pd_{x>4}Si$ and Pd_3Si, respectively. Thus, the graphitic contribution to the spectrum in Figure 4f should greater than that in Figure 4e. This, however, is not observed, and in fact, the overall intensity of the C-KLL in Figure 4f is slightly less than Figure 4e. This is consistent with the *silicide overlaying the graphite* on the stepped surface, which contrasts with a graphitic overlayer for the standard surface.

This behavior once again suggests possible differences in the reactant transport and mobility mechanisms for the stepped and standard surfaces. Specifically, the results are consistent with silicide growth by Si out diffusion and reaction on the stepped surface, while growth on the standard surface involves Pd in diffusion. In this case, it appears that the surface and near surface damage on the standard surfaces not only facilitates the initiation of the reaction but also helps to set the direction of reactant transport.

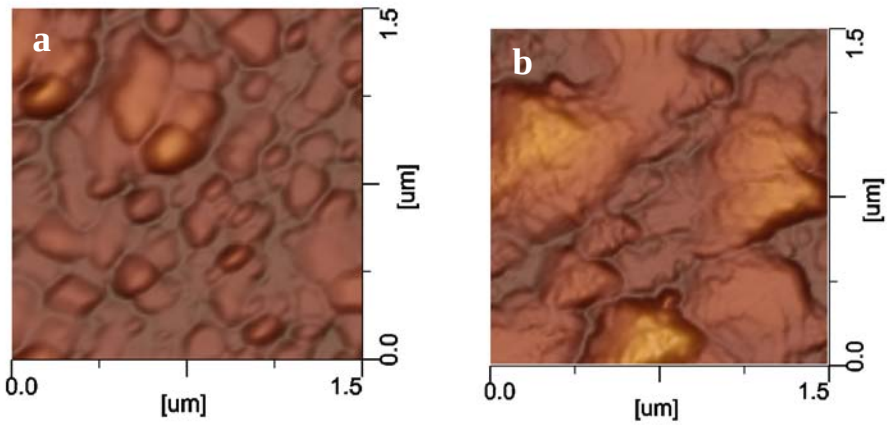

Figure 5 AFM images for a) an annealed 8.5 nm film on the standard SiC surface and b) an annealed 10.5 nm film on the stepped surface.

As mentioned previously the as deposited Pd films are conformal with the substrate surface. Annealing these films at 670 ^oC leads not only to silicide formation but also to characteristically different film morphologies that depend on the initial surface. Figure 5 shows AFM images of an annealed 8.5 nm film on the standard surface and a 10.5 nm film on the stepped surface. Here the different morphologies are evident. Hillock-like islands are formed on the standard surface (Figure 5a), while triangular crystallites are formed on the stepped surfaces (Figure 5b). AFM analyses of the thinner films reveal that the hillocks and triangular crystallites first appear as small, isolated features only after AES indicates the formation of Pd_xSi. This occurs for 0.4 nm films on the standard surface and 0.5 nm films on the stepped surface. As the initial film thickness increases, the hillocks and crystallites increase in size and extent of overlap. AFM line profiles show that the hillock-like features are columnar in structure, while the crystallites are relatively flat. For the 0.4 nm films on the stepped surface, we did not observe hillocks, crystallites, or Pd_xSi formation. This again suggests that the stepped surface is more

thermally stable than the standard surface. The observed morphologies are consistent with the transport modes discussed above.

When a 46.5 nm Pd film on the standard surface was annealed at 670 ^{o}C, a hillock-like Pd_3Si structure was once again observed consistent with the morphology shown in Figure 5a. When a 46.5 nm Pd film on the stepped surface was annealed at 670 ^{o}C, hillock-like Pd_3Si features replaced the triangular crystallites observed for the thinner films. Thus, a different growth mode may exist for the thick Pd films on the stepped surface, or there may simply not be enough thermal energy in the system to allow the thicker film to crystallize at 670 ^{o}C.

CONCLUSIONS

As deposited Pd films on both standard and stepped 6H-SiC surfaces are conformal with the initial surface morphology regardless of thickness for films ranging from 0.4 nm to 46.5 nm. There is no apparent room temperature reaction to form Pd_xSi. When these films are annealed at 670 ^{o}C, however, the resulting morphology and composition are strong functions of the initial surface morphology and film thickness.

With respect to the formation of Pd_xSi, the stepped surface appears to be more thermally stable than the standard surface. This is most likely due to enhanced reactant mobility in the damaged surface and near surface layers of the standard surface. For annealed thin Pd films (0.4 nm to 10.5 nm) on the stepped surfaces, it appears that silicide growth occurs by out diffusion of Si accompanied by the conversion Si depleted SiC layers to graphite. For the standard surface Pd in diffusion may be play a role. Again, the stage appears to be set for this by the surface and near surface damage on the standard surfaces.

The morphology of the annealed films is quite dependent on the initial surface with triangular crystallites being formed on the stepped surfaces and hillock-like clusters being formed on the standard surface. For thick 46.5 nm films, the silicide morphology is hillock-like regardless of initial surface conditions. This may simply be insufficient thermal energy to crystallize thick Pd_xSi film on stepped surface. Another difference between the stepped and standard surfaces is the presence of a graphitic overlayer on the silicide grown on the standard surface. This may again be indicative of different transport mechanism for the two surfaces.

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CHARACTERIZATION OF THE METAL-SEMICONDUCTOR INTERFACE FOR SILICON CARBIDE BASED SENSORS

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1. Introduction

Silicon carbide (SiC) is a robust, wide band gap semiconductor suitable for fabricating gas sensors.[1] The simplest sensors are Schottky diodes that change electrical characteristics when gases such as H_2, O_2, CO, NO, and hydrocarbons are adsorbed on the metal contact.[2]

Lifetime studies indicate that thermally induced compositional and structural changes at the metal-SiC interface adversely impact the performance of these sensors.[3] One factor that may contribute to the observed thermal instability is the quality of the SiC substrate surfaces on which the devices are fabricated. Vendor supplied 6H-SiC substrates contain a large number of surface and sub-surface defects associated with the polishing process as well as native defects associated with SiC growth.

High temperature hydrogen etching of SiC is known to remove surface and sub-surface polishing damage and leaves behind a periodically stepped surface.[4] In this paper, we report studies comparing the thermal stability of Pd-SiC interfaces formed on these stepped surfaces with those formed on the standard surfaces commonly used in SiC sensor device fabrication.

2. Experimental Procedure

The samples used for these studies were 1 cm x 1 cm, 6H-SiC squares cut from n-type wafers purchased from CREE Research Inc. and Sterling Semiconductor. All wafers had vendor polished (0001)-Si faces. The CREE wafers were cut 3.5^o off axis, while the Sterling samples were on axis. The nominal resistance of all the wafers was 0.03 ohm-cm.

Standard SiC surfaces were prepared by wet chemical (HF based) cleaning to remove the oxide layer. Stepped surfaces were prepared using an additional H_2 etching step. The details of preparation procedure are discussed elsewhere.[5] The pre-treated samples were mounted on a molybdenum puck and load-locked into the ultrahigh vacuum growth system. The growth system, described elsewhere [5], was equipped with an effusion cell for Pd deposition, a resistance heater, an optical pyrometer, and an Auger electron spectrometer (AES). Deposition rates for Pd were determined by weight gain.

AES peak intensities and known elemental sensitivity factors were used in a standard manner to determine the amount of each element present in the AES sampling volume.[6] In addition, the lineshape of AES transitions involving a valance band state are sensitive to the chemical bonding of the atoms in the solid. In fact, Bermudez [7] demonstrated that the stoichiometry of Pd_xSi can be determined from the lineshape of the Si-LMM AES peak.

Surface morphology was determined by *ex-situ* atomic force microscopy (AFM). As with the AES analyses, AFM was performed before and after each surface preparation step, before and after Pd deposition, and after annealing the Pd films.

3. Results and Discussion

AFM images of the standard surface reveals a random scratch pattern. These scratches may be as deep as 20 nm and as wide as 250 nm wide. These surfaces typically have overall rms values on the order of 1.5 nm. Hydrogen etching of the standard surface produces a periodically stepped surface. Depending upon the angle at which they are cut, the stepped surfaces have terraces that are 50 nm – 100 nm wide and steps heights of ~1.5 nm. Overall rms values for these surfaces are typically 1.0 nm and half that for the terraces.

After the deposition of 46 nm of Pd, AFM analyses revealed that the coatings were conformal with little if any change in the rms roughness. Given the thickness of these films and the limited AES sampling depth [6] (e.g., ~3 nm), AES analyses revealed only features associated with elemental Pd.

When the 46nm Pd films were annealed at 670^{o}C, distinctly different cluster formation modes were observed for the standard and stepped surfaces. The clusters formed on the standard surfaces were hillock-like, while the clusters formed on the stepped surfaces were columnar. The AES line shapes for the Si-LMM peaks (Figure 1) revel that for both surfaces, Si has reacted with Pd to form a Pd-rich silicide with approximately the same stoichiometry (Pd_3Si). [7] This level of reaction clearly indicates significant interdiffusion of Si and / or Pd. Moreover, both surfaces exhibit graphite-like C-KLL peaks. [8] The major differences in these spectra are in the relative intensities. The stepped surface has silicide peaks that are more than twice the intensity of those observed on standard surface, while the corresponding carbon (graphite) peak for the stepped surface is less than one half of that for the standard surface.

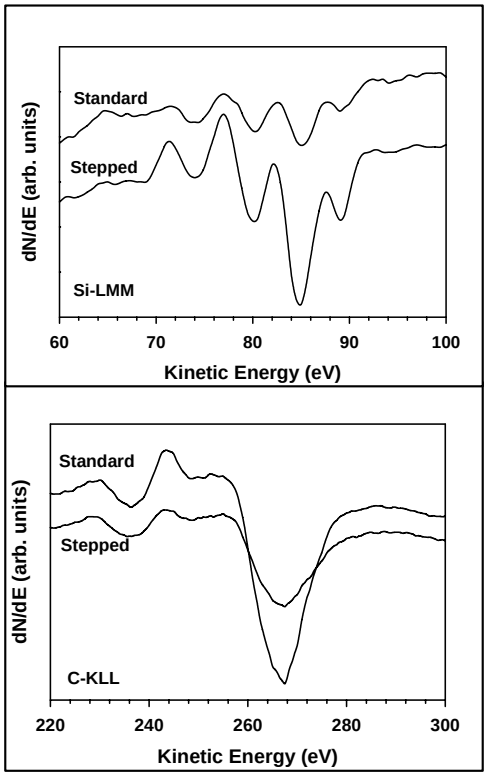

Figure 1. Si-LMM and C-KLL AES spectra for annealed 46 nm films on stepped and standard surfaces.

These AES and AFM results reflect differences in the reaction product microstructure that may be due to differences in the transport process for the two surfaces. For the standard surfaces, Pd diffuses into the substrate to react with Si leaving a graphitic overlayer with hillock-like morphology. This graphitic overlayer produces a large C-KLL peak (since it is at the surface), and it attenuates the Si-LMM peak from the underlying silicide. For the stepped surfaces, Si diffuses out to react with the Pd and produces a silicide overlayer with a columnar morphology. This leaves a C-rich (graphite-like) underlayer. The silicide overlayer produces a large Si-LMM peak (since it is at the surface), and it attenuates the C-KLL peak from the underlying graphitic layer.

To investigate the basis for the observed behaviour of the 46 nm films, a series of annealing studies was performed for very thin films (0.3 nm, 0.4 nm, 0.5, nm, 0.6 nm, and 2.4 nm). For both types of initial surface, AFM revealed that the as deposited films were conformal, and AES revealed no evidence of reaction between Pd and Si.

After annealing, AES analyses showed that silicides always form on the standard surfaces regardless of the initial film thickness. AFM analyses indicate that 0.3 nm and 0.4 nm thick films remain

conformal. For thicker films, the formation of hillock-like clusters was observed along with the reaction to form silicides and a strong graphite component. These observations are consistent with those for the annealed 46 nm films deposited on the standard surfaces.

AES analyses of annealed films deposited on the stepped surfaces reveal little, if any, reaction of Pd with Si for films of 0.3 nm and 0.4 nm. For films of this thickness, stepped surfaces appear to be more thermally stable than the standard surfaces. As with the standard surfaces, there was no change in the surface morphology. For 0.5 nm and thicker films, annealing led to the formation of silicides in the form of triangular crystallites on the terraces. These crystallites appear to be the precursors to the columnar features observed on the annealed 46 nm films.

4. Conclusions

These data illustrate the dependence of the Pd-SiC interaction (reaction and transport) on initial surface preparation. For the standard surfaces with thick (46 nm), annealed (670 ^{o}C) Pd films, the Pd appears to diffuse into the substrate to form Pd_xSi leaving a graphitic overlayer with a hillock-like morphology. For the stepped surfaces, Si diffuses out of the SiC substrate to form Pd_xSi columns on the surface leaving a graphitic underlayer. The differences in reactivity can be seen for films of several monolayers and less, while differences in morphology (i.e., transport) can be seen for films of several monolayers and greater.

5 Acknowledgments

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VII. PRESENTATIONS

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