

August 2004 • NREL/CP-520-36668

Progress in Silicon Heterojunction Devices by Hot-Wire CVD

Preprint

M.R. Page, E. Iwaniczko, Q. Wang, D.H. Levi,
Y. Yan, H.M. Branz, and T.H. Wang
National Renewable Energy Laboratory

V. Yelundur and A. Rohatgi
Georgia Institute of Technology

*To be presented at the 14th Workshop on Crystalline
Silicon Solar Cells and Modules
Winter Park, Colorado
August 8–11, 2004*



NREL

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
by Midwest Research Institute • Battelle

Contract No. DE-AC36-99-GO10337

NOTICE

The submitted manuscript has been offered by an employee of the Midwest Research Institute (MRI), a contractor of the US Government under Contract No. DE-AC36-99GO10337. Accordingly, the US Government and MRI retain a nonexclusive royalty-free license to publish or reproduce the published form of this contribution, or allow others to do so, for US Government purposes.

This report was prepared as an account of work sponsored by an agency of the United States government. Neither the United States government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States government or any agency thereof.

Available electronically at <http://www.osti.gov/bridge>

Available for a processing fee to U.S. Department of Energy
and its contractors, in paper, from:

U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831-0062
phone: 865.576.8401
fax: 865.576.5728
email: <mailto:reports@adonis.osti.gov>

Available for sale to the public, in paper, from:

U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
phone: 800.553.6847
fax: 703.605.6900
email: orders@ntis.fedworld.gov
online ordering: <http://www.ntis.gov/ordering.htm>



Progress in Silicon Heterojunction Devices by Hot-Wire CVD

M.R. Page¹, E. Iwaniczko¹, Q. Wang¹, D.H. Levi¹, Y. Yan¹, H.M. Branz¹,
V. Yelundur², A. Rohatgi², and T.H. Wang¹

¹ National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401, USA

² Georgia Institute of Technology, 777 Atlantic Dr., Atlanta, GA 30332, USA

ABSTRACT

We report on fabrication of silicon heterojunction (SHJ) solar cells based on Al-backed p-type silicon wafers, with hot-wire chemical vapor deposition (HWCVD) hydrogenated amorphous silicon (a-Si:H) emitter layers. The two-layer emitters are comprised of an extremely thin (~5-nm) intrinsic a-Si:H (a-Si:H(i)) layer topped with a slightly thicker phosphorous-doped a-Si:H layer (a-Si:H(n)). Open-circuit voltages (V_{oc}) above 620 mV are routinely achieved with a maximum of over 640 mV, indicating effective passivation of the crystalline silicon (c-Si) surface by the thin a-Si:H(i/n) stack. We used real-time spectroscopic ellipsometry (RTSE) as an in-situ diagnostic tool to monitor film thickness and roughness in real-time and to observe silicon crystallinity by further ex-situ data analysis. The deposited films were also examined by high-resolution transmission electron microscopy (HRTEM). Immediate a-Si:H deposition and a flat interface to the c-Si is the key factor in obtaining high V_{oc} . On commercial p-type B-doped Czochralski silicon (CZ-Si) wafers with a polished surface and 2.1 $\Omega\cdot\text{cm}$ resistivity, the best efficiency obtained is 14.8%. Efficiency above 15.7% is achieved on a 1.3 $\Omega\cdot\text{cm}$, p-type B-doped float-zone silicon (FZ-Si) wafer with a chemically polished front surface and a screen-printed Al-BSF.

1. INTRODUCTION

Although plasma-enhanced chemical vapor deposition (PECVD) is the dominant method for heterojunction silicon solar cell fabrication, HWCVD may have simpler reactor design and control, higher deposition rates, reduced ion bombardment of the base wafer, and atomic hydrogen (H) generation, which can be used for in-situ surface treatment and may passivate the c-Si. Furthermore, knowledge learned from the development of HWCVD heterojunction solar cells will advance our understanding of the a-Si/c-Si heterointerface.

The most important step in SHJ device development is to determine the optimum deposition condition for a-Si:H(i) and a-Si:H(n) layers to obtain immediate a-Si:H deposition with an abrupt interface to c-Si with good conformal coverage, no epitaxy, and insensitivity to c-Si substrate orientation. With RTSE and HRTEM as the in-situ and ex-situ characterization tools, it was found that, under the conditions at which a good a-Si:H film is deposited on a glass substrate, epitaxial growth on a clean c-Si substrate is usually obtained [1]. The extent of epitaxial growth is larger as substrate temperature gets higher or with a (100)-oriented wafer. Similar deposition ambiguities have also been reported by E. Centurioni [2]. Partial epitaxy is especially difficult to avoid with HWCVD. This is undesirable because it roughens the a-Si/c-Si interface and increases the interface area and may increase the total number of interface defects. Worse yet, if part of the epitaxy reaches the doped a-Si:H region, the much higher density of trap states in doped a-Si:H (compared to those in a-Si:H(i)) will provide tunneling recombination centers for photo-generated electrons and degrade the solar cell performance. The best interface passivation and solar cell performance is achieved by a clean and flat c-Si surface in contact with a-Si:H(i). To optimize a heterojunction solar cell's performance, the a-Si:H(i/n) emitter thickness must be minimized so that parasitic light absorption in the emitter is reduced. Finally, the a-Si:H(i) should be as thin as possible too

permit photogenerated holes to tunnel through to the doped a-Si:H(n) layer [3]. Here we report improved device performance after carefully tailoring growth conditions to obtain abrupt a-Si:H growth for truly heterojunction c-Si devices.

2. EXPERIMENTAL

Fig. 1 shows a schematic of our SHJ device structure. The pre-cleaned medium quality, commercial p-type B-doped CZ-Si wafers used in our device development have a polished front surface and a damage-removed back surface. We have studied a wafer resistivity range from 0.4 to 3 $\Omega\cdot\text{cm}$. These wafers are diamond scribed and cleaved into 25-cm by 50-cm substrates that fit into our HWCVD chamber. They are then subjected to a stringent cleaning procedure including degreasing in trichloroethylene, acetone, isopropyl alcohol, and methanol followed by drying with N_2 gas. This is followed by 1) an immediate 10-min soak in boiling de-ionized (DI) water (90 $\text{M}\Omega\cdot\text{cm}$), 2) a 1-min DI water cascade rinse, 3) a 1% by volume hydrofluoric acid (HF) dip for 1-min or until the c-Si surface turns hydrophobic, 4) a 1-min DI water cascade rinse, and 5) drying with N_2 gas. We then deposit 800-nm of aluminum at 2-nm/s by electron beam evaporation at room temperature on the back surface and alloy this back contact in a quartz tube furnace at 600°C for 20-min in 99.999% pure (5-N) forming gas (10% H_2 + 90% N_2). This Al-based back contact is capable of achieving 80% fill-factor and V_{oc} exceeding 640 mV. Chemically polished 1.3 $\Omega\cdot\text{cm}$ p-type B-doped FZ-Si wafers are cleaved into the same size as the CZ-Si substrates, screen-printed with Al paste and fired at a peak temperature around 750°C for a few minutes at Georgia Tech. At NREL the same top surface cleaning protocol is performed before HWCVD emitter deposition.

Deposition of the heterojunction emitter a-Si:H(i/n) stack (Fig. 1) is performed by HWCVD with a tungsten filament at $\sim 1800^\circ\text{C}$. A brief rinse of the front surface with 5-vol.% HF is employed prior to loading substrates onto the HWCVD sample platen and into the chamber load lock maintained at 1×10^{-6} Torr. NREL's System-T HWCVD chamber is equipped with optical access ports for RTSE at a 70° angle of incidence. A typical deposition consists of a brief 10-sec atomic H surface treatment at 60-mTorr with 80-sccm H_2 gas flow at 100-150°C substrate temperature, followed by 10-sec (5-nm) a-Si:H(i) deposition at 100-150°C and 20-sccm silane gas (SiH_4) flow at 10 mTorr. The 5 to 20-nm a-Si:H(n) layer is deposited using SiH_4 , phosphine (PH_3), and H_2 gases at 100-300°C substrate temperature and 2.5-sccm, 3-sccm, 50-sccm gas flows respectively. The entire deposition process is continuously monitored by RTSE for in-situ film thickness and surface roughness feedback and for post-deposition analysis of material properties [4].

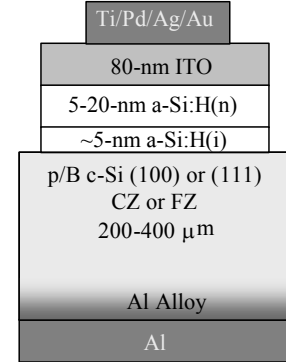


Fig. 1 Schematic of heterojunction solar cell structure.

With a completed emitter, we then deposit of 80-nm of indium-tin-oxide (ITO) as the front contact and single-layer anti-reflection coating (ARC). The ITO is deposited by thermal evaporation in an oxygen ambient at a substrate temperature of 170°C, from a 5-N purity indium-tin (90% In + 10% Sn) source in a boron nitride crucible at 900°C. This step is also believed to activate the dopants for a-Si:H(n) layers that are deposited at low temperatures (100-150°C). We then deposit the metal (50-nm Ti/60-nm Pd/2- μm Ag/50-nm Au) front grid over the surface of the ITO using a physical shadow mask with 4% grid shadow loss over the 1-cm² cell area. A photolithographically defined mesa is used to mask the grid and ITO for device isolation. The ITO is etched using 57-wt. % hydriodic acid in DI water [5] for 5 to 15-min at room temperature. The a-Si:H(i/n) heterojunction emitter is then etched using

reactive ion etching at 20W 13.5-MHz radio-frequency power for 2-min in a sulfur hexafluoride (SF_6) plasma at 130 mTorr.

Illuminated current-voltage characteristics (I-V) of a finished solar cell were measured by a calibrated XT-10 solar simulator maintained by NREL's Measurements and Characterization Division. The simulator was adjusted to approximate AM1.5 direct spectrum current using a primary c-Si reference cell certified in accordance with the world photovoltaic scale.

Internal quantum efficiency (IQE) is measured by combining global reflectance data taken on a Varian Cary 5G UV-Vis-NIR Spectrophotometer and external quantum efficiency (EQE) measured on a grating spectral response system also maintained by NREL's Measurements and Characterization Division. All light sources of the EQE system are filtered and a chopped triple grating monochromator (Acton Research Corporation, SpectraPro-300i) is used to produce the desired narrow spectral bands.

3. RESULTS AND DISCUSSIONS

3.1 AM1.5 J-V Results

Solar cell efficiencies of 15.7% and 14.8% have been achieved on high quality FZ-Si and lower quality CZ-Si respectively as shown in Fig. 2. From the I-V curves of Fig. 2 it is apparent that the V_{oc} for CZ-Si is lower, most likely due to the higher resistivity of 2.1 $\Omega\cdot\text{cm}$. This CZ-Si has a minority carrier diffusion length (L_e) of 230- μm and is slightly higher quality than the 1.0 and 0.4 $\Omega\cdot\text{cm}$ CZ-Si $L_e < 100\text{-}\mu\text{m}$ we used in earlier studies [1]. An efficiency of 15.7% has been achieved on the high quality 1.3 $\Omega\cdot\text{cm}$ p-type FZ-Si with a screen-printed Al-BSF. We believe this is the highest reported efficiency for a SHJ solar cell produced by HWCVD. On 1 $\Omega\cdot\text{cm}$ material a V_{oc} of 628 mV is the highest we have achieved by HWCVD and the highest short-circuit current (J_{sc}) we have achieved is 31.8 mA/cm^2 without employing the high efficiency features like double ARC or texturing. The fill-factor (FF) is 78.8% but reducing the series resistance of the a-Si:H(n)/ITO interface may improve the FF further.

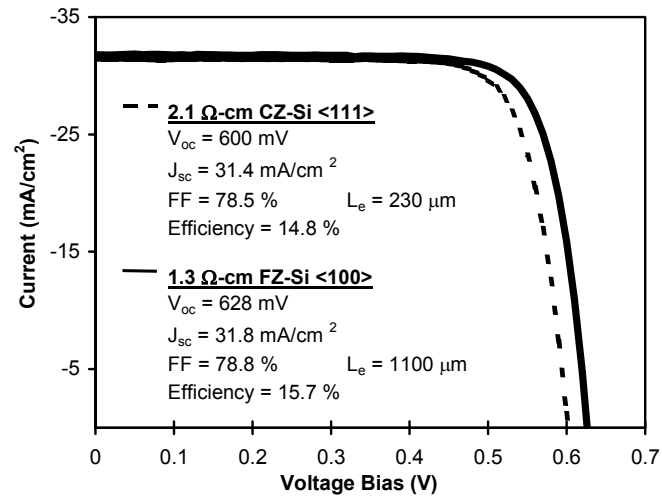


Fig. 2 AM1.5 J-V curve for high efficiency HWCVD SHJ devices on polished p-type B-doped CZ and FZ silicon.

3.2 IQE Results

FZ-Si is typically much higher quality material, which results in much higher FZ-Si cell IQE response than is obtained with the CZ-Si device (Fig. 3). The largest difference between these two devices is the L_e as calculated from the red spectral response [6]. The longer L_e for the FZ-Si material indicates that it is of much higher quality than the CZ-Si. The fact that the L_e (1100- μm) is so much longer than the FZ-Si thickness (250- μm) indicates a strong contribution from the Al-BSF. Surprisingly, the good red response of the FZ-Si device did not translate into appreciably higher current than in the CZ-Si device. From the global reflectance curves (Fig. 3) there is >5% reflectance loss even at the minimum in the FZ-Si compared to <1% loss at the minimum reflectance for the CZ-Si device. The efficiency for

the FZ-Si device would be even better had the ITO surface reflectance been as low as the CZ-Si device we suspect; more analysis of variations in ITO is necessary. Optimization of the n-layer thickness is also necessary to improve the blue response for both devices. Fig. 4 shows that the IQE response in the blue spectrum decreases as the n-layer thickness is increased from 10-nm to 30-nm due to parasitic light absorption in the n-layer. However, as the a-Si:H(n) thickness is reduced from 30-nm to 10-nm we also observed a decrease in V_{oc} as great as 10 mV due to shunting or n-layer depletion. Further optimization of a-Si:H(n) is needed.

4 Summary

We have demonstrated SHJ solar cell conversion efficiencies of 15.7% for FZ-Si and 14.8% for CZ-Si using HWCVD-deposited a-Si:H(i/n) emitter layers on polished p-type c-Si with Al-BSF. With the addition of high efficiency features like surface texturing and double ARC to improve light trapping, these efficiencies will improve significantly.

Acknowledgements

We thank Yueqin Xu, Scott Ward, Charles Teplin, and Anna Duda for their valuable technical assistance. This work is supported by U.S. DOE under Contract #DE-AC36-99G010337.

References

- [1] T.H. Wang, Q. Wang, E. Iwaniczko, M.R. Page, D.H. Levi, Y. Yan, C.W. Teplin, Y. Xu, X.Z. Wu, and H.M. Branz, 19th EUPVSECE, June 7-11, 2004, Paris, France
- [2] E. Centurioni, D. Iencinella, R. Rizzoli, C. Summonte, A. Desalvo, F. Zignani, A. Migliori, 19th EUPVSECE, June 7-11, 2004, Paris, France
- [3] T.H. Wang, M.R. Page, E. Iwaniczko, D.H. Levi, Y. Yan, H.M. Branz, V. Yelundur, A. Rohatgi, G. Bunea, A. Terao, and Q. Wang, 14th Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes, Aug. 8-11, 2004, Winter Park, Colorado, USA
- [4] D.H. Levi, C.W. Teplin, E. Iwaniczko, R.K. Ahrenkiel, H.M. Branz, Q. Wang, T.H. Wang, To be published in MRS Proceedings, Vol. 808, 2004
- [5] G. Bradshaw and A.J. Hughes, Thin Solid Films, Vol. 33(1976) L5-L7
- [6] P.A. Basore, Proceedings of the 23rd IEEE Photovoltaics Specialists Conference, May 11-14, 1993, pp. 147-157, Louisville, Kentucky, USA

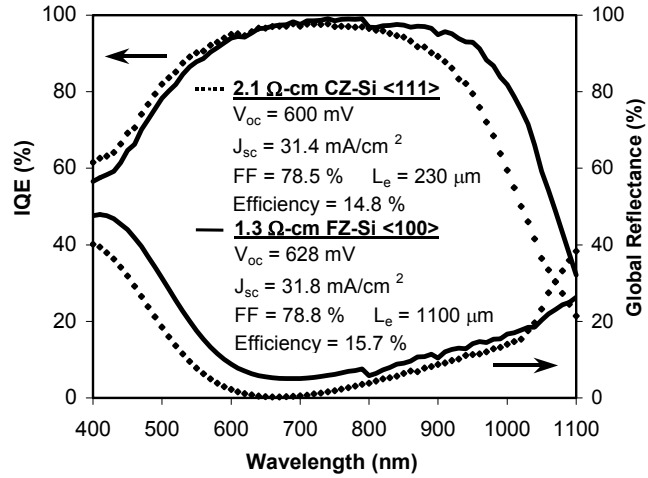


Fig. 3 IQE and global reflectance data for high efficiency p-type B-doped FZ-Si and CZ-Si devices.

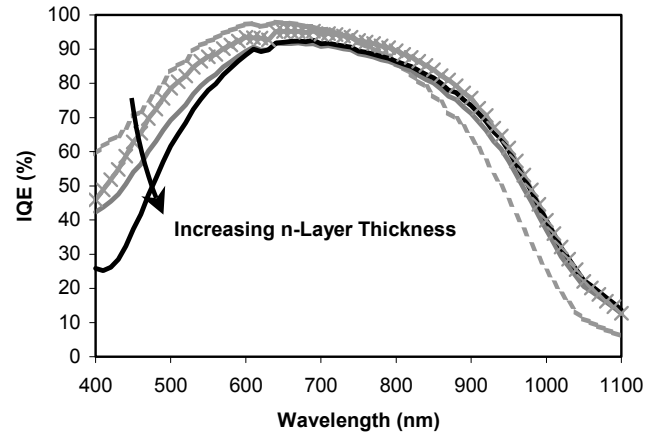


Fig. 4 Plot of IQE for SHJ devices with varying n-layer thicknesses; 10-nm, 15-nm, 20-nm, and 30-nm.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Executive Services and Communications Directorate (0704-0188). Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ORGANIZATION.

1. REPORT DATE (DD-MM-YYYY) August 2004			2. REPORT TYPE Conference Paper		3. DATES COVERED (From - To)	
4. TITLE AND SUBTITLE Progress in Silicon Heterojunction Devices by Hot-Wire CVD: Preprint				5a. CONTRACT NUMBER DE-AC36-99-GO10337		
				5b. GRANT NUMBER		
				5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S) M.R. Page, E. Iwaniczko, Q. Wang, D.H. Levi, Y. Yan, H.M. Branz, V. Yelundur, A. Rohatgi, and T.H. Wang				5d. PROJECT NUMBER NREL/CP-520-36668		
				5e. TASK NUMBER PVP4.4101		
				5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) National Renewable Energy Laboratory 1617 Cole Blvd. Golden, CO 80401-3393				8. PERFORMING ORGANIZATION REPORT NUMBER NREL/CP-520-36668		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)				10. SPONSOR/MONITOR'S ACRONYM(S) NREL		
				11. SPONSORING/MONITORING AGENCY REPORT NUMBER		
12. DISTRIBUTION AVAILABILITY STATEMENT National Technical Information Service U.S. Department of Commerce 5285 Port Royal Road Springfield, VA 22161						
13. SUPPLEMENTARY NOTES						
14. ABSTRACT (Maximum 200 Words) We report on fabrication of silicon heterojunction (SHJ) solar cells based on Al backed p type silicon wafers, with hot-wire chemical vapor deposition (HWCVD) hydrogenated amorphous silicon (a-Si:H) emitter layers. The two-layer emitters are comprised of an extremely thin (~5-nm) intrinsic a-Si:H (a-Si:H(i)) layer topped with a slightly thicker phosphorous-doped a Si:H layer (a-Si:H(n)). Open-circuit voltages (Voc) above 620 mV are routinely achieved with a maximum of over 640 mV, indicating effective passivation of the crystalline silicon (c-Si) surface by the thin a Si:H(i/n) stack. We used real-time spectroscopic ellipsometry (RTSE) as an in-situ diagnostic tool to monitor film thickness and roughness in real-time and to observe silicon crystallinity by further ex-situ data analysis. The deposited films were also examined by high-resolution transmission electron microscopy (HRTEM). Immediate a-Si:H deposition and a flat interface to the c-Si is the key factor in obtaining high Voc. On commercial p type B-doped Czochralski silicon (CZ-Si) wafers with a polished surface and 2.1 Ω·cm resistivity, the best efficiency obtained is 14.8%. Efficiency above 15.7% is achieved on a 1.3 Ω·cm, p-type B-doped float-zone silicon (FZ-Si) wafer with a chemically polished front surface and a screen-printed Al-BSF.						
15. SUBJECT TERMS PV; photovoltaics; solar cells; crystalline silicon; materials and processes; module; impurities; device process; crystal growth; defect; passivation; microelectronics						
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UL	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON	
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			19b. TELEPHONE NUMBER (Include area code)	