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The Commercial Status of the PV Industry in 2004—Identifying Important and Unimportant Factors

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The Commercial Status of the PV Industry in 2004 – Identifying Important and Unimportant Factors

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This Paper reviews the current status of the commercial PV Industry. It assesses the current status of commercially available modules, most of which use silicon wafers or ribbons. My analysis will show that the choice of Si wafers or substrates, once deemed to be the most important aspect, ended up making only negligible differences for commercial products, as long as cells are prepared by diffusion and screen printing. I will also address the prospects and requirements for both next generation thin-film modules and super-high (>20%) efficient commercial crystalline Si cells. It is shown that traditional recombination loss analyses provide a poor tool for understanding limitations of cell and module performance, because those analytical schemes ignore dominating interactions between different loss mechanisms (e.g., of surface and bulk recombination).

1. Results used for Discussion

A survey was conducted using PV module manufacturer's product specifications on their corporate websites. Table 1 gives the results of the survey as of May 2004. The ranking by efficiency was calculated as module power divided by total module area.

Eff. (%)	Module	T.coeff. (%P/°C)	comments
16.9	SunPower SPR210	na ('low')	Rear contact cells, FZ wafers
16.1	Sanyo HIP190BA2	-0.33	"HIT" heterojunction cell, n-type CZ wafers
14.2	Sharp NT-185-U1	na	CZ wafers, diffused cells
13.5	BP4170	-0.5	Laser-grooved buried contacts, CZ wafers
13.1	Kyocera KC167G	$V_{OC} = -0.12$	Cast multi-Si wafers
13.0	RWESchott ASE-300-DGF/315	-0.47	EFG ribbon
12.8	Sharp ND-167-U1	na	Cast multi-Si wafers
12.7	BP3160	-0.5	Cast multi-Si wafers ("Solarex")
12.1	Shell SQ160-C	-0.52	CZ wafers ("semisquare, CA Siemens Solar")
11.6	Evergreen Solar EC115	-0.4	"String ribbon" Si
11.5	GEPV-165M	(up to)-0.5	Reclaimed semiconductor wafers ("AstroPower")
11.1	Shell S115-C	-0.45	Cast multi-Si wafers (German cells)
11.0	WürthSolar WS31050/80	-0.36	"CIGS" thin-film
9.4	Shell Solar ST-40	-0.6	"CIGSS" thin-film
7.6	First Solar FS55	-0.25	"CdTe" thin-film
6.4	Mitsubishi Heavy MA100	-0.2	a-Si single-junction thin-film, vhf deposition
6.3	Uni-Solar US-64	(<0.3)	a-Si triple junction, rating increase to 68W (6.7%) pending

For several manufacturers, the same module is available with different power ratings. In those instances, the highest power rating was used for calculating the indicated total-area efficiencies. Also indicated are the expected power loss rates for higher than standard (25°C) operating temperatures, when provided on the module

Row	Material or Device Enhancement Measure	Commercial cell eff. (%)
1	“Conventional” Silicon Cell	14.7
2	High Lifetime Base	14.8
3	Back Surface Field (BSF)	15.6
4	Rear Local Contacts (RLC)	16.5
5	Passivated Emitter (PE)	16.8
6	Selective Emitter (SE)	17.1
7	BSF + PE	18.3
8	SE + RLC	19.7
9	High Lifetime + SE + RCL	21.2

specification sheet.

The second set of data used for my analyses comes from a presentation by R. Swanson [1], which outlines a pathway towards achieving much higher crystalline Si solar cell efficiencies. His analysis provides a detailed breakdown which device manipulations or process modifications would increase the present-day “standard” average 14.7% Si solar cell efficiency to higher numbers. Table 2 summarizes these conclusions.

2. Discussion

These 2 tables make it quite clear that for cells with diffused junctions and screen-printed contacts, “Si-quality” or lifetime has become a factor that no longer drives cell performance, even though many experimental lifetime measurements may find a correlation between measured wafer lifetimes and cell parameters. The proof of this statement also comes from the observation that today RWE-Schott can deliver 13% efficient commercial product with EFG cells, where EFG is often referred to as the lowest quality Si material (compared to CZ and cast-ingot multi-Si), while the “best” wafers (reclaimed semiconductor wafers) result in lower efficiency product for GE (‘AstroPower’). In other words, we have now been taught by commercial reality that the processing by diffusion and screen printing has become an “equalizer,” while it had been expected that Si quality (usually ranked as $Q_{FZ} > Q_{CZ} > Q_{multi} > Q_{ribbon}$) would determine the commercially achievable efficiency rates.

The data in the two tables suggests that losses (i.e., less-than-ideal performance) are not simply individual factors that arithmetically subtract from some “realistic-ideal” cell efficiency value (often taken as approximately 25% for Si cells operating at 1-sun intensity). Rather it is quite evident that the losses are quite interactive. This is directly evident from the difference between lines 8 and 9 in table 2. The rankings in Table 1 make it clear that the choice of alternative junction processes (BP Solar, Sanyo, and SunPower) has been implemented with varying degree of success. While two approaches rely on ‘traditional’ concepts of geometrical contact restriction, it is quite remarkable that a “full surface” Sanyo ‘HIT’ contacting approach employing heterojunction contacts can give very high commercial solar cell performance as well. When first reported, many of those working on wafer-Si based solar cells questioned whether it would make sense to

‘contaminate’ a perfect crystalline Si wafer with dirty amorphous silicon contact layers. Commercial reality indicates that those concerns were unwarranted. It is also interesting to realize that in the case of the HIT cell, it took 10 years from first reporting this type of device in 1992 [2] to becoming a commercial supplier with measurable product volume supplied. In 1992, Sanyo reported 1 cm² laboratory cells of 18.1% efficiency on single crystal Si and 15.5% on multicrystalline Si. As I will argue below, the difference in cell efficiency between these two types of wafers is significant and it is unlikely that better HIT-cell processes would be able to reduce such difference.

However, the commercial reality also demonstrates that alternative junction schemes are no panacea for increasing commercial efficiencies as expected. The BP ‘Saturn 5’ technology has barely outperformed the best screen printed approaches (BP Solar has now announced 16-18% cell efficiencies for ‘Saturn 7’ series cells, which may translate to module efficiencies near 15%). Taken the information from Tables 1 and 2 as guidance, there is little point in developing alternative junction processes for anything but the highest quality Si (CZ or FZ). This is borne out by the experimental efficiency differential when new contacting schemes were tried out comparing different single and multicrystalline Si wafers. There is no point for developing commercialization schemes using (inherently more expensive) geometrical or HIT contacting schemes for ribbon or multicrystalline wafer Si. Just like the full-surface diffused screen-printed cell process has acted like an ‘equalizer’ for achieving rather similar commercial cell efficiencies with different ‘quality’ Si wafers or ribbons, the high lifetime will become an equally genuine requirement for achieving >20% commercial Si cells using more sophisticated junction schemes.

Seeing the rankings in Table 1 and the factors contributing to higher efficiencies in Table 2 makes it clear that these advances were not really achieved by minimizing bulk and surface recombination losses in solar cells. Rather, cell and module efficiencies seem to be dominated by finding ways to overcome the “junction dilemma” pointed out by Swanson. In any solar cell, a high-quality semiconductor has to be contacted by a ‘dirty’ contact. Improved junction formation schemes should not only be viewed as better “passivation,” but also, perhaps predominantly, as electrical separation of the semiconductor and the contact via a semi-insulating buffer layer. I have argued before that this concept is also used in diffusion processed, screen printed crystalline Si cells [3,4]. The obvious mechanism is that of forming a compensated (low-mobility!) buffer layer when the n-type dopant is driven into the p-type base, and this mechanism makes V_{OC} so very sensitive to base doping level. A second buffer layer scheme commonly used in crystalline Si cells is the fire-through SiN_x:H coating that not only acts as passivation, but also as a buffer layer between the metal grid and the cell emitter.

Longer-term photovoltaic module technology planning strategies in the United States, Europe, and Japan seem to all be in agreement that at some point in the future, PV modules will transition from Si wafer or ribbon based technologies to true thin film technologies. The obvious benefit would be elimination of wafer or ribbon costs, which typically amounts to about 40% of PV module cost. This means that a thin-film module eliminates about 40% of module cost, if the efficiencies are equivalent. Today, as can be seen in Table 1, the efficiency of thin film modules are slightly to significantly lower than those of crystalline Si modules, but high enough for enabling thin film modules to compete for market share with silicon modules. Module performance appears to be a significant aspect of cost-competitiveness, now and in the future, not only within

crystalline Si technologies, but also for thin films. To assure competitiveness in the future, thin film PV module performance has to show as much relative efficiency progress as will be made for crystalline Si modules. Due to monolithic fabrication, there may be further manufacturing cost reductions for thin film PV modules, compared to crystalline Si that requires cell processing and string assemblies. It can also be expected that future developments will reduce the cost of the module package for both thin films and crystalline Si technologies [5]. Finally, the entire PV systems cost will change once PV is integrated into buildings, rather than being added to buildings as modules. Again, for these applications thin films possess some advantages over crystalline Si.

Thin films appear to have reached the necessary maturity to compete with crystalline Si and be available as a technology to assure further PV cost-reduction potential at the point in time when crystalline Si technology cost reductions will saturate. This can be expected to occur once Si technology becomes limited by raw materials cost, at a wafer cost of \$0.42/W_p, (a silicon feedstock price of \$30/kg and a projected 14kg/kW_p requirement), or after 2 to 4 more doublings of today's commercial output [6]. Contrary to some past beliefs, thin film PV is not 'inherently cheap' if the efficiency is too low (currently, I argue, if it is <6%). In the context of this workshop, there has always been a strong expectation that wafer (ribbon) Si PV technology would transition to thin-film Si technology. However, at present, it looks like CuInGaSe₂-cells (CIGS) and CdTe modules may outperform Si thin films by a significant enough margin to give them a competitive edge. Already today, best CIGS products and some older Si module products are of equal performance [7]. Amorphous silicon performance also remains competitive, but less so than the polycrystalline thin films. Integration into roofing systems, an approach pursued by Uni-Solar, may offset the lower efficiency potential. True thin film crystalline Si PV approaches deserve further research as well; but based on today's performance, commercialization is unlikely until better cell and module performance, and manufacturing yield, have been demonstrated [8].

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