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Electronic/Photonic Interfaces for Ultrafast Data Processing

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LDRD 129585 Final Report

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Abstract

This report summarizes a 3-month program that explored the potential areas of impact for electronic/photonic integration technologies, as applied to next-generation data processing systems operating within 100+ Gb/s optical networks. The study included a technology review that targeted three key functions of data processing systems, namely receive/demultiplexing/clock recovery, data processing, and transmit/multiplexing. Various technical approaches were described and evaluated. In addition, we initiated the development of high-speed photodetectors and hybrid integration processes, two key elements of an ultrafast data processor. Relevant experimental results are described herein.

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1. Introduction

A nation's security is strongly tied to the ability to defend its information resources. Advances in the fields of electronics and photonics have given rise to sophisticated data processing hardware that enables the security of cyber information systems. A reliance on existing technologies, while key to implementing information security, is risky as potential adversaries continue to improve their own technical competencies.

Within the next five years, fiber optic data rates are anticipated to reach 100 Gb/s per channel. As is the case now, the data processing needs of government customers will not be satisfied by an assembly of off-the-shelf components. Engineering a solution for these high-speed networks will necessitate cross-cutting expertise in electronic design, photonics and integration. In this late-start LDRD, we studied several application areas required for ultrafast data processing with the goal of determining which functions could be significantly impacted by technological advances in hybrid electronics/photonics integration. The areas investigated include data processing cores, optical receivers/demultiplexing(DEMUX)/clock recovery, and optical transmitters/multiplexing(MUX). Various technical approaches can be used to implement each function, and Section 2 of this report is a condensed review of the technology study.

After determining the areas where photonic/electronic integration has high impact potential, we began to investigate the hardware implementation of one function, namely high-speed optoelectronic optical-to-electrical (O/E) conversion using custom detector elements and hybrid integration processes. Section 3 describes the experimental progress in this area. The final section of this report summarizes our work.

2. Target Applications and Technologies

A wide variety of information processing applications could benefit from electronic/photonic integration, but here we limit the discussion to those with the following characteristics: We anticipate the need to operate on optical network data streams operating at ≥ 100 Gb/s/channel, and expect that these data streams will be separated from other network traffic by filtering out a single, high-speed wavelength division multiplexing (WDM) channel. The simple on-off keying (OOK) format is assumed, as it represents the overwhelming majority of signals today. The need for a clock recovery function is uncertain but likely, as our input data stream will have some degree of uncertainty in both frequency and phase.

Data processing at full line rates of 100 GHz will be difficult. In some cases, the clock rate of a data processing engine may not need to match the optical signaling rate; hence, the use of electrical processing cores operating at lower frequencies could provide sufficient processing power in some applications. Nonetheless, processing complexity is assumed to be high, and thousands to millions of gates may be required to implement certain data manipulation functions.

Retransmission of optical data after signal processing has occurred will require high-performance photonics hardware that can perform the high-speed transmit and MUX functions. Because the characteristics of incoming optical signals will be established by the network on which they reside, the outgoing signal integrity must be high, with similar wavelength, data format, bit rate, amplitude and optical signal-to-noise ratio (OSNR) to that of the input.

2.1. Data Processing

Although several network-level data processing functions can be performed using a small number of gates (i.e., only a handful of gates is needed for header recognition in packet-switched networks), the majority of information security applications require several orders of magnitude higher logical complexity. Logical complexity, clock rate, technology maturity and cost are likely to be the important factors in determining which technology is used for the data processing engine of the overall system.

2.1.1. All-Optical Logic

Of many all-optical logic technologies that have been investigated or proposed for use in high-speed processing applications, few can be considered suitable for this application due to fundamental flaws such as lacking scalability in complexity/speed, or high power dissipation. Far fewer still have been demonstrated at a level of maturity that justifies their consideration as a viable alternative to microelectronics in the near term (which continues to progress rapidly due to immense ongoing worldwide investments). Published results on cross-gain and cross-phase modulation in semiconductor optical amplifiers (SOAs) [1, 2] suggest that these technologies have the ability to perform ultrafast optical data processing at a limited density (and with high power dissipation), while other approaches such as symmetric self-electrooptic effect devices (S-SEEDs) [3], photodiode/electroabsorption modulator (PD/EAM) pairs [4], and nonlinear optical circuits based on chalcogenide glasses are promising [5].

Despite this ongoing work, its immaturity relative to electronics will preclude the use of all-optical processing for the next several years. Advances in the area of ultrafast photonics will nonetheless be useful, as we may be able to use semiconductor optoelectronic devices at the edge of the processing core for limited MUX, DEMUX, and other processing functions that require a small number of high-speed optical gates.

2.1.2. Electronic Integrated Circuits

Multiple electronic integrated circuit (IC) technologies exist as candidates for high-speed data processing. Silicon and silicon-on-insulator (SOI) CMOS technologies are an extremely compelling choice, offering the lowest cost and lowest power solutions for data processing. Advanced technology nodes allow dense packing of millions or billions of transistors, with >10 GHz clock speeds already demonstrated using mainstream technologies. Complex data processing at speeds of 20-30 GHz will likely be possible within the 3-5 year timeframe using state-of-the-art CMOS technologies.

Silicon-germanium (SiGe)-based BiCMOS electronics exploit both the low-power/high-density quality of silicon CMOS electronics and the high-speed characteristics of SiGe heterojunction bipolar transistors (HBTs) by combining them on a single platform. Currently-available process technologies for SiGe microelectronics have allowed the implementation of very high-speed MUX and DEMUX functions (up to 100 Gb/s) but consume relatively large amounts of power. SiGe electronics are somewhat limited by moderate-to-low gate counts, with ~100k gates being the current estimated upper maximum for single-chip designs.

InP and GaAs compound semiconductor ICs have traditionally operated with the highest clock speeds and correspondingly highest power dissipation of all electronics technologies. Pushed by both the telecommunications industry and RF analog applications (i.e., cellular telephones), compounds have the advantage of a higher operating frequency and higher output

voltage (typically required for driving optoelectronic modulators). Only low levels of integration complexity have been demonstrated, suggesting that compound semiconductor electronics are not viable for use in most data processing cores. Additionally, the steady advance of silicon technologies has enabled low-cost SiGe circuits to supplant compounds in certain applications, forcing the industry into yet narrower niche markets.

It is important to compare the anticipated direction of the electronics industry as well. It is well-established that the performance of CMOS is expected to steadily improve for another decade due to ongoing investments by the industry. On the other hand, some experts suggest that SiGe and InP/GaAs performance may have reached a plateau due to the enormous costs of new foundries and continued R&D. Thanks to the high gate counts, low power and low cost of SOI CMOS, it appears that a CMOS data processing core will be a good choice for the majority of information security applications going forward, provided parallel cores can be utilized. If clock speed is paramount, SiGe-based electronics should be leveraged to operate at full (100 GHz) optical line rates, albeit with limitations on computational complexity. Compound semiconductor electronic technologies are likely to find application in only the simplest functions, or where the higher operating frequency and/or voltage are necessary for interfacing with optoelectronic devices.

2.2. Receivers, DEMUX and Clock Recovery

The functions associated with the optical-to-electrical interface include the detect/receive process, as well as clock recovery and perhaps demultiplexing (time-based DEMUX of a single WDM channel is considered here, while WDM spectral DEMUX is assumed to use conventional optical add/drop multiplexing (OADM) components). Electronic/photonic integration likely has a large role to play at the network-to-processor edge because electronics alone cannot be used for an O/E interface and commercial off-the-shelf (COTS) photonics are limited in performance and functionality.

2.2.1. High-Speed Photodiodes

One of the simplest high-speed O/E conversion technologies is the low-capacitance p-i-n photodiode (PD). Devices with increasingly smaller areas have been demonstrated in the literature, as a reduction in size (and RC time constant) dramatically enhances bandwidth. The best recent example of this approach is work performed by a group in Germany [6] where PDs as small as $5\mu\text{m} \times 7\mu\text{m}$ were fabricated. The devices exhibit a 120 GHz 3-dB bandwidth and responsivity up to 0.5 A/W. Further increases (to 150 GHz) are expected with greater optimization of the InGaAs absorber layer thickness. Bandwidth improvements may be expected with the use of travelling-wave configurations and multimode interference structures [7]. The main challenge with this approach is efficient optical coupling into such a small device. Beling *et al.* incorporated mode-coupled waveguides under their PD structure to accomplish high coupling efficiency. Note that surface-normal photodetectors with even smaller areas and higher bandwidths should be possible where precision micro-optics are used for optical coupling.

Published results on unitraveling-carrier (UTC) PDs from NTT in Japan [8] have been very impressive. Results include 3-dB bandwidths of 310 GHz, high-power handling, and 100+ Gb/s operation in optical logic gates. The devices are based on absorption layers where the slower-traveling holes are the majority carriers and swept immediately into the contacts, eliminating the major speed bottleneck in conventional p-i-n PDs. Despite such impressive results, other research groups that have tried making UTC PDs have been unable to come close to approaching

NTT's results, which may reflect that the design, growth and/or fabrication may be particularly challenging. Nonetheless, UTC PD development may be a possible high-risk, high-reward alternative to a low-capacitance p-i-n PD development effort if signaling rates above 100 Gb/s are needed.

Various electrical receiver circuits are generally combined with high-speed photodiodes to complete the O/E conversion process. Typical designs employ a transimpedance amplifier with high gain/bandwidth product, followed by additional limiting amplifier stages that ensure rail-to-rail amplitudes and high slew rates at the output of the receiver. High-performance 40+ Gb/s receivers have been demonstrated with both state-of-the-art SiGe and InP technologies, while lower power/lower speed receivers are possible using advanced CMOS designs.

2.2.2. Electrical, All-Optical and Hybrid DEMUX

Time-division demultiplexing will be required for applications that employ parallel processing cores that operate at a subharmonic of the line rate. Taking a simple 1:4 DEMUX ratio (with a 100 Gb/s input data rate) as the target, it is possible to envision implementing this function in several different ways. All-optical DEMUX is a common approach used in high-speed optical networks, where the entire function is performed in the optical domain. Various schemes have employed optoelectronic devices and non-linear optic components. For instance, one approach uses ultrafast non-linear phase-shifts in symmetric Mach-Zehnder interferometers which are activated by input pulses in SOAs. A group from NEC, Japan [9] demonstrated DEMUX of a 168-Gb/s data pulse stream at a 10 GHz repetition rate using a hybrid-integrated device, while a German group [10] later showed similar results to 16 channels using a monolithically-integrated device on InP. EAM-PD pairs have been used to perform a similar function at high speeds [4], while four-wave mixing in SOAs and parametric amplification in periodically-poled lithium niobate (PPLN) have been demonstrated as well. All of these all-optical approaches involve a significant amount of complexity and dissipate large amounts of power, but provide the highest switching bandwidth of all DEMUX techniques.

Signal DEMUX in the electrical domain is typically performed with input signals of 10 Gb/s or lower, although recent demonstrations leveraging advanced electronics technologies have pushed to much higher performance. The current state-of-the-art is represented by a 1:2 electronic DEMUX operating at 100 Gb/s, recently demonstrated using InP HBT technology [11] with 3.8-W power consumption. Another impressive result employed SiGe technology [12]. This circuit performed a 1:2 DEMUX as well as clock recovery at 107 Gb/s, with unquoted power dissipation (but exceeding 5.5 W).

A hybrid approach to high-speed DEMUX may offer advantages by reducing power dissipation while increasing the achievable bandwidth. High-speed electrical sampling can be performed very precisely using optical triggering, and we suggest combining a high-speed photodiode with an optically-triggered electrical sampler prior to connection with the receiver circuit. The exact approach is not highlighted in this report, but is currently under investigation. Hybrid optical sampling techniques have also been employed by NTT to demonstrate a 4:1 DEMUX operating at 40 Gb/s [13].

Actively mode-locked lasers (MLLs) would be critical elements for optical sampling of the incoming optical data stream for both all-optical and hybrid DEMUX. The high-quality commercial MLLs available today can produce pulsewidths <150 fs, but are fiber-based and relatively large. Several groups have made progress in the area of chip-scale MLLs including

UCSB which recently demonstrated a hybrid III-V/Si 40-Gb/s MLL [14] with a pulsewidth of 3.7 ps. A number of other groups have demonstrated 10-GHz InP-based MLLs (i.e., see [15]).

2.2.3. Clock Recovery

Clock recovery, which is used to generate a local clock synchronized with the incoming optical signal, will be important for data sampling, DEMUX, and data processing operations. Generally clock recovery is accomplished by combining the data stream with a slower-response envelope function. High-speed optical clock recovery has been demonstrated by a Mach-Zehnder interferometer at 80 Gb/s [16], cross-absorption modulation [17] and two-photon absorption in a Si PD at 80 Gb/s [18]. The first two approaches offer the possibility of being integrated into an InP platform. As mentioned previously, all-electrical clock recovery has been demonstrated at rates up to 107 Gb/s.

2.3. Transmitters and MUX

In order to ensure the interoperability of a custom data processing element and the larger optical network with which it interfaces, the optical transmitter portion of the hardware must have uncompromised performance. The strict requirements placed on network signal integrity leave little design space in which customization can lead to significant system improvements. Hence, the optoelectronic transmitter technologies employed by a government data processing application are likely to employ commercial (or commercial-like) devices as in conventional network hardware.

Similarly, once 100 Gb/s data streams are in use on fiber networks, the MUX function used to serialize parallel data streams will already be well-developed and there exists little reason to create a custom solution here. Note that many approaches to passive all-optical MUX at ≥ 100 GHz have been commonplace for the last decade, while several all-electrical MUX circuits have been demonstrated at high speeds – MUX functions are typically demonstrated before DEMUX operations are achieved due to the simpler circuits that are employed therein.

2.4. Optochip Vision

By combining the best technologies for each function studied above, it is possible to realize an optimal approach for future high-speed data processing systems. Our vision for this system is shown in Figure 1 and termed the “optochip”. While perhaps comprised of more than one technology (and potentially more than one integrated circuit), the optochip performs all of the functions described above (receive/DEMUX/clock recovery, data processing, transmit/MUX) in a very small footprint. Hybrid integration enables the use of the best technology for each function, thereby allowing independent system optimization for low power, processing complexity, signal integrity, and overall cost.

The technology review suggests that an optimized optochip implementation combines InP-based optoelectronics (for the detect/DEMUX/clock recovery functions) with CMOS or SiGe circuits (to implement the receivers and processing core functions). The use of 1:4 optoelectronic MUX/DEMUX will enable the use of state-of-the-art CMOS technology for parallel processing cores operating at a subharmonic (i.e., 25 GHz or lower) of the 100 Gb/s input line rate. The electrical output of the processing cores will need to be amplified and conditioned by high-voltage driver circuits, likely fabricated on InP substrates. The optical transmitters themselves will be implemented in an InP-based optoelectronic technology, with the MUX function either electrical or all-optical.

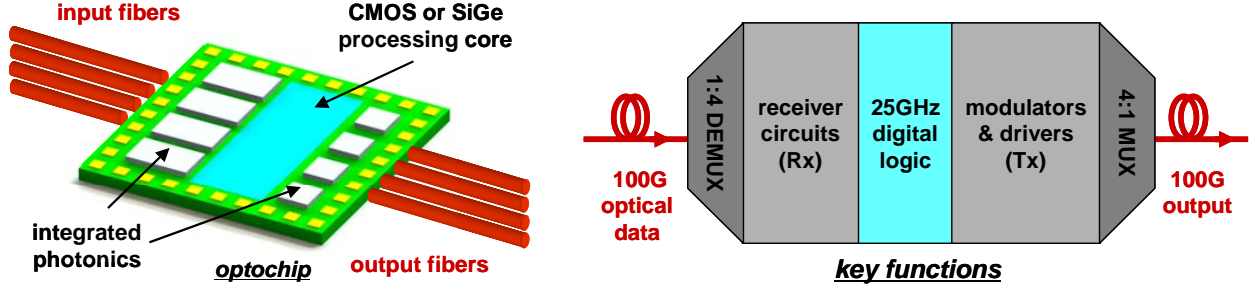


Figure 1. Optochip conceptual view and a schematic of its required functions.

3. Hardware Demonstration

In parallel with the technology study aspect of this program, we chose to experimentally investigate some key hardware elements that would be required by any electronic/photonic data processing system architecture. The technologies selected for demonstration were photodetectors and hybrid integration, both of which could be key enablers for future photonic processing engines. Below we discuss our progress in the area of high-speed photodetectors and hybrid integration for ultrafast data processing applications.

3.1. High-Speed Photodiode Design

The high-speed photodetectors developed in this program are relatively-simple p-i-n structures that utilize InAlGaAs quaternary materials and operate under surface-normal illumination. Unlike typical waveguide detectors, surface-normal devices can be formed into dense 2-D arrays and maintain compatibility with flip-chip integration to an optoelectronic processing chip. Reassuringly, during the technology review we became convinced that such photodetectors are, in fact, one of the best approaches for O/E conversion in ≥ 100 Gb/s systems. Additionally, they are compatible with high-speed optoelectronic DEMUX techniques developed during this effort.

The photodiodes designed in this work are circular, mesa-etched vertical p-i-n diodes. The active absorber of the detector consists of a multiple quantum well (MQW) intrinsic region with a thickness of one-half micron. While the MQW design was chosen to leverage ongoing programs, it was expected to have slower performance than a bulk heterostructure design due to decreased hole velocity and finite carrier escape time from the wells. The epitaxial material was grown by metallorganic chemical vapor deposition (MOCVD) on an undoped InP substrate. Figure 2 shows a schematic of the device and the epitaxial layers it employs.

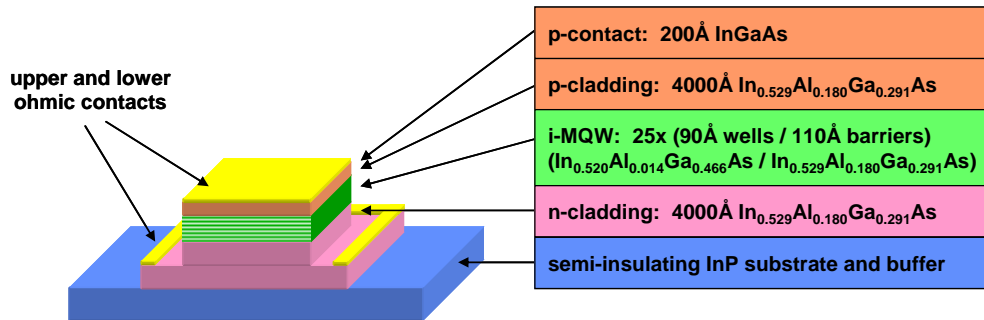


Figure 2. Photodetector schematic and its epitaxial layer structure.

Photodetector fabrication was performed with a mask set designed for top-side, high-speed modulator testing, and later with a second mask set designed for flip-chip device integration. The detector bandwidth is expected to be dominated by only a few factors: 1) the RC charging time where R is the load seen by the photodiode (typically 50 ohms during device testing but determined by the receiver circuit in practice) and C is the device/parasitic capacitance, and 2) the carrier transit time across the absorbing region. In the material used here, carrier escape from the quantum wells may also be a limiting element. In consideration of these factors, device fabrication minimizes mesa size to reduce capacitance with diodes fabricated as small as 15 microns in diameter. Additionally, the epitaxial design incorporates a moderately-thin absorber to minimize carrier sweep-out while maintaining reasonable responsivity. Figure 3 shows a photograph of fabricated diodes prior to hybrid integration. Varying mesa sizes are present to study the effects of increased capacitance on device bandwidth.

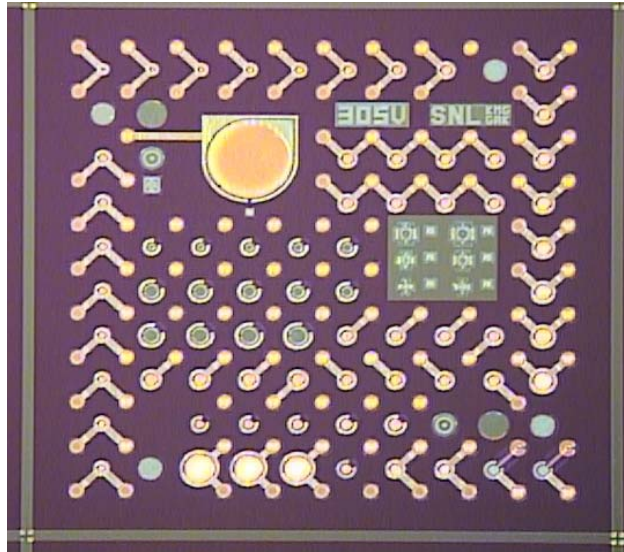


Figure 3. Photomicrograph of a fabricated photodiode array prior to integration.

3.2. Hybrid Integration

Regardless of the photonic device technologies chosen for use, dense hybrid integration will help to overcome the electrical parasitics that limit commercial O/E receiver modules. Added benefits include miniaturization, reconfigurability, and enhanced functionality (i.e., optoelectronic demultiplexing).

In parallel with concurrent integration efforts of other programs, this LDRD helped to develop a heterogeneous photonic integration approach that uses indium flip-chip bonding, thereby leveraging concepts developed by the focal plane array industry. Extremely small bonding pads enable electronics/photronics hybridization while introducing minimal electrical parasitics. We developed our flip-chip techniques using custom, low-cost electrical substrates (rather than custom CMOS chips), but processed and bonded actual photodiode devices to verify that good performance was achieved. Figure 4 shows the photodiode die from Figure 3 following its integration with an electrical substrate.

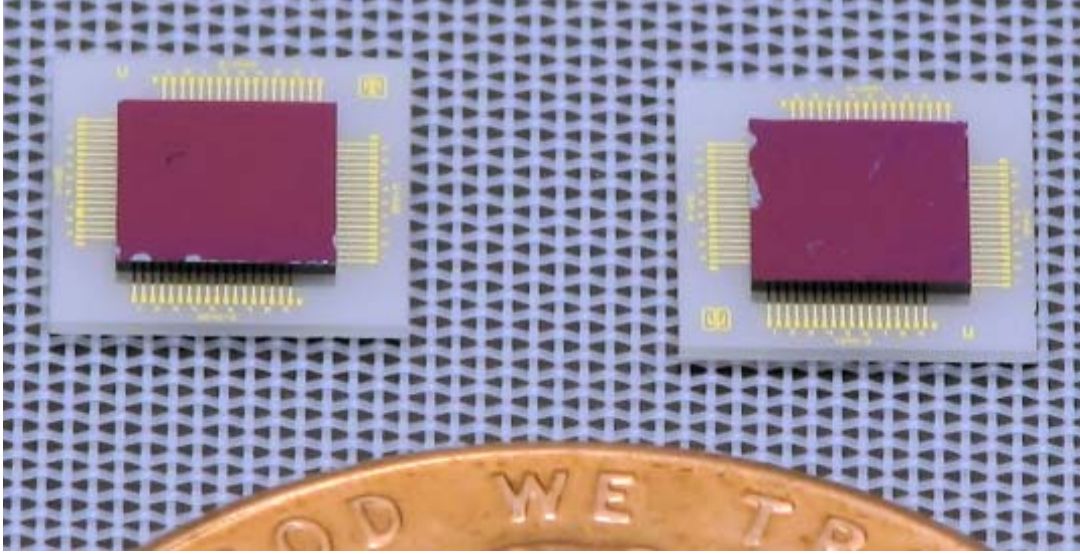


Figure 4. Photodiode arrays on electrical substrates following hybrid integration.

3.3. Experimental Characterization

High-speed photodetectors were characterized experimentally both on-wafer and following flip-chip integration. Detector bandwidths were anticipated to exceed 20 GHz, sufficient for use in preliminary high-speed system work. Testing was performed using the custom RF optoelectronic probing station illustrated in Figure 5. Photodiode bandwidth characterization was performed by illuminating the devices with the focused output of a passively modelocked fiber laser whose pulsewidth is approximately 1 ps. The devices were probed with a 40-GHz electrical RF probe and reverse-biased through a high-speed bias tee. The impulse response of the photodiode was recorded using a 50-GHz electrical sampling oscilloscope.

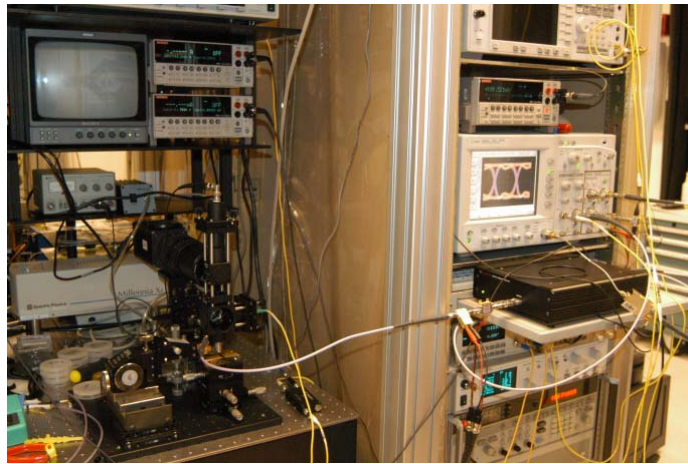


Figure 5. High-speed optoelectronic characterization setup.

Representative electrical data from a 15-micron aperture photodetector is shown in Figure 6. The 10% – 90% risetime is 13.7 ps and the pulsewidth is 17.8 ps. Given this data, one can estimate the 3-dB frequency response of the detector in different ways: First, we consider that the bandwidth of the electrical measurement setup is instrument-limited to no better than

40 GHz, which corresponds to a maximum achievable risetime of 8.8 ps. The measured signal risetime goes as the sum of the squares of the device and instrument risetimes, suggesting a corrected device response of 10.6 ps. This corresponds to a 3-dB bandwidth of 33 GHz.

RC charging is likely not setting this bandwidth limit, because the device capacitance is only 35 fF (which makes RC ~ 2 ps). It is likely that simple electron and hole transit times are determining the response time of the photodetector. Carrier saturation velocities in this material are expected to be approximately $v_{\text{sat,e}} = 0.7 \times 10^7$ cm/s and $v_{\text{sat,h}} = 0.5 \times 10^7$ cm/s [19]. For a 0.5-micron intrinsic layer thickness, these velocities correspond to a response time of ~ 10 ps. Slow carrier escape from the wells would account for the slight tail seen in the impulse response curve.

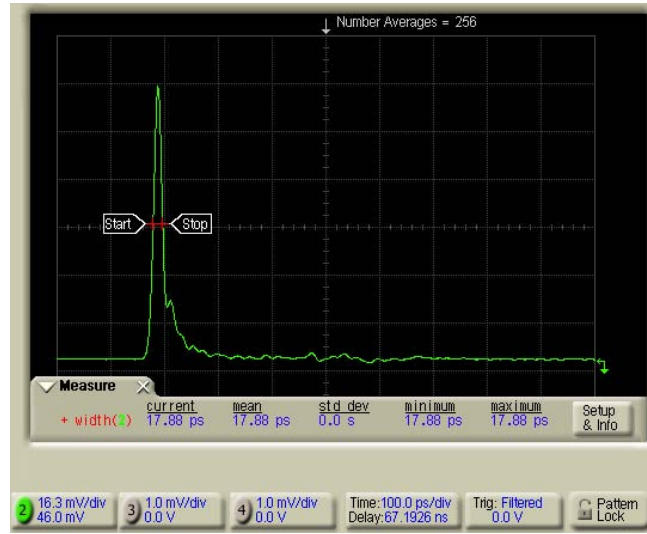


Figure 6. Impulse response of a 15-micron photodiode biased at 6V.

Alternatively, one can calculate the frequency response of a detector by taking the Fourier transform of the diode's impulse response. Figure 7 shows the calculated response as a function of frequency, both for the raw data in Figure 6 and after correction where the 40-GHz system response is removed. From this calculation we see a 3-dB bandwidth of only 16 GHz, largely due to the slow tail seen at the trailing end of the impulse peak. Encouragingly, this tail is rather small and has a correspondingly small effect on the overall frequency response: it creates an initial drop in response at frequencies below 10 GHz, after which the response is relatively flat again. The photodiode's 6-dB bandwidth is >40 GHz, suggesting that simply removing the quantum wells (and the long tail) should dramatically improve PD performance.

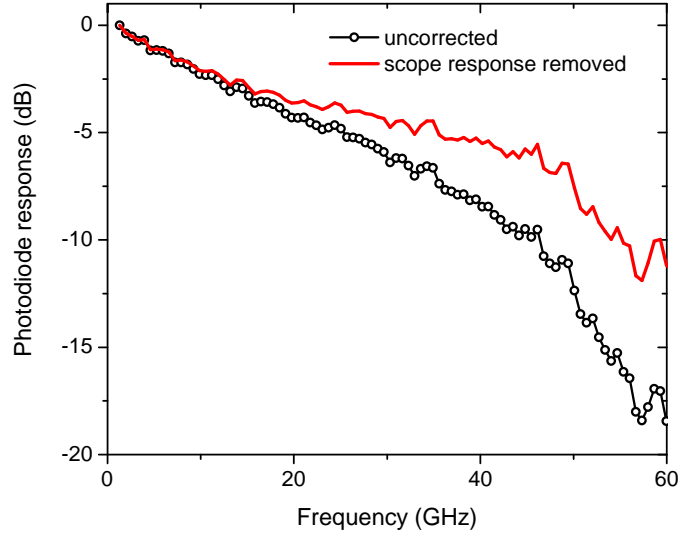


Figure 7. Calculated frequency response of the photodiode.

4. Summary

The goal of this late-start LDRD program was to develop an understanding of the areas in which electronic/photonic integration can impact the creation of next-generation data processing systems designed for operation with 100+ Gb/s networks. We performed a technology review that targeted three key functions, namely receive/DEMUX/clock recovery, data processing, and transmit/MUX. Advanced photonics, and hybrid electronic/photonic solutions appear to have the highest impact potential at the front end of the system, with possibilities in the functions of high-speed detect/receive, clock recovery, DEMUX, and small-scale data processing.

The combination of custom optoelectronic devices and state-of-the-art Si CMOS (or SiGe electronics) would enable the creation of an ultrafast data processing chip, or “optochip”, that achieves optical I/O at the chip level. Leveraging mature silicon CMOS electronics will enable high levels of logical complexity for the processing core function while minimizing cost and power dissipation. Optical transmission is likely to continue needing COTS-like optoelectronic technologies, perhaps in concert with compound semiconductor driver ICs.

In addition to the paper study element of this program, we initiated the development of high-speed photodetectors and hybrid integration processes. Due to the short scope of our effort, the photodiodes were simple p-i-n structures whose performance was limited by the MQW absorber region they contained. Nonetheless, respectable high-speed performance was obtained along with an understanding of how to improve future devices. Hybrid integration of the detectors was performed using actual photonic devices and low-cost electrical substrates. Follow-on work should investigate the challenges and opportunities provided by integration of custom photonics and actual integrated circuits.

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