DISTRIBUTED SCALABLE MODEL FOR CMOS FET POWER AMPLIFIER

BY

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THESIS

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Abstract

Integrated circuits are very popular for understandable reasons. A circuit implemented within an IC is more cost effective and reliable. A vast majority of ICs are created using silicon because it is cheap and the technology is mature. Unfortunately, communications power amplifiers have been scarce, due to the electrical advantages provided by III-V semiconductors.

In order to reach similar power levels, power amplifiers implemented on silicon require larger transistors. It is common practice to create such transistors using multiple smaller transistors connected in parallel. As the frequency of operation increases, the connections between the smaller transistors affect the overall system's behavior. Current industry standard models do not accurately compensate for these connections. This work discusses the development and results for a high-multiplicity MOS FET power amplifier model using layout transmission line considerations.

Acknowledgments

I would like to thank my adviser, Milton Feng, for sharing his wisdom. He showed me the practical side of engineering, and helped bridge the gap between the academic classroom knowledge and the practical information to make integrated circuits function. He also helped improve my professional communication. Having great ideas is of little use if they cannot be shared and used. His guidance and aid made this work possible.

Dr. Giang Nguyen, Dr. Doris Chan, Eric Iverson, Mark Stuenkel, and Huiming Xu should also be thanked for their support and instruction. Their day-to-day assistance was a great boon in making this work come to be. They helped keep me on track, and helped keep the work interesting.

Finally, I would like to thank my family: my mom Katsumia, my dad Mark, Cindy and Wayne. Their love and guidance have helped make me the man I am today.

Contents

1. Introduction

This work covers the development and implementation of a high frequency model for large gate width, high multiplicity silicon NMOS devices for use in power amplification applications. The vast majority of the current semiconductor circuitry is based on silicon technology. There are compelling economic reasons for this, as silicon is abundant and is a mature technology. However, in high speed power amplifiers, silicon is largely absent, due to advantages provided by III-V semiconductors. Accurate large-width models would aid designers by giving them the capacity to successfully design and implement high frequency silicon NMOS power amplifiers. This can lead to greater system integration, which will help lower manufacturing costs.

To reach large gate width, a common method used is to increase multiplicity. That is, take multiple, smaller transistors and connect them in parallel. Thus, the overall gate width would appear to be the sum of all the component unit cells. For instance, to reach a 2 mm total width, ten unit cells with width 200 μm each can be connected together [1]. However, when wavelengths approach the millimeter regime, layout considerations of interconnects between the unit cells cannot be ignored. Accurate modeling of these interconnects dramatically improves model accuracy.

Theory related to understanding layout effects will be discussed in Chapter 2, and then some problems with the common model will be described in Chapter 3. Chapter 4 will focus on the model presented in this work and comparison with experimental data. Conclusions will be drawn in Chapter 5.

2. Power Cell Modeling

2.1 Scattering Parameters (S Parameters)

For high frequency applications, direct measurement of currents and voltages can be difficult to accurately measure. However, accurate RF wave measurement is practical and accurate. Thus, to describe a two-port network, the wave amplitudes traveling at each port can be described. V_n^+ is the amplitude of the voltage wave incident on port n, and V_n^- is the amplitude of the voltage wave exiting port n. Using this definition, the S parameters for a system are defined as follows:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} * \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}$$

Thus, $S_{ij} = V_i^- / V_j^+$. The application of S parameters allows for detailed analysis of RF circuits. S_{11} represents the reflection at Port 1, if Port 2 is in a matching condition, terminated with a 50 Ω load. Similarly, S_{22} is the reflection at Port 2. Minimizing these values using matching networks allows an engineer to ensure that RF power can enter and exit the network easily, increasing the system's efficiency [2]. In an amplifier, S_{21} represents the system's gain, while S_{12} shows an amplifier's isolation. From these measurements, important design considerations, such as stability, return loss, matching and maximum power transfer conditions can be calculated.

2.2 Ft, FMax Calculations

Two common metrics for determining RF transistor performance are Ft, or maximum frequency for current gain, and FMax, or maximum frequency for power gain.

For FET designs, FMax is a cutoff for the highest oscillation frequency the device can support, and the maximum useable frequency for the device in an amplification circuit [3].

To calculate Ft, H parameters, or hybrid parameters, are used. These have a similar structure to impedance or admittance parameters, as the H parameters form a matrix relating the currents and voltages at each port in a two port network. The H parameter matrix is as follows:

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_1 \end{bmatrix}$$

Standard transformations are used to convert measured S parameters into H parameters . By definition, $H_{21} = I_2/I_1|V_2$. Therefore, the frequency at which H_{21} equals 1 is Ft.

To calculate FMax, Manson's unilateral power gain, or U, is calculated. U is a standard figure of merit in comparing active devices. U is calculated from admittance, or Y, parameters. Thus, standard conversions from measured S parameters to Y parameters are necessary. The calculation of U is as follows:

$$U = \frac{\left|Y_{21} - Y_{12}\right|^2}{4 * (RE[Y_{11}] * RE[Y_{22}] - RE[Y_{21}] * RE[Y_{12}])}$$

Unfortunately, in many cases Ft and FMax are higher than the maximum measurement frequency. Thus, in order to characterize Ft and FMax, extrapolation is necessary. At higher frequencies, Ft and FMax fall off at a rate of -20 dB/decade [4]. Therefore, to extrapolate the actual values for Ft and FMax, the cross-over point can be calculated assuming that the extrapolation point is within the fall-off region. Graphically checking H21 and U21 can confirm that the extrapolation point is correctly placed.

2.3 Transmission Line Model

When the electrical length of a transmission line is moderately short relative to the wavelength of the signal that is propagating through it, it is reasonable to use a lumped element model. A common model is shown in Figure 2.1.

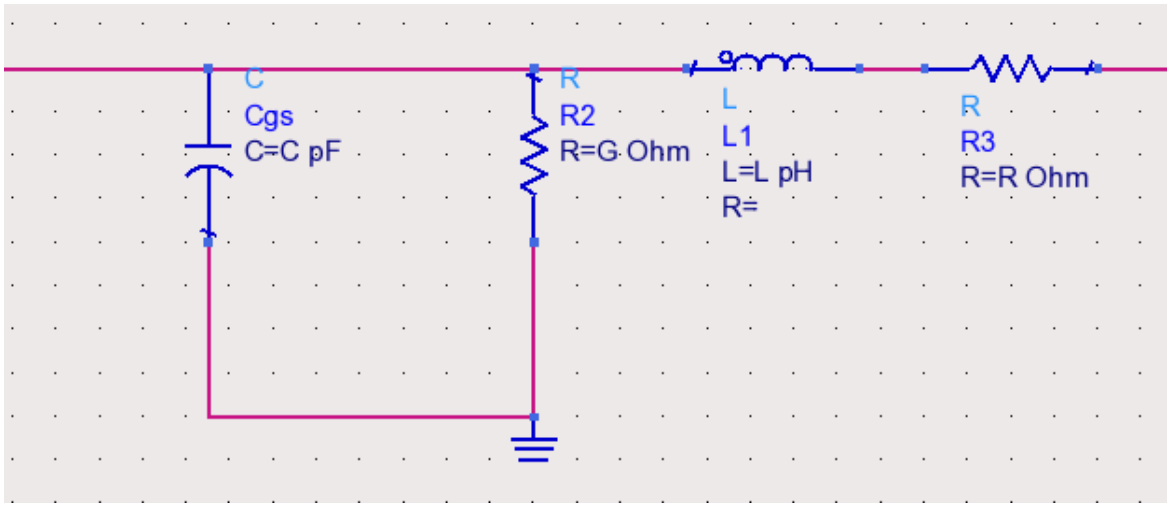

Figure 2.1: Transmission Line Model

Applying Kirchhoff's voltage and current laws, the following phasor based equations can be drawn:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z)$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z)$$

Solving the above equations simultaneously yields:

$$\frac{d^2V(z)}{dz^2} - \gamma^2 * V(z) = 0$$

$$\frac{d^2I(z)}{dz^2} - \gamma^2 * I(z) = 0$$

Here, γ is the complex propagation constant,

$$\gamma = \alpha + j * \beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

where α represents the loss component of the transmission line and β represents the phase change within the transmission line [5]. These are all frequency-dependent variables and rely on a time-dependent signal. This model is used within this work to predict layout effects within the power cell.

3. BSIM Model and Measured Data

When power cell multiplicity increases, industry standard models do not properly account for the additional effects imposed by the structure of the power cell. To demonstrate this, DC and S-parameter data were taken on large gate width NMOS power cells manufactured by UMC Semiconductors. The power cells measured were as follows: gate length = 130 nm, finger width = 7.2 μm, number of fingers = 16, and M (multiplicity) = 8 and 16. The last three measurements are abbreviated 7.2x16x8 and 7.2x16x16, indicating an overall gate width of 921.3 μm and 1843.2 μm, respectively. For comparison, another power cell with width 921.3 μm was measured. This cell was created using a 3.6x16x16 layout. Figure 3.1 shows the layout for a single 7p2x16x1 unit cell. The drains, gates, and sources are marked using D, G, and S, respectively.

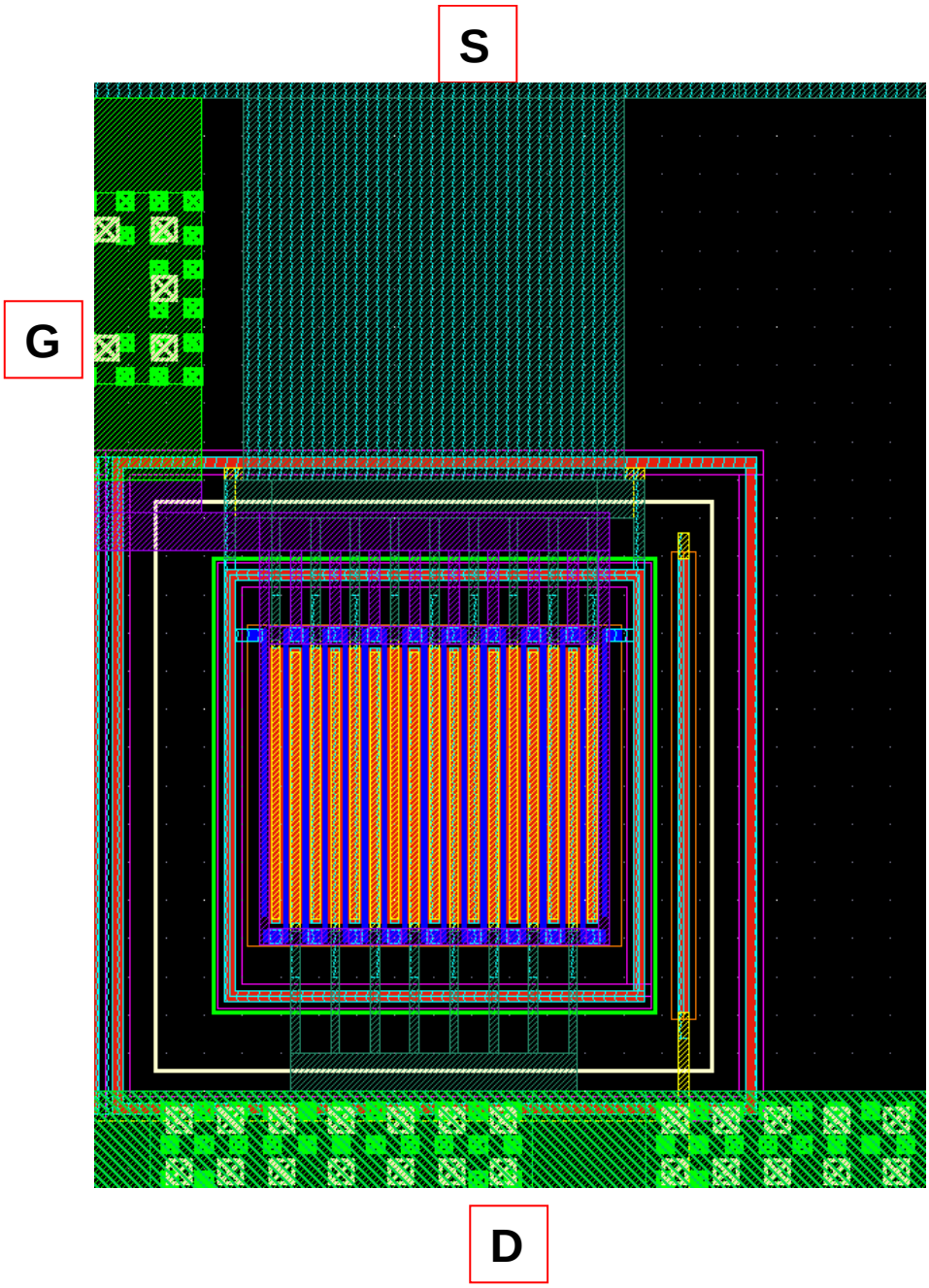

Figure 3.1: NMOS Unit Cell

The foundry-provided design includes the substrate and metal layers within the outermost red N-well rectangle in Figure 3.1. Figure 3.2 shows the overall layout for a 7p2x16x16 cell, in which the terminals of the unit cells are connected using metal layers.

Multiple metal layers were connected with vias for the source and drain terminals in order to handle the greater current density.

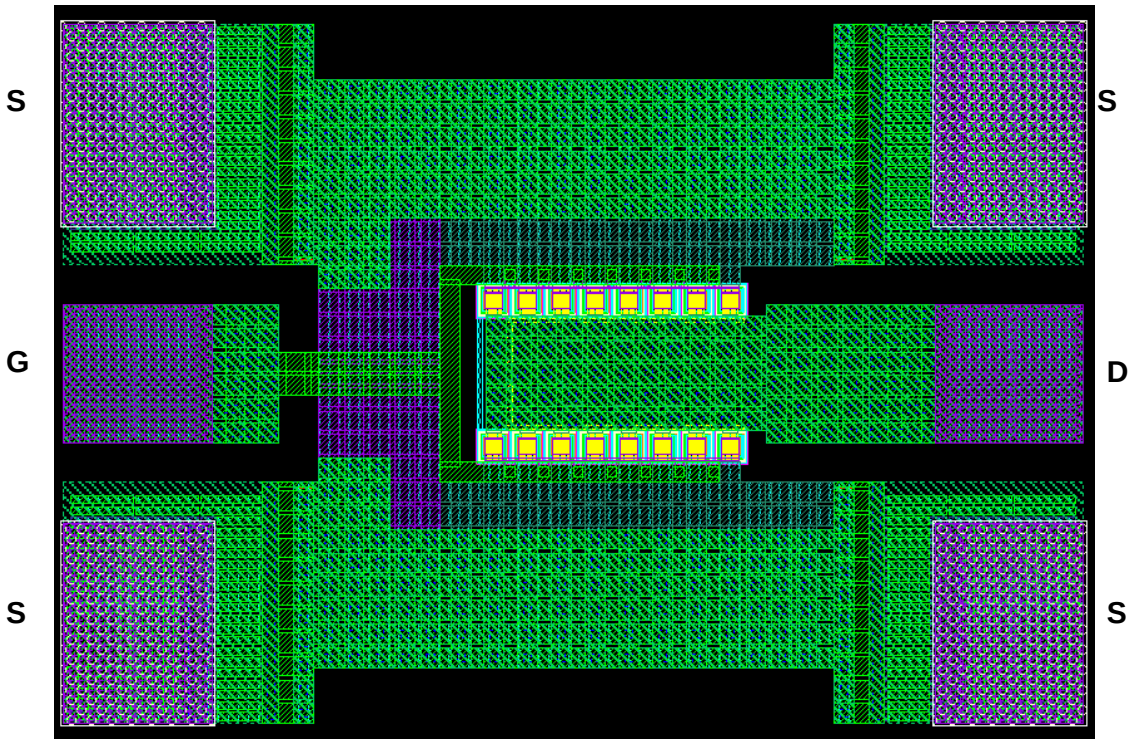

Figure 3.2: 2x8 NMOS Power Cell

Measurements of the previously described NMOS power cells were taken using an Agilent E8364A PNA for RF data and an Agilent 4142B SMU for DC data. These machines were connected to the circuit via SMA and tri-axial DC cables, respectively, connected with Agilent 11612B Bias-T's. The probes used were Cascade Microsystems ground-signal-ground coplanar microprobes. Figure 3.3 shows the measurement system configuration. Port 1 was taken to be the left-hand gate terminal, and Port 2 was the right-hand drain terminal. DC family curve, Gm, and S parameters were measured for the power cells and the individual unit cell devices.

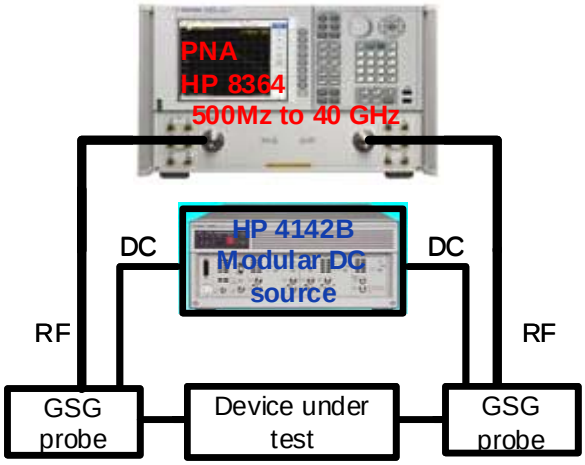

Figure 3.3: Measurement System

Figure 3.4 shows the family curves for the 115.2 unit cells, with multiplicities ranging from 1 to 16. As the multiplicity increases, the current density for a given voltage level decreases by up to 18 percent. In addition, Vd,sat increases from 0.3 V to 0.6 V. As the multiplicity increases, the parasitic resistances begin to adjust the power cell's operational parameters.

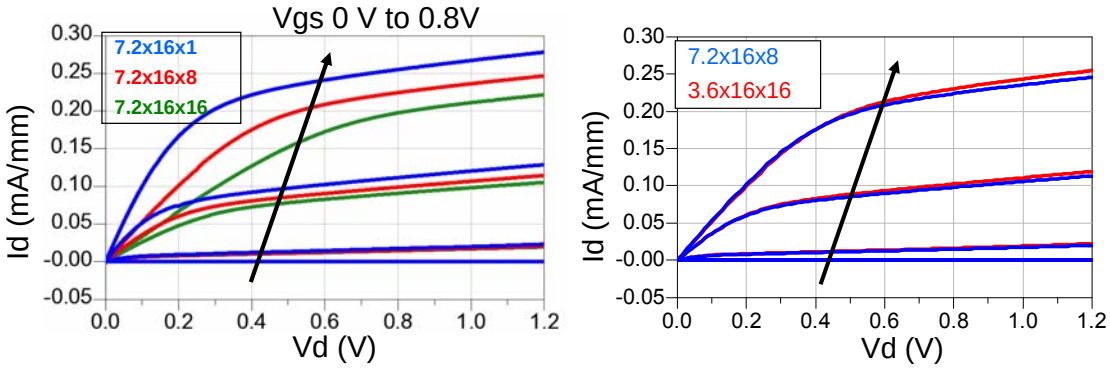

Figure 3.4: 7.2x16 Power Cell Family Curves

The family curves for the two measured power cells with equivalent gate width, the 3.6x16x16 cell and the 7.2x16x8 cell, are similar, indicating that the increase in total gate width is the primary contributor to the current density decrease.

However, the S-parameter data showed more varied results based on multiplicity. Comparisons of each power cell's Ft (unity current transfer frequency) and Fmax (maximum frequency of oscillation) are shown in Figure 3.5, with Ft and Fmax plotted versus the logarithmic drain current density.

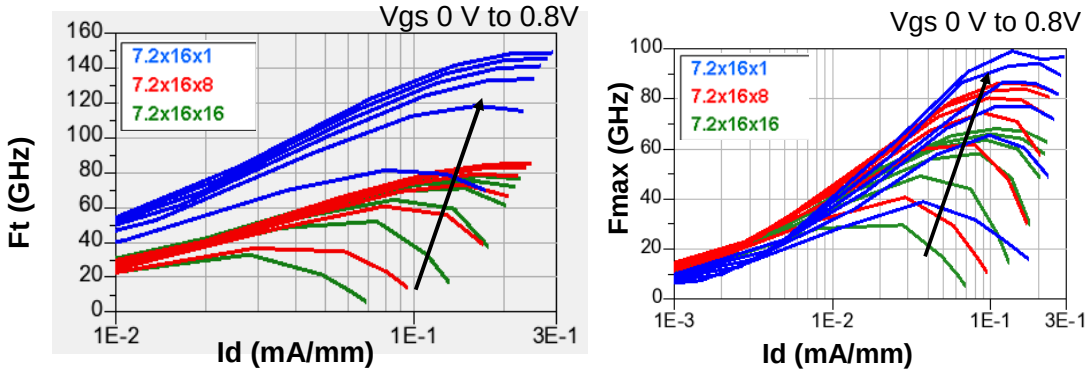

Figure 3.5: 7.2x16 Power Cell Ft, FMax Measurement

The values for Ft and Fmax fall off significantly as the multiplicity increases. Ft loses 40 GHz between the unit cell and the 16 multiplicity cell, and Fmax loses 35 GHz over the same range. This is a similar effect to that seen in the family curves. However, unlike the drain current density, additional unit cells decrease RF performance, even with equivalent total gate width, shown in Figure 3.6. While Ft was similar in both power cells, the Fmax of the 7.2x16x8 cell was 15% lower than that of the 3.6x16x16 cell. This indicates that the additional layout parasitic effects have a significant impact on power cell design.

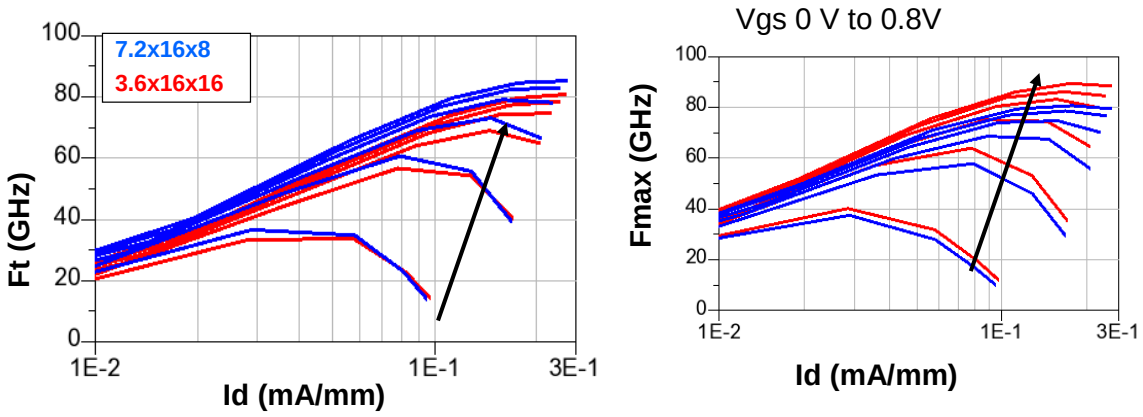

Figure 3.6: Equivalent Width Ft, FMax Measurement

A primary industry standard model for RF design is the RF-BSIM3 model. This model is regularly adjusted for each foundry and supplied as part of the design kit with a license. However, this model is optimized for small cell sizes. Figure 3.7 shows the Id data for both BSIM3 and experimental data. The 115.2x16 data shows the greatest discrepancy, with the BSIM model indicating 270.5 mA/mm Id, while the measured data is 221.5 mA/mm. The overall family curves are shifted to the left, indicating that the model is overestimating the drain voltage seen by the active components.

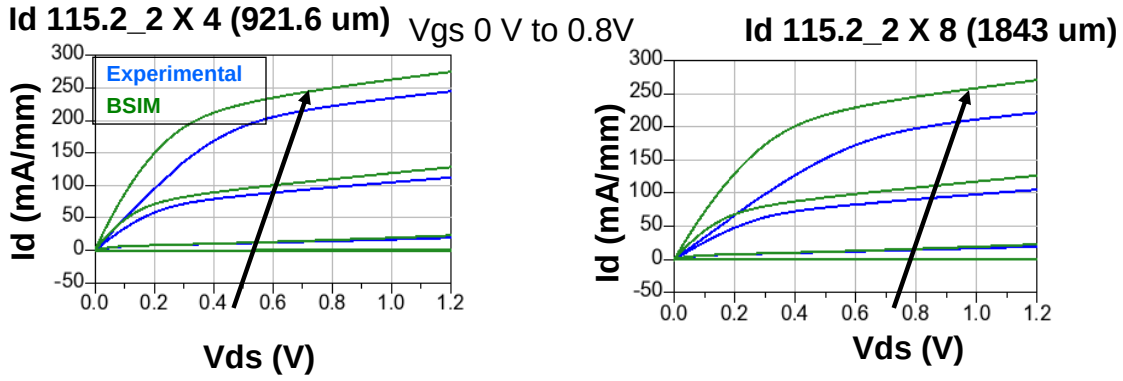

Figure 3.7: Experimental vs. BSIM Id Measurement

Similar effects can be seen with RF data. Figures 3.8 and 3.9 show the Ft and Fmax data for 115.2x16 and 115.2x8 power cells, respectively.

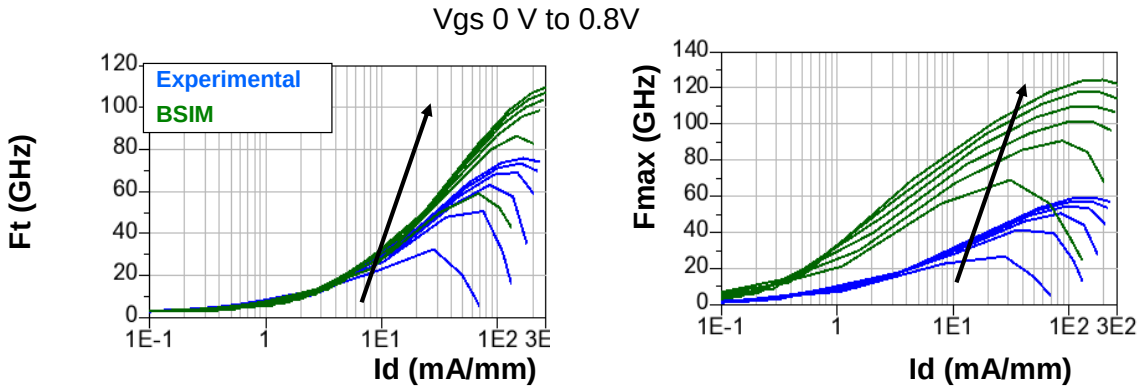

Figure 3.8: Ft and Fmax 7.2x16x16, Measurement vs. BSIM

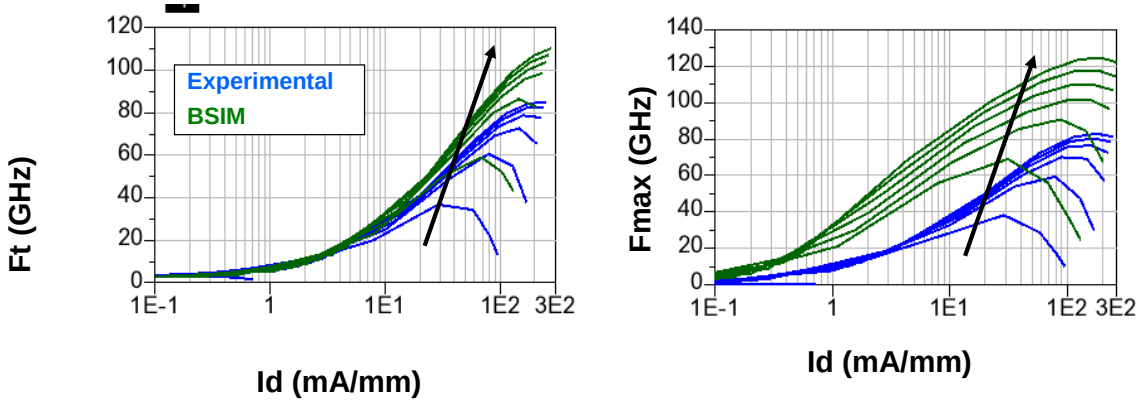

Figure 3.9: Ft and Fmax 7.2x16x8, Measurement vs. BSIM

The BSIM3 model overestimates the Ft for the larger cell by 38 GHz and 27.5 GHz for the smaller cell. While the RF-BSIM3 model is an industry standard, these significant estimation errors indicate that an updated model must be created to account for the layout effects induced by large power cells for RF design.

4. Power Cell Model

4.1 Model Overview

The Power Cell model was created as an expansion of the foundry-provided RF-BSIM3 model for high multiplicity power cells. Layout interconnections are modeled between unit cells and device-level parasitic effects are taken into consideration to create a scalable model that accurately predicts high frequency effects. Figure 4.1 shows a graphic of the 115.2x16 power cell with the model components for the gate terminal overlaid.

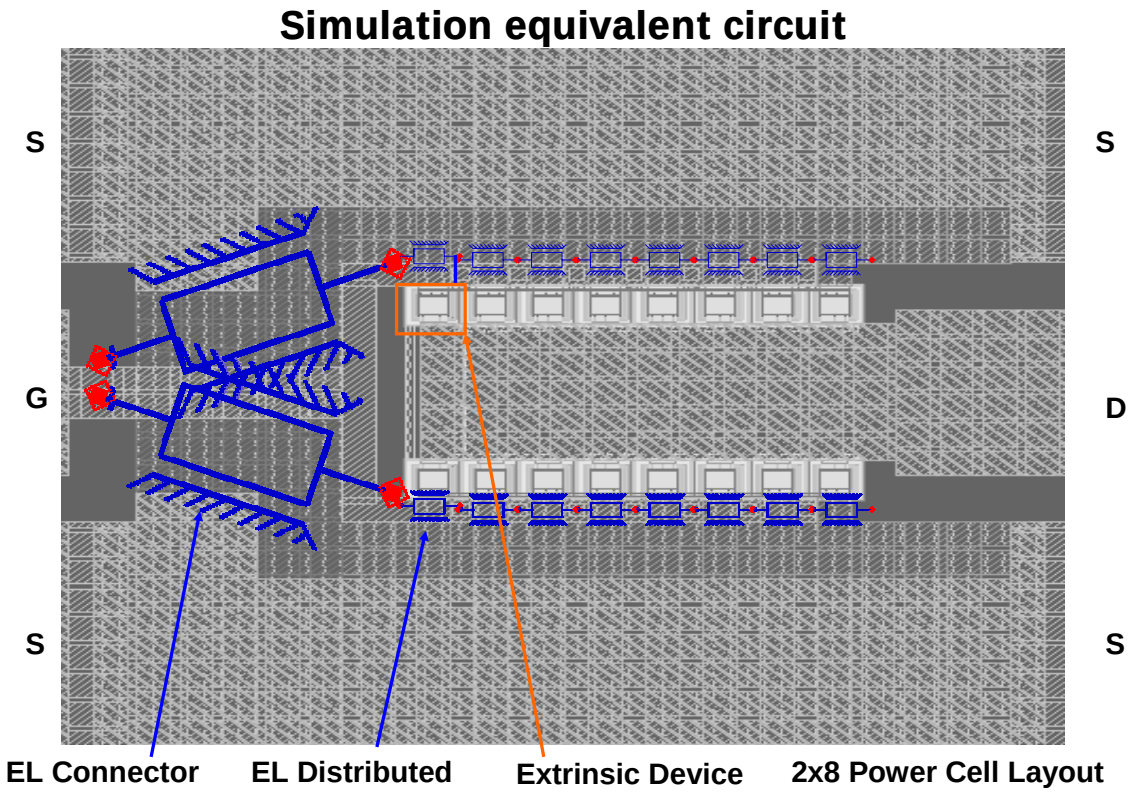

Figure 4.1: Simulation Equivalent Circuit

The model is divided into three types of elements: connector blocks, distributed blocks, and extrinsic device blocks. Connector blocks contain parasitic effects relating to the transmission lines leading to the first transistor in the cell. The distributed blocks model effects between transistors and these are added to scale the model. Extrinsic device blocks model inaccuracies independent of the size of the power cell. More details about these blocks and their behavior are described in the following section.

4.2 Model Blocks

The Power Cell model uses three types of modeling blocks to capture high frequency behavior: connector blocks, distributed blocks, and extrinsic device blocks. Figure 4.2 shows the circuit diagram of a connection block. Each terminal is modeled individually as a lossy transmission line. The conductance term is isolated by a DC_Block component to ensure that these terms to not affect DC bias behavior. The resistive loss is indicated within the inductor component.

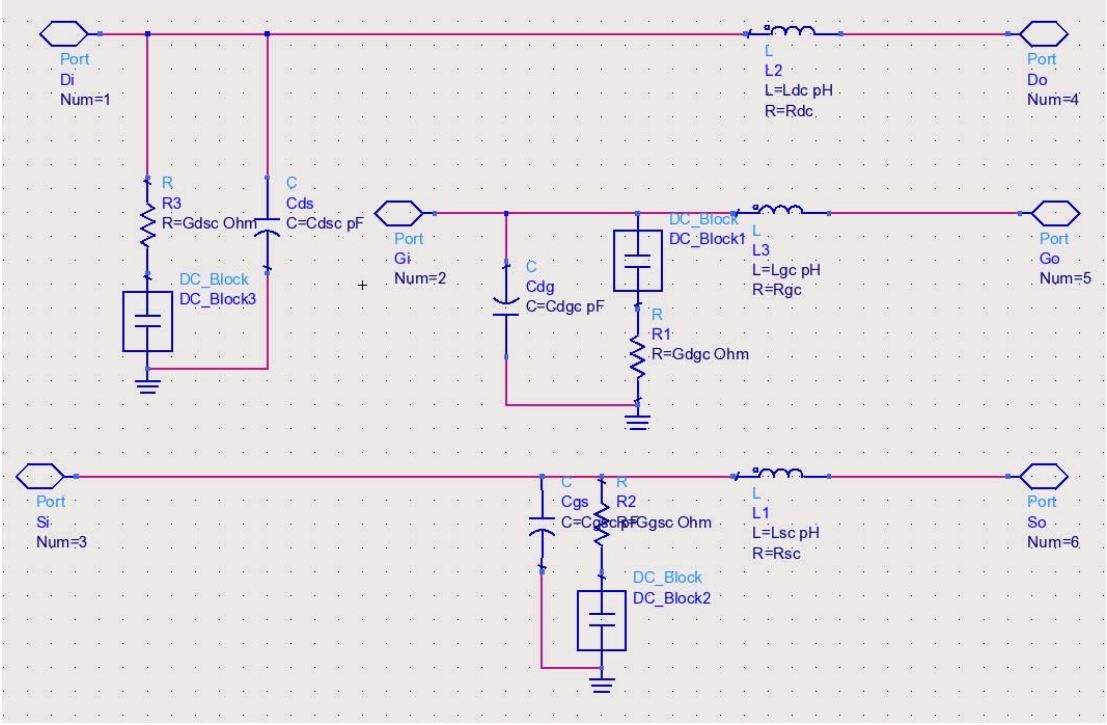

Figure 4.2: Connection Block Circuit

Figure 4.3 shows the distributed block. Again, the transmission lines that connect the transistor terminals are modeled as lossy transmission lines. However, the distributed block contains the device block within it. Thus, connecting additional distributed blocks in series facilitates scaling within the model.

Figure 4.4 shows the device block. The center of the block has a foundry-provided RF-BSIM3 model configured to model a single unit cell. It is connected in a common source configuration, which is consistent with the measured circuit [6]. The parasitic effects surrounding the BSIM3 model correct inaccuracies induced by the metal layers connecting the device to the transmission lines. The topology has been previously utilized successfully to improve model performance [7].

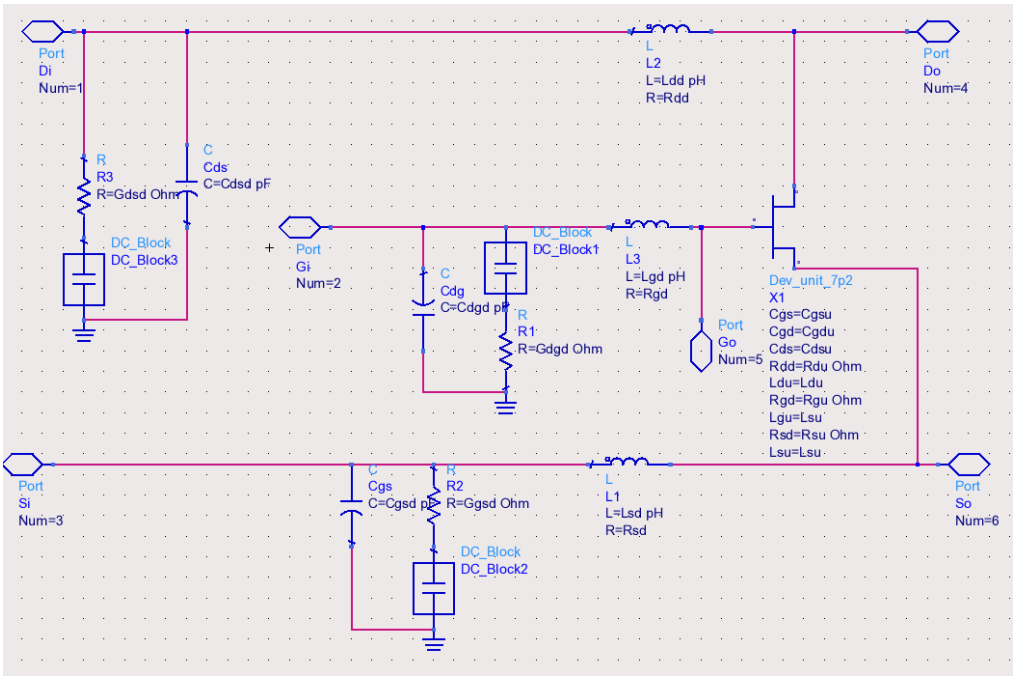

Figure 4.3: Distributed Block Circuit

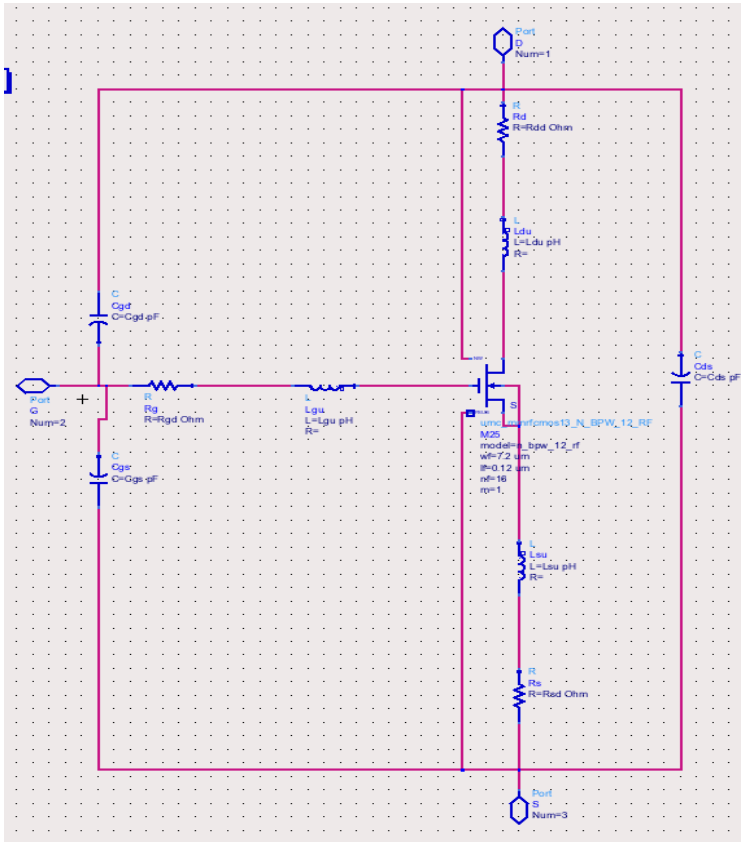

Figure 4.4: Device Block Circuit

The above blocks are connected together in accordance with the measured power cell configurations. There are two source connectors modeled, as there are two source ground connections in the measured power cell, one for each port. Figure 4.5 shows the complete power cell model for the 115.2x8 power cell.

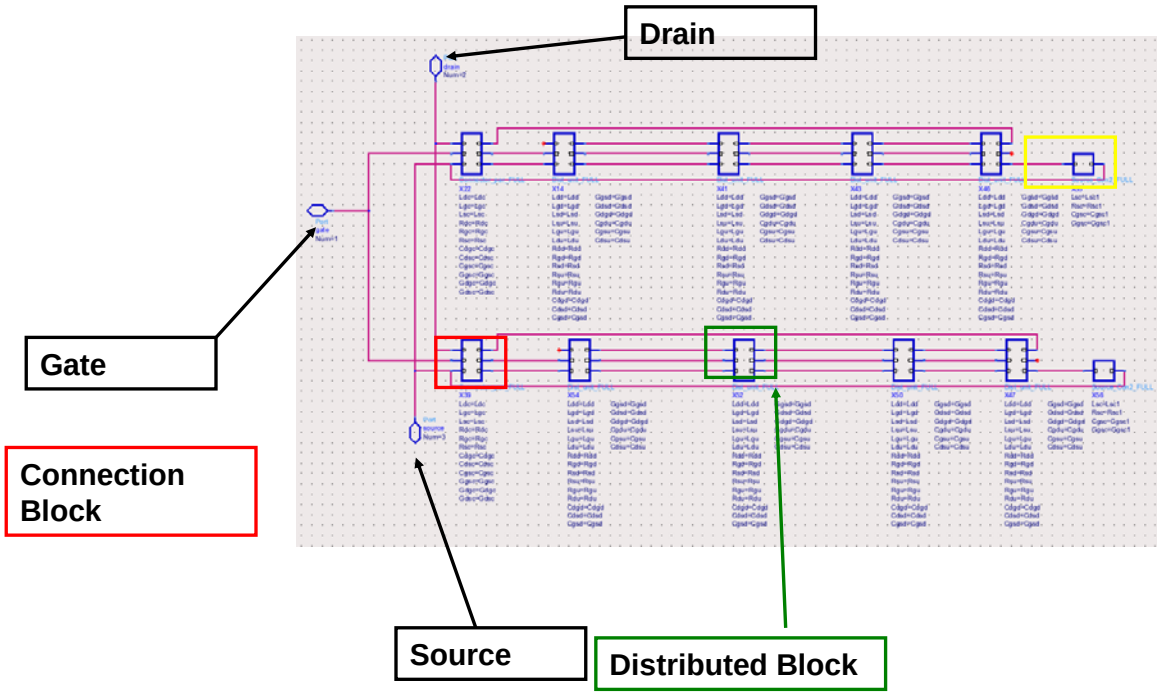

Figure 4.5: Device Block Circuit

The above described model was constructed, and the values for the circuit components were determined using an optimization algorithm in the Agilent ADS software suite. Strong improvements in both DC and RF modeling were observed. The results are shown below.

4.3 Results

After determining optimal circuit values, the Power Cell model was simulated and compared with both the measured data and the RF-BSIM3 modeled responses. Figure 4.6

shows the DC family curve and Gm analysis for the RF-BSIM3, Power Cell model and measured data for the 115.2x8 and 115.2x16 power cells.

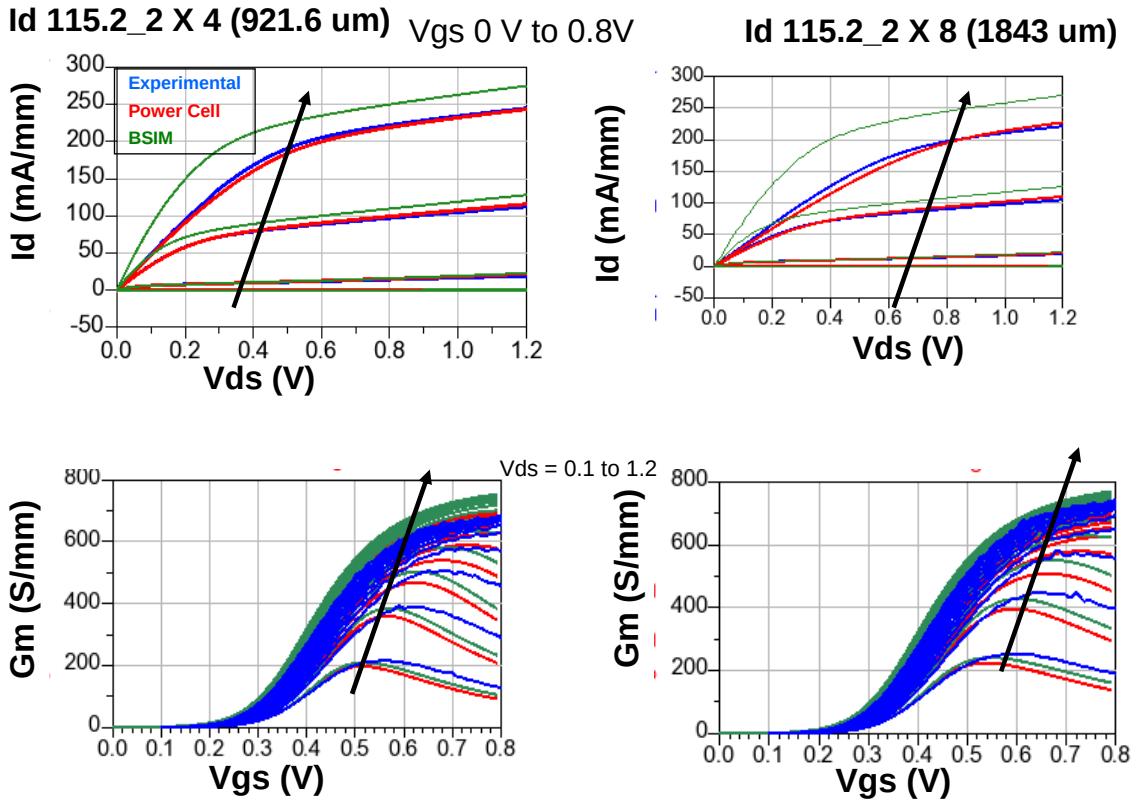

Figure 4.6: DC Model Simulation Results

The Power Cell model is significantly more accurate than the BSIM3 in both the turn-on and saturation regions. Correcting the voltage seen at the active device terminals is a necessary step towards correcting RF behavior. S parameters were modeled between frequencies of 0.5 GHz and 10 GHz every 100 MHz. From the results of these data, Ft and Fmax were computed. Figure 4.7 shows the Ft and Fmax for both the 115.2x8 and 115.2x16 power cells.

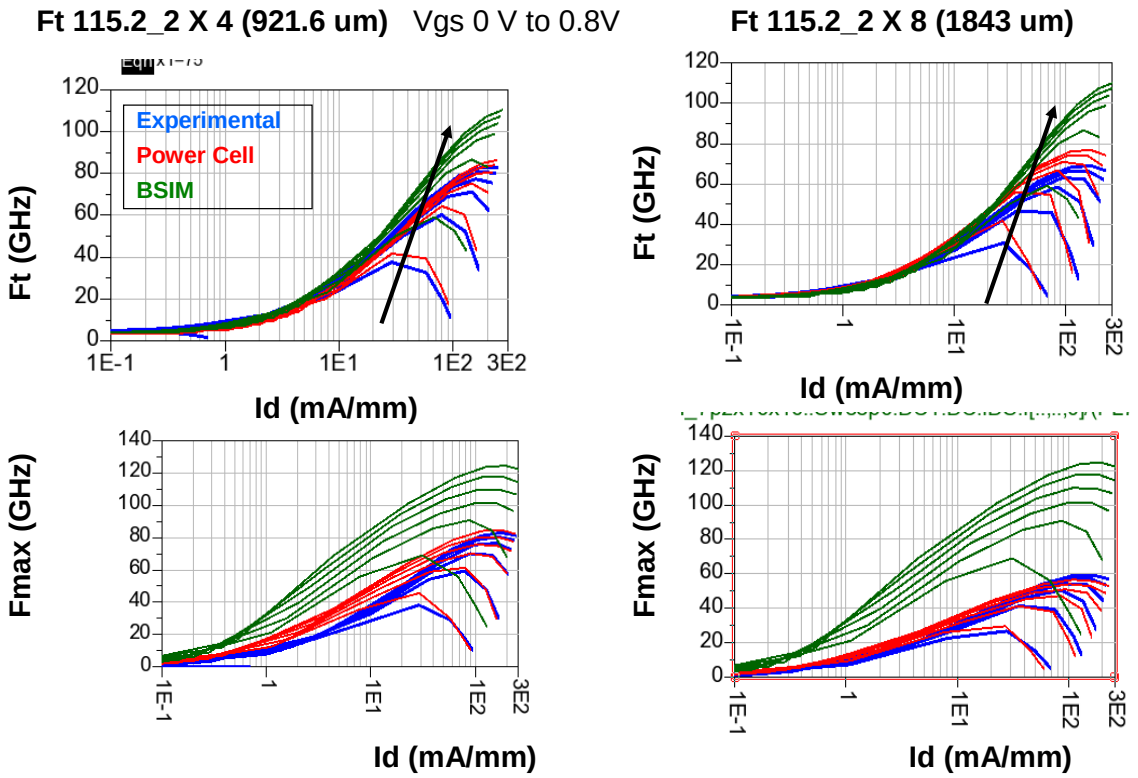

Figure 4.7: Ft, FMax Model Simulation Results

The Power Cell model provides significantly more accurate simulation results than the standard RF-BSIM3 for large gate width power devices.

5. Conclusions

By incorporating layout effects and scalability, the Power Cell model more accurately predicts both DC and high frequency behavior than the RF-BSIM3 model at high multiplicity. As wavelengths at higher frequencies approach the size of power cells, connectors within the power cell need to be treated as transmission lines. Phase delay over the power cell and substrate loss must be accounted for to significantly improve model behavior. In the Power Cell model, connectors are modeled in a modular fashion, allowing the model to be easily scaled by adding component blocks. A summary of the results for the RF-BSIM3, Power Cell model and measured results is given in Table 5.1.

The ability to accurately predict large gate width NMOS amplifiers will enable for the successful design of silicon power amplifiers at high frequencies. This will allow for greater levels of integration within high speed communication systems, lowering cost for manufacturers.

Table 5.1: Results for Comparison of RF-BSIM3 and Power Cell Model

Power Cell	Id (mA/mm)	Gm (mS/mm)	Ft (GHz)	Fmax (GHz)
7p2x16x16 BSIM3	270.5	752.5	107.2	124.5
7p2x16x16 Power Cell	227.5	695	76.8	56.6
7p2x16x16 Measured	221.5	679	69.1	58.8
7p2x16x8 BSIM3	275	769	110.3	123.8
7p2x16x8 Power Cell	243.4	709.5	86.4	84.7
7p2x16x8 Measured	244.8	721.9	82.8	82.9

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