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COMPACT DEVICE MODELING AND MILLIMETER-WAVE
OSCILLATOR DESIGN FOR III-V HBT TECHNOLOGY

BY

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DISSERTATION

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ABSTRACT

The double heterojunction bipolar transistor (DHBT), through its bandgap engineering, possesses several very favorable traits that allow it to operate at high frequencies while still maintaining impressive breakdown, linearity, and current driving characteristics. These traits make it a highly desirable device for both millimeter-wave and high-speed mixed-signal circuits. However, as the complexity of the circuits that can be realized with DHBTs increases, new compact large-signal models are needed to properly model the physical operation of these devices, because current models are based on older homojunction bipolar technology. A physically scalable DHBT model, the UIUC SDD2, is developed specifically for DHBT technology and shown to outperform the often-used VBIC model in both individual device modeling and full circuit simulation. Additionally, tunable clock generator and frequency synthesizer circuits implemented in an indium phosphide (InP) DHBT technology are designed, fabricated, and measured to show the ability of this technology to implement fully integrated sources with moderate power dissipation at millimeter-wave frequencies.

For my family

ACKNOWLEDGMENTS

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1. INTRODUCTION

Even with the current dominance of CMOS in the IC industry, radio frequency and high-speed mixed-signal circuits continue to rely on compound semiconductor devices to push circuit operation deep into the millimeter (>30 GHz) and sub-millimeter (>300 GHz) frequency range [1]. InP-based heterojunction bipolar transistors (HBTs) are capable of simultaneously achieving both a unity current gain frequency (f_T) and maximum frequency of oscillation (f_{MAX}) in excess of 300 GHz, while maintaining a respectable breakdown voltage ($BV_{ceo} > 4$ V), which serves to further increase the linearity of the device. These traits, when coupled with the intrinsically good thermal properties of the devices, due to the low thermal resistance of InP, make them a prime technology for ultra-high-speed radio frequency (RF) circuit design [2-3]. HBTs further distinguish themselves from InP-based high electron mobility transistors (HEMTs) by their current driving capability, which results in both higher f_T and, possibly more importantly, it is claimed, their C_{bc}/I_c metric that dictates how fast mixed-signal and digital designs operate, making them appealing to high-speed mixed-signal designers [4].

Commercially accessible HBT foundries still rely on the readily available VBIC model to simulate their complex HBT devices. The use of the VBIC model can prove problematic, especially for complex nonlinear designs, because it was developed for older silicon bipolar technology and does not completely model the physics of modern HBT devices [5]. Effects stemming from the heterostructure nature of both junctions are poorly modeled in the VBIC model, which can lead to poor large-signal modeling of III-V devices and circuits [6], or to limiting the range of operation over which the VBIC model can confidently model device performance. These model inaccuracies limit the circuit designer to only that device operating

range which can be properly modeled, and potentially limits the performance of her/his design. To truly allow for the full utilization of the device technology, HBT foundries need to change their default model from the antiquated VBIC to a more suitable model that can better simulate the performance of these more complex devices.

This dissertation is focused on further developing large-signal double heterojunction transistor (DHBT) models, and using these models to design millimeter-wave mixed-signal circuits that have been taped out in industrial 500 nm InP DHBT processes. Chapter 2 documents the development of a physically scalable Type-I DHBT large-signal model, the Type-I UIUC SDD2 model, for the modeling of commercial devices, and the development of a Type-II DHBT model, the Type-II UIUC SDD2 model, to project the circuit performance of cutting edge Type-II DHBTs being developed at the University of Illinois. Chapter 3 describes the design and measurement of a circuit designed with the Type-I UIUC SDD2 model in order to validate the model's ability to simulate the performance of a complete circuit, and to directly compare the simulation accuracy, versus measured data, of the SDD2 and VBIC models. Chapter 4 gives an overview of a high-frequency tunable clock generator designed in a commercial InP-based DHBT technology, and Chapter 5 documents an innovative push-push oscillator with integrated 128x frequency division which comprises the high-frequency circuit components of a PLL-based frequency synthesizer. Future work needed to advance both III-V DHBT models and monolithically integrated oscillators is discussed in Chapter 6.

2. LARGE-SIGNAL INP DHBT DEVICE MODELING

2.1 – Scalable Type-I DHBT SDD Model

2.1.1 – Introduction

Several models that are specifically based on modern HBT devices (AgilentHBT, HiCUM and UIUC SDD2) have been developed in an attempt to give more accurate large-signal modeling and more reliable circuit designs. The UIUC SDD2 (symbolically defined device) model has been shown to be especially good at modeling large-signal characteristics for both individual devices and complex circuits [7]. The SDD's strength is its ability to model carrier velocity modulation in the collector and the current blocking of the base-collector junction. The model however lacks emitter scalability and temperature dependence, limiting circuit designs to the use of only one size of device at one operating temperature.

A temperature dependent, scalable large-signal DHBT model that is based on the UIUC SDD model is developed and is the focus of this section. This new SDD2 model is currently capable of providing accurate DC, RF, and large-signal modeling over emitter sizes from $0.5 \times 3.0 \mu\text{m}^2$ to $0.5 \times 5.2 \mu\text{m}^2$. The model, when compared with the VBIC model extracted and issued by the device manufacturer, is shown to be far superior in modeling all aspects (DC, RF, and nonlinear large-signal) of the device. As there are no AgilentHBT or HiCUM models currently available in HBT design kits, a direct comparison of the UIUC SDD2 model to these models cannot be made. Attempts at extracting these more advanced models to allow for a direct comparison to the UIUC SDD2 model would lead to inaccurate comparisons, as the quality of the model's fit to measured data would rely greatly on the skill and knowledge of the model extractor and would most likely not extract the full capability of the model. For this reason,

direct simulation comparisons are only made with the VBIC model extracted by the foundry and delivered with the process design kit (PDK). Ideally for a true comparison of the model, model developers would extract their model for a given set of measured device data, and use the model to simulate a given circuit. Comparisons of the measured circuit performance to the simulated would give a good indication of the ability of each model.

2.1.2 – UIUC SDD2 Model Overview

In the late 1990s the HSIC group at the University of Illinois began developing a large-signal model for the heterojunction bipolar transistor. The initial model, the SDD1 model, was developed for single heterojunction bipolar transistors and is based on the Gummel-Poon integral charge control relation which models the Early effect and gain compression at high collector currents due to the Kirk effect. In addition, a thermal network was included in the SDD1 model to account for device self-heating effects [8].

The UIUC SDD2 model is an extension of the SDD1 model for double heterojunction transistors. Effects stemming from the heterostructure nature of the base-collector junction, such as current blocking and velocity modulation of the carriers as they pass through the collector, were added to create a model that physically describes current flow through DHBTs. One of the principal features that distinguishes this model from VBIC is the SDD2's ability to accurately model bias dependent current blocking effects. Figure 2.1 shows the band configuration at the base-collector interface for two identical devices operated in the forward-active mode ($V_{BC} < 0$) with a common reverse bias, but different levels of current injection. Little current blocking occurs at a low injection level because the external electric field bends the bands in such a way that the band discontinuity has little effect on the electron current flow. At a high injection, the

large number of mobile electrons in the collector reduces the magnitude of the reverse biased field. With the bias effectively reduced, the band discontinuity is no longer suppressed, leading to a significant current blocking. This effect is modeled in the SDD2 model through the use of a voltage and current dependent nonlinear resistance at the collector. As the magnitude of the collector current increases, the resistance increases to model the increased current blocking. As the reverse bias increases, the resistance decreases, simulating the bending of the bands that reduces the current blocking.

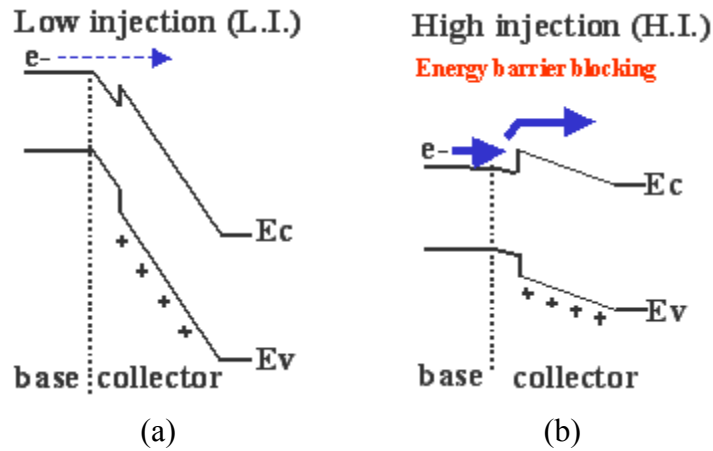


Fig. 2.1: Base-collector charge transport at low and high injection.

The consequence of hetero-interface current blocking is most easily seen in the device's DC current-voltage family of curves (Figure 2.2). Graphically this effect manifests itself by rounding out the sharp bend seen in the current loci at the knee voltage. This reduction of collector current also affects the velocity modulation of carriers traveling through the depleted collector, because the reduction of current reduces the number of mobile carriers in the depleted collector and therefore alters the total induced field in the collector. Also, the effective base transit time of the device increases, since some percentage of the electrons traversing the base region are reflected back into the base by the conduction band discontinuity.

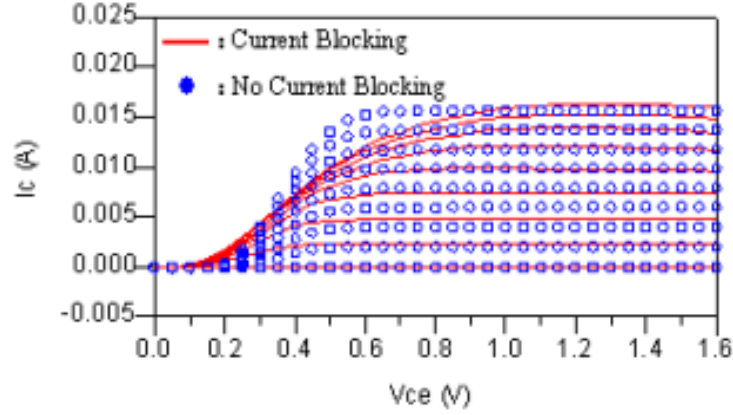


Fig. 2.2: Current blocking effects in the DC-IV family of curves.

Through the accurate modeling of current blocking and velocity modulation in the collector, the SDD2 model provides a very accurate modeling of Type-I DHBT device nonlinearities, and allows for the accurate simulation of high-frequency nonlinear circuits. As a confirmation of the SDD2's modeling ability, a variable gain amplifier was designed. Two-tone intermodulation distortion measurements were compared with the simulated intermodulation distortion. Figure 2.3 shows the superior performance of the SDD2 model over the foundry distributed VBIC model [9]. However, this version of the SDD2 model is limited to modeling a single size device since it incorporates no device scaling equations. To be truly useful, the model must be made scalable.

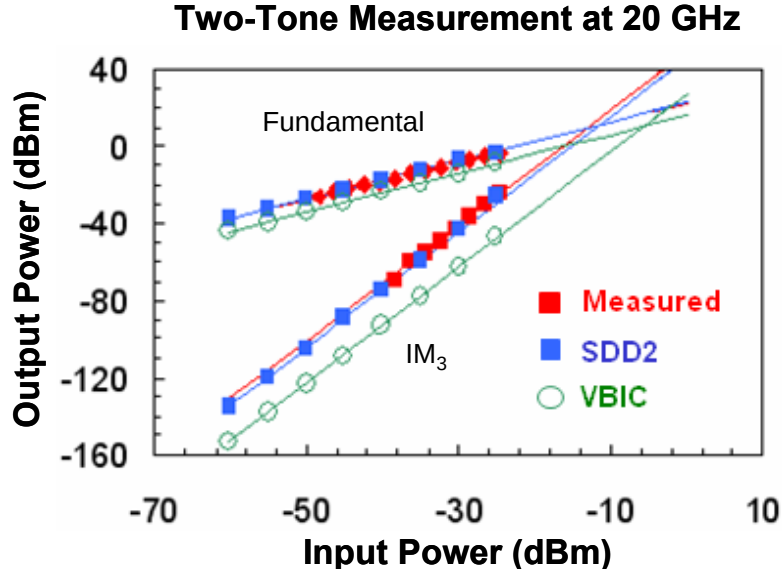


Fig. 2.3: Measured vs. SDD2 and VBIC modeled intermodulation measurement [7].

2.1.3 – Scalable Model

The scalable SDD2 model is developed from the original UIUC SDD2 model, which, at its foundation, is based on the Gummel-Poon integral charge control relationship derived for high current density bipolar devices [10]. The SDD2's model topology (Figure 2.4) is developed for a standard mesa-based heterojunction process with contacts arranged in a collector-emitter-base (CEB) configuration. In its parasitic and extrinsic modeling, the model incorporates the parasitic capacitances and inductances of the contacts to the device, the extrinsic base-collector junction along with its associated capacitance, the extrinsic distributed base resistance, the extrinsic emitter resistance, and the extrinsic collector resistances. The parallel diodes, capacitor, and current source shown in Figure 2.4 model the intrinsic device (the portion of the HBT directly beneath the emitter). It is here that the transistor action occurs.

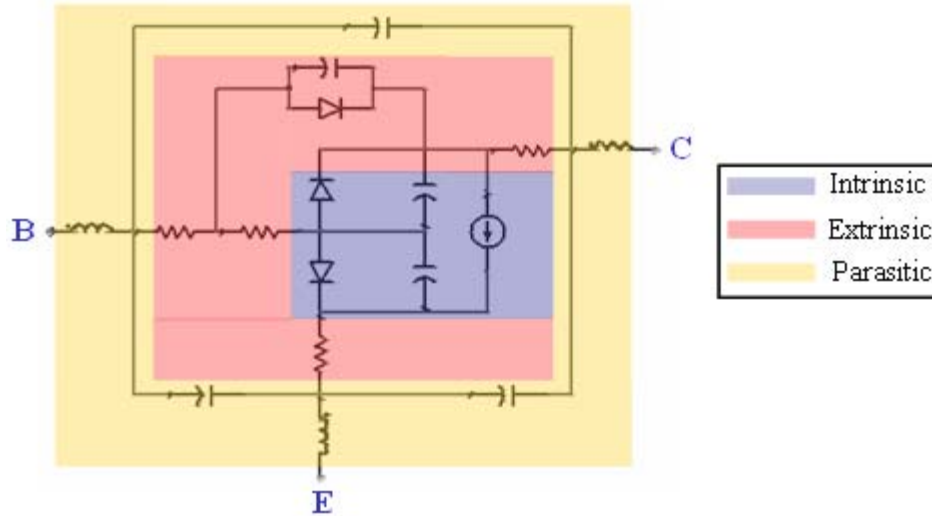


Fig. 2.4: Scalable SDD2 topology.

This model, implemented as a symbolically defined device in Agilent's Advanced Design System (ADS), is extracted for the Vitesse VIP2 DHBT process. The scaling of the model is unique in that it closely models the physical scaling of modern DHBT devices. High-speed HBT devices have been shrunk to such small sizes that the width of an emitter finger is often on the same scale, if not smaller, than the minimum diameter of the via used to contact the semiconductor. To allow current flow into the device, a via must connect the lowest metal layer and the emitter. The need for this large contact results in a separation of the emitter into a wide non-scalable region, the region around the emitter via where current is injected, and a narrow scalable region, the remainder of the finger (Figure 2.5).

The actual dimensions of the intrinsic device (the portion directly beneath the emitter) are quite different from the drawn length that is given to the circuit designer. An attempt to model the scalable device parameters with only the given length and width would result in scaling errors, and any fits that would be achieved would be non-physical. Decomposing the emitter into two separate regions in the SDD2 model gives a much more accurate representation of

device scaling than is achieved by simply scaling by the overall area of the device, and leads to the SDD2 model giving a much better model of the actual device performance than does the VBIC.

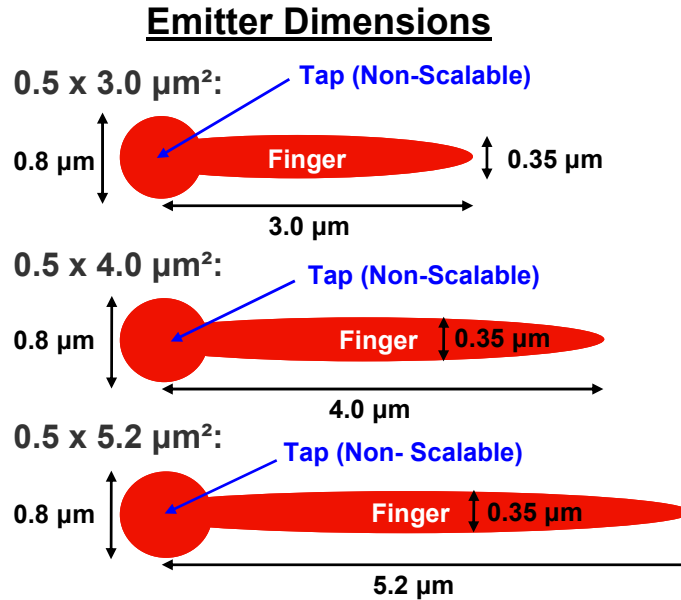


Fig. 2.5: Realistic emitter dimensions of high-speed HBT devices.

Effects from the emitter's tab section can be separated by first removing the finger section from the model and modeling a device consisting solely of a tab (non-scalable emitter portion). After a model is developed for this simpler device, finger parameters can be added to the model and larger devices can be modeled. In this way, the individual contributions of the separate parts of the device can be determined independently, giving a fairly straightforward way of modeling the effects that result from the non-uniform current density across the emitter of the device.

In order to scale properly, each level of the model (intrinsic, extrinsic, and parasitic) must be scaled to reflect the effect of dimension change on electrical properties. This is fairly straightforward for the intrinsic portion, as resistances, capacitances, and currents of the emitter

finger are either directly or indirectly proportional to the intrinsic finger size. However, there is not a direct relationship between the intrinsic size of the device and the electrical properties of the extrinsic and parasitic levels. Extrinsic parameters associated with the finger, such as the emitter resistance and extrinsic emitter base capacitance, are implemented as a function of finger area in a three-term power series, while parasitic parameters are functions of the overall area.

2.1.4 – Model Extraction Procedure

In order to properly extract the scalable model, a device that consists entirely of the non-scalable portion of the transistor needs to be modeled first. By modeling this device, one can get an accurate separation of the scalable and non-scalable components of the model. After this device is properly modeled, the non-scalable parameters of the model have been completely determined and should not be changed when later modeling larger device sizes. As can be seen from Figure 2.6, the non-scalable tab is important to the operation of the device because it accounts for approximately half of the current that passes through the device and should therefore be extracted with care.

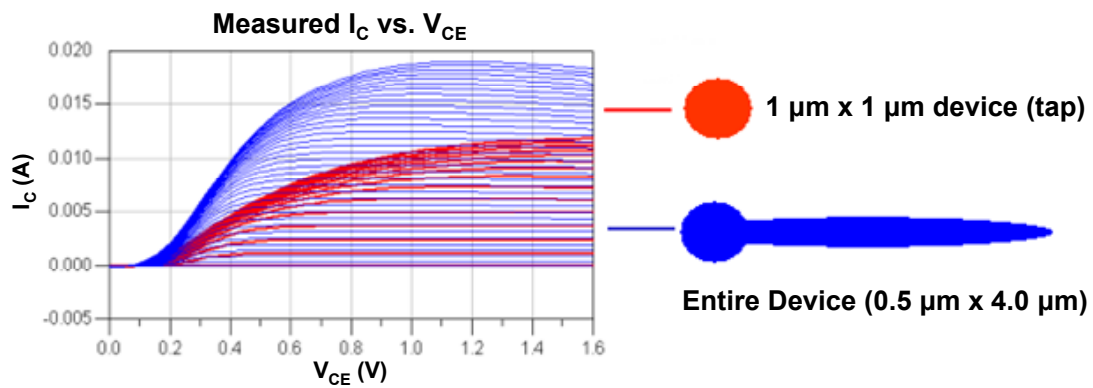


Fig. 2.6: Separation of current between emitter tab and emitter finger.

After the nonscalable section of the model has been extracted, a larger device that consists of both the nonscalable tab and a scalable emitter needs to be modeled in order to

correctly extract the parameters of the finger. Only the scalable portion of the model and its associated parameters should be used in extracting this larger device since the nonscalable device parameters are already extracted and should remain constant across device size.

Once both the scalable and nonscalable portions of the device have been extracted for a single size device, the remaining devices of different sizes are used to extract the linear and nonlinear scaling factors of the area-dependent scaling equations in the model. These equations account for the fact that device operation might not perfectly scale along with the overall size of the device. However, if the model has been properly extracted up to this point, then it should automatically scale to give fairly decent fits to measured data from other size devices.

2.1.5 – Verification

Four means of verifying the scalable modeling ability of the SDD2 model are presented. Measured versus modeled comparisons are shown for large-signal DC current-voltage families, extrapolated f_T , forward-Gummel plots and large-signal single-tone measurements.

All DC measurements were taken using an HP4142B DC source monitor unit. Figures 2.7 and 2.8 show the large-signal DC modeling ability of the scalable SDD2 and the VBIC model that was provided by Vitesse. The scalable SDD2 model gives a much more accurate fit across all of the measured devices than does the VBIC. The discrepancy between the models is most evident around the knee voltage, where significant current blocking occurs. SDD2 also correctly models the drop in current at high biases caused by the self-heating effects of the device. Forward-Gummel measurements and model comparisons are shown in Figure 2.9 on page 13. The scalable SDD2 provides nice fits to the measured data across all devices sizes.

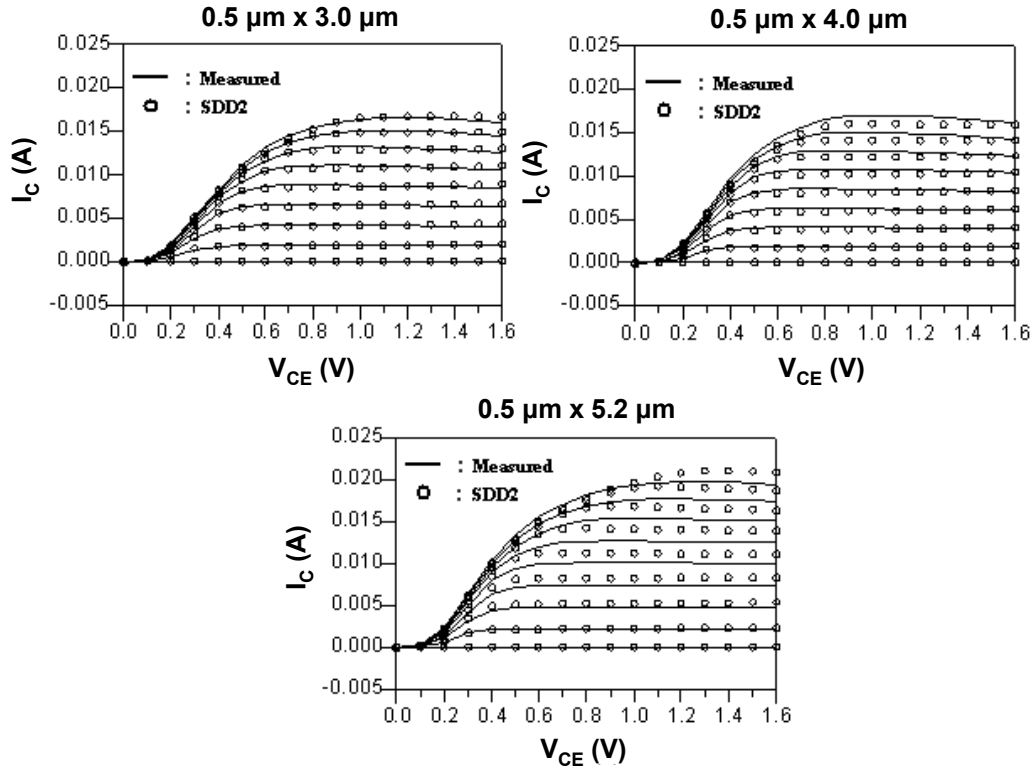


Fig. 2.7: Measured vs. SDD2 modeled large-signal DC results (V_{CE} : 0-1.6 V, I_B : 0-160 μA).

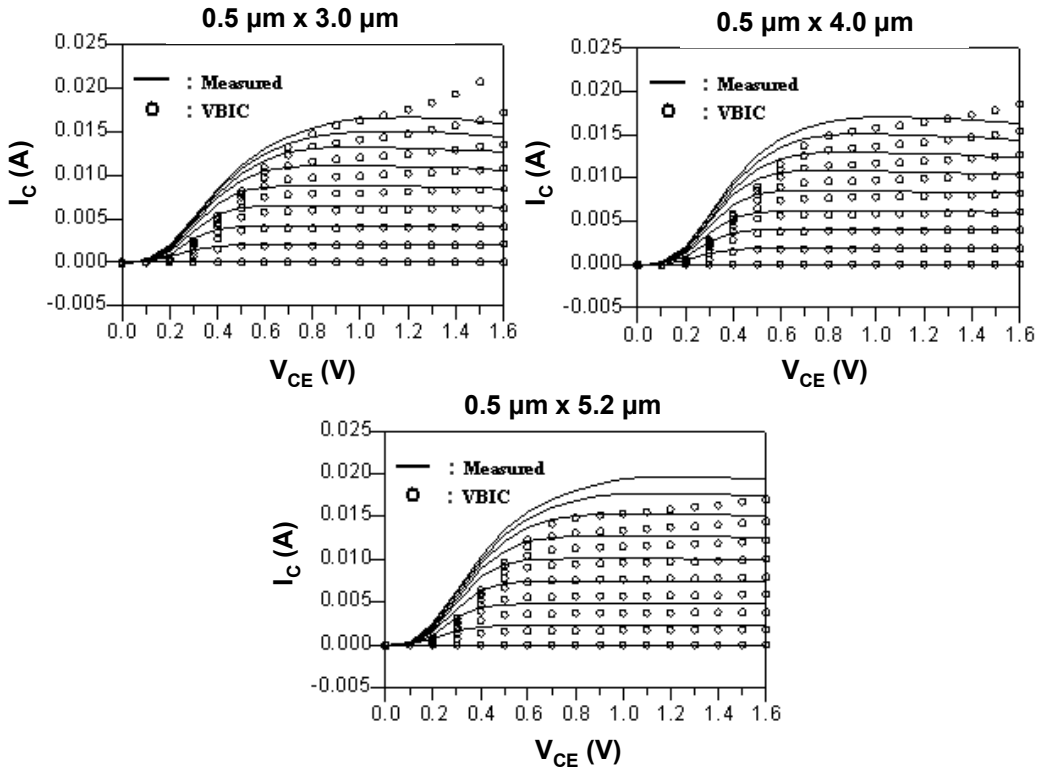


Fig. 2.8: Measured vs. VBIC modeled large-signal DC results (V_{CE} : 0-1.6 V, I_B : 0-160 μA).

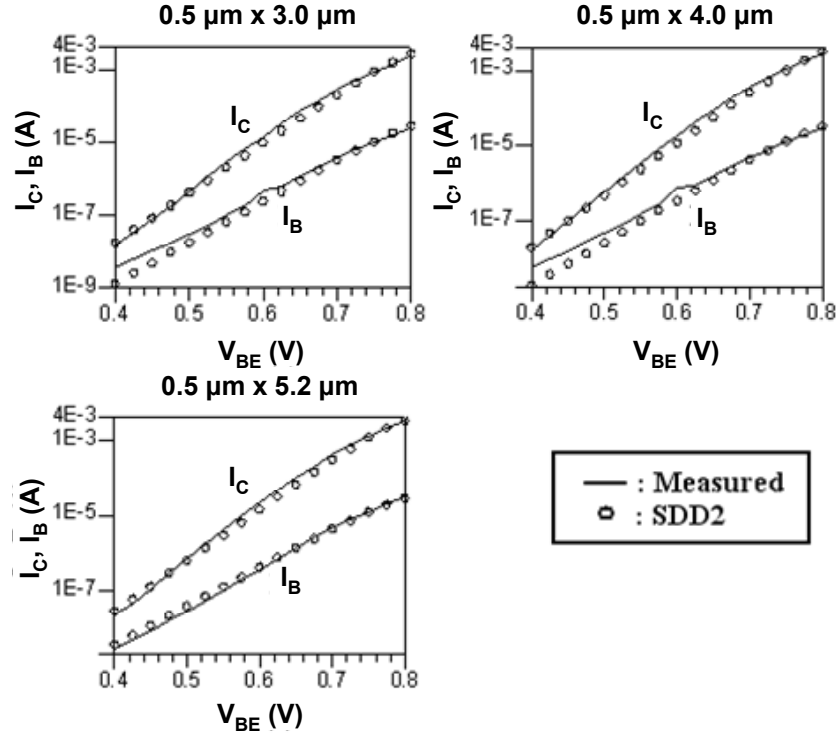


Fig. 2.9: Measured and SDD2 modeled forward-Gummel data (I_C and I_B vs. V_{BE} , as V_{CB} is held at 0 V).

The measured versus modeled device unity current gain frequency (f_T) is plotted with respect to bias current and shown in Figures 2.10 and 2.11. S-parameters of the devices were measured with an Agilent 8364A PNA and the f_T at each bias was extrapolated with a -20 dB/decade slope from the calculated h_{21} at 40 GHz. The scalable SDD2 model provides very accurate results, while the VBIC model under-calculates the measured f_T by approximately 50 GHz.

The ability of a model to accurately model the nonlinearity of a device is extremely important if it is going to be used to design any large-signal circuit such as an oscillator or power amplifier. One method of determining the linearity of a device is to send a large-signal into the device and measure the power of the harmonics at the output. This single-tone measurement was carried out on the Vitesse devices using an Agilent 8364A PNA as a power source and an

Agilent 8565E spectrum analyzer to measure the first three output tones (fundamental and 2nd and 3rd harmonics). This measurement was simulated in ADS through the use of a harmonic balance simulation, and modeled values for the output harmonics with respect to input power were obtained. Figure 2.12 shows the measured and scalable SDD2 modeled values obtained for a 2 GHz input tone from -20 dBm to 0 dBm at a $V_{CE} = 0.6V$, $I_B = 140 \mu A$ bias.

The SDD2 model gives a very nice fit at this high current bias point, which is in the highly nonlinear knee region of the device. The modeling of the fundamental output and third harmonic is extremely accurate across the entire power range. The second harmonic is under-predicted at lower input powers, but converges with the higher power data. There is no VBIC modeled data given due to the fact that the given VBIC model would not converge in simulation.

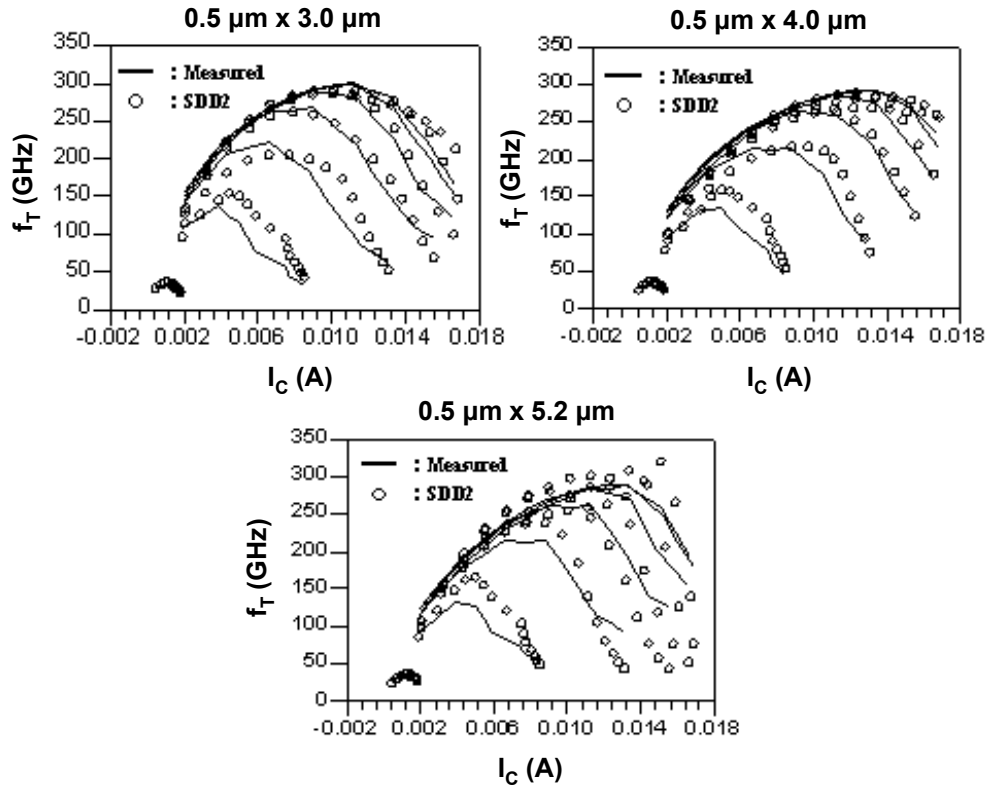


Fig. 2.10: Measured vs. SDD2 modeled f_T results (V_{CE} : 0-1.4 V, I_B : 0-160 μA).

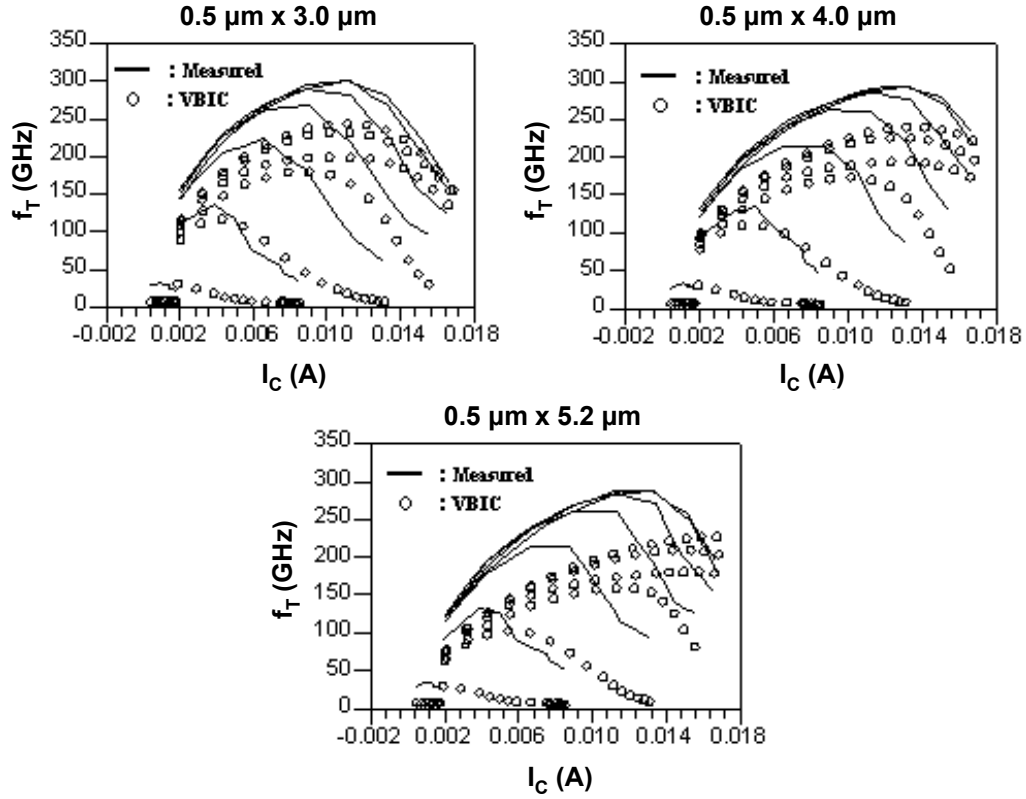


Fig. 2.11: Measured vs. VBIC modeled f_T results (V_{CE} : 0-1.4 V, I_B : 0-160 μA).

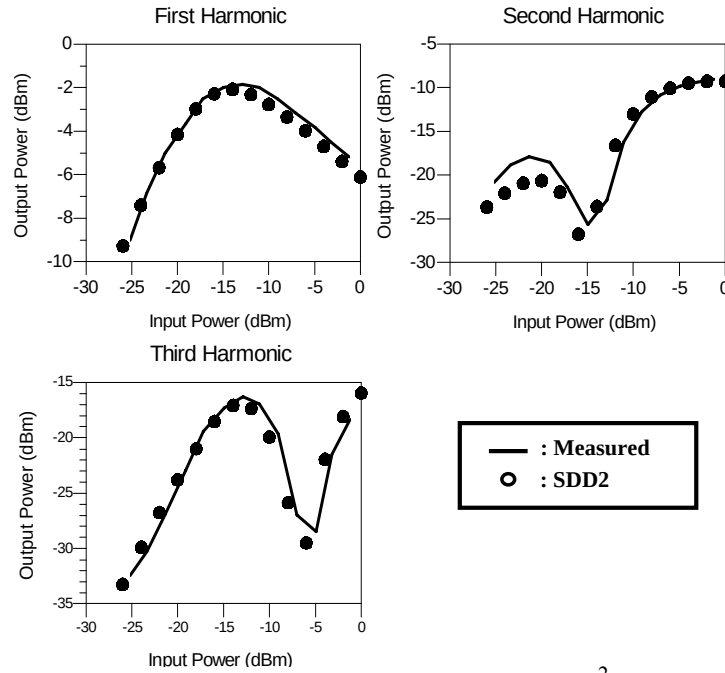


Fig. 2.12: Measured and SDD2 modeled output of a 0.5 X 3.0 μm^2 device with 2 GHz input tone swept from -25 dBm to 0 dBm.

2.2 – Type-II DHBT SDD Model

2.2.1 – Introduction

Type-II InP/GaAsSb devices, similar to the DHBTs previously discussed but with a different layer structure, have been fabricated at the University of Illinois with cutoff frequencies (f_T) of over 630 GHz and balanced f_T/f_{MAX} of 480/420 GHz, all with a breakdown of over 3 V [11]. Given their impressive frequency performance and breakdown voltage, Type-II DHBTs are poised to be a major player in microwave and high-frequency mixed-signal circuits as operational frequencies approach the terahertz band. In order to precisely design these nonlinear microwave and mixed-signal circuits, an accurate large-signal model is required. As these devices are currently not available on commercially accessible processes, there is a lack of models to simulate their operation. Even Agilent, which runs a closed Type-II DHBT process, developed their AgilentHBT model for the modeling of Type-I DHBTs [12].

In order to accurately project the large-signal behavior of future integrated Type-II DHBT circuits based on the measured performance of devices fabricated at the University of Illinois, a large-signal InP/GaAsSb Type-II model was developed at the University of Illinois. The model is implemented as a symbolically defined device in Agilent's Advanced Design System (ADS), and is based on the well-established UIUC SDD Type-I InP/InGaAs model, but has been altered to model the different charge transport phenomena that occur in Type-II devices. The model is extracted for a balanced f_T/f_{MAX} Type-II device fabricated at the University of Illinois and is capable of giving an excellent fit to both measured DC and RF data across the entire bias range of the device. The UIUC SDD Type-II model has been tested in high-frequency mixed-signal circuit simulations through the design and simulation of a 200 GHz static frequency divider, which will be described.

2.2.2 – Type-I/Type-II DHBT Comparison and Model Overview

Type-II DHBTs have charge transfer characteristics that are significantly different than their Type-I counterparts due to the relative position of their base conduction and valence band. Typical band alignments for Type-I and Type-II DHBTs are shown in Figure 2.13. Injection of carriers from the emitter to the base is totally thermionic since there is no conduction band spike at the BE junction, as in Type-I alignment, leading to Type-II devices having longer base transit times than Type-I devices, when Type-I devices are biased so the heterointerface current blocking is minimized. Type-II devices however have a desirable base-collector offset that allows minority carriers in the base to be energetically injected into the collector. The Type-I base-collector barrier blocks current injection into the collector, giving Type-I devices poorer linearity due to the DC current blocking effect and a greater modulation of the collector transient velocities.

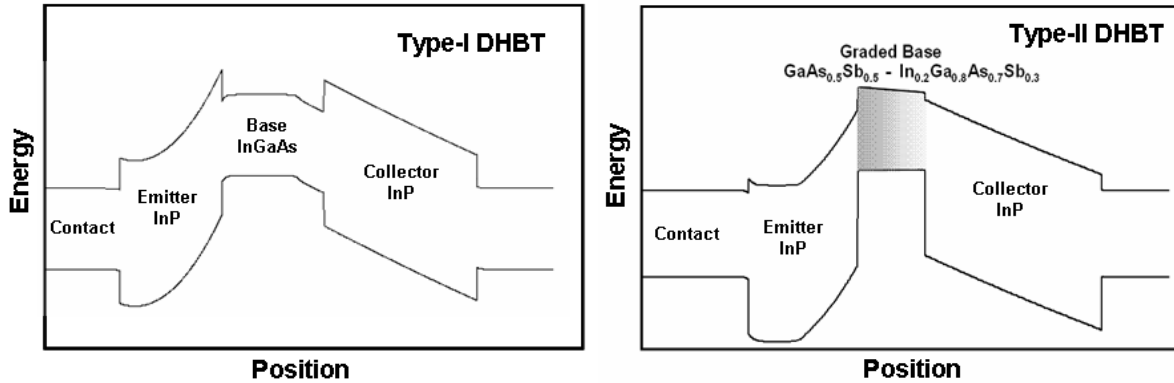


Fig. 2.13: Type-I and Type-II DHBT band structures.

Another advantage of the Type-II DHBT over the Type-I DHBT is a lowered V_{CE} turn-on voltage. This is a result of the reduction of the minority electron current that is injected from the collector to the base at positive base-collector voltages. Since, in mesa-based HBT designs, the collector is physically much larger than the emitter, at low V_{CE} biases, the electron current

flowing from the collector to the base can be larger than the electron current flowing from the emitter to the base, giving a net negative output I_c current (positive carriers). The reduction of this backwards injecting electron current by the obstructive base-collector conduction band discontinuity reduces the reverse current that the emitter has to overcome before the device “turns on” and provides a positive collector current. This effect is easily seen in Figure 2.14, in which the output current family of curves for a Type-I and a Type-II DHBT are compared. This lower turn-on is very beneficial for the Type-II device in that it increases the allowable voltage swing in the device. Furthermore, it is beneficial in that it allows for a lower power operation in Type-II devices since they can be operated at lower collector-emitter voltage biases than can Type-I DHBTs.

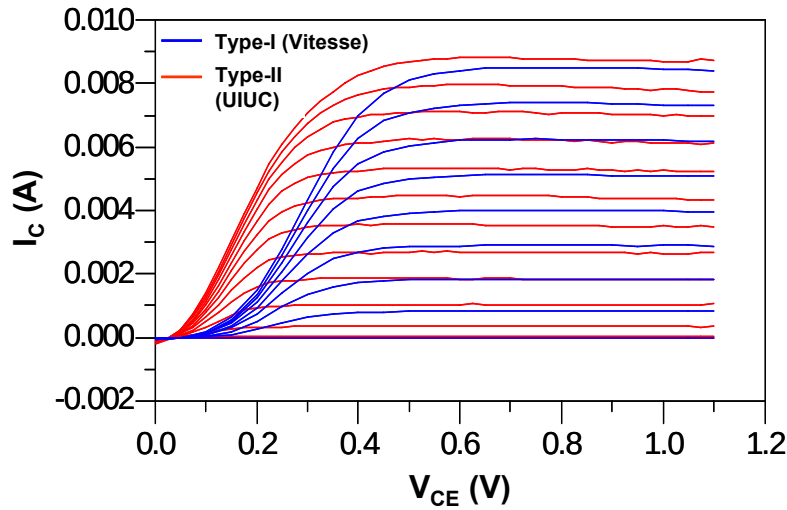


Fig. 2.14: Measured Type-I/Type-II DC comparison.

The UIUC SDD Type-II model is based upon the UIUC SDD Type-I model [6], which at its core is based on the traditional Gummel-Poon integral charge control relation [10]. This relation has been modified in this Type-II model to account for the thermionic transfer of carriers from both the emitter and the collector into the base by the incorporation of the Richardson thermionic emission voltage-current relationship:

$$J = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (2.1)$$

where ϕ_B is the barrier potential and A^* is the effective Richardson coefficient [13]. In addition, the base-emitter diffusion capacitance is increased and collector transient times are decreased to account for slower base and faster collector carrier velocities. The magnitude of the UIUC SDD Type-I heterointerface current blocking modeling parameters [6] is reduced to account for the reduced, but not eliminated, current blocking that occurs at the base-collector junction [14].

The overall model topology is identical to the UIUC SDD Type-I model, as is seen in Figure 2.4. The model has three levels: intrinsic, extrinsic, and parasitic. The model topology is developed for a standard mesa-based heterojunction process. It is in the intrinsic level that the core Type-II modeling is embedded.

2.2.3 – Model Verification

Three means of verifying the modeling ability of the UIUC SDD Type-II model are presented. Measurements were taken of device DC current and voltage families, forward-Gummel characteristics, and extrapolated unilateral current gain frequency (f_T) versus I_C bias. Each of these measurements was used to extract the parameters of the model and, when compared to the modeled values, gives an indication of the modeling accuracy.

All DC measurements were taken using an HP4142B DC source monitor unit. Figure 2.15 shows the measured and modeled collector current versus collector-emitter voltage and base-emitter voltage versus collector-emitter voltage for a base current from 0 to 2 mA. From the I_C versus V_{CE} plot we can see that the model is extremely capable of modeling the DC large-signal characteristics of the device. It properly models the device collector-emitter turn-on

voltage and knee effects. The V_{BE} versus V_{CE} measurement is used as a metric to determine the model's accuracy at modeling base current injection across all bias points. At high base current injection, the model accurately calculates the increased hole leakage into the emitter due to increase in device temperature, which shows itself as a roll-off of the V_{BE} versus V_{CE} curve.

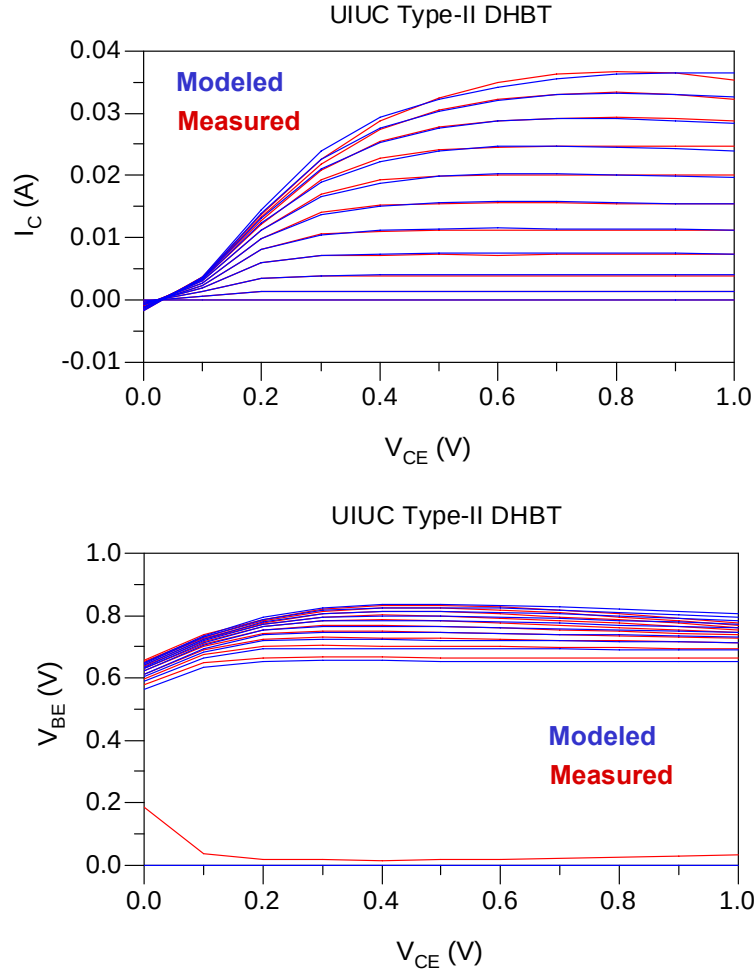


Fig. 2.15: DC current and voltage families of device ($I_b = 0 - 2$ mA).

Comparisons of the measured and modeled forward-Gummel characteristics of the device (Figure 2.16) show that the model correctly models both minority and majority charge injection across the base-emitter junction. This device has a very large I_C - I_B crossover voltage, which is believed to be due to bad isolation of the base and emitter metals. The UIUC SDD Type-II

model is still able to model this with the addition of an additional leakage current path around the junction.

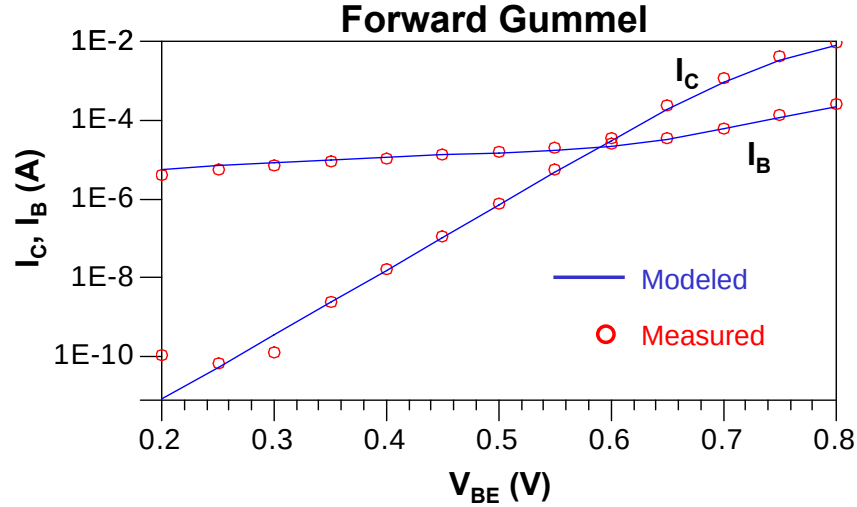


Fig. 2.16: Forward-Gummel characteristics of device.

The S-parameters of the device were measured from 500 MHz to 50 GHz with an Agilent 8364A Parameter Network Analyzer (PNA). From the S-parameters, the unity current gain frequency (f_T) of the device was determined by extrapolating the magnitude of h_{21} at a slope of -20 dB/decade to 0 dB. The measured (extrapolated) values of f_T are used as the main assessment of the model's small-signal RF modeling ability. Figure 2.17 shows a comparison between the measured and modeled f_T versus I_C bias. Each locus of points represents a constant collector-emitter voltage, with I_B being swept from 0 to 2 mA. The model gives a good representation of the device RF characteristics.

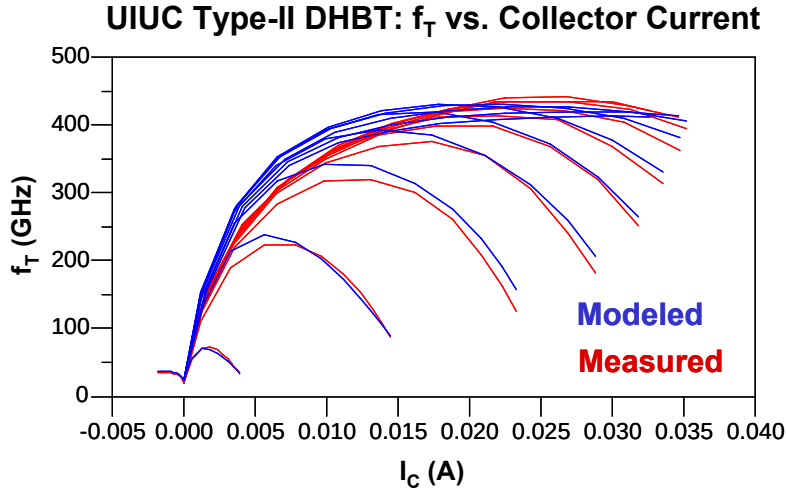


Fig. 2.17: f_T vs. collector current.

2.2.4 – Mixed-Signal Circuit Design

Since the UIUC Type-II process has not yet developed to a circuit level, as verification that this device model will work properly and give the expected results in high-frequency mixed-signal circuit design, the UIUC SDD Type-II model is used to design and simulate a static frequency divider. Static frequency dividers are a common mixed-signal circuit, and are often used to benchmark a new technology or process, because they give a clear indication of how fast the given devices can operate in a tightly integrated mixed-signal design where typical metrics like f_T and f_{MAX} are not as relevant. They are also commonly used in the feedback path of phase-lock loops to facilitate high-frequency synthesis, since they are capable of providing frequency division across a broad bandwidth.

A static frequency divider is essentially a flip-flop with negative feedback between its output and input so that the output transitions every time the clock signal transitions twice, providing an output signal whose fundamental frequency component is half that of the input clock signal. A schematic showing the basic operating principles of the divider is shown in

Figure 2.18. When operated at high frequencies, the input and output device impedances tend to filter all but the fundamental component of the signal, giving practically sinusoidal signals.

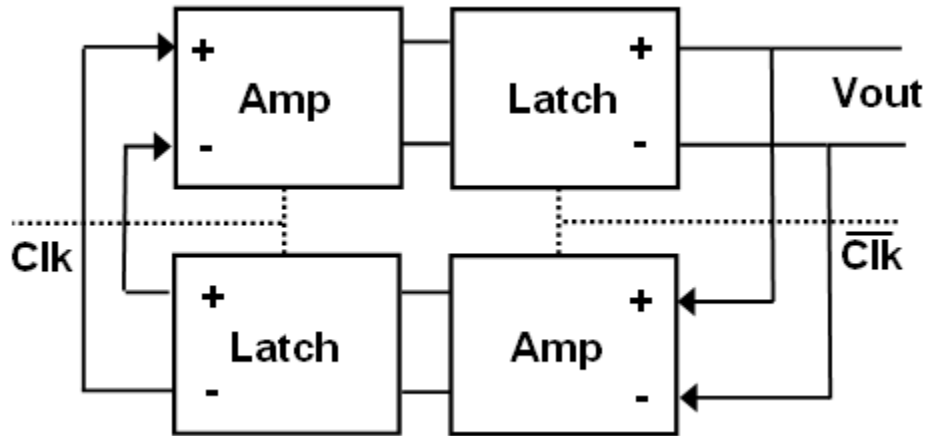


Fig. 2.18: Block diagram of static frequency divider.

This design is implemented in emitter coupled logic (ECL) because this logic style is extremely fast and well suited to DHBTs. ECL circuits are capable of operating at very high frequencies due to the fact that ideally all of the devices in the circuit will remain in the forward-active mode of operation at all times. In the forward-active mode, the base-collector junction is reversed bias, which results in short collector transit times and a low intrinsic base-collector capacitance. Reduced transit times and capacitances allow transistors to be charged rapidly [15].

The core design consists of two identical amp/latch pairs as shown below in Figure 2.19. A differential input clock signal drives a differential pair that essentially routes current between the amplifier stage and the latching stage. When the amplifier is active, it amplifies its differential input and charges the inactive latch to create a seed voltage. When the latch is activated, this seed voltage is amplified and latched by positive feedback through the emitter follower stage. Peaking inductors are used at the amplifier load in an attempt to cancel out the

output parasitic load capacitance, effectively putting a zero in the transfer function, to increase the bandwidth of this circuit.

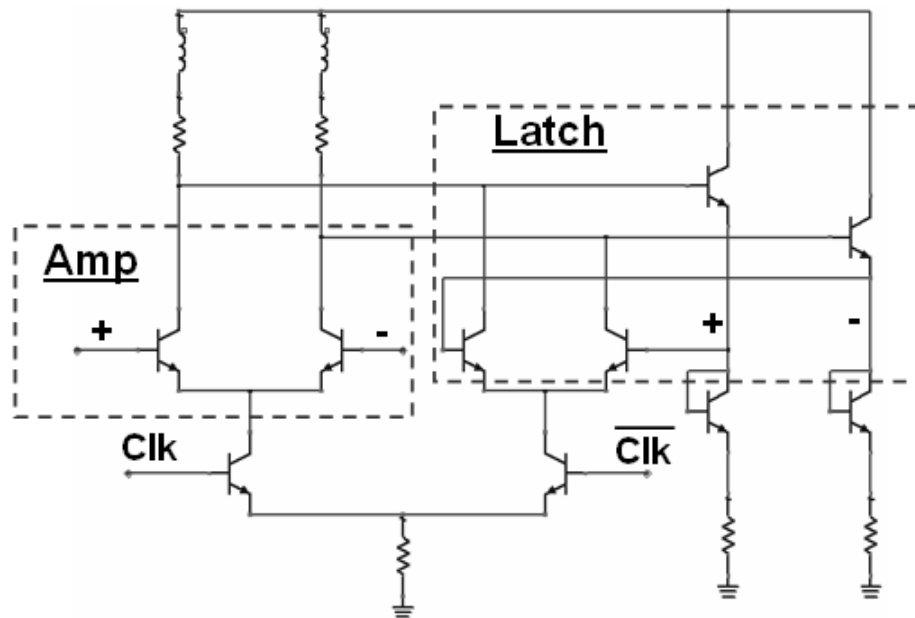


Fig. 2.19: Circuit implementation of static frequency divider latch (one half of core circuit).

The circuit, based on the UIUC SDD Type-II model, simulates nicely in an Agilent ADS transient simulation with sinusoidal or square clock inputs. It has no convergence issues, and simulates in less than a minute on a conventional 2.5 GHz PC.

The circuit was simulated from 50 GHz to 205 GHz, the maximum frequency at which it has the proper operation. Correct circuit operation and simulation convergence is seen at all frequencies in this range. The input (clk) and output voltage waveforms are shown for an input frequency of 205 GHz in Figure 2.20.

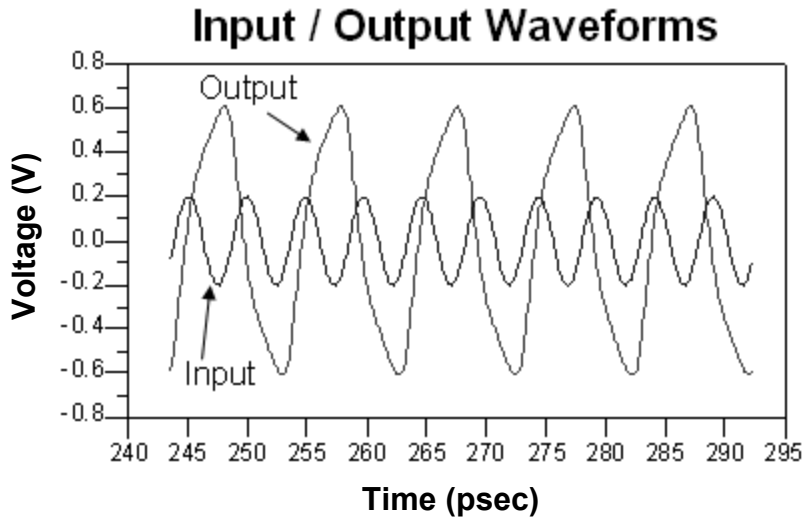


Fig. 2.20: Simulated input and output waveforms.

Parasitic interconnect capacitances are not taken into account in this simulation. Diva layout extractions carried out in Cadence indicates that line-to-line capacitance and line-to-ground capacitance would decrease the maximum operating frequency to 180 GHz.

3. TEST CIRCUIT FOR UIUC SDD2 / VBIC MODEL COMPARISON

3.1 – Objective

To truly evaluate the accuracy and capabilities of a large-signal model, a test circuit needs to be designed, simulated with the model, fabricated, and measured. Measured data can be compared to the simulation results to verify the accuracy of the model. The objective of this design is to generate a 32 GHz system clock for an electronic warfare band system on a chip (SOC) transceiver being developed in industry, both for Type-I SDD2 model validation and for use in the SOC. The preferred means of generating the system clock is to cascade a voltage controlled oscillator, operating at twice the desired output frequency, with a static frequency divider [16]. The oscillator generates the initial seed oscillation and drives the digital divider to produce a pseudo-square wave output at a frequency half that which is generated by the oscillator. An overview is given in Figure 3.1.

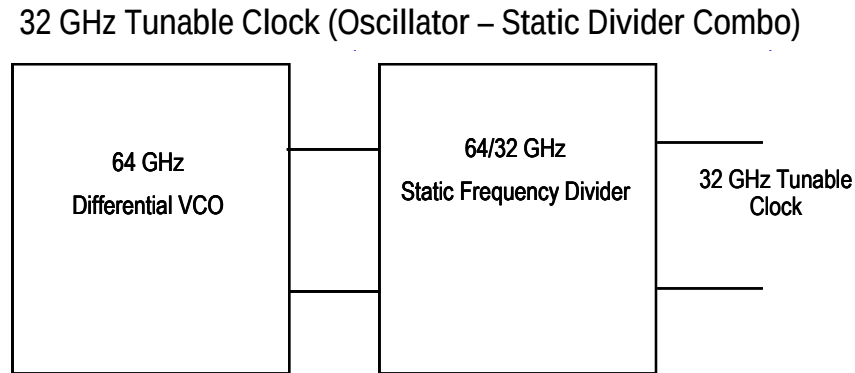


Fig. 3.1: Overview of the proposed system.

3.2 – Fundamentals of Sustained Electrical Oscillations

Electrical oscillators are energy restoring resonant cavities that can effectively store and regenerate energy at the resonant frequency, while not storing energy at frequencies that do not

coincide with the resonant modes of the cavity. An ideal cavity with no loss, once excited with energy at a frequency equal to the resonant frequency of the tank, would store this energy forever. This ideal situation, of course, is not physical or even desirable, as practical oscillators need to transfer energy to a load, which results in power being lost from the cavity. All cavities practical for use in integrated circuits have some form of loss (conductive, dielectric, or radiative) and therefore will not be able to hold an oscillation forever. Sustained oscillation is possible when a circuit is able to restore energy to the cavity to compensate for the energy that is lost. The energy must be restored in a manner such that it is delivered to the cavity in phase with the signal resonating in the cavity. Injection at another phase would disturb the oscillation and sum with the energy in the tank in a destructive manner to squelch oscillation. When viewed from a microwave perspective, this leads to the Barkhausen criteria presented in Figure 3.2 and Equations 3.1 and 3.2 [17].

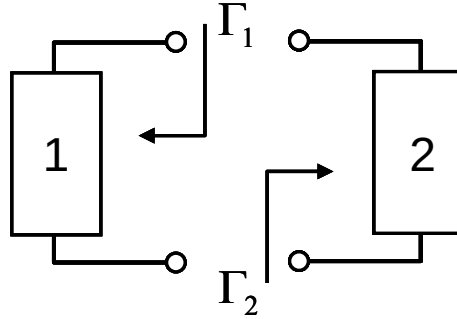


Fig. 3.2: Two one-port microwave representation of electrical oscillator.

$$|\Gamma_1 \Gamma_2| > 1 \quad (3.1)$$

$$\angle(\Gamma_1) + \angle(\Gamma_2) = 0 \quad (3.2)$$

By breaking the circuit into two networks, a sustained oscillation can be created when the product of the reflection coefficients from networks 1 and 2 is one. This makes intuitive sense in

that the round trip gain through the circuit is one. Energy goes into network 2, gets reflected to network 1, and then gets reflected back into network 2 at the same magnitude and phase which it initially had. However, to get an appreciable output power, the initial small-signal output reflection product should be much greater than one, to allow the magnitude of the oscillation to build up to a power level that, through gain compression of the active transistors, lowers the product of the reflection coefficient to one. The load should only have a moderate mismatch so that a significant amount of power can escape the output cavity. It is possible to generate a reflection coefficient with a magnitude greater than one with a properly terminated two-port bilateral active network, such as that shown in Figure 3.3. Equation 3.3 gives the output reflection coefficient (Γ_{OUT}) of the network for a given source match (Γ_S) and the S-parameters of the network. If the Rollet's stability factor (K) of the network is less than one (Equation 3.4), it is possible to find a source match that causes the output reflection coefficient to be greater than one in magnitude [18].

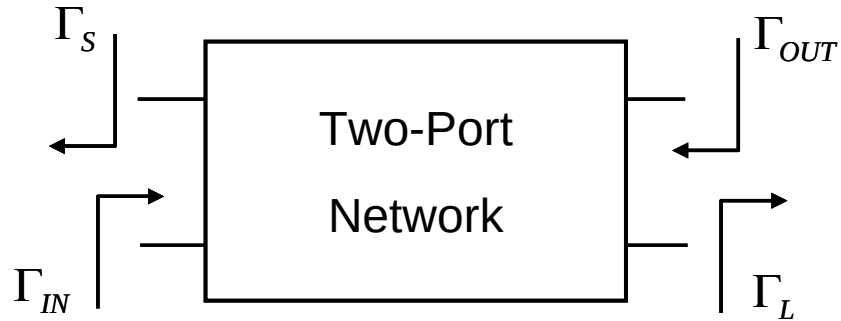


Fig. 3.3: Two-port microwave representation of bilateral device.

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 + S_{22}\Gamma_S} \quad (3.3)$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \quad (3.4)$$

In some cases a differential oscillator with two output oscillations 180 degrees apart is desired. To achieve this, a differential circuit configuration is used in which the common-mode oscillations are diminished, while the differential mode oscillations are enhanced. The key to achieving a proper differential oscillation is to realize that the output reflection coefficients for each of the modes of oscillation, in a properly designed circuit, will be different. The goal is to design terminating networks so the differential mode half-circuit is very unstable while keeping the common-mode half-circuit stable.

3.3 Oscillator Design

The oscillator is designed to operate at a center frequency of 64 GHz, and needs to be cascaded with a buffer stage to drive the static frequency divider. For best operation, the conventional emitter coupled logic static frequency divider requires a differential input. It was decided to design a differential oscillator to directly provide a differential signal to the divider, instead of trying to use a high-frequency balun to convert from single-ended to differential signaling inside of the divider. For the oscillator, a common emitter design is proposed in which the emitters of each oscillating transistor are capacitively tied together and further degenerated with a transmission line. Initial analysis and simulations show that capacitive degeneration will reduce that stability of the differential mode, enabling differential mode oscillations, while the transmission line will increase the stability of the common-mode, eliminating the possibility of common-mode oscillations. Diode connected devices will be connected to each base transmission line to serve as varactors so that the oscillations can be tuned. An initial schematic of the proposed oscillator design is shown in Figure 3.4.

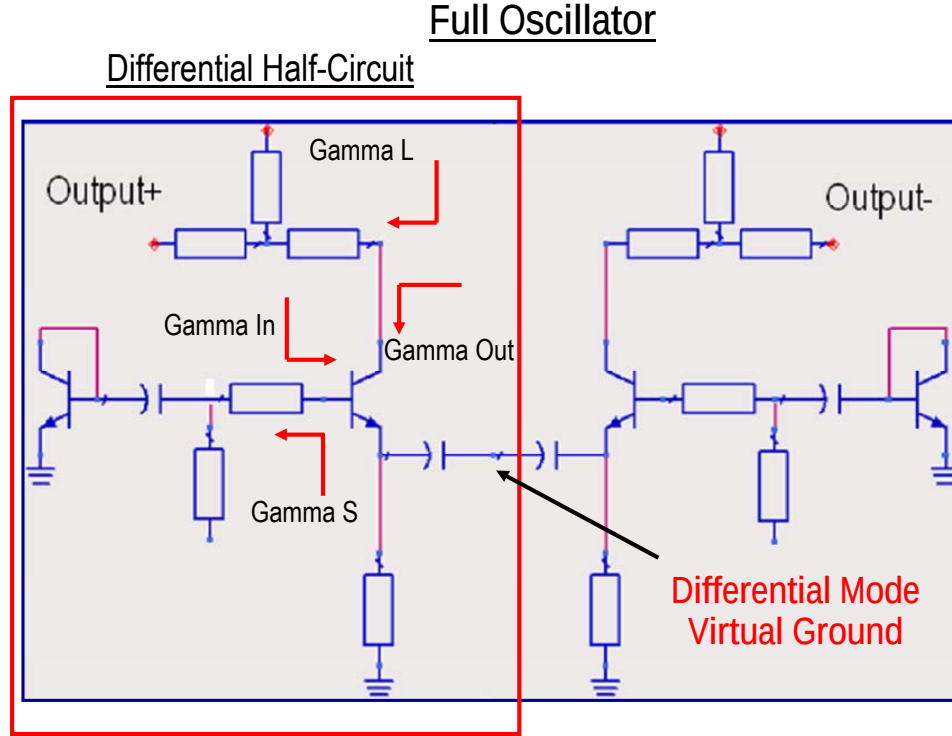


Fig. 3.4: Schematic showing basic reflection based differential oscillator topology.

For the $0.5 \times 5 \mu\text{m}^2$ Type-I DHBTs in the Teledyne process operating at moderate current levels around 10 mA, the stability of the devices increases when their emitters are terminated in short transmission lines whose lengths do not exceed 150 μm . This stabilization is due to the inductive degeneration seen by the transistors, which lowers the magnitude of their forward gain and S_{21} . Through small-signal stability analysis, it was determined that a 65 μm long emitter transmission line should keep the common-mode oscillations suppressed across all frequencies up to the f_{MAX} of the device. To cause an instable differential mode circuit, the virtual ground that appears at the line of symmetry in all differential circuits was leveraged so that the effective emitter degeneration would be different for differential and common-mode signals. By coupling the two half-circuits together with 0.23 pF capacitors, it is possible to alter the series feedback so Γ_{OUT} looks different depending on the mode of operation. These feedback capacitors are only

seen by differential mode oscillations and cause the transistors to become unstable when oscillating out of phase, thus promoting differential mode oscillations.

Once the transistors have been properly destabilized to promote differential mode oscillation, a resonant tank must be designed to resonate at the design frequency. As the transistor provides the energy restoration needed to overcome the losses in the tank, and therefore to produce a sustained oscillation, it must be strongly coupled to the resonant cavity. Typical cavities at lower frequencies consist of inductor-capacitor (LC) tanks. However, as there are no inductors provided in this technology and they would be lossy and have a relatively low self-resonance frequency, they are not used. The resonant tank is composed primarily of coplanar wave guide transmission lines, and the resonant frequency of the tank is selected by the use of single-stub matching networks at both the base and collector of the oscillating devices. To set the resonant frequency, the matching networks are designed so that the Barkhausen criteria are satisfied at the collector. In setting the frequency, the phase condition (Equation 3.2) is most important, since it determines what mode will resonate in the cavity.

Since, in this circuit, transmission lines are used to destabilize the network, store the energy of oscillation, and select the frequency, it is important that they be carefully characterized. In this work, it was chosen to forgo the use of analytic computer based transmission line models, and to develop models based on measured data. Pertinent equations for the extraction of the necessary transmission line parameters are shown in Equations 3.5 to 3.8 [19].

$$[ABCD]_{TL} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma d) & Z_0 \sinh(\gamma d) \\ Y_0 \sinh(\gamma d) & \cosh(\gamma d) \end{bmatrix} \quad (3.5)$$

$$Z_0 = \pm \sqrt{\frac{a_{12}}{a_{21}}} \quad (3.6)$$

$$\gamma = \alpha + j\beta = \frac{\cosh^{-1}(a_{11})}{d} = \frac{\ln(a_{11} \pm \sqrt{a_{11}^2 - 1})}{d} \quad (3.7)$$

$$Q_{TL} = \frac{\beta}{2\alpha} \quad (3.8)$$

S-parameter measurements of 500 μm long coplanar transmission lines with varying geometries were taken. Through converting the measurements to ABCD parameters and using Equations 3.5 to 3.8 above, the parameters of the transmission lines were extracted from measured data. From these extractions, the transmission line quality factor (Q_{TL}), the ratio of the energy storage to energy loss of each transmission line, was determined. As the oscillator's resonating tank is primarily composed of these transmission lines, it is extremely important that Q_{TL} is maximized in order to increase the overall Q of the resonator to maximize the oscillator's stability. For this reason, a 73 Ω coplanar waveguide transmission line geometry with a transmission line quality factor of 18.9 at 50 GHz was chosen over a typical 50 Ω coplanar waveguide (CPW) geometry which has a Q_{TL} of only 12.3 at 50 GHz. Verification of the transmission line model, a comparison of the measured data and the simulation results over the frequency range from 1 to 50 GHz, is given in Figure 3.5.

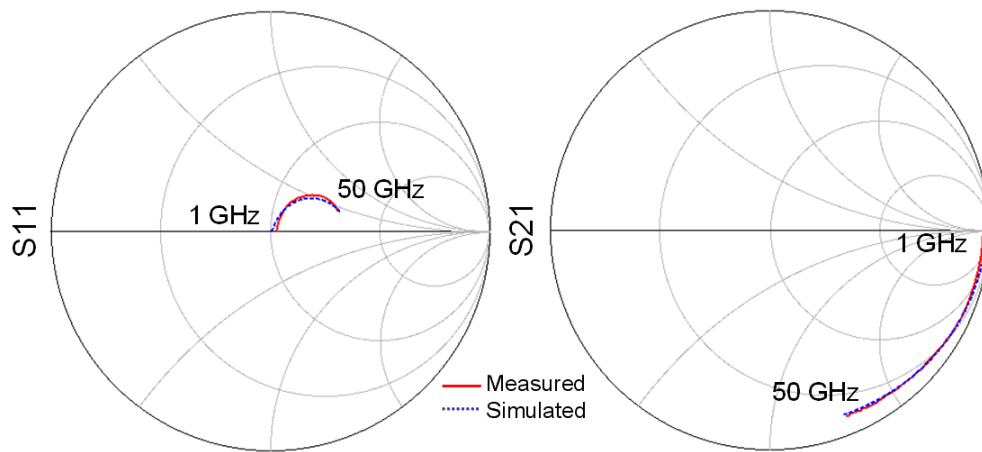


Fig. 3.5: S-parameter comparison of the extracted transmission line model to the measured characteristics of a 500 μm line 73 Ω transmission line from 1 to 50 GHz.

An idealized circuit that is similar to that shown in Figure 3.4 is designed to test the validity of this design scheme and emitter termination choice. This design is configured such that both the base and collector are driving $50\ \Omega$ loads. The design is simulated in harmonic balance and the output is shown in Figure 3.6.

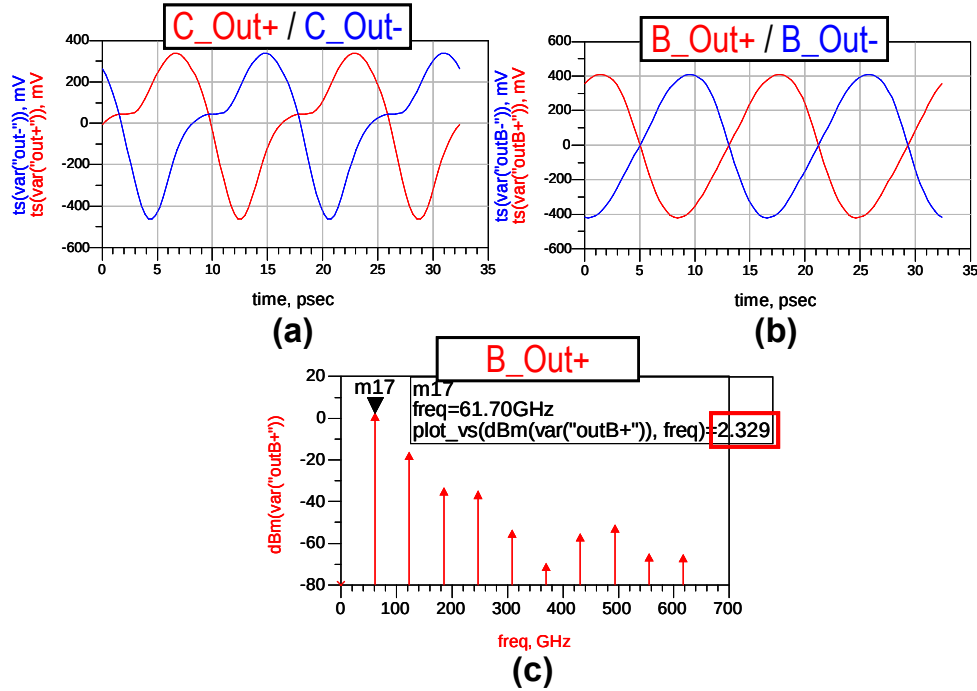


Fig. 3.6: Simulated harmonic balance output of the circuit in Figure 3.4 using the UIUC SDD2 model with (a) the voltage waveforms at the collector output, (b) the voltage waveforms at the base output, and (c) the output spectrum of the base.

The simulated oscillator core is designed to test the validity of the chosen oscillator topology, and it is therefore highly idealized: it drives $50\ \Omega$ loads and has ideal DC and AC current blocking elements. The transmission line models used to design the stub matching networks are based on the measured characteristics of a $500\ \mu\text{m}$ coplanar waveguide transmission line, previously discussed, whose dimensions are identical to the waveguides used in this circuit. The transmission line models account for the fact that the measured characteristic

impedance is not $50\ \Omega$, and for the per unit length loss seen in the transmission line. These transmission line models are used throughout the remainder of the design.

This design is simulated with both the VBIC model supplied by TSC and the UIUC SDD2 model and is found to have differential oscillations around 62 GHz with a single-ended output power of ~ 2.3 dBm from the base termination. The output from the base is found to be much more linear and to have approximately 2 dB more output power than the oscillation from the collector. This result is observed for each device model. Though unexpected, this result can be explained. Figure 3.7 shows a small-signal representation of the oscillator differential half-circuit. The device's output current source is driving a load that is the parallel combination of the output load and the feedback impedance presented to the output through the base-collector capacitance (C_{BC}). The output signal is therefore delivered both to $Z_{OUT,C}$, the collector output impedance, and through C_{BC} to $Z_{OUT,B}$, the base output impedances (both collector and base impedances are labeled as “output impedances” since the oscillating transistor is operating as a source and happens to deliver power to two loads). As this oscillator is being driven into compression, there are multiple harmonics of the oscillation frequency manifesting themselves in the output collector current. At node B we get a filtering effect, with the higher order harmonics seeing a reduced impedance path to ground through C_{BE} and C_E , which serves to reduce the harmonic powers seen at $Z_{OUT,B}$. The filtering of the harmonics at node C is reduced due to the series combination of C_{BC} and C_{BE} resulting in a higher impedance path to ground, which enables the harmonics to show up more pronouncedly in the $Z_{OUT,C}$ output. In matching this circuit so that it would fulfill the oscillating conditions, the magnitude of $Z_{OUT,B}$ is larger than that of $Z_{OUT,C}$, resulting in a higher fundamental output power at the base. Given that the base

output of the oscillator has higher power and linearity, a complete design is developed that takes the oscillator output from the base.

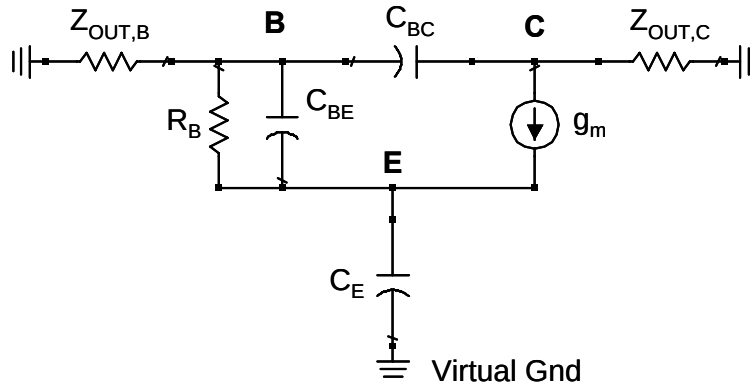


Fig. 3.7: Small-signal representation of oscillator half-circuit under differential conditions.

The idealized oscillator core is updated to incorporate physical biasing and an output buffer to drive the frequency divider. The differential mode series feedback capacitors of the previous design were removed and replaced with a capacitively terminate transmission line. Ideally, assuming a lossless transmission line, this substitution would have the same electrical characteristics as the previous differential mode feedback, but it would serve to physically separate the emitter transmission lines so as to reduce coupling. Device biasing is accomplished by feeding DC levels through shunt matching stubs and capacitively loaded quarter-wave biasing stubs. The configurations of the base networks, emitter networks, and initial oscillator buffer stage are shown in Figure 3.8, and the collector matching and varactor networks are shown in Figure 3.9.

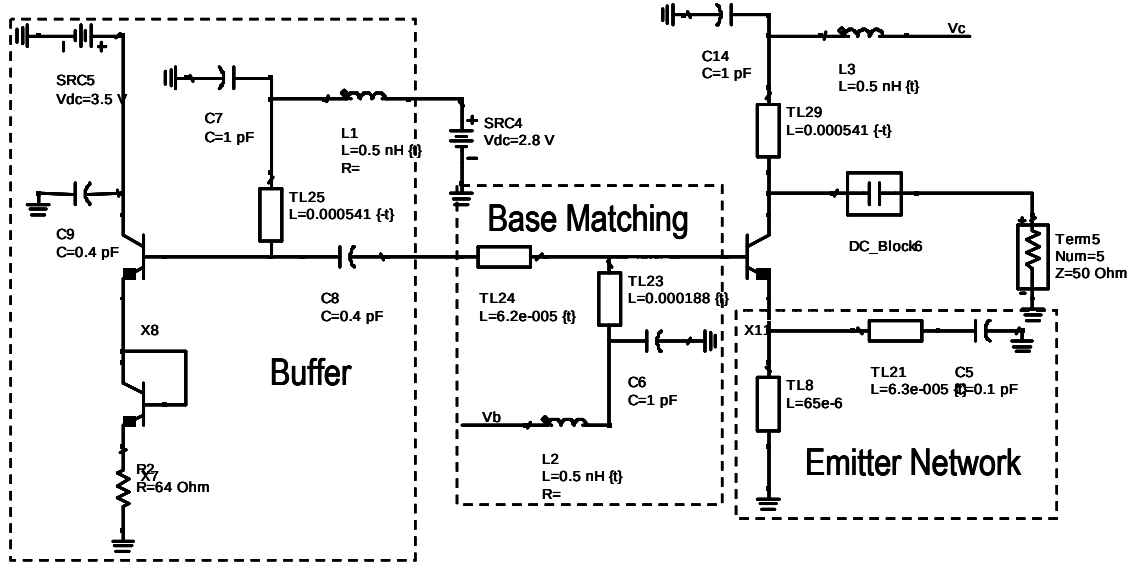


Fig. 3.8: Differential oscillator half-circuit showing emitter, base, and buffer networks.

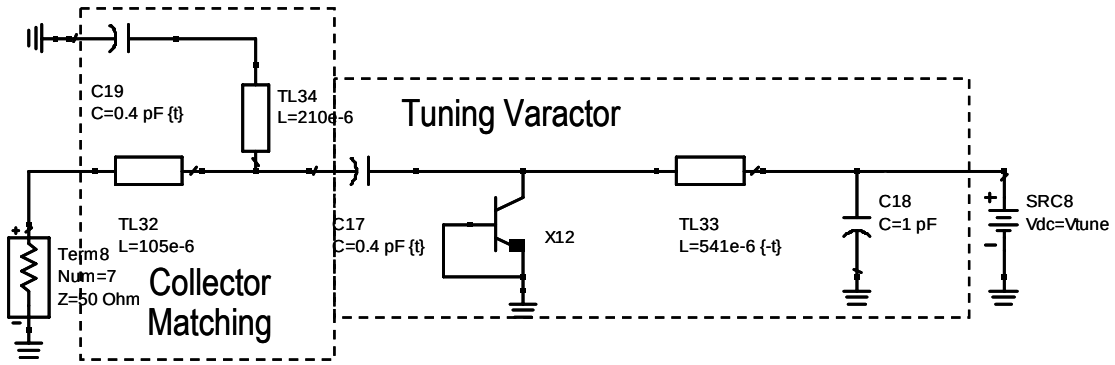


Fig. 3.9: Differential oscillator half-circuit showing collector and varactor networks.

Both the oscillator buffer stage and the varactor are capacitively coupled to the oscillator so that the biases for each can be controlled independently of the oscillator. The buffer is designed to give a low impedance output and set the input bias of the frequency divider. The base-collector diode of a $0.5 \times 5 \mu\text{m}^2$ device is used as the varactor. The bias to the buffer and the tuning signal to the varactor are delivered through quarter-wavelength stubs, so as not to present a load to the circuit and disturb the matching.

3.4 – Static Frequency Divider Design

A static frequency divider is essentially a positive edge triggered flip-flop with the negative output fed back to the input. This feedback results in a change in the output level each time a positive edge is seen, effectively reducing the input frequency by a factor of two. To realize this functionality at high-frequency, very fast logic must be employed. This design is similar to the simulated Type-II divider in Section 2.24 in that emitter coupled logic (ECL) is used to create the circuit. An overview of the design is shown in Figure 3.10(a) and 3.10(b). In ECL, a D-latch can be thought of as having two stages, an amplifier and a regenerative latch, each of which is controlled by opposite clock signals. When the amplifier turns on, it amplifies the differential signal it sees across its inputs and sends its value to the latch and the output. When the amplifier turns off, the regenerative latch turns on and maintains the logic level from the amplifier. The latch is effectively transparent when the amplifying signal is positive, and it stores the input value when the latch signal is positive. Figure 3.10(b) shows the topology of the latch, and Figure 3.10(a) details its use in the overall divider.

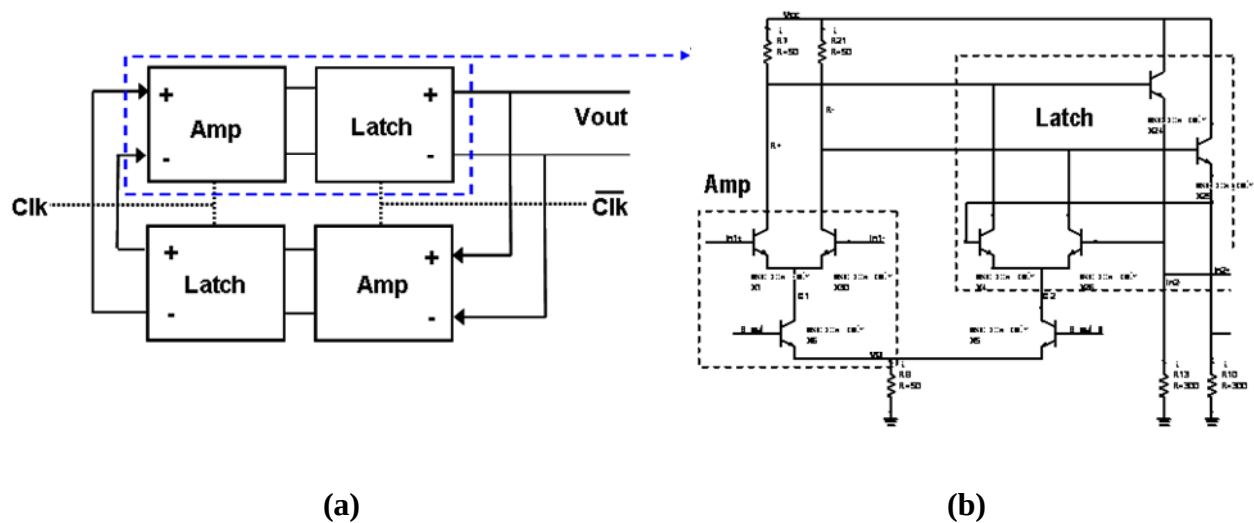


Fig. 3.10: (a) Static frequency divider block diagram, (b) topology of ECL D-latch used in static frequency divider.

The key to achieving high speeds in emitter coupled logic designs is always keeping the transistors biased in the forward-active mode of operation. In this mode of operation, the emitter-base junction is forward biased, and the base-collector junction is reversed biased. If the base-collector junction is kept reversed biased, the output capacitance of the device remains small and the circuit charging time is reduced. It is for this reason that an ECL topology is preferred over a current mode logic (CML) topology where there is no final output emitter follower stage. The emitter follower stages help assure that the core transistors of the regenerative latch will remain in the forward-active mode by keeping the base-collector junction at a reverse bias approximately equal to the base-emitter voltage of the emitter followers.

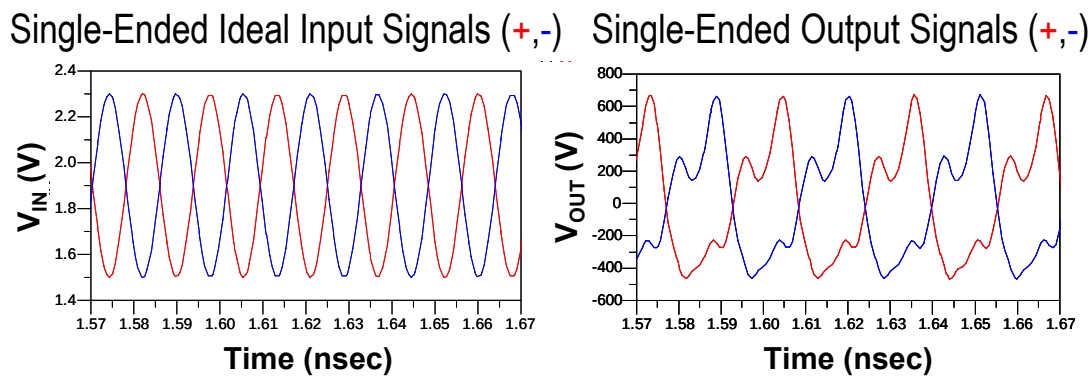


Fig. 3.11: Single-ended input and output divider signals.

The input and output signals of the static frequency divider are shown in Figure 3.11. In this simulation, the input is a differential sinusoid at 64 GHz and the output is a more complex waveform at 32 GHz. The sharp peak in the output waveform comes from the regenerative latch latching the output value, and the dip immediately prior to the peak is the result of the amplifier being turned off and the regenerative latch being turned on. The shape of the output waveform is characteristic of static frequency dividers.

3.5 – Differential Half-Circuit Impedance Analysis

Both the original oscillator (Figure 3.12) and the divider design operate well independently. When cascaded, however, so that the oscillator feeds the divider, the operation of both circuits is disturbed, such that the output from the oscillator does not properly drive the divider. These problems stem from a strong mismatch in impedances. In fact, the output impedance the oscillator presents to the divider is negative. This necessitated the redesign of the inter-oscillator-divider buffer, so that the divider is driven with the correct impedance.

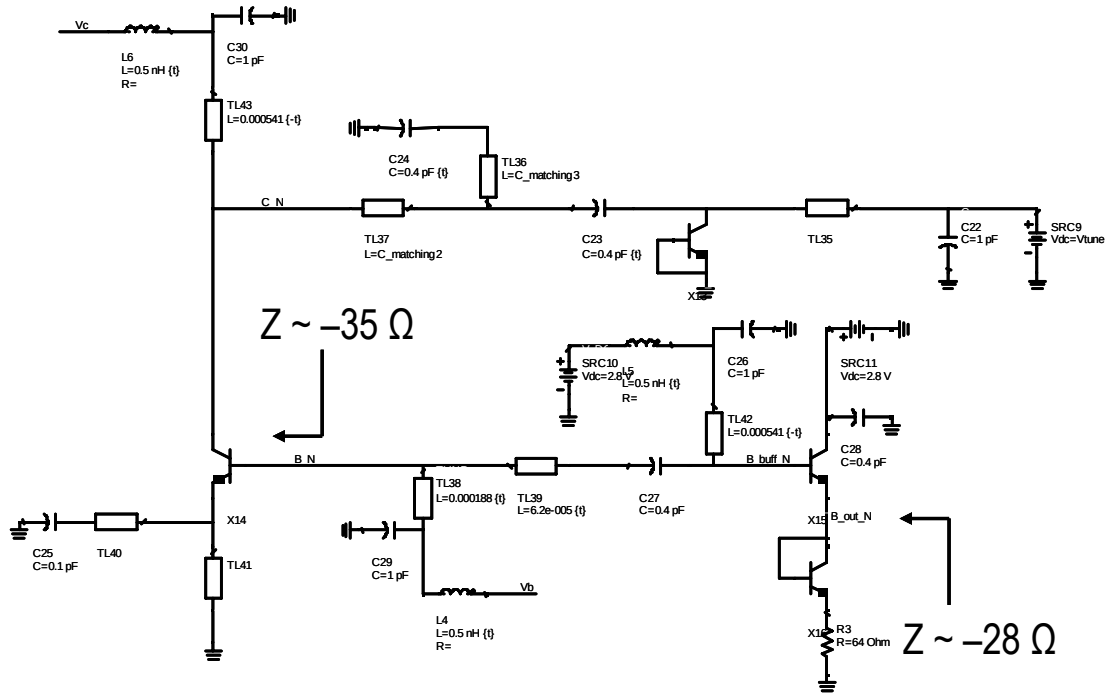


Fig. 3.12: Original oscillator and emitter follower buffer with intrinsic and extrinsic node impedance labeled. The output impedance of the oscillator is -28Ω , making this configuration incapable of driving the divider.

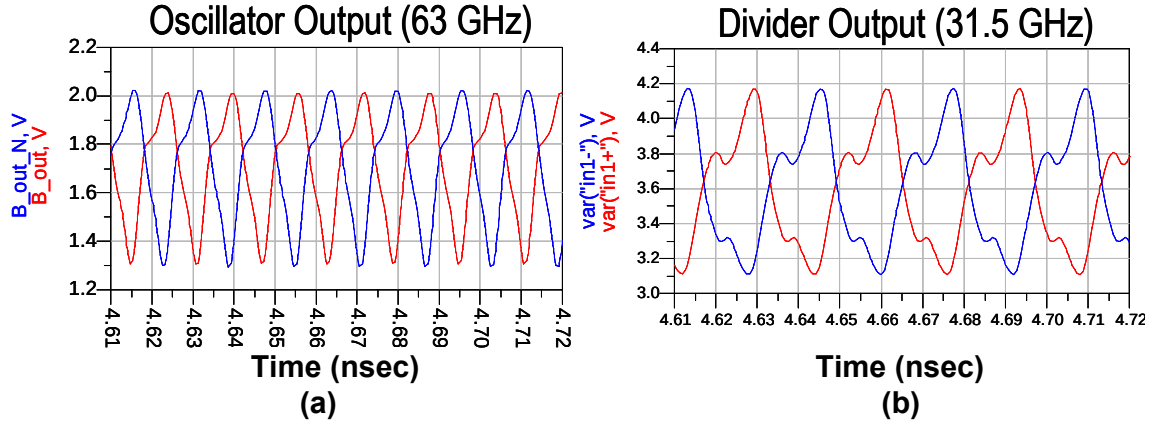


Fig. 3.14: (a) Plots of the voltage signals at the node between the common-emitter stage and the divider and (b) plots of the divider's output voltage showing proper oscillator-divider operation.

A final output buffer is included between the divider and output. The design for this buffer was received from British Aerospace Enterprise Systems (BAE) and was modified to work with this circuit. The buffer, shown in Figure 3.15, is essentially a differential cascode topology that has an output resistance of approximately $50 \, \Omega$ and is resistively degenerated to provide a unity voltage gain. The circuit consists of an initial emitter follower stage, a series resistance to help isolate the cascode section from the EFs, the differential cascode stage, and the biasing network for the common base transistors.

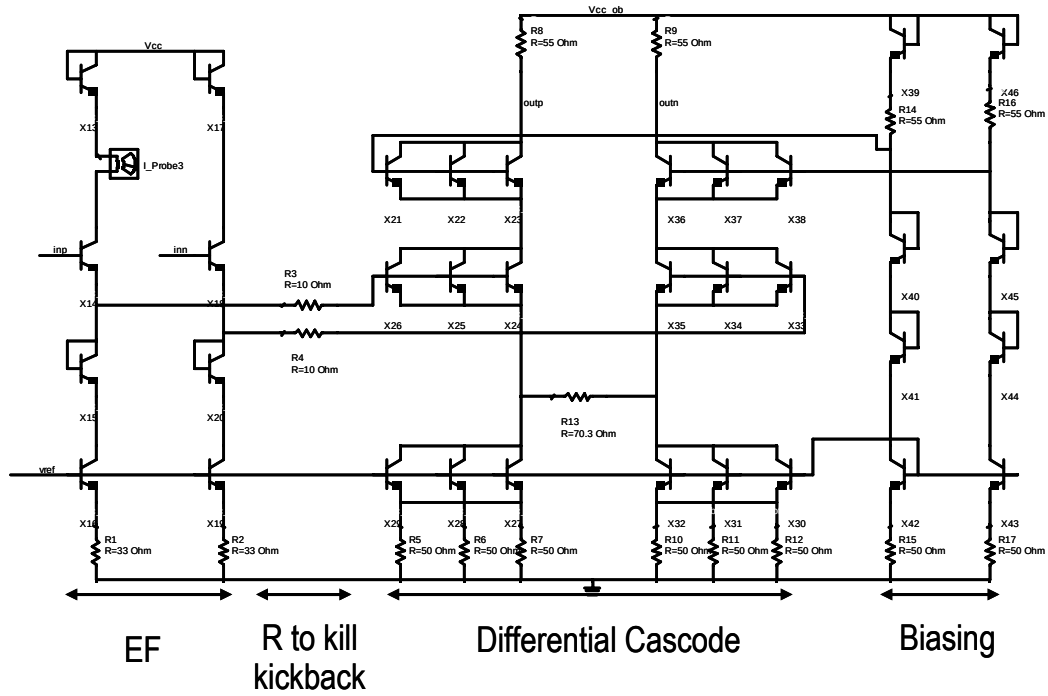


Fig. 3.15: Differential output buffer received from BAE and altered to work with this design.

To help facilitate the testing of this circuit, an additional divider is added to the circuit, resulting in a 16 GHz signal. A block diagram overview of the final design and final simulations are shown in Figure 3.16.

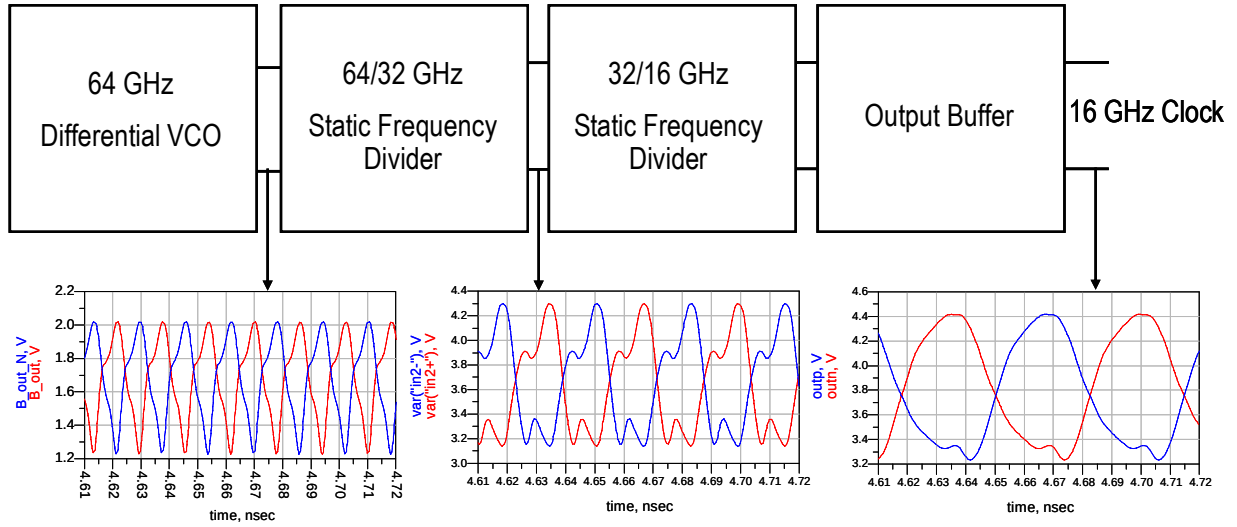


Fig. 3.16: Block diagram overview of the entire circuit and node voltages simulated at different points in the circuit. The frequency division can clearly be seen in the plots of output voltage.

3.6 – Circuit Layout and Measurement

The individual circuit components (divider, buffer, and oscillator) were laid out individually and then incorporated into one final circuit. The distributed oscillator's topology was slightly modified from that previously shown in order to reduce the complexity and the unwanted electromagnetic coupling between the transmission line terminations at the base and collector terminals of the oscillating transistor (Figure 3.17). The modification consisted of a transmission line stub, which was previously attached to the base, being removed and added beside the oscillator buffer DC blocking capacitor. It presents the same impedance to the device, but allows for a better physical layout.

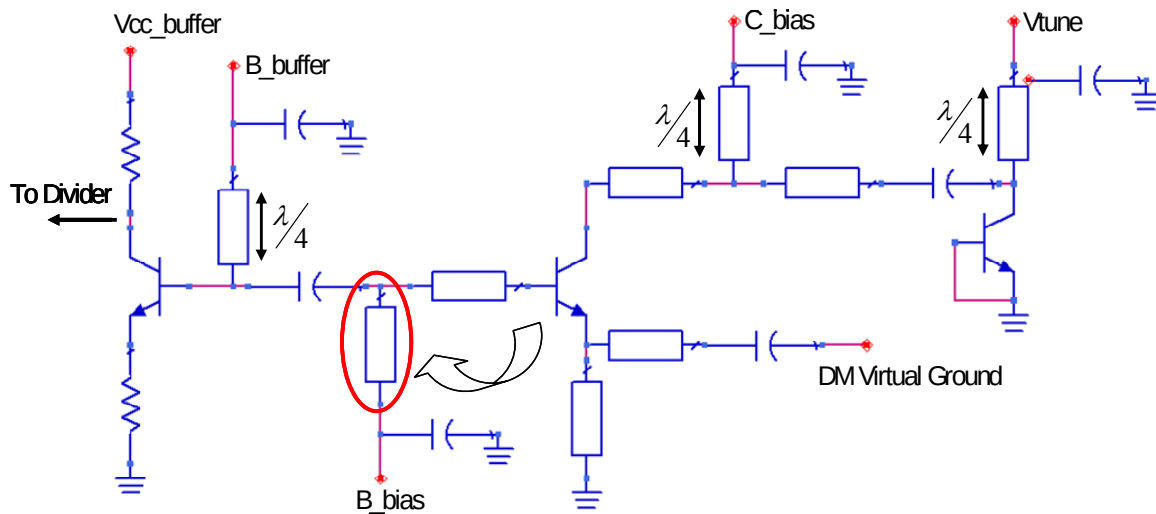


Fig. 3.17: Modified differential half-circuit topology.

The circuit is taped out and fabricated in the Teledyne Scientific 0.5 micron Type-I DHBT process. A micrograph of the entire circuit is shown in Figure 3.18 with overlaid notation indicating the individual components in the circuit. As this is a differential circuit, it is laid out symmetrically along a horizontal line passing through the center of the circuit. The circuit has a total of 132 $0.5 \times 5 \mu\text{m}^2$ Type-I DHBTs, an area of $1350 \times 1400 \mu\text{m}^2$ and requires DC rail voltages of 3.8 V, 4.5 V, and 5 V. In addition to these supplies, there are pads for tuning voltages to adjust the different internal bias levels of the circuit. All of the tuning pads can be left floating; ideally no bias would need to be applied for proper circuit operation. The DC bias and tuning pads are spaced so that they can be used with both $125 \mu\text{m}$ and $140 \mu\text{m}$ pitch probes. The output signal is single-ended and capacitively coupled to the output. The negative output is capacitively coupled to an on-chip 50Ω termination. Standard $150 \mu\text{m}$ pitch RF pads are used for the output signal.

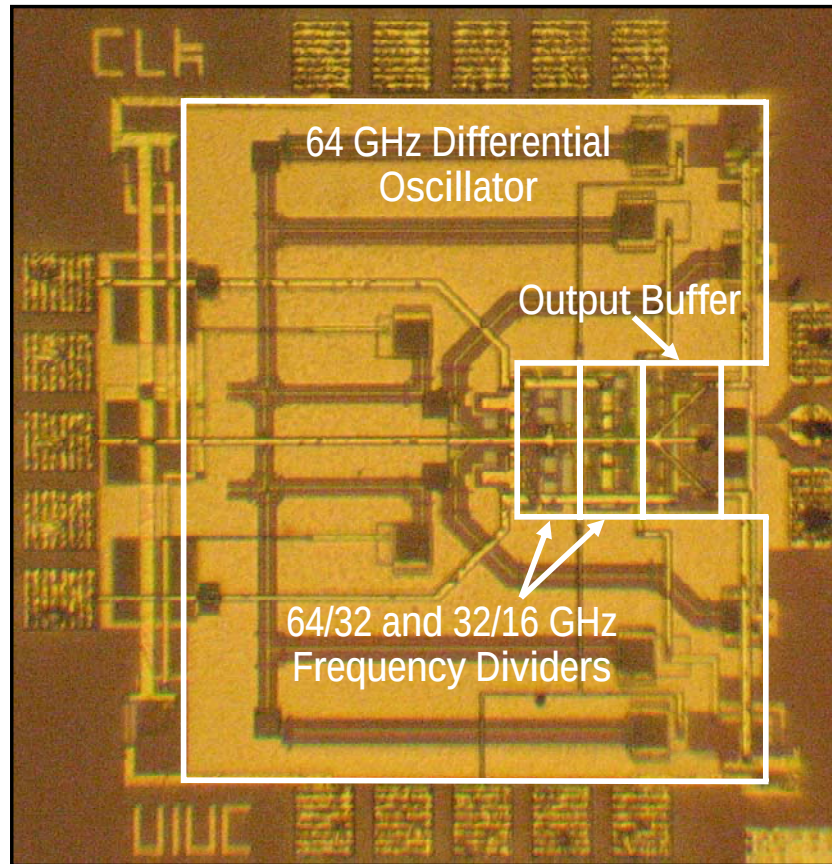


Fig. 3.18: Micrograph of completed clock generator circuit with additional divider to give 16 GHz output.

The fabricated circuit is measured through on-wafer probing using AC grounded DC probes and 50 GHz bandwidth RF probes. Biases were applied to the circuit with an HP 4142B precision DC source monitor unit (SMU) and the output spectrum was measured with a 50 GHz bandwidth HP 8565E spectrum analyzer. The measured output spectrum is compared with the simulated output from both the UIUC SDD2 and foundry supplied VBIC model and shown in Figure 3.19. The measured data is “uncorrected” in the sense that the output loss of the RF probe and cable have not been factored out of the measurement, giving the disparity in amplitude between the measured and simulated data.

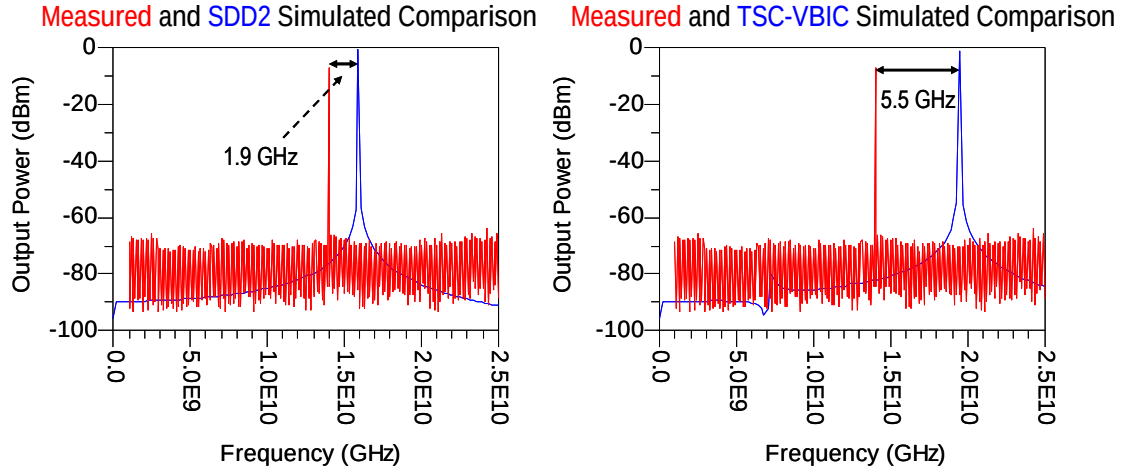


Fig. 3.19: Measured and modeled circuit output comparison showing that though not perfectly predicting the output characteristics of the clock generator, the SDD2 model gives a much closer estimate of the final output than the foundry provided VBIC model.

The measured output frequency is lower than that which was projected by either the UIUC SDD2 model or the VBIC model distributed by the foundry, which is likely due to an incomplete extraction of circuit parasitics during circuit simulation. The SDD2 model, however, gives a much better estimate of the oscillation frequency than does the VBIC model, only having 35% of the error shown in the VBIC model. The oscillator had no measured output tuning range, likely due to an under-designing of the varactor tuning network. Being differential and using distributed biasing and matching networks, it also consumes a significant amount of power and area. This circuit does however show that the UIUC SDD2 model provides a significant improvement over the VBIC model for this 0.5 μm Type-I DHBT technology; however, for the reasons noted above, the design was updated.

4. TUNABLE CLOCK GENERATOR DESIGN, LAYOUT, AND MEASUREMENT

4.1 – Objective

A second clock generating circuit is designed specifically to address some issues with the design detailed in Section 3.1, namely its size and lack of tuning. This circuit is not simply an updated version of the previous circuit, but a complete redesign, implementing a different circuit architecture and oscillator design. Unfortunately, as these designs are being implemented in an experimental and continually evolving device technology, the epitaxial layer structure of the active devices was changed between the previous design and the design presently documented. No samples of these devices could be obtained for UIUC SDD2 model extraction, so the design of this circuit is carried out with an updated factory supplied VBIC model. A simplified overview of the entire circuit is shown in Figure 4.1. The circuit consists of four stages: a tunable single-ended oscillator, a narrow-band active balun, a static frequency divider, and a cascaded differential output buffer. Each of these stages is described in detail in the following sections. This tunable oscillator is shown to have an output power of 2.5 dBm over a 2.4 GHz tuning range and a free-running phase noise of -89 at a 1 MHz offset, while being able to generate multiple clock shapes.

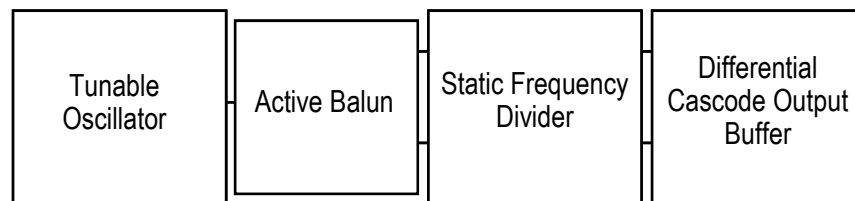


Fig. 4.1: Overview of entire circuit in terms of its sub-circuit functional components.

4.2 – Oscillator / Active Balun

A tunable common-base reflection oscillator is designed to oscillate at 64 GHz and is capacitively coupled to a narrow band active balun which generates a differential oscillation. A simplified schematic of the circuit, neglecting the biasing network, is shown in Figure 4.2.

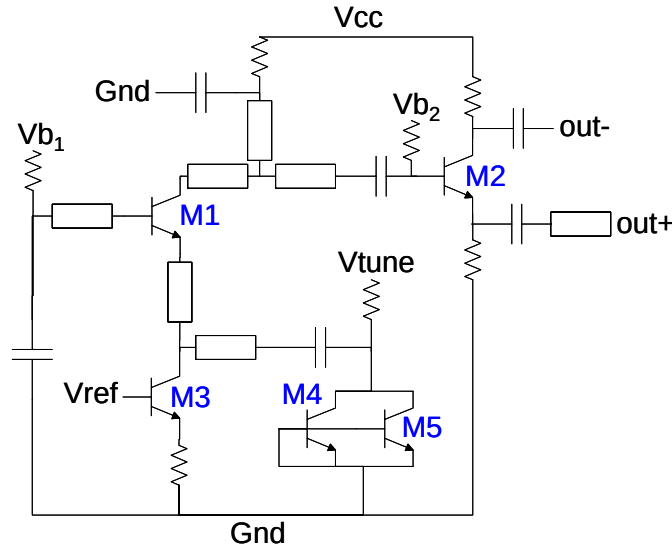


Fig. 4.2: Common-base oscillator with tuning network that is capacitively coupled to narrow band active balun (M2 network). The bias network is not shown.

The composite oscillator-active balun consists of four main components: the unstable active element and the associated energy storing transmission line tank network (M1 and transmission lines), a capacitively coupled tuning network (M4 and M5), the bias controlling device (M3), and the active balun network (M2). The primary concern in this design, as in any good oscillator design, is to generate a stable and sustained oscillation. M1 must therefore be made unstable at the desired oscillation frequency so that it can compensate for the energy lost in the tank at this frequency. The oscillating common-base configured transistor, M1, is made unstable through the addition of a length of transmission line between its base and the AC ground. The length of the transmission line is optimized in order to minimize the Rollett

stability factor of the resulting base-degenerated common-base two-port network [18]. A low bias current of 3.6 mA was chosen for this circuit, since at this bias the transistor could be made sufficiently unstable while only injecting a low level of noise into the tank circuit. To aid in the discussion of the design of the common-base amplifier shown in Figure 4.2 above, Figure 4.3 gives a simplified view of the oscillator/balun network from which the design technique can be more easily discussed.

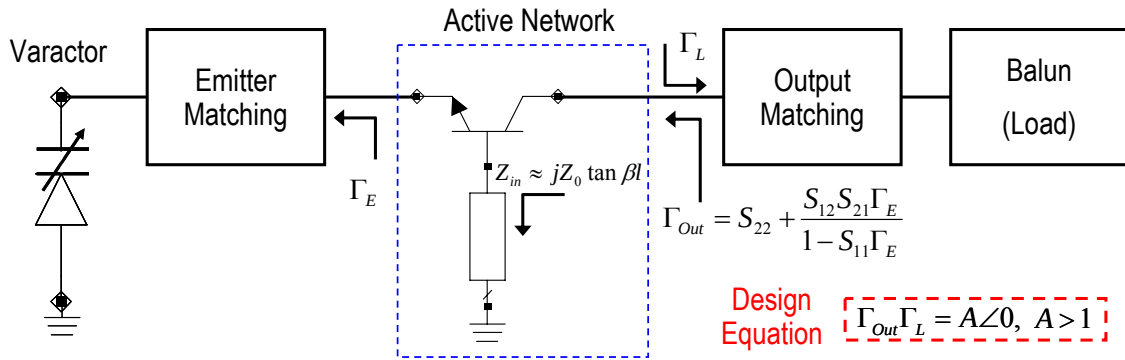


Fig. 4.3: Overview of common-base reflection oscillator design.

Once the circuit configuration is chosen, the design of this circuit can be broken down into four steps. (1) The first is the choice of an optimal bias for the oscillating transistor. For optimum performance, the device is to be biased at a highly linear, yet low current bias. Having a low current will lead to less noise being injected into the resonant cavity and a lower power dissipation, while increased linearity will allow for a larger oscillation magnitude to build up before the fundamental tone of the device is harmonically compressed. (2) Once the bias of the device is set, a proper base termination must be designed to maximize the instabilities of the network. In this design a coplanar waveguide transmission line is used to destabilize the circuit. (3) After destabilizing the active network, an emitter matching network must be designed to present an impedance to the emitter that will maximize the reflection coefficient seen at the

collector of the active device. (4) The output matching network is then designed to couple the oscillation to the balun load, and to set the accumulated closed-loop phase delay to 360 degrees at the design frequency. Single-stub matching networks are designed at both the emitter and collector terminals to create a tank that is resonant at the desired frequency and to maximize the power that is delivered to the active balun. The base-collector diodes of two HBTs are used to create a tuning varactor network which is capacitively coupled to the emitter transmission line to provide a tuning of the oscillation frequency.

A narrow band active balun is coupled to the output of the oscillator to give the single-ended to differential signal conversion that is needed in order to correctly drive the static frequency divider. The conversion is achieved by taking the in-phase output from the emitter of M2 and taking the out of phase from the collector. As the output impedance at the collector is different than that of the emitter, the emitter and collector load resistors have to be tuned so as to give outputs with identical magnitudes. The phase imbalance resulting from the difference in base-emitter and base-collector capacitance is compensated by adding an additional length of transmission line to the emitter output.

4.3 – Static Frequency Divider

As previously discussed in Section 3.1.4, the static frequency divider is a positive edge triggered flip-flop in which the output is inverted and fed back to its input. The feedback results in a change in the output level each time a positive edge is seen at the input, effectively reducing the input frequency by a factor of two. To realize this functionality at high-frequency, emitter coupled logic (ECL) is used in this design. An overview of the design is shown in Figure 4.4(a) and 4.4(b). In ECL, a D-latch can be thought of as having two stages: an amplifier and a

regenerative latch, each of which is controlled by an opposite clock signal. When the amplifier turns on, it amplifies the differential signal it sees across its inputs and sends its value to the latch and the output. When the amplifier turns off, the regenerative latch turns on and maintains the logic level from the amplifier. The latch is effectively transparent when the amplifying signal is positive, and it stores the input value when the latch signal is positive.

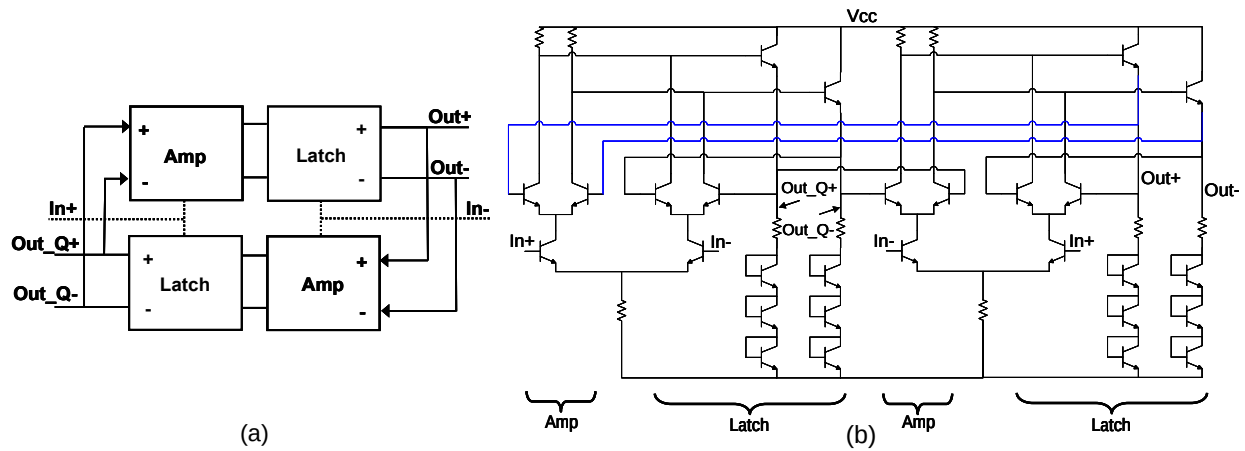


Fig. 4.4: (a) Symbolic high-level overview of static frequency divider operation, (b) static frequency divider circuit topology.

Besides simply being a means to provide a pseudo-square-wave clock, the static frequency divider can be used to generate quadrature clock signals. Signals taken from Out_Q+ and Out_Q- will be 90 degrees out of phase with the signals taken from Out+ and Out-. This quadrature relation between the signals is due to the fact that the quadrature output (Out_Q) changes levels on the rising edge of In+ while the standard output changes levels on the rising edge of In-. Figure 4.5 shows the simulated quadrature output of the circuit in Figure 4.4.

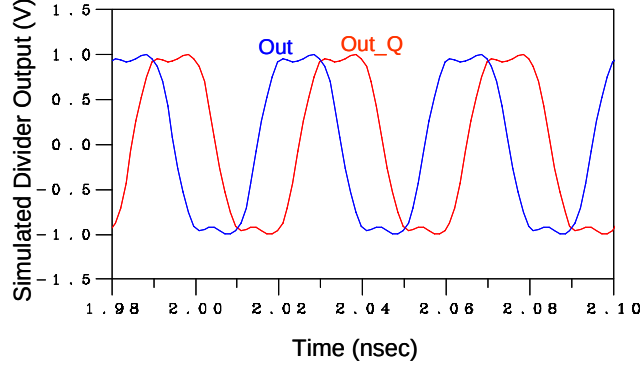


Fig. 4.5: 50 GHz simulation of static frequency divider showing quadrature output clock signals.

4.4 – Differential Output Buffer

An emitter-follower driven differential cascode amplifier, similar to that described in Section 3.6, is used to drive the $50\ \Omega$ RF output load, while presenting a high impedance to the frequency divider. The emitter followers are resistively coupled to the differential amplifier to increase the stability of the stage.

4.5 – Measurement Results

Figure 4.6 shows a micrograph of the fabricated clock generator as it was laid out for on-wafer testing. The circuit is fabricated in the Teledyne $0.5\ \mu\text{m}$ InP Type-I DHBT process. At optimum current, this technology has an f_T/f_{MAX} of 300/280 GHz. The entire die area, considering both the DC and RF pads together with the six on-wafer decoupling capacitors, totals $1.2\ \text{mm}^2$. All measurements were taken on-wafer at the ambient room temperature. The output frequency spectrums were measured with an Agilent 8565E spectrum analyzer.

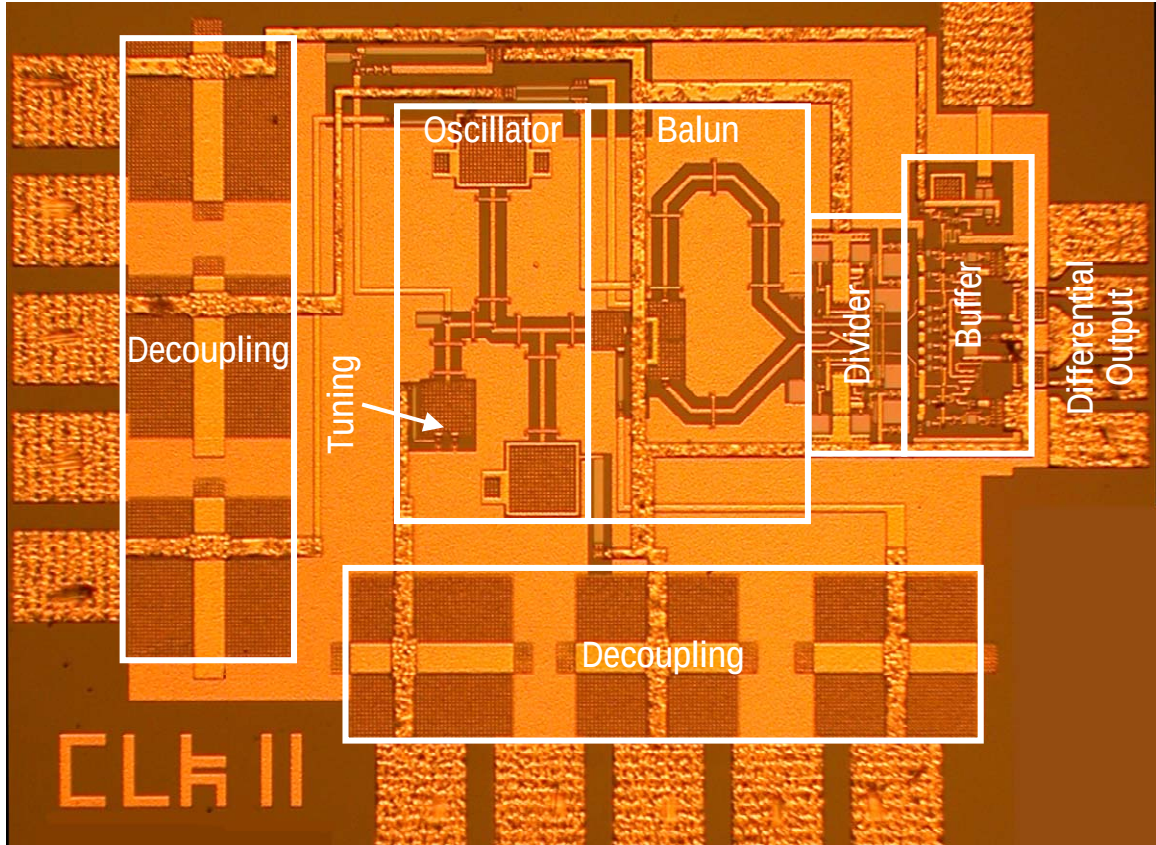


Fig. 4.6: Micrograph of fabricated millimeter-wave clock circuit.

Single-ended frequency spectrum measurements were taken on the overall clock circuit with one of the differential outputs terminated in $50\ \Omega$. The clock is measured to have a single-ended output power of 0.6 dBm at an un-tuned oscillation frequency of 26.7 GHz, giving a total differential output oscillation of 3.6 dBm, and a fundamental oscillation frequency of 53.4 GHz. The circuit was designed for 64 GHz. This significant output frequency discrepancy is attributed to unaccounted parasitics in the layout and the use of questionable foundry provided active device models at high operating frequencies. A maximum output tuning range of 1.2 GHz is measured for applied tuning voltages from $-0.4\ \text{V}$ to $2\ \text{V}$ with a maximum $\Delta f/\Delta V_{\text{tune}}$ ratio of 2.3 GHz/V for the frequency divided clock output, indicating a tuning range of 2.4 GHz and a

maximum $\Delta f/\Delta V_{\text{tune}}$ ratio of 4.6 GHz/V for the fundamental distributed oscillator. Tuning characteristics are shown in Figure 4.7.

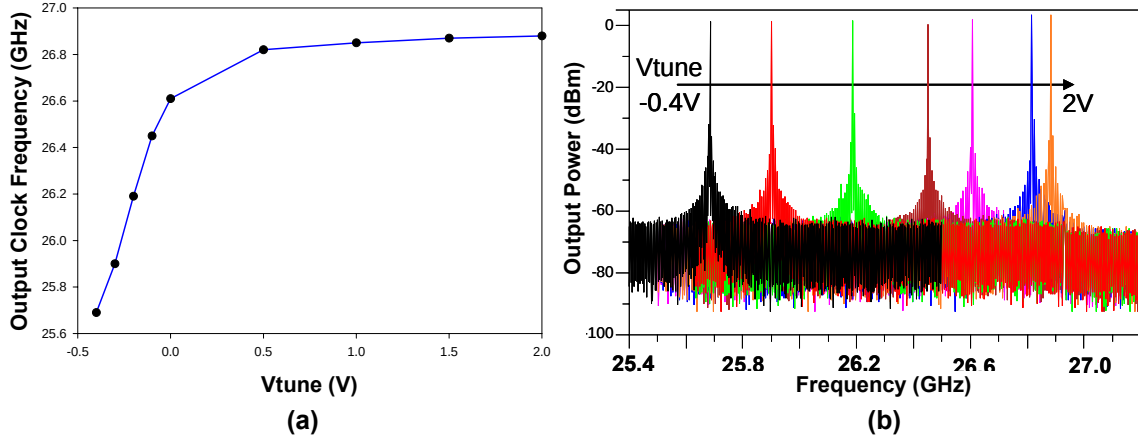


Fig. 4.7: (a) The measured output clock frequency vs. tuning voltage and (b) the measured output spectrum as the tuning voltage is swept.

Single-ended measurements were taken on a stand-alone oscillator-active balun circuit, equivalent to that shown in Figure 4.2 with one output terminated in $50\ \Omega$, in order to directly measure the output power and phase-noise of the fundamental oscillator. The fundamental oscillator has a single-ended output power of $-0.5\ \text{dBm}$ for a total output power of $2.5\ \text{dBm}$. The oscillator has a single-ended phase noise of less than $-89\ \text{dBc/Hz}$ at a $1\ \text{MHz}$ offset. A spectral measurement of the fundamental oscillator is shown in Figure 4.8.

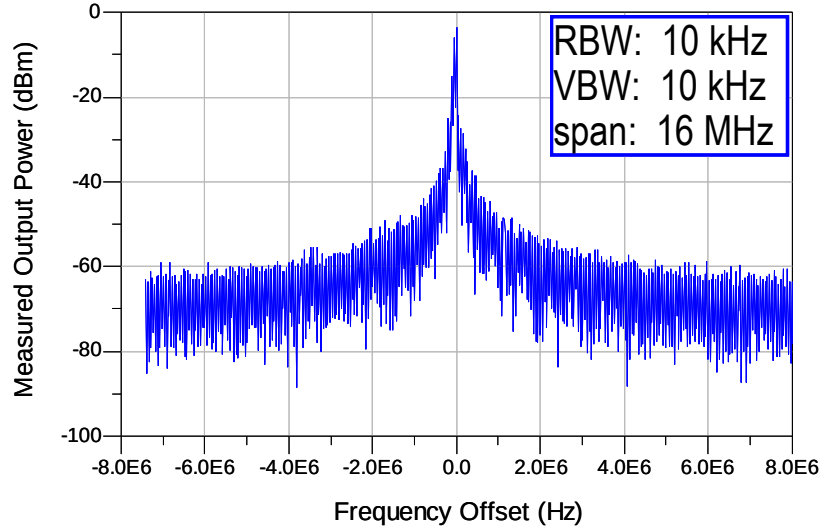


Fig. 4.8: Measured output spectrum of fundamental VCO.

4.6 – Comparison

Table 4.1 gives a comparison of the performance of the fundamental oscillator to other published microwave and millimeter-wave oscillators in CMOS, SiGe, and InP processes. This oscillator has a fundamental output power greater to or equivalent to each of those listed. Its phase noise is competitive with all listed HBT oscillators, while having a significant tuning range for its output power and phase noise. Neglecting the balun, the oscillator's power dissipation is competitive with the published results, being only 18 mW. As a first-pass design, the measured oscillator output frequency has shifted from that simulated. The circuit could be retuned in successive designs to address this issue. However, the primary goals of increasing the tuning range while reducing the power consumption and circuit area are achieved.

Table 4.1: Comparison of measured results to other published results.

Reference	This Work	[20]	[21]	[22]	[23]	[24]
Year	2010	2010	2008	2006	2002	2001
Technology	InP DHBT	90 nm CMOS	SiGe	InP DHBT	InP DHBT	InP HBT
Frequency (GHz)	53.4	55.7	49.4	35.0	43.5	18.6
Output Power (dBm)	2.5	-21.2	2.3	3.2	-6	0.2
Tuning Range (GHz)	2.4	FIXED	FIXED	0.35	13	7.75
Phase Noise (dBc @ 1MHz)	-89	-86.7	-93.8	-92	-	-90
Power Dissipation (mW)	87	14	-	17.2	197	130

5. 77 GHZ FREQUENCY SYNTHESIZER

5.1 – Circuit Design Overview

Phase lock loop (PLL) based feedback control can be employed to both stabilize and precisely tune the oscillation of a tunable high-frequency oscillator. By using frequency dividers in the PLL feedback path and having the phase detector and charge pump of the PLL operate at a much lower frequency, it is possible to lock a marginally stable high-frequency oscillator to a stable reference oscillator operating at only a fraction of the synthesizer's output frequency. Locking the high-frequency output to the low frequency reference in this negative feedback configuration serves to stabilize the phase variations at the output, leading to greater long-term and short-term stability (phase noise). As the high-frequency output is directly locked to the behavior of the high-fidelity reference input, the tuning of the reference input gives a corresponding tuning, scaled by the division ratio of the feedback, of the synthesizer's output frequency. Additionally, in more complex synthesizers, the divider ratio can also be dynamically altered to shift the output frequency, giving a means to digitally control the output frequency of the synthesizer. A diagram of a basic PLL-based frequency synthesizer is given in Figure 5.1.

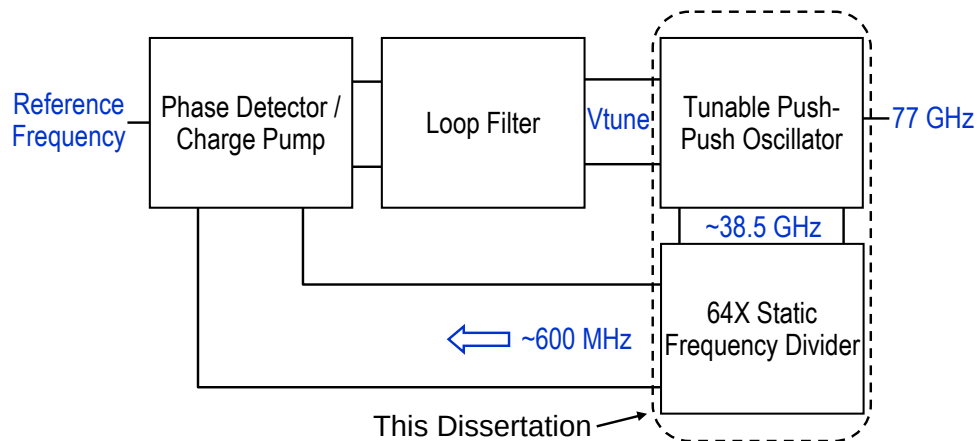


Fig. 5.1: Overview of a basic PLL-based frequency synthesizer, with the portion focused on in this dissertation circled.

This work focuses on the design of the synthesizer's high-frequency components, namely the integrated tunable push-push oscillator and a 64x frequency divider. As we are designing in a high performance non-complimentary InP HBT process (nnp configured transistors only), the implementation of the synthesizer's lower frequency components (phase detector and charge pump) in this technology would require a great deal of power dissipation, and would therefore be inferior in this regard to a less expensive and readily available CMOS based alternative.

The push-push oscillator generates both a 77 GHz output frequency ($2f_0$) and a 38.5 GHz (f_0) frequency that is used internally to drive the frequency dividers. A push-push oscillator is chosen over a fundamental oscillator for several reasons. The first is that it simplifies the design of the divider network and reduces its power consumption. Through the implementation of a push-push oscillator, it is possible to get 128x frequency division from the synthesizer output to the feedback signal with only the use of a 64x divider, eliminating the need for a power hungry high-frequency divider. There is also a direct correlation between the speed at which a static frequency divider can operate and the power which it must draw from the DC supply. Reducing the frequency of the signal that must be divided allows for the use of lower power divider stages. Another reason the push-push topology is beneficial is that the $2f_0$ and f_0 outputs of the push-push oscillator can be separated in such a way that the high-frequency output ($2f_0$) can be intrinsically isolated from the dividers, thereby eliminating the divider loading effects on the synthesizer output. Finally, it is possible to realize a resonant tank with a higher quality factor at f_0 than at $2f_0$, which will increase the stability of the oscillator.

5.1.1 – Push-Push Oscillator

Push-push oscillators use the coupling of two sub-oscillators operating at the same frequency and a relative phase of 180 degrees to double the output frequency of the overall

circuit. The diagram in Figure 5.2 illustrates the main principles behind the proper operation of a push-push oscillator. At the fundamental frequency, the sub-oscillators are out of phase, and therefore combine destructively and compress the summed output at the fundamental and at all odd harmonics. The second and all even harmonics of the sub-oscillators are in phase with one another and combine constructively to enhance the output at these frequencies. So in a properly designed push-push oscillator, a frequency doubling can be achieved through the suppression of the fundamental and enhancement of the second harmonic by the addition of an additional fundamental sub-oscillator.

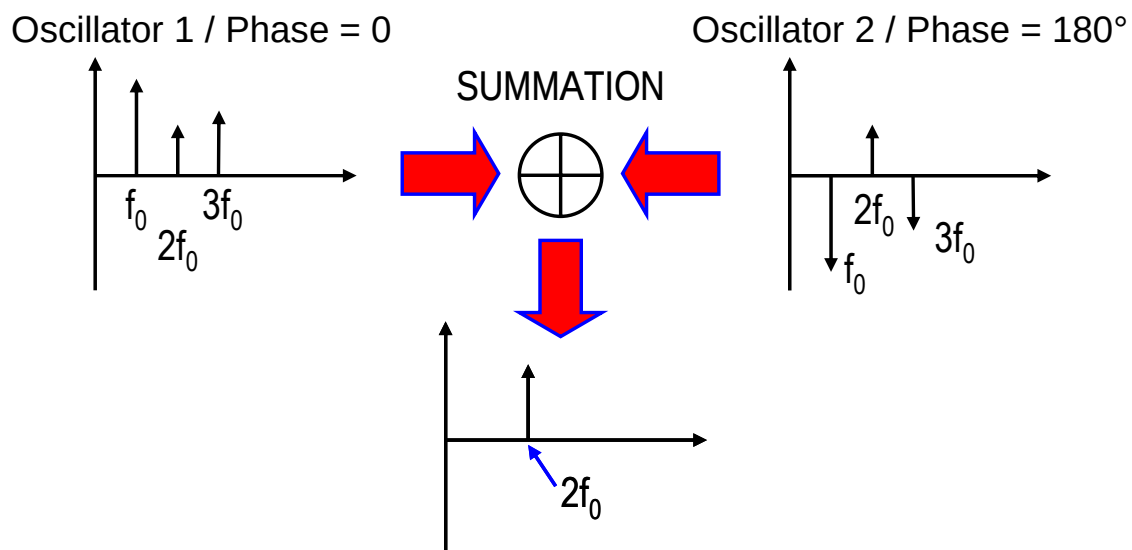


Fig. 5.2: High level illustration of push-push oscillator operation.

Ideally the total output power of the push-push oscillator will be the power in the second harmonic of an individual sub-oscillator, plus 3 dB from the summation. If possible, it is therefore desirable to maximize the second harmonic of the sub-oscillator while minimizing the magnitude of the third harmonic, because it is the third harmonic that is principally responsible for clamping the fundamental gain of the sub-oscillator's energy restoring amplifier.

A Colpitts topology is chosen for the sub-oscillators in this design because its resonant tank can be straightforwardly implemented with minimal loss [25], and since differential versions can be made perfectly symmetric in layout with only a minimal amount of parasitic coupling. Diagrams of the basic Colpitts oscillator topology are given in Figures 5.3(a) and 5.3(b), with the typical configuration shown in 5.3(a) and a rearranged yet identical configuration in 5.3(b).

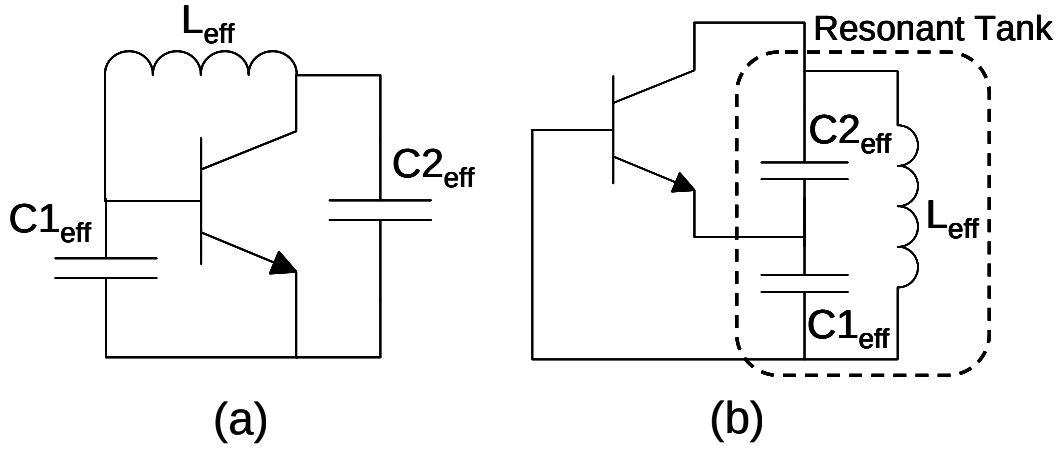


Fig. 5.3: (a) Typical Colpitts oscillator configuration and (b) rearranged configuration that shows resonant tank which stores the energy of oscillation.

When arranged in the configuration shown in Figure 5.3(b), the makeup of the resonant LC tank and the means through which positive feedback through $C1_{eff}$ and the active transistor gets fed into the tank become clearly visible. The resonance frequency of the tank is determined by inspection to be

$$\omega_0 = \frac{1}{\sqrt{L_{eff} \frac{C1_{eff} C2_{eff}}{C1_{eff} + C2_{eff}}}} \quad (5.1)$$

A differential common-base configured topology is designed and shown in Figure 5.4. Capacitors $C1$ and $C2$ are labeled to coincide with Colpitts labeling shown in Figure 5.3, and to

distinguish them from the DC blocking and AC grounding capacitors. Inductors are realized from electrically short AC grounded transmission lines. Differential oscillation is induced and common-mode oscillation prohibited through the coupling of the C1 capacitors. Only through the existence of a virtual ground at the PP_out node, seen in differential oscillation, can the oscillator feedback to the base of Q1 and Q2 be complete (Figure 5.3(a)). It is at this virtual ground PP_out node that the final oscillator output is taken, since differential mode (fundamental harmonic) suppression and common-mode (second harmonic) enhancement is seen. The negative and positive fundamental oscillator output used to drive the dividers is taken from the collector of Q1 and Q2 and buffered through an emitter follower, which helps drive the dividers and to isolate the oscillator from the kickback of the dividers.

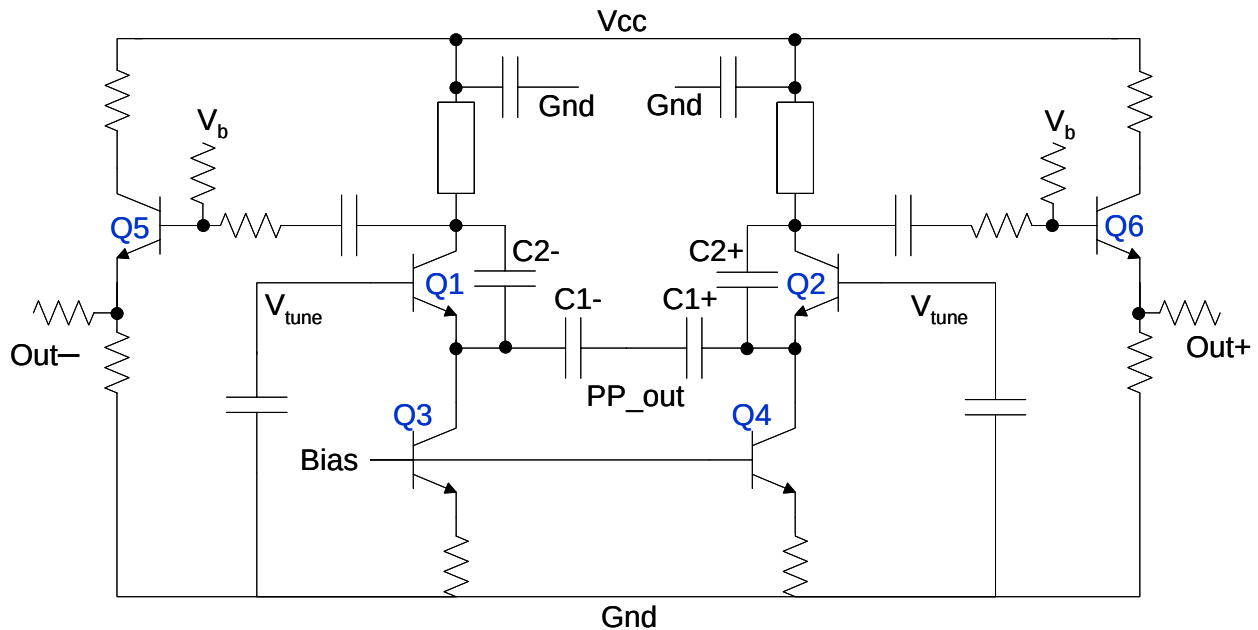


Fig. 5.4: Schematic of push-push oscillator.

Unlike most tunable oscillators, which use an external varactor network coupled to the resonant tank to alter their resonance frequency, this design uses the built-in tunable parasitics of

the network. Through the careful analysis and design that follows, it can be shown that through varying the base bias voltage of the oscillation transistors (Q1 and Q2), the base-collector junction capacitance of the oscillating and bias transistors can be varied to give a considerable tuning range without the addition of an additional varactor network.

Varying the applied base voltage serves to predominantly vary the voltage across the base-collector junction of both the Q1 and Q3 transistor (for this analysis, only the left half-circuit will be considered). This is easily recognized from the low frequency impedance seen “looking into” the emitter of Q1, $1/(g_m + g_b)$, and the collector of Q3, $r_{out}(1 + g_m R_E)$. Varying the applied base voltage also varies the voltage seen across the base-collector junction of Q1, because the collector of Q1 is DC coupled to V_{cc} ; therefore, the tuning behavior of this circuit is not immediately recognized and needs some analysis.

To start this analysis one must consider all of the parasitics loading the explicitly defined Colpitts oscillator. Neglecting the small charge transient time delay effects in the transistors, Q1, the oscillating transistor, loads the oscillator with its junction capacitances (C_{bc} and C_{be}) and the parasitic collector-emitter overlap capacitance (C_{ce}). It is reasonable to neglect the base and depleted collector transient time because this circuit is operating at one-eighth of the measured device f_T ; therefore, the device transient times are much shorter than a period of oscillation. As the Bias node is a small-signal ground, the base-collector junction capacitance of the Q3 current source transistor (C_d) also directly loads the resonant tank. Figure 5.5 gives a more physically accurate representation of the Colpitts schematic from Figure 5.3(b).

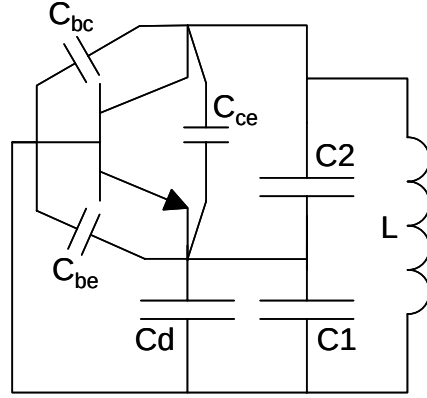


Fig. 5.5: Oscillator schematic showing a more accurate representation of the resonant tank.

From Figure 5.5, it is possible to calculate the effective capacitances and inductance in the idealized oscillator tank to be

$$C1_{eff} = C_{be} + C1 + Cd \quad (5.2)$$

$$C2_{eff} = C_{ce} + C2 \quad (5.3)$$

$$L_{eff} = \frac{L}{1 - \omega_0^2 L C_{bc}} \quad (5.4)$$

A qualitative understanding of the oscillator tuning can be gained from these equations. As V_{tune} increases, the applied voltage across C_{bc} is reduced, increasing the capacitance of C_{bc} , which serves to increase the effective inductance seen in the tank (L_{eff}). This increased effective inductance reduces the oscillation frequency of the tank. However, as V_{tune} is increased, the voltage applied across Cd increases, reducing the capacitance, which directly reduces the effective $C2$ capacitance, increasing the frequency of the tank. To get a quantitative tuning relationship, the nature of the capacitance tuning needs to be determined.

The circuit is designed in an epitaxially grown HBT technology, giving an abrupt interface between the p-doped base and the n-dope collector. As the junction is abrupt, the capacitance grading factor (m) simply equals 0.5, yielding the approximations for capacitance variation with applied voltage given in Equations 5.5 and 5.6 below. As transistors Q1 and Q3 have identical layer structures, the built-in junction potential, V_{jco} , will be the same for both capacitors.

$$Cd = \frac{Cd_0}{\sqrt{1 - \frac{V_{dbc}}{V_{jco}}}} \quad C_{bc} = \frac{C_{bc0}}{\sqrt{1 - \frac{V_{bc}}{V_{jco}}}} \quad (5.5, 5.6)$$

Substituting Equations 5.5 and 5.6 into Equations 5.2 and 5.4, will give an expression for the total frequency of oscillation of

$$\omega_0 = \left[\frac{L}{1 - \omega_0^2 LC_{bc}} \frac{(C_{be} + C_1 + C_d)(C_{ce} + C_2)}{C_{be} + C_1 + C_d + C_{ce} + C_2} \right]^{-\frac{1}{2}} \quad (5.7)$$

Differentiating this with respect to the tuning voltage, gives a tuning slope of

$$\frac{d\omega_0}{dv_T} = \frac{\omega_0}{4C1_{eff}} \left[\frac{YCd}{V_{jc0} - V_{dbc}} - \frac{C_{bc}}{Y(V_{jc0} - V_{bc})} \right] \quad (5.8)$$

where Y is defined as

$$Y = \frac{C2_{eff}}{C1_{eff} + C2_{eff}} \quad (5.9)$$

From Equations 5.8 and 5.9, it can be seen that the simultaneous tuning effects of C_d and C_{bc} work against each other in the overall tuning of the oscillator. By increasing the magnitude of C_d , through the selection of a larger effective current supply transistor, thereby increasing C_d , one can mitigate the counter effect of the parasitic C_{bc} tuning. Furthermore, by allowing C_1 to be small, while keeping the resonator's effective series capacitance constant, it is possible to increase the tuning range. Reducing C_1 increases the tuning coefficient, while also letting Y approach 1. Finally, the tuning range is also increased by biasing the circuit so that the collector-emitter bias (V_{ce}) of Q1 is larger than Q3, giving $(V_{jc0} - V_{dbc}) < (V_{jc0} - V_{bc})$ and increasing the sensitivity of C_d to the tuning voltage.

5.1.2 – Static Frequency Divider

The 64x static frequency divider is the straightforward cascade of six current mode logic (CML) topology static frequency dividers. The input to the divider chain is capacitively coupled to the 38.5 GHz Out+ and Out– signals from the oscillator shown in Figure 5.6, and each divider stage is capacitively coupled to the next within the chain, in order to eliminate the need for inter-stage emitter followers to level shift and drive the next stage.

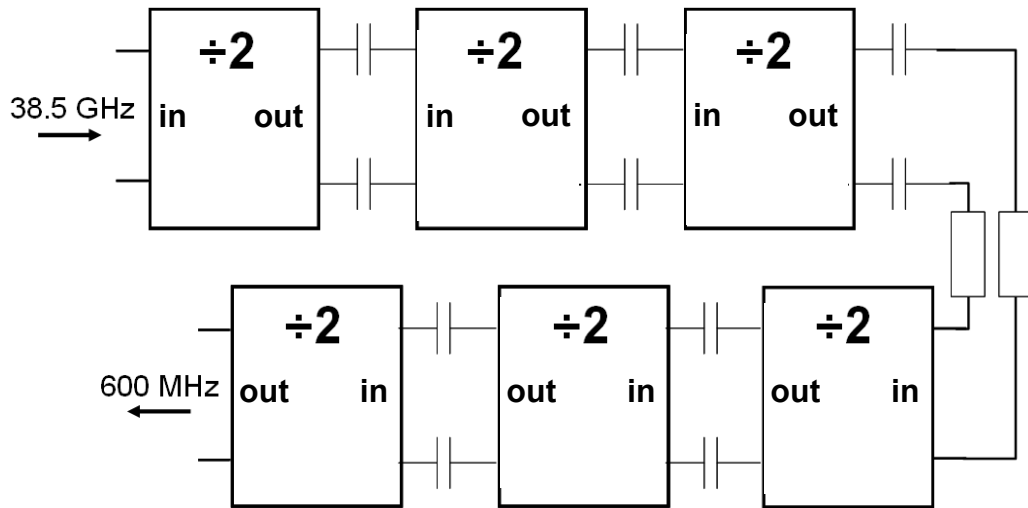


Fig. 5.6: Static frequency divider chain.

Eliminating inter-stage bias-shifting reduces the power consumption of the design and increases the design flexibility. The power consumption of the divider chain is also significantly reduced by driving the chain with the 38.5 GHz fundamental frequency of the oscillator, not directly driving it with a 77 GHz output. By reducing the frequency which has to be divided, it is possible to achieve proper operation with each stage having a lower current draw, because the required output rise time is reduced.

Figure 5.7 shows the topology of the static frequency divider that is used in this design. Resistive current sources are used to reduce degenerative parasitic loading and therefore to increase the input impedance and stability of the dividers. The bias current, and therefore speed of these dividers, is solely controlled by the common-mode bias applied to the differential inputs. The circuit is biased at the lowest voltage that gives proper 38.5 GHz operation.

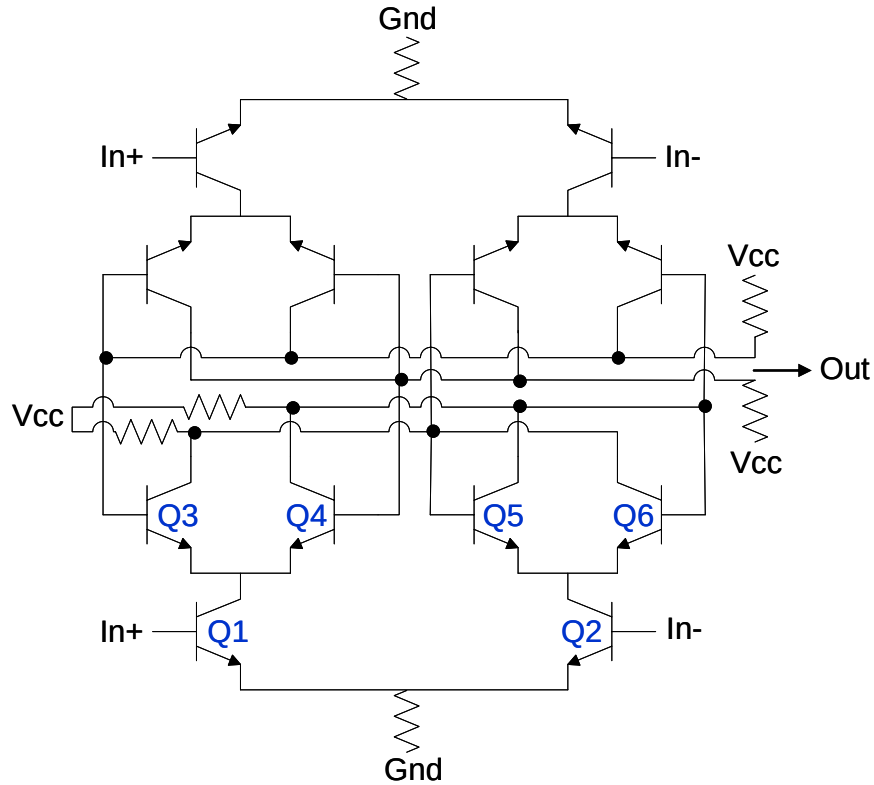


Fig. 5.7: CML static frequency divider topology.

5.2 – Technology

The circuit is laid out and fabricated in the Teledyne 0.5 μm InP/InGaAs DHBT process. This process has a measured peak f_T (unity current gain cutoff frequency) of 300 GHz and a maximum frequency of oscillation that scales with device length from 370 GHz for a 3 μm device to 300 GHz for a 10 μm device. The impressive frequency performance of this process enabled the circuit to be designed with low bias currents, while still achieving proper operation, thus reducing the power draw of the overall circuit.

A micrograph of the fabricated circuit is given in Figure 5.8. The total circuit, including power source decoupling capacitors and pads, is $1500 \times 900 \mu\text{m}^2$, with the intrinsic oscillator only consuming $140 \times 425 \mu\text{m}^2$ and the divider chain consuming $840 \times 465 \mu\text{m}^2$. From the micrograph, it can be seen that a significant portion of the intrinsic oscillator is composed of the capacitively terminated coplanar transmission lines which are used to implant the inductors in the Colpitts oscillator. Through implementing the inductors as short and straight transmission line segments, we are able to increase the quality factor, Q , of the resulting inductors by reducing the radiation loss that occurs at each inductor bend, and to increase the self-resonant frequency of the inductor by reducing self-capacitive coupling. Furthermore, we are free to choose a relatively high impedance transmission line ($>50 \Omega$) to reduce transmission line loss, increasing the intrinsic transmission line Q .

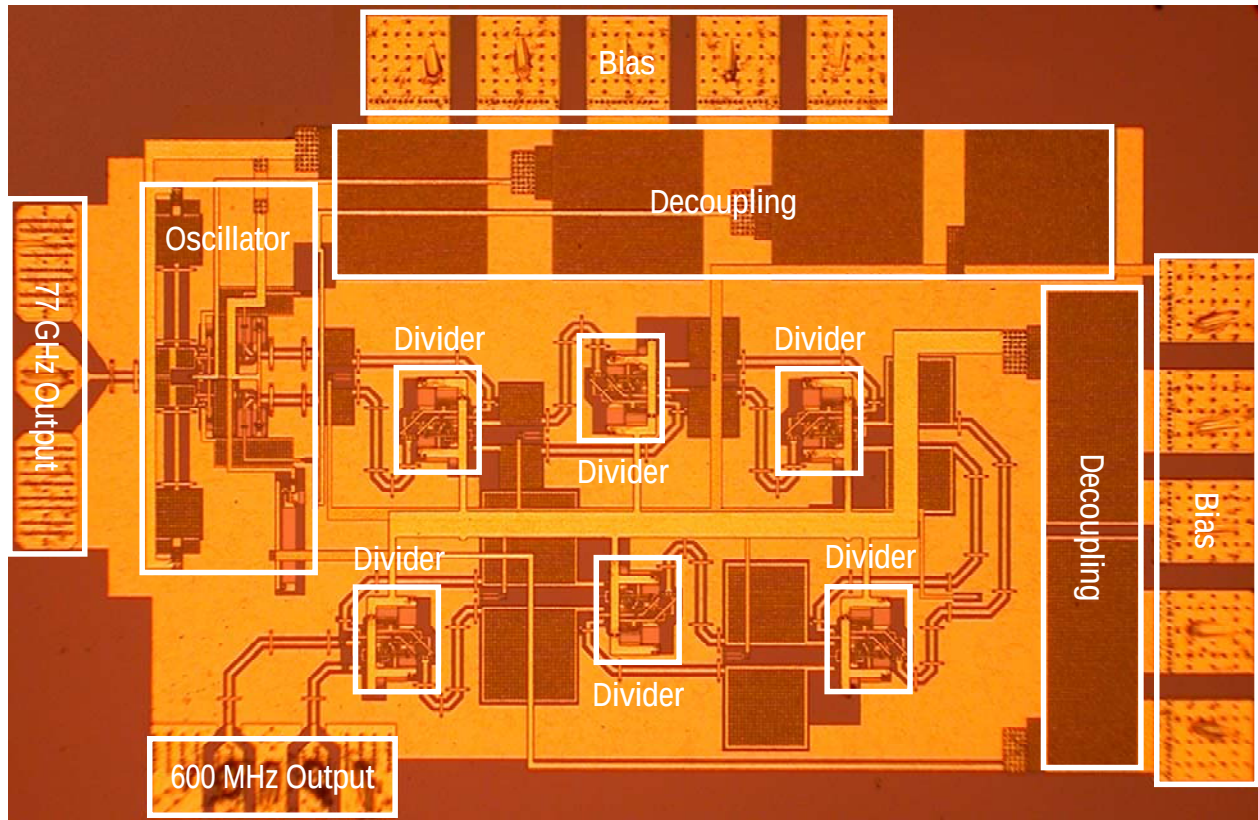


Fig. 5.8: Fabricated frequency synthesizer showing 77 GHz output, 600 MHz output, oscillator, dividers, decoupling capacitors and bias pads.

5.3 – Measurement Results

W-band (75 GHz to 110 GHz) frequency spectrum measurements were taken on the circuit's push-push output using an Agilent 8565E spectrum analyzer with an HP 11970W harmonic mixer to down convert the W-band output of the circuit to the operating band of the spectrum analyzer (<50 GHz). From these measurements, the output frequency and power characteristics were determined over the tuning range and are shown in Figure 5.9. The synthesizer's push-push output has a center frequency of 77.75 GHz and a tuning range of 1.3 GHz, while maintaining a 2.5 dB power variation across the tuning bandwidth. The oscillator has a peak output power -21.5 dBm in the W-band. This output power is relatively small, which

is expected of a push-push oscillator with a low power consumption. In most III-V applications, this output would be amplified and buffered [26].

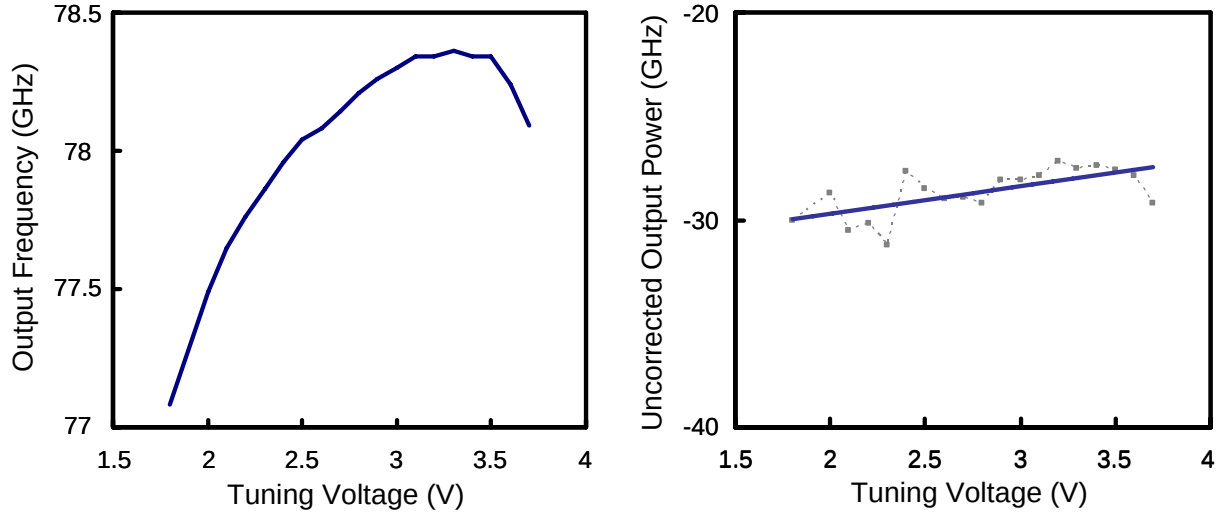


Fig. 5.9: Measured output frequency and power of the push-push output versus tuning voltage.

The 600 MHz baseband output showed a frequency tuning characteristic perfectly scaled by 128x to the W-band push-push output (Figure 5.10). The tuning characteristic matches with that derived in Equation 5.8. Below 3.2 V, the tuning is primarily from the variation of the C_d capacitance, giving a positive tuning slope. Above 3.2 V, the base-collector capacitance of the oscillating transistors (Q1 and Q2) dominates the tuning, giving a negative tuning slope. Further optimization of the oscillator design, through increasing the ratio of C_d to C_{bc} , would increase the tuning range and push the negative tuning slope out of the usable tuning range. The baseband output power is static across frequency, as it is set by the output voltage swing of the CML static frequency dividers at the output.

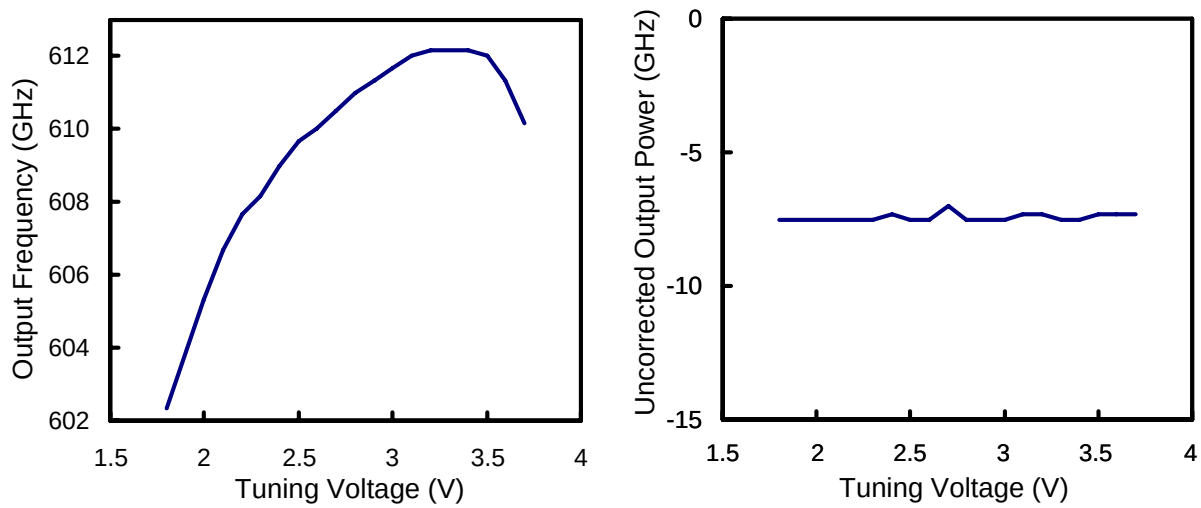


Fig. 5.10: Measured output frequency and power of the baseband (~600 MHz) output vs. tuning voltage.

A close-in, short-term stability measurement was taken on the spectrum analyzer to determine the phase noise of the W-band output and is shown in Figure 5.11. Due to the relatively low output power and phase noise of the push-push output signal, at an offset of 1 MHz from the peak, the signal power is in the noise floor of the spectrum analyzer. Due to this undesirable result, an exact calculation of the phase noise cannot be obtained; however, it is possible to determine that the phase noise at a 1 MHz offset must be less than -94 dBc/Hz.

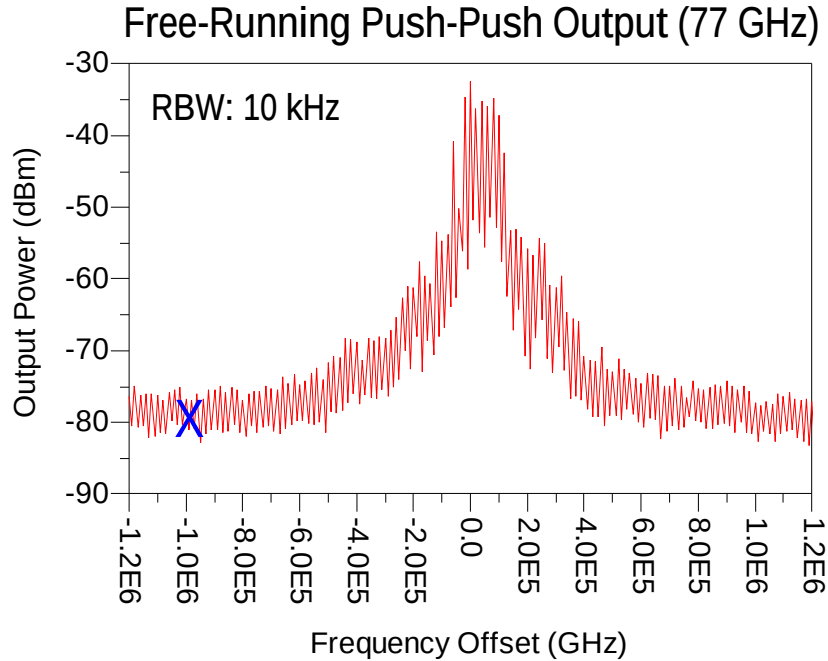


Fig. 5.11: Close-in spectrum measurement for phase noise approximation.

A measured base-band differential trace (Figure 5.12) shows the expected CML static frequency divider output with fast rise and fall times and a “noisy” hold value due to the charging and discharging of the regenerative latch in the CML topology. This signal had a peak-peak total jitter of 29 picoseconds. The “noisy” hold value of the trace can be cleaned up significantly through the use of an ECL topology static frequency divider, and it could also be sent through a limiter amplifier prior to being fed to a phase detector to stabilize the voltage signal.

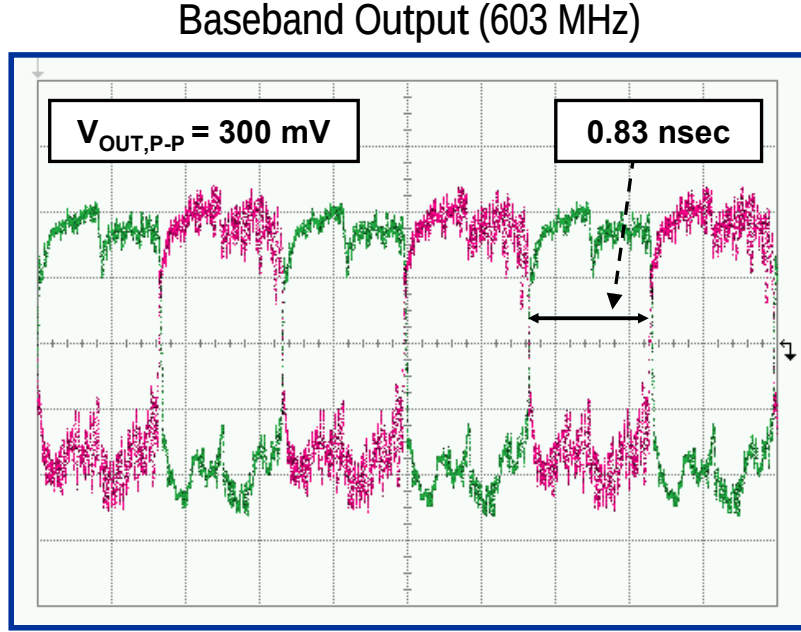


Fig. 5.12: Measured baseband differential output trace.

5.4 – Comparison

The oscillator figure-of-merit metric (FOM) that was proposed in the 2003 edition of *The International Technology Roadmap for Semiconductors* [26] has become the standard by which oscillators are compared. The figure of merit is given in Equation 5.10:

$$FOM = 20 \log \left(\frac{f_{osc}}{\Delta f} \right) - L(\Delta f) - 10 \log(P_{diss}) \quad (5.10)$$

The frequency of oscillation, phase noise, and power dissipation are heavily emphasized in this FOM. Because it is straightforward to amplify and buffer the oscillator's output signal prior to driving subsequent circuit stages, the oscillator's output power is not directly included in the FOM, since systems designers are primarily concerned with the noise performance and tuning

range of the oscillator. However, since an oscillator's phase noise is dependent on its total output power, the figure of merit does indirectly reward high power oscillations [27].

The power consumption of the oscillator circuit shown in Figure 5.4 is 84 mW, which is comparable to the lowest power CMOS oscillators, and significantly better than the BiCMOS or HBT oscillators at this frequency range (Table 5.1). This power consumption includes the power consumed in the two buffer amplifiers used to drive the frequency dividers, which is experimentally inseparable from the power consumed by the intrinsic oscillator. Even with its relatively low output power and the fact that only an upper estimate of the phase noise could be obtained, the oscillator designed here has an FOM of >173 dB. Due to its low power consumption, superior process technology, and being a direct oscillator, the fundamental 90 nm CMOS oscillator reported in [25] has a higher FOM than that reported here. We are confident that the FOM of our intrinsic oscillator, disregarding divider-driving buffers, which are not present in the CMOS oscillator in [25], is actually higher than 173 dB, and therefore more competitive. With technology advances to the transistor process that result in higher device f_T and f_{MAX} metrics, the circuit shown here could be redesigned at an even lower bias to reduce the power consumption, thus achieving an even higher FOM.

Table 5.1: Comparison of measured results to other published results.

Reference	This Work	[28]	[29]	[30]	[25]	[31]	[32]
Year	2011	2011	2009	2007	2006	2004	2003
Technology	500 nm InP DHBT	65 nm CMOS	180 nm SiGe	100 nm GaAs mHEMT	90 nm CMOs	1 μ m InP DHBT	GaAs HBT
Push-Push	Yes	No	Yes	Yes	No	No	Yes
Center Freq [GHz]	77.75	60.5	78.5	92	77	72.95	76.5
Tuning Range [GHz]	1.28	5	7	3.4	6.1	4.1	2.4
Free Running Phase Noise [dBc/Hz]	<-94 @1 MHz	-85 @1 MHz	-95 @1 MHz	-53 @100 kHz	-100 @1 MHz	-97 @1 MHz	-92 @1 MHz
Power Consumption [mW]	84	77.5	214	890	37.5	770	486
Output Power [dBm]	-21.5	-	4	6.1	-13.8	7.8	-2
FOM [dB]	>173	162.1	170.0	142.9	182.3	165.6	162.9

6. FUTURE WORK

One of the primary limitations affecting the performance of monolithically integrated oscillators is their short-term stability (phase noise). The oscillator phase noise dictates several crucial system parameters in transceivers, such as channel spacing, dynamic range, and sensitivity, and is a principal limitation on the stability of electromagnetic beams generated by phased array radar systems. As can be seen by the oscillator designs presented and cited in this dissertation, traditional integrated electrical oscillators in the millimeter-wave band typically have a phase noise greater than -100 dBc/Hz at a 1 MHz offset. This limited phase noise is a result of the limitations of the quality factor – which is a measure of the ratio of the peak energy stored in a resonant cavity to the energy lost per cycle – that can be achieved in the integrated resonant tank, which result from the high losses that occur in electrical resonators at millimeter-wave frequencies. As high quality factors are needed for improved stability [33], some other means of storing the energy of oscillation is needed that will have significantly less loss than is observed in traditional conductor based electrical resonators.

It has been shown that optical photons can be used to store the energy of oscillation in a dielectric resonator or delay line to produce electronic oscillations with a significantly improved phase noise over traditional electrical oscillators [34-35]. However, these optoelectronic oscillators are typically constructed as large, bulky, and sensitive lab bench setups that are not conducive to monolithic integration. In order to make fundamental improvements to the noise performance of integrated oscillators, some of the features of the existing bulky optoelectronic oscillators need to be integrated to create a fully monolithic optoelectronic design.

As III-V materials are needed for integrated optical components, e.g. lasers and LEDs, it is likely that III-V based HBTs will be the natural choice for electrical transistors for these new circuit architectures and material systems. Therefore, continued DHBT model development will be needed to accurately model the physical processes. Whenever fundamental changes are made to a BJT/HBT's layer structure, the models currently being used need to be reevaluated and most likely updated and replaced. As was shown in this dissertation, models that can sufficiently model bipolar junction transistor and single-heterojunction bipolar transistor performance are lacking when used to model double-heterojunction bipolar transistors; therefore, they need to be updated or replaced. The same will be true for the HBT models needed for the accurate simulations that will be required for these monolithically integrated optoelectronic oscillators.

REFERENCES

- [1] S. Raman, C. Tsu-Hsi, I. Abdomerovic, C. L. Dohrman, C. Maxey, and M. J. Rosker, "The DARPA COSMOS and ELASTx programs: towards next generation linearized microwave/mm-wave transmitters," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2010, pp. 1-4.
- [2] D. Caruth, S. C. Shen, D. Chan, M. Feng, and J. Schutt-Aine, "A 40 Gb/s integrated differential PIN+TIA with DC offset control using InP SHBT technology," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, 2002, pp. 59-62.
- [3] H. Fukuyama, K. Sano, M. Ida, K. Kurishima, K. Murata, K. Ishii, T. Enoki, and H. Sugahara, "InP/InGaAs DHBT parallel feedback amplifier with 14-dB gain and 91-GHz bandwidth," in *16th International Conference on Indium Phosphide and Related Materials*, 2004, pp. 659-662.
- [4] Z. Griffith, M. Urteaga, R. Pierson, P. Rowell, M. Rodwell, and B. Brar, "A 204.8 GHz static divide-by-8 frequency divider in 250 nm InP HBT," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2010, pp. 1-4.
- [5] C. C. McAndrew, J. A. Seitchik, D. F. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D. J. Roulston, M. Schroter, P. van Wijnen, and L. F. Wagner, "VBIC95, the vertical bipolar inter-company model," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1476-1483, 1996.
- [6] J. W. Lai, D. Caruth, Y. J. Chuang, K. Cimino, R. Elder, D. Jansen, F. Strolili, M. Le, and M. Feng, "300 GHz InP DHBT large signal model including current blocking effect and validated by Gilbert multiplier circuits," in *IEEE Compound Semiconductor Integrated Circuit Symposium (CSIC '05)*, 2005, p. 4.
- [7] Y.-J. Chuang, J.W. Lai, K. Cimino, M. Feng, M. Le, R. Milano, R. Elder, and F. Strolli, "InP/InGaAs DHBT large signal model for nonlinearity harmonic predictions in ICs," in *CS Mantech*, 2006, pp. 261-264.
- [8] J. Lai, "Large signal HBT model and integrated circuit design using 300-GHz InP HBT technology," Ph.D. Dissertation, Univeristy of Illinois at Urbana-Champaign, Urbana, IL, 2005.
- [9] J.-W. Lai, Y.-J. Chuang, K. Cimino, and M. Feng, "Design of variable gain amplifier with gain-bandwidth product up to 354 GHz implemented in InP-InGaAs DHBT technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, pp. 599-607, 2006.

- [10] H. K. Gummel and H. C. Poon, "An integrated charge control model of bipolar transistors," *Bell Systems Technical Journal*, vol. 49, pp. 827-852, 1970.
- [11] W. Snodgrass, W. Bing-Ruey, K. Y. Cheng, and M. Feng, "Type-II GaAsSb/InP DHBTs with record $f_T = 670$ GHz and simultaneous $f_T, f_{MAX} > 400$ GHz," in *IEEE International Electron Devices Meeting*, 2007, pp. 663-666.
- [12] T. Low, private communication, Apr. 2008.
- [13] W. Liu, *Handbook of III-V Heterojunction Bipolar Transistors*. New York: John Wiley and Sons, 1998.
- [14] C. R. Bolognesi, M. W. Dvorak, O. Pitts, S. P. Watkins, and T. W. MacElwee, "Investigation of high-current effects in staggered lineup InP/GaAsSb/InP heterostructure bipolar transistors: Temperature characterization and comparison to conventional Type-I HBTs and DHBTs," in *International Electron Devices Meeting (IEDM)*, 2001, pp. 35.2.1-35.2.4.
- [15] M. Alioto and G. Palumbo, *Model and Design of Bipolar and MOS Current-Mode Logic*. Norwell, MA: Kluwer Academic Publishers, 2005.
- [16] R. Elder, private communication, Sept. 2008.
- [17] J. Bongiorno and D. Graham, "An extension of the Nyquist-Barkhausen stability criterion to linear lumped-parameter systems with time-varying elements," *IEEE Transactions on Automatic Control*, vol. 8, pp. 166-170, 1963.
- [18] J. Rollett, "Stability and power-gain invariants of linear twoports," *IRE Transactions on Circuit Theory*, vol. 9, pp. 29-32, 1962.
- [19] R. Shimon, "Ion-implanted GaAs MESFET MMICs for 77-GHz automotive radar," Ph.D. Dissertation, University of Illinois at Urbana-Champaign, Urbana, IL, 2000.
- [20] A. H. T. Yu, T. Sai-Wang, K. Yanghyo, E. Socher, W. Hant, M. C. F. Chang, and T. Itoh, "A dual-band millimeter-wave CMOS oscillator with left-handed resonator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, pp. 1401-1409, 2010.
- [21] I. Ocket, J. B. Mills, A. John, and B. Nauwelaers, "60 GHz ultra low phase noise sigc common base oscillator using a wirebond coupled mcm integrated micromachined cavity resonator," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2008, pp. 182-185.
- [22] Z. Xin, W. Jing, and D. Pavlidis, "First InP/GaAsSb/InP DHBT Ka-band MMIC oscillator," in *The 1st European Microwave Integrated Circuits Conference*, 2006, pp. 153-156.

- [23] Z. Liyang, R. Pullela, C. Winczewski, J. Chow, D. Mensa, S. Jaganathan, and Y. Ruai, "A 37~50 GHz InP HBT VCO IC for OC-768 fiber optic communication applications," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2002, pp. 85-88.
- [24] H. Djahanshahi, N. Saniei, S. P. Voinigescu, M. C. Malikpaard, and C. A. T. Salama, "A 20-GHz InP-HBT voltage-controlled oscillator with wide frequency tuning range," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 1566-1572, 2001.
- [25] K. W. Tang, S. Leung, N. Tieu, P. Schvan, and S. P. Voinigescu, "Frequency scaling and topology comparison of millimeter-wave CMOS VCOs," in *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2006, pp. 55-58.
- [26] International technology roadmap for semiconductors – system drivers (2003 Edition).
[Online] Available: <http://www.itrs.net/Links/2003ITRS/SysDrivers2003.pdf>.
- [27] A. Hajimiri and T. J. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 179-194, 1998.
- [28] A. Musa, R. Murakami, T. Sato, W. Chaivipas, K. Okada, and A. Matsuzawa, "A 58 - 63.6 GHz quadrature PLL frequency synthesizer using dual-injection technique," in *16th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2011, pp. 101-102.
- [29] S. Trotta, B. Dehlink, A. Ghazinour, D. Morgan, and J. John, "A 77 GHz 3.3 V 4-channel transceiver in SiGe BiCMOS technology," in *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2009, pp. 186-189.
- [30] R. Weber, M. Kuri, M. Lang, A. Tessmann, M. Seelmann-Eggebert, and A. Leuther, "A PLL-stabilized W-band MHEMT push-push VCO with integrated frequency divider circuit," in *IEEE/MTT-S International Microwave Symposium*, 2007, pp. 653-656.
- [31] R. E. Makon, K. Schneider, R. Driad, M. Lang, R. Aidam, R. Quay, and G. Weimann, "Fundamental low phase noise InP-based DHBT VCOs with high output power operating up to 75 GHz," in *IEEE Compound Semiconductor Integrated Circuit Symposium*, 2004, pp. 159-162.
- [32] F. Lenk, M. Schott, J. Hilsenbeck, J. Wurfl, and W. Heinrich, "Low phase-noise monolithic GaInP/GaAs-HBT VCO for 77 GHz," in *IEEE MTT-S International Microwave Symposium Digest*, 2003, pp. 903-906.
- [33] E. J. Shelton, Jr., "Stabilization of microwave oscillators," *Transactions of the IRE Professional Group on Electron Devices*, vol. 1, pp. 30-40, 1954.
- [34] X. S. Yao and L. Maleki, "High frequency optical subcarrier generator," *Electronics Letters*, vol. 30, pp. 1525-1526, 1994.

- [35] X. S. Yao and L. Maleki, "Opto-electronic oscillator and its applications," in *1996 Internatonal Topical Meeting on Microwave Photonics*, 1996, pp. 265-268.