INVESTIGATION OF THE HAZARDS OF SUBSTRATE CURRENT INJECTION: TRANSIENT EXTERNAL LATCHUP AND SUBSTRATE NOISE COUPLING

BY

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THESIS

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ABSTRACT

Substrate current injection is the origin of external latchup and substrate noise coupling. The trigger current for external latchup depends on the duration of the trigger event. A physics-based model is provided to model the effects of aggressor to victim spacing and orientation on transient triggering of external latchup. The latchup susceptibility of standard cell based designs is also investigated. Guard rings are used to reduce latchup susceptibility and to reduce the substrate noise coupled to sensitive analog circuits. In this work, the effectiveness of different guard ring topologies for the reduction of substrate noise coupling is also investigated.

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CHAPTER 1: INTRODUCTION

Substrate current injection is the source of substrate noise coupling. If the magnitude of the injected current is sufficiently large, latchup may be triggered. The relatively small substrate currents that cause noise but not latchup are generally majority carrier currents, resulting from displacement current injection across PN junctions or bounce on the lines connected to the substrate taps. The milliamp range or larger substrate current needed to trigger latchup generally results from a forward-biased PN junction and can be either a majority or minority carrier current.

1.1 Transient external latchup

Latchup is termed as a state in which a low-impedance path, resulting from an overstress that triggers a parasitic PNPN structure, persists after removal or cessation of the triggering condition [1]. Parasitic PNPNs are present in all bulk-Si CMOS integrated circuits and an example of how one is formed is illustrated in Figure 1.1. Once latchup is triggered, the resulting current flowing from the power supply to the ground rail could result in circuit malfunction or permanent damage to the integrated circuit. If latchup is triggered by a voltage perturbation at one of the terminals of the parasitic PNPN, then it is termed as internal latchup. On the other hand, external latchup (ex-LU) is said to have occurred if the PNPN is triggered into the low impedance state due to the collection of excess carriers from the substrate [2].

Standardized I-tests described in the JEDEC latchup test standard, JESD78B, are relevant to external latchup [1]. Positive (negative) I-tests correspond to positive (negative) current injected at the signal pins. The test is performed while the chip is powered on and the injected current is the trigger source. Current drawn through each power supply is monitored and if any power supply shows an appreciable increase in current after the trigger source is removed, then latchup is said to have occurred. The trigger current (I_{trig}) is the smallest value of injected current that causes latchup. The current source used for the standardized I-tests have a slow rise-time (5μs-5ms) and long pulse-width (10μs-1s) and this is therefore termed as static testing. However, under real-world conditions, external latchup is triggered by current injection at a signal pin, resulting from cable discharges [3],[4] or other power-on ESD events. These disturbances are quite transient; e.g., a cable discharge event might last just 10s or 100s of nanoseconds [5],[6]. This has motivated previous investigations of transient external latchup [3],[4],[7],[8],[9].

Previous works on ex-LU show that the trigger current depends on the circuit layout; specifically, it depends on the spacing between the aggressor and the PNPN victim, denoted as d_{victim}, and on the orientation of the victim with respect to the aggressor, denoted as o_{victim} [4],[7],[10]. However, these previous works did not investigate how the transient properties of external latchup vary with layout. This work investigates and models the many ways in which layout affects the time scale on which non-steady-state behavior is observed. In addition to d_{victim} and o_{victim}, the effect of victim topology is considered. Figure 1.2 shows the layout of the test structures used in

[3],[4],[7],[8],[10]; such test structures are commonly used to characterize latchup. Note that the four diffusion stripes defining the victim PNPN are all co-linear. This does not represent the topology of a parasitic PNPN in a typical CMOS chip. Figure 1.3(a) shows a standard cell based layout. Figure 1.3(b) shows a PNPN test structure laid out using the standard cell style.

1.2 Substrate noise coupling

Substrate noise coupling is a problem faced while designing modern mixed signal ICs with digital and analog circuits on the same die. The digital circuits, which are constantly switching, inject into the substrate undesired noise that gets coupled to the noise-sensitive analog circuits due to the conductive nature of the substrate.

The use of guard rings is a popular noise isolation technique to reduce the amount of noise coupled to the analog circuits. In this work, various guard ring topologies are investigated and their effectiveness is compared. Emphasis is placed on the area efficiency of the different guard ring designs. Furthermore, using the fully characterized aggressor, victim and guard ring system, the effects of the aggressor and victim impedance on the noise isolation and guard ring placement are analyzed.

1.3 Thesis organization

In Chapter 2, transient external latchup measurement results are presented and discussed. Chapter 3 focuses on modeling the effects of d_{victim} and o_{victim} on the transient properties of external latchup. The effects of PNPN layout on latchup susceptibility are

investigated in Chapter 4. In Chapter 5 substrate noise coupling is discussed and the effectiveness of different guard ring topologies is compared. Finally, conclusions are drawn and future work is suggested in Chapter 6.

1.4 Figures

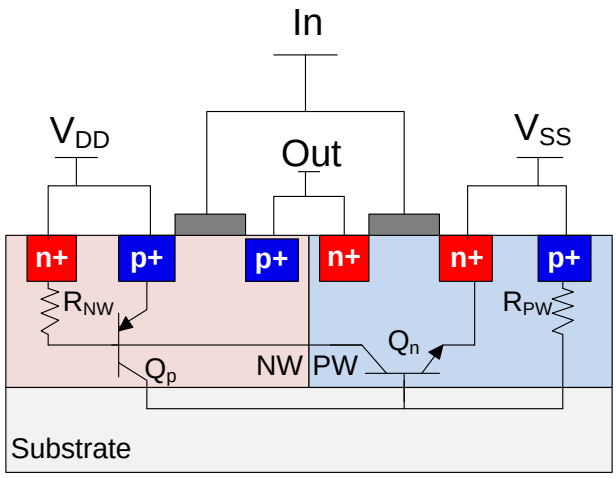

Figure 1.1: Cross-section of a CMOS inverter showing the parasitic BJTs that form the PNPN between the power supply and the ground rail. A P-type substrate is assumed.

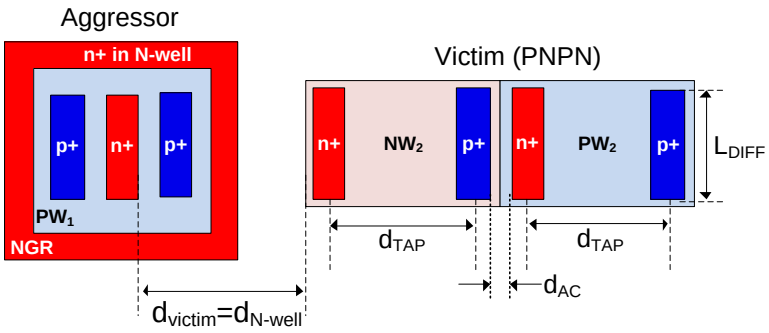

Figure 1.2: Layout view of test structure used to study negative ex-LU. Aggressor is surrounded by an N-well guard ring (NGR). A P-type substrate is used.

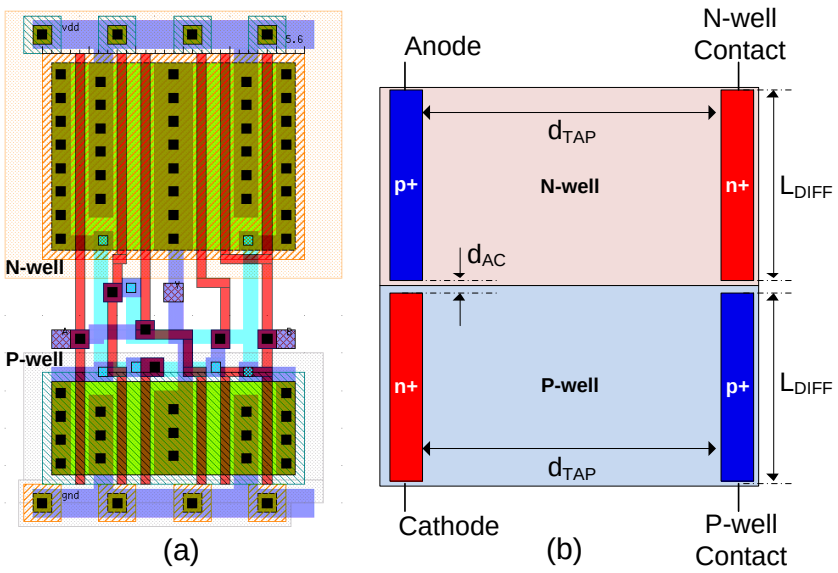

Figure 1.3: (a) Example standard cell layout [11]. (b) Parasitic PNPN in a standard cell type layout.

CHAPTER 2: TRANSIENT EXTERNAL LATCHUP MEASUREMENT RESULTS AND DISCUSSION

2.1 Experimental setup

The experimental setup is illustrated in Figure 2.1. A high power pulse generator is used to generate pulses with variable amplitude and pulse-width (T_{PW}). The rise time filter is used to fix the rise time (t_r) to 10ns unless otherwise specified. The pulse generator has an output impedance of 50Ω and a 50Ω matching network is used to facilitate current measurement; the voltage drop across R_s (Figure 2.1) is measured and the injected current (I_{inj}) is calculated. The pulse is applied to the signal pad of the test structure (I/O) and the current through the victim (I_{DD}) is monitored. Before latchup is triggered, the victim, i.e. PNPN, is in a high impedance state (I_{DD}<1nA). Latchup is said to have been triggered if I_{DD} exceeds 10mA once the trigger source has been removed. Even though the trigger current I_{trig} would be positive for the positive I-test and negative for the negative I-test, in this work only the magnitude of the I_{trig} will be reported.

I_{trig} is only a weakly decreasing function of V_{DD} [12]; moreover, latchup cannot be sustained for V_{DD}<1.1V, hence unless otherwise specified, the supply voltage V_{DD} is fixed to 1.5V.

2.2 Test structure design

Test structures were specifically designed to study transient ex-LU in a 130nm CMOS technology. To eliminate the parasitics associated with long jumper wires and multiple probes, a common problem for die level testing, care was taken to make most of

the connections on chip and to minimize the number of contact pads per test structure. Furthermore, the contact pad layout was made compatible for the use of RF probes. Test structures were fabricated to study both negative and positive I-tests. For the test structures used to study the negative I-tests, the number of contact pads required per test structure was minimized by connecting all the terminals that were to be biased at V_{SS} to a single contact pad (Figure 2.2). The n^+ in NW_2 and p^+ in NW_2 were also connected to a single contact pad. A total of five contact pads were required per test structure. Previously it was reported that during the positive I-tests, the inductance of the cable that connects the power supply to the test structure degraded the injected current waveform [12]. This was due to the fact that the power supply and the cable that connects the power supply to the test structure were present in the return path of the current injected at the I/O pad. The setup used in [12] is shown in Figure 2.3(a). In order to avoid the problem previously faced, the test setup was modified and the number of contact pads per test structure was minimized. In the modified test setup (Figure 2.3(b)) the N-wells are biased at V_{SS} and the P-wells are biased at $-V_{DD}$, and here the power supply is no longer present in the return path of the injected current, resulting in a much shorter return path, which in turn results in a much improved injected current waveform (Figure 2.4) when compared to the current waveform in [12]. The guard ring and all the other terminals that were to be biased at $-V_{DD}$ were connected to a single pad. Separate test structures were included with the guard ring unbiased to study the effect of the guard ring. It should be noted that in both the experimental setups (Figure 2.3 (a) and (b)) the potential difference between the

N-wells and the P-wells is V_{DD}; the modified experimental setup used in this work only helps in shortening the return path of the injected current at the I/O pad.

To study orientation effects, test structures with three different victim orientations 0°, 90° and 180° were fabricated (Figure 2.5 and Figure 2.6). To study the effects of aggressor to victim distance (d_{victim}) for the negative I-tests, test structures with different d_{victim} were fabricated. Apart from the traditional aggressors (N-well and P-well ESD diodes), an additional type of aggressor was also fabricated in which the I/O pad was directly connected to an N-well (Figure 2.7). In this case the entire N-well/P-well junction gets forward biased, injecting minority carriers into the substrate which trigger latchup (similar to negative I-test case).

During negative (positive) I-tests, minority (majority) carriers are injected into the substrate; traditionally to reduce latchup susceptibility, the P-well (N-well) aggressor is surrounded by an N-well guard ring or NGR (P-well guard ring or PGR) which help in collecting a portion of the electrons (holes) injected into the substrate before they reach the victim. In this work, an NGR is denoted as active if it is connected to V_{DD} and an active PGR is connected to V_{SS}. Inactive guard rings are left floating. An inactive guard ring is virtually identical to having no guard ring at all since an inactive NGR does not block minority carriers and an inactive PGR does not block majority carriers [12].

2.3 Negative I-test

To study the effect of pulse-width on trigger current, the T_{PW} is varied and the I_{trig} for different T_{PW} is recorded. As previously reported [3],[4],[7],[8],[9], the I_{trig} for

negative I-tests increases as the pulse-width is decreased (Figure 2.8). This is the first study in which test structures with different d_{victim} were available to study transient ex-LU, and Figure 2.8 compares the I_{trig} for the structures with three different d_{victim} as the pulse-width is varied. Measurement results are presented with the NGR active (Figure 2.8) and with the NGR inactive (Figure 2.9). It can be observed that as d_{victim} is reduced, the pulse-width at which transient effects become significant also decreases. Furthermore, activation of the NGR increases the 'DC' value of I_{trig} as expected; moreover the dependence of I_{trig} on T_{PW} also changes. The reason for these two phenomena will be explained in Chapter 3.

In Figure 2.10 the effect of orientation is illustrated. Even though the test structures with o_{victim} of 90° and 180° have the same $d_{N\text{-well}}$, the dependence of I_{trig} on T_{PW} for the two cases is quite different. $d_{N\text{-well}}$ is a function of d_{victim} and o_{victim}; specifically:

$$For\ o_{victim} = 90° \ or\ 180°,\ d_{N-well} = d_{victim} \tag{2.1}$$

$$For\ o_{victim} = 0°,\ d_{N-well} = d_{victim} + d_{TAP} \tag{2.2}$$

One might expect $I_{trig}(T_{PW})$ to be only a function of $d_{N\text{-well}}$, as this should determine the base width of Q_1 (Figure 2.5), which in turn should govern the transient characteristics of Q_1, but as explained in Chapter 3, $d_{N\text{-well}}$ alone does not determine the dependence of I_{trig} on T_{PW}; it has been hypothesized that the minority carrier current flow path has a significant influence on the transient characteristics.

The test structure with o_{victim}=0° (Figure 2.5(a)) could not be triggered into latchup during the negative I-test. As shown in [13], collection efficiency falls exponentially as the distance between the aggressor and the N-well of the detector ($d_{N\text{-}well}$) is increased. For o_{victim}=0°, the NW_2 is an additional d_{TAP} (40μm) distance away from the aggressor when compared to the o_{victim}=180° (Figure 2.5(a) and Figure 2.5(b)) and hence the collection efficiency for o_{victim}=0° would be significantly smaller when compared to o_{victim}=180°. In this technology (1-2 Ω-cm substrate resistivity), the collection efficiency for o_{victim}=0° had a very small value which resulted in I_{trig} above the current limit of the experimental setup.

As previously observed [8], rise time did not have a significant impact on I_{trig} (Figure 2.11). Reducing the rise time would increase the displacement current; however, since displacement current is a majority carrier current and since during negative I-tests latchup is triggered by minority carriers, the observed trend is as expected.

2.4 Positive I-test

In this study, during the positive I-test, no significant change in the I_{trig} was observed as the T_{PW} was varied from 100ns to 1ms (Figure 2.12). This was observed with test structures with all 3 victim orientations (constant d_{victim}=4μm). As explained in [8] the pulse-width dependence of I_{trig} is governed by the base width of Q_2 (Figure 2.6(a)). The base width for Q_2 is determined by the N-well depth. Q_1's base width (Figure 2.5(a)) on the other hand is determined by $d_{N\text{-}well}$. Hence, since Q_2 has a much shorter base than

Q_1, the pulse-width dependence of negative I_{trig} would be more pronounced than that of positive I_{trig}.

As rise time was varied, no significant change in I_{trig} was observed with the PGR inactive; however, with the PGR active, a small decrease in I_{trig} was observed as the rise time was decreased (Figure 2.13). Displacement current increases as rise time is reduced and since displacement current is a majority carrier current, it would aid in triggering latchup as majority carriers trigger latchup during positive I-tests. With the PGR active, the I_{trig} is roughly 30 times larger when compared to the case with the PGR inactive. This larger trigger current would translate to a larger voltage applied across the PN junction of the aggressor, which would in turn result in a larger displacement current. With the PGR inactive, the I_{trig} is small (~10mA) and the voltage across the diode would be relatively small, resulting in an insignificant displacement current. Hence the effect of rise time on I_{trig} is observed only in the case with the PGR active.

2.5 N-well aggressor

With an N-well aggressor (Figure 2.7), the I/O pad directly connects to the N-well and when pulsed, the entire N-well/P-well junction gets forward biased, injecting minority carriers into the substrate. The dependence of I_{trig} on T_{PW} is plotted in Figure 2.14. It can be observed that the I_{trig} does not have a very strong dependence on T_{PW}. For the same d_{victim} (12μm), with a P-well ESD diode as the aggressor, I_{trig} shows a strong dependence on T_{PW} for T_{PW} below ~1μs (Figure 2.8); however, this is not observed with the N-well aggressor. The transient properties of Q_1 would be dominated by its base

width, and since in both the cases the base width is expected to be the same, one would not expect a change in the transient properties of ex-LU. However, due to the test structure design, with an N-well aggressor, it was hypothesized that ex-LU was not triggered in the conventional manner and a new triggering mechanism is proposed to explain the transient characteristics.

Minority carriers are injected into the substrate by applying a negative pulse on the I/O pad to forward bias the NW_1/substrate PN junction. For o_{victim}=180°, the substrate contact closest to NW_1 is the p^+ diffusion in PW_2 (Figure 2.7(a)), which is 92μm from NW_1. Hence R_{SUB} would have a large value. Most of the current injected by NW_1 will have to flow through R_{SUB} before it is collected by the substrate tap; therefore, to inject more and more current, a large negative voltage needs to be applied on the I/O pad. Most of the voltage applied on NW_1 will drop across R_{SUB}, and ~0.7V will drop across the NW_1/substrate PN junction. Due to this, the substrate potential near NW_2 will be significantly lowered. NW_2 is biased at V_{DD} (1.5V). It was found that due to the lowering of the substrate potential in the vicinity of NW_2, the reverse bias across the NW_2/substrate PN junction would be large enough to break down this PN junction. Once the NW_2/substrate junction breaks down, latchup would be triggered at the victim. This breakdown mechanism would not be significantly affected by the change in pulse-width and hence I_{trig} does not change significantly as the pulse width is reduced. With o_{victim}=90° (Figure 2.7(b)), R_{SUB} has a smaller value and hence a larger I_{trig} is observed (Figure 2.14).

2.6 Figures

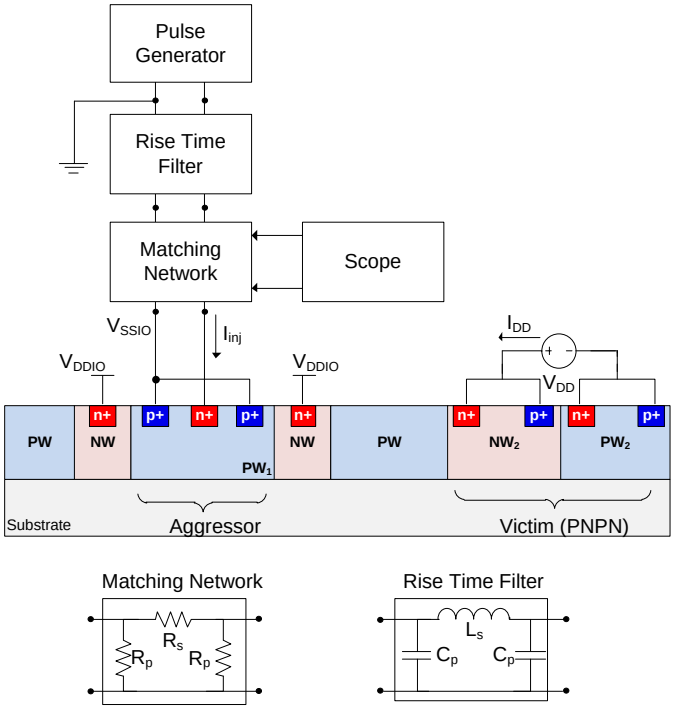

Figure 2.1: Experimental setup. I_{inj} is the injected current. A P-well diode aggressor is illustrated; in this case, negative pulses would be applied and I_{inj} is negative. V_{DD}=V_{DDIO}=1.5V. 130nm CMOS. r_{sub}=1-2 Ω-cm.

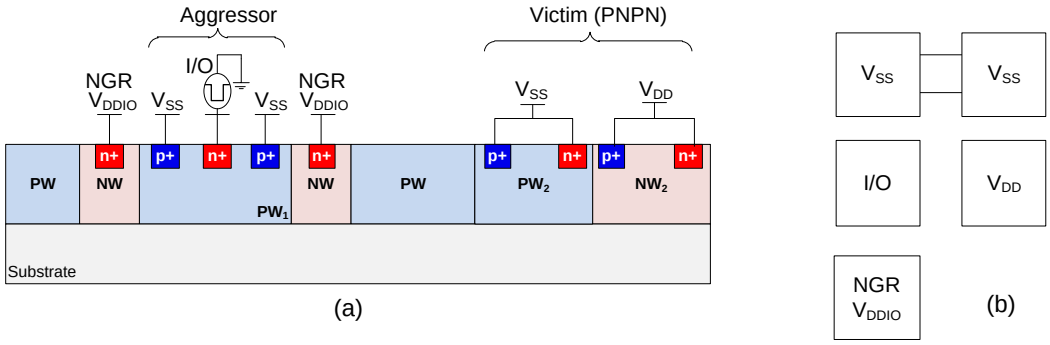

Figure 2.2: (a) Negative I-test experimental setup. (b) Corresponding contact pad layout. Two V_{SS} pads (which are shorted on chip) are present to make the contact pad layout compatible for the use of RF probes.

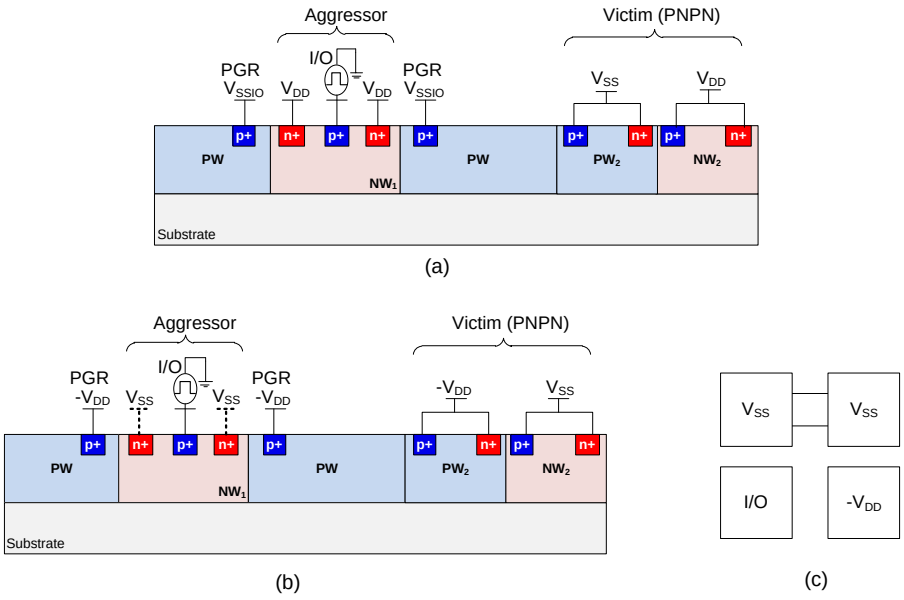

Figure 2.3: (a) Experimental setup used for positive I-test in [12]. A jumper is used to connect the shield of the pulse generator and power supply probes. (b) Modified experimental setup for positive I-test used in this work. No jumpers are required if an RF probe is used. (c) Corresponding contact pad layout. Two V_{SS} contact pads (which are shorted on chip) are present to make the pad layout compatible for the use of RF probes. Separate test structures were included with the guard ring unbiased.

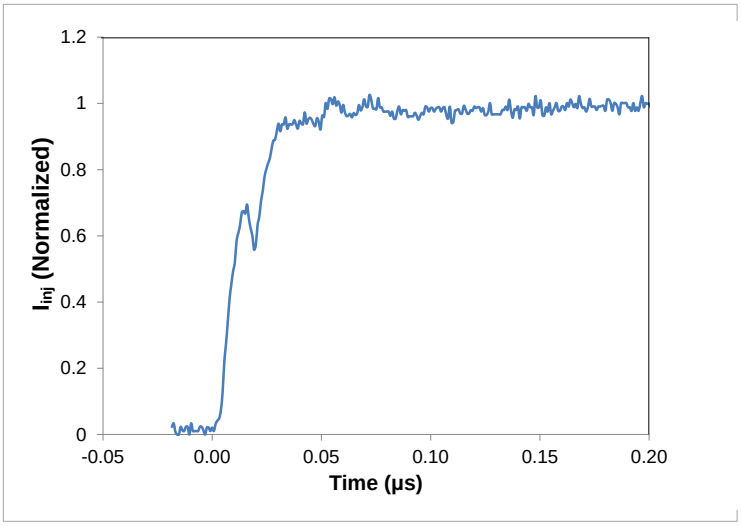

Figure 2.4: The injection current as a function of time during a transient positive I-test. The kink observed on the rising edge is artificial and is not a result of the parasitics in the test setup. The reason for the kink has been explained in [14].

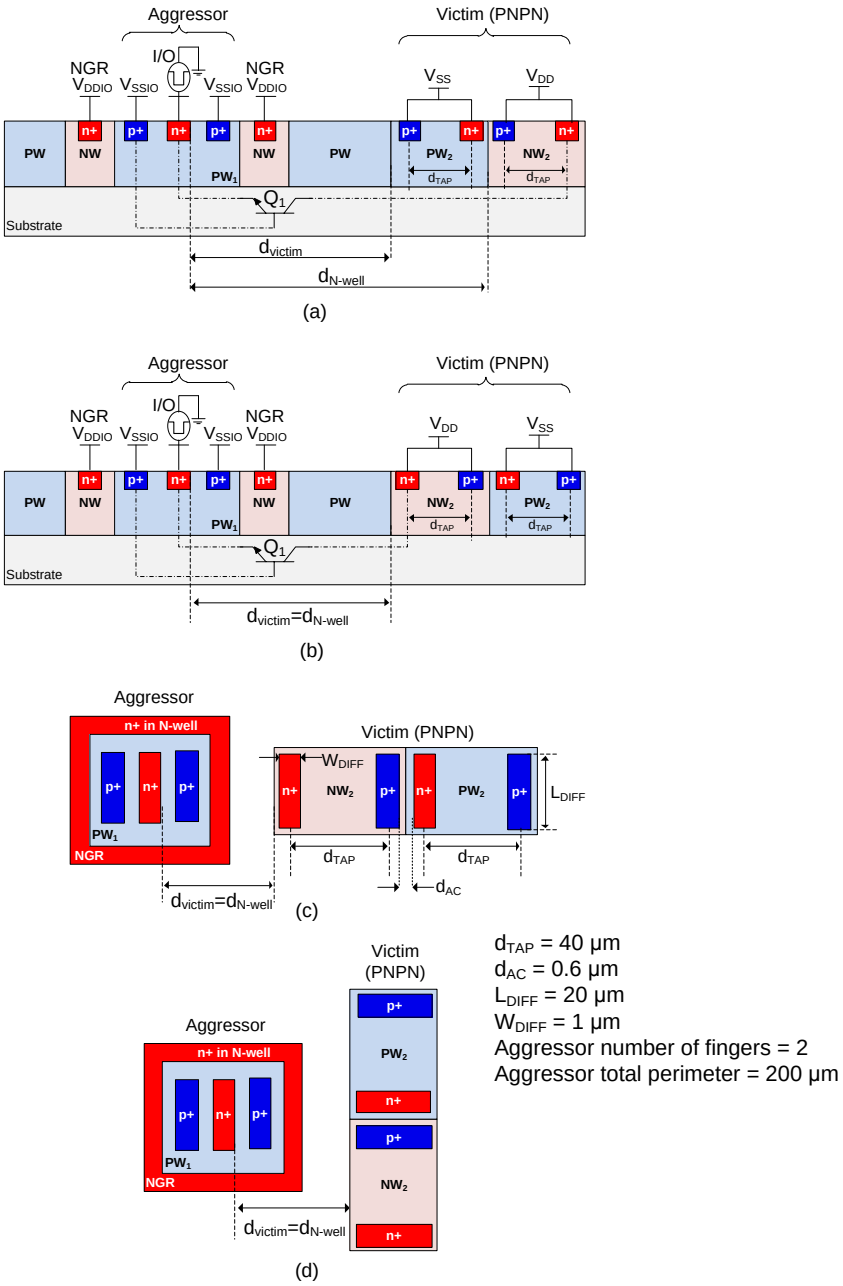

Figure 2.5: Cross-section and layout views of test structures used for negative I-tests. Each test structure consists of a victim (PNPN) and an aggressor (P-well ESD diode) with 2 fingers (only one shown). Three different victim orientations are illustrated: (a) Cross-section of 0° victim orientation with the P-well of the victim (PW_2) closer to the aggressor. (b) Cross-section of 180° victim orientation with the N-well of the victim (NW_2) closer the aggressor. (c) Layout view of the 180° victim orientation. (d) Layout view of the 90° victim orientation with both PW_2 and NW_2 adjacent to the aggressor.

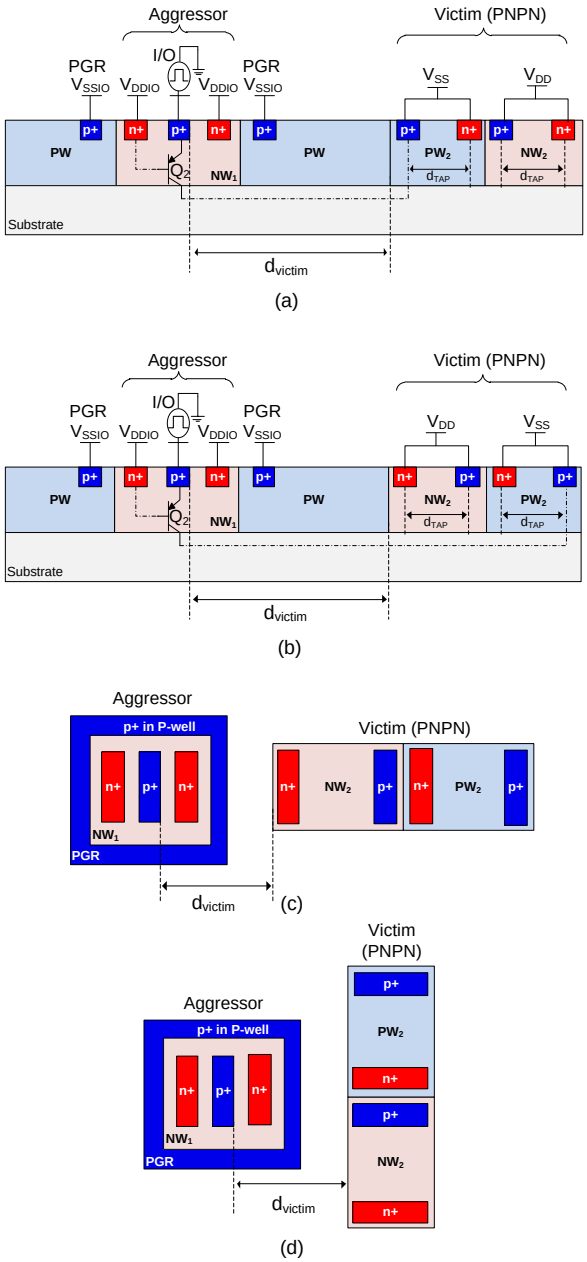

Figure 2.6: Cross-section and layout views of test structures used for positive I-tests. Each test structure consists of a victim (PNPN) and an aggressor (N-well ESD diode) with 2 fingers (only one shown). Three different victim orientations are illustrated: (a) Cross-section of 0° victim orientation with the P-well of the victim (PW_2) closer to the aggressor. (b) Cross-section of 180° victim orientation with the N-well of the victim (NW_2) closer the aggressor. (c) Layout view of the 180° victim orientation. (d) Layout view of the 90° victim orientation with PW_2 and NW_2 of the victim adjacent to the aggressor.

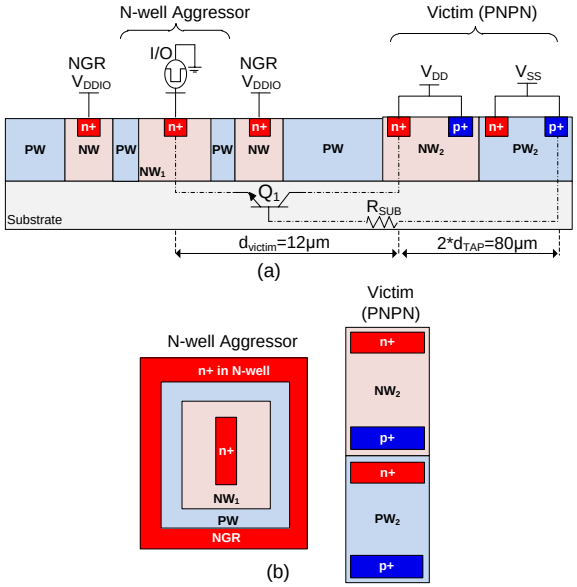

Figure 2.7: Test structures used to study N-well aggressors. The aggressor consists of the I/O pad directly connected to the n^+ fingers in the N-well (only one of 2 fingers shown). Two different victim orientations illustrated. (a) Cross-section of 180° orientation with the N-well of the victim (NW_2) closer the aggressor. (b) Layout view of the 90° victim orientation with PW_2 and NW_2 of the victim adjacent to the aggressor.

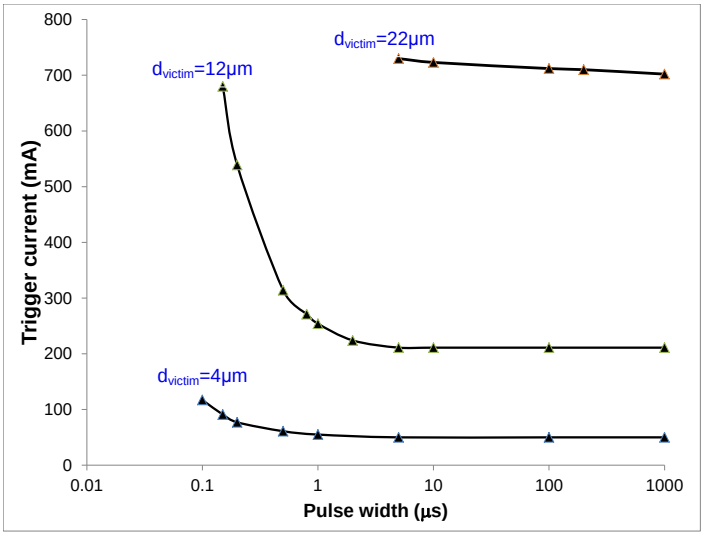

Figure 2.8: I_{trig} vs. T_{PW}. Negative ex-LU. o_{victim}=90° (Figure 2.5(d)).When d_{victim}=22µm, I_{trig} is near the current limit of the experimental setup. The experiment is repeated with the NGR unbiased (see Figure 2.9) so that the variation of I_{trig} with T_{PW} can be observed more precisely.

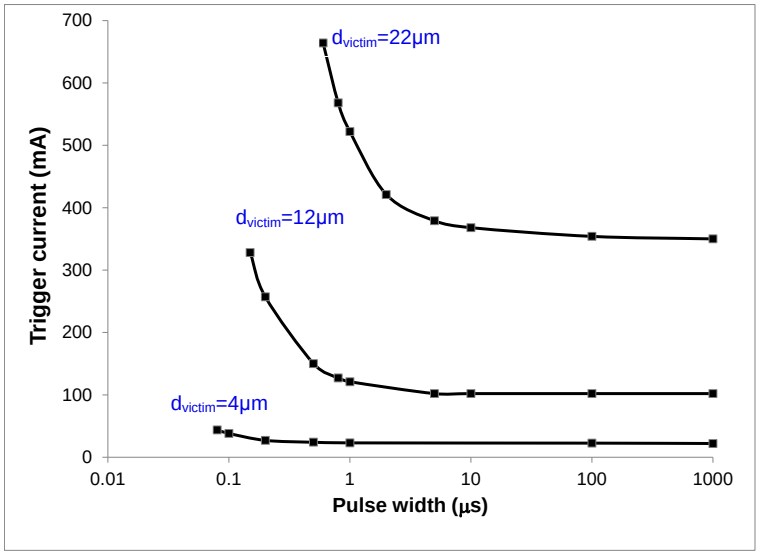

Figure 2.9: I_{trig} vs. T_{PW}. Negative ex-LU. o_{victim}=90°. NGR inactive.

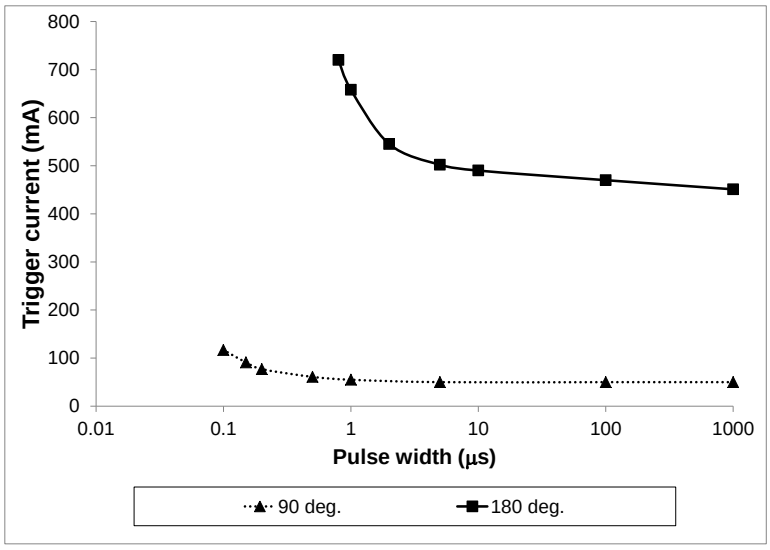

Figure 2.10: Negative ex-LU. Influence of orientation on $I_{trig}(T_{PW})$. Both test structures have $d_{victim}=d_{N\text{-}well}$=4µm. For o_{victim}=0°, I_{trig} was beyond the current limit of the experimental setup.

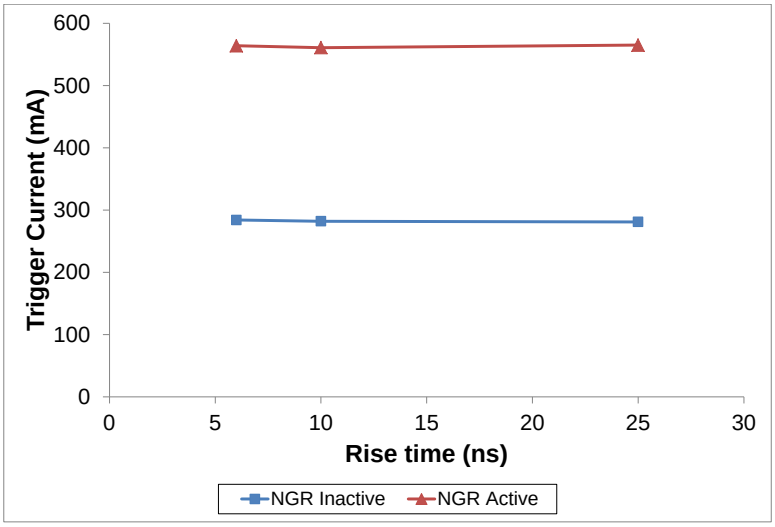

Figure 2.11: I_{trig} vs. Rise time for negative I-test. o_{victim}=90̊, d_{victim}=12µm. T_{PW}=200ns.

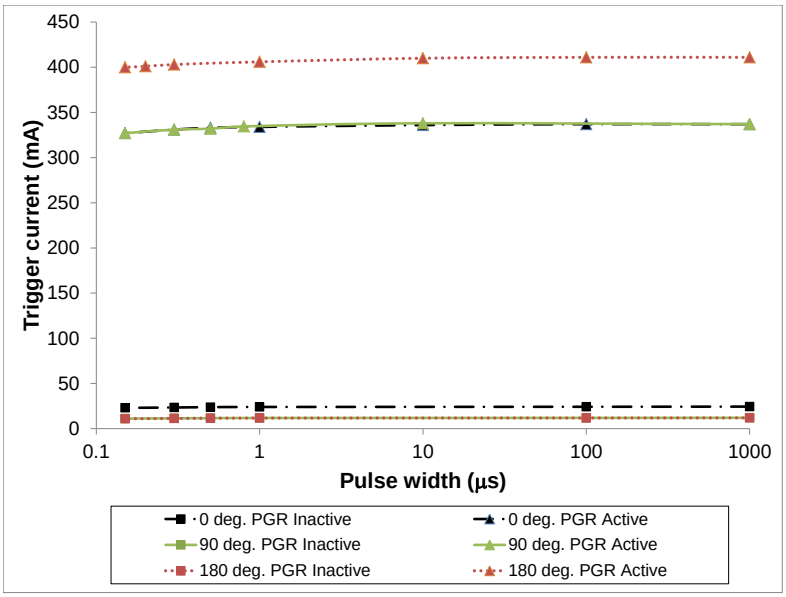

Figure 2.12: I_{trig} vs. T_{PW} for positive I-test for three different orientations. All 3 structures have d_{victim}=4µm.

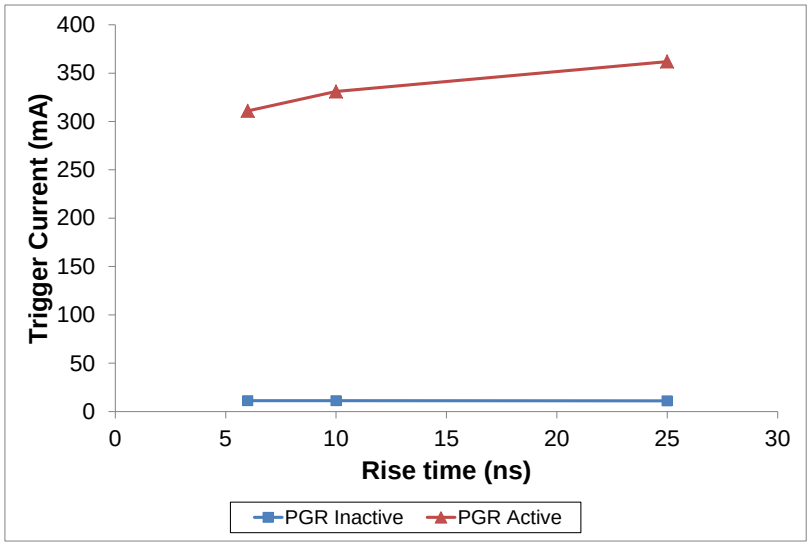

Figure 2.13: I_{trig} vs. rise time for positive I-test. o_{victim}=90˚, d_{victim}=4µm. T_{PW}=200ns.

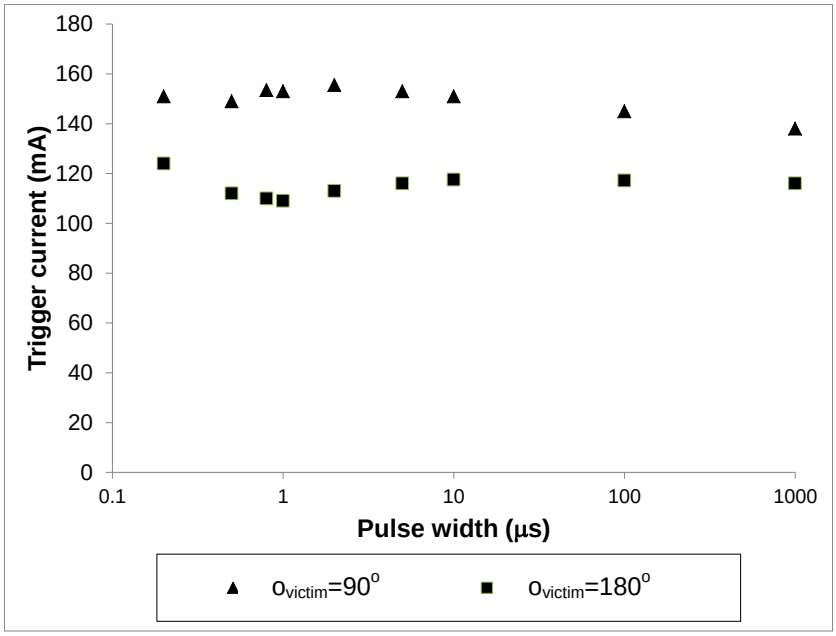

Figure 2.14: I_{trig} vs. T_{PW} for test structures with N-well aggressors. Both structures have d_{victim}=12µm.

CHAPTER 3: MODELING TRANSIENT EXTERNAL LATCHUP

3.1 Single pole model for collection efficiency (α)

In [3] and [12] it was shown that a single pole model for collection efficiency can be used to model the effects of pulse-width on trigger current. Until now, the single pole model has been used as a fitting expression for the measurement data. However, in this work, using a circuit level model for Q_1, the single pole model has been derived. As described in [10], the I_{trig} during the negative I-test can be expressed as follows:

$$I_{trig} = \frac{I_{NW}^{crit}}{\alpha_0} \tag{3.1}$$

Latchup is triggered if the current collected by NW_2 (Figure 2.5) exceeds the critical value I_{NW}^{crit}. α_0 is the common-base current gain of Q_1 and is also referred to as the collection efficiency of NW_2. As explained in [8], the pulse-width dependence of I_{trig} during the negative I-test is attributed to the bandwidth limitations of transistor Q_1. In order to derive the pulse-width dependence of α, let us consider the circuit level model for Q_1 in Figure 3.1(b):

$$Q_B = I_C \tau_B, \;\; I_C = \beta_0 I_D \tag{3.2}$$

$$I_\pi = \frac{dQ_B}{dt} = \tau_B \beta_0 \frac{dI_D}{dt} \tag{3.3}$$

$$\beta_{eff} = \frac{I_C}{I_D + I_\pi} = \frac{I_C}{I_D + \tau_B \beta_0 \frac{dI_D}{dt}} \tag{3.4}$$

In the Laplace domain, equation (3.4) transforms to:

$$\beta_{eff}(s) = \frac{I_C}{I_D + \tau_B \beta_0 I_D s} = \frac{I_C}{I_D} \cdot \frac{1}{1 + \tau_B \beta_0 s} = \frac{\beta_0}{1 + \tau_B \beta_0 s} \tag{3.5}$$

From the expression for $\beta_{eff}(s)$, the following expression for $\alpha_{eff}(s)$ can be derived:

$$\alpha_{eff}(s) = \frac{\beta_{eff}(s)}{\beta_{eff}(s) + 1} = \frac{\beta_0}{\beta_0 + 1 + \tau_B \beta_0 s} = \frac{\alpha_0}{1 + \tau_B \alpha_0 s} \tag{3.6}$$

$$\omega_{3dB} = \frac{1}{\alpha_0 \tau_B} \quad or \quad f_{3dB} = \frac{1}{2\pi \alpha_0 \tau_B} \tag{3.7}$$

Q_B is the charge stored in the base, τ_B is the base transit time, β_0 is the DC common-emitter current gain and α_0 is the DC common-base current gain. From the single pole model of α_{eff} in equation (3.6), it can be observed that the pole frequency is f_{3dB}, which can be expressed in terms of α_0 and τ_B as shown in equation (3.7).

In the time domain, equation (3.6) transforms to:

$$\alpha_{eff}(t) = \alpha_0 \left(1 - e^{-2\pi f_{3dB} t}\right) \tag{3.8}$$

Substituting the expression for α_{eff} in equation (3.1) we get:

$$I_{trig}(T_{PW}) = \frac{I_{NW}^{crit}}{\alpha_0 \left(1 - e^{-2\pi f_{3dB} T_{PW}}\right)} = \frac{I_{trig}^{DC}}{\left(1 - e^{-2\pi f_{3dB} T_{PW}}\right)} \tag{3.9}$$

Equation (3.9) models the pulse-width dependence of I_{trig}. In Figure 3.2 the model is compared to the measurement data and a good fit is observed.

3.2 Modeling base transit time

In Figure 3.3 the variation of f_{3dB} with d_{victim} and the effect of the NGR being active or inactive are illustrated. It can be observed that f_{3dB} decreases as a function of d_{victim}; moreover, for a small d_{victim} (4μm), with the NGR active, the f_{3dB} decreases but for larger d_{victim}, the presence or absence of the NGR does not affect f_{3dB} significantly.

To explain the trend observed, the variation of f_{3dB} with d_{victim} should be understood. From equation (3.7) it can be observed that f_{3dB} is inversely proportional to α_0 and the base transit time (τ_B) of transistor Q_1. In this work, α_0 was modeled as a function of $d_{N\text{-}well}$. The procedure for modeling α_0 as a function of $d_{N\text{-}well}$ is described in [15]. The carrier diffusion length L_n, which is a parameter required to model α_0 [15], was extracted from the measurement data obtained from test structures with three different d_{victim} with the same o_{victim}=90°. The relation between $d_{N\text{-}well}$ and d_{victim} was given in section 2.3.

Now, the variation of τ_B with d_{victim} should be analyzed. As shown in [16], a simple model relating τ_B and base width of Q_1 (W_B) is as follows:

$$\tau_B = K \cdot W_B^2 \tag{3.10}$$

K depends on the diffusion coefficient and the base doping profile. In this work, K is treated as a fitting parameter and has been extracted from the measurement data.

In Figure 3.4 the model for τ_B (3.10) is plotted along with the measurement data. From the measured values of f_{3dB} and α_0 and using equation (3.7), the measurement data for τ_B can be calculated. Measurement data was obtained from 3 structures, each with a different d_{victim} (4μm, 12μm, 22μm). In order to understand the trend observed in the variation of τ_B with the NGR active and inactive, the effect of the NGR on W_B should be first analyzed. As explained previously [8], when the NGR is inactive (Figure 3.5(a)), it does not block the flow of minority carriers and the effective distance the minority carriers have to travel in the base (substrate) is smaller ($W_B \approx d_{N\text{-}well}$) than in the case when the NGR is active (Figure 3.5(b)), in which case, as illustrated, the minority carriers should bypass the NGR to reach the victim's N-well. The increase in the distance travelled by the minority carriers when the NGR is active would translate to an increase in effective base width by roughly twice the well depth ($W_B \approx d_{N\text{-}well} + 2d_{Well}$). In this technology, with the NGR active, the effective base width of Q_1 increased roughly by 1.7μm ($d_{Well} \approx 0.85\mu m$).

3.3 Variation of f_{3dB} with W_B

With the behavior of α_0 and τ_B understood, the variation of f_{3dB} with W_B can be plotted using equation (3.7). From Figure 3.6, it can be seen that f_{3dB} decreases rapidly initially, and then for larger base widths it tends to saturate. Intuitively this trend can be understood by studying the variation of charge stored in the base as W_B is increased. The amount of charge stored in the base would influence the bandwidth or f_{3dB} of the transistor (since stored charge directly influences the diffusion capacitance), and by

understanding how the charge stored in the base varies with W_B, the variation of f_{3dB} with W_B can be justified. By integrating the expression for base minority charge distribution in [17], an expression for charge stored in the base can be obtained:

$$Q_B = n_{b0}(e^{\frac{qV_{BE}}{KT}} - 2)L_n \tanh\left(\frac{W_B}{2L_n}\right) \tag{3.11}$$

V_{BE} is the base emitter bias, n_{b0} is the thermal equilibrium minority carrier concentration in the base and L_n is the minority carrier diffusion length. Equation (3.11) has been normalized and plotted in Figure 3.7. It can be observed that Q_B rapidly increases for small W_B ($<2L_n$) and then saturates for large W_B. As Q_B increases, the diffusion capacitance would increase and the f_{3dB} bandwidth of the transistor should decrease, and when Q_B saturates for larger W_B, f_{3dB} should follow the same trend and saturate. As illustrated in Figure 3.6, this expected trend is observed for f_{3dB}.

It should be noted that equation (3.11) is an accurate representation of the dependence of Q_B on W_B. On the other hand, for modeling purposes, in this work Q_B is approximated to the expression in equation (3.2). Equation (3.2) is valid only for relatively small W_B (less than ~$3L_n$). For large W_B, Q_1 would no longer behave as a BJT and equation (3.2) would not be valid. However, for large W_B (i.e. large d_{victim}) the collected current by the victim would be very small and external latchup susceptibility would be extremely small. Hence the model for Q_B presented in this work would be sufficient to model the transient properties of external latchup.

3.4 Effect of NGR on f_{3dB}

From the trend observed for the variation of f_{3dB} with W_B, the effect of NGR on f_{3dB} can be justified. The structure with a 90° victim orientation and d_{victim}=4µm has an f_{3dB} of 1450 kHz and 850 kHz with the NGR inactive and active respectively (Figure 3.3). When the NGR is active, the effective base width is increased by $2d_{Well}$ (1.7µm) as explained previously; now from Figure 3.6 it can be observed that around W_B=4µm, f_{3dB} is still decreasing with increase in W_B and has not yet saturated. Hence in this case, a significant change in f_{3dB} is observed with the NGR active, since with the NGR active, W_B would increase by 1.7µm, which would translate to a decrease in f_{3dB}. On the other hand, for the structures with d_{victim}=12µm, 22µm, even though an active NGR increases the effective base width by $2d_{Well}$ (1.7µm), the f_{3dB} does not change significantly (Figure 3.3) since from Figure 3.6 it can be seen that beyond W_B=10µm, f_{3dB} is no longer very sensitive to small changes in base width.

3.5 Effect of orientation on f_{3dB}

The effect of orientation on transient ex-LU during negative I-test was illustrated in Figure 2.10. For a fixed value of d_{victim} (4µm), the test structure with o_{victim}=90° has an f_{3dB} of 850 kHz; on the other hand, the test structure with o_{victim}=180° has an f_{3dB} of 190 kHz which is significantly smaller. In the latter case, since the f_{3dB} is considerably smaller, this indicates that even though the distance of the N-well from the aggressor is the same for both the orientations, the effective base width of Q_1 is larger for the 180° victim orientation when compared to the 90° victim orientation. For o_{victim}=90°,

$W_B \approx d_{N\text{-well}} \approx d_{victim}$ since the minority carrier current that travels only a distance of $d_{N\text{-well}}$ before being collected by NW_2 (see the dotted arrows in Figure 3.8(b)) will help forward bias the p^+/NW_2 junction and trigger latchup. From the illustration in Figure 3.8(a) it can be seen that as explained in [8], for o_{victim}=180°, not all the minority carrier current that is collected by the victim aids in triggering latchup. As shown, the portion of the current which triggers latchup travels a longer distance through the substrate for this victim orientation, and hence Q_1 will have a larger effective base width when compared to the o_{victim}=90°. It was estimated that for the test structure with d_{victim} = 4μm, the effective base width (W_B) for o_{victim}=180° should be close to 20μm. It was found that, for o_{victim}=180°, W_B can be approximated to be equal to $d_{victim}+d_{TAP}/2$. For o_{victim}=0°, W_B can be approximated to be equal to $d_{N\text{-well}} = d_{victim}+d_{TAP}$ and f_{3dB} is expected to be small.

3.6 Effect of temperature on f_{3dB}

In Figure 3.9 the dependence of I_{trig} on T_{PW} has been plotted for two different temperatures. It can be observed that, as explained in [12], I_{trig} is smaller at the higher temperature. Moreover, it was found that there was no significant change in f_{3dB} when the temperature was changed.

3.7 Negative I-test transient ex-LU circuit simulation

In [10] a circuit level model to simulate negative I-tests has been described and parameter extraction procedures for the different components for a DC simulation were explained. In order to include the transient effects, base transit time for Q_1, which has been modeled in this work, should also be included. Once τ_B is included in the circuit

simulation, the I_{trig} vs. T_{PW} trend observed in the measurement data can be simulated in the circuit simulator. In this work Spectre was used to simulate negative I-test transient ex-LU and the circuit schematic used is shown in Figure 3.10. In Figure 3.11, the circuit simulation results are plotted along with the measurement data and a good match can be observed.

3.8 Figures

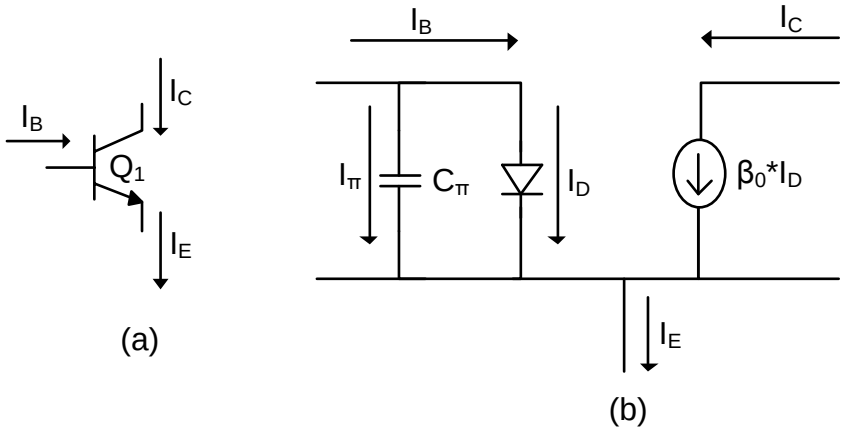

Figure 3.1: (a) BJT Q_1 with collector, base and emitter current labeled. (b) Expressing $I_C=\beta_0 I_D$ and including C_π (base charging capacitance). I_D represents the current through the base-emitter PN junction.

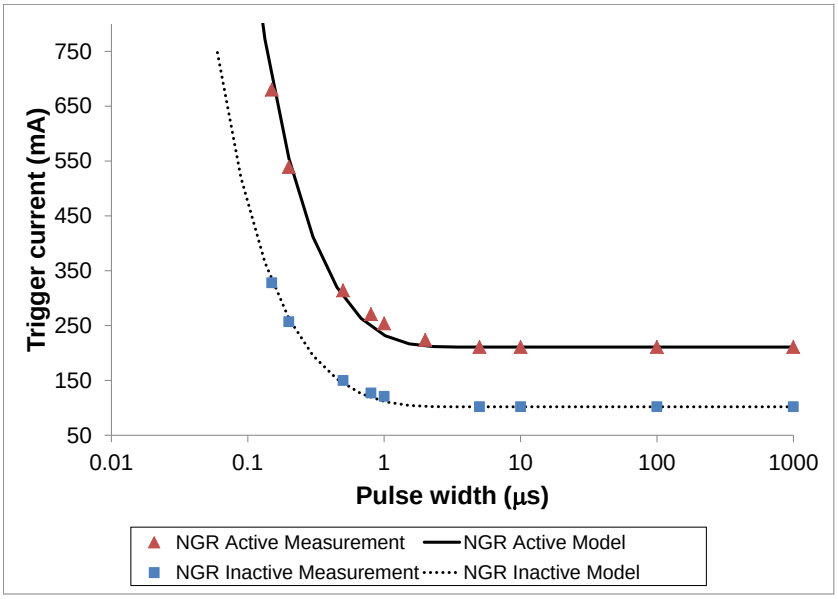

Figure 3.2: I_{trig} vs. T_{PW} for negative I-test, o_{victim}=90˚ with d_{victim}=12µm. Symbols represent the measurement data and lines represent the single pole model. With NGR inactive f_{3dB}=390 kHz. With NGR active f_{3dB}=380 kHz.

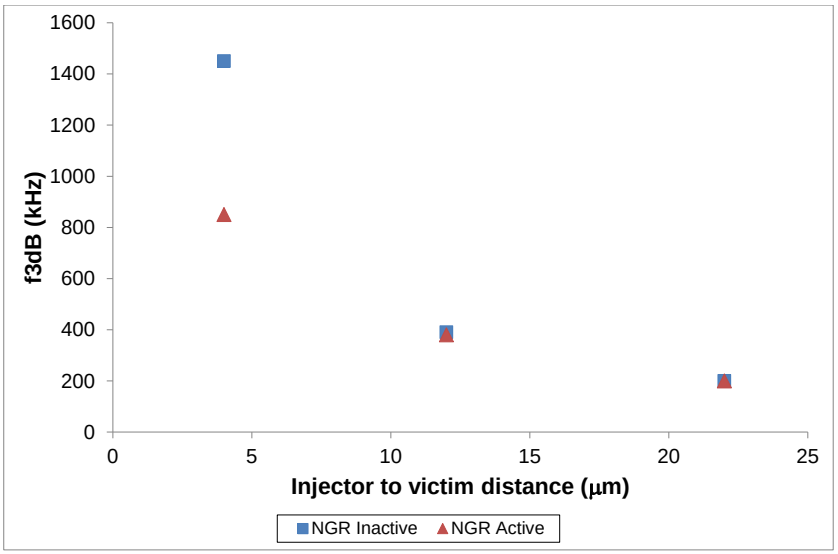

Figure 3.3: Variation of f_{3dB} with d_{victim} for o_{vcitim}=90˚.

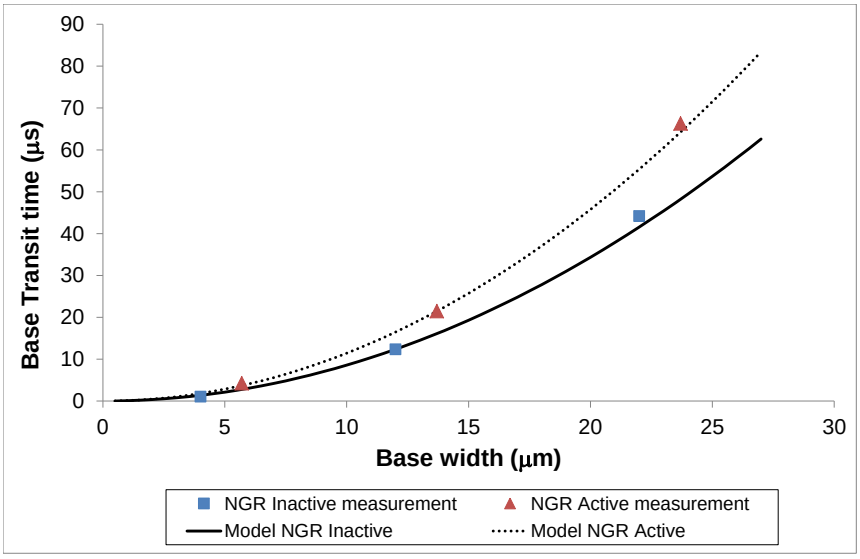

Figure 3.4: Base transit time (τ_B) vs. base width (W_B) for o_{victim}=90°. Symbols represent the measurement data and lines represent the model.

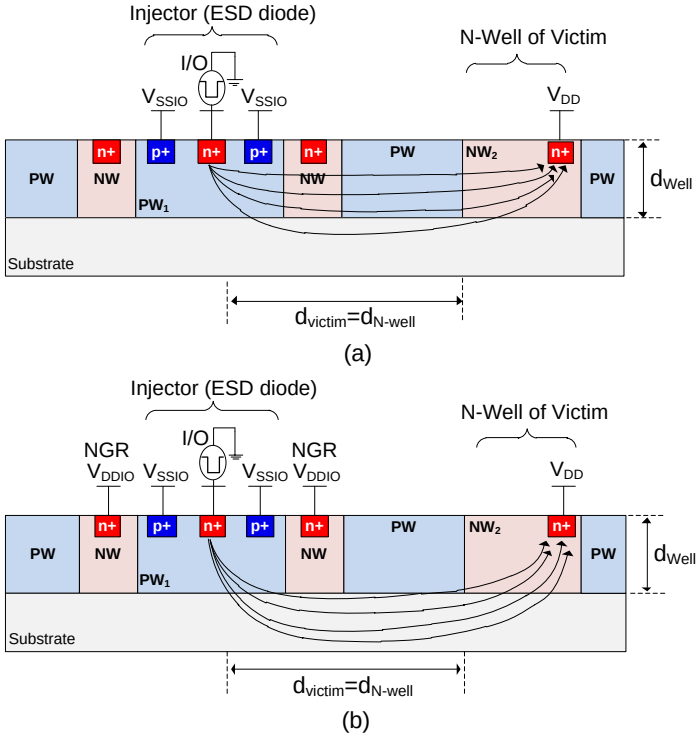

Figure 3.5: Effect of NGR on the minority carrier flux between the aggressor and victim. Flux is illustrated using solid lines. Only the current collected by NW_2 has been illustrated. d_{Well} is the N-well/P-well depth. (a) NGR inactive. (b) NGR active.

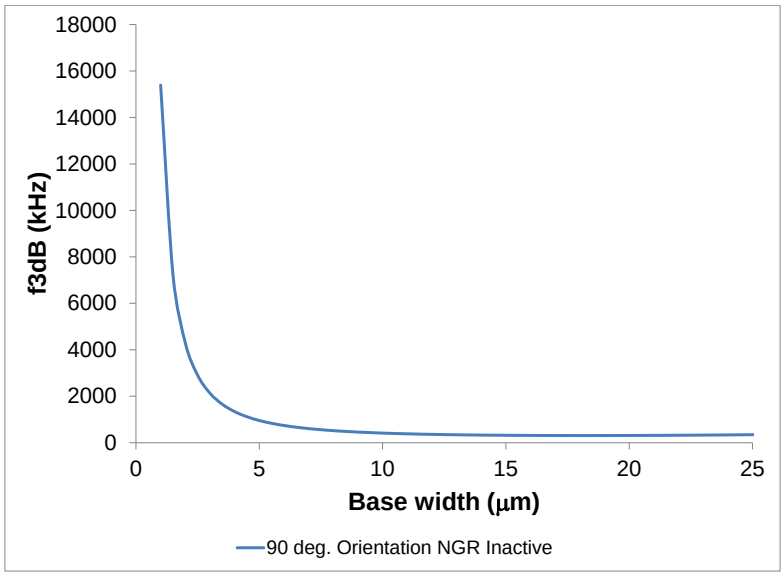

Figure 3.6: Variation of f_{3dB} with base width (W_B). o_{victim}=90°.

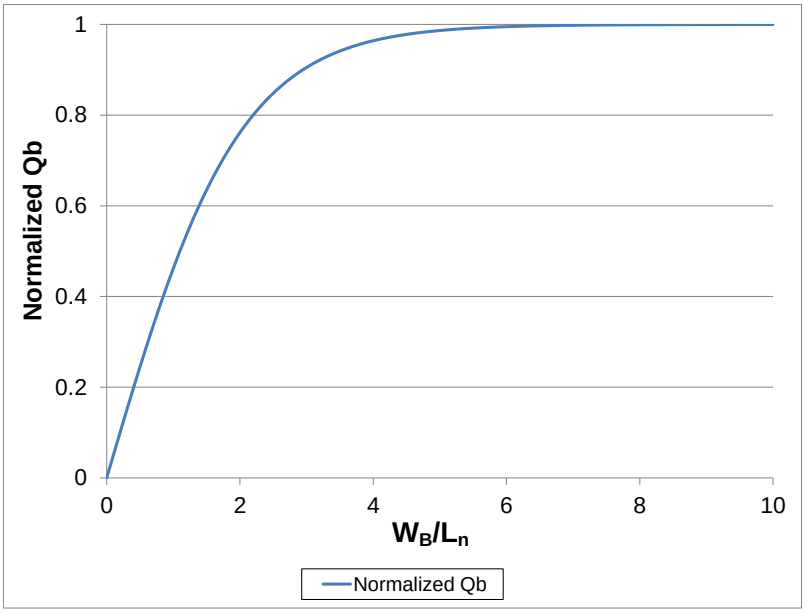

Figure 3.7: Normalized Q_B vs. W_B/L_n.

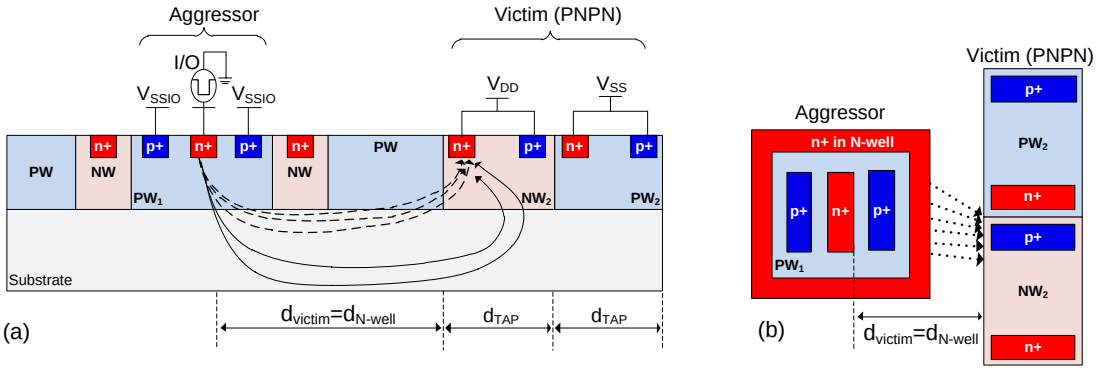

Figure 3.8: (a) o_{victim}=180°. Minority carrier flux between the aggressor and victim. Only the carriers collected by NW_2 are illustrated. The solid lines represent the portion of the current that lowers the N-well potential in the vicinity of the p^+ diffusion and thus leads to latchup being triggered at the victim. (b) o_{victim}=90°. Minority carrier flux between the aggressor and victim is represented by dotted arrows.

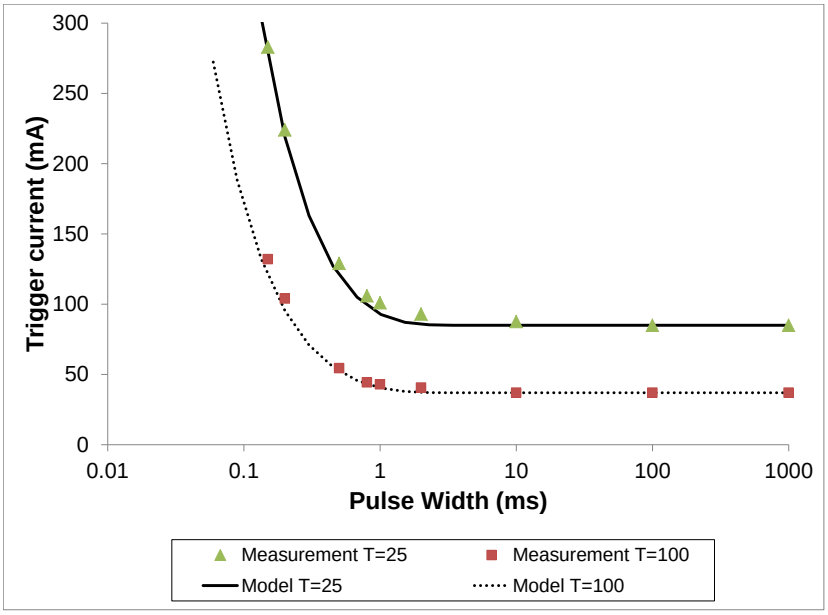

Figure 3.9: I_{trig} vs. T_{PW} for negative I-test at 25℃ and 100℃. o_{victim}=90°, d_{victim}=12µm and NGR inactive. Single pole model plotted along with measurement data. f_{3dB}=390 kHz at both temperatures.

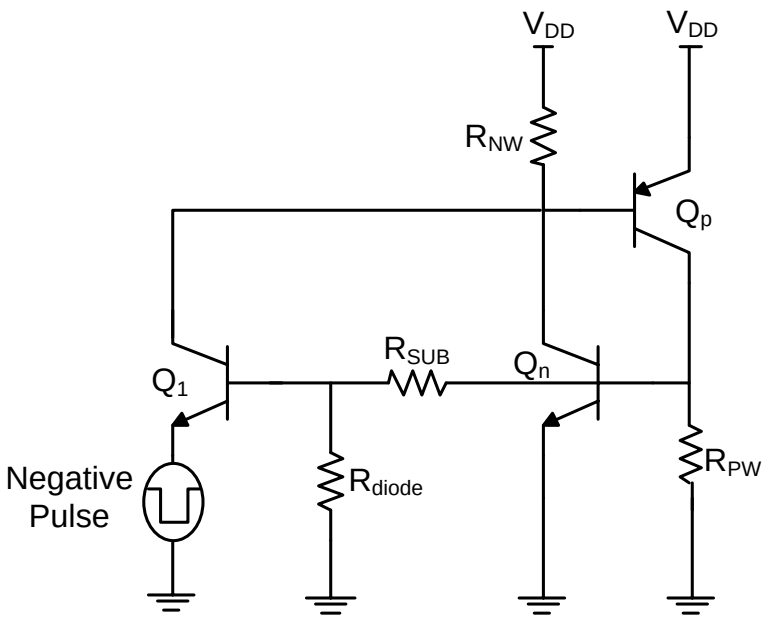

Figure 3.10: Negative I-test ex-LU circuit schematic including parasitic components.

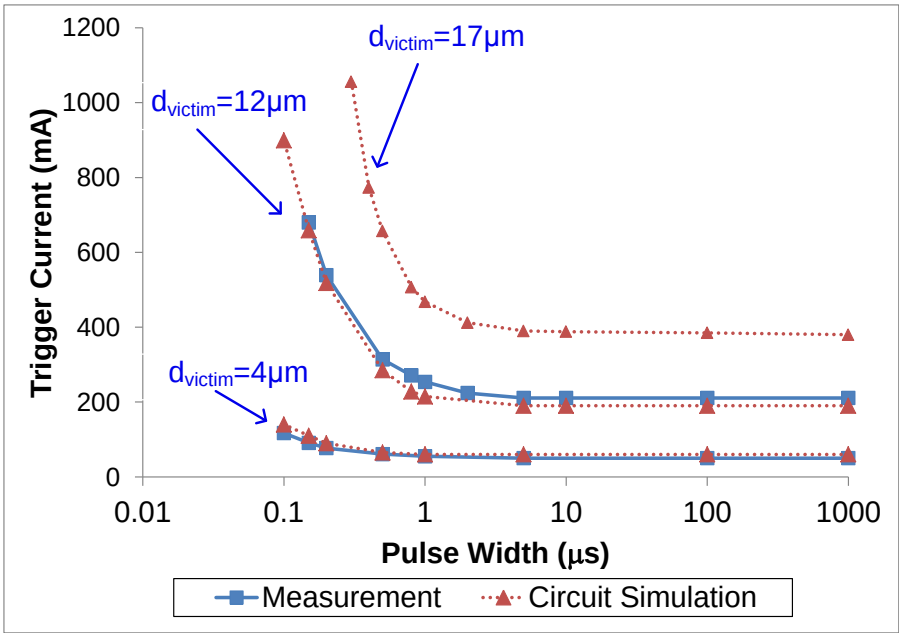

Figure 3.11: $I_{trig}(T_{PW})$ from measurements and circuit simulation. o_{victim}=90°.

CHAPTER 4: STANDARD CELL LAYOUT BASED PNPN

4.1 Holding voltage

Figure 1.2 shows the layout of the test structures used in [3],[4],[7],[8],[10]; such test structures are traditionally used to characterize latchup. Note that the four diffusion stripes defining the victim PNPN are all co-linear. In Figure 4.1(b) the current/voltage characteristics of the standard cell layout type PNPN (Figure 1.3(b)) are compared with those of the traditional PNPN (Figure 1.2). To obtain the I-V curves, the cathode and P-well are at V_{SS}, N-well is at V_{DD} and the anode current is ramped. Both I-V curves show two NDR (negative differential resistance) regions; once the PNPN is triggered, Q_n turns on and as the current through the PNPN is increased, the current through Q_n steadily increases and the voltage across the PNPN drops (initial NDR region). Once the current through Q_n is large enough for the overall loop gain to become larger than unity, the PNPN would fully turn on (snap back) to enter its low impedance state.

It can be seen that the trigger voltage and trigger current are larger for the standard cell layout type PNPN than for the traditional PNPN; this can be attributed to the difference in R_{NW} and R_{PW} for the two structures. The traditional PNPN had a slightly larger R_{NW} and R_{PW}, which can explain the smaller V_{t1} and I_{t1} observed for this case. Even though both structures have the same d_{TAP} and d_{AC}, they can have different R_{NW} and R_{PW} since these resistors depend on the current flow path during the PNPN turn-on [2]. It can be seen from Figure 1.2 that for the PNPN with the traditional layout, the anode and cathode are parallel to the N-well/P-well junction; on the other hand, from Figure 1.3(b)

it can be observed that for the standard cell layout type PNPN, the anode and cathode are not parallel to the N-well/P-well junction. This will result in a different current flow path in the parasitic NPN and PNP transistors in the two PNPNs, leading to a difference in the measured R_{NW} and R_{PW}.

The vital difference between the two I-V curves in Figure 4.1 is that the two PNPNs show significantly different holding voltage (V_h) in spite of the fact that both of them have the same d_{TAP} and d_{AC}. The standard cell layout type PNPN has a V_h=1.8V and the traditional PNPN has a V_h=1.1V. This would indicate that the standard cell layout type PNPN would always remain in its high impedance state if the V_{DD}<1.8V; on the other hand, for the traditional PNPN, V_{DD}<1.1V would be the condition for it to always remain in its high impedance state. In this technology, the V_{DD} for the core domain is 1.2V and 3.3V for the I/O domain. Hence, the parasitic PNPNs in the core circuitry with the standard cell type layout would not be susceptible to latchup (since $V_{DD}<V_h$); whereas the parasitic PNPNs with the traditional layout could latch up (since $V_{DD}>V_h$). On the other hand, in the I/O domain, parasitic PNPNs with either layout type would be susceptible to latchup since $V_{DD}>V_h$ for both the PNPNs.

4.2 Modeling the change in V_h

There are many parameters that affect V_h [2], but it was found that R_{W1} and R_{W2} (Figure 4.1(a)) had the most significant influence on V_h. By changing R_{W1} and R_{W2}, the holding point (V_h, I_h) could be calibrated to match the measurement data. The trigger point (V_{t1}, I_{t1}) was calibrated by making sure that R_{NW} and R_{PW} in the simulation matched

the measured values. In Figure 4.2 (single PNPN simulation) it can be seen that the trigger and holding points in the simulation match the measurement results; however, it can be observed that the R_{on} for the single PNPN simulation is different when compared to the measurement data.

To accurately model the change in V_h in the standard cell layout type PNPN, the reason for the change in R_{W1} and R_{W2} should be first understood so that it can be accurately represented in the circuit simulation. For the traditional PNPN (Figure 1.2), it can be seen that the anode and cathode are parallel to the N-well/P-well junction, and for simulation purposes it can be represented by a single PNPN with a constant d_{AC}. On the other hand, from Figure 4.3 it can be seen that for the standard cell layout type PNPN, the anode and cathode are not parallel to the N-well/P-well junction. Hence, as we move away from the N-well/P-well junction, the d_{AC} increases; therefore, this PNPN structure cannot be modeled accurately by a single PNPN, but needs to be modeled by multiple PNPNs in parallel, each with a different d_{AC} as illustrated. Clearly $PNPN_1$ would be the first to trigger since it has the smallest d_{AC}; this would be followed by the other PNPNs triggering. The distributed PNPN circuit schematic has been illustrated in Figure 4.4. $PNPN_1$ would govern the trigger and holding point. The trigger point can be calibrated by ensuring the correct measured values for R_{NW} and R_{PW} are used. To calibrate the holding point it is important to include R_{W1} and R_{W2}. R_{W1} (R_{W2}) represents the resistance between the base region of Q_p (Q_n) and the point where the current is collected by Q_n (Q_p). This resistance would depend on the distance between the anode and cathode, d_{AC}, and cross-sectional area of the anode and cathode.

It can be seen from Figure 4.3 that in spite of $PNPN_1$ having the same d_{AC} as the traditional PNPN layout, the cross-sectional area of the anode and cathode is much smaller. The cross-sectional area in this case would be governed by W_{DIFF} (1μm), which is much smaller when compared to the cross-sectional area of the anode and cathode in the traditional PNPN case, which is governed by L_{DIFF} (20μm) (Figure 1.2). As we move away from the N-well/P-well junction, the R_{W1} and R_{W2} of the PNPNs would increase and the β of the parasitic NPN and PNP transistors which form the PNPNs would decrease. In this work, a distributed PNPN was simulated with five PNPN in parallel and the simulation results can be seen in Figure 4.2. With a single PNPN, the trigger and holding points can be calibrated, but R_{on} will not match the measured R_{on} since R_{W1} and R_{W2} affect not only the holding point, but also R_{on}. On the other hand, with a distributed PNPN structure, the trigger and holding points can be calibrated by calibrating parameters of $PNPN_1$, and R_{on} can be calibrated by adding PNPNs in parallel with $PNPN_1$. Once $PNPN_1$ is triggered, it would in turn trigger $PNPN_2$; $PNPN_2$ would trigger $PNPN_3$ and so on. As the PNPNs, which are in parallel with each other, are triggered into their low impedance state, the overall R_{on} would reduce and hence R_{on} can be calibrated to match the measured value.

It should be noted that for simulating external latchup, it is sufficient to represent the standard cell layout type PNPN with a single PNPN, with the trigger and holding points calibrated, since R_{on} of the PNPN does not influence the external latchup trigger current.

4.3 External latchup characteristics

In order to study external latchup with a standard cell layout type victim, test structures with four different victim orientations were fabricated. In Figure 4.5 and Figure 4.6 the test structures used to study positive I-tests and negative I-tests are illustrated, respectively. All structures have the same aggressor to victim distance (4μm). The supply voltage V_{DD} is fixed to 2.5V.

4.3.1 Positive I-test

In Figure 4.7 the positive I-test DC I_{trig} for the four orientations has been plotted. It can be seen that the orientation of the victim influences latchup susceptibility. As explained previously [12], this effect is due to the current flow path of the majority carriers in the substrate for the four different victim orientations. If a larger portion of the current collected by the P-well of the victim aids in raising the potential near the cathode (n^+ in P-well), then that would result in an increase in latchup susceptibility and lower I_{trig}. Moreover, with the PGR active, I_{trig} increases, but for the o_{victim}=90°, external latchup could not be triggered with the PGR active. The reason for this can understood from Figure 4.5(c); it can be seen that the PGR around the aggressor is adjacent to the cathode and hence with the PGR active, the substrate potential around the cathode would be pinned to V_{SS} and it would be very hard to raise the potential in the vicinity of the cathode to forward bias the n^+ in PW_1 PN junction. Hence with the PGR active, latchup could not be triggered for this victim orientation.

4.3.2 Negative I-test

In Figure 4.8 the negative I-test DC I_{trig} for the four orientations has been plotted. The orientation effect is also observed for the negative I-test. As seen in the figure, the I_{trig} values for o_{victim}=90° and o_{victim}=180° indicate unusual behavior. For o_{victim}=90° in Figure 4.6(c), latchup could not be triggered at the victim. As the current through the aggressor was increased, the aggressor-victim PNPN formed by PW_1, n^+ in PW_1, p^+ in NW_2 and NW_2 was triggered into its low impedance state. This victim orientation has the smallest distance between the n^+ in PW_1 and p^+ in NW_2, making this aggressor-victim parasitic PNPN susceptible to being triggered into its low impedance state. Once the aggressor-victim PNPN is triggered into its low impedance state, most of the injected current flows through this PNPN. The current flowing between n^+ in PW_1 and p^+ in NW_2 (anode and cathode of the aggressor-victim PNPN) does not result in latchup being triggered at the victim. It should be noted that the aggressor-victim parasitic PNPN returns to its high impedance state once the trigger source is removed.

A similar behavior was observed for o_{victim}=180°; but in this case, apart from the aggressor-victim PNPN being triggered, the PNPN formed by the victim was also triggered.

For o_{victim}=0° and 270°, the n^+ in PW_1 and p^+ in NW_2 are far apart and hence the aggressor-victim PNPN is not triggered and external latchup is triggered in the usual fashion.

Whether or not the victim PNPN is triggered during the negative I-test would depend on the whether or not the victim NPN, Q_n (Figure 3.10), turns on. As more and more current is injected by the aggressor, a portion of it will flow through R_{NW} and eventually the base-emitter junction of Q_p would get forward biased. This would turn on Q_p, which would result in current flowing through Q_p's collector terminal. A portion of this collector current will flow through R_{PW} and the rest through R_{SUB}. If the current flowing through R_{PW} is sufficiently large to forward bias the base-emitter PN junction of Q_n, then latchup will be triggered at the victim. However, if R_{SUB} has a very small value, most of Q_p's collector current will flow through R_{SUB} and there would not be sufficient current flowing through R_{PW} to turn on Q_n and hence latchup would not be triggered at the victim. Therefore the ratio of R_{SUB} to R_{PW} would significantly influence external latchup susceptibility. Hence, to simulate external latchup in a circuit simulator using the schematic shown in Figure 3.10, apart from using accurate models for Q_n, Q_p and Q_1 and accurate values for R_{NW} and R_{PW}, it would be important to use an accurate value for R_{SUB}. From Figure 4.6 it can be seen that the p+ in NW_2 is at a different distance from the aggressor for each of the four different orientations. Therefore R_{SUB} for each victim orientation would be different. R_{PW} on the other hand is determined by the tap spacing in the PNPN, which is a constant. Hence the ratio of R_{SUB} to R_{PW} would be different for the four different orientations, resulting in the difference in external latchup susceptibility.

4.3.3 Transient external latchup

Transient latchup testing on structures with standard cell layout type PNPN victim resulted in a trend in the variation of I_{trig} with T_{PW} similar to that seen with the traditional

PNPN victim. From Figure 4.9 it can be seen that for the positive I-test, no significant variation in I_{trig} is observed as T_{PW} is varied, and for the negative I-test, I_{trig} increases as T_{PW} is decreased. The transient ex-LU data shown was obtained using test structures with o_{victim}=0° (Figure 4.5(a) and Figure 4.6(a)).

For the measurement data shown for the negative I-test, equation (3.9) in Chapter 3 was used to model the dependence of I_{trig} on T_{PW}, and the f_{3dB} for this structure was found to be 185 kHz. It can be seen from Figure 4.6(a) that for the 0° victim orientation, the PW_2 is closer to the aggressor and NW_2 is farther away from the aggressor. For this particular structure, the distance of the NW_2 from the aggressor is 24μm. The base width W_B of the NPN transistor Q_1 (Figure 3.10) formed by the n^+ in PW_1, PW_1 and NW_2 would roughly be equal to the distance of NW_2 from the aggressor ($W_B \approx 24\mu m$). It can be seen from Figure 3.3 that the f_{3dB} (185 kHz) for this structure with the standard cell layout type PNPN, corresponds well with the f_{3dB} observed for the structure with Q_1 having a similar W_B, i.e. 22μm, but with the victim having a traditional PNPN layout. Hence, the same modeling technique described in the previous sections to model transient ex-LU for structures with PNPNs having a traditional layout can be used to model transient ex-LU for structures with PNPNs having a standard cell type layout.

4.4 Figures

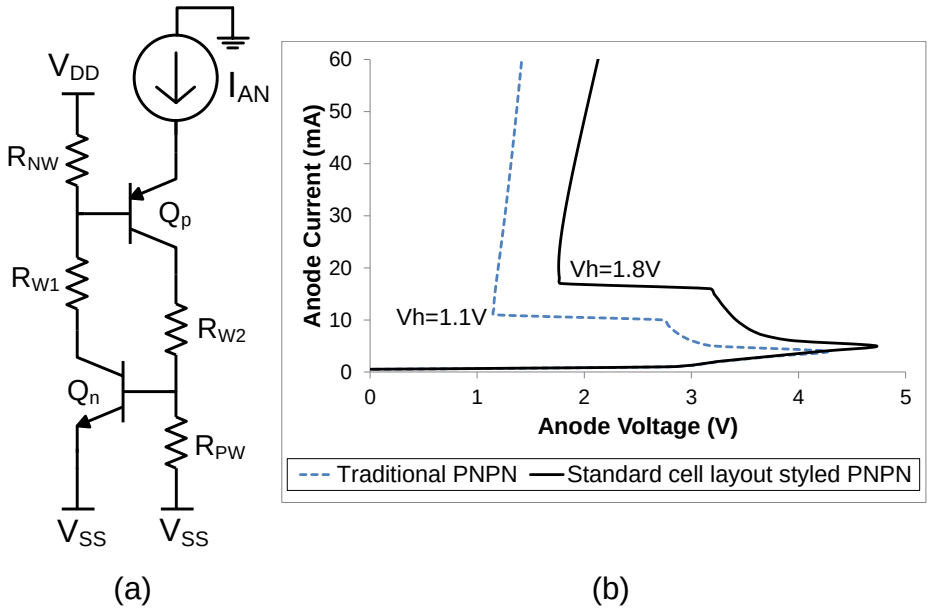

Figure 4.1: (a) Illustration of the test performed to obtain the current/voltage characteristics of the two PNPNs. (b) Measurement data. The "traditional PNPN" layout is illustrated in Fig. 1. V_{DD}=2.5V, V_{SS}=0V.

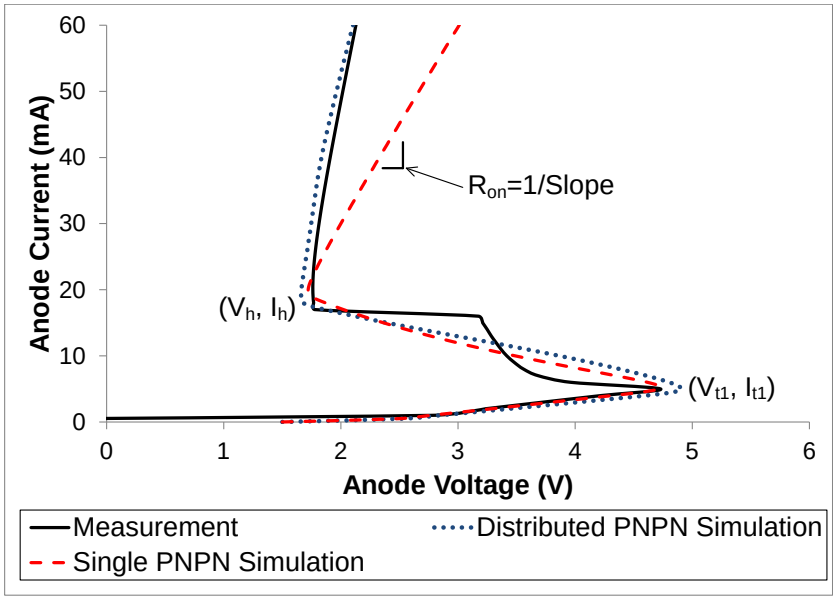

Figure 4.2: Simulation vs. measurements for a standard cell layout styled PNPN.

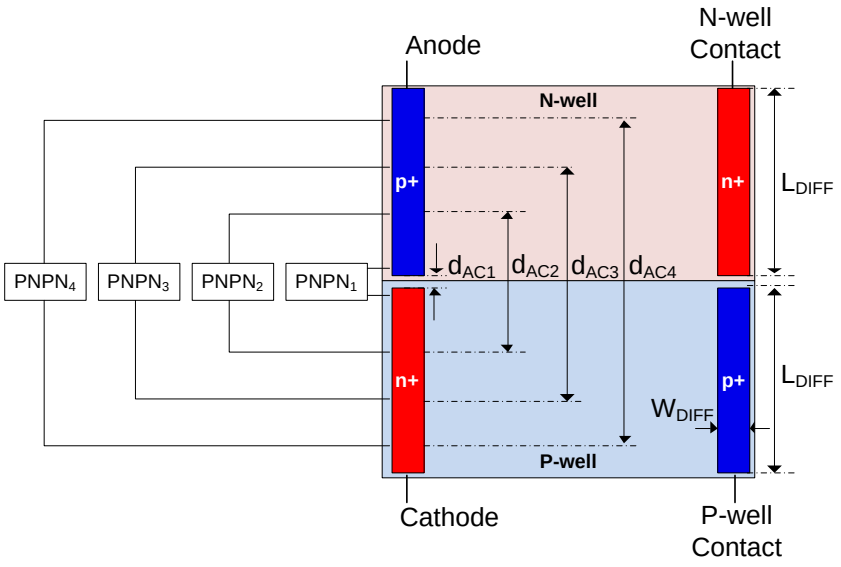

Figure 4.3: Standard cell styled PNPN, with illustration of how anode to cathode spacing (d_{AC}) varies across the stripe width L_{DIFF}. This suggests the device be modeled as a distributed PNPN.

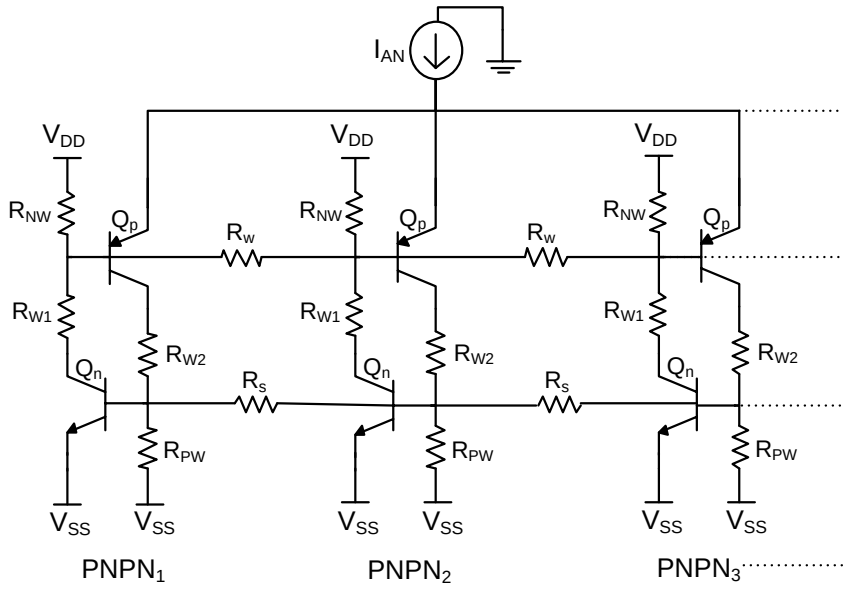

Figure 4.4: Schematic of the distributed PNPN used to simulate the behavior of the standard cell styled PNPN.

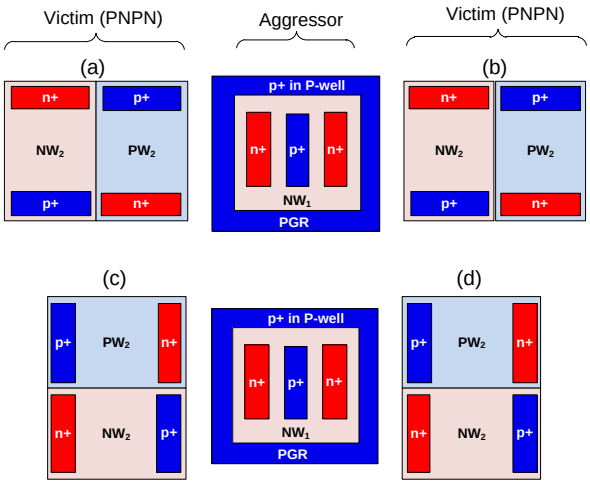

Figure 4.5: Layout view of test structures used for positive I-tests. Each test structure consists of a victim (standard cell layout type PNPN) and an aggressor (N-well ESD diode) with a constant distance between aggressor and victim (4µm). Four different victim orientations are illustrated: (a) o_{victim}=0° with the P-well of the victim closer to the aggressor. (b) o_{victim}=180° with the N-well of the victim closer the aggressor. (c) o_{victim}=90° with the anode and cathode of victim closer to the aggressor. (d) o_{victim}=270° with the N-well and P-well contacts of victim closer to the aggressor.

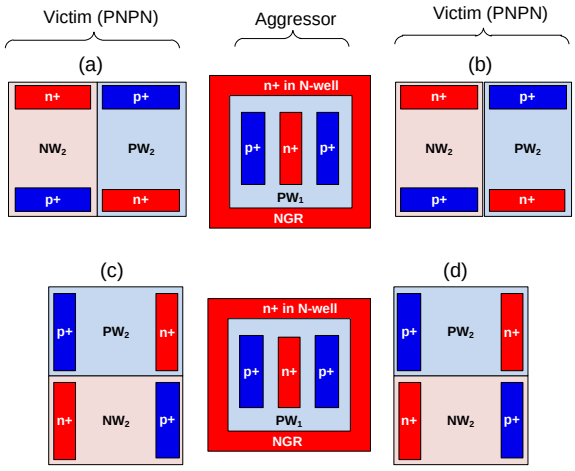

Figure 4.6: Layout view of test structures used for negative I-tests. Each test structure consists of a victim (standard cell layout type PNPN) and an aggressor (P-well ESD diode) with a constant distance between aggressor and victim (4µm). Four different orientations are illustrated: (a) o_{victim}= 0° with the P-well of the victim closer to the aggressor. (b) o_{victim}=180° with the N-well of the victim closer the aggressor. (c) o_{victim}= 90° with the anode and cathode of victim closer to the aggressor. (d) o_{victim}=270° with the N-well and P-well contacts of victim closer to the aggressor.

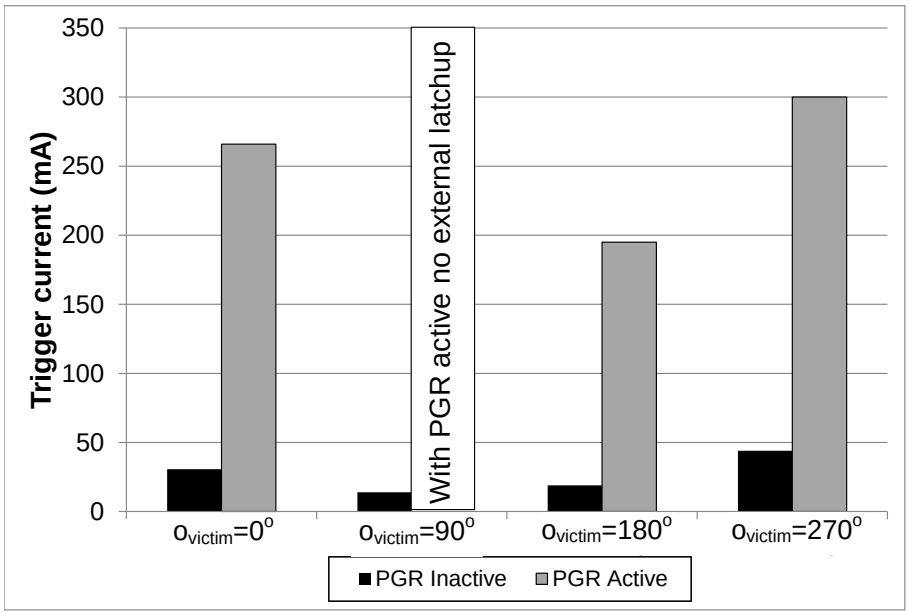

Figure 4.7: Positive I-test DC I_{trig} for 4 victim orientations (standard cell layout type PNPN). Black bars represent I_{trig} with PGR inactive and grey bars represent I_{trig} with PGR active.

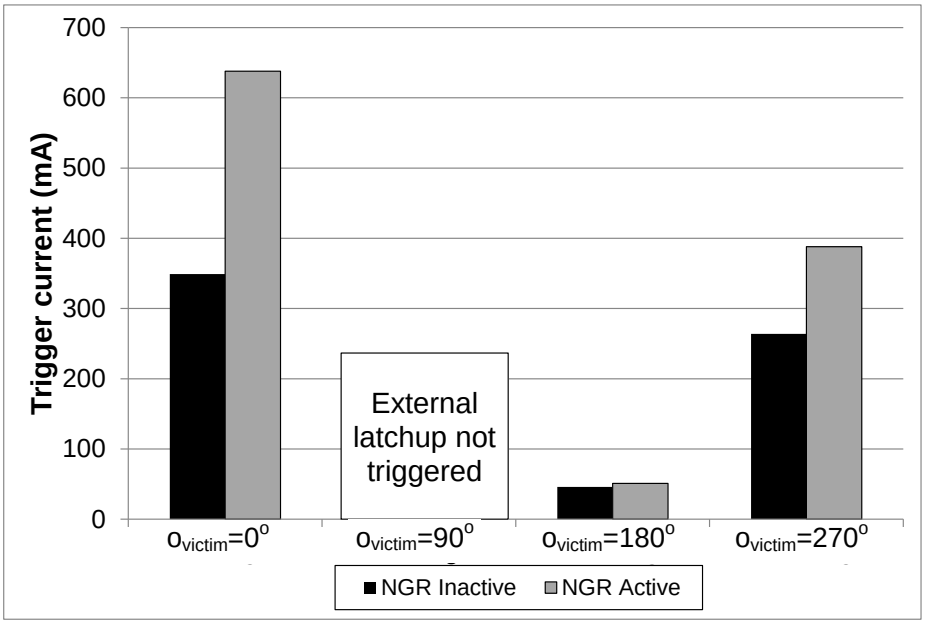

Figure 4.8: Negative I-test DC I_{trig} for 4 victim orientations (standard cell layout type PNPN). Black bars represent I_{trig} with NGR inactive and grey bars represent I_{trig} with NGR active.

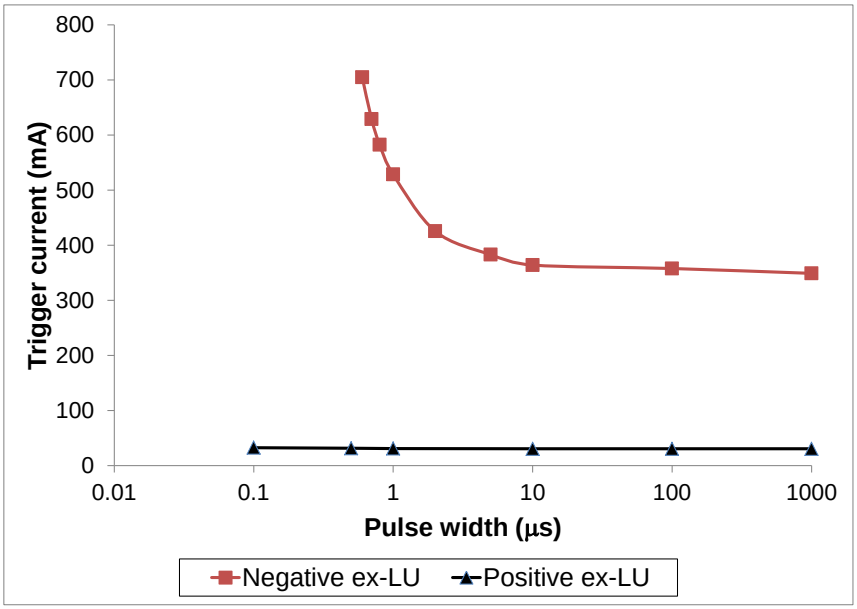

Figure 4.9: I_{trig} vs. T_{PW} for a standard cell layout styled victim. o_{victim}=0°. V_{DD}=V_{DDIO}=2.5V. Guard rings inactive.

CHAPTER 5: SUBSTRATE NOISE COUPLING

In modern mixed-signal ICs, limiting the noise coupling from the digital to the analog circuits is important. The semiconductor substrate shared by the analog and digital circuits is one of the important media through which noise is coupled [18]. The noise generated by the digital circuits, which are constantly switching, spreads through the substrate and causes substrate potential variations in the vicinity of sensitive analog devices. The coupled noise is typically weak, but it can degrade the performance of sensitive low noise amplifiers, local oscillators, etc. Many noise isolation strategies have been reported [18]-[20] and the use of guard rings is one of the most commonly used method to reduce noise coupling.

When comparing different guard ring topologies, previous studies have not ensured that the total Si area allocated for the guard rings was constant [19]-[21]. The push for lower cost, smaller size, and more features forces designers to minimize the area consumed by the SOCs. Since guard rings could consume a significant amount of Si area, it is important to study the area efficiency of different guard ring topologies. In this work, the area consumed by the different guard ring designs is held constant and their effectiveness is compared.

5.1 Area efficiency of guard rings

In this study, several different guard ring topologies have been compared. Each test structure consisted of two substrate contacts, each measuring 10μm x 10μm, which are 60μm apart (center to center). The second port is surrounded by the guard ring or

Table 1: Guard ring topologies

Case	Guard Ring 1	Guard Ring 2
1	PGR (12μm)	
2	PGR (2μm)	NGR (10μm)
3	PGR (10μm)	NGR (2μm)
4	PGR (2μm)	P-well block (10μm)
5	PGR (2μm)	Deep N-well (10μm)

combination of two guard rings. The test structure layout is illustrated in Figure 5.1. The sum of the widths of guard ring 1 and guard ring 2 is fixed to 12μm. The different guard ring topologies compared in this study are listed in Table 1. In the table, PGR stands for P-well guard ring and NGR stands for N-well guard ring. P-well block refers to blocking the P-well dopants resulting in a region of high resistivity, assuming a high resistance substrate has been used. The cross-section of case 5 is illustrated in Figure 5.2. Apart from these five topologies, two other test structures were included. One was used as a reference case, with no guard rings around either the aggressor or the victim. The other test structure consisted of a PGR around both the aggressor and the victim, each with a width of 2μm (Figure 5.3).

Two GSG probes, one at the aggressor and one at the victim, are used to take the measurements and the PGRs are connected to the ground potential on chip. The NGR and the deep N-well are biased at V_{DD} (1.5V) using an additional probe. Using a network analyzer, the S-parameters for each of the test structure were measured. S_{21} (forward voltage gain) is plotted in Figure 5.4. Port 1 is the aggressor and Port 2 is the victim. It

would be desirable to have a very small S_{21}, which would indicate a good level of noise isolation. It should be noted that for all the cases, the S_{21} plotted in dB has a negative value.

As expected, the reference case, with no guard rings, has the largest value of S_{21} indicating poor noise isolation. It can also be observed that the case with the PGR around both the aggressor and the victim has the lowest value of S_{21}, indicating very good noise isolation between the two ports. It should be noted that even though, in this case, there is a guard ring around both the aggressor and the victim, they are each just 2μm wide. On the other hand, in all the other cases, with the guard rings around the victim alone, the total width of the guard ring is 12μm, which is significantly larger, even in terms of total area consumed. Hence the case with the PGR (2μm) around both the aggressor and the victim was found to be the most area efficient guard ring topology. The reason for this can be explained by understanding how PGRs improve noise isolation. PGRs reduce substrate noise coupling by presenting a low impedance path to ground, to the substrate current. Depending on the width of the PGR, a portion of the substrate current is collected by it. If the PGR is around the aggressor, it reduces the substrate noise coupling by collecting a portion of the substrate current injected by the aggressor. On the other hand, if the PGR is around the victim, it improves noise isolation by maintaining the substrate potential in the vicinity of the victim close to V_{SSA} (analog ground rail potential) by acting as a sink for the substrate current. One would expect the noise isolation to improve linearly with the width of the PGR; however, as shown in [22], the noise isolation improves as a logarithm of the width. Hence, beyond a certain width, it is no

longer beneficial to increase the width of the PGR in order to improve noise isolation. However, by having PGRs around the aggressor and the victim, the amount of injected substrate current is reduced by the PGR around the aggressor, and the PGR around the victim collects a portion of any remaining substrate current, hence resulting in the best level of noise isolation when compared to the other guard ring topologies.

Of the five cases listed in Table 1, it can observed that the case with P-well block (10μm) surrounding the PGR (2μm) provides the least noise isolation. The other four cases are plotted separately in Figure 5.5. From Figure 5.5 it can be seen that around 1 GHz, the S_{21} for the structures with the NGRs and deep N-well guard rings show distinct peaks in the S_{21} vs. frequency plots. This is similar to the phenomenon observed during LC resonance. It was found that the probe used to bias the NGR and deep N-well had an inductance L_P of around 2nH which resonated with N-well (deep N-well) to substrate junction capacitance (C_{NW}) at around 1 GHz (see Figure 5.6). Beyond the resonant frequency, the impedance of the inductance of the probe would dominate and the N-well (deep N-well) would no longer be at AC ground.

NGRs are capacitively coupled to the substrate; the N-well to substrate junction capacitance (C_{NW}) would typically be in the range of hundreds of femtofarads, which would translate to a relatively large series impedance, especially at lower frequencies. Hence NGRs are not expected to be very effective as a current sink for substrate noise at low frequencies. However, as explained in [23], NGRs help in reducing the substrate noise coupling by blocking the flow of majority carriers and forcing it through the

relatively high-resistance bulk. As described earlier, in the experiments presented in this work, the NGR were not be maintained at AC ground over the entire frequency range due to the inductance of the additional probe used to bias the NGR; however, this is not expected to make a difference at lower frequencies since NGRs are not likely to be sinking substrate current. However, it is probable that at higher frequencies, an improvement in noise isolation could be achieved if the NGRs were to be maintained at AC ground. Moreover, the distinct peaks in the S_{21} vs. frequency plots observed for the structures with the NGRs and deep N-well guard rings would not result if the NGRs and deep N-wells were maintained at AC ground in the entire frequency range.

Of the four cases presented in Figure 5.5, it can be seen that the case with the wide PGR surrounded by a narrow NGR (PGR(10μm), NGR(2μm)) provides the best noise isolation, even better than the case with a single PGR with a width of 12μm. This can be attributed to the fact that the narrow NGR, which is the outer guard ring, blocks the flow of the substrate current near the die surface, forcing it to flow through the high-resistance bulk. On the other hand, the wide inner PGR presents a low impedance path to AC ground, acting as an effective current sink for the substrate current.

5.2 Modeling substrate noise coupling

Good models of the substrate exist and these may be used to simulate noise coupling through the chip substrate [18]. However, full chip simulation would be required if all the substrate current collectors in the layout are represented, which is computationally infeasible. Practical guidelines are needed for minimizing the size of the

netlist to be simulated. In particular, it is worthwhile to investigate whether it would be sufficient to model only the noise aggressor, victim and the guard ring around the victim, analogous to what is done for latchup simulations. Two additional test structures illustrated in Figure 5.7 and Figure 5.8 were used to study the effects of additional noise collectors on the substrate noise coupled to the victim.

From Figure 5.9 and Figure 5.10 it can be seen that for the case with the PGR (12μm) around the victim, the additional p^+ taps have a significant impact on the S_{21}. On the other hand, for the case with the PGR (2μm) around the aggressor and the victim, the additional p^+ taps have a much smaller effect on the S_{21}. Hence with guard rings around both the aggressor and the victim, the results presented here indicate that the guard rings determine the amount of noise coupled to the victim and the additional noise collectors have only a small influence on the noise coupling.

In order to understand these observations we need to analyze the effect of the additional noise collectors in the two cases. The additional noise collectors are essentially an extra guard ring since they sink a portion of the substrate current. A few of them are around the aggressor and a few around the victim. In Figure 5.11 a simplified substrate network is used to represent the test structure with PGR (12μm) around the victim. I_{SUB} is the injected substrate current by the aggressor, R_{PGR1} is the resistance of the PGR, R_{SUB} is the substrate resistance, R_L is the resistance of the victim and R_{NC} is the resistance to ground of the additional noise collectors, some of which are around the aggressor and

some around the victim. I_{victim} is the portion of I_{SUB} that gets collected by the victim. For the case without the additional noise collectors, I_{victim} can be calculated and is given by:

$$I_{victim} = \frac{R_{PGR1}}{R_{PGR1} + R_L} I_{SUB} \tag{5.1}$$

In the presence of the additional noise collectors I_{victim} can be approximated to:

$$I_{victim} = \left(\frac{R_{NC}}{R_{NC} + R_{SUB}} \right) \left(\frac{R_{PGR1} \,||\, R_{NC}}{R_{PGR1} \,||\, R_{NC} + R_L} \right) I_{SUB} \approx \left(\frac{R_{NC}}{R_{NC} + R_{SUB}} \right) \left(\frac{R_{PGR1}}{R_{PGR1} + R_L} \right) I_{SUB} \tag{5.2}$$

In equation (5.2), $R_{PGR1}||R_{NC}$ is approximated to R_{PGR1}, which would be generally true since R_{PGR1} would be much smaller than R_{NC}. From (5.1) and (5.2) it can be seen that I_{victim} would be significantly smaller in the presence of the additional noise collectors as the extra term in equation (5.2) ($R_{NC}/(R_{NC}+R_{SUB}) < 1$) would have a small value since $R_{NC}<R_{SUB}$. Hence a significant improvement in the noise isolation is observed for this case in the presence of the additional noise collectors (see Figure 5.9).

In Figure 5.12 a simplified substrate network is used to represent the test structure with PGR (2μm) around both the aggressor and the victim. R_{PGR1} and R_{PGR2} are the resistance of the PGRs. For the case without the additional noise collectors, I_{victim} can be approximated to:

$$I_{victim} = \left(\frac{R_{PGR1}}{R_{PGR1} + R_{SUB}} \right) \left(\frac{R_{PGR2}}{R_{PGR2} + R_L} \right) I_{SUB} \tag{5.3}$$

In the presence of the additional noise collectors I_{victim} can be approximated to:

$$I_{victim} = \left(\frac{R_{PGR1} \,||\, R_{NC}}{R_{PGR1} \,||\, R_{NC} + R_{SUB}} \right) \left(\frac{R_{PGR2} \,||\, R_{NC}}{R_{PGR2} \,||\, R_{NC} + R_L} \right) I_{SUB} \tag{5.4}$$

From equation (5.3) and (5.4) it can be seen that I_{victim} would be smaller in the presence of the additional noise collectors since $R_{PGR1}||R_{NC}<R_{PGR1}$ and $R_{PGR2}||R_{NC}<R_{PGR2}$. However if the same approximation made in equation (5.2) is made in equation (5.4) we get:

$$I_{victim} = \left(\frac{R_{PGR1}}{R_{PGR1} + R_{SUB}} \right) \left(\frac{R_{PGR2}}{R_{PGR2} + R_L} \right) I_{SUB} \tag{5.5}$$

which is exactly the same as equation (5.3), indicating that the additional noise collectors have a very small influence in this case. Therefore, for the case with the PGR around both the aggressor and the victim, the calculations predict that I_{victim} (or noise coupled to the victim) should reduce in the presence of the additional noise collectors, but not significantly. This is observed in the measurement results shown in Figure 5.10.

5.3 Substrate noise coupling and guard ring placement

In many published works, substrate noise coupling is evaluated by measuring, or simulating, S_{21} between the aggressor and the victim [19]-[21]. It must be noted however that S_{21} does not fully characterize the aggressor, victim and guard ring system. S_{11}, S_{12} and S_{22} are required to fully model the system. S_{21} only represents the noise coupled from a 50Ω source to a 50Ω load. As the load presented by the victim is changed, the magnitude of noise coupled to the victim will change. However, if the system is fully

characterized, the noise coupled to the victim can be determined for any arbitrary load or source impedance.

To illustrate the importance of fully modeling the system, the effect of load and source impedance on the noise coupling can be analyzed. For the majority of the test structures, the guard ring is around the second port (victim). Since for a passive system, $S_{21}=S_{12}$, even if the guard ring was placed around the aggressor instead, the S_{21} would not change. This would lead us to conclude that the position of the guard ring does not influence the noise coupled to the victim, but this is only true if the load and source impedances are identical; if they differ, this would not be the case. In this work, transducer power gain is used quantify the noise coupled to the victim:

$$G_T = \frac{P_{victim}}{P_{avs}} \tag{5.6}$$

$$P_{avs} = \frac{V_S^2}{8R_S} \tag{5.7}$$

Above, P_{victim} is the noise power coupled to the victim and P_{avs} is the available noise power. ADS (Advanced Design Systems) is used to calculate G_T and all four S-parameters are used to define the substrate network. The simulation setup is illustrated in Figure 5.13. In order to illustrate the effect of Z_S and Z_L on the transducer power gain, a few cases with realistic values of Z_S and Z_L are considered. For the cases illustrated in this section, the substrate network fully models the test structure in Figure 5.1 with a

single PGR (12μm) around one of the ports. It should be noted that the aggressor and victim ports can be interchanged to study the influence of the guard ring location.

There are many sources of substrate noise [18], key sources include the noisy power and ground rails of the digital domain. In this case, the noise injected into the substrate by the ground rail is considered. The digital domain's noisy ground rail is coupled to the substrate through multiple substrate contacts. The routing and contact resistance is lumped to a single approximate value of Z_S=2Ω.

There are also several ways the sensitive analog circuits can be affected by substrate noise [18]. Modulation of the threshold voltage of the transistors in the sensitive analog circuits is one of key ways substrate noise affects these circuits. Some of the injected substrate current is collected by the substrate contacts in the analog domain, and a potential difference is developed between the MOSFET channel region and the closest substrate contact. This potential difference would modulate the threshold voltage of these MOSFETS due to the phenomenon known as the body effect [16]. This would in turn degrade the performance of the analog circuits. The potential difference developed would depend on the resistance between the MOSFET channel and the nearest substrate contact; here an approximate value is used: Z_L=100Ω.

Clearly for this case it can be seen that the values of Z_S and Z_L are very different and the effect of having different Z_S and Z_L on the noise isolation is illustrated in Figure 5.14. Two cases have been compared, one with the guard ring around the victim and the other with the guard ring around the aggressor. It can be observed that the location of the

guard ring influences the amount of noise coupled to the victim. With the guard ring around the victim, the noise coupled to the victim is significantly smaller when compared to the case with the guard ring around the aggressor. Furthermore, it was found that placing the guard ring around the port with the larger impedance always results in better noise isolation.

From Figure 5.15 it can be observed that for a constant Z_S, as Z_L is varied, the amount of noise coupled to the victim changes. To estimate the effect of the substrate noise let us assume that the noise in the digital domain's ground rail has a peak voltage of 20 mV. The magnitude of the noise on the digital ground rail depends on many factors including layout style and the type of chip packaging used; as shown in [24] the value assumed here is a reasonable estimate. Considering the case with Z_S=2Ω and Z_L=100Ω in Figure 5.15, an average transducer power gain of -55 dB is used to calculate change in the threshold voltage (V_{th}) of the transistors in the analog domain. For the assumed value of peak noise voltage in the digital domain's ground rail, the peak voltage across Z_L (victim) was found to be 89 μV. Assuming a body effect coefficient (γ) of 0.4, a maximum ΔV_{th} of 21 μV would result.

Another way substrate noise could impact the performance of the analog circuits is through the coupling of noise from the digital domain's ground rail to the analog domain's ground rail. For this case, the same value of Z_S used previously (2Ω) is used; however, Z_L is the impedance from the substrate tap in the analog domain to the off-chip quiet ground (system ground). Z_L used for this simulation is shown in Figure 5.16. R_{lay} is

the series resistance due to the layout and metal routing, and L_{BW} is the inductance of the bond-wire which connects the on-chip ground to the quiet off-chip system ground. Clearly, Z_L in this case is frequency dependent as the impedance of L_{BW} would change with frequency. Hence, it can be seen from Figure 5.16 that the variation trend of transducer power gain with frequency in this case is different from the other cases illustrated previously (with real Z_L), while using the same substrate network.

The results presented in this section highlight the need to fully characterize the substrate network in order to understand the influence of Z_S, Z_L and guard ring position on the noise coupled to the victim.

5.4 Figures

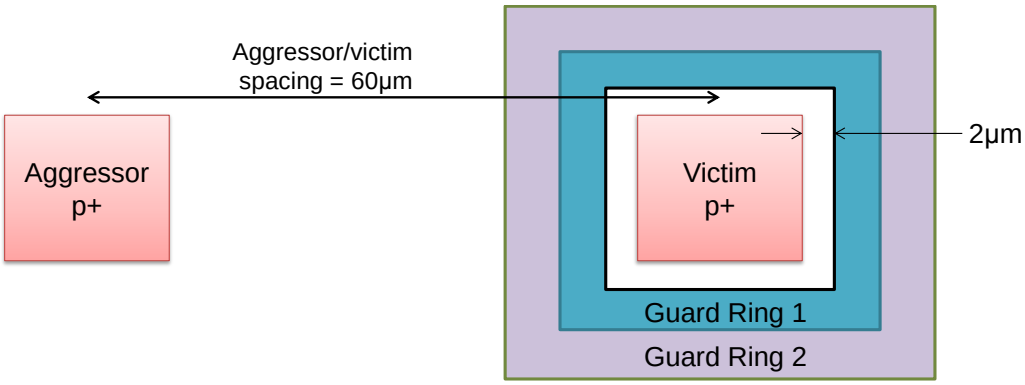

Figure 5.1: Illustration of test structure layout. P-type substrate is used.

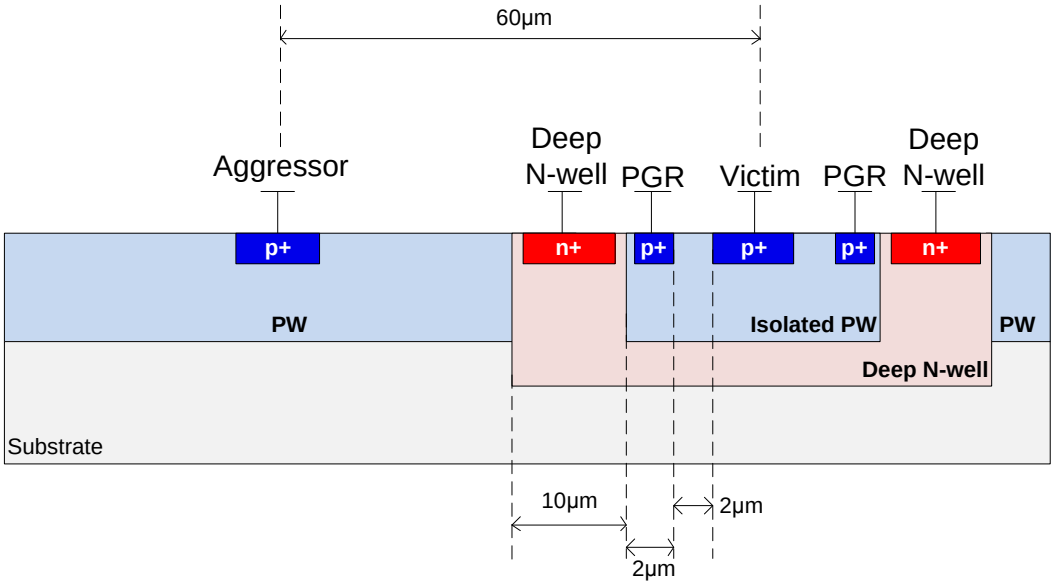

Figure 5.2: Cross-section of case 5 in Table 1.

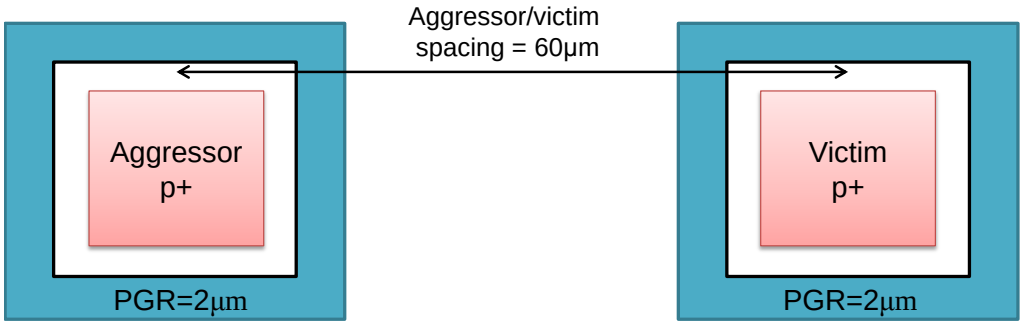

Figure 5.3: Test structure with PGR around both the aggressor and the victim.

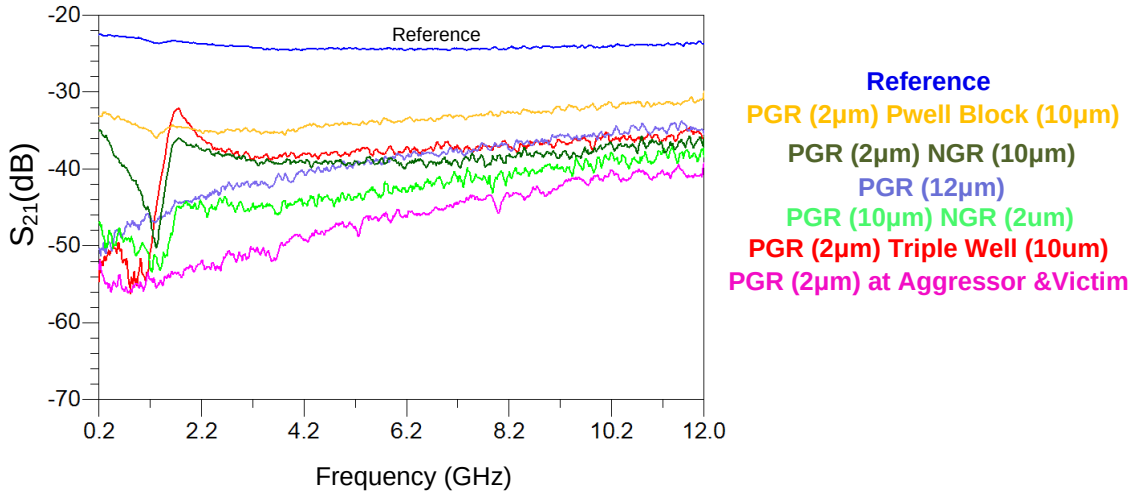

Figure 5.4: Measurement data. S_{21} vs. frequency.

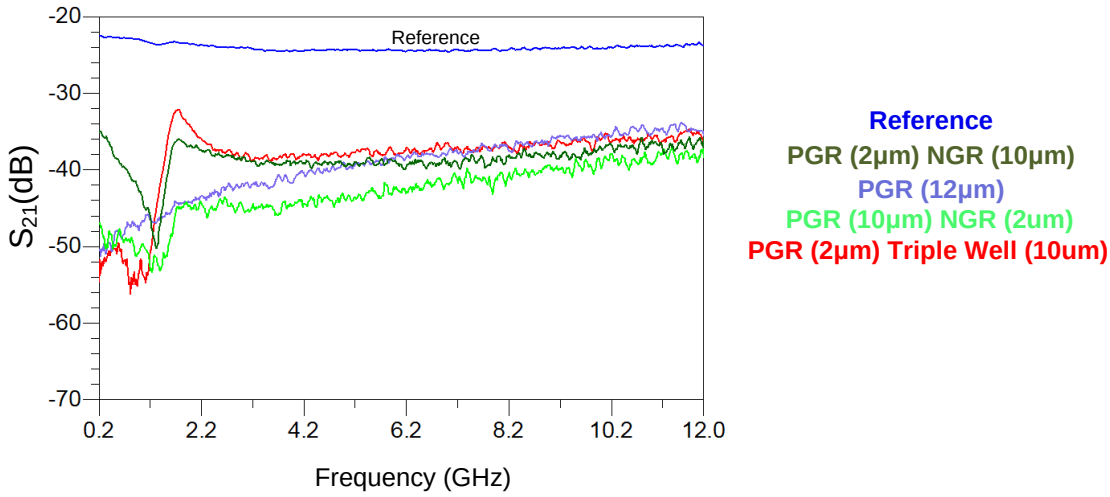

Figure 5.5: Measurement data. S_{21} vs. frequency. Four out of the five cases in Table 1 are plotted.

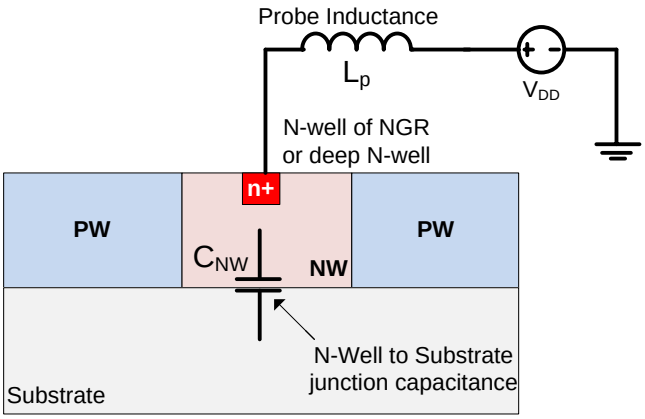

Figure 5.6: Illustration of parasitics added due to the probe used to bias the NGR/deep N-well.

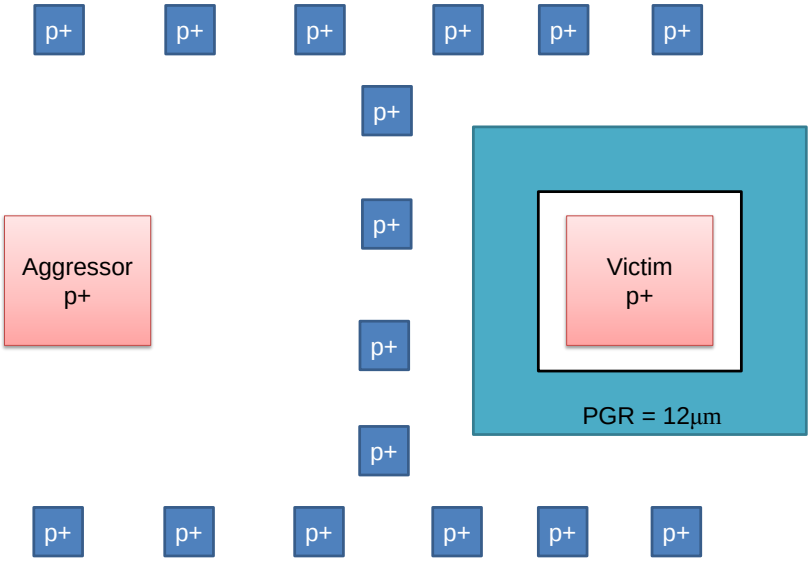

Figure 5.7: Test structure with PGR (12μm) around the victim with additional p^+ regions (noise collectors). The additional p^+ taps are grounded.

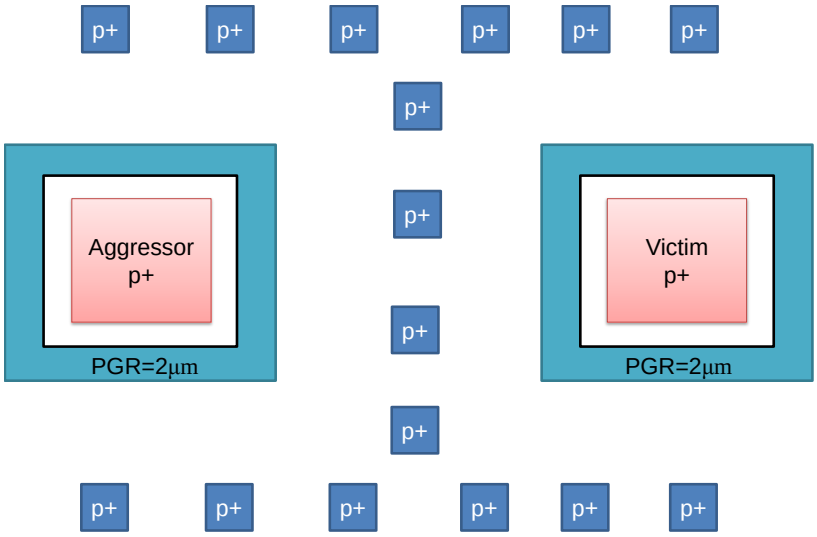

Figure 5.8: Test structure with PGR (2µm) around the aggressor and the victim with additional p^+ regions (noise collectors). The additional p^+ taps are grounded.

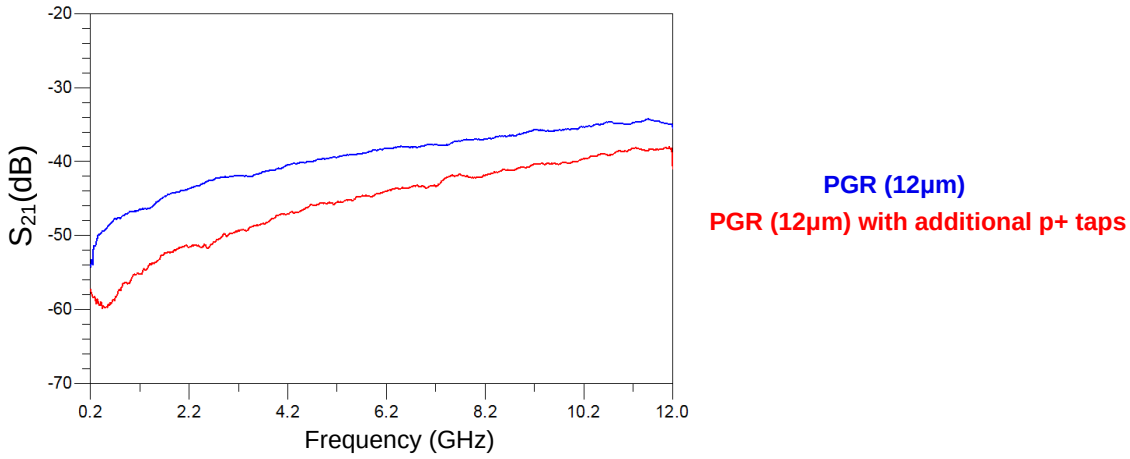

Figure 5.9: S_{21} vs. frequency for the case with PGR (12µm) around the victim, with and without the additional p^+ taps.

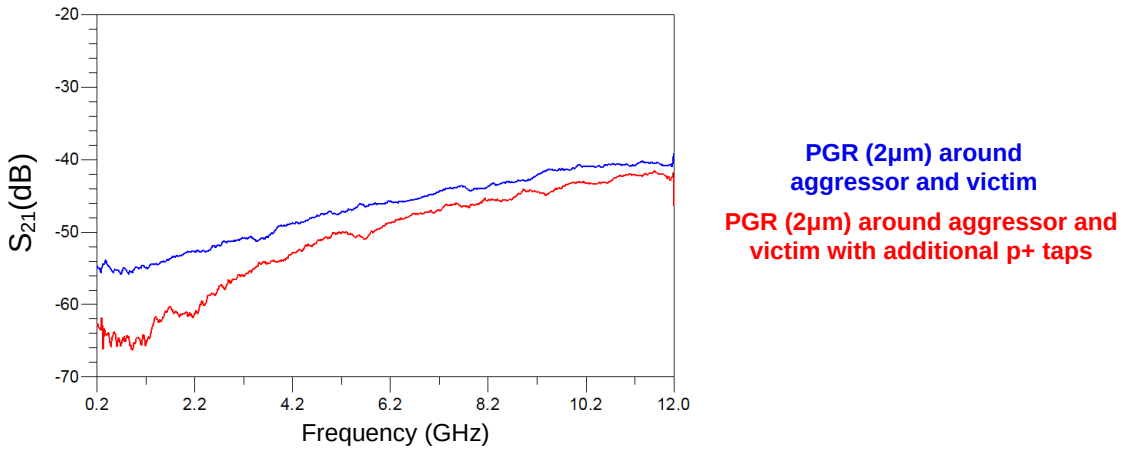

Figure 5.10: S_{21} vs. frequency for the case with PGR (2µm) around the aggressor and the victim, with and without the additional p^+ taps.

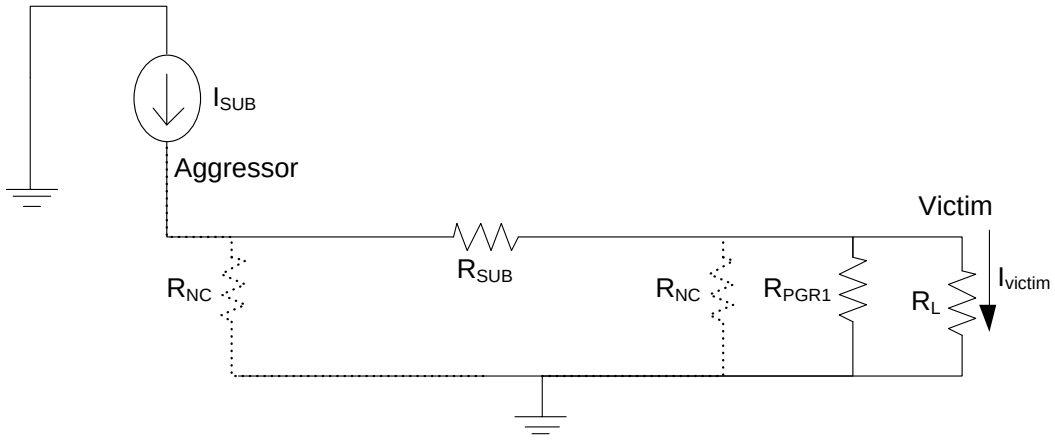

Figure 5.11: Substrate network for the case with PGR (12µm) around the victim.

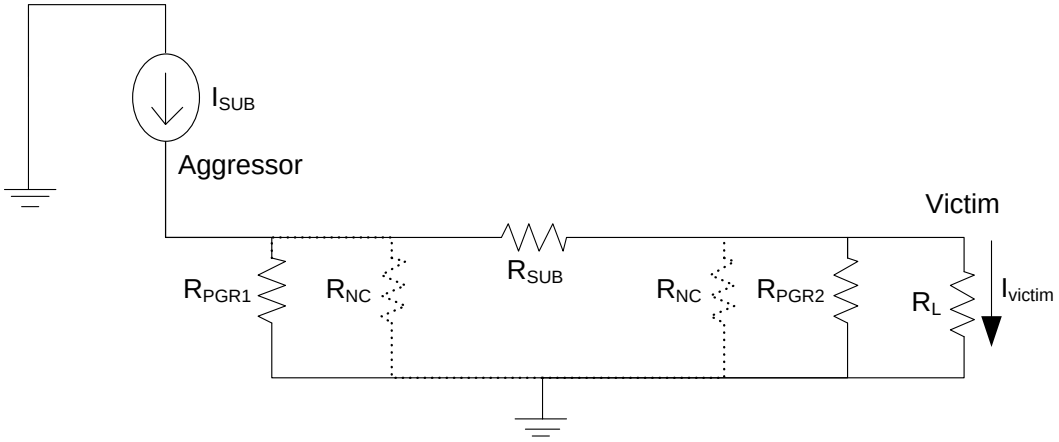

Figure 5.12: Substrate network for the case with PGR (2μm) around aggressor and victim.

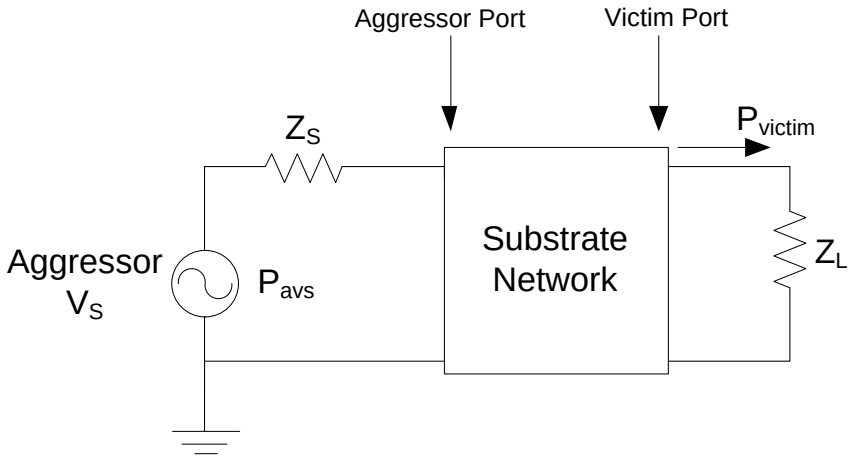

Figure 5.13: Illustration of simulation setup to determine the noise coupled to the victim.

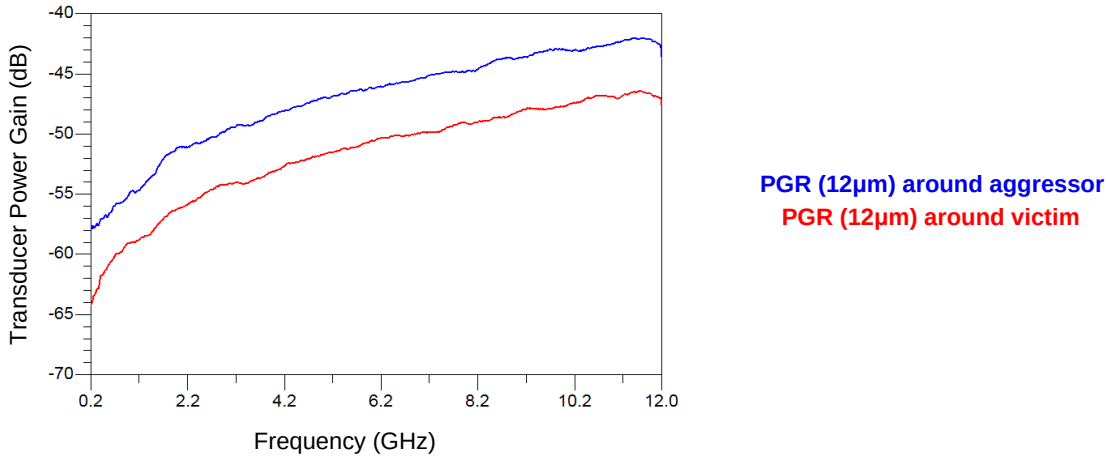

Figure 5.14: Transducer power gain vs. frequency for Z_S=2Ω and Z_L=100Ω.

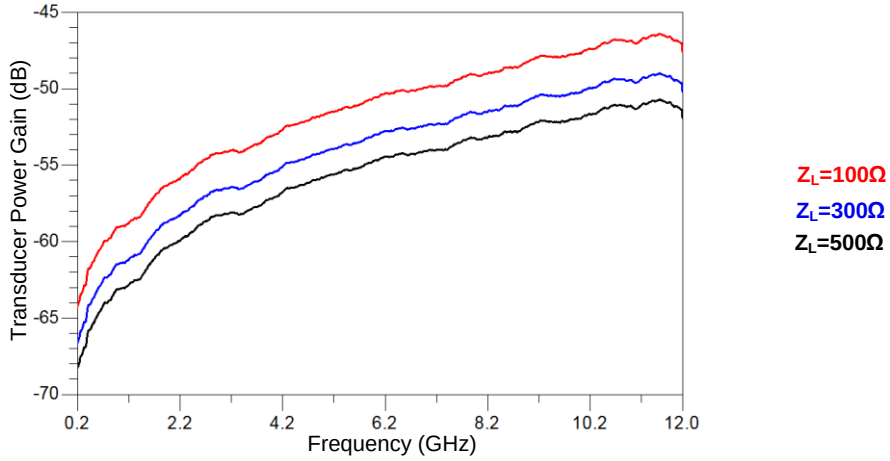

Figure 5.15: Effect of Z_L on the noise coupled to the victim. Z_S=2Ω. PGR (12µm) around victim.

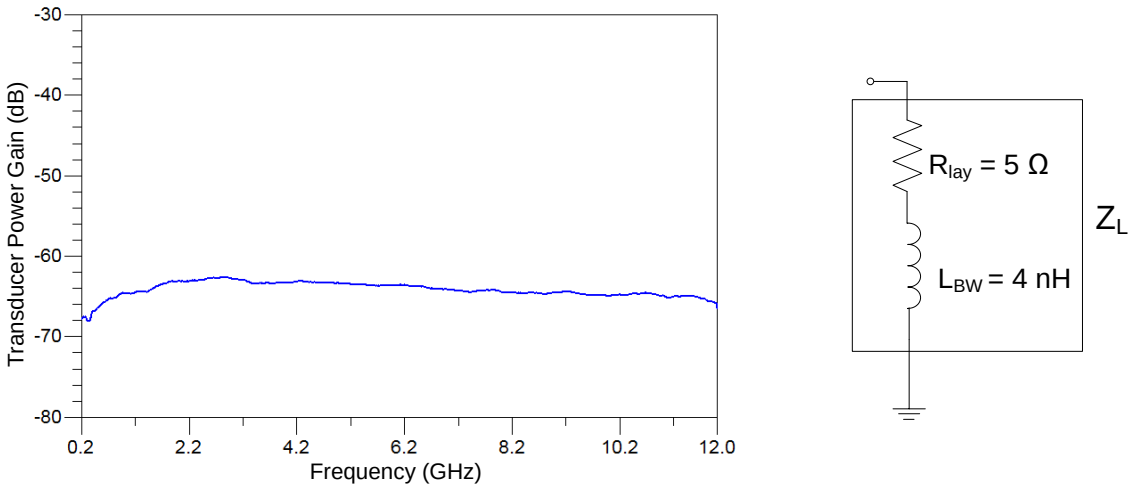

Figure 5.16: Transducer power gain vs. frequency with $Z_S=2\Omega$ and $Z_L=R_{lay}+j\omega L_{BW}$.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

The effects of spacing and orientation on transient ex-LU have been modeled and a method to simulate transient ex-LU in a circuit simulator has been described. It was shown that the layout style has a significant impact on latchup susceptibility. Furthermore, the area efficiency of different guard ring topologies in reducing substrate noise coupling has been compared and a new method to quantify the noise coupled to the victim has been described which takes into account the impedance of the noise source (aggressor) and the impedance of the victim.

6.1.1 Transient external latchup

It was found that I_{trig} was very sensitive to the d_{victim} and o_{victim}. In this work, the 90° victim orientation was found to be the worst case during negative current injection in transient external latchup testing.

During TLU testing, it was found that the relationship between I_{trig} and T_{PW} was a function of d_{victim} and o_{victim}. For small d_{victim}, it was also affected by the presence or absence of the NGR. From the measurement data shown, it can be inferred that it would be best to have a small f_{3dB} to protect against TLU (in Figure 2.10 the 180° victim orientation has a smaller f_{3dB} than the 90° victim orientation). For test structures with a smaller f_{3dB}, the pulse-width at which transient effects become significant is larger, so triggering latchup for small T_{PW} would require very high current levels. In order to have a small f_{3dB}, d_{victim} can be increased and the 90° victim orientation should be avoided.

As highlighted previously [8], since I_{trig} during the positive I-test does not change (increase) significantly as the pulse-width is reduced, for real world stresses such as cable discharges, positive current injection would be the worst case.

The PNPN (victim) layout has a significant influence on its holding voltage and therefore on latchup susceptibility. In this work, by changing the layout of the PNPN diffusions, the V_h changed by 0.7V. In standard cell based designs, latchup is not expected to be sustained unless $V_{DD} > 1.8$ V, due to the topology of the parasitic PNPN devices that are formed.

6.1.2 Substrate noise coupling

Overall it was found that the guard ring topology with the PGR around both the victim and the aggressor resulted in the best noise isolation and consumed the least area. For the cases with the guard ring(s) around the victim alone, it was determined that the case with a wide PGR surrounded by a narrow NGR resulted in the best noise isolation.

The importance of fully characterizing the aggressor, victim and guard ring system was highlighted. S_{21} alone does not fully characterize the substrate network. It was shown that using a fully characterized substrate network, the influence of noise source (aggressor) and victim impedance on the noise isolation can be investigated. It was shown that Z_S and Z_L affect not only the magnitude of noise coupled to the victim, but also the decision whether to place the guard ring around the aggressor or the victim to achieve the best noise isolation.

6.1.3 Latchup and substrate noise

Substrate noise coupling and external latchup share a common origin: substrate current injection. Guard rings are used to reduce both substrate noise coupling and latchup susceptibility. PGRs and NGRs are commonly used to prevent latchup as well as to suppress substrate noise coupling. However, it is essential to use the correct type of guard ring or combination of guard rings after taking into consideration the nature of the aggressor and the victim.

Proper substrate modeling is essential for simulating both substrate noise coupling and external latchup. Considerable research efforts have been invested in characterizing and modeling the substrate [18]. In this work, the importance of the substrate network has also been highlighted and its influence on external latchup and substrate noise coupling has been analyzed.

6.2 Future Work

6.2.1 External latchup

It has been shown in this work and in [12] that R_{SUB} (Figure 3.10) has a significant influence on the latchup trigger current. A sophisticated extraction method based on existing works such as [19] needs to be developed.

In this work and in previous works such as [12] it has been shown that R_{NW} and R_{PW} in the proposed circuit models are functions of the victim orientation. Analytical

models for the victim orientation dependence of R_{NW} and R_{PW} can be developed in future work.

With the N-well aggressors, test structures with o_{victim}=90° and 180° were studied in this work. The only substrate contact in these test structures was a part of the victim, i.e. PNPN (Figure 2.7), and it was at a large distance from the aggressor. This affected the ex-LU triggering mechanism. In the future, the effects of placing substrate contacts closer to the aggressor could be studied. Furthermore, with the N-well aggressors, the effects of d_{victim} on transient ex-LU could be investigated.

In this work it was shown that the PNPN layout can have a significant influence on its holding voltage and therefore on latchup susceptibility. The traditional PNPN in Figure 1.2 was compared with the standard cell layout based PNPN in Figure 1.3(b). It was shown that the standard cell layout based PNPN can be modeled as a distributed PNPN. In the future, it might be worthwhile to study the effects of varying the length and the width of the diffusions on the PNPN characteristics.

6.2.2 Substrate noise

In this work, the NGR and deep N-well were biased at V_{DD} using an additional probe. Due to the parasitic inductance of this probe, the NGR and deep N-well could not be maintained at AC ground at all frequencies, which affected the results of the experiments. In the future, on-chip decoupling capacitors could be added to these test structures in order to effectively bias the NGR and deep N-well and reduce the effects of the parasitics of the probes.

Test structures with sensitive analog circuits such as noise sensitive LNAs, VCOs, etc., as the victims could be studied in the future. The effectiveness of the recommended guard ring topologies could be analyzed with the realistic noise victims.

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