CONFINEMENT OF MICROPLASMA IN SILICON TRENCHES WITH WIDTHS AS SMALL AS 2.5 μm

BY

EUNG SOO KIM

THESIS

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Advisor:

Professor J. Gary Eden

Abstract

In plasma science, the ability to confine plasma in cavities with characteristic dimensions less than 1 μm would represent a major milestone. In this thesis, realization of microplasma inside channel devices with the characteristic dimensions of 5 μm and 2.5 μm is discussed. Data collected during the characterization of 5 μm devices are consistent with Paschen's curve. Operating devices with a characteristic dimension of 2.5 μm are also introduced in this thesis. Finally, a few potential strategies for creating "nanoplasma" devices are discussed.

To Father and Mother

Acknowledgments

First of all, I would like to thank everyone at the Laboratory for Optical Physics and Engineering (LOPE) at the University of Illinois at Urbana-Champaign, especially Dr. Cho, Min, DS, and Taegon for their assistance in my research. In addition, I would like to give special thanks to my advisors Professor J. Gary Eden and Professor Sung-Jin Park who let me work and learn at the laboratory and gave great support, guidance, and advice throughout both my undergraduate and graduate research. Finally, I would like to give my utmost thanks to my father and mother whom I dearly love and admire.

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1. Introduction

Plasmas comprise 99% of the matter in the universe [1]. In everyday life there are lamps, TVs, lightning, and auroras; in the semiconductor industry, reactive ion etching (RIE) and plasma-enhanced chemical vapor deposition (PECVD) are two of the most widely used processing techniques.

Microplasmas are one type of plasma having characteristic dimensions of 1 μm to 1000 μm. Plasmas with these characteristic dimensions have many unique physical properties compared with well-known regular plasmas. Microplasmas operate in high-pressure, high-power, high electron density, and low-temperature states [2]. According to Sung-Jin, in order to operate in atmospheric pressure, microplasmas require characteristic dimensions of less than 10 μm [3].

Previously, microplasmas confined in 10 μm squares have been reported [4]. As the characteristic dimension of microplasmas approaches 1 μm, microplasmas are expected to exhibit previously undisplayed behavior. As the characteristic dimensions approach Debye lengths and as pressure increases above atmospheric pressure, the plasma will begin to resemble the behavior of a supercritical liquid [5].

There are many available substrate materials to reliably confine microplasmas [6, 7, 8]. Among these materials, in the near future, silicon is the most promising for the confinement of microplasmas (or even nanoplasmas) as semiconductor fabrication techniques have already achieved 20 nm features in mass production. Sub-nanometer features have been achieved with other techniques such as electron beam lithography and extreme ultraviolet (EUV) lithography. Although the possibility of confining plasma in nanometer-scaled devices has yet to be

demonstrated, fabrication techniques and experiments with silicon devices to achieve nano-scale plasma devices are discussed in this thesis.

2. Previously Demonstrated Microplasma Devices

In this chapter, the previous device structure and its test setup used by Taek-Lim Kim in the Laboratory for Optical Physics and Engineering (LOPE) are discussed [9]. In addition, the limitations to this experimental setup are introduced, but the suggestions and the solutions to these limitations are explained in detail in Chapter 3.

2.1 Channel Device

Multi-dielectric-layered silicon devices having V-grooved cavities fabricated in silicon were used at the LOPE for large cavities arrays and addressable arrays with 50 μm and 100 μm width squares [10, 11]. This structure was then modified for plasma channels as shown in Figure 2.1 for applications such as lasers. The fabrication techniques used to create this V-grooved channel device have been utilized to create several other devices that will be described throughout this thesis.

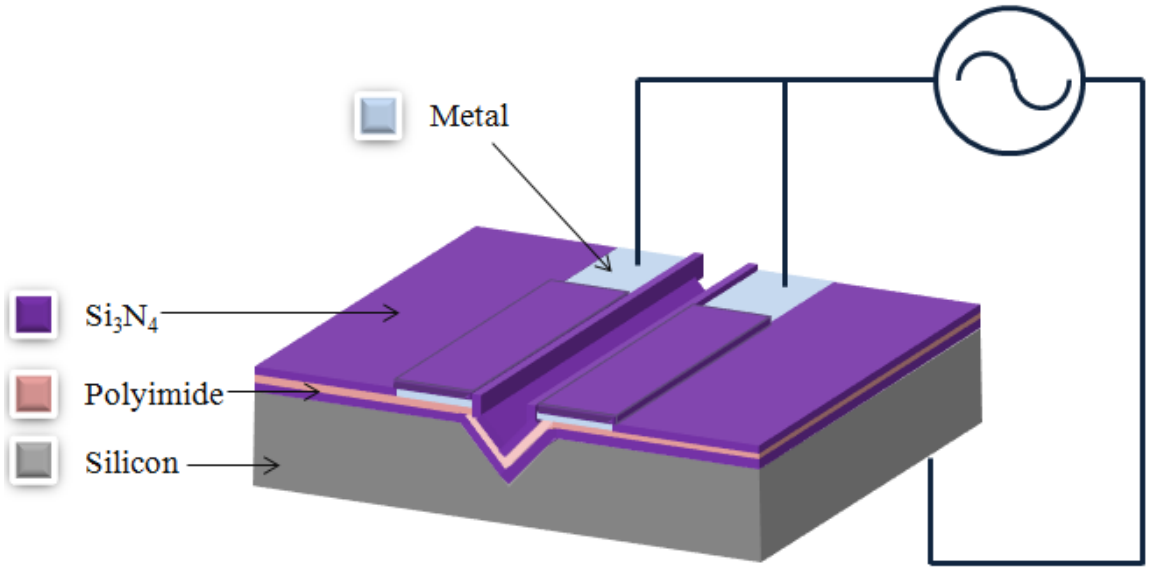

Figure 2.1: Previous V-grooved channel device structure [12].

To fabricate the device shown in Figure 2.1, silicon nitride was deposited with PECVD on both sides of the silicon wafer after naturally grown oxides were removed using HF solution. This silicon nitride layer was then patterned and etched. The remaining silicon nitride served as a barrier for KOH wet etching. With KOH wet etching, the silicon was etched into a V-grooved channel. The existing silicon nitride was then removed and a new 2 μm layer of silicon nitride was deposited on top of the device and served as the main dielectric layer of the device. Then an 8 μm layer of polyimide was coated on top of the silicon nitride to create a gap between the silicon and the electrodes. The electrodes were then deposited on top of the polyimide. This metal served as a barrier for etching polyimide with reactive ion etching (RIE). Once polyimide in the channel region was etched away by RIE, metal was patterned with photoresist and etched with HCl and HNO_3 etchant. Finally, a 4 μm-thick silicon nitride layer was deposited on top of everything to protect the device.

2.2 Test Setup

The completed device is then loaded inside the testing chamber in the vacuum system like the one represented in Figure 2.2. The system is first pumped down to the 10^{-3} Torr range with the roughing pump and then the turbomolecular pump pumped the system further down to the 10^{-7} Torr range. A system that reached this level of pressure ensures that there were only few impurities inside the chamber and, therefore, the desired gas mixtures could then be injected into the testing chamber. High AC voltage was finally applied to the device to ignite the microplasma. [9]

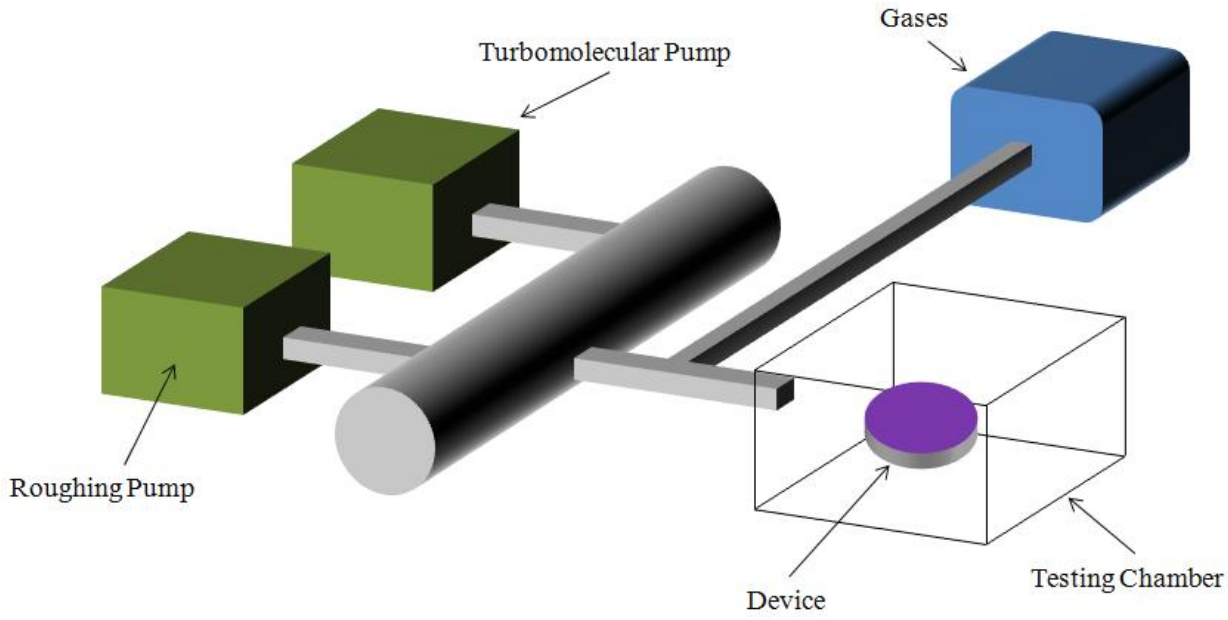

Figure 2.2: Schematic diagram of vacuum system.

2.3 Limitations of Previous Devices and Test Setup

The test setup mentioned above, however, had some limitations. Its main weakness was the fact that the whole device was exposed to gas. This problem becomes serious when the microchannel widths become smaller than 50 μm because of surface discharge, which is shown in Figure 2.3. Surface discharge occurs at the edges of the electrodes. As the channel gets narrower, higher voltage is required to ignite microplasma inside the channel. However, before the voltage reaches this ignition voltage of microplasma, the electric field strength at the edges of the electrodes is sufficient enough to ignite surface discharge. Once this surface discharge occurs, most of the current from the power supply is consumed, preventing microplasma from being confined inside the channel. The solution to this surface discharge is discussed in the following chapters as 5 μm devices and their test setup are explained.

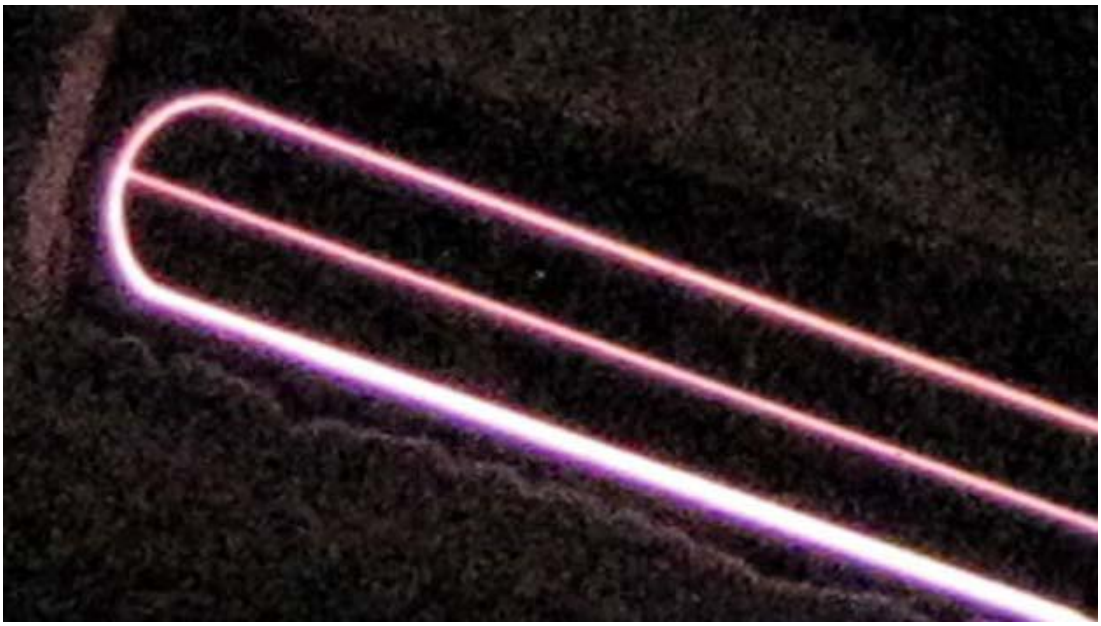

Figure 2.3: Undesired surface discharge on the electrode edge [9].

Limited visibility of the devices was another inherent problem of the test setup of Figure 2.2. Taking images of the microplasma was challenging because the device was positioned inside the testing chamber. As the device size decreased, greater magnification was required, which not only decreased the intensity of the collected images but also made focusing the light from the plasma difficult. Obtaining images of the sides of the channel was difficult because there was only a limited number of windows on the chamber. These significant weaknesses of the test setup of Figure 2.2 necessitated the development of a new testing setup and procedure, which will be discussed in the next chapter.

3. Microplasma in 5 μm Silicon Devices

This thesis focuses on reducing the size of microplasma devices. To that end, this chapter describes the reduction of the channel widths by an order of magnitude from 50 μm to 5 μm. In order to ensure microplasma confinement in 5 μm devices, surface discharge must be prevented. The first section of this chapter describes a few modifications to the previous device and experimental setup intended to prevent surface discharge. Then, the results of 5 μm microplasma devices are presented in the last section.

3.1 External Device

The general structure for 5 μm devices is almost the same as that described in Chapter 2.1 except that the 5 μm devices have a thicker layer of polyimide than on the 50 μm devices. This thicker dielectric layer helps the device withstand higher voltages across its electrodes. The cross sections of the 50 μm and 5 μm silicon devices are shown in Figure 3.1. The thicker polyimide in the 5 μm devices presents increased difficulty in etching, which results in a U-shaped trench instead of a V-grooved channel like those of the 50 μm devices.

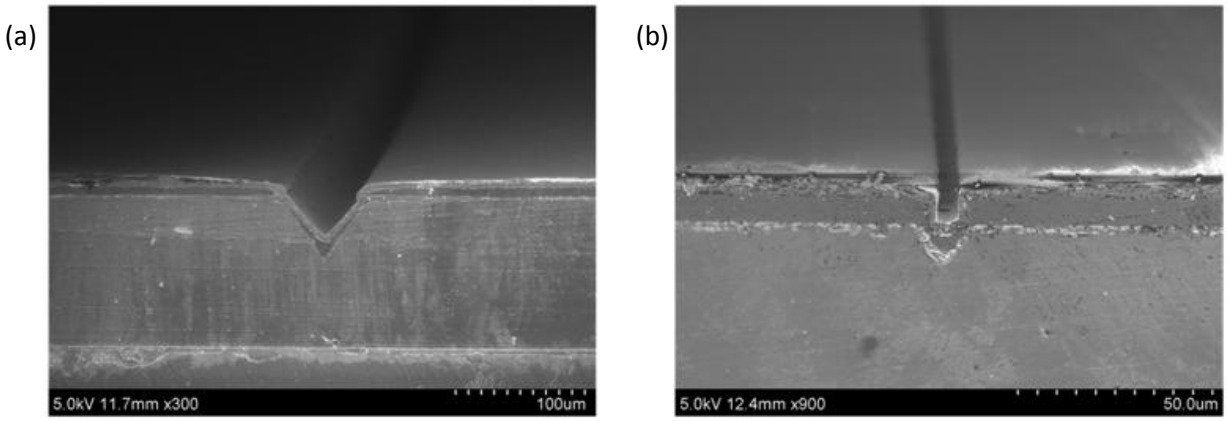

Figure 3.1: Scanning electron microscope (SEM) images of (a) 50 μm channel and (b) 5 μm channel [12].

The packaging of the 5 μm devices is significantly different from that of the 50 μm devices. The 5 μm devices are called an external device because they are loaded outside the vacuum system (which will be described in the following section). The device schematic is shown in Figure 3.2. A glass piece which has a smaller area than that of the electrode is prepared with a hole which serves as a gas inlet. This glass piece is then secured to the top of the device and finally a tube is connected to the glass. Gas is injected inside the channel only through this tube, and the gas inlet prevents the outer edges of the electrodes from being exposed to the gases. By packaging the devices in this way, surface discharge on the edges of the electrodes has been successfully prevented.

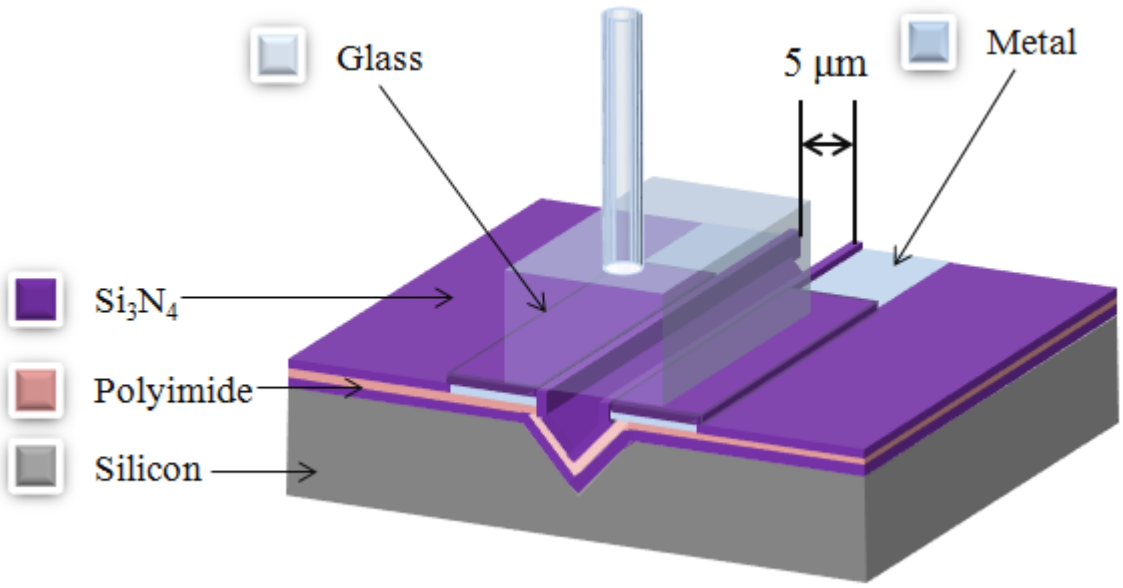

Figure 3.2: External device structure.

3.2 Test Setup

In order to test the external device mentioned in the previous section, a slight modification was made to the test setup described in Chapter 2. Previously, the device was loaded inside the testing chamber leaving the whole device exposed to gas. Instead of placing the external devices inside this testing chamber, the devices are directly connected to the vacuum system as shown in Figure 3.3. Other experimental methods are described in Section 3.3.

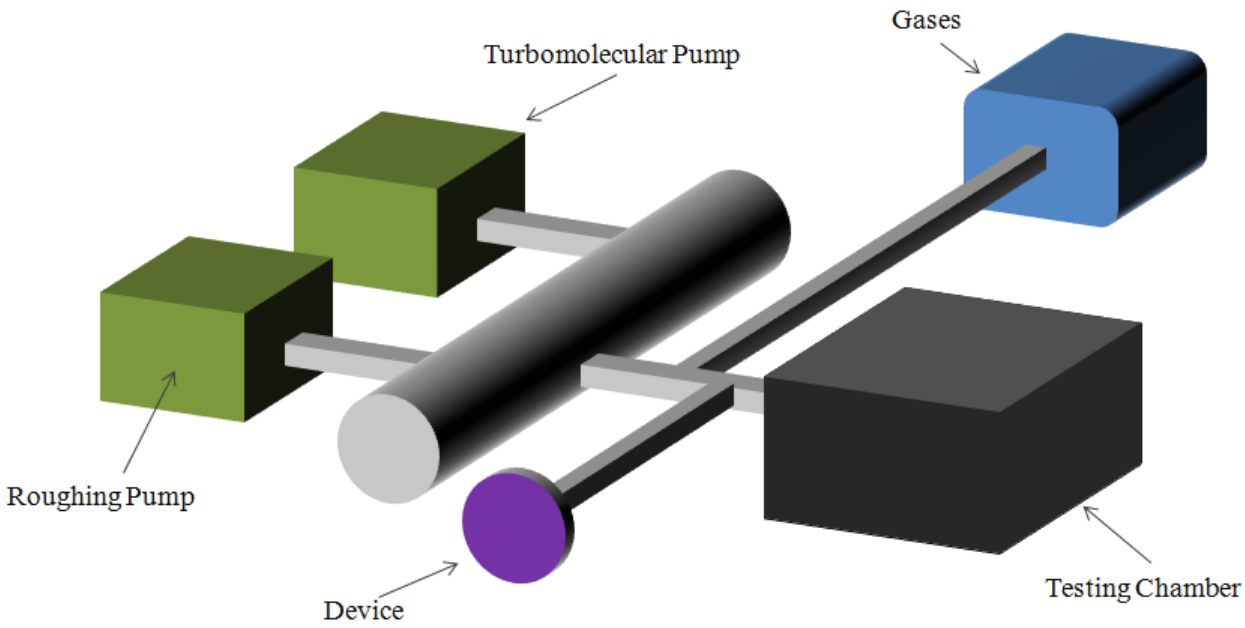

Figure 3.3: Schematic diagram of vacuum system.

3.3 Results

Microplasma was successfully confined in a 5 μm device and a photograph of a device in operation is shown in Figure 3.4.

Figure 3.4: Operating 5 μm channel device [13].

The 5 μm device was tested with an argon/neon mixture. A small amount of nitrogen was intentionally injected to the system in order to prevent any surface discharges because nitrogen has high ignition voltages. Because the ignition voltage for a 5 μm device was much higher than those of 50 μm device, surface discharges on the electrode surface and even inside the tube were unavoidable at some high voltage levels without nitrogen. Ignition for several gas mixtures was measured as a function of pd (pressure multiplied by the channel width) and those data are shown in Figure 3.5.

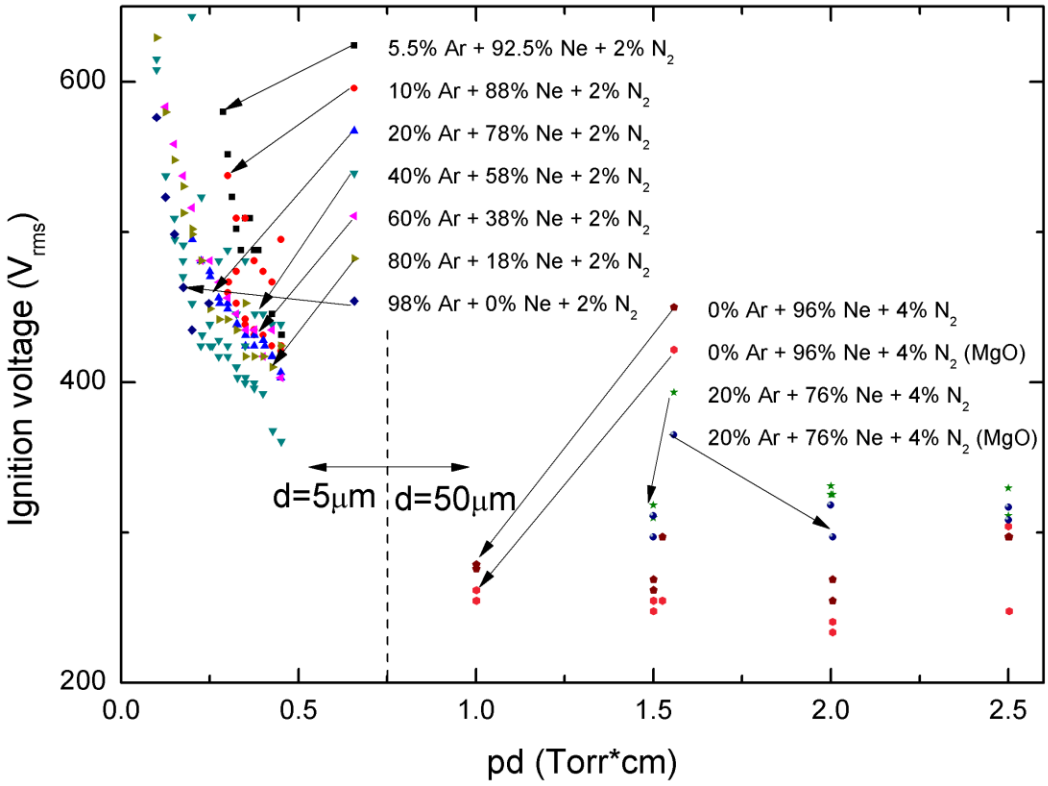

Figure 3.5: Paschen's curve obtained with 5 μm and 50 μm devices.

Points at the top-left part of the graph in Figure 3.5 are the data for 5 μm and those at the bottom right part are the data for 50 μm. For 5 μm, as pd decreases the ignition voltage increases

dramatically. In contrast, for 50 μm, ignition voltage increases as pd increases. Somewhere in between, there must be optimal points where the ignition voltage is the lowest, the measurement of which is suggested as future work in the next chapter. The combined data for both 5 and 50 μm devices follow the pattern of Paschen's curve, which is the black line of Figure 3.6. Figure 3.6 is a theoretical Paschen's curve calculated by Go and Pohlman [14]. This curve was calculated to represent Paschen's curve specifically for microplasma with 760 Torr air. The resemblance of the data of Figure 3.5 and the black line of Figure 3.6 indicates that microplasma is well confined in the 5 μm silicon devices. However, Go and Pohlman used a metal-to-metal discharge technique, which is different from the dielectric-barrier-discharge method used for the channel devices in this thesis. In addition, Go and Pohlman varied the electrode gap for his device (the discharge distance), but the gap for the device in this thesis was fixed and the pressure was varied.

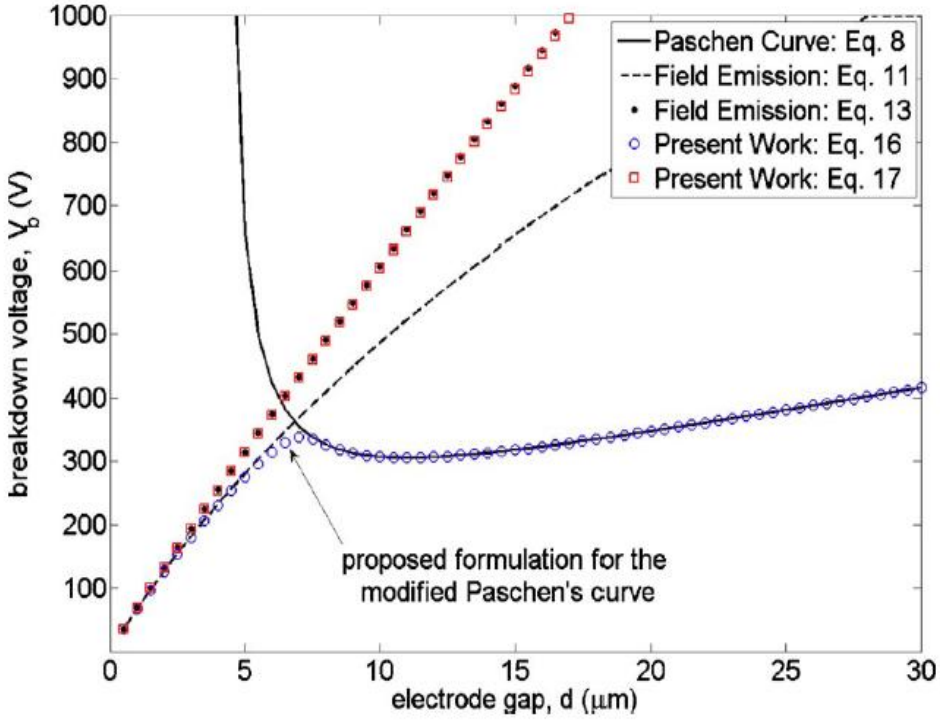

Figure 3.6: Calculated Paschen's curve from Go and Pohlman [14].

An interesting feature of Figure 3.6 is the trend represented with blue circles labeled "Present Work: Eq. 16". The work of Go and Pohlman suggests that Paschen's curve collapses for d ~ 7 μm. As they vary the electrode gap, the collapse around d ~ 7 μm suggests that microplasmas no longer follow the pattern of Paschen's curve at less than 7 μm, which contradicts the data shown in Figure 3.5. Since the results of this thesis follow the black line of Figure 3.6, it is clear that plasmas can actually be confined in 5 μm without any collapse of Paschen's curve.

Figure 3.5 also contains interesting results on gas mixtures. As the percentage of neon atoms increases, the ignition voltage drops, which is clearly shown for 50 μm channel devices. However, this is not true for 5 μm channel devices and they act the opposite way. As the percentage of neon atom increases, the ignition voltage also increases for 5 μm devices. Because there are many ill-understood phenomena even at 5 μm, sizing down microplasma into the nanometer range would open up a whole new field.

3.4 Limitation of the Device Structure

There were two major problems with the device described in the preceding sections, which hinder its scalability. The first problem is the required ignition voltage for microplasma. As mentioned in Section 3.3, the required ignition voltage increased dramatically as the device size became smaller. However, the device structure used for 5 μm devices could not sustain high voltages due to weak dielectric strengths.

The other major issue associated with the structure involves alignment during device fabrication. Because several lithography steps must be performed at the same location of the device, the errors in these lithography processes are unavoidable, especially with the limited

tools available for fabrication at the University of Illinois at Urbana-Champaign. Figure 3.7 shows the cross-sectional view of a misaligned device. When the characteristic dimension of the device approaches 1 μm, these errors would be unacceptable. In order to decrease these lithographic errors while keeping the device structure the same, a self-alignment method may be adopted [15]. However, as it may change the device structure, new fabrication processes must be studied before being implemented.

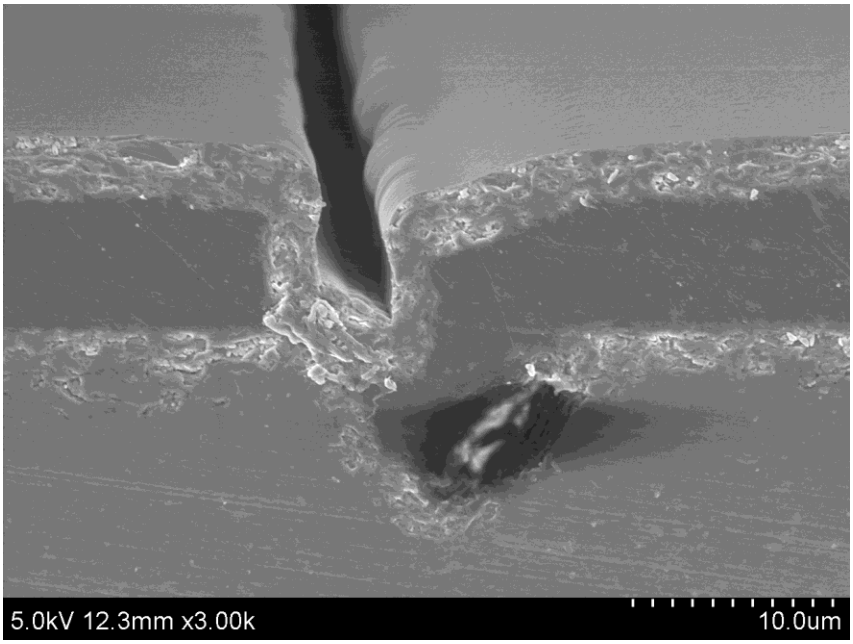

Figure 3.7: Misaligned device picture taken with SEM.

4. Microplasma in 2.5 μm Silicon Devices

At the end of Chapter 3, the limitations of the device structure presented therein were discussed. In this chapter, a new device structure with 2.5 μm channel width that resolves the previous problems is described. Results and limitations of this new structure are also discussed.

4.1 New Device Fabrication

In order to minimize the lithographic error, it was necessary to change the device structure from that shown in Chapter 3. The basic structure is similar to the device of Chapter 2 except for a few key changes. The device structure of this chapter consists of two parts: silicon and glass. The silicon part is similar to that of the previous device, and the glass part is similar to the glass of the external device, except that it now includes the electrode. Combined, these two parts produce the device represented in Figure 4.1.

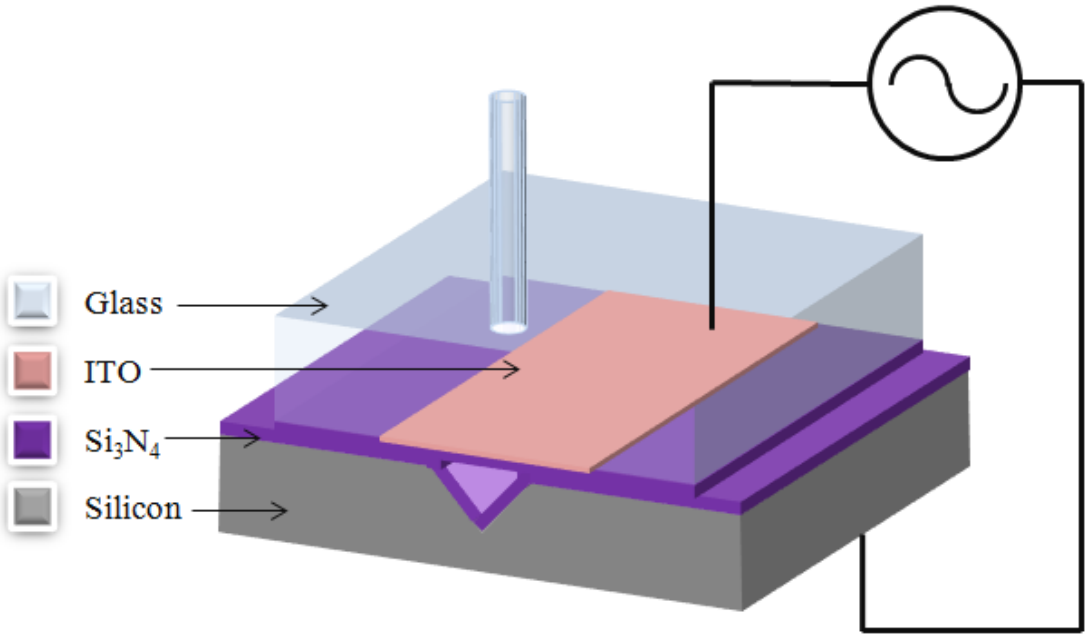

Figure 4.1: 2.5 μm device structure.

To fabricate this device, a V-grooved channel was first etched with KOH wet etching. However, instead of using a multi-layered dielectric, 3 μm of silicon nitride was the only dielectric layer deposited on the surface of the silicon. Previously, electrodes were patterned on top of the dielectric layer and the glass was used to cover the channel. However, for the new structure, transparent metal, indium tin oxide (ITO), was coated and patterned on the glass surface. After the ITO was patterned, 3 μm of silicon nitride was deposited on top of it as well, so as to give enough gap between the ITO and silicon electrodes. This glass part with ITO and silicon nitride was put on top of the silicon part of the device just like the glass for the external device mentioned in Chapter 3.

The picture of the cross section of the silicon part was taken using a microscope and is shown in Figure 4.2. Because the fabrication process only has one lithography step, the device in this photograph does not show evidence of significant errors in alignment. Note the device in Figure 4.2 is a 5 μm device, not a 2.5 μm device. This is a prototype of the new structure.

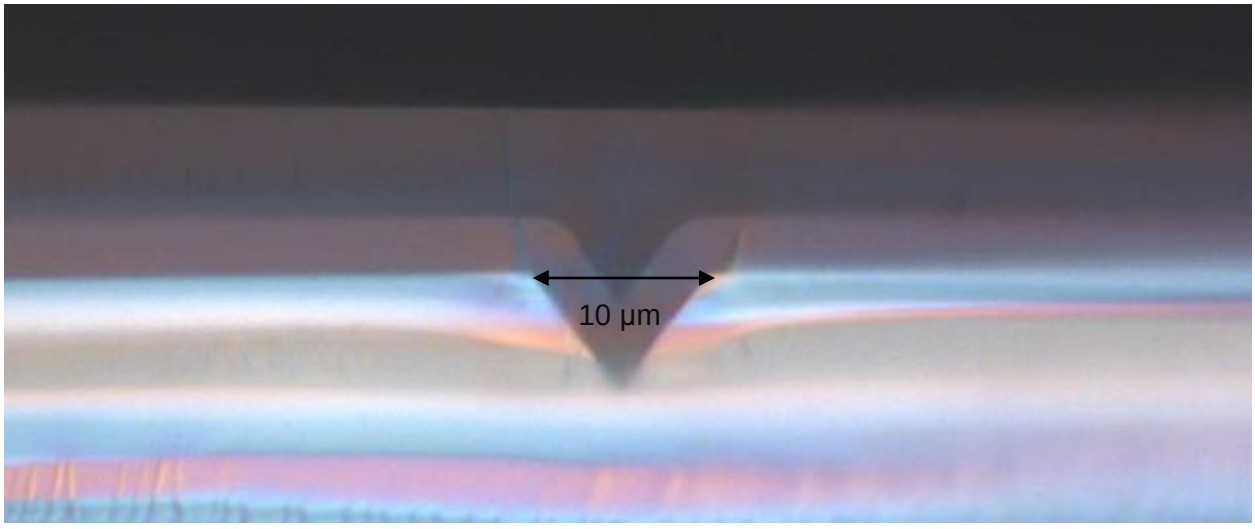

Figure 4.2: Cross-sectional view of the new device taken with microscope.

4.2 New Device Design

Another major problem with regards to decreasing the microplasma size is the requirement for high voltage in order to ignite the plasma. 2.5 μm devices were expected to require extremely high voltages (a few kV) compared to 5 μm devices, but the dielectric layer in these devices cannot sustain these high voltages. In order to resolve this problem, an I-design was adopted. Instead of using a conventional channel design, an I-design which resembles a capital "I" shape was etched on the silicon surface, resulting in bigger regions at the top and the bottom, as shown in Figure 4.3. Since these bigger regions require lower ignition voltage, microplasmas are expected to be ignited in these regions first, helping to confine microplasma in the smaller 2.5 μm channel in the middle.

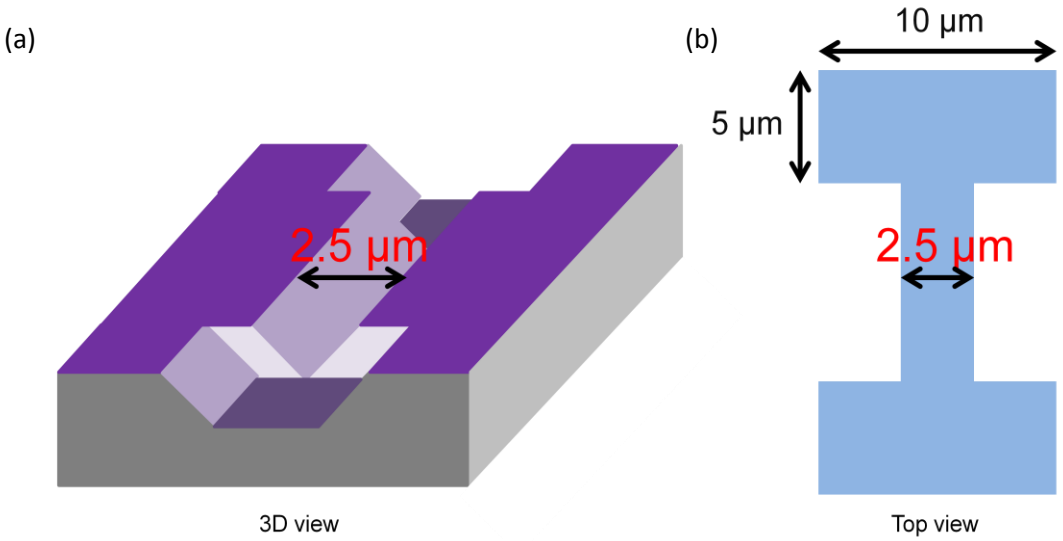

Figure 4.3: Device designed drawn from (a) bird's-eye view; (b) top view.

Since the device is small, successful operation would be extremely hard to detect even though the microplasma is confined inside the device. Therefore, instead of using a single I-design, an array of these I-structures was fabricated on the wafer. Two different array designs

were used and the top views of these designs are shown in Figure 4.4 (a) and (b). The first arrangement places I-designs in both horizontal and vertical directions. The channels in the second design share the big top and bottom area and form a tall I-design.

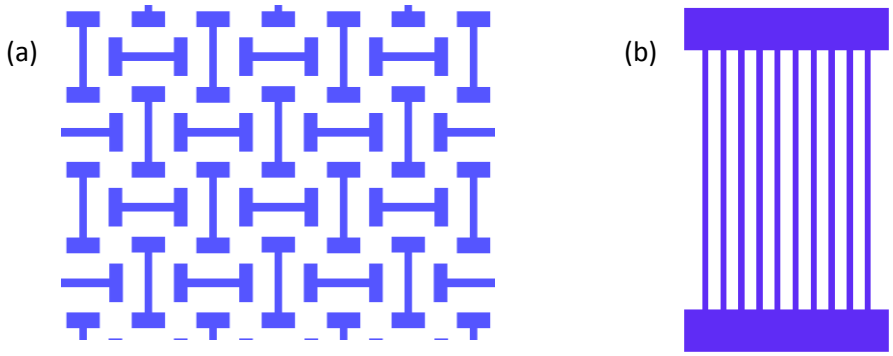

Figure 4.4: Top view of I-design arrays.

4.3 Results

I-design arrays mentioned in Section 4.2 were tested with a neon and argon mixture. A picture of an operating first device with the arrangement of Figure 4.4 (a) was taken with a CCD camera and is shown in Figure 4.5. The total array size of this device is 1,960 μm which corresponds to 862 pixels. Therefore, each pixel in this image represents about 2.26^2 μm^2. The microplasma size is estimated by the number of pixels, as shown in Figure 4.5.

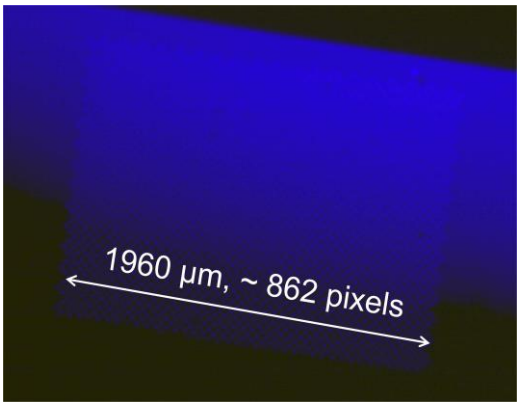

Figure 4.5: Operating device picture.

Figure 4.6 (a) is a magnified version of Figure 4.5 and Figure 4.6 (b) is a false-color image for Figure 4.6 (a). The overall shape of the I-design array in Figure 4.5 and the channel inside the circled area is only one pixel wide. Since each pixel is 2.26^2 μm^2 in dimension, the actual width of the channel is around 2.26 μm. The possibility of confining microplasma inside less than 2.5 μm has thus been demonstrated.

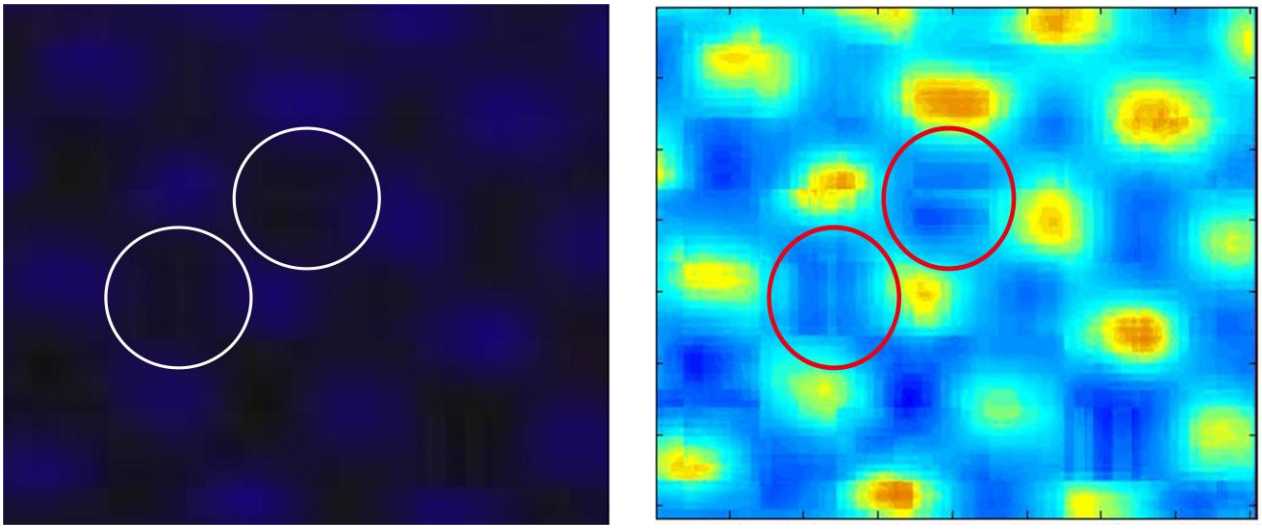

Figure 4.6: (a) Magnified version of Figure 4.5; (b) False-color image of Figure 4.6 (a).

The arrangement of Figure 4.4 (b) was also tested under the same experimental conditions as the device shown in Figure 4.5 and 4.6. An ICCD camera was used to capture photographs of this device in operation in order to increase the intensity of the picture of the channel regions. False-color images of an operating device with different operating voltages were generated and are shown in Figure 4.7; and a magnified version of one of these images is shown in Figure 4.8.

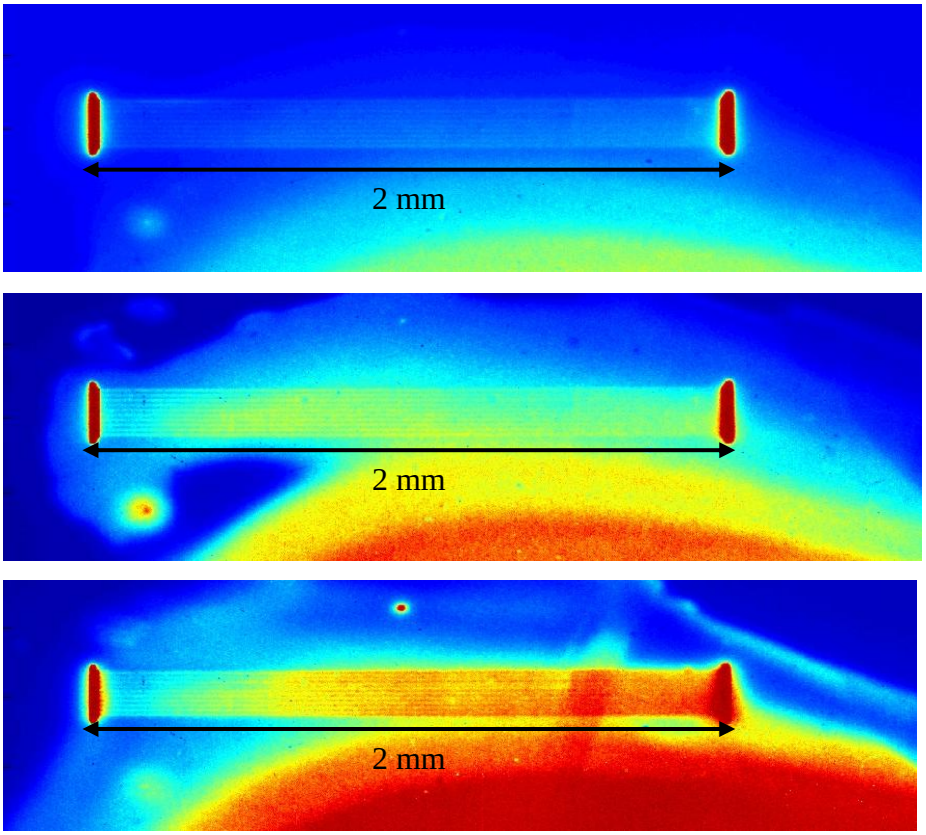

Figure 4.7: False-color image of operating second I-design.

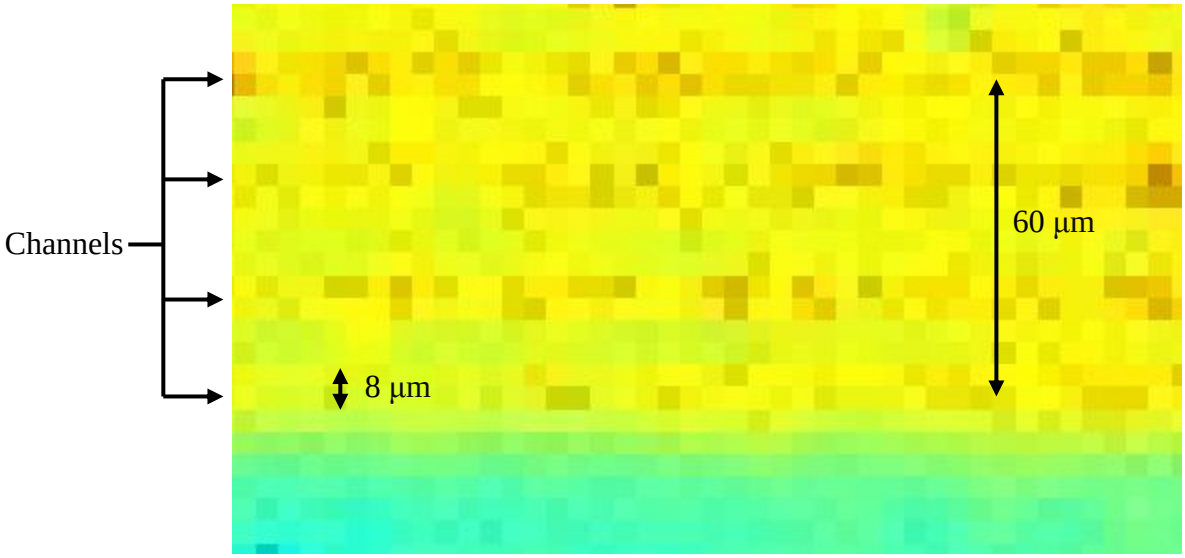

Figure 4.8: Magnified version of Figure 4.7.

Again, using the magnified image of Figure 4.8, the width of the channels can be estimated. The distance between each channel is 20 μm, giving about 4 μm for each pixel. Although the ICCD camera has much greater sensitivity compared to the CCD camera used in this research, the pixel size of this ICCD is bigger than that of the CCD camera. In addition, the ICCD pictures shown above are the results of accumulation of 100 pictures of 100 μs exposure time. Due to this long integration time, small vibrations of the device caused a fair amount of smearing of the images. Therefore, this data set was not adequate to explain the size of the device. However, these images do show that microplasma was successfully ignited along the channels, although the confinement of microplasma could not be verified. Figure 4.9 more clearly illustrates the issues at hand. There was an unavoidable gap between the silicon and glass portions of the device. A surface discharge, therefore, was first formed inside this gap. Microplasmas were also generated near the channels. However, the confinement of microplasma inside the channel could not be checked due to the resolution limit of the ICCD camera and vibration of the experimental setup.

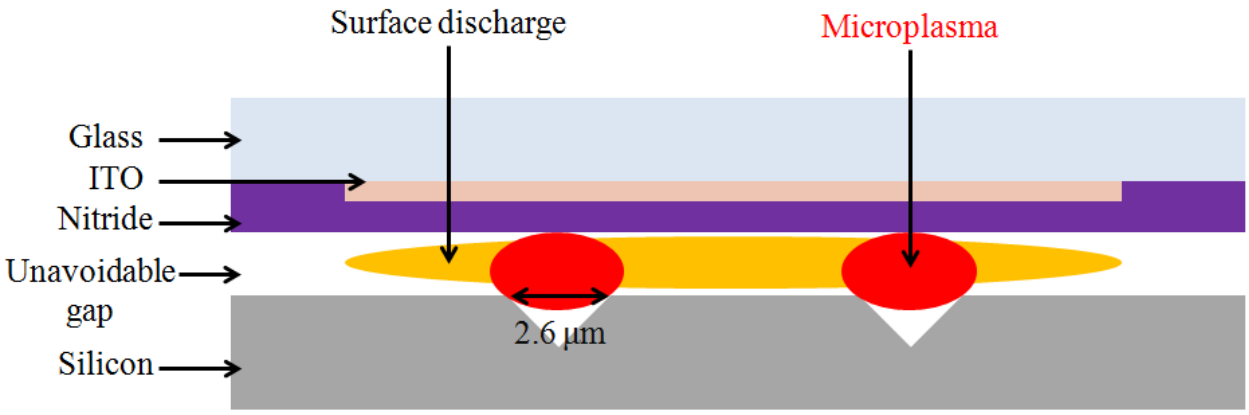

Figure 4.9: Illustration of second I-design.

4.4 Future Work

Attempts to confine microplasma inside 2.5 μm channels are still in progress. There are two problems that need to be solved in order to confine microplasma in a 2.5 μm channel. First, surface discharge must be eliminated in these devices. Even though mechanical force is applied when bonding the silicon and glass parts to make the final device, the gap between them is unavoidable as explained in the previous chapter. This gap between them may even be bigger than the actual channel width. Even if the gap is smaller than 2.5 μm, surface discharge occurs throughout the whole surface of the device and dominates the result of data because it consumes most of the current from the power supply. In order to analyze data for microplasma, this surface discharge must be eliminated first. This can be done by completely bonding the silicon and the glass part by anodic bonding [16]. In order to do so, there must be a structural change to the device and the anodic bonding must be performed before depositing any electrodes because the electrodes cannot survive the high temperature anodic bonding process. Assuming there is no gap between silicon and glass due to anodic bonding, gas inlets must also be fabricated on the device itself to inject gas inside the channel.

The second major issue with plasma confinement in 2.5 μm channels is the required ignition voltage. If channel devices are used instead of I-designs, the required voltage would increase dramatically. In order to sustain these high voltages, new dielectric materials must be used. Silicon nitride deposited with PECVD (the deposition method used in this thesis) has many pinholes [17], and therefore new fabrication techniques must be used. Silicon nitride and silicon dioxide can be either deposited with low-pressure chemical vapor deposition (LPCVD) or grown on the silicon for better dielectric performance. The device structure must be redesigned in order to utilize these fabrication techniques.

5. Conclusion

Downsizing of microplasma from 50 μm to 5 μm and finally to 2.5 μm has been demonstrated. For 5 μm microplasma, an inverse-pyramidal channel structure was used, resulting in a pd curve consistent with the theoretical Paschen's curve of Go and Pohlman [14]. For 2.5 μm microplasma, a new structure with assisted I-design was proposed and implemented to minimize alignment issues and reduce ignition voltage. With this new structure, the possibility of confining microplasma in 2.5 μm or smaller characteristic dimensions was shown. New device structures or modification of the current fabrication techniques will be necessary to confine microplasma in characteristic dimensions smaller than 2.5 μm.

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