TOWARD HIGH-PERFORMANCE, LOW-POWER, CARBON-BASED INTERCONNECTS AND TRANSISTORS

BY

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THESIS

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Abstract

As the physical limits of Moore's law scaling are immediately apparent, industry has explored new ways of pushing technological progress. For integrated circuit applications, major limiting factors are the electrical and thermal performance of interconnects and transistors. This thesis explores two topics, the first regarding future interconnects and the second regarding nanoscale transistors, both based on low-dimensional carbon materials, which could present opportunities for extending Moore's law.

As integrated circuit performance is increasingly limited by interconnect time delays at nanoscale dimensions, graphene nanoribbons (GNRs) may serve as an effective solution. In this thesis, a comprehensive study of sub-50 nm width copper (Cu), aluminum (Al), and GNR interconnects is presented. Existing models are refined to qualitatively understand the size effect, and various interconnect geometries are simulated using finite-element solvers to study coupling capacitance. Aluminum exhibits the best performance for horizontal geometries (where the interconnect width W is greater than the height H) for 5 nm < W < 20 nm due to a superior resistivity; below 5 nm, GNRs offer better performance as coupling capacitance rapidly increases delay in Al and Cu interconnects. For vertical geometries (where H is greater than W), lower Cu resistivity yields the shortest interconnect delay until W < 8 nm; in this size regime, the width-independent GNR resistivity results in superior GNR performance over Al and Cu interconnects.

For nanoscale transistors, as dimensions of traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) decrease, short channel effects degrade performance and limit further scaling. New silicon-based transistors such as the tunneling field effect transistor (TFET) and the impact ionization transistor (I-MOS) use novel carrier injection techniques to improve performance, but do not extend benefits beyond a single generation. For continued scaling, one-dimensional carbon nanotubes (CNTs) appear to be ideal, as their perfect crystalline structure and inherent cylindrical symmetry yield electrical properties superior to that of Si at similar dimensions. Thus, the second part of this document examines the possibility of CNT I-MOS transistors as a way to combine high-performance and low-power operation in highly scaled devices. If successful, the CNT I-MOS may operate at drain-source voltages of only 0.2-0.4 V for a channel length of 100 nm, which represents an order of magnitude improvement in operating voltage over existing Si-based I-MOS designs.

Acknowledgments

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CHAPTER 1
Low-Dimensional Carbon Materials

1.1 Introduction

Sparked by the invention of the first solid state transistor in 1947 by Bardeen, Brattain, and Shockley [1] and fueled by the introduction of the integrated circuit in 1959 by Kilby [2] and Noyce [3], the semiconductor industry has grown enormously, topping $300 billion in 2012 [4]. The rapid industry growth results mostly from Moore's law, named after Intel co-founder Gordon Moore who stated in 1965 that the transistor count of integrated circuits would double roughly every two years [5]. To maintain progress in line with Moore's law, the silicon industry has relied on down-scaling transistor channel lengths, which has allowed more complicated circuitry (i.e. multi-core processors) without increasing overall chip area. For a given supply voltage, channel length scaling also generally increases other performance metrics such as the on-current. Unfortunately, continued down-scaling is increasingly difficult as short-channel-effects (SCEs) negatively affect threshold voltages and subthreshold slopes, reducing device design windows [6]. With the surging popularity of portable devices, maximum power dissipation considerations have imposed even further design restrictions. Coupled with other detrimental effects such as increasing contact series resistance and coupling capacitance [6], nanometer scale physics already restrict transistor scaling to a rate below Moore's law [7].

Currently, the semiconductor industry uses single-generation fixes to silicon (Si) transistors to circumvent detrimental nanoscale effects. One well-known example is the recent replacement of silicon dioxide (SiO_2) gate dielectrics with high-k materials (oxides for which the relative dielectric constant $k > 4$, the SiO_2 dielectric constant). The downscaling of gate-oxide thickness is limited physically to ~2 nm—below this value, gate-leakage currents increase exponentially as carriers quantum tunnel through the gate dielectric [6]. This significantly restricts future transistor design windows as engineers historically down-scaled SiO_2 gate oxides to increase gate-capacitances ($C_{ox} \sim \varepsilon_{ox}/t_{ox} = k\varepsilon_0/t_{ox}$, where $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of free space and t_{ox} is the oxide thickness) and combat SCEs by increasing transistor on-currents ($I_{on} \sim C_{ox}W/L$, where W and L are the channel width and length, respectively). Since k is the only other means of increasing gate-capacitance, industry explored CMOS-processing compatible high-k dielectrics for many years, and as a result, Intel now uses hafnium oxide (HfO_2) in all their latest

processors [8]. Similar patch fixes have been incorporated over the years to overcome other parasitics including increasing contact resistance (raised silicide contacts), decreasing threshold voltages and reduced electrostatic control (metal top gates and the tri-gate or FinFET transistor), and hot carriers which reduced reliability (lightly doped drain profiles) [6]. Unfortunately, despite the enormous research and development efforts (the semiconductor industry spent over $53.4 billion worldwide in 2012 alone [9]), such fixes are effective for only a single generation, and without a direct avenue for advancement, the semiconductor industry has explored new, novel approaches towards "beyond-Moore" computing.

In the ultimate scaling limit, a monolayer of semiconducting material would serve as the channel for transistor operation. However, Si is hardly ideal in this case— the electron mobility, a measure of how easily an electron traverses through a solid, of 0.9 nm thick silicon is only 7 $cm^2V^{-1}s^{-1}$, significantly lower than the bulk value of ~1500 $cm^2V^{-1}s^{-1}$ as transport in the channel is hampered by dangling bonds and surface roughness [10]. Since the degradation is a result of imperfect fabrication processes inherent to all bulk semiconductor materials, the performance degradation is not isolated to SOI technology; similar problems arise with other semiconductors and even occur in FinFETs as the fin width scales down [11].

As crystalline nanomaterials, the carbon allotropes of graphene and carbon nanotubes (CNTs) may replace bulk semiconductors for several reasons: relative abundance and low material cost; fabrication compatible with existing planar CMOS processes; and most importantly, electrical properties superior to those of Si at nanometer scale dimensions. Graphene is a monolayer of carbon atoms arranged in a hexagonal crystal lattice (Fig. 1.1) while a CNT can be visualized as a rolled up sheet of graphene. Compared to Si and bulk semiconductor materials, graphene and CNTs demonstrate extremely high mobility (on the order of 10,000 $cm^2V^{-1}s^{-1}$ [12] for CNTs) resulting from weakly bound cross-plane $2p_z$ electrons, a trait unique to these low-dimensional carbon allotropes. Another exemplary trait of graphene and CNT is high thermal conductivity (~3000 $Wm^{-1}K^{-1}$ [13]), critical for future scaling as power density has also scaled upwards in line with Moore's law [14]. For these reasons, graphene and CNTs are both considered potential channel materials for future CMOS technologies [7]. However, several fabrication issues still hamper full adoption of graphene and CNTs in industry. While these issues will be presented briefly in the following sections, direct work towards improving fabrication problems is outside the scope of this thesis.

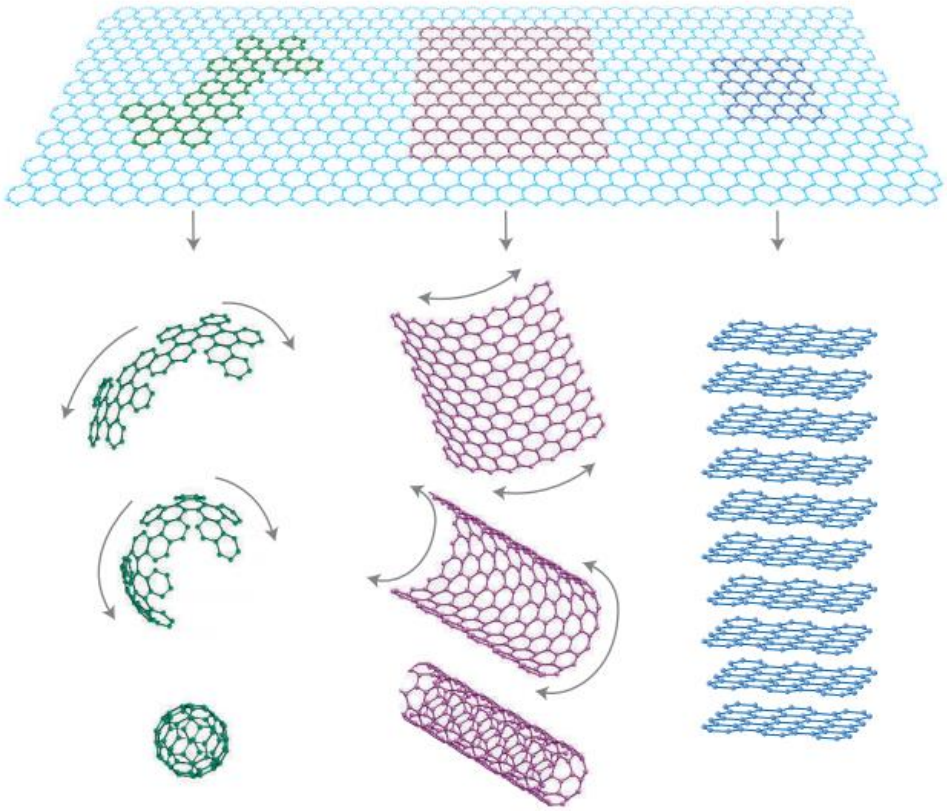

Figure 1.1 The various carbon allotropes, from left to right: zero-dimensional (0D) – buckyballs; one-dimensional (1D) – carbon nanotube; two-dimensional (2D) – graphene [15].

1.2 Two-Dimensional Electrical Properties (Graphene)

Studied theoretically for several decades, graphene was only recently demonstrated experimentally by Novoselov and Geim, who exfoliated monolayers sheets from bulk graphite in 2004 [16]. Since then, multiple researchers have confirmed experimentally the excellent electronic, mechanical, and thermal properties theoretically predicted, resulting in exponential growth of publication coverage. As a planar material easily compatible with existing CMOS processes, graphene is particularly attractive for mass production—as a result of large research efforts towards large-scale graphene production, chemical vapor deposition (CVD) recipes now exist which yield relatively uniform monolayer graphene on copper [17]. While the electrical and thermal properties of CVD graphene are non-ideal due to defects such as wrinkles and grain boundaries, dirty transfer processes, and substrate interactions [18], the ease of graphene production has greatly shifted research focus away from CNTs (Fig. 1.2).

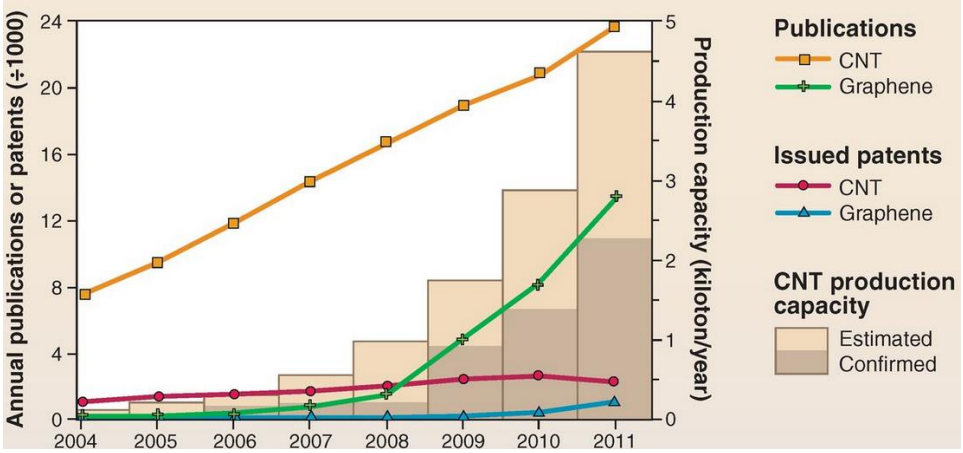

Figure 1.2 Recent publication and production trends for graphene and CNTs [19].

As the band diagram corresponds to the possible states that carriers can occupy, a brief discussion of the band structure is important towards understanding electron transport in graphene. First-principle numerical simulations [20] show that the graphene band structure (Fig. 1.3A) exhibits properties unique even to two-dimensional materials.

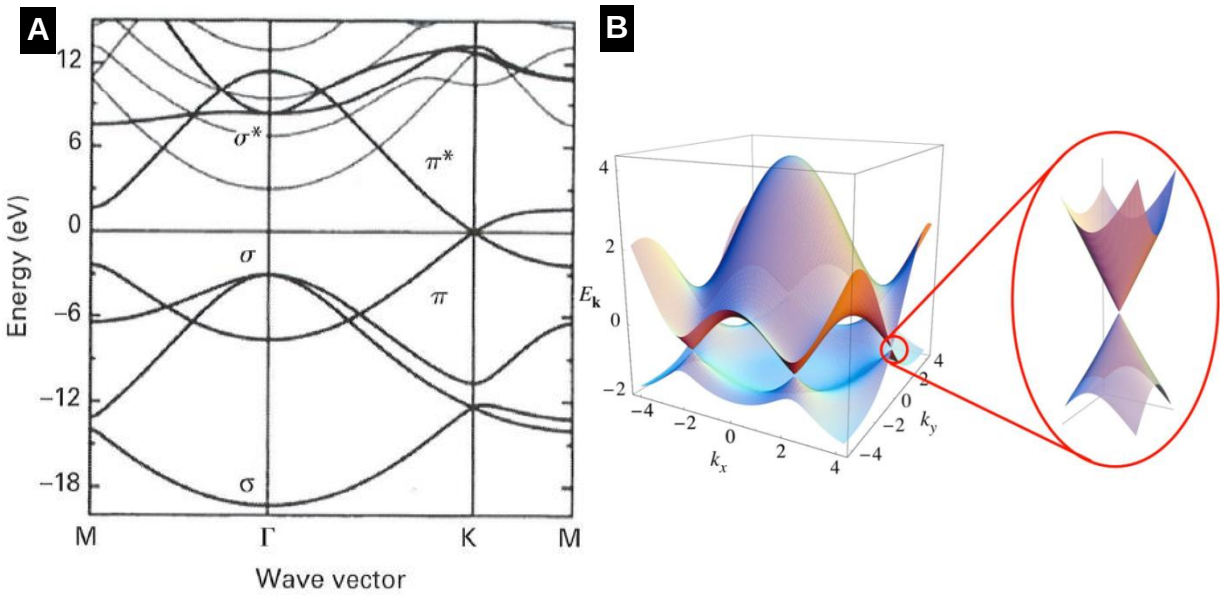

Figure 1.3 (A) Energy band diagram for graphene, including both σ and π bond interactions [20]. (B) Three-dimensional band diagram showing only π bond interactions [23]. The magnified region corresponds to the K point.

Although the band diagram includes all possible states, for most practical device situations, one only needs to focus on low energy behavior, where $E < 2$ eV. In this energy regime, electron transport is described by interactions near the K point. Here, the conduction and valence energy bands are symmetric, giving rise to identical hole and electron (ambipolar) transport in ideal

situations. The bands around the K point are also highly linear, yielding the well-known graphene dispersion relation for energies < 0.6 eV [21]:

$$E(\mathbf{k}) = \pm\hbar v_F|\mathbf{k}| \quad (1.1)$$

where $\hbar$ is the reduced Planck constant, v_F is the Fermi velocity (typically ~10^8 cm/s [22]), and $\mathbf{k}$ is the wave vector.

While the linear dispersion relation is important for transport derivations and physically interesting, other properties of the band structure limit graphene usefulness in digital applications. Precisely at the K point, corresponding at thermodynamic equilibrium to $E = E_F = 0$ eV, the conduction and valence bands meet. This location is frequently referred to as the *Dirac point* (Fig. 1.3B). For classical bulk materials, the overlap of the conduction and valence bands would imply that a material is *metallic*—however, as a result of the linear dispersion relation, the graphene density of states vanishes to zero at the K point. Thus, graphene is commonly referred to as a *semi-metal* since it ideally should be nonconductive in the absence of electrostatic doping, despite the band overlap. Realistically, graphene is always doped to a certain degree by impurities that provide carriers even when graphene is biased at the Dirac point. As a result, on-off current ratios of graphene field-effect transistors (GFETs) rarely exceed 10, far below the >10^4 ratio specified by the ITRS [7]. This fact greatly limits the use of graphene in digital applications where an off-current as low as possible is desirable to minimize static power leakage. According to theoretical studies, narrow strips of graphene nanoribbons (GNRs) may circumvent this problem as nanometer ribbon widths eliminate certain physical quantum states, resulting in a small band gap at the Dirac point [24]. Unfortunately, the GNR edges must be perfect with no dangling bonds for this solution to work—this is far from reality as no known fabrication method exists to make perfect edges. Fortunately, graphene is still relevant for analog applications where managing off-state leakage is not critical, as its high mobility can yield a fast frequency response (f_T as high as 300 GHz have previously been reported [25]).

GNRs may be better suited for passive electrical applications given the current fabrication issues that prohibit ideal active device behavior. As GNRs exhibit a breakdown current density higher than that of copper (~2×10^9 A/cm^2 [26]), one potential GNR use is as an interconnect material. As transistor dimensions scale down, so too do interconnects, the connections combining the transistors. As the widths of these interconnects decreases to nanometer ranges, material imperfections such as grain boundaries and surface roughness contribute greatly to

rapidly increasing interconnect delay times. This thesis includes an in-depth study of graphene as an interconnect material, which shows that several sheets of graphene outperform copper and aluminum at certain nanometer dimensions.

1.3 One-Dimensional Electrical Properties (Carbon Nanotube)

As the one-dimensional member of the carbon allotrope family, the carbon nanotube (CNT) can be best described as a rolled up sheet of graphene. CNTs can be further classified as single-wall and multiwall nanotubes, the latter of which actually contain several concentric tubes. The single-wall nanotube is most relevant for transistor applications as gated behavior is lost with multiwall nanotubes [27]. With the same chemical structure as graphene, carbon nanotubes maintain the same excellent electronic properties of graphene, but exhibit different transport behavior due to their one-dimensional nature. To illustrate this point further, Fig. 1.4 defines and illustrates a few attributes of the CNT crystal lattice.

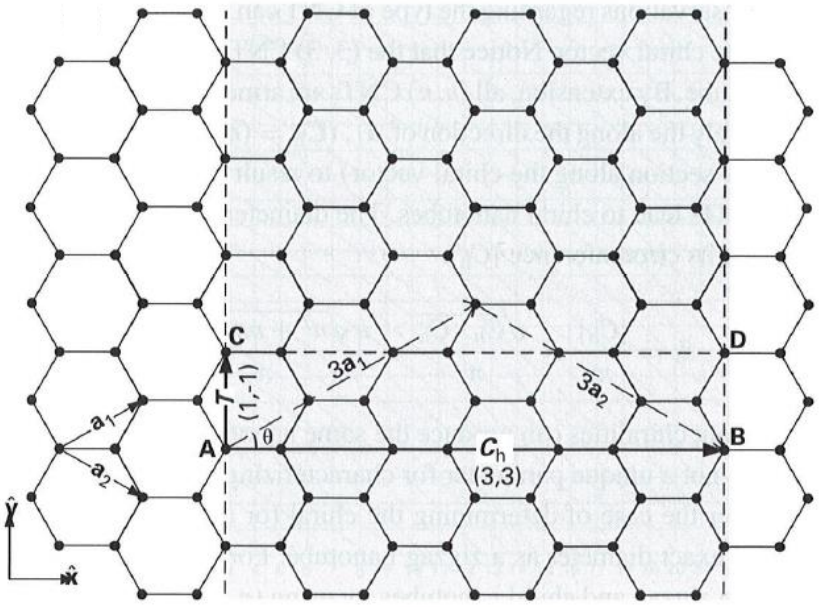

Figure 1.4 Lattice properties for a (*n*, *m*) = (3,3) CNT [21]

$\boldsymbol{C}_h$ is the *chiral vecto*r and connects the two points (in this case **A** and **B**) in a plane of graphene that would meet if the graphene sheet were rolled up (for this reason, it is also sometimes referred to as the *circumferential vector* [21]). Relative to the primitive lattice vectors $\boldsymbol{a}_1 = [\sqrt{3}a/2, a/2]$ and $\boldsymbol{a}_2 = [\sqrt{3}a/2, -a/2]$, where the Bravais lattice constant $a = 2.46$, $\boldsymbol{C}_h$ is given by:

$$\boldsymbol{C}_h = n\mathbf{a}_1 + m\mathbf{a}_2 \quad (n, m \text{ are positive integers with } 0 \leq m \leq n) \tag{1.2}$$

For long nanotubes where the nanotube length $L \gg C_h = |\mathbf{C}_h|$, the Bloch wave function solutions along the circumferential direction in the CNT Brillouin zone are actually discretized—therefore, the allowed CNTs states that comprise the band structure are one-dimensional slices of the graphene band structure, as shown in Fig. 1.5.

Figure 1.5 Diagram illustrating how the CNT can be considered a rolled up slice of graphene. Depending on the slice, the Dirac point can be included, yielding a *metallic* nanotube; otherwise, the nanotube is *semiconducting* [28].

If *n-m* in the CNT chiral vector is an integer multiple of three, the band diagram includes the K-point and a CNT is considered *metallic*. Otherwise, the K-point is eliminated, a band gap results, and the CNT is *semiconducting* [21]. Without chirality sorting, a large distribution of randomly grown CNTs (i.e. CNTs grown via CVD on metal catalysts) will result in a ratio of 2:1 metallic to semiconducting nanotubes, which limits the number of CNTs useable for digital applications.

Despite these processing issues, CNTs are extremely valuable as a nanoscale transistor material since the carrier confinement to one dimension results in transport behavior relatively immune from the SCEs that plague two-dimensional materials [21]. As such, the work presented focuses not on CNT processing, but rather on exploiting unique CNT transistor properties in order to create a high performance device previously found to be impractical with silicon-based technology: the impact-ionization transistor.

CHAPTER 2
Graphene Interconnects

2.1 Introduction

As complementary metal on semiconductor (CMOS) transistor sizes scale down, the connections between transistors start to limit operation times. Growing at a rapid pace, this interconnect delay may reduce maximum critical path delay of integrated circuits (ICs) by as much as 35% in 2020 [29]. The rising time delay of these interconnects is well documented and attributed to a combination of the size-effect and coupling capacitance (Fig. 2.1) as dimensions scale down [30]-[42].

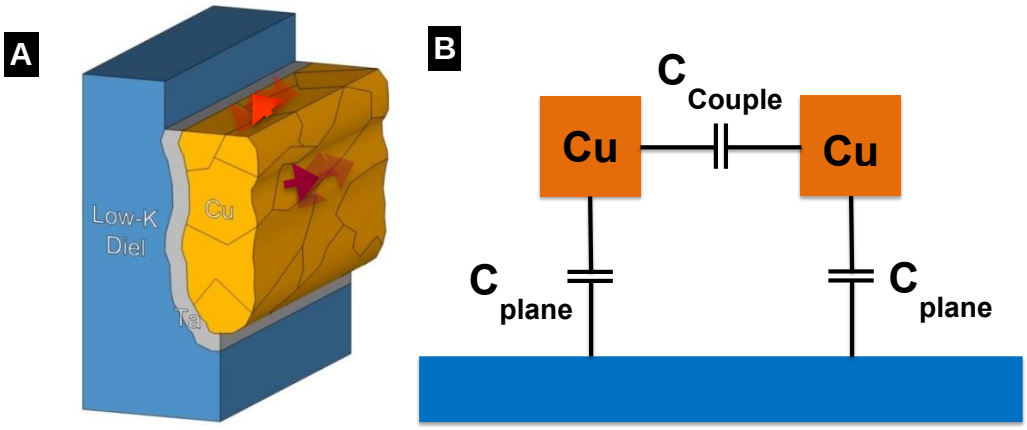

Figure 2.1 (A) Scattering at interconnect sidewalls and grain boundaries begins to dominate at nanometer linewidths, increasing resistivity. (B) Decreased spacing between interconnects results in higher $\mathbf{C_{couple}}$.

In this chapter, the sources of increasing delay in modern interconnects are reviewed. Existing three-dimensional resistivity models are then extended to two dimensions to understand better the size-effect in graphene nanoribbons (GNRs) in the sub-50 nm regime at room temperature. Afterwards, COMSOL finite-element simulation results are presented to explore the capacitive advantages of GNRs over metal interconnects. Finally, the results of both models are combined to obtain resistive-capacitive (RC) delay times.

2.2 The Size Effect and Metal Interconnect Resistivity

At dimensions larger than the mean free path (MFP), electron-phonon scattering dominates bulk resistivity at room temperature. However, as interconnects scale below the mean free path, resistivity rises despite the absence of typical scattering mechanisms. Fuchs first observed this size-effect in metal thin-films, and Sondheimmer later derived an expression dependent solely on

surface scattering (FS model) [30],[31]. Mayadas and Shatzkes later showed a significant contribution to the size-effect from grain boundary scattering for polycrystalline films (MS model) [32]. As these works described only thin-films, Steinhöegl developed a semi-empirical model below that describes rectangular wires [33]:

$$\rho = \rho_{Bulk}\left\{\frac{1}{3}\Big/\left[\frac{1}{3}-\frac{\alpha}{2}+\alpha^2-\alpha^3\ln\left(1+\frac{1}{\alpha}\right)\right]+\frac{3}{8}C(1-p)\frac{1+AR}{AR}\frac{\lambda}{w}\right\} \tag{2.1}$$

with

$$\alpha = \frac{\lambda}{d}\frac{R}{1-R} \tag{2.2}$$

where ρ_{Bulk} is the bulk resistivity, λ is the bulk mean free path, d is the mean distance between grains, AR is the aspect ratio (height over width), w is the width, R is the grain boundary reflection coefficient, p is the surface specularity, and C is a fitting parameter.

The first term and second term in Eq. (2.1) represent the contribution from grain boundary scattering and surface scattering, respectively. Outside of the fitting constant C, all other parameters in Eq. (2.1) have physical meaning. However, there is no method of measuring the specularity (p) nor the reflection coefficient (R), and therefore many works simply assume fully diffusive scattering at the surfaces (p=0) in an attempt to fit the Steinhögl model to their data [34]-[36]. The values obtained using this method do not definitively indicate the dominance of either surface or grain boundary scattering in the size-effect regime, although authors erroneously conclude otherwise [34],[36].

We consult the work of Critchley for a better understanding of the relative contribution of surface and grain boundary scattering to the size-effect [37]. In this study, Critchley examined atomically smooth, pentagonal gold (Au) nanowires with diameters down to 29 nm (well below the mean free path of 38 nm in gold [38]). The wires were crystalline and therefore surface scattering should have dominated. Yet, Critchley observed a miniscule increase in resistivity (2.5 μΩ-cm vs. Au bulk value of 2.2 μΩ-cm) for his atomically smooth samples. This suggests that surface scattering is solely a function of *roughness*, which Eq. (2.1) does not account for. Critchley uses a roughness-dependent specularity model first developed by Soffer and later adopted by Sambles to explain the resistivity increase in cylindrical nanowires due to surface

scattering [39],[40], where λ_B is the bulk mean free path, a is the radius of the nanowire, and H is the RMS roughness height divided by the Fermi wavelength (h_{RMS}/λ_F) [1]

$$\frac{\rho_{Bulk}}{\rho} = 1 - \left(\frac{6\lambda_B}{\pi a}\right)\int_0^{\frac{\pi}{2}} \sin^2\theta\cos^2\theta\, d\theta \int_0^{\frac{\pi}{2}} \sin\psi \frac{\left(1-\exp\left(-\left(4\pi H\right)^2\sin^2\theta\sin^2\psi\right)\right)\left(1-\exp\left(-\frac{2a\sin\psi}{\lambda_B\sin\theta}\right)\right)}{1-\left(\exp\left(-\left(4\pi H\right)^2\sin^2\theta\sin^2\psi\right)\right)\exp\left(-\frac{2a\sin\psi}{\lambda_B\sin\theta}\right)} d\psi \quad (2.3)$$

The main variables in the equation are still the dimensions and the MFP, but of note is the angular dependent specularity term:

$$p(\theta) = \exp\left[-\left(\frac{4\pi h_{RMS}}{\lambda_F}\right)^2 \cos^2\theta\right] \quad (2.4)$$

where θ is the electron angle of incidence normal to the surface, h_{RMS} is the mean roughness height of the surface, and λ_F is the Fermi wavelength of the material. In Sambles's model, the θ dependence disappears by integration over the circular cross section of the wire, and the equation is mainly dependent on h_{RMS}/λ_F, which Critchley labels as H. For $H \ll 1$ (an atomically smooth surface), the size-effect is muted and the model results in near bulk resistivity values; for $H \gg 1$ (a rough surface), the resistivity rapidly increases, approaching values that closely mirror size-effect results reported in literature [37]. By incorporating a measurable roughness parameter, the Sambles's model provides a more physical description of the surface scattering contribution to the size-effect.

To derive a resistivity model for metallic nanowires, Mathiessen's rule can be used to combine Sambles's model for surface scattering with the MS model for grain boundary scattering. This approach implies that surface scattering and grain boundary scattering are independent [30],[41]. Most values used in the calculations (Table 2.1) were pulled from the literature, but derived values (h_{RMS}, R, and $d_{Grain,\,Cu}$) require further discussion.

Both Al an Cu share the same arbitrarily chosen h_{RMS} value as Sambles's model varies little as a function of roughness for $H \gg 1$ [37]. For rough nanowires, a lumped specularity parameter is obtained *without the need for experimental fitting* by equating Sambles's model to the FS model. In doing this, two different physical theories (kinetic theory and Boltzmann transport) are used to explain the same phenomena and obtain values of $p_{Cu} = 0.4$ and $p_{Al} = 0.78$. A value of

R_{Cu} = 0.34 can be obtained for copper by fitting Eq. (2.1) to Steinhögl's data in [33]. With these values for p_{Cu} and R_{Cu}, Fig. A.2 (Appendix A) shows that Eq. (2.1) agrees with other Cu interconnect data in the literature [45]. Without data for aluminum, the value R_{Al} reported in literature for aluminum *thin-films* must be used, which introduces a potential source of error. Finally, as Cu grain size is a function of line width due to the damascene fabrication process, the model includes a quadratic fit (Fig. 2.2A) based on grain sizes reported in copper thin-films and interconnects [33],[41]. With the methodology fully explained, the resistivity of circular Al and Cu nanowires is plotted in Fig 2.2B using the modified Sambles-MS model. Note that Al exhibits a lower resistivity than Cu at ~8 nm. Although partially explained by the constant grain size of Al, the superior resistivity results from the lower λ_F and λ_{MFP} values for Al, which indicate that the size-effect is less pronounced in Al than in Cu.

Table 2.1 Resistivity Model Parameters

	Aluminum	**Copper**
$\rho_{bulk,300K}$	2.82 μΩ·cm [42]	2.2 μΩ·cm [41]
λ_{MFP}	19.8 nm [42]	39 nm [41]
P	0.78	0.4
R	0.59 [42]	0.34
d_{Grain}	20 nm [43]	See Fig 2.2
λ_F	0.36 nm [44]	0.46 nm [44]

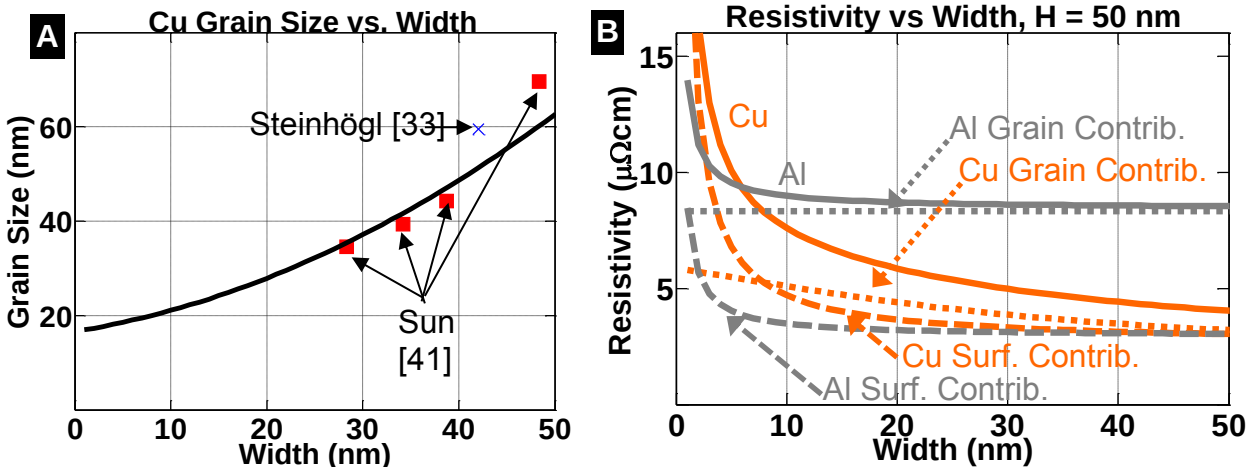

Figure 2.2 (A) Grain size vs. line width of sub-50 nm Cu interconnects. (B) Resistivity of rectangular Cu and Al nanowires as function of width.

2.3 Graphene Resistivity Modeling

To treat GNR resistivity, the Fuchs resistivity model is re-derived for two-dimensions:

$$\frac{\rho_0}{\rho} = 1 - \left(\frac{2\lambda_{MFP}}{\pi W}\right)\int_0^{\pi} \sin^2\theta\left|\cos\theta\right|\left\{\left(1-p(\theta)\right) - \frac{(1-p(\theta))^2\exp(-W/\lambda_{MFP}\left|\cos\theta\right|)}{\left[1-p(\theta)\exp(-W/\lambda_{MFP}\left|\cos\theta\right|)\right]}\right\}d\theta \quad (2.5)$$

where ρ_0 is the bulk resistivity, W is the GNR width, and $p(\theta)$ is the angle-dependent specularity [30]. The model is then fit to both Murali's experimental data [43] and Naeemi's theoretical work [47] to yield GNR resistivity values. While this data set is the most comprehensive available, the GNRs studied were not optimally doped; for practical IC applications, graphene can be doped up to ~10^{14} cm^{-2} [48] (see Appendix A for other values considered). The results of two-dimensional resistivity model (Eq. (2.5)) are not directly comparable to the three-dimensional model (Eq. (2.1)), and thus the GNR resistivity results obtained from Eq. (2.5) have not been plotted in Fig. 2.3 to avoid confusion. Nevertheless, this model is used later to generate the resistance values for 500 nm long GNR interconnects.

2.4 COMSOL Capacitance Simulations

As transistor sizes shrink, industry is fast approaching dimensions where interconnect coupling capacitance is on the order of inverter load capacitance [49]. Whereas the resistance can be decreased by shortening the interconnect length, this coupling capacitance is not easily adjusted. Therefore, any method to reduce coupling capacitance leads to a valuable reduction of the circuit RC delay times (τ).

To understand the possible GNR benefits in terms of coupling capacitance, COMSOL, a finite element solver, is used to simulate the capacitance of two different interconnect configurations. These configurations are referred to as the horizontal and vertical configurations (Fig 2.3). In the horizontal configuration, the graphene mono-layer conduction plane is oriented horizontally. Interconnect spacing is given by $S = 2 \cdot W$, where W is the interconnect width. The height (H) of the graphene monolayer is set to 0.34 nm, while the H of Al and Cu is set to 5 nm. In the vertical configuration where the multi-layer GNR's thickness varies (W), the conduction plane is oriented perpendicular to the ground plane. Here, H = 50 nm and S = 22nm for Al, Cu and GNR's. To calculate the capacitance, each configuration is simulated with V_1 = 1.8 V and V_2

= 2.8 V applied to the center conductor, and all other surfaces grounded. The other pertinent simulations parameters are found in Table 2.2.

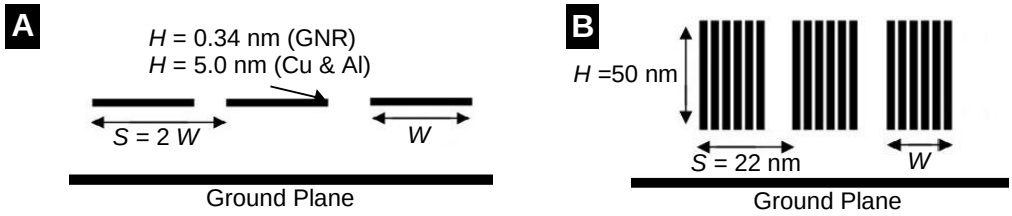

Figure 2.3 (A) Horizontally oriented interconnects. (B) Vertically oriented interconnects. Note all GNR sheets in one block are at same potential and no capacitive coupling exists between sheets in one block. We therefore simulate a block with width *W* for the vertically oriented GNR stacks.

Table 2.2 COMSOL Simulation Parameters

Configuration	Material	Height (H)	Spacing (S)	Dielectric Constant	Ground Plane Distance
Horizontal	GNR	0.3 nm	S=2*W*	4.2	300 nm
Horizontal	Al, Cu	5 nm	S=2*W*	4.2	300 nm
Vertical	GNR, Al, Cu	50 nm	S=22 nm	4.2	30 nm

The surface charge density over the center conductor is then integrated to obtain $Q(V)$ (charge per meter). The capacitance is obtained by the following equation with L = 500 nm:

$$C = \frac{\Delta Q \cdot L}{\Delta V} = \frac{\left(Q(V_2) - Q(V_1)\right) \cdot L}{V_2 - V_1} \tag{2.6}$$

The capacitance results in Fig. 2.4 show that, in the horizontal configuration, mono-layer GNR's maintain a much lower coupling capacitance than Al and Cu for all *W*. In particular, GNR's are ideal below 10 nm as the capacitance of Al and Cu interconnects increases exponentially. To understand the advantages of a vertical configuration in terms of reduced ground plane coupling capacitance, a ground plane is placed 30 nm below the interconnects. As shown in Fig 2.4, the capacitance changes little below 15 nm, even for very small *W*, indicating a large fringing capacitance to the ground plane. Above 15 nm, the capacitance increases exponentially as coupling capacitance dominates.

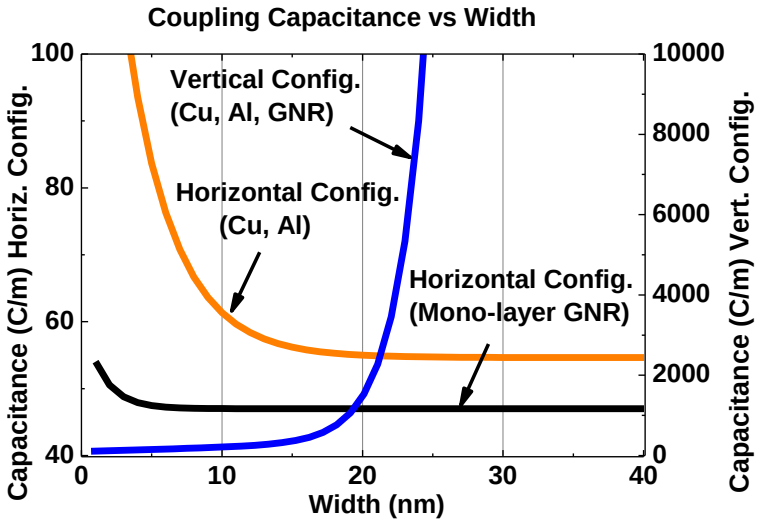

Figure 2.4 Resulting capacitance as a function of width *W* from COMSOL simulations.

2.5 RC Delay Time

To calculate the RC time delay (τ), the resistance is multiple with the capacitance for all *W*. Along with the parameters derived in Table 2.1, the FS-MS model is used to generate Al and Cu resistance values. Note that for Cu resistivity, the finite width of the Ta liner is taken into account. This increases the width of the copper interconnects by 2 nm [46]. Note also that high-frequency skin effects are *not* taken into account since the impact on resistance is negligible for frequencies below 10 GHz [50]. In addition, below 50 nm, the size effect dominates over the skin effect, regardless of frequency. For GNR resistivity, the value varies depending on configuration. In the horizontal configuration, Eq. (2.5) is fitted to Naeemi and Murali's data to generate resistivity values. For the vertical configuration, the GNR resistivity is a constant GNR 10 μΩ-cm, reflecting the use of *W* as the *thickness* of the GNR (line edge roughness contribution is constant).

In the vertical configuration (Fig. 2.5), τ increases as $W \rightarrow 0$ due to size effects and as $W > 20$ nm due to coupling capacitance. With a much lower bulk resistivity value (2.2 μΩ-cm), the τ of Cu is superior for intermediate values of *W*. However, the resistivities of the vertical GNRs are independent of the IC width (LER only on top and bottom), allowing τ to remain lower than that of Cu and Al below ~8 nm.

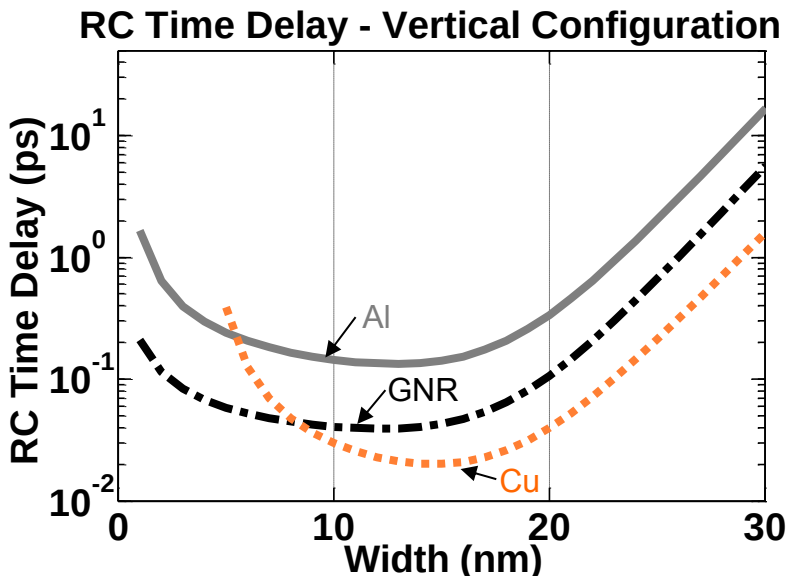

Figure 2.5 Vertical configuration with GNR *S* = 22 nm. Cu is best for intermediate values of *W* due to low bulk resistivity, but GNR's are better below ~8 nm.

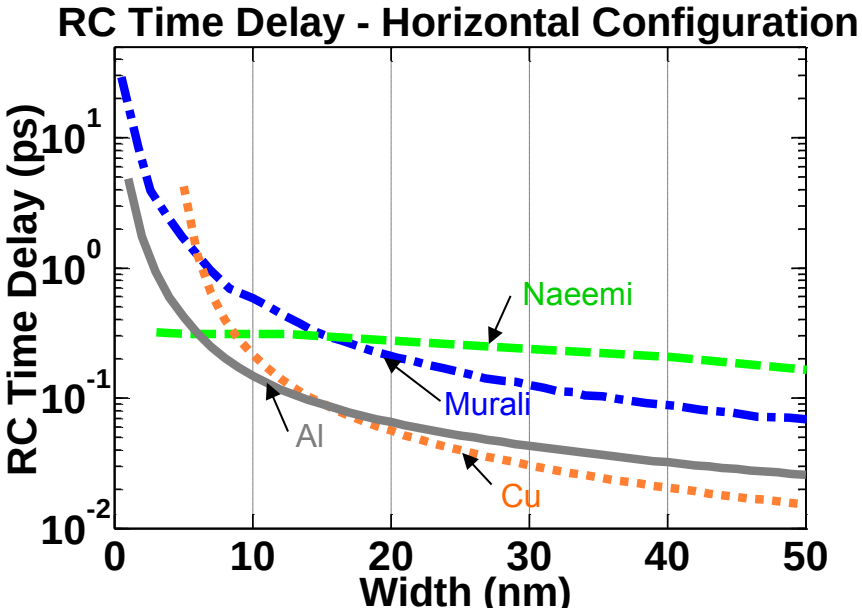

Figure 2.6 Horizontal configuration. Al is superior at widths < 15 nm due to a lower resistivity.

The results of the horizontal configuration are shown in Fig. 2.6, where the lower delay of Al at 5 nm < W < 20 nm is due to a lower resistivity. Below ~5 nm, GNRs should theoretically offer better performance as coupling capacitance dominates delay in metal ICs. However, the most relevant experimental data currently available [46] suggest that GNRs on SiO2 could outperform both Cu and Al below ~6 nm. (This observation is subject to change, when more experimental data on highly-doped GNRs becomes available.)

CHAPTER 3
Carbon Nanotube I-MOS

3.1 Introduction

As industry can no longer rely on channel scaling to maintain continual increases in circuit complexity, novel designs such as tunneling field-effect transistors (TFETs) and impact ionization MOS (I-MOS) transistors may yield greater performance than conventional silicon MOSFETs. The basic operation of the TFET shown in Fig. 3.1 is as follows: in the off state, the tunneling of carriers from the source into the channel is negligible, and the leakage current is dictated by the reverse-biased p-i-n junction. As the gate is biased towards the on-state, the channel region bands are pushed further down, increasing the band bending between the channel and the source for this n-type device. The electrons are thus able to tunnel directly from the valence band into the conduction band, resulting in a subthreshold slope (SS) as low as 43 mV/dec for Si devices [51]. Unfortunately, for Si TFETs, I_{on} is lower than that of classical MOSFETs due to a wide band gap, which restricts the number of tunneling carriers. Yet, the low power operation (as low as V_{dd} = 0.5 V [52]) makes the TFET an attractive candidate for next generation devices.

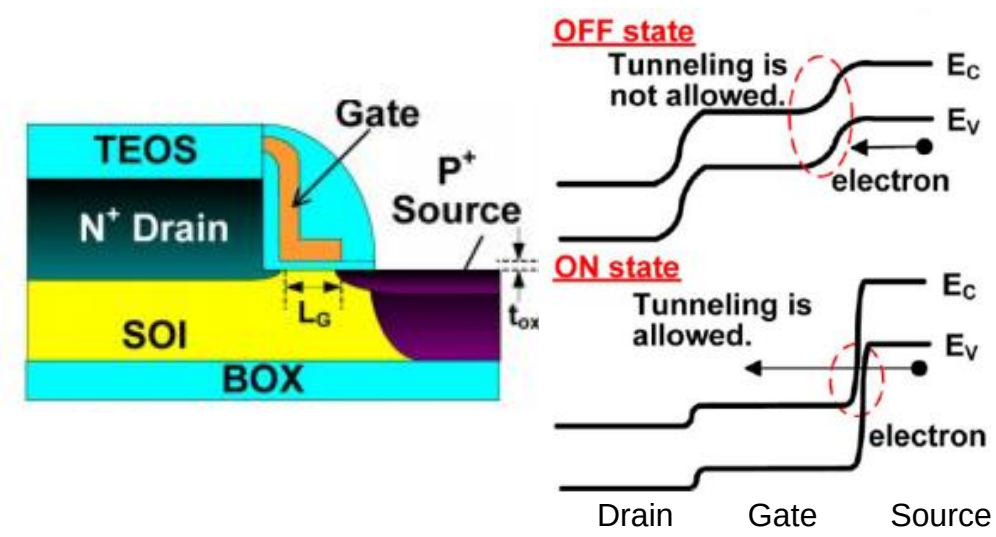

Figure 3.1 Summary of TFET off and on state operation [53].

For high-performance applications that require a high I_{on}, the I-MOS transistor is an alternative that achieves even steeper SS. In the I-MOS transistor, the channel is biased into the region where impact ionization (also known as avalanche multiplication) occurs. With impact

ionization, carriers in the channel gain energy from the high field, colliding with atoms, and releasing bound electrons from. These carriers are then free to repeat the process of electron-hole pair generation, thus providing a source of carrier gain by which rapid current saturation occurs. The I-MOS (shown in Fig 3.2) originally proposed by Gopalakrishnan in 2002 [54] consists of a gate that covers only a portion of a p-i-n junction. With the gate on, the lateral potential drop underneath the gate is reduced, shortening the region along which the rest of the potential drops. The resulting fields in the exposed region, called L_I, are strong enough to induce impact ionization.

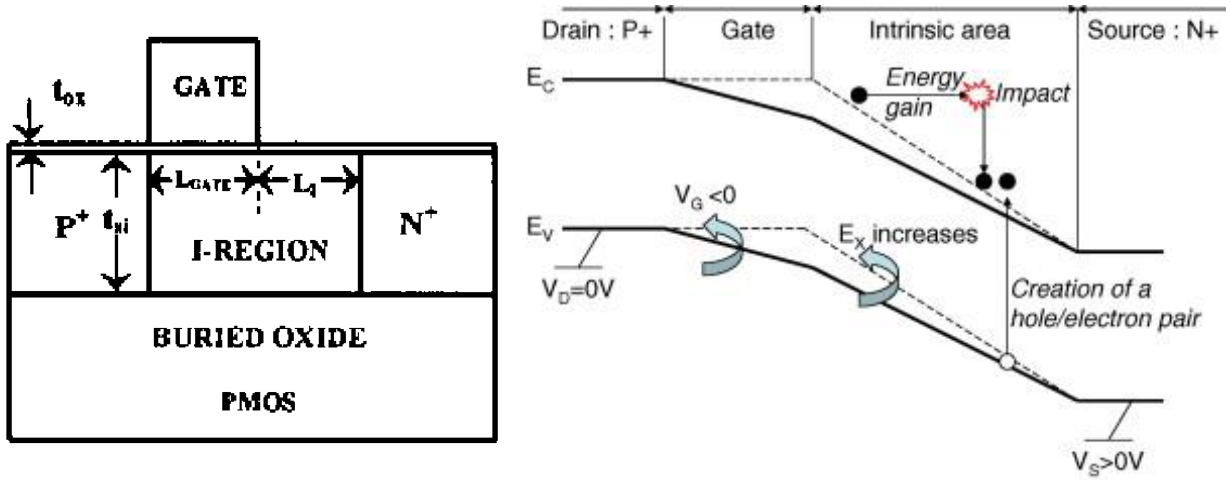

Figure 3.2 Cross section of partially-gated Si IMOS device [54] and corresponding band diagram [55]. In the band diagram, the off-state corresponds to the solid line in the channel while the on-state corresponds to the dashed line.

Si I-MOS devices have demonstrated subthreshold slopes of 3 mV/dec [56]—however, as this particular device was operated at $|V_{GS}|$ = 5.5 V to induce impact ionization, the increased performance came at the cost of operating voltages far exceeding values required for modern applications. The lack of impact ionization voltage scaling with channel length is another issue preventing I-MOS implementation– studies show that impact ionization saturates at 100 nm at gate voltages of roughly 4.5 V for Si due to SCEs [57]. Finally, the delay for the seed carrier that triggers impact ionization can be significant depending on the length of the intrinsic region. For L_I = 50 nm, the seed carrier delay has been predicted to be a few picoseconds [58], which may pose a fundamental limit on how quickly these devices can be turned on.

3.2 Avalanche in Carbon Nanotubes and CNT I-MOS

When compared to the wealth of studies conducted for Si devices, impact ionization in CNTs is not as well-understood. However, CNTs exhibit traits that may make them ideal for low-power avalanche operation. For example, large diameter semiconducting CNTs (d_t > 1 nm) result in a band gap smaller than that of Si, potentially leading to enhanced impact ionization. Also, the reduced dimensionality of CNTs results in stronger electron-electron interactions, which also suggests more favorable conditions for impact ionization [59].

One of the first experimental reports of impact ionization in CNTs in 2008 by Liao [60] confirms some of these assumptions. For this study, Liao fabricated back-gated CNT FETs of various channel lengths and measured these in a vacuum so as to prevent catastrophic breakdown. Some of his results are shown below in Fig. 3.3 [60].

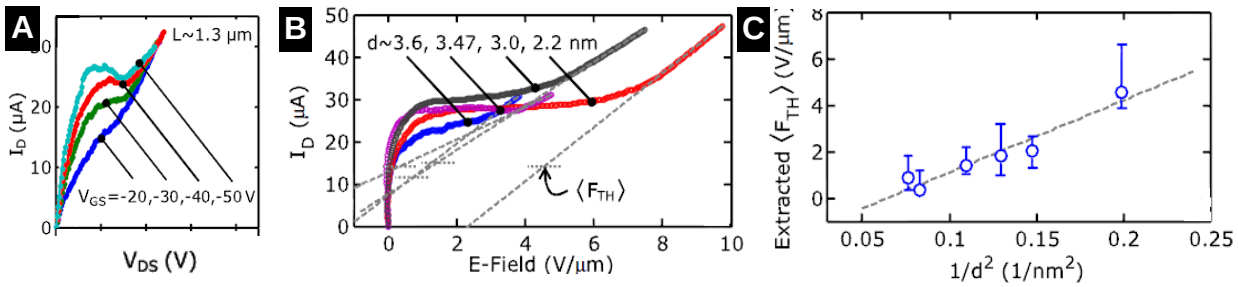

Figure 3.3 (A) I_d vs V_d plots for L = 1.3 μm device. The onset of impact ionization is independent of gate voltage. (B) Drain current as a function of drain field with impact ionization threshold F_{th} labeled. F_{th} occurs at lower fields for larger diameters, which results from a smaller band gap. This trend is verified with the plot shown in (C). [60]

In Liao's work, the increase in current beyond the saturating limit of 25 μA was attributed to impact ionization due to the high drain voltages applied—band to band tunneling was also considered, but the probability was deemed too low for this to be the dominant factor. Liao found that for a given length, the onset of impact ionization occurs at the same source to drain field (source-drain fields of at most ~10 V/μm for d ~ 2 nm), suggesting the impact ionization voltage can still scale with the channel length. Note that for an equivalent diameter tube, impact ionization could be induced at only 0.2-0.4 V for a channel length of 100 nm. As the applied gate biases were large enough to occupy the third subband, the paper also discussed another source of impact ionization via inter-band excitation [61]. However, given that the onset of impact ionization was observed for all gate voltages above the threshold, this observation does not seem to be a necessary requirement. Thus, while the gate voltages reported (V_{GS} = -20 V) would usually be concerning, high voltage operation can be avoided if the device is optimized for

traditional impact ionization through carrier-atom interactions in the channel rather than through inter-band processes. Nevertheless, Liao's study provides the only glimpse of impact ionization in CNTs. Other subsequent studies have tried to study impact excitation of carriers, focusing on exciton generation [59], but another study is clearly necessary to study the impact ionization scaling and CNT ionization rates. Such a study would be significant not only to explore fundamental physics, but also to determine technological feasibility of CNT IMOS technology.

As stated earlier, Liao's paper demonstrated that impact ionization could occur in CNTs at voltages much smaller than necessary for Si devices. However, Liao's device was not optimized for impact ionization operation—in particular, the use of a back-gated structure with 90 nm of SiO_2 not only exposes the CNT to ambient air conditions where CNTs break down rapidly, but also results in non-optimal electrostatic control of the channel. For more efficient impact ionization, this work reintroduces the top-gated structure first introduced by Gopalakrishnan for Si devices, with a few fabrication modifications to make the design more suited for CNTs—this device is referred to as the CNTFET IMOS (Fig. 3.4A).

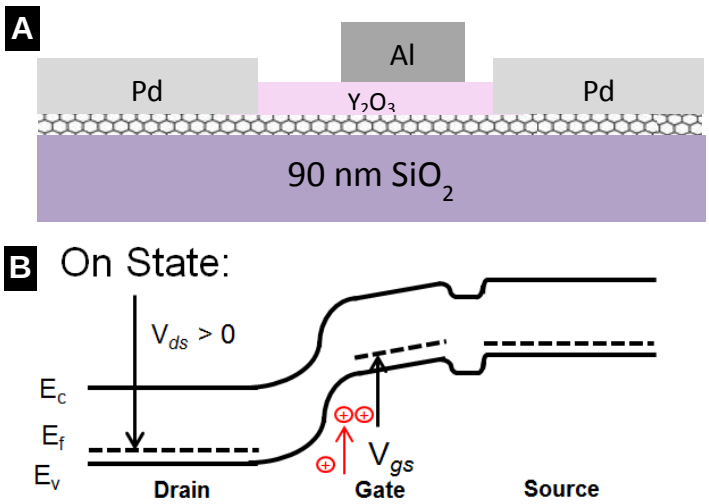

Figure 3.3 (A) Cross section of CNTFET I-MOS and (B) band structures in off and on state. As this is a p-type device, V_{ds}> 0 to maintain reverse bias while V_{gs}< 0 to electrostatically dope the gated region to p-type.

For a p-type CNTFET IMOS, the band structure along the channel is shown qualitatively in Fig 3.4B. Despite the presence of a p-i-p channel for the CNTFET I-MOS, operation is the same as Gopalakrishnan's original Si device with a p-i-n channel. The prototype CNTFET I-MOS gate metal is composed of Al, chosen to slightly deplete the CNT of holes in the off-state, as shown in Fig.3.4B by the slight shift of the Fermi level underneath the gate region towards the conduction band. By depleting the channel regions of holes, this gate stack should be an effective method of

minimizing the off-current without resorting to potentially destructive implant doping techniques. The choice of high-*k* Y_2O_3 is non-conventional, but is a result of local processing limitations—the interested reader should consult Appendix B for further information. The source/drain contacts consist of Pd contacts. As the work function of Pd (~5.22-5.6 eV [62]) is larger than that of the semiconducting CNT (~4.5 eV [63]), the band bending of the CNTs underneath the contacts favors hole transport. Thus, the CNT Fermi level at equilibrium underneath the contacts is shifted closer to the valence band.

For on-state operation, a negative gate bias is applied to the gate, electrostatically doping the gate region to p-type and therefore aligning the channel Fermi level to that of the source. Like in the Si I-MOS, the gate bias shortens the region over which the majority of the potential drops, inducing impact ionization. Since the gate in this configuration does not overlap the source contact, a critical design parameter is the drain to gate spacing. As the potential drop across this region must be kept to a minimum, the gate must be within a few mean paths of the source to ensure quasi-ballistic transport of the carriers. Also, given the efficiency of impact ionization in CNTs, properly biasing the CNTFET I-MOS may prove problematic. Impact ionization may be induced at very low drain biases, depending on channel lengths. The devices would thus be independent of applied gate voltage, which undermines transistor operation—capturing this design aspect via a critical parameter will certainly be necessary to fully characterize the CNTFET I-MOS.

3.3 Fabrication

For full detailed fabrication steps up to source/drain deposition, please consult Appendix C. A brief description of the CNFET IMOS fabrication corresponding to Fig. 3.5 follows: iron catalyst windows are first defined on the substrate wafers (90 nm SiO_2 on p++ Si) using optical photolithography techniques. Iron is then deposited via electron-beam (e-beam) evaporation and lifted off, leaving behind rectangular catalyst features. The deposited catalysts serve as carbon seed sites for crystalline nanotube growth via chemical vapor deposition (CVD) in a quartz furnace. Once the nanotubes are grown, yttrium oxide (Y_2O_3) is deposited everywhere via thermal evaporation. The source/drain windows are defined via optical photolithography, where the Y_2O_3 is etched away using hydrochloric acid (HCl). Palladium (Pd) contacts are then deposited via e-beam evaporation, followed by lift-off. The top gate is then defined using e-beam lithography to define submicron channels. Once the channels are defined, aluminum (Al) is

deposited and lifted off, thereby completing the structure. For proof of concept, the first iteration of devices will have L~ 1 μm, but have a gate length around 0.5 μm (resulting also in L_I = 0.5 μm). Upon successful completion of the first device, dimensions will be reduced further to study scaling effects.

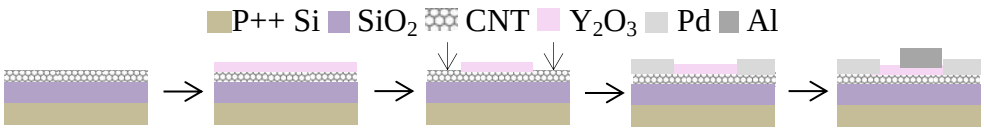

Figure 3.5 CNTFET IMOS fabrication. CVD growth and photolithography steps are eliminated for simplicity. The fabrication steps are as follows: yttrium oxide (Y_2O_3) is deposited on the CNT via e-beam evaporation. Source/drain windows are opened up using optical photolithography and the exposed Y_2O_3 is etched away using HCl. Pd is then deposited and lifted off, leaving behind Pd source/drain pads in the exposed regions. Finally, the top gate is defined using e-beam lithography, Al is deposited and lifted off, resulting in the final structure.

3.4 Modeling

While the current up-kick in Liao's back gated CNTFETs was clearly a result of impact-ionization, a partially-gated CNTFET may have a rapid upswing due either to impact-ionization, band-to-band tunneling, or even a combination of both. To determine the dominant physical effect, a variety of physical models can be used. However, while Monte Carlo, finite element, or first principles models may provide the most accurate results, this is often at the expense of long computation times. Since we are interested in only qualitatively understanding the relative contributions of impact-ionization and band-to-band tunneling to overall conduction in high-field CNTFETs, simpler analytical models can be used. For band to band tunneling, Jena [22] derived a temperature dependent current equation for semiconducting CNTs:

$$I_{BTBT} = \frac{2g_v q^2}{h} T_{WKB} \times V_T \ln\left[\frac{1}{2}\left(1+\cosh\frac{V}{V_T}\right)\right] \tag{3.1}$$

where

$$T_{WKB} = \exp\left[-\frac{\pi}{4}\cdot\frac{E_g^2}{\hbar v_F qF}\right], V_T = \frac{k_b T}{q} \tag{3.2}$$

g_v is the valley degeneracy (g_v = 2 for CNTs [64]); v_F is the Fermi velocity (v_F ~ 10^8 cm/s [22]); T is the temperature (T = 300 K); $V = F \cdot L$ is the channel potential with applied field F and nanotube length L; and E_g = 0.9/d eV, where d is the nanotube diameter in nanometers [21]. For

avalanche, Liao's original equation is still the most accurate physical description of avalanche in CNTs.

$$I_{II} = I_s \exp\left(E_1 / q\lambda_1 F d^2\right) \tag{3.3}$$

where I_s is the saturation current, E_1 and λ_1 are the threshold energy and MFP for a nanotube with d = 1 nm [60]. Figure 3.6 shows the results of Eqs. (3.1) and (3.3) for three diameters (d = 1 nm to 3 nm) as a function of drain field—for all cases, impact ionization is dominant, implying that impact ionization will be the major mechanism behind a steep SS in a partial gate CNTFET.

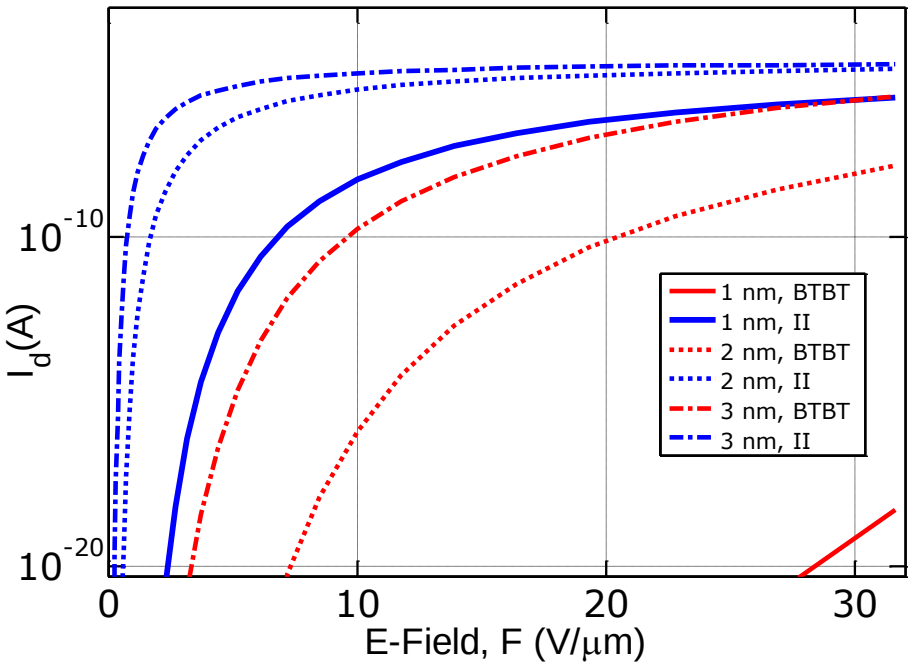

Figure 3.6 Band-to-band tunneling (BTBT, Eq. (3.1)) and impact ionization (II, Eq. (3.3)) drain currents in a CNTFET where L = 1 μm. For all simulated diameters, impact ionization dominates conduction.

CHAPTER 4
Conclusions and Future Work

In this work, both graphene interconnects and the carbon nanotube impact ionization transistor were presented as means of extending future integrated circuits progress beyond Moore's law. In the graphene interconnect study, finite-element COMSOL simulations show that horizontal GNRs can reduce coupling capacitance for sub-10 nm dimensions. Depending on horizontal or vertical configuration, RC time delays of Al and GNRs may be lower than those of Cu at linewidths below ~8 nm.

Full experimental realization of the GNR resistivity simulation results is not yet possible given the current state of fabrication technology. The vertical GNR configuration is particularly difficult to fabricate, as no known method exists by which GNRs can be stacked densely in a vertical manner. The horizontal configuration is easily achievable; however as stated previously, current GNR resistivity values are not competitive with Cu and Al interconnects. Novel doping methods must be further explored to dope GNRs and lower resistivity without electrical damage. As the technology matures, simulation results can be updated as more realistic LER, grain size, and GNR resistivity data become available.

With an order of magnitude more efficient avalanche process than found in Si I-MOS devices, the CNTFET I-MOS proposed yields a high performance transistor (subthreshold slope < 60 mV/dec) with low operating voltage (V_{DS} ~ 0.2-0.4 V at channel length of 100 nm). Work on this device is ongoing—if initial devices are successful, a full scaling study will follow to determine optimal IMOS operating voltages. Analytical CNT IMOS equations will also be derived from existing work on p-i-n diodes in other semiconductor materials and fit to experimental data. These equations can then be extended to compact models, which can assist future circuit designers to study and incorporate the CNT IMOS in the next generation of high-performance, low-power devices.

APPENDIX A
Supplementary Material for GNR Interconnect Study

A.1 GNR Resistivity Compilation

Figure A.1 plots the results of simulations and experimental measurements of GNR resistivities from various sources. In addition to the resistivity values discussed in the main body, simulated results by Xu are included [65]. These values are displayed in the purple, red, blue, and green curves and incorporate a specularity (p) into a linear response Landauer approach using Mathiessen's rule. Xu's results for undoped and AsF_5 doped GNRs, shown in Fig. A.1, reveal that fully diffuse edge scattering can increase the resistivity in GNR's by up to an order of magnitude. AsF_5 doped graphite, which has been reported to have a resistivity of 1.68 μΩ-cm, is shown to outperform Cu for $p > 0.8$ [66]. Also shown in Fig. A.1 is the result of a computational study by Naeemi [47].

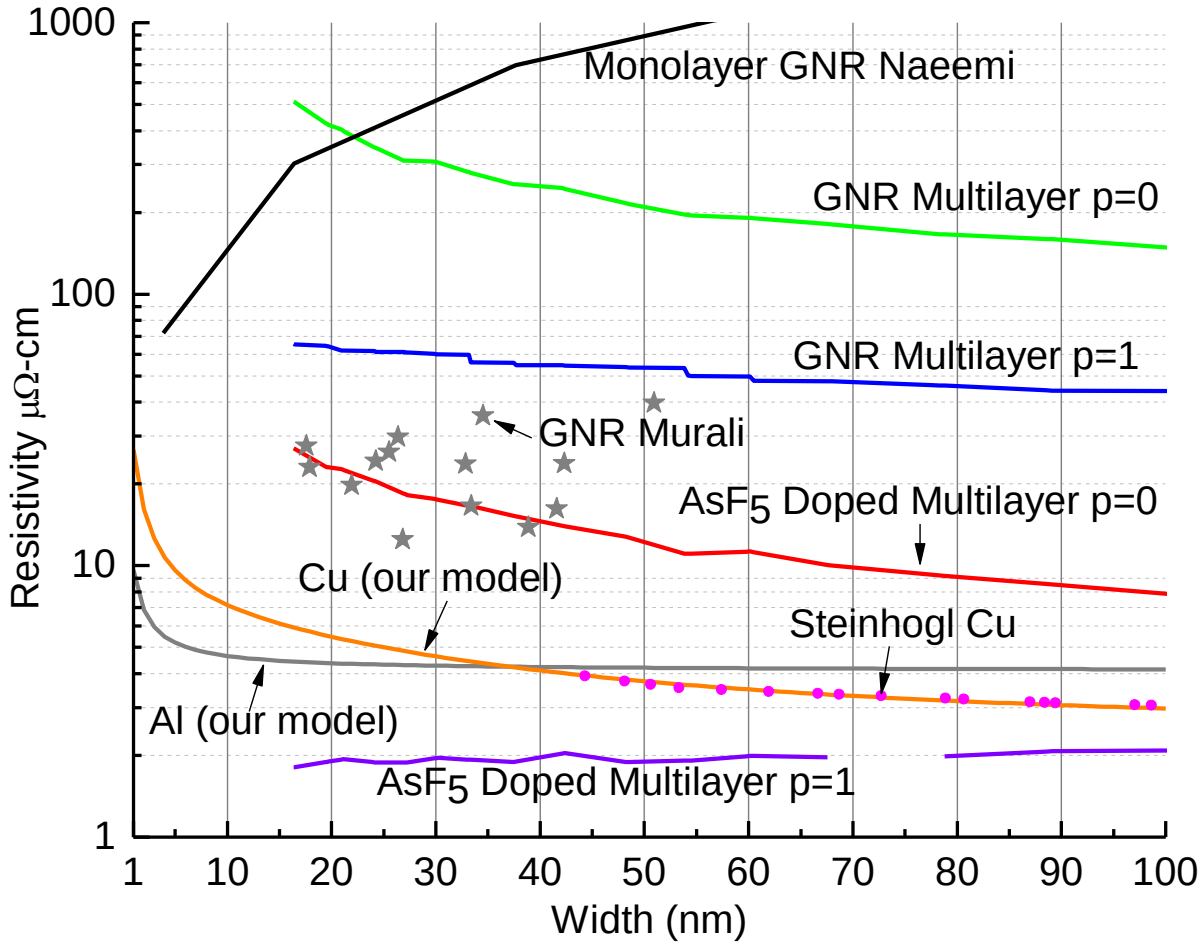

Figure A.1 Resistivity vs. line width for GNR interconnects [47],[65],[66].

A.2 Model Comparison with Literature

Figure A.2 plots the Steinhögl FS-MS size-effect model with our Sambles' derived fitting parameters (p = 0.4, R = 0.34) for copper. For comparison, Fig. A.2 also plots the only other data present in the literature besides Steinhögl's for widths below 50 nm [45]. Our model with the fit agrees well, although we had to increase our grain size function by a factor of four to fit the data better. This would mean the grain sizes are very large, muting the contribution due to grain boundary scattering, but as [45] does not provide any grain measurements, we can only assume this is correct based off the SEM images, which do not show any grains despite the small line width.

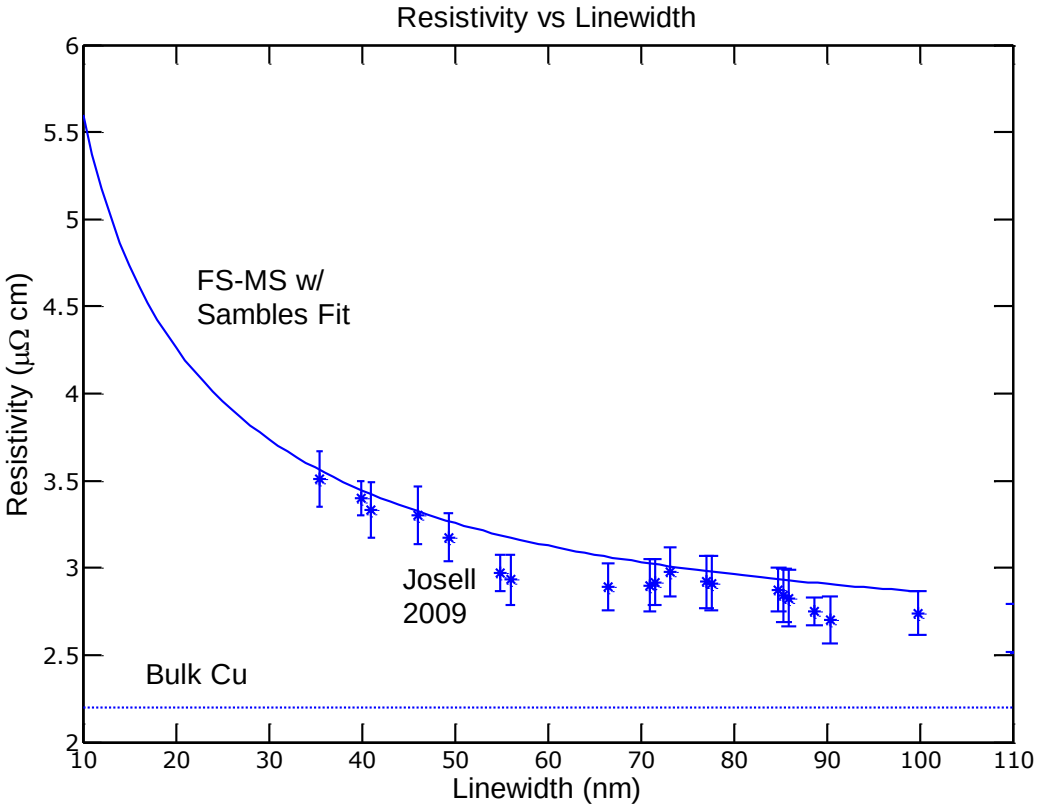

Figure A.2 Resistivity vs. line width of sub-100 nm Cu interconnects [45].

APPENDIX B
CNT Top Dielectric Selection

Atomic layer deposition (ALD) of thin (< 10 nm) high-k dielectric on CNTs is nontrivial as CNTs are crystalline with no dangling bonds. For this reason, several potential dielectrics were reviewed first before fabrication trials began.

Table B.1 Potential CNT Top Dielectrics

AUTHOR	JOURNAL	DIELECTRIC	Capacitance	Leakage	SS (mV/dec)
V. Sangwan [67]	ACS Nano (2012)	VA-SAND (6 nm)	630 nF/cm^2 **	10^{-7} A/cm^2	~ 150
Z. Chen [68]	IEEE EDL (2008)	NO_2 Functionalized w/ ALD Al_2O_3 (7 nm)	--	--	250
A. Javey [69]	**Nano Lett (2004)**	**ALD HfO_2 (8 nm)**	**2.9 pF/cm ***	**10^{-10} A**	**70**
A. Javey [70]	Nat Mat (2002)	ALD ZrOx (8 nm)	5 pF/cm *	~pA	70
S. K. Kim [71]	**APL (2007)**	**ALD Al_2O_3 (15 nm)**	--	**~pA**	**105**
Z. Wang [72]	**Nano Lett (2010)**	**Evap Y_2O_3 (5 nm)**	**1200 nF/cm^2, 1.5 pF/cm ***	**~pA**	**60**

* Theoretical values estimated from models fit to experimental top-gated CNT devices.
** Experimental values measured on parallel plate graphene configurations.

The **bold** entries in Table B.1 were explored directly in this work as they met the following requirements necessary for successful fabrication of a high-performance FET:

- High-k and thin film deposition to maximum electrostatic control.
- High coverage and low leakage to minimize off-state power leakage.
- High deposition quality to minimize hysteresis.
- Fabrication compatibility with standard CMOS processes for industrial relevance.
- Ease of deposition within tool capabilities at the Micro and Nanotechnology Laboratory (MNTL) at the University of Illinois Urbana-Champaign.

To test deposition quality, electrical I_d -V_g and I_d -V_d sweeps of back-gated CNTFET devices before and after dielectric deposition were performed in an air environment using a Keithley 4200 Semiconductor Characterization System (SCS). A high quality, non-destructive process

should result in nearly identical backgated electrical characteristics before and after dielectric deposition. The test parameters are as follows:

- Low field (V_d = 0.05 V) I_d -V_g sweeps at 0.25 V gate steps to confirm semiconducting behavior.
- I_d -V_d sweeps from V_d = 0 V to 8 V at 0.25 V drain steps (V_d limited to 8 V to prevent joule break down in air). V_g was varied to make sure CNT is on and saturated.

Figure B.1 is the measurement results for 15 nm of Al_2O_3 deposited at 200 °C using the Cambridge Nanotech ALD at MNTL. HfO_2 results were also measured, but not shown as the behavior post-deposition is very similar.

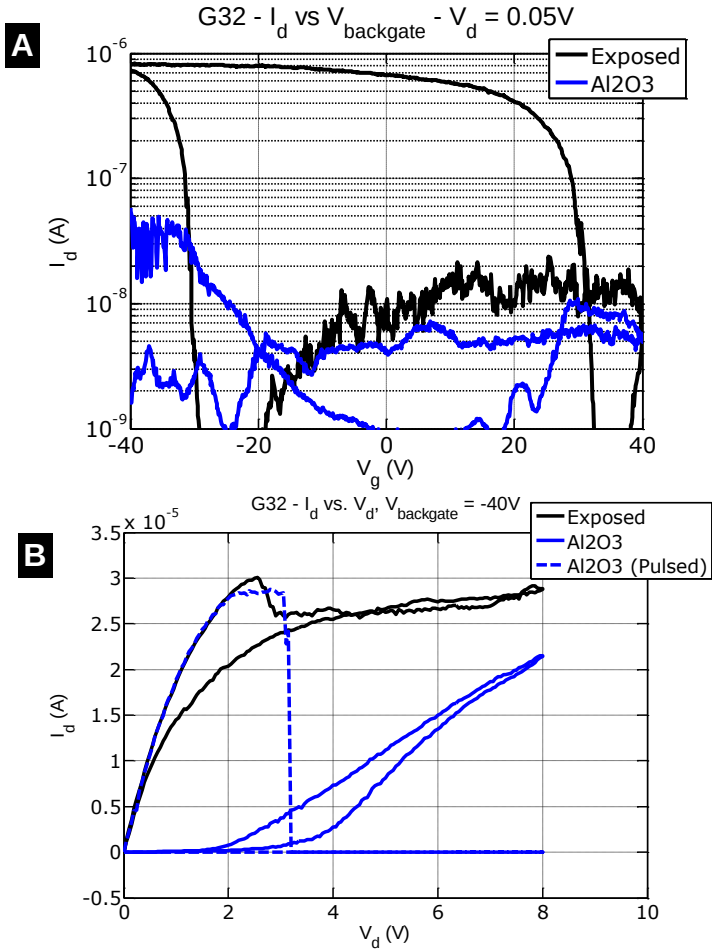

Figure B.1 (A) Low-field (V_d = 0.05 V) I_d vs. V_g curves for a backgated CNTFET device (L ~3 μm) before and after deposition of 15 nm Al_2O_3. Deposition of top-dielectric greatly degrades electrical performance, lowering on-current and introducing hysteresis. (B) I_d vs. V_d curves for V_g = -40 V. Post dielectric deposition, drain current is also degraded. Pulsed measurements (t_{on} = 0.1 s, t_{off} = 1 s) recover original CNT behavior, but CNT is evidently damaged during Al_2O_3 deposition as the CNT breaks down prematurely.

For both dielectrics, the on-current is reduced and hysteresis worsens post-deposition; however, the reason for electrical degradation differs between the two dielectrics. For HfO_2, the presence of an optical phonon mode at an energy far lower than present in CNTs (~50 meV [73] vs. the CNT value of ~160 meV [21]) greatly suppresses the on-current. The Al_2O_3 deposition process, on the other hand, appears to introduce defects. This hypothesis is supported by Fig. B.2, where a pulsed $I_d - V_d$ measurement (for which hysteretic behavior is minimized) recovers ideal CNT behavior until the drain current sharply drops to zero at $V_d \sim 3$ V. Further scanning electron microscopy (SEM) analysis (Fig B.3) shows that the CNT is completely destroyed by this measurement, indicating that the Al_2O_3 deposition process damages the CNT enough to induce premature breakdown.

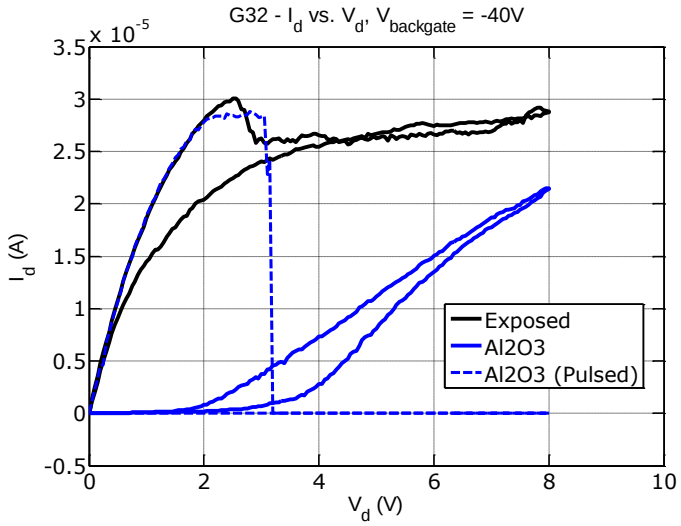

Figure B.2 I_d–V_d sweep of device G32 before and after Al_2O_3 deposition. Ideal device performance is recovered only with pulsed measurement, which promptly destroys the device at $V_d \sim 3$V.

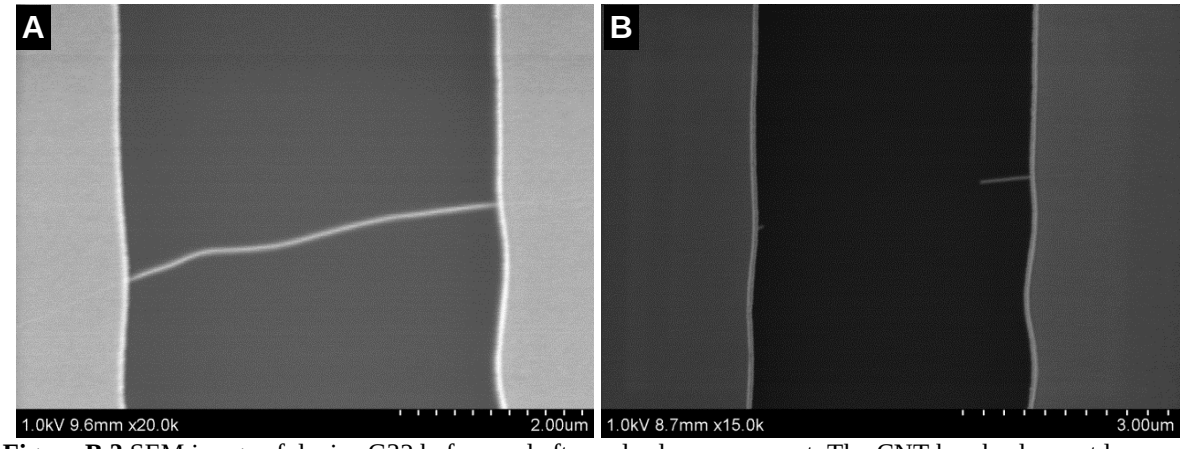

Figure B.3 SEM image of device G32 before and after pulsed measurement. The CNT breaks down at lower voltages when covered with Al_2O_3 than when exposed to air, suggesting a destructive Al_2O_3 deposition process.

For these reasons, evaporated Y_2O_3 was then pursued, despite its relative industrial obscurity. Previous academic results [72] indicate that the Y_2O_3 deposition method process (done at room temperature in a high-vacuum environment) for this dielectric is nondestructive and preserves the excellent intrinsic CNT properties. Figure B.4 shows the initial results of ~3 nm yttrium deposited in a Cooke Thermal evaporator, which then oxidizes in air to form Y_2O_3. These results are promising, with in-air measurements reproducing results similar to those reported in [72]. While further testing is necessary to establish long-term reliability, Y_2O_3 so far appears to be the preferred top-dielectric material for the CNT I-MOS.

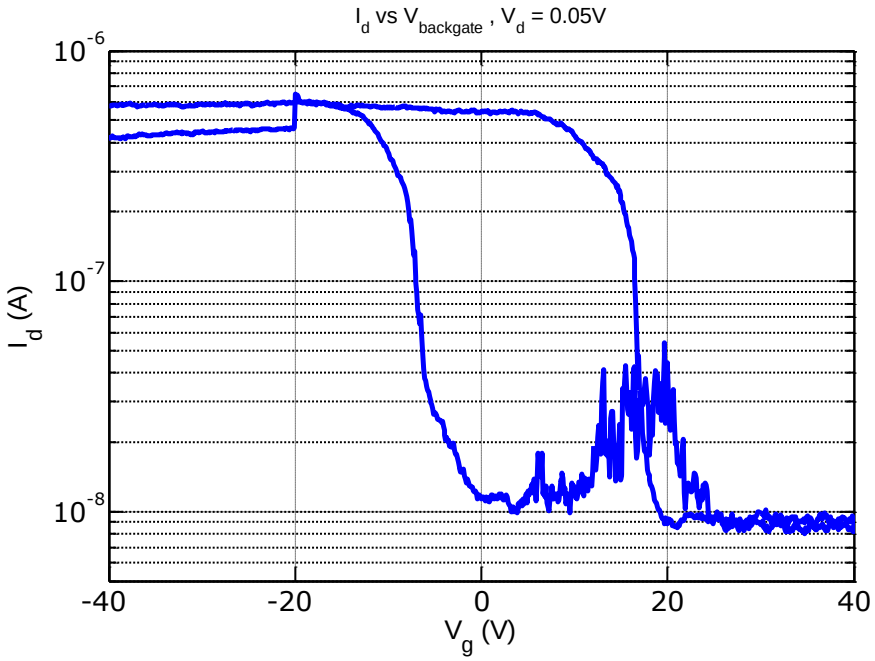

Figure B.4 Low field measurement of Y_2O_3 coated CNTFET. Hysteresis and drive current are on par with other, exposed devices. No exposed data exists for this device as it was fabricated using a dielectric-first process.

APPENDIX C
Back-gated Carbon Nanotube Field Effect Transistor Fabrication Steps

C.1 Etch SiO_2 Markers (Mask Layer 1)

1. Degrease wafer [Acetone → Methanol → Isopropyl Alcohol (IPA) → Deionized Water (DI) → IPA].
2. Bakeoff @ 125 °C for at least 120 seconds in air.
3. Drop Hexamethyldisilazane (HMDS) while spinning at 3000 rotations per minute (RPM). Amount depends on wafer size (general rule is 6 drops with eyedropper). Stop spinner as soon as color ceases to change.
4. Coat wafer with Shipley Photoresist (PR) S1813, spin @ 3000 rotations per minute (RPM) for 30 seconds.
5. Prebake at 110 °C for 90 seconds.
6. Align wafer to first marker set of PopMask and expose using Karl Zuss for 5 seconds. Note time may change depending on aligner lamp intensity.
7. Develop PR in MF319 for at least 25 seconds or for ~10 seconds after features are exposed.
8. Post-bake at 110 °C for 120-135 seconds.
9. Etch down to Si with 10:1 Buffered Oxide Etch (BOE) for at least 100 seconds.
10. Remove PR in acetone. Degrease wafer (see Step 1).

C.2 Putting Down Catalysts (Mask Layer 2)

1. Piranha etch substrate (make your own, 3:1 Sulfuric Acid: Hydrogen Peroxide recommended) for at least 10 minutes.
2. Bakeoff @ 200 °C for 5 minutes.
3. Spin on @ 5000RPM for 30 seconds.
4. Postbake @ 175 °C for 5 minutes exactly.
5. Spin on PR S1813 @ 5500 RPM for 30 seconds.
6. Prebake @ 110 °C for 90 seconds.
6. Align wafer to second marker set of PopMask and expose using Karl Zuss for 5 seconds. Note time may change depending on aligner lamp intensity.

8. Develop off PR with MF319 for at least 50 seconds or for ~10 seconds after features are exposed. MAKE SURE THAT YOU CAN SEE THE SUBSTRATE THROUGH THE CATLYST HOLES.
9. Deposit 1-2 Å of iron (Fe) via CHA electron-beam evaporation at base pressure of ~10^{-7} Torr.
10. Liftoff in Remover PG for 10 minutes at an elevated temperature. When removing the sample from Remover PG, you should soak it in IPA for a bit to remove residue and then degrease it.

C.3 Nanotube Growth

Growth conditions vary by furnace. For the 1" Atomate Furnace located in the Micro and Nanotechnology Lab (MNTL) at the University of Illinois, the following steps serve as a good starting point:

1. Follow furnace instructions for loading a sample and open the argon (Ar), methane (CH_4), and hydrogen (H) gas lines. BE SURE TO LEAK CHECK AFTER STARTING PROCESSES.
2. Anneal substrate @ 900 °C in 500 standard cubic centimeters per minute (SCCM) of Ar for ~40 minutes.
3. Reduce substrate @ 900 °C in 500 SCCM H for 5 minutes.
4. Grow carbon nanotubes in 500 SCCM CH_4 and 90 SCCM H for 20 minutes.
5. Post-growth anneal @ 400 °C in 700 SCCM Ar for 10 minutes.
6. Change anneal conditions to 400 °C in 500 SCCM Ar/500 SCCM H for 40 minutes
7. Set furnace temperature to 0 °C and cool furnace in 500 SCCM Ar for ~30 minutes.
8. Once thermocouple reads ~150 °C, shut off all gas values and unload sample.

To get higher density increases the flow rate of carbon feedstock gases or decrease the flow rate for hydrogen. Do the opposite for lower density.

C.4 Depositing Metal Source/Drain Contacts (Mask Layer 3)

1. Bakeoff @ 200 °C for 5 minutes.
2. Spin on PMGI SF6 @ 3500RPM for 30 seconds.
3. Postbake @ 160 °C for 5 minutes exactly.
4. Spin on PR S1813 @ 5000RPM for 30 seconds.
5. Prebake @ 110C for 75-90 seconds.

6. Align wafer to third marker set of PopMask and expose using Karl Zuss for 2-3 seconds. Note time may change depending on aligner lamp intensity.
7. Develop off PR with MF319 for ~85-90 sec. MAKE SURE THAT ALL PMGI IS REMOVED AND UNDERCUTTING PR.
10. Postbake @ 110 ^{o}C for 90 seconds.
11. Deposit metal (2 Å of titanium, 40 nm palladium) via CHA e-beam evaporator. Operate CHA in manual mode for better results.
12. Liftoff in Remover PG for 10 minutes at an elevated temperature. When removing the sample from Remover PG, you should soak it in IPA for a bit to remove residue and then degrease it.

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