DESIGN TECHNIQUES FOR TEMPERATURE INSENSITIVE, LOW PHASE NOISE OSCILLATOR

BY

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THESIS

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ABSTRACT

A reference clock generator is one of the most important components in many electronic devices. Common clock references are based on quartz crystals which offer high quality factor, good phase noise performance and excellent stability against temperature, voltage and process variation. However, due to incompatibility with silicon integration and high power consumption, they are not suitable for biomedical devices which require long battery lifetime, low cost and especially small size but do not require near-crystal accuracy. This thesis focuses on eliminating the quartz crystals and generating reference clock on a silicon chip. Moreover, this thesis proposes a way of combining two major oscillator types available in CMOS (RC and Ring) technology, while preserving the unique qualities of both of them and coming up with the proposed RCR (resistor-capacitor-ring) oscillator, that offers an excellent alternative for biomedical devices and wireless sensor networks. We coin the term RCR signifying the proposed approach of combining RC oscillators with ring oscillators to achieve a performance better than the performance of individual RC and ring oscillators.

In order to generate stable clock frequency against temperature and supply variations a novel CMOS reference clock oscillator is proposed which exploits the RC and ring oscillator performances, providing the best of both worlds in performance. The proposed oscillator employs a supply-regulated ring oscillator in a feedback loop that follows a frequency insensitive RC oscillator, which minimizes the frequency sensitivity to supply and temperature variations. The clock oscillator achieves negligible frequency variation against supply variation of 1.1 V to 1.3 V and $\pm 0.37\%$ against temperature variation of -40 °C $\sim$ 125 °C. In addition, low power consumption is achieved by using mostly digital circuitry operating at very low frequencies. Even the phase noise performance of the proposed oscillator shows a very high FoM of about 160 dB at the offset frequencies of 100 kHz and 1 MHz. This stabil-

ity to temperature and supply along with excellent noise performance is the unique cornerstone of RCR oscillators proposed in this thesis, which cannot be found in any full-CMOS oscillators. When the performance of the clock oscillator is compared to that of the recently reported low power CMOS reference clock oscillators, the frequency variation to supply variation is reduced to zero, temperature sensitivity is also improved by approximately a factor of 3 and normalized power consumption to frequency output is reduced by a factor of 5. The proposed CMOS clock oscillator is implemented in 65 nm TSMC CMOS technology and consumes just 220 μW from 1.2 V supply at an output frequency of 50 MHz.

To my Mother, for her love and support.

ACKNOWLEDGMENTS

I am using this opportunity to express my gratitude to everyone who supported me throughout the course of my master's study. I am thankful for their inspiring guidance and friendly advice during the project. I am sincerely grateful to them for sharing their truthful and illuminating views on a number of issues related to my study, my research and my thesis.

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LIST OF ABBREVIATIONS

ASIC	Application-Specific Integrated Circuit
BBPD	Bang-Bang Phase Detector
CMOS	Complementary Metal-Oxide Semiconductor
CP	Charge-Pump
CS	Common Source
D-PLL	Digital Phase-Locked Loop
DAC	Digital-to-Analog Converter
FoM	Figure-of-Merit
LC	Inductor-Capacitor
LP	Loop Filter
LVT	Low Voltage Threshold
P2D	Phase-to-Digital
PLL	Phase-Locked Loop
PVT	Process-Voltage-Temperature
RC	Resistor-Capacitor
RCR	Resistor-Capacitor-Ring
SoC	System-on-Chip
TDC	Time-to-Digital Converter
VCO	Voltage-Controlled Oscillator
XCO	Crystal-Controlled Oscillator

CHAPTER 1

INTRODUCTION

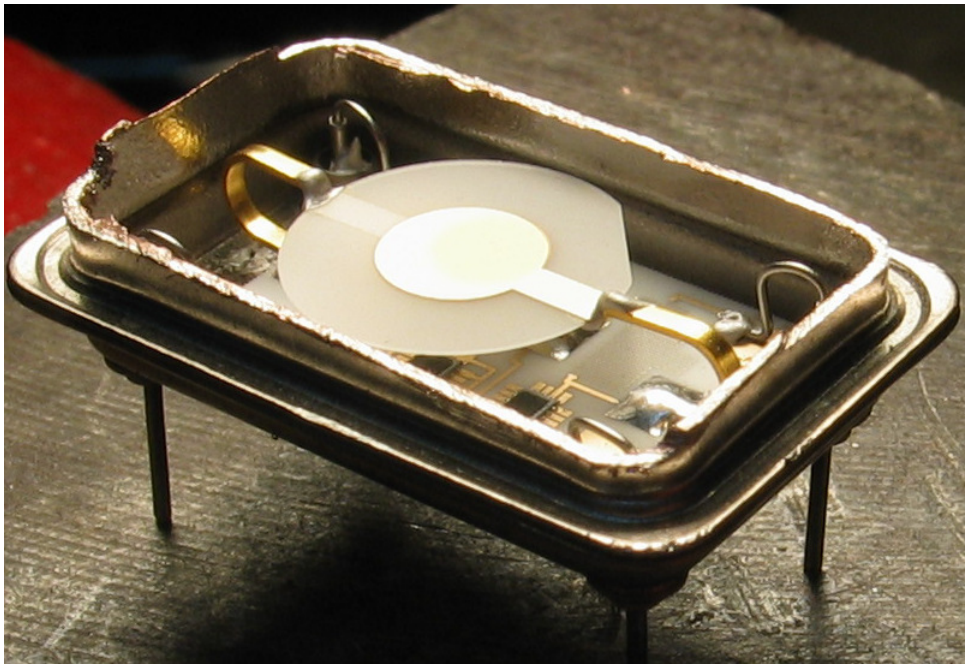
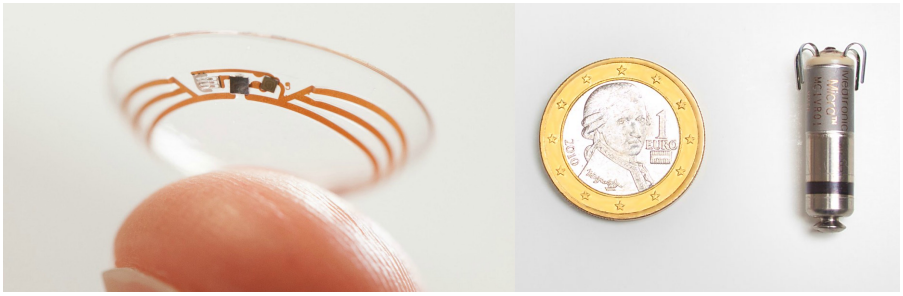


Figure 1.1: Packaged Crystal Oscillator

1.1 Motivation

A reference oscillator is one of the most important components in many electronic devices. Common clock references are based on quartz crystals shown in Fig. 1.1 which offer high quality factor, good phase noise performance and excellent stability with silicon integration and high power consumption. However they are not suitable for biomedical devices in Fig. 1.2, which require low cost, small size and near crystal accuracy. Hence we investigate on-chip clock generation without the use of crystal oscillator. In this thesis we propose and demonstrate a CMOS oscillator solution for sensors and



(a) Retina Chip (b) Pacemaker

Figure 1.2: Biomedical Devices

biomedical devices.

CMOS oscillators for biomedical devices and sensors require 3 pivotal properties. Firstly, the oscillator should generate stable frequency against process, voltage and temperature (PVT) variations. Secondly, the oscillator should demonstrate excellent phase noise performance. And lastly, it should consume low power in addition to being integrable in a very small area.

Many works focusing on eliminating the quartz crystals in clock and frequency generators have recently been presented. RF MEMS micro-resonators have received attention as replacement components of the crystal due to their excellent stability and high-Q [1],[2]. However, these approaches still suffer from the compatibility with standard CMOS process technologies, and therefore their use in the low cost and small area applications is restricted. This problem of RF MEMS micro-resonators has stimulated alternative research such as RF temperature-compensated LC oscillators (RF-TCLCOs), which can be monolithically integrated with standard CMOS process technologies [3]. However, this approach is not suitable for biomedical devices and wireless sensor networks in spite of the compatibility with standard CMOS process technologies, since it consumes too much power. The RF-TCLCOs consume 10s of mW mainly due to the high bias current that guarantees stable operation and dividers that scale the RF frequency to the desired reference frequency at few 10s of MHz. Previous works for low-power low-cost applications have been based on either RC oscillators, relaxation oscillators or adaptively biased voltage-controlled-oscillators (VCOs) [4],[5],[6],[7]. Although RC oscillators provide good frequency stability, their phase noise performance is generally very bad [4],[5],[8]. On the other hand ring oscillators provide very good phase noise performance [8], but their inherent

property of delay variation with temperature makes their stability highly sensitive to temperature. One way to compensate for variations against supply and temperature is to adaptively bias the control voltage of a VCO shown in [7]. Unfortunately, it consumes large power of the order of mW and more importantly, its performance is not much superior to that of conventional approaches.

1.2 RC and Ring Oscillators

Much work has been done in the field of RC oscillator design, showing that they provide an excellent choice for temperature-stable frequency output [9],[10] for very low power consumption. However the phase noise performance of such oscillators is rarely reported. Also, such oscillators generally operate at a few kHz. On the other hand, ring oscillators with very good phase noise at high frequencies have been demonstrated before [11],[12], but they generally consume power in the order of few mW and their temperature stability, being very bad, is hardly ever reported.

RC oscillators possess the two important features that are necessary for a biomedical device oscillator, namely excellent frequency stability and very low power consumption. In order to use them for our purpose we need to improve their phase noise performance. However as argued in [8], for a given power consumption the fluctuation-dissipation theorem of thermodynamics dictates the lower limit for phase noise in RC oscillators. The authors of [8] define the "wastefulness factor" as the difference between minimum achievable phase noise and the actual achievable phase noise for a specific oscillator. And using this definition shows that the wastefulness factor of ring oscillators is generally much smaller than that of the other relaxation oscillators. They further deduce that since the minimum achievable phase noise of ring oscillators is only 3.7 dB higher than that of other relaxation oscillators, ring oscillators are more attractive in terms of the power versus phase-noise trade-off.

In this thesis we propose a CMOS RCR (resistor-capacitor-ring) oscillator that combines the virtues of RC oscillators, namely excellent frequency stability and low power consumption with the virtues of ring oscillators namely high frequency operation and good phase noise performance, as a perfect

solution for oscillators with sensor and biomedical applications.

1.3 Proposed RCR CMOS Oscillator

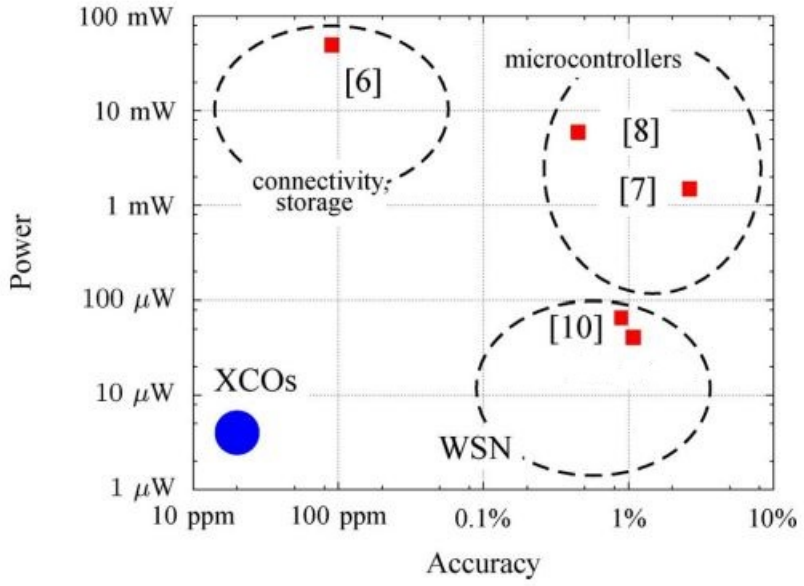


Figure 1.3: Comparison among Fully Integrated Oscillators that Can Replace XCOs in Various Applications

For designing a CMOS oscillator it is necessary to determine a target performance. The frequency stability and power required for various applications are shown in Fig. 1.3 from [13]. Connectivity and storage applications such as USB and hard devices require frequency stability of 10 to 800 ppm and power consumption of 1 to 100 mW. Micro-controllers have a limitation of frequency stability of 0.1 to 1 % and power consumption of 1 to 100 μW. RF-TCLCOs [3] can provide accuracy and phase noise performances comparable to XCOs; however, their power consumption typically exceeds 100 W due to the limited Q of integrated inductors and the possible need for high-speed frequency dividers. The accuracy of the compensated ring oscillator in [7] is high enough for biomedical applications, but its power consumption is in the mW range. Among developed CMOS clock oscillators, the performance of relaxation oscillators and trimmed RC oscillators may be most suitable

for use in biomedical applications [6]. However, the frequency stability is not enough. Therefore, none of the previous works cover all the key properties. We target the frequency stability of about $\leq 0.5\%$ for the entire temperature range of -40 °C to 125 °C, with a phase noise performance similar to that of [14]. The target frequency of oscillation is a few MHz, with power dissipation of about 100 μW for every 10 MHz of frequency.

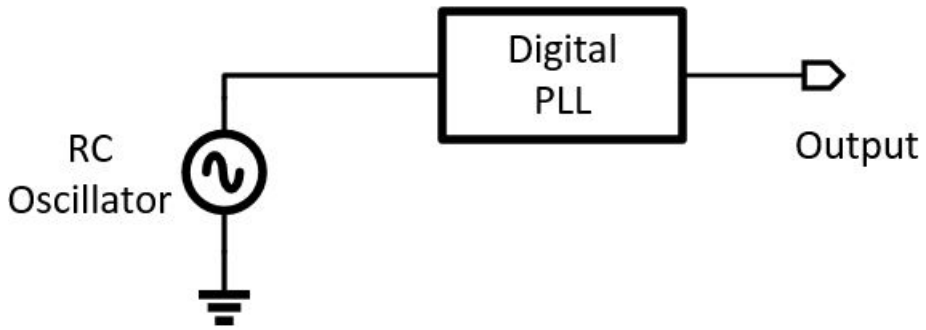


Figure 1.4: Overall System for the Proposed CMOS Oscillator

We use a primary RC oscillator as shown in Fig. 1.4 operating at 500 kHz frequency and having a temperature stability of about 45ppm/°C over the entire temperature range of -40 °C to 125 °C. The primary oscillator is then followed by a Digital PLL based clock multiplier, whose output frequency is about 50 MHz. The output oscillator of the digital PLL is a voltage controlled ring oscillator with a very good phase noise Performance. In this design since the reference oscillator has a temperature stability of around 45ppm/°C, the digital PLL based loop makes sure that the output of the loop-controlled VCO has the same temperature stability. Also by having a very low bandwidth for the loop, most of the phase noise of the RC reference oscillator is filtered, leaving only ring oscillator phase noise at the output. Thus this architecture provides us with the temperature stability of RC oscillators at high frequency, while giving an excellent phase noise performance of ring oscillators.

1.4 Outline

The thesis proposes RCR (resistor-capacitor-ring) oscillators that achieve high frequency stability against voltage and temperature variations, while providing excellent phase noise performance. Such properties are provided by the temperature insensitive RC oscillator, the temperature compensated and noise filtering feedback loop, and the supply insensitive ring oscillator.

The thesis is organized as follows.

Chapter 2 focuses on the choice and performance of the RC oscillator, which is used as a reference oscillator for the noise filtering loop of the RCR oscillator. It explains the excellent temperature stability of the oscillator.

Chapter 3 introduces the proposed ring oscillator that forms the output part of the temperature compensated feedback loop of the RCR oscillator. It shows the excellent phase noise performance of the oscillator compared to the RC oscillator in addition to its supply insensitivity.

Chapter 4 explores the viability of analog vs. digital PLL loops to couple the two oscillators mentioned in the above two chapters. It explains the choice of using all digital PLL and lists its advantages over the traditional analog PLL.

Chapter 5 provides the overall implementation and performance of the proposed RCR oscillator as a combination of the RC oscillator, ring oscillator and the feedback loop between them as discussed in the previous three chapters.

Finally, the conclusion is in Chapter 6

CHAPTER 2

RC OSCILLATOR

2.1 Architecture

The main idea of the thesis is the architectural proposal of a CMOS oscillator, hence for the primary oscillator we decided to use a slight modification of the existing RC oscillators in the literature. The oscillator design in [15] shows promising temperature stability for relatively high frequency of oscillation for an RC oscillator. However, the power consumption of the design was almost half our entire power budget. The design in [16] uses offset cancellation technique in addition to good temperature stability but also suffers from power consumption of about 25 μW. [17] demonstrates a novel idea of power averaging feedback, and also uses very small circuitry for design, but the design consumes a few μWs of power. [9] shows a low frequency RC oscillator design that consumes only 190 nW power while having excellent temperature stable frequency output. However in this design, since the output is drawn from the inverter that is been driven by a local regulated supply, the output swing is very susceptible to temperature and in fact varies a lot. Finally, the design that was chosen to implement the primary oscillator[10], had excellent temperature stability, offset cancellation and a few 100s of nWs of power consumption. The other advantage of the oscillator design was that since the output of the oscillator came from the inverter chain, the output swing could be maximized to Vdd. Also by making the inverter chain very fast, we could potentially have a differential output oscillator.

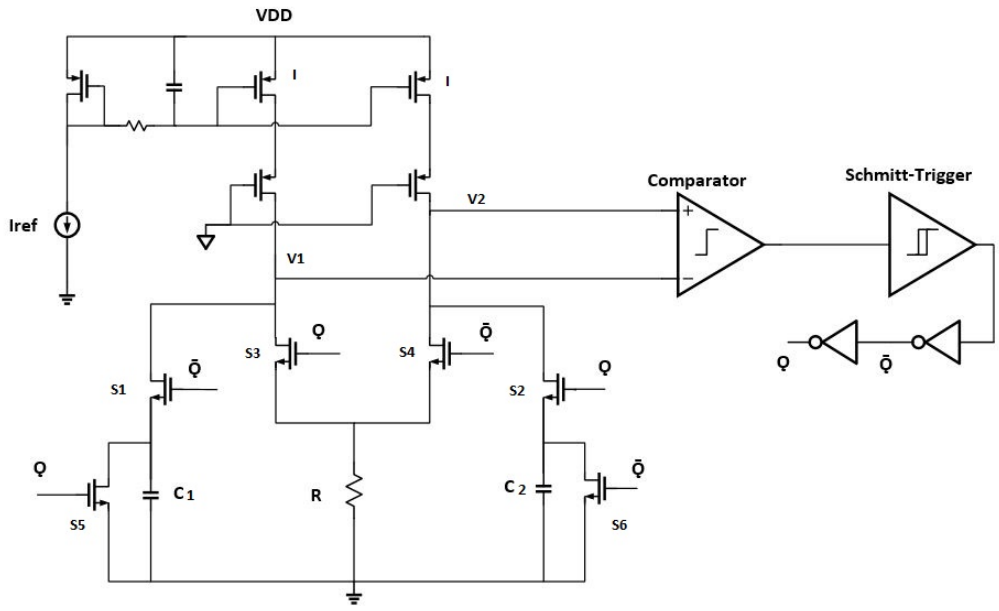


Figure 2.1: RC Oscillator Top Level Schematic

2.2 RC Design Details

Figure. 2.1 shows the design of the entire RC oscillator. When phase ϕ=0, a current I passes through resistor R to generate a voltage I∗R on node V_2. At the same time, a matched current source charges capacitor C_1, such that node V_1 crosses V_2 at time RC. After t_{delay} corresponding to the delay of the comparator and subsequent buffers, ϕ changes to 1, which then resets the capacitor voltage. In addition, the role of the two comparator inputs is reversed, with V_1 being the resistor voltage and V_2 the voltage across capacitor C_2. The period of the oscillator is thus nominally 2R∗C + t_{delay}. Two separate capacitors are used in the two phases so that the delay of capacitor discharge is not included in the period. This switching scheme also cancels comparator offset. For example, if the comparator has an offset V_{os}, as shown in Fig. 10.7.2 of [10], the duration of phase ϕ=0 increases by C∗V_{os}/I; however, the opposite phase ϕ=1 decreases by the same amount, thus the total period of oscillation is constant. This cancellation scheme allows significant power reduction in the oscillator by: (a) permitting low-swing oscillations since offset and temperature variations of the offsets do not proportionally affect frequency stability, (b) requiring only one comparator as opposed to two in traditional architectures, and (c) relaxing the specifications on the comparator offset, and allowing optimization of gain and bandwidth.

The offset cancellation also attenuates the effect of flicker noise, improving long-term stability of the oscillator.

2.2.1 Core Oscillator

In this design R is chosen to be 200 kΩ and C_1 and C_2 are 4 pF so that the comparator delay in addition to for the RC time constant is 2 μs. The charging current I is 1.6 μA on each branch, for a swing of 350 mV. Temperature stability of the oscillator is affected by the on-resistance and off-leakage of switches S_1-S_6 in addition to comparator delay variations. The switch size is optimized by considering that large devices give low on-resistance while smaller devices give lower leakage. For example, discharging switches S5, S6 are sized weak since the discharge delay does not affect frequency. The transistors used in the current mirrors supplying the charging current are thick oxide devices, with a very high V_{th} to reduce current leakage to minimum. Also the current mirrors implemented are cascode current mirrors, this was done so as to ensure constant current flow through the mirroring transistor. The cascode pair helps maintain a constant voltage across the mirroring transistors, thus keeping the constant value of current while capacitor charging. The switches S_1-S_6 were also implemented as thick oxide devices to minimize leakage through them and hence an excellent frequency stability against temperature was achieved in 65 nm TSMC technology.

2.2.2 Comparator

The comparator design is shown in Fig. 2.2. In order to handle low common-mode inputs, a PMOS-input design is used and saturation of the input pair is ensured. Transconductance efficiency (g_m/I_d) is also maximized, hence reducing power. The delay of the comparator is about 100 ns, $< 0.4\%$ of the period. In addition, to keep the period of the clock independent of temperature, a constant current reference is used, such that the delay change of the comparator cancels the increase in R with temperature. The comparator was designed such that it provided a gain of about 45 dB. The input transistors of the comparator were LVT devices, and all other transistors were used as thick oxide devices to minimize leakage in comparator. The bias current for

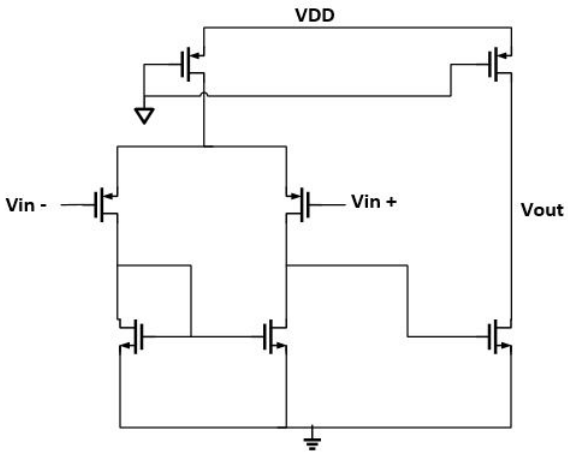


Figure 2.2: Comparator

the comparator was around 600 nA for the differential stage and 100 nA for the second (CS) stage.

2.2.3 Schmitt-Trigger and Inverter Chain

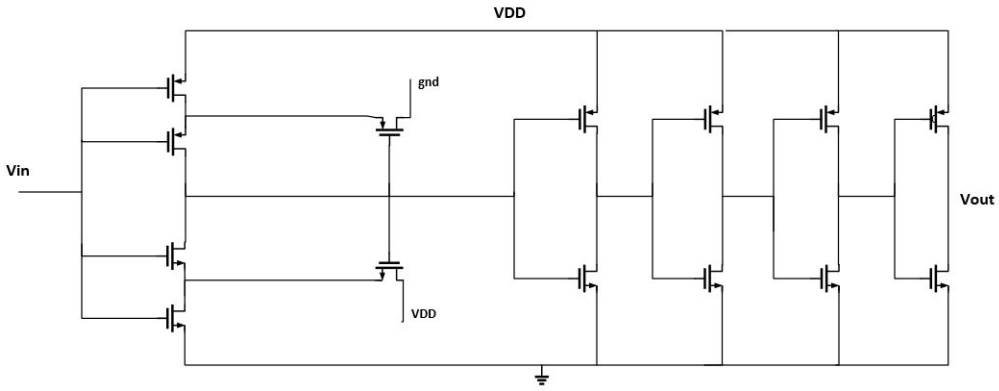


Figure 2.3: Schmitt Trigger and The Inverter Chain

During the change of phase, when nodes V_1 and V_2 switch roles, the comparator has small voltage glitches, which may result in rail-to-rail glitches at the output of the inverters. In order to prevent these glitches, and limit cycling, the first buffer stage connected to the comparator is a Schmitt trigger, implemented in a digital fashion as seen in Fig. 2.3. A small hysteresis minimizes asymmetry in the switching point of the comparator in the two phases. The Schmitt trigger and subsequent inverters add < 5 ns to the over-

all delay, and hence do not affect temperature stability of the oscillator. The inverter chain was sized to achieve optimum delay to the switches. Thick oxide devices were used for inverter transistors to get rid of short circuit power dissipation. Since the V_{th} of these devices is around 600 mV, with 1 V supply voltage PMOS switches on after NMOS is completely off which helps in getting rid of the short circuit power.

2.3 Simulation Results

The proposed RC oscillator is fabricated in a TSMC 65 nm standard CMOS process. R is implemented using a combination of p-Poly and n-Poly resistor. This was done to achieve minimum deviation of resistance with temperature as p-Poly and n-Poly have opposite temperature co-efficients. The current reference consumes 300 nA from 1 V supply. The charging currents for the capacitors are 1.6 μA each. The capacitors are implemented as mom capacitors. The total power consumption of the RC Oscillator is 5μW from 1 V supply.

To verify frequency stability to temperature, the frequency of the oscillator is plotted from -40 °C to 125 °C and shown in Fig. 2.4. It can be seen that the Frequency has a nominal value of 502 kHz at 27 °C and a temperature drift of about $\pm$1.8 kHz for the entire temperature range, i.e. a mean temperature drift of 45 ppm/°C.

The phase noise performance of the oscillator was also simulated and the results can be seen in Fig. 2.5. The figure shows that the phase noise at far-off offset frequency of 100 kHz is 97 dBc/Hz. At a close-in offset frequency of 1 kHz, phase noise is -50 dBc/Hz. The majority of the integrated noise is contributed by the current mirror charging the capacitors.

The performance of the of the oscillator is summarized in Table 2.1.

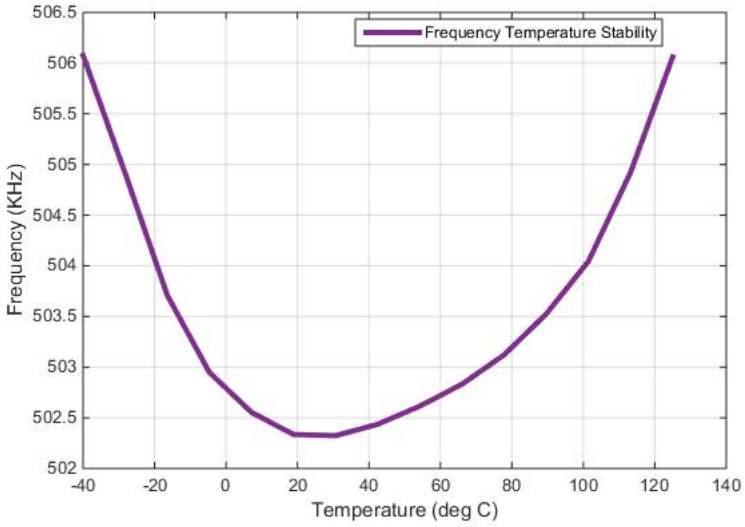


Figure 2.4: Simulated Frequency Stability of RC Oscillator against Temperature

Table 2.1: RC Oscillator Performance Matrix

Frequency	502 KHz
Power	4.98 μW
Temperature Range	-40 °C - 125 °C
Temperature Stability	45 ppm/°C ($\pm$ 0.37%)
Phase Noise @ 1 KHz	-69.9 dBc/Hz
Phase Noise @ 10 KHz	-90.6 dBc/Hz
Phase Noise @ 100 KHz	-110.6 dBc/Hz

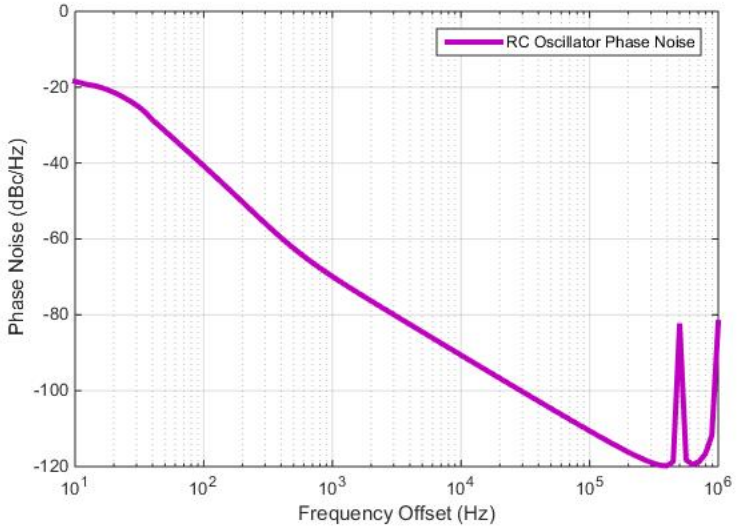


Figure 2.5: Phase Noise Performance of the RC Oscillator

CHAPTER 3

RING OSCILLATOR

3.1 Architecture

The ring oscillator used in [18] shows good supply insensitivity due to the LDO type control for frequency tuning; however, by adding an error amplifier, the flicker and thermal noise of the devices in it dominate the phase noise performance. Also the current source used at the output of the error amplifier has a large g_m amplifying the noise of the devices in the error amplifier. A capacitive tuning based ring VCO is proposed in [19]. Tuning is done by variable loading the ring oscillator with capacitors. The phase noise performance of such an oscillator is promising; however, with the inverters directly connected to VDD, the design is highly sensitive to DC supply variation. The frequency changes out of the tunability range of the oscillator even with 50 mV supply variation. Current starved ring oscillator are also a good choice for high performance VCO; however, our simulations showed that the temperature sensitivity of such oscillators is bad.

We needed a VCO which could be tuned back to its nominal operation frequency, from any temperature between -40 °C to 125 °C. Also it should be able to run at nominal frequency by changing control voltage in case of supply voltage variation of ± 100 mV. Since current starved architecture showed good DC supply rejection and phase noise performance, a slight design change was required to make them insensitive to temperature, without adding many devices and hence noise in the oscillator. Keeping in mind this performance matrix of phase noise, DC supply rejection and temperature sensitivity, the following architecture for VCO was proposed to operate at 50 MHz.

3.2 Proposed Design

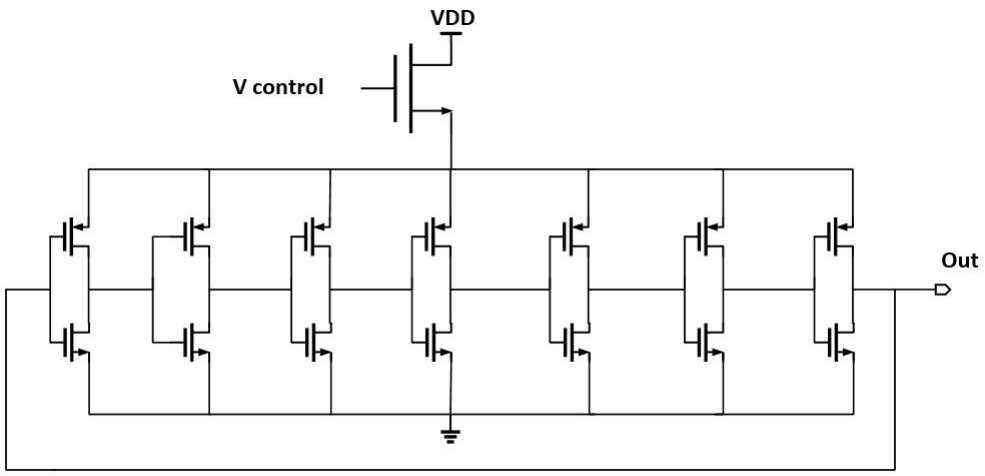


Figure 3.1: Ring Oscillator Schematic

The complete schematic of the proposed ring oscillator is shown in Fig. 3.1. The oscillator consists of a 7-stage single-ended inverter ring and the current source NMOS device at the top controlling the current through the inverters. The choice of the devices and their sizing is very important in this design. The PMOS and the NMOS devices of the inverters were used as LVTs, so as to ensure oscillation of the ring even at low control voltage of about 0.7 V (assuming the V_{gs} drop across the current source device is around 100 mV). The current source device was used as a native thick oxide device. The reason behind using it as a thick oxide device was to minimize leakage through the gate. Also since native devices have very small or almost zero threshold voltage, the V_{gs} drop across the current source device is only around 100 mV, thus ensuring high swing at the output. The device used in this design had a threshold voltage of about -15 mV, because of which we could use a NMOS device at the top of the ring oscillator. This also ensures that the impedance looking from the VDD into the oscillator is r_{ds} of the native device and hence even with $\pm$100 mV supply voltage variation the frequency of oscillation changes by a few 100s of kHz. This ensures a good DC supply rejection.

Sizing the devices was done after some initial analysis of frequency of operation, phase noise and power consumption. For any inverter the propagation delay can be approximated to $t_p = 0.69.C_L.\frac{(R_n+R_p)}{2}$, where C_L is the load

capacitance, and R_p and R_n are the average resistances of the NMOS and PMOS devices. However, for a ring oscillator the load capacitance (C_L) is the input capacitance of the next stage in addition to the output capacitance of the current stage. $C_L = C_{ox}.W.L$, where C_{ox} is the capacitance per unit area for the MOS devices of length L and width W. The average resistance of the MOS devices R_p and R_n is inversely proportional to the saturation current flowing through them and hence directly proportional to $\frac{L}{W}$. If f is the frequency of oscillation, then

$$f \propto \frac{1}{t_p} \tag{3.1}$$

$$t_p = 0.69.C_L.\frac{(R_n + R_p)}{2} \tag{3.2}$$

$$C_L \propto W.L \tag{3.3}$$

$$R_p, R_n \propto \frac{1}{Id_{sat}} \propto \frac{L}{W} \tag{3.4}$$

From equations (3.1) and (3.2), we see that

$$f \propto \frac{1}{C_L.R_{p,n}} \tag{3.5}$$

From equations (3.3), (3.4) and (3.5), we see that

$$f \propto \frac{1}{W.L.\frac{L}{W}} \tag{3.6}$$

$$Thus \quad f \propto \frac{1}{L^2} \tag{3.7}$$

Therefore, the frequency of oscillation is dependent only on the length of the CMOS devices.

Similar analysis can be done to calculate power consumption of the oscillator. Power dissipation of any digital circuit can be given by

$$P_{disp} = {V_{DD}}^2.C_L.f \tag{3.8}$$

From equations (3.3) and (3.5), we see that

$$P_{disp} \propto W.L.\frac{1}{L^2}. \tag{3.9}$$

$$Thus \quad P_{disp} \propto \frac{W}{L} \tag{3.10}$$

Therefore, power dissipation is a function of $\frac{W}{L}$ of the MOS devices. It can also safely be assumed that since the phase noise of the oscillator is dominated by flicker noise of the devices, phase noise $\propto \frac{1}{W.L}$.

The device sizes of the oscillator were picked up such that power dissipation could be minimized along with minimizing phase noise while having a frequency of oscillation close to 50 MHz. The tuning range of the oscillator was decided to be 0.7 V to 1 V. The native current source device was sized so as to provide the necessary current to the ring oscillator for oscillation at 50 MHz at a supply voltage of 1.2 V.

3.3 Simulation Results

The proposed ring oscillator is fabricated in a TSMC 65 nm standard CMOS process. Current source NMOS is implemented using native thick oxide NMOS device, whereas the inverters in the core oscillator are implemented as LVT (low voltage threshold) devices. The current source provides 150 μA from 1.2 V supply. The total power consumption of the ring oscillator is 180 μW from a 1.2 V supply.

To verify frequency sensitivity to temperature and supply voltage, the frequency of the oscillator is plotted from -40 °C to 125 °C at 3 supply voltages (1.1 V, 1.2 V and 1.3 V) and shown in Fig. 3.2. It can be seen that the nominal frequency changes by only few 100s of kHz due to supply voltage change. Also frequency changes about 10% over the entire temperature range of -40 °C to 125 °C. We can see from this figure that the worst voltage vs. temperature corners are 1.3 V and -40 °C, and 1.1 V and 125 °C. To ensure that the control voltage remains between 700 mV and 1 V for tuning the oscillator to 50 MHz between the worst corners, frequency tunability was plotted for the worst voltage/temperature corners and nominal corner and is shown in Fig. 3.3. We can see that the control voltage range to cover the maximum range of temperature and voltage variation is about 140 mV (780 mV - 920 mV).

The phase noise performance of the oscillator was also simulated and the results can be seen in Fig. 3.4. The performance shown is at a nominal

temperature and frequency of 27 °C and 50 MHz, with a control voltage of 815 mV. The figure shows that the phase noise at far-off offset frequency of 1 MHz is -124 dBc/Hz. At a close-in offset frequency of 10 kHz, phase noise is -78.4 dBc/Hz. The majority of the integrated noise is flicker noise contributed equally by all the transistors in the design.

The performance of the of the oscillator is summarized in Table 3.1.

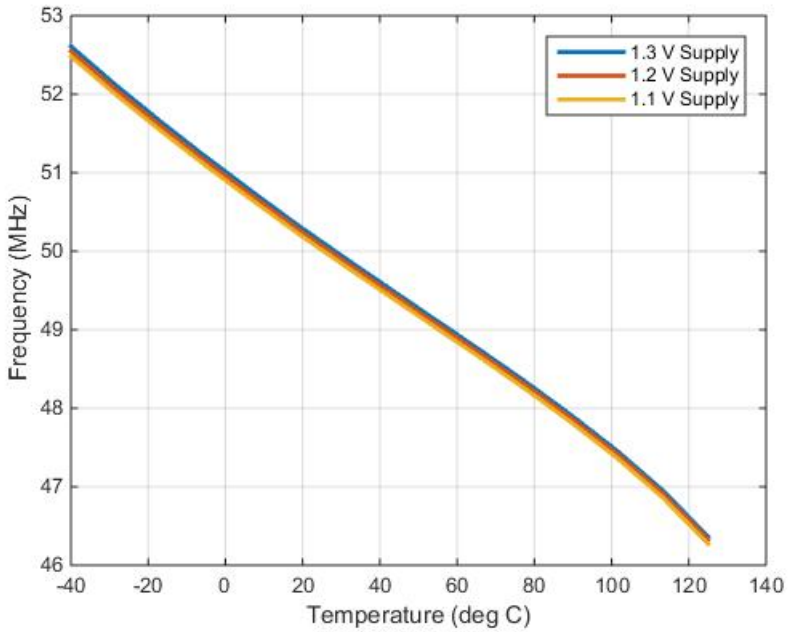


Figure 3.2: Simulated Frequency Sensitivity to Temperature and Supply Voltage

Table 3.1: Ring Oscillator Performance Matrix

Frequency	50 MHz
Power	180 μW
Phase Noise (FoM) @ 10 KHz	159.9 dB
Phase Noise (FoM) @ 100 KHz	164.7 dB
Phase Noise (FoM) @ 1 MHz	165.5 dB

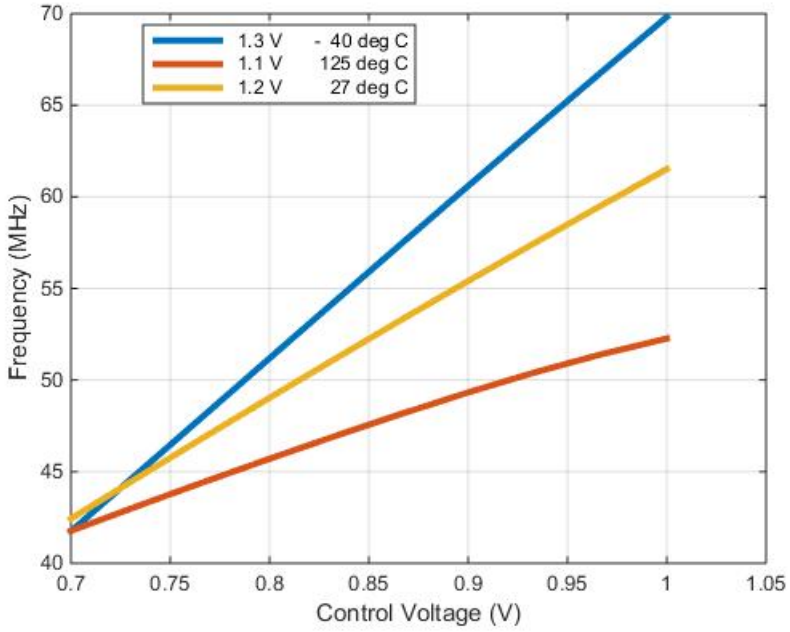


Figure 3.3: Simulated Frequency Tunability at Worst Voltage and Temperature Corners

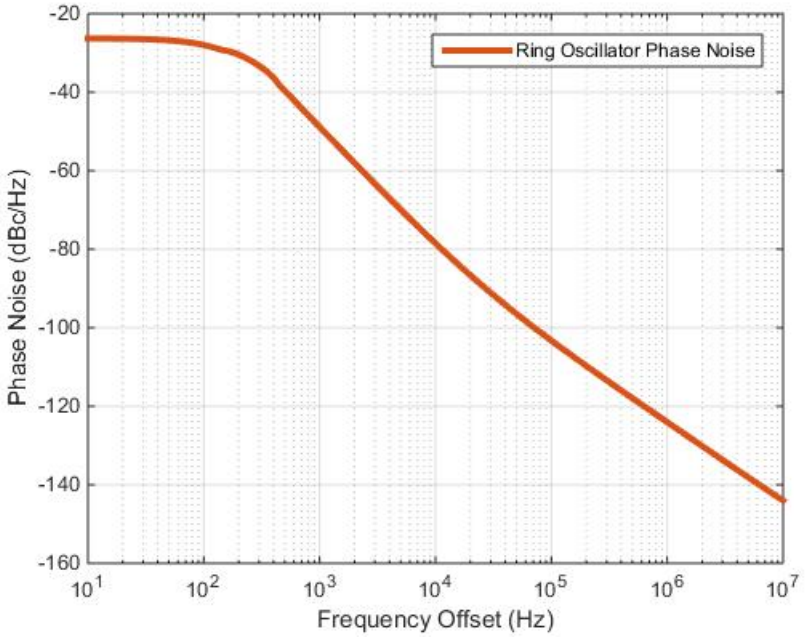


Figure 3.4: Phase Noise Performance of the Ring Oscillator

CHAPTER 4

FREQUENCY MULTIPLIER

4.1 Frequency Multiplication and Noise Filtering

The final part of the design was a frequency multiplier between the previously designed RC oscillator and ring oscillator. The reference clock to the frequency multiplier would be coming from the RC oscillator and the output clock from the ring oscillator. Also as discussed in Chapter 1, the phase noise of the RC oscillator has to be filtered in this multiplier block such that the output phase noise of the whole system is dominated by the VCO (ring) oscillator Phase Noise. Since our RC oscillator's nominal frequency of operation is 500 kHz and that of ring oscillator is 50 MHz, we would need a multiplication factor of 100 from our clock multiplier. Also, the bandwidth of the filter (in clock multiplier) should be low enough such that all the RC phase noise is filtered at the output. This gives us the basic two design specifications of our clock multiplier block. The multiplier block itself will add some noise into the whole system; for this purpose we need to select the optimum design architecture for the block.

There are broadly two ways in which we can design this block, namely by the use of PLL (phase-locked loop) and D-PLL (digital-phase-locked loop). Both of them have their merits and drawbacks. PLLs can be area intensive and add lot of phase noise through CPs (charge-pumps) and resistors in LP (loop filter), whereas D-PLLs can be done in relatively less area but introduce deterministic jitter at the output clock. Both of the above approaches are quantified for viability of area and power, in the section below, while maintaining our assumption that the noise added by the multiplier block is negligible or at least in acceptable limits at the output.

4.2 Design Analysis

4.2.1 PLL Analysis

A detailed analysis of designing an analog PLL is discussed in [20]. The paper talks about designing optimum PLL parameters given the input/output frequencies and the bandwidth. To calculate an optimum bandwidth for our design, we do parametric simulations for different values of bandwidth in MATLAB. If the bandwidth is too small, it is difficult to implement an analog PLL as the capacitor values will be too high. However if the bandwidth is too high the RC oscillator noise may not get filtered at the output. The optimum bandwidth for our design is the maximum bandwidth at which the output phase noise is dominated by ring oscillator phase noise, as this is the objective of our proposed oscillator system. The PLL is designed as type-II, order-II PLL as shown in Fig. 4.1 consisting of a three state PFD, CP, LF and a frequency divider.

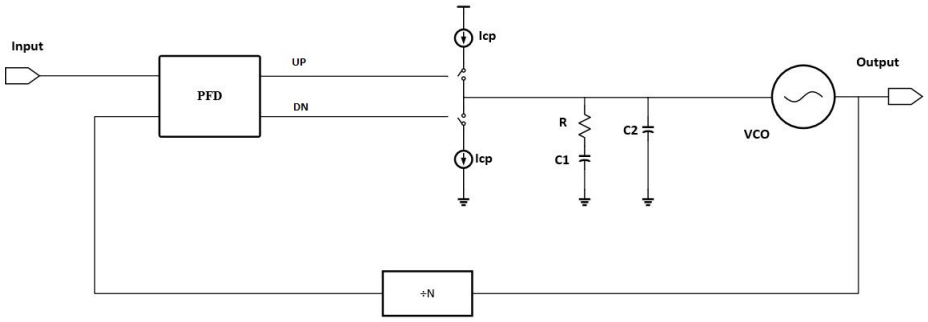


Figure 4.1: Block Diagram of an Analog PLL

The PLL would also add its noise to the output; this noise is also modelled in MATLAB. The PLL noise mainly consists of thermal noise from the CP (charge-pump) and resistor in the LF (loop filter). Thus the total output phase noise of the system is plotted in Fig. 4.2 as a sum of the reference RC oscillator noise, output VCO noise, input resistor and CP noise. The figure shows that the optimum bandwidth of the PLL for VCO noise to be dominant at the output is about 500 Hz. Following the design procedure mentioned in [20], the parameters of the PLL were calculated for optimum design. The parameters required for the above mentioned bandwidth are as follows:

- $I_{cp} = 340$ nA
- $R = 4$ kΩ
- $C_1 = 450$ nF
- $C_2 = 14.4$ nF
- $N = 100$
- $K_{vco} = 66.66$ MHz/V

With such a large value of capacitor C_1, the area required to implement the design would be tremendously high. The capacitor requirement is too high because of a low bandwidth requirement of about 500 Hz. This shows that it is not viable to implement an analog PLL as clock multiplier in light of the huge area requirement.

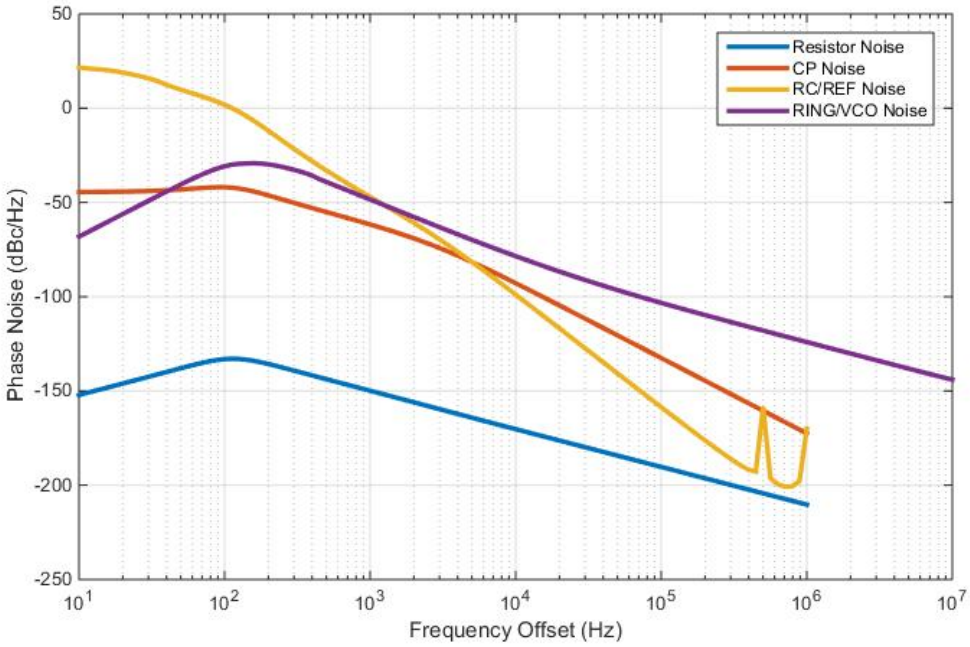


Figure 4.2: Simulated Analysis for Optimum Bandwidth of Analog PLL

4.2.2 D-PLL Analysis

Digital-PLL consists of a phase-to-digital (P2D) converter, followed by a digital filter, a digital-to-analog converter and a feedback divider. The overall

block diagram of the D-PLL can be seen in Fig. 4.3. The P2D senses the phase difference between the reference clock and the DAC-VCO divided clock, converting it into digital format. This information is filtered by the first order digital LF and is then used to control the DAC-VCO.

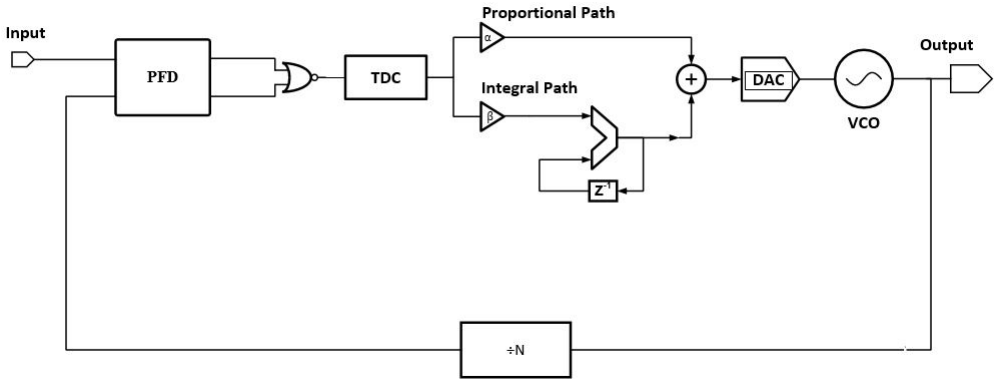


Figure 4.3: Block Diagram of a Digital PLL

In order to transform the above evaluated analysis in analog domain to digital domain, we need to evaluate the equivalent digital parameters for the D-PLL. Since the reference frequency, output frequency and bandwidth requirement remains the same, it is easy to evaluate equivalent digital parameters. The bandwidth requirement in the analog case could not be made too small because of the huge capacitor requirement; however, this requirement is not that stringent in digital domain. The transformation of parameters from analog to digital was done as discussed in [21].

Assuming the DAC to be of 12 bit, the calculations for the filter and the TDC are done. The values for the digital LF are $\alpha = 3997.77$, $\beta = 4.44$.

With the VCO sensitivity of 66.66 MHz/V and the 12 bit DAC range of 0.7 V to 1 V, the DVCO of the design is around 5 kHz/LSB. This gives us the deterministic jitter of about 3 ps accumulated for 500 KHz reference clock. This is the only issue of using a D-PLL.

4.3 Design Used

With the above detailed analysis of the clock multiplier block, it is now easy to make a decision for implementation stage of the block. Analog PLL shows promising phase noise results at the output. However, the implementation of

a capacitor of μF value is very area intensive. The capacitor density for 65 nm TSMC technology is about 2 fF/μm^2, and hence would require tremendous area to implement. There is an alternative of using an off-chip capacitor for the design; however, we wanted to build a full on-chip CMOS oscillator. In recent years, there has been a practice of using on-chip capacitor multipliers as discussed in [22] and [23]. [22] uses a CMOS circuit to suitably magnify the value of a grounded unit capacitance. The multiplication factor is achieved through the gain of current mirrors and its maximum value is solely limited by power consumption constraints. Using such a technique would only add some noise coming from the capacitor multiplier circuit.

However, using an all digital-PLL provides a much simpler alternative of implementation with the only disadvantage being deterministic jitter at the output. The DAC at the input of the VCO can be implemented as a current steering DAC followed by a resistor. The P2D, digital LF and the feedback divider can be directly synthesized from the 65 nm TSMC standard cell library. Also since the frequency of operation is only 500 kHz, the power consumption of the D-PLL is very small compared to that of the Ring VCO. This helps the figure-of-merit numbers for our oscillator. The complete oscillator is described in the next chapter.

CHAPTER 5

PROPOSED SYSTEM OVERVIEW

5.1 Top Level Design

The top level diagram of the proposed CMOS oscillator is shown in Fig. 5.1. The digital PLL as discussed in the previous section was implemented in a non-conventional way. Instead of a TDC based design, a (BBPD) bang-bang phase detector with a very high gain was used which was followed by a one bit accumulator with a proportional path added on to it. This overall system was clocked at 500 kHz frequency or the update rate of the reference RC frequency. This part of the design was implemented to achieve a very low bandwidth of 500 Hz required for our clock multiplier loop. The accumulator had a bit width of 15 bits but only 12 bits were used at the output (3 LSBs were dropped). The output of the accumulator block was then up-sampled by 5 MHz clock, that came from the output of the first frequency divider. The data encoded in these 12 bits is the control voltage value and hence is a DC value. This data can be easily converted with the help of DACs to the required $V_{control}$ value. The width of the data encoding the information was chosen to be 12 bit so that the jitter resulting from its quantization noise was 1 order less than the jitter of the free-running VCO. The free-running VCO gave a peak-to-peak jitter performance of about 10 ps. Hence the DAC width of 12 bit was used so that the deterministic jitter due to quantization was close to 3 ps, making a very small impact on the overall performance of the oscillator. However, constructing a 12 bit DAC is a challenging task, as it might add considerable noise at the control of the VCO. This problem was solved by implementing the 12 bit DAC, as a combination of a second order digital 12-bit to 1-bit delta-sigma modulator followed by a one bit DAC, as discussed in [24]. As the information encoded by the accumulator was low frequency information, use of noise-shaping second order delta-sigma

modulator, as shown in Fig. 5.2, made perfect sense. The one bit output of the delta-sigma modulator was then passed by an inverter and then a low pass filter. As the information encoded has the DC control voltage value, a low pass filter with a very sharp and low cut-off frequency was used to get rid of almost all the quantization noise at the output. The low pass filter used was a simple two stage RC filter as shown in Fig. 5.3. The cut-off frequency was chosen to be around 2 kHz, so that it is higher than the loop bandwidth of 500 Hz and still low enough to get rid of the quantization noise. In order to reduce area, capacitor values were chosen as C_1= 10 pF and C_2= 30 pF. This made the values of resistors to be about 2-3 MΩs. Such big resistors would require very big area, hence the technique of using a switched resistor was used as described in [25]. The resistor values in the final design used were $R_1 = 3$ kΩ and $R_2 = 1$ kΩ. The resistors were switched by a 5 MHz clock from the first divider with a duty cycle of $\frac{1}{400}$. This small duty cycle clock was implemented by a delay block having a delay of 0.5 ns and then passing the original clock along with the inverted and delayed clock through an AND gate. This design made the effective resistances 400 times larger than their original value, while saving huge area and achieving a cut-off frequency of about 2 kHz both at the same time. The output of the low pass filter was then used to control the frequency of oscillation of the VCO.

5.2 Performance

Individually the RC or the ring oscillator cannot fulfill the performance matrix required for the application of biomedical devices or wireless sensor networks application. However with our proposed structure, all the performance matrices as shown in Table 5.1, fulfill the required standards. The RC oscillator has an open loop temperature sensitivity of 45 ppm/°C over the temperature range of -40 °C $\sim$ 125 °C. The clock multiplier loop makes sure that the output clock from the ring oscillator also oscillates at the same sensitivity to temperature at 50 MHz, thus achieving 45ppm/°C stability at 50 MHz frequency. As the temperature variations happen at a slow speed, the feedback loop adjusts the control voltage of the ring VCO to ensure high stability oscillation at the output. As we have seen in chapter 3 that supply regulation of the ring oscillator is very good, and variation is only few 100s of

kHz which is taken care of by the clock multiplier loop, adjusting the control voltage such that the frequency change at the output due to supply regulation is negligible. And finally the phase noise performance is also shown in the performance matrix; as expected, the system phase noise is dominated by the ring VCO and the FoM figures of around 163 dB are achieved at an offset frequency of 1 MHz.

Table 5.1: Proposed RCR Oscillator Performance Matrix

Technology	TSMC 65 nm
Temperature Range	-40°C - 125°C
VDD	1.2 V
Power	220 μW
Frequency	50 MHz
Temperature Stability	45ppm/°C
Phase Noise (FoM) @ 100 KHz	162.5 dB
Phase Noise (FoM) @ 1 MHz	163 dB

$$FoM = |\, L(\Delta f) + 20\, log\,(\frac{\Delta f}{f_0}) + 10\, log\,(\frac{P_{disp}}{1mW})| \tag{5.1}$$

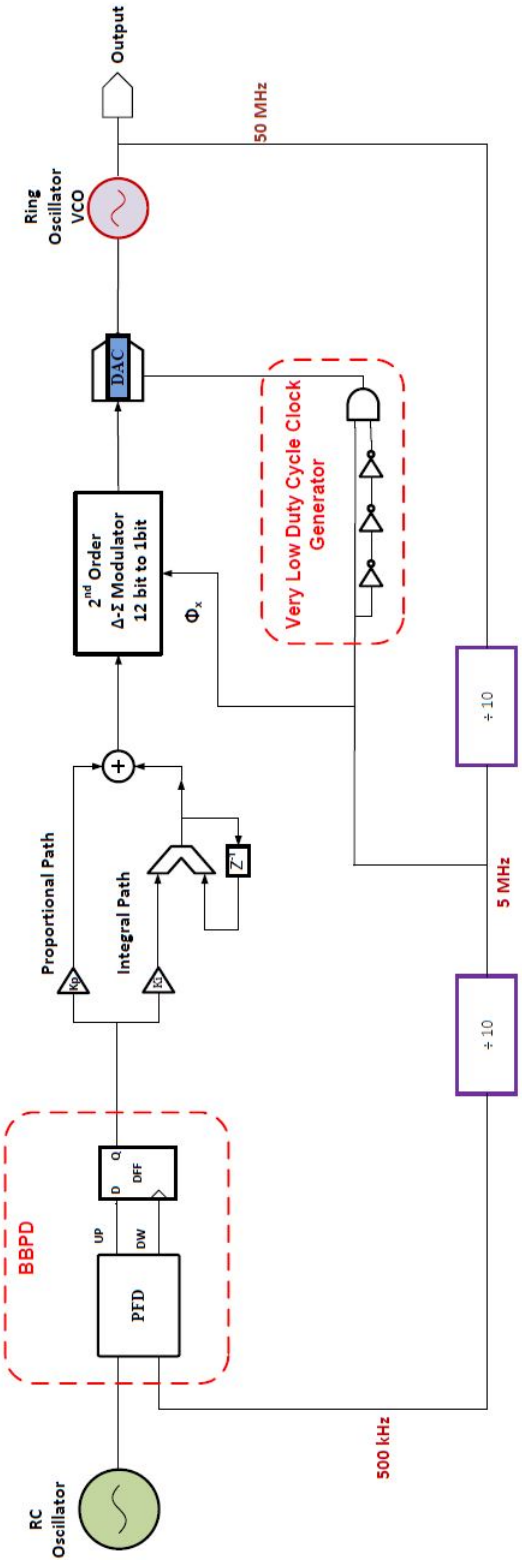


Figure 5.1: Proposed Oscillator Block Diagram

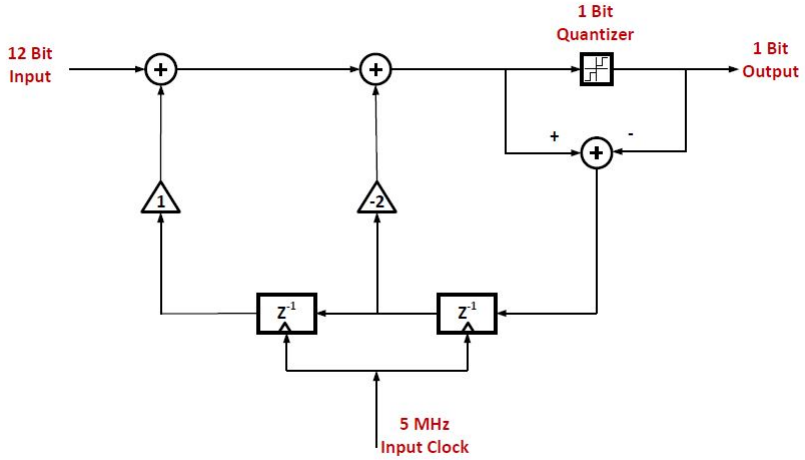


Figure 5.2: Second Order Digital Δ-Σ Modulator

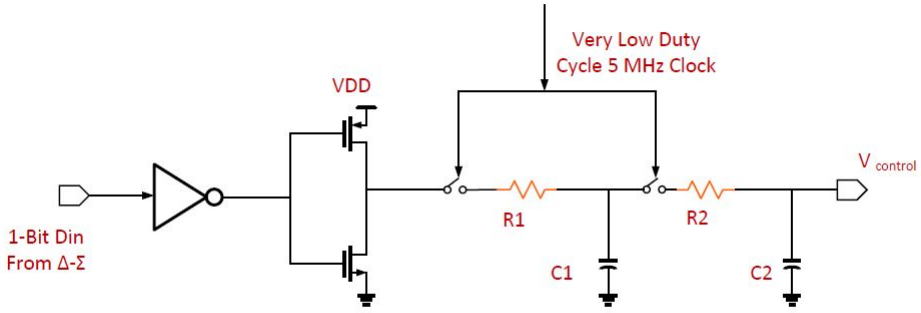


Figure 5.3: 1-Bit DAC Implementation

CHAPTER 6

CONCLUSION

A reference clock generator is one of the most important components in many electronic devices. Common clock references are based on quartz crystals which offer high quality factor, good phase noise performance and excellent stability against temperature, voltage and process variation. However, due to incompatibility with silicon integration and high power consumption, they are not suitable for biomedical devices which require long battery lifetime, low cost and especially small size but do not require near-crystal accuracy. This thesis focuses on eliminating the quartz crystals and generating the reference clock on a silicon chip. Moreover, this thesis proposes a way of combining two major oscillator types available in CMOS (RC and Ring) technology, while preserving the unique qualities of both of them and coming up with the proposed RCR (resistor-capacitor-ring) oscillator, which offers an excellent alternative for biomedical devices and wireless sensor networks.

In order to generate stable clock frequency against temperature and supply variations a novel CMOS reference clock oscillator is proposed which exploits the RC and ring oscillator performances, providing the best of both worlds in performance. The proposed oscillator employs a supply-regulated ring oscillator in a feedback loop that follows a frequency-insensitive RC oscillator, which minimizes the frequency sensitivity to supply and temperature variations. The clock oscillator achieves negligible frequency variation against supply variation of 1.1 V to 1.3 V and $\pm 0.37\%$ against temperature variation of -40 °C $\sim$ 125 °C. In addition, low power consumption is achieved by using mostly digital circuitry operating at very low frequencies. Even the phase noise performance of the proposed oscillator shows a very high FoM of about 160 dB at the offset frequencies of 100 kHz and 1 MHz. This stability to temperature and supply along with excellent noise performance is the unique cornerstone of RCR oscillators proposed in this thesis, which cannot be seen in any full-CMOS oscillators. When the performance of the clock

oscillator is compared to that of the recently reported low power CMOS reference clock oscillators, the frequency variation to supply variation is reduced to zero, temperature sensitivity is also improved by approximately a factor of 3 and normalized power consumption to frequency output is reduced by a factor of 5. The proposed CMOS clock oscillator is implemented in 65 nm TSMC CMOS technology and consumes just 220 μW from 1.2 V supply at an output frequency of 50 MHz.

Table 6.1 provides a comparative performance analysis of RC, ring and the proposed RCR oscillator. We compare the oscillators for phase noise performance, supply regulation and temperature stability. Phase noise performance of the RC is relatively bad compared to the ring and RCR oscillators, whereas temperature sensitivity of ring is very bad compared to the RC and RCR oscillator. And lastly, ring and RCR oscillators are more immune to supply variation than the RC oscillator, thus showing that the proposed RCR oscillator's performance matrix matches those of RC and ring oscillators while leaving behind their individual short comings.

Table 6.1: Proposed RCR Oscillator Performance Matrix Compared to RC and Ring Oscillator

	RC Oscillator	Ring Oscillator	Proposed RCR Oscillator
Power	5 μW	180 μW	220 μW
Frequency	502 kHz	50 MHz	50 MHz
Temperature Stability (-40 °C $\sim$ 125 °C)	$\pm$0.37% (45 ppm/°C)	$\pm$5%	$\pm$0.37% (45 ppm/°C)
Phase Noise (FoM @ 100 KHz)	147.5 dB	164.7 dB	162.5 dB
Phase Noise (FoM @ 1 MHz)	-	165.5 dB	163 dB

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