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A Study on Effects of Copper Wrap Specifications on Printed Circuit Board Reliability

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Abstract

During the manufacturing of Printed Circuit Boards for a Flight Project it was found that a European manufacturer was building its boards to a European standard that had no requirement for copper wrap on the vias. The amount of copper wrap that was measured on coupons from the panel containing the boards of interest was less than the amount specified in IPC-6012 Rev B, Class 3. To help determine the reliability and usability of the boards, three sets of tests and a simulation were run. The test results, along with results of simulation and destructive physical analysis are presented in this report. The first experiment involved subjecting coupons from the panels supplied by the European manufacturer to thermal cycling. After 17000 cycles the test was stopped with no failures. A second set of accelerated tests involved comparing the thermal fatigue life of test samples made from FR4 and polyimide with varying amounts of copper wrap. Again, the testing did not reveal any failures. The third test involved using interconnect stress tests coupons with through hole vias, and blind vias that were subjected to elevated temperatures to accelerate fatigue failures. While there were failures as expected, the failures were barrel cracks, not in the wrap location. In addition to the experiments, this report also discusses the results of finite element analysis using simulation software that was used to model plated through-holes under thermal stress using a steady state analysis, also showing the main failure mode was barrel cracking.

The tests show that although copper wrap was sought as a better alternative to butt joints between barrel plating and copper foil layers, manufacturability remains challenging and attempts to meet the requirements often result in features that reduce the reliability of the boards. Experimental and simulation work discussed in this study indicate that the standard requirements for copper wrap are not contributing to overall board reliability, although it should be added that a design with a butt joint is going to be a higher risk than a reduced copper wrap design. The study further shows that procurement requirements for wrap plating thickness from Class 3 to Class 2 would pose little risk to reliability (minimum 5 µm/0.197 mil for all via types). Experimental results corroborated by modeling indicate that the stress maxima are internal to the barrels rather than at the wrap location. In fact, the existence of Cu wrap was determined to have no appreciable effect on reliability.

Keywords*: Copper wrap, plated through hole, printed circuit board, interconnect stress testing, failure analysis*

Background

Printed circuit boards (PCBs) are the platform for electronic packaging upon which electronic components are formed into electronic systems. PCBs are used in a variety of electronic circuits from simple one-transistor amplifiers to large super computers. A PCB serves three main functions: 1) it provides the necessary mechanical support for the components in the circuit 2) it provides the necessary electrical interconnections, and 3) it bears some form of legend that identifies the components it carries [1].

Printed circuit boards can be classified into three categories based on their construction and physical characteristics, namely rigid, flexible and rigid-flex boards. Rigid circuit boards are

composed of a composite layered structure in which solid copper sheets are laid down and separated with a dielectric material, which is commonly an epoxy resin system. Rigid boards represent the most widely used category and they can be built from different materials systems. Flexible printed circuits consist of thin copper foil bonded to a thin plastic base. The third category is the rigid-flexible boards, which is a combination of rigid and flexible boards bonded together. Multilayer boards are made by a combination of the processes used for single sided boards and double-sided boards with plated through-holes (PTH). The individual internal layers, which may be single or double sided, are first etched in the same manner as single boards (after being punched and drilled for locating dowels), and then the layers are bonded together. The layers are laid up with prepregs between the etched layers on the alignment dowels and the assembly is placed in a powerful press to obtain a blank.

Initially a light pressure is applied to close the layers together, and then the system is heated up. The full bonding pressure is applied and the resin is cured at elevated temperature. Once this stage is complete, the blank is ready for the outer layer processes. Early circuit boards contained one layer of copper foil adhered on to a phenolic backing [2]. The electronic parts, usually axially-leaded parts, were mounted with screws. Since these were single layer boards, there was little opportunity for traces to cross one another. The first big development was to go from a one-sided board to a two-sided board. The leads of the parts were used to connect one side of the board to the other. Where a trace had to go from one side to the other without the use of a part lead, a short wire known as a Z-wire was used. With either the part lead or the Z-wire the standard required the wire to be bent over and touching the trace as it left the solder pad area. During this time, it was learned how to get copper into the holes to help conduct the current along with the leaded part lead, or Z-Wire. The PTH is referred to as a via. The vias were not trusted to carry current without the addition of some form of wire being added. As vias matured, the number of layers to a PCB began to grow. In a 4-layer configuration, power started to be carried solely by the vias between the board layers.

With advent of computer-aided design (CAD), designers and fabricators were able to bridge the gap from the electrical schematics to the controls involved in building the boards. With the use of CAD, higher layer count boards could be fabricated, and as the boards could handle more layers, the electronics going on the boards could be smaller, which in turn placed additional demands on the PCB. One of the newer tricks to make a board higher in signal density has been to make vias that no longer go through the entire board. Holes now may start on the outside of the PWB but stop somewhere inside of the board; these are known as blind vias. There are other places where a via can go between layers, but never surface and these are called buried vias. In both the cases of a blind via and a buried via it becomes impossible to use the old technique of using a Z-wire to assure a signal is able to go from one layer to another.

One problem that has followed printed circuit boards is thermal expansion. The typical root cause of filled plated through hole failures under thermal cycling is the difference in Z-axis coefficient of thermal expansion (CTE) between the PCB material (a polymer), the material that fills the PTH, and surrounding copper. The Z-axis of PCBs is conventionally defined as the axis parallel to the PTHs. When materials are heated, they physically expand, and when cooled, contract. The X- and Y-axis CTEs of a PCB are constrained by the glass fiber weave and are not typically involved in PTH failures under thermal cycling. This constraint forces any expansion in the Z-axis. Z-axis CTE values for typical PCBs are about 30 ppm per degree Celsius when below the glass transition temperature (Tg). However, this CTE value will vary based on multiple factors including the polymer type, epoxy, and polyimide, which have significantly different Tg values, whereas the CTE value for copper is about 18 ppm/°C.

The physical expansion and contraction of the materials at different rates generates stress. The stress may be relieved by forming cracks in the copper, which may lead to an electrical intermittent or open circuit. Unfilled PTH cracks induced by thermal cycling typically occur near the middle of the PTH barrel, where the stress is highest [3][4][5][6]. When the PTHs are filled with polymer material, stress is also applied at the edges of the polymer fill between the copper wrap and copper cap plating layers [4][5]. This crack initiates at this intersection and propagates horizontally away. Electrical intermittent opens or full opens are observed when the crack angles

toward the board and propagates through the copper wrap and copper foil layers.

In the past, one of the accepted practices was to form a crook in the lead to allow for thermal expansion. Now without leads other solutions are needed to overcome the thermal expansion problem. Smaller parts have helped, but in space applications the material in the boards themselves has changed. The choice in the past was FR4, which has a higher coefficient of expansion than the parts, so there is a mismatch; it also has a low glass transition temperature, causing even more expansion issues as well as delamination problems. For PCBs that have to survive high temperatures the material of choice is polyimide. FR4 however is still a common material that is used widely in the commercial world.

One of the areas that has been placed into focus in recent times has been the amount of copper that comes over the edge of a via hole and onto the layer plane. This could be on the surface layers in the case of a through hole, or it could be at the end of a buried via. Copper wrap is defined as the electrolytic hole plating, extending onto the surface from a plated via structure. In certain PCB fabrication processes a planarization process reduces the wrap thickness. The question has become how much copper wrap is needed to form a reliable via? A schematic illustration of copper wrap and a corresponding butt joint is shown in Figure 1 and Figure 2.

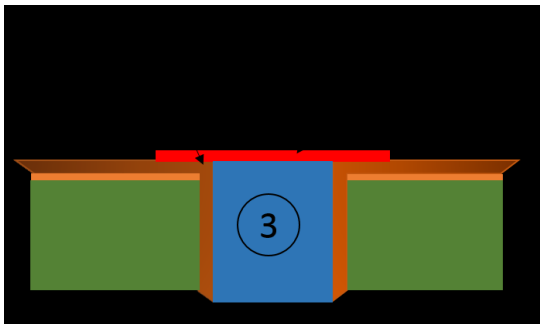


Figure 1 Copper wrap is the electrolytic hole plating deposition continuously extending onto the surface from a plated via structure. Schematic illustration of a wrap plating, 1 - cap plating, 2- wrap plating and, 3 - via fill.

Copper is added in multiple steps to a single PCB copper layer. The first is copper foil that makes up the base copper of each copper layer in a PCB. This foil is etched to form the pattern of pads for components and the traces to connect them. After lamination, which joins all of the individual layers, the PTHs are drilled. The copper wrap plating includes the plating that covers the inside of PTHs. It covers the copper foil annular ring on the top and bottom PCB surfaces. The plating is continuous, thus wrapping around the PTH shoulders and electrically connecting the top and bottom layers.

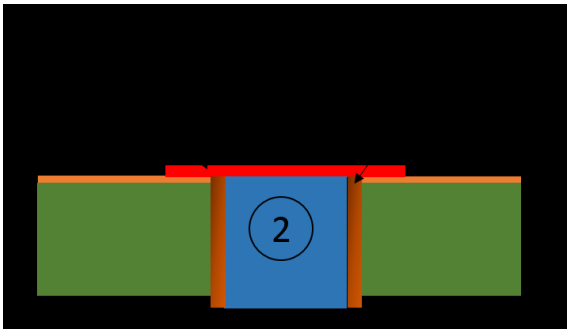


Figure 2 Butt plating joint is a via structure of a surface interconnect termination with absence of copper wrap plating. In the schematic illustration, 1 - butt joint plating, 2 - via fill and, 3 - cap plating.

The fabrication steps relevant to the final wrap plating thickness begin with the copper wrap plating step. Current technology is more than sufficient to plate the minimum copper wrap and wrap plating thickness specified for Class 3 in IPC-6012 Rev B. After the copper is plated to a sufficient thickness, the PTHs are filled with a polymer. All polymer fill processes leave some cured polymer above the surfaces of the PCB.

A planarization step follows PTH fill and polymer cure because the PCBs must be flat for later fabrication steps. This planarization step removes excess polymer but also removes some copper wrap, reducing the wrap plating thickness. The amount of copper wrap removed during planarization is difficult to control.

Industry Specifications

Copper wrap plating and wrap plating thickness are dimensions specified for all filled PTHs in the IPC-6012 standard published by IPC. These dimensions are measured by preparing a cross-section like the ones shown in Figure 3. The micro-sections are etched to reveal the different copper layers prior to performing the wrap thickness measurements.

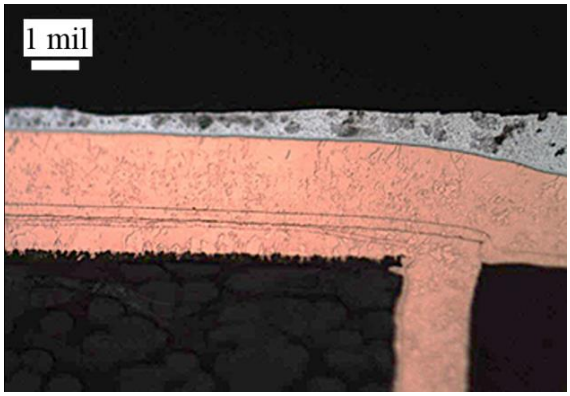


Figure 3 Copper wrap dimensions are measured after preparing micro-sections.

The wrap plating and thickness are defined in a graphic similar to Figure 4. The cap plating is not considered in the wrap plating thickness measurement.
In many IPC standards including IPC-6012 Rev B, three values for a specified dimension are provided, categorized by performance classes. Classes 1, 2, and 3 represent different groups of electronics and are described in IPC-6011 Rev L, paragraph 1.2.

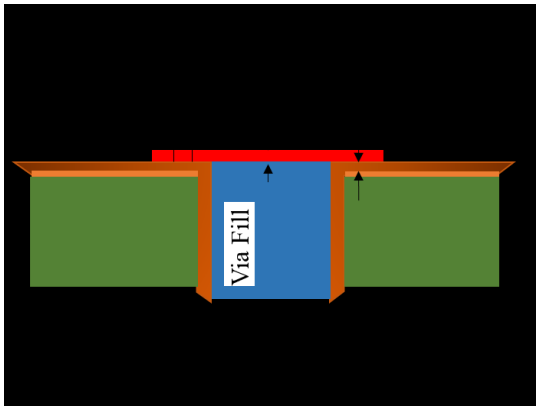


Figure 4 Copper wrap measurement, as shown in IPC-6012C.

By definition, Class 1 represents general electronic products, which includes products suitable for applications where the major requirement is function of the completed assembly, Class 2 is dedicated service electronic products, which includes products where continued performance and extended life are required, and for which uninterrupted service is desired, but not critical. Typically, the end-use environment would not cause failures, and Class 3 represents high-reliability electronic products. Class 3, or high reliability electronic products, include products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems. IPC-6012 Rev B paragraph 3.6.2.11.1, Figure 3-13, and Table 3.2 together call out minimum wrap plating for PTHs and a minimum thickness for each Class. These requirements are captured in Table 1.

Table 1 IPC-6012 Rev. B Minimum Wrap Plating Thickness

	Class 1	Class 2	Class 3
Minimum Wrap Plating Thickness	As Agreed Between User and Supplier	5 ε m [1 9 7 ε or 0.2 mil]	1 2 ε m [4 7 2 ε or 0.5 mil]

The basis for the copper wrap requirement described in Table 1 is unclear, however it appears that in some comparative experiments reported in the open literature, a higher reliability was reported with copper wrap as compared to plated through holes that are fabricated with a butt joint. The scenarios are illustrated in Figure 2.

One premise for the copper wrap requirement is perhaps the perception that thicker copper requirements resulting in the wrap can be used as a safety margin against manufacturing variations that are introduced during the planarization process. Note that this planarization process is used in the wrap fabrication. Since wrap planarization can cause 0.3 mil or higher variations across a typical panel; printed circuit board fabricators must target a higher value for the copper wrap [3]. It was further stated in literature that sufficient wrap cannot be achieved at required thickness for designs with tight line-width spacing and/or with multiple lamination/plating steps [8][9][10][37]. However, a review of section 6 and other sections of the ECSS-Q-ST-70-11C: Space Product Assurance - Procurement of Printed Circuit Boards shows that there is no existing requirement for a minimum copper wrap thickness [11]. There are instances in literature that state a wrap that is 5.0 Õm robust, whereas a wrap of less than 5.0 µm is prone to early failure, although this study [12] does not provide specifics of board material,

thermal cycling regime, or any other relevant information about context.

The requirements placed in the IPC specifications can not only contribute to a project ô s i n a b i l i t y t o s t a y w i t h i n b u d g e t a n d scheduled timelines, but also its ability to deliver the printed circuit board hardware with high quality. The delays or lost build schedules are expensive, but failures are even more expensive. However, test sample non-conformances to a Standard do not, in general, equate to printed circuit board failures. In light of the lack of supporting reliability data and the requirements imposed in the IPC specifications, a process was implemented to utilize a risk-based decision to determine acceptability of non-conformances stemming from the printed circuit board copper wrap requirements [38]. The impact of the non-conformance to Standards and the resulting defects was explored and the merits of requirements were established using a series of experimental and modeling efforts that are described in the following sections.

Experiments

Three experiments and one computer modeling effort are described in the following section. The tests were undertaken in order to understand the effects of copper wrap thickness that did not meet the specifications. Accelerated tests on printed circuit boards used in the Flight Project that were exhibiting copper wrap violation during structural integrity testing were the starting point. These constituted the first of the three tests that were conducted in order to understand the implication of violation in copper wrap thickness.

Experiment 1 Testing Flight Coupons

The structural integrity coupon evaluations determined that the boards represented by the coupons did not meet the IPC-6012B Class 3/A wrap copper requirement (minimum of 0.47 mils). The printed circuit boards were supplied by a European manufacturer, and met the European standards ECSS-Q-ST-70-11C [11] to which the boards were manufactured. When the coupons for the boards were reviewed at GSFC it was found that the copper wrap was insufficient to meet the 6012B 3/A standard that was imposed on the project at the time. A detailed examination of the original micro-sections as well as spare coupons that were submitted for each board/panel indicated that the wrap copper varied for top vias from 0.00 mil to 0.17 mils, bottom vias 0.00 mils to 0.29±0.16 mils. A total of sixteen top vias and 16 bottom vias were examined for each board/panel. Examples of the findings, showing a copper wrap of 0.16 mil, and another example with no copper wrap, are shown in Figure 5.

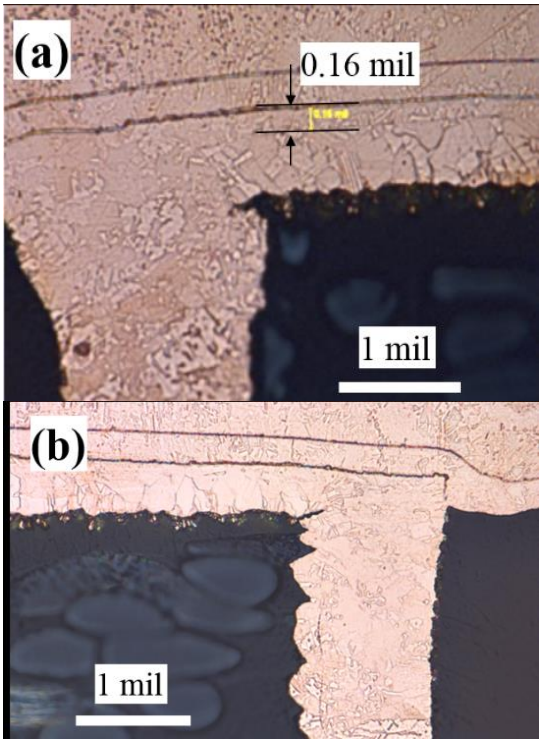


Figure 5 Examples of wrap copper findings (a) wrap copper of 0.16 mils from a micro-section and (b) no wrap copper from a micro-section.

The detailed examination found no evidence of poor bonding between the copper foil and plating; these boards were built to ECSS-Q-ST-70-11C, which does not address wrap copper. For the purpose of this test, the coupons that are provided at the periphery of the panel were used. An image of the test coupons is shown in Figure 6.

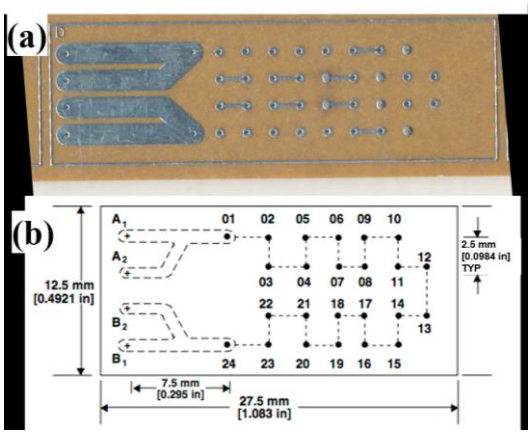


Figure 6 (a) an image of the "D" coupon used for thermal cycling and (b), the hole pattern in the "D" coupon. There are 28 holes in total, out of which 24 are in the daisy chain and 4 at locations A_1 A_2 B_1 B_2.

The boards consisted of ten layers, which included a mix of buried vias, internal conductors and plated through hole features. A schematic cross-section of the ten-layer stack is shown in Figure 7.

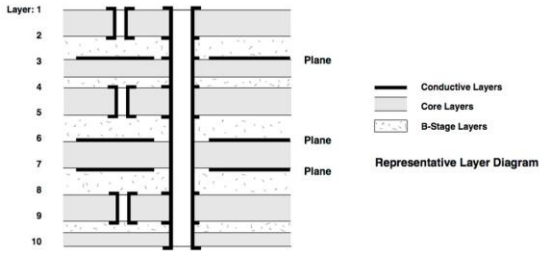
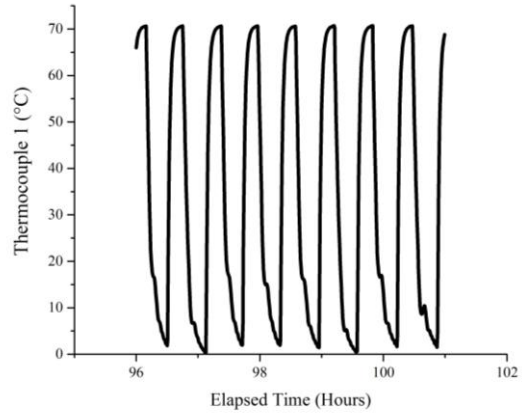


Figure 7 Schematic showing the stackup of the ten-layer board received from the European manufacturer.

Prior to accelerated temperature cycling, the test coupons were subjected to assembly process simulation where the coupons were thermally stressed using IPC TM-650 2.6.8 Test Condition C (to simulate the vapor phase soldering at +230 °C), followed by test condition A (to simulate hand soldering at +288 °C) with cooling in between. There was no rework on the flight boards, so rework was not simulated. In order to perform the ground testing and flight simulation, coupons were thermally shocked (and cycled) using IPC TM-650 2.6.7.2 Test Condition A (0 to +70 °C). This test condition was selected because it is closest to the expected ground testing and flight temperature range. The assembly simulations completed 17765 cycles between 0 and +70 °C. Out of these, the first 1078 cycles were performed in a thermal shock chamber and the remaining cycles were performed in a conventional thermal cycling chamber. The resistances of six nets were monitored using a data-logger, with source current of 1 mA for the resistance measurements. The resistance monitoring interval was thirty seconds. A plot of the net resistance in ohms as a function of the time and cycle number is shown in Figure 8 and Figure 9. The colors in Figures 8 and 9 refer to the resistance measurements taken on individual samples. In total, six D coupons were tested, with each coupon containing one net: two D coupons representing a single board/panel and four additional D coupons representing two additional boards/panels (2 from each board/panel). These details have been added to the manuscript. It can be seen in the plots of resistance that the six monitored nets continued to exhibit the levels that were observed at the beginning of the temperature cycling tests.



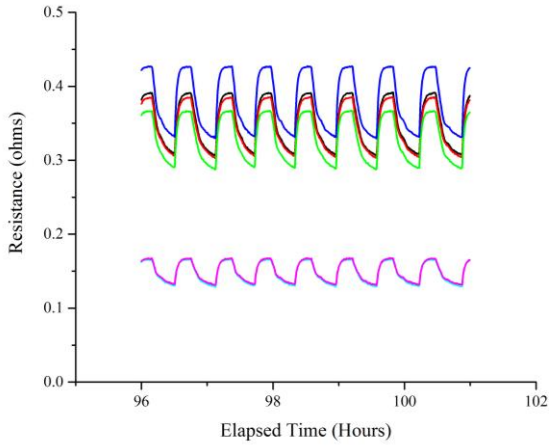


Figure 8 Plot showing a snapshot of the thermal shock profile (top) and the corresponding change in resistance (bottom).

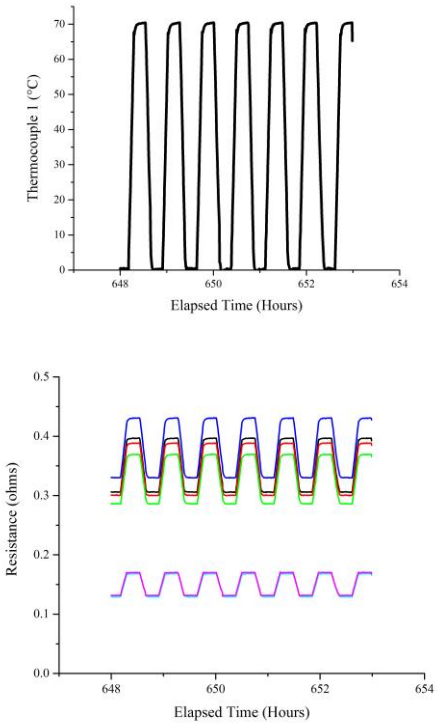


Figure 9 Plot showing a snapshot of the temperature cycling profile (top) and the corresponding changes in resistance (bottom).

During the temperature cycling and the thermal shock tests, intermittent changes in the resistance were observed on three of the six coupons. One of the D coupons developed spikes at cycle 386, which continued until the test setup was rewired into a thermal cycling chamber at cycle 1078 cycles. No spikes were observed since the setup was rewired. An additional D coupon exhibited the resistance spikes at cycle 517, 518 and 520, however no other spikes have been observed. An additional D coupon developed resistance spikes at cycle 285. These spikes stopped after the test was stopped and the coupon probed to determine the cause of the spikes. There have been no observed trends in the absolute value of the resistance of the coupons during any of the cycling. Even though earlier probing of the test setup or the coupons could not get the spikes to occur, it appears that rewiring the test setup eliminated the intermittent resistance spikes.

Experiment 2 Thermal Cycling of Test Boards

While the boards in experiment 1 provide a very specific test sample, coupon and material set with specific test results, simultaneously a more general test was designed to determine the limit of where copper wrap started to fail. For the second set of tests, an outside laboratory was brought in to research copper wrap plating in typical PCBs procured by GSFC. The primary objective of this second test was to demonstrate the relationship between the wrap plating thickness dimension defined in IPC-6012 Rev B, Figure 3-13, and thermal cycles to failure of the copper wrap plating. Test samples were exposed to simulated manufacturing followed by thermal cycling. The test sample design was based on a standardized interconnect stress testing (IST) coupon [13][14][15]. As per the test laboratory, this standardized IST coupon design was chosen as the base design because it contained many PTHs connected in series. One test sample was designed with 16 copper layers and another with 22 copper layers. These layer counts and the signal and plane layer stack-up were designed similarly to typical PCBs procured by GSFC. The test comprised four sets of boards; two sets were fabricated with polyimide and two sets were glass-reinforced epoxy FR-4. Two different board layer configurations were used for each of the two materials, one with 16 copper layers, and the other with 22 copper layers. Within each set, the boards were divided into four groups with three groups having different amounts of copper wrap.

Two laminate materials were chosen. The first was Isola P95 polyimide, with the test samples constructed with individual laminate containing 1080-style and 2116-style glass fabric weaves, and having either 1oz copper on both sides, 1oz on one side and 0.5oz on the other, or 0.5oz on both sides. The prepreg material was Neltec N7305-3 with either one 1080 or one 2113 style glass fabric weave. The second laminate material was Isola PCL-FR-370HR, an FR-4 epoxy-based glass reinforced printed circuit board material. These test samples were constructed with individual laminate each containing one C0040 style glass fabric weave, and having either 1oz copper on both sides, 1oz on one side and 0.5oz on the other, or 0.5oz on both sides. The prepreg material was Isola PCL-FRP-370HR with a single 1080 style glass weave. The plated

through holes were filled for all panels with a Taiyo THP-100 DX1 VF material.

Sixteen circuit board panels were designed and fabricated by Electro Plate Circuitry, Inc (EPC). Each panel contained twenty-two test samples and twenty-five or twenty-six A/B coupons, and had a unique construction identified by a number-letter combination. The construction variables were wrap plating thickness designated by the numbers 1 through 4, laminate material, and number of copper layers both designated by the letters A through D. Although controlling wrap plating thickness is difficult, an attempt was made by EPC to vary this dimension. The objective was to fabricate panels with the four different ranges listed below:

1. Test Sample Groups with Designation 1: 0.0mil
2. Test Sample Groups with Designation 2: >0.0 to 0.2mil
3. Test Sample Groups with Designation 3: >0.2 to 0.5mil
4. Test Sample Groups with Designation 4: >0.5mil to 0.7mil

In the manufacturing process, there were some samples rejected by the board manufacturer such that in some cases there were as few as 18 boards, out of the 22 total that were manufactured. As per the board fabricator, EPC, it is difficult to fabricate to precise targets due to large variation resulting from the planarization process. Of the missing boards the loss of boards was seen to be random in terms of the intended copper wrap thicknesses. Extra micro section coupons were fabricated to characterize panel variations, four or seven coupons were examined per panel, and eight measurements were taken per coupon, with two holes each.

The micro-section procedure involved first cutting the A/B coupons perpendicular from the strip along designated lines using a table equipped with a diamond blade. While cutting, it was ensured that the cutting path is far enough away from PTHs so as not to induce damage. After sectioning, the coupons were rinsed with deionized water and then dried. The A/B coupons from each coupon strip were placed in a bake out oven where these are baked for six to eight hours at 135°C ± 14°C. The thermal stress tests on A/B coupons was performed as per methods described in the IPC-TM-650 2.6.8, Test Condition A. During this test, the temperature of the pot was verified before initiating the test, and after thermal stressing, ethanol was used to ultrasonically clean the coupons for approximately five minutes to remove any flux residues. The coupons were then micro-sectioned as per the procedures described in IPC-TM-650 2.1.1. Measurements of the amount of copper wrap were taken after the coupons were micro-sectioned. Four box and whisker plots, one for each desired copper wrap thickness are shown in Figure 10 and summarized in **Table 2**.
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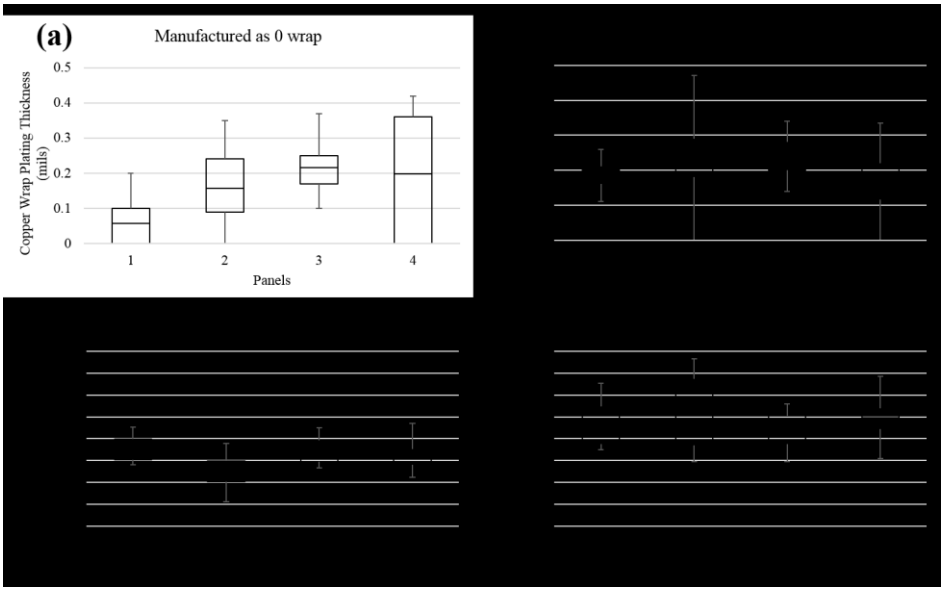


Figure 10 Four box and whisker plots showing the measured wrap thickness as a function of the intended wrap thickness. In this plot, panel 1 refers to 16-Layer Polyimide, panel 2 refers to 22-Layer Polyimide, panel 3 refers to 16 Layer FR4 and, panel 4 refers to 22-Layer FR4.

Table 2 Average and Standard Deviation of A/B Coupon Wrap Plating Thickness

	Polyimide				FR4			
	16 Layer		22 Layer		16 Layer		22 Layer	
	A (mil)		B (mil)		C (mil)		D (mil)	
Test Samples	Avg	StDev	Avg	StDev	Avg	StDev	Avg	StDev
1 (0.0mil)	0.06	0.06	0.16	0.11	0.22	0.07	0.2	0.16
2 (>0.0 to 0.2mil)	0.2	0.05	0.23	0.09	0.24	0.06	0.17	0.11
3 (>0.2 to 0.5mil)	0.95	0.19	0.5	0.14	0.67	0.12	0.65	0.12
4 (>0.5mil to 0.7mil)	0.7	0.12	1.05	0.31	0.86	0.15	0.99	0.16

While these results shown in Figure 10 are representative of the test samples, the wrap plating thickness varied across each panel surface, sometimes significantly. There is significant variation in the wrap thickness across each panel. The smallest observed range was 0.2 mils, and the largest was 0.94 mils. A gradient in thickness exists across the board from top to bottom and side to side, which suggests that localized variation in wrap thickness for adjacent coupons is likely minimal, while the variation from corner to corner can be large. Despite an emphasis on controlling wrap thickness, it was difficult to achieve.

Before the temperature cycling tests were started, a preconditioning process was performed to simulate typical soldering of Center electronic products and verify the electrical continuity of each test sample. The test samples were exposed to two identical reflow cycles to simulate one tin/lead (Sn/Pb) surface mount soldering profile and one Sn/Pb rework profile. A 22-layer test sample was used to profile the reflow oven and therefore was exposed to at least seven reflow profiles. This sample was chosen as one that would be most likely to fail, with the minimum wrap thickness and maximum board thickness. The preconditioning reflow profile with details is shown in Figure 11.

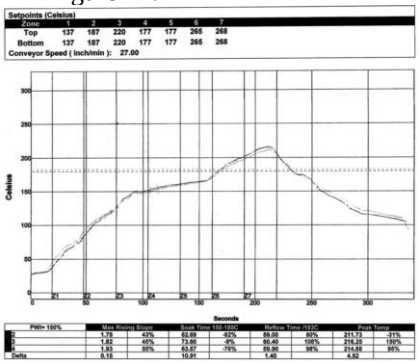


Figure 11 Reflow profile that was used to precondition the test samples. A Vitronics Soltec XPM730 seven-zone reflow system was used for the preconditioning.

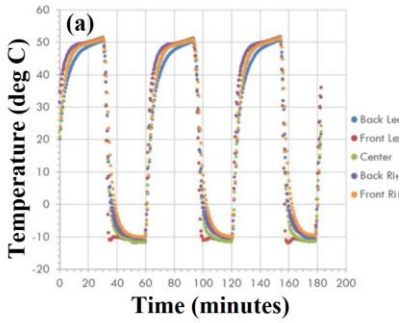
A micro-ohmmeter was used in a 4-wire setup to measure the resistance of the S1 circuit on each test sample. Resistance measurements were recorded at the beginning and end of the preconditioning process to verify electrical continuity after manufacturing and before test. The test samples were then placed in a temperature chamber for a bake out. The bake out was a typical manufacturing profile with a temperature of 125°C and bake out time of 24 hours.

Test samples were then exposed to and cycled between two temperature extremes to induce failures. The initial temperature ranges and thermal cycles that were requested were representative of typical environments Goddard electronics products are exposed to in project lifecycles. The two temperature ranges were -10°C to 50°C and -10ÁC to 75ÁC, for a of 60°C and 85°C, respectively. The high temperature tolerance was -0°C, +5°C. The low temperature tolerance was -5°C, +0°C. The test samples were exposed to 500 thermal cycles, defined as the period of time beginning at the ambient chamber temperature, followed by one high temperature excursion and one low temperature excursion, and ending at the chamber ambient temperature after the low temperature excursion. Data from the test are presented in Figure 12 showing the thermal profiles. Two-wire resistance measurements, with common ground, were recorded every three minutes during thermal cycling using a datalogger. These measurements were used to

identify breaks in electrical continuity of test samples that could then be removed from the thermal chamber and further analyzed to identify the failure location and mechanism. The temperature was recorded using thermocouples. Thermocouple readings were recorded every 20 or 30 seconds using a datalogger.

The relevant failure site at the PTH shoulders was the targeted site for these tests because it is the only location expected to be affected by the wrap plating thickness. During thermal cycling, an open circuit was defined as a recorded resistance measurement greater than 2kÙ. Cycles to failure of a sample was defined as the number of thermal cycles up to and including the first cycle during which at least one open circuit was measured, and at least one open circuit was measured during both of the two following cycles. If and when a test sample failure is recorded, the Test Laboratory planned to locate the failed PTH and cross-section the test sample to determine the location and morphology of the failure in the PTH.

Additional thermal cycles were requested after no failures were observed during the 500 thermal cycles. The temperature differential was increased in both thermal chambers. The low qpT chamber was cycled at 25ÁC to 125ÁC for a qpT chamber was cycled between the largest temperature extremes possible with the test setup: -55ÁC to 125Á180°C. Test a qpT samples in both thermal chambers were exposed to 200 cycles of the before-stated temperature ranges.



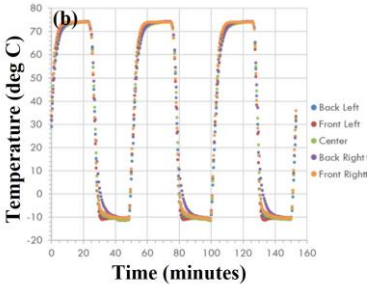


Figure 12 Thermocouple Profiles showing the temperature in the low qpT chamber (a) and high qpT thermal chambers.

No failures were observed during or after the first five hundred thermal cycles or after the additional two hundred cycled. The average difference of no greater than plus or minus one milliohm indicated that any measured difference was most likely from variation in applied pressure during measurement. While the pre-test measurements were taken with clips, many of the post-test measurements required probes because the wires had become brittle during the test and broke during test sample removal.

Experiment 3: Interconnect Stress Testing

The third test, an interconnect stress test (ISTqT: [13][14][15] was extended to take all coupons to qpT failure. The test was to use the IST test method, which involves passing current through a specially designed coupon to heat up the board. In an IST, DC current is applied to a test coupon, which contains a combination of heating circuits, test and monitoring net. The DC current causes a temperature rise in the conductors present in the coupon. Thermal cycling is achieved by cycling the current on and off. IST can simulate temperatures of solder reflow (up to 260°C) and thermal cycling from ambient to 190°C in ambient pressure conditions. Typically, a set number of solder simulation cycles are performed followed by temperature cycles to failure. Cycles to failure provide a figure of merit for ñrobustnessò.

In this case there were three sets of vias on a coupon. The first set of vias went completely through the 14-layer board. The second set of vias goes half way through the coupon, ending in a blind via. Because of the manufacturing process two different sets of coupons are required for the blind vias. One set has the vias on the ñTopò, while the second set

has the vias on the third set of vias has the current path going down only one layer of the coupon, except at one place where the via goes all of the way through the board. The through hole is half way through the circuit and is used to take the current to the other side of the board where it again then goes up and down one layer. This circuit is called the "power" or heating circuit, which is intended to heat the ends of the board, to balance out any end effects. A schematic showing the top surface of the IST coupon is shown in Figure 13.

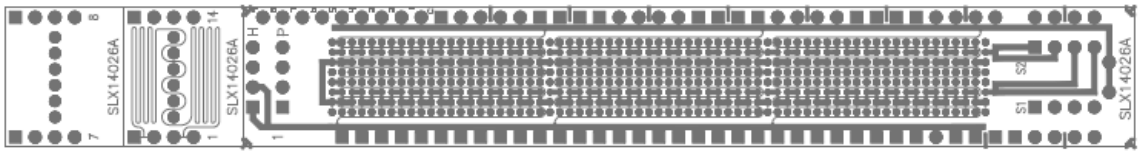


Figure 13 Top layer of IST coupon. Note provisions for 4 wire resistance measurements.

In the 3rd experiment, three copper wrap scenarios were used: one with no wrap, one with 0.2 mil wrap, and one with the standard 0.5 mil copper wrap (per the requirement). The coupons were polyimide, manufactured by Viasystems. Micro-sectioning was performed on samples and showed that the requested dimensions had been achieved. Tests are run by thermal cycling coupons to failure or test termination (time-terminated). Failure is defined as an increase in the resistance of 10% above the original resistance of the daisy-chained vias at ambient temperature.

Prior to the start of the IST tests, the coupons were subjected to a simulated soldering condition by exposing them to a 245°C temperature. Testing, starting with the temperatures cycling between ambient and 150°C, was performed on 6 coupons. All of the failures that occurred were on the via network that traverses all 14 layers. The earliest failure was recorded after 2001 cycles, and the longest was after 2323 cycles. No failures were reported with either the 7 layer vias, or the 1 layer (power) vias. At this time, it was realized that the boards were made of Polyimide and not a G-4 material as initially assumed. G-4 uses the 150°C as the baseline test temperature, with polyimide normally being tested to 190°C. It was then decided to run the next thirty-six coupons to a peak test temperature of 210°C.

Of the thirty-six coupons tested at 210°C all had failures of the through holes. The blind hole vias had 9 failures, and the power vias had only a single failure. All types of boards had cases where all of the 7-layer vias failed, and only one coupon had a 1-layer via failure. Coupons that did not fail in test were terminated at 1300, 1500, or 1700 thermal cycles respectively. Resistance was monitored continuously during testing.

The cumulative failures per type of via and copper wrap thickness were documented and are shown in Table 3. Note the coupon that experienced a power or heater circuit failure could only be cycled up to 1013 cycles. *-test was suspended

Table 4 shows the minimum number of cycles on a type of wrap before any failure was noted, in this case too, the coupon that experienced a power or heater circuit failure could only be cycled up to 1013 cycles.

Table 3 Number of failures per type of via and copper wrap thickness.

	0.0 mil Wrap	0.2 mil Wrap	0.5 mil Wrap
14 Layer Via	12	12	12
7 Layer Via	4	6	0 after 1500* Cycles
1 Layer Via	0 after 1500 Cycles	0 after 1500 Cycles	1

*-test was suspended

Table 4 Minimum cycles to a failure.

	0.0 mil	0.2 mil	0.5 mil

	Wrap	Wrap	Wrap
14 Layer Via	259	135	128
7 Layer Via	448	372	0 after 1500* Cycles
1 Layer Via	0 after 1500 Cycles	0 after 1500 Cycles	1013

*-test was suspended

A Weibull analysis of the coupon test failures was performed. The through-hole via data were compared using normal, log-normal and Weibull distributions. Using the software, Weibull distribution provided the best statistical goodness-of-fit, after the multi-modal distributions were accounted. A comparison of the failure distributions for the through hole via coupons is shown in

Figure 14.

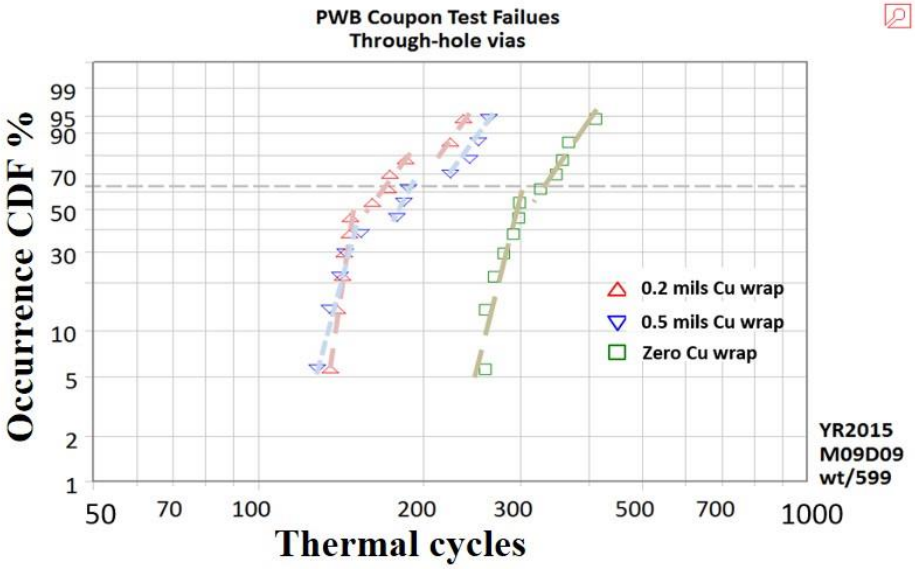


Figure 14 Comparison of failure distributions of the IST coupons for the through-hole vias geometry.

For through-hole via, all (no-wrap, 0.2 and 0.5 mils copper wrap) exhibited multi-modal distributions for cycles-to-failure. It was observed that the coupons with no wrap show a bimodal distribution and a likely tri-modal for the coupons manufactured with the 0.2 and 0.5 mils copper wrap. Further, comparisons between through-hole via samples showed statistically significant differences, at a 90% confidence, for cycles-to-failure between both early and later distributions for the no wrap and 0.2 mil or 0.5 mil copper wrap coupons. The Weibull shape parameters for all through-hole via failure distributions were not significantly different. For through-hole vias, cycles-to-failure were not significantly different between 0.2 and 0.5 mil copper wrap coupons, for either the early or later distributions. The reliability of zero copper wrap coupons is better (i.e., exhibited longer times-to-failure) than either 0.2 or 0.5 mils copper wrap coupons. It is important to emphasize here that these failures only occurred in the extreme test conditions that were required to induce a failure, which were well outside of any application range for GSFC ôs There was no statistically significant difference in lifetimes (reliabilities, or cycles-to-failure) between 0.2 and 0.5 mil copper wrap coupons.

In the coupons with the blind via geometry, only the 0.2 mils copper wrap coupons provided sufficient data for comparison with through-hole via coupons. The blind via samples exhibited a larger variation in cycles-to-failure that occurred at longer times than for copper-wrapped through-hole vias. This larger variance is consistent with

general fatigue testing, which shows greater times-to-failure scatter in test units that are at lower stress levels[36]. A comparison of the through hole coupons with other blind via coupons was not performed due to the insufficient failure data among the other blind via coupons tested. Later examination with a thermal camera of the coupons could not find where the flaw was located. It is unclear if the resistance change seen was from a single via, or found across many vias.

Out of the 36 test coupons that were stressed, six coupons were examined by micro-section. One from each type of coupon was selected for the test. Also of note is that for any wrap thickness (3 types) there was always one sample from an early failure group, and one from a delayed failure group, and the selection of sectioned coupons was random. For the six sections, all have shown barrel cracks as the failure mechanism. The micro-sectioning suggests that the failure sites are at the copper barrel and not at the location of the copper wrap as projected. Representative images of the three cases: no-wrap, 0.2-mil and the 0.5-mil, are shown in Figure 15. The arrows in the micro-sectioned images shown in Figure 15 point to the crack tips at the plated through holes. Cracks appear to be caused by fatigue, induced due to the differential in CTE between the organic PCB material and the copper barrel.

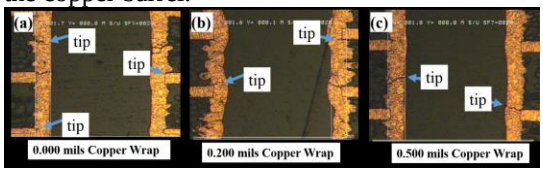


Figure 15 Representative images of the three cases, no-wrap, 0.2mil and the 0.5 mil showing cracks in the copper plated barrel of the plated through hole.

Table 5 lists the geometry parameters, with dimensions as defined in Figure 16.

Finite Element Modeling

In conjunction with the physical testing on the IST coupons, a finite element analysis was adopted, which helped in supplementing the test results. Using the COMSOL Ê Multiphysics software, plated-through-holes were modeled under thermal stress conditions. A steady state analysis was used, applying a 190°C boundary condition to the ambient article. Three vias were simulated in COMSOL Ê. They were to simulate a fourteen-layer polyimide laminate with an epoxy material. The COMSOL Ê modeling assumed no defects.

A single PTH surrounded by laminate was created as the model geometry. This was considered to be the worst-case condition, as the heated laminate would expand locally around the PTH without constraint from mounting fixtures or any adjacent PTHs. Opting to use a single PTH, as opposed to an array of vias, also significantly reduced the FEA computation time. Given that this simulation is a parallel to experimental testing performed on PCB coupons, the geometry of the finite element article correlates to the previously discussed IST coupons from the ICESat-2 GPS receivers. These are 14-layer polyimide boards fabricated to IPC-6012B Class 3/A quality criteria. The geometry was defined in accordance with the design drawing, fabrication notes, and coupon microsection report (minimum observed values).

Table 5 Geometry definitions for finite element analysis

Parameter	Variable	Value [in]	Source
Board layers	layers	14	Design
Board stack-up	t_stackup	0.124	Calculated from below parameters
Dielectric thickness	t_dielectric	0.0076	Microsection
Hole diameter	hole_diameter	0.012	Design (nominal value)
Cap plating thickness	t_cap	0.003	Microsection
Wrap plating thickness	t_wrap	0.0005	IPC-6012B 3/A
Barrel plating thickness	t_barrel	0.0017	Microsection
External foil thickness	t_extfoil	0.0007	Microsection
Internal foil thickness	t_intfoil	0.0014	Microsection

Annular ring/pad size	EAR	0.0155*.8	Design, 20% reduction per IPC-6012B 3/A
Etchback	etchback	0.00035	Microsection

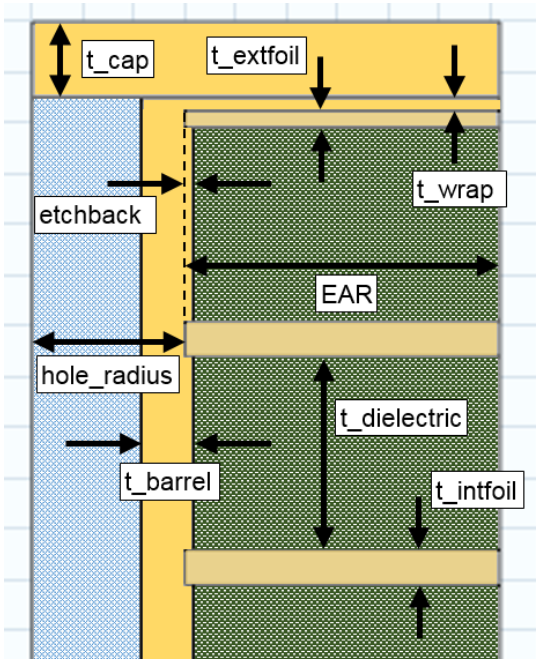


Figure 16 Sketch showing the geometry variables as defined in the virtual cross-section

This study was evaluated in a 3D space to allow for orthotropic material definition and to account for the multiaxial interactions occurring with thermal expansion. The PTH was modeled by defining a 2D work plane for a quartile of the cross-section, which was mirrored over the XY plane and rotated 360° to create the 3D hole structure. The PTH was then surrounded by a block of dielectric to represent the PCB test article (dielectric may be virtually hidden in some of the figures so as to not obscure the PTH).

The material properties were defined in accordance with manufacturer data sheets and literature, [16]-[29], as summarized in Table 6. The laminates and via fill materials were selected based on historical usage in NASA GSFC flight PCBs. The mix includes different laminate blends including polyimides, FR-4, and ceramic materials. The Taiyo THP-100DX1 VF via fill is electrically non-conductive, while the DuPont CB100 fill is conductive, lending to sufficiently differing characteristics for this analysis.

Table 6 Material definitions for laminates, via fills, and copper

	T_g [°C]	Ǔ / ₂Ǔ [ppm/°C]	c_p [J/gK]	ɟ [lb/in³]	k [W/mK]	E [ksi]	ə
Laminate							
Isola P95	260	{13,14,55}	0.95	0.058	0.2	3892	0.187
Arlon 85N	250	{16,16,55} / {16,16,149}	0.94	0.058	0.2	3200	0.15
Nelco N7000-2 HT	260	10	1.06	0.061	0.45	3100	0.146
Rogers RO4350B	280	{10,12,32}	0.9	0.067	0.69	2432	0.4
Duroid 6002	N/A	{16,16,24}	0.93	0.076	0.6	120	0.4
Isola HR370	180	{13,14,45} / {14,17,230}	0.94	0.058	0.4	3744	0.177
Via Fill							
Taiyo THP-100DX1 VF	155	32 / 81	900	0.059	0.58	652.67	0.34
DuPont CB100	115	27 / 47.2	309	0.2	3.5	2000	0.34
Copper							
Copper foil	N/A	17.7	385	0.32	391	17000	0.35
Electroplated copper	N/A	17.7	385	0.32	401	18850	0.34

T_g = glass transition temperature, Ǔ / ₂Ǔ = coefficient of thermal expansion (CTE) Ǔ below/above T_g, c_p = specific heat capacity at constant pressure, ɟ = density, k = thermal conductivity, E = elastic modulus

Figure 22 Strain plotted on the model cross-section

The strain results were compiled for the various test cases simulated, as well as for the volumes or interfaces of interest as plotted in the subsequent figures, as shown in

Table 7. These results are further discussed in the risk analysis section.

Table 7 Compilation of simulation results for maximum strains.

Wrap Thickness Sweep				
Wrap Thickness [in]		**Barrel Strain**	**Wrap Strain**	**Wrap Edge Strain**
0.0006		0.017	0.019	0.012
0.0004		0.017	0.021	0.012
0.0002		0.017	0.019	0.012
0		0.017	0.017*	0.012
Electroplated Copper Property Sweep				
Elastic Modulus [ksi]	**Poisson's Ratio**	**Barrel Strain**	**Wrap Strain**	**Wrap Edge Strain**
E=18855	ə = 0.34	0.017	0.020	0.012
E+10%=20740		0.017	0.020	0.013
E-10%=16969		0.016	0.020	0.012
E=18855	ə + 10% = 0	0.016	0.019	0.012
	ə-10%=0.306	0.017	0.021	0.013
Laminate and Via Fill Material Mix				
Laminate	**Via Fill**	**Barrel Strain**	**Wrap Strain**	**Wrap Edge Strain**
Isola P95	Taiyo THP-100DX1 VF	0.017	0.020	0.012
	DuPont CB100	0.015	0.014	0.012
Arlon 85N	Taiyo THP-100DX1 VF	0.017	0.020	0.013
	DuPont CB100	0.016	0.014	0.012
Nelco N7000-2 HT	Taiyo THP-	0.014	0.020	0.010

would be suitable for most common use environments (i.e., not at extreme temperatures).

Comparing the via fills, the Taiyo THP-100DX1 VF presented slightly higher strains than the DuPont CB100 material. While the Taiyo fill has a higher T_g at 155°C compared to the DuPont's 115 °C, the post-T_g CTE is nearly double (81 vs. 47.2 ppm/°C). Further, the elastic modulus of the DuPont material is over triple that of the Taiyo. Again, for most use environments these fills would perform similarly; these differences are exacerbated in this study given the high-temperature environment.

Table 10 Maximum strains for variable laminate and via fill materials

Laminate and Via Fill Material Mix				
Laminate	**Via Fill**	**Barrel Strain**	**Wrap Strain**	**Wrap Edge Strain**
Isola P95	Taiyo THP-100DX1 VF	0.017	0.020	0.012
	DuPont CB100	0.015	0.014	0.012
Arlon 85N	Taiyo THP-100DX1 VF	0.017	0.020	0.013
	DuPont CB100	0.016	0.014	0.012
Nelco N7000-2 HT	Taiyo THP-100DX1 VF	0.014	0.020	0.010
	DuPont CB100	0.013	0.014	0.010
Rogers RO4350B	Taiyo THP-100DX1 VF	0.015	0.020	0.011
	DuPont CB100	0.013	0.014	0.011
Duroid 6002	Taiyo THP-100DX1 VF	0.015	0.020	0.012
	DuPont CB100	0.015	0.014	0.012
Isola HR370	Taiyo THP-100DX1 VF	0.045	0.021	0.022
	DuPont CB100	0.046	0.021	0.022

Of the properties studied in this simulation, the laminate and fill material selection will have the greatest impact on the risk for fatigue failures in PTHs. To mitigate the risk, high reliability materials should be used that have lower expansion rates and a glass transition temperature well above the expected use environment.

To validate the model against the test data, a prediction of cycles to failure may be estimated from the FEA-computed strain values. IPC-TR-579 [35] presents an equation and graphical representation of a Coffin-Manson cyclic strain life, originally developed by Engelmaier and Kessler for electroplated copper in PTHs [37].

Figure 29 Coffin-Manson cyclic strain vs. fatigue life plot for electrodeposited copper (IPC-TR-579)

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