NASA Electronic Parts and Packaging (NEPP) Field Programmable Gate Array (FPGA) Single Event Effects (SEE) Test Guideline Update

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I. INTRODUCTION

Critical space-applications require minimal malfunction, high percentages of availability, and virtually no risk of device damage during mission deployment. Because it has been shown that electronic devices are susceptible to space environment ionizing particles (radiation effects) [1-3], significant effort is given to device radiation hardness assurance.

Field Programmable Gate Arrays (FPGAs) are widely used in critical space-flight applications as controllers, data-flow infrastructure, and data processors. Due to their principal roles throughout systems, the integrity of FPGA operation is instrumental to mission success.

In 2012, NASA Electronic Parts and Packaging (NEPP) developed a robust test and analysis (hardness assurance) methodology for FPGA component evaluation and SEE data application [4]. Since 2012, FPGA circuit complexity has increased exponentially. With the combination of complexity management and years of lessons learned material, the documentation is currently being updated. This manuscript highlights a select portion of the guideline updates.

II. OVERVIEW OF UPDATES

The following are updated or new subjects added to the NEPP FPGA SEE Test Guidelines manual: academic- versus mission-specific device evaluation, single event latch-up (SEL) test and analysis, SEE response visibility enhancement during radiation testing, mitigation evaluation (embedded and user-implemented), unreliable design and its effects to SEE data, testing flushable architectures versus non-flushable architectures, intellectual property core (IP Core) test and evaluation (addresses embedded and user-inserted), heavy-ion energy and linear energy transfer (LET) selection, proton versus heavy-ion testing, fault injection, mean fluence to failure analysis, and mission specific system-level single event upset (SEU) response prediction.

Most sections within the guidelines manual provide information regarding best practices for test structure and test system development. The scope of this manual addresses academic- versus mission-specific device evaluation and visibility enhancement in IP Core testing.

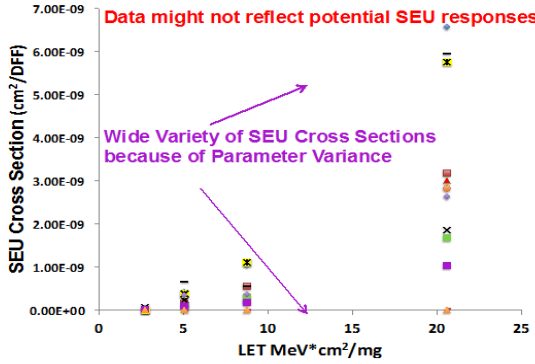# III. ACADEMIC- VERSUS MISSION-SPECIFIC DEVICE EVALUATION

Figure 1: Shift Register SEU cross sections with design parameter variation [5].
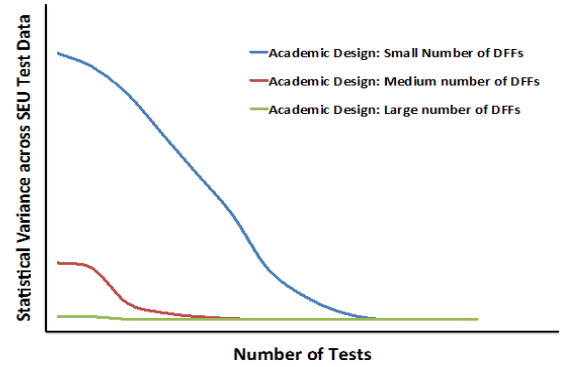

Figure 2: Statistical variation of SEU data across the number of tests based on the number of DFFs in the shift register test structures. All test parameters are held constant except for the number of DFFs.

Currently, radiation beam accessibility for device sensitivity testing is limited; hence it is important to carefully define goals and means for achievement. As a part of goal identification, a distinction should be made regarding the purpose of radiation-susceptibility data collection: (a) academic study for component-level SEE sensitivity; or (b) extrapolation for mission survivability predictions.

A. Academic Component-Level Studies

Conventionally, shift registers are used for academic component-level SEE analysis. Shift registers are implemented using flip-flops (DFFs), combinatorial logic, and global routes (clocks and resets). They are commonly selected as test structures because of the following:

- The study is geared to analyze flip-flop (DFF) sensitivity.
- Test structures are relatively easy to create and fabricate.
- The full state space is visible to the test system; hence data collection is easily comprehensible.

Shift registers can be tested with a range of parameters: operational frequency, number of combinatorial logic gates between stages, and input data patterns. It is important to note that parameter variation can significantly impact SEU data. Figure 1 illustrates shift register SEU data obtained during heavy-ion testing in the form of SEU cross sections (SEU_{errors}/(DFF•(particle-fluence/cm^2))). Figure 1 shows that parameter selection can cause susceptibility data to vary with orders of magnitude. If the full range of parameters is not explored, data interpretation can be misleading. As a clarification, if test parameters are overlooked or unobtainable during test, then component susceptibility reporting can cause incorrect design implementations; and hence can lead to catastrophic events.

Statistics should be taken into account during testing. If the test structure contains a small number of repeatable components, then it is up to the investigator to increase the number of tests in order to decrease statistical variation between data. Figure 2 illustrates statistical variation based off of repeatable test components versus number of tests performed.

A benefit of academic component-level testing is that it gives the investigator an insight into individual component sensitivity sans masking-effects. However, it is imperative that results be correctly interpreted and extrapolated. As an example, design topology and design complexity can cause component susceptibility to either decrease (due to de-rating) or increase (due to poor design decisions). As a result, a significant amount of research targets extrapolation of data into synchronous design topologies and smart selection of mitigation strategies per device susceptibility. Although work is being done to better perform data extrapolation, discrepancies and limitations currently exist. In response, if the goal is to determine mission-specific survivability, a new approach is being developed under the NASA Electronic Parts and Packaging (NEPP) program [6]. This approach incorporates combining academic component-level SEU testing and mission-specific design SEU testing.

B.   Mission-Specific Evaluation

In order to calculate mission survivability predictions, it is best to analyze systems that closely resemble those that will be employed in the mission. This requires the system-under-test have comparable complexity and maintain proper design topology. As an example, due to reliability, most missions strictly require synchronous design topology be implemented throughout all digital circuits. Hence, in order to obtain representative data, it is imperative that systems-under-test also strictly use synchronous design topology.

The primary concern for SEU testing is that mission-specific applications are complex systems that make SEU data collection challenging. This is mostly because visibility into system circuitry and state space traversal are minimized per SEE test. As a result, data obtained during radiation testing can be misrepresentative. Consequently the susceptibility data might not correctly characterize SEU response per mission specific operational modes, and could hence lead to poor (and perhaps catastrophic) design implementations.

The following are a few methods that have been developed to enhance SEU data collection: (1) investigate a variety of test structures that vary in complexity; (2) vary operational frequency and input patterns; (3) force a variety of state-space traversal schemes per test; (4) perform as many tests as possible; (4) and increase visibility of internal circuits and their contributions to susceptibility. The intent of variation is to study trends of SEU responses across a variety of parameters, designs, and state traversal. These actions help to identify dominant sources of error and better extrapolate data to mission-specific systems.

IV.   MISSION-SPECIFIC SURVIVABILITY PREDICTION

The current method for SEU survivability prediction is based off of transistor-level energy deposition and extrapolation [7]. As previously mentioned, NEPP is currently developing a novel methodology for calculating mission survivability through potential single events. The new strategy uses a top-down system-level approach using empirical SEU data and classical reliability models [8]. An interesting aspect of the methodology is that classical reliability models are transformed from the time domain to the particle fluence (Φ) domain. In addition, the system level approach acknowledges the nonhomogeneous nature of FPGA transistors by moving away from performing transistor level energy deposition calculations. Alternatively, the method relies on the strength of the SEU empirical data obtained by testing systems that represent mission-specific requirements.

The following is a synopsis of the proposed methodology:
- Create a histogram of particle flux (Φ for a given time window) versus LET. The time window and fluence per LET is selected from mission requirements. An example histogram for a 10-minute required window of operation is illustrated in Figure 3.
- Obtain SEU data and calculate mean-fluence-to-failure (MFTF) per LET. LETs used in this calculation are the effective LETs selected during radiation testing.
- Graph reliability with respect to particle fluence ($R(\Phi)= e^{-\Phi/MFTF}$) for each histogram bin [6][8]. Although each bin contains a range of LETs, the selected MFTF for the reliability calculation is and upper-bound; i.e., the selected

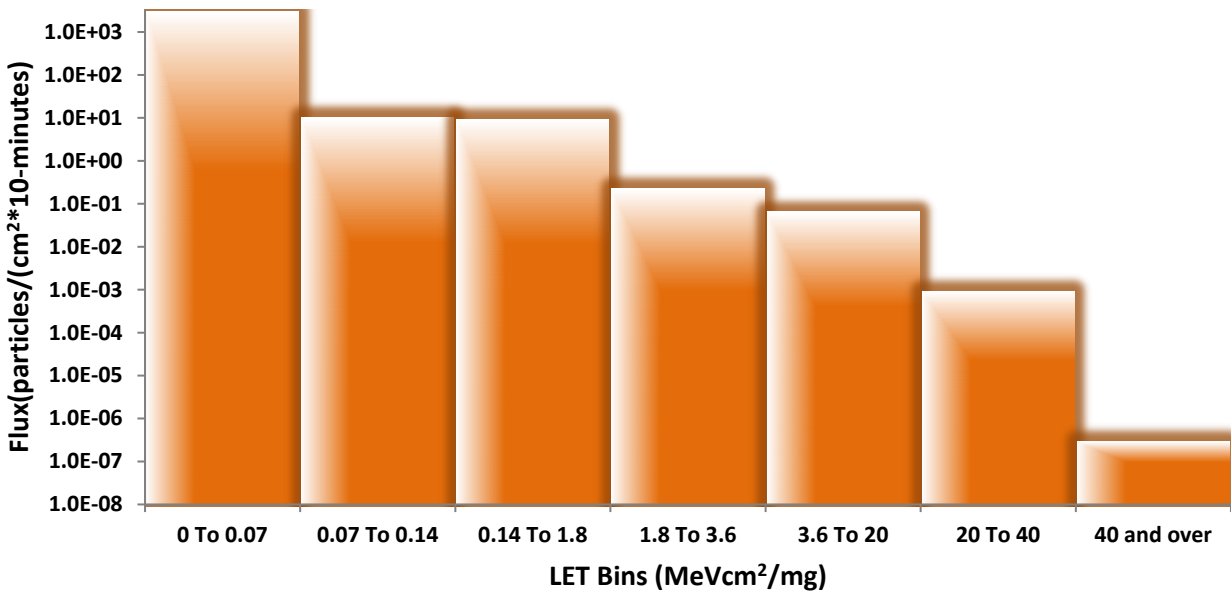MFTF corresponds to the highest LET within the bin under investigation.

Figure 3: Environment Data: Flux versus LET Histogram for A 10-minute Window. Target environment is Geosynchronous Equatorial Orbit (GEO) with 100-mils shielding. Bin boundaries are selected based off of effective LET values used during SEU testing.

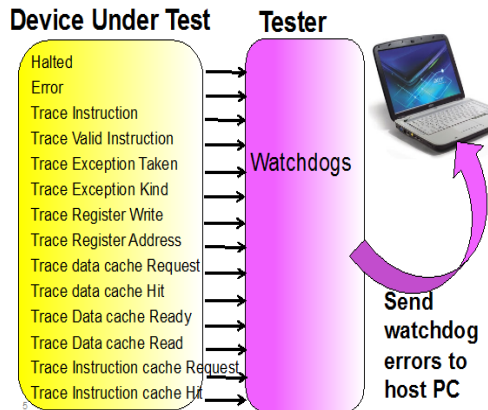## V.   VISIBILITY ENHANCEMENT IN IP CORE TESTING

Figure 4: Increasing visibility for a microprocessor IP Core during SEU testing.
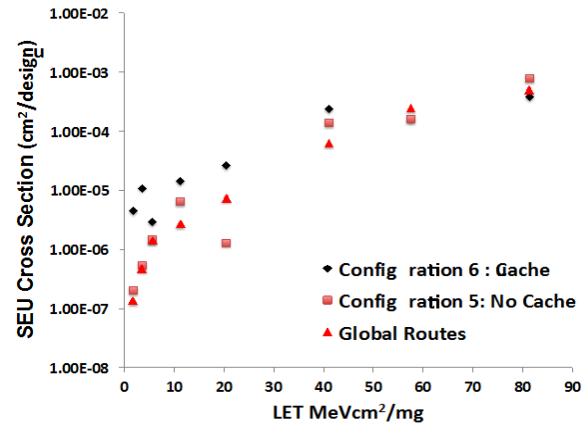

Figure 5: Heavy-ion SEU data for microprocessor IP Core. Two architectures were tested: with cache and without cache. Cache implementation had no fault tolerance.

IP Core test and analysis (T&A) is challenging because the IP are generally considered black-boxes of complex circuitry. Consequently, visibility of internal sensitivity is minimal.

IP Cores are implemented in a variety of methods: embedded in FPGA fabric (hard IP), user-inserted hardware description language (HDL), user-inserted gate-level netlist (GLN), or user-inserted encrypted circuitry. Embedded and encrypted IP Core circuitry are not visibility to the user. Alternatively, HDL and GLN user-inserted IP cores are visible. The challenge is, although visible, IP Core circuitry can be too complex to parse or comprehend.

One method of enhancing visibility during SEE testing is to parse HDL and GLN IP Cores, collect internal-vital signals, send the signals to a tester, and watchdog the signals for correct operation. A couple of benefits with applying this enhancement are: SEU data can be better attributed to component sensitivities; and SEU cross sections can be more accurately calculated. This level of visibility into embedded microprocessors for SEU testing is a novel approach . Extracting

internal-vital signals for SEU testing is a difficult process, however, it is feasible and should be performed.

As a test case, NEPP tested an embedded microprocessor IP Core in a Xilinx Virtex 5 FPGA. Two microprocessor architectures were analyzed: (1) IP Core instantiation with cache (no fault tolerance) and (2) IP Core instantiation without cache. The intent was to evaluate the sensitivity of IP Core cache circuitry.

The core was parsed in order to extract critical internal microprocessor signals. A portion of the signals is depicted in Figure 4. As previously described, the signals were fed to a customized tester and watchdogs were developed based off of expected signal behavior. Watchdog violations were time-stamped, packaged, and sent to a host PC for SEU data collection.

Figure 5 illustrates the microprocessor IP Core calculated SEU cross sections obtained from heavy-ion testing. As a result from implementing test enhancements, data was compartmentalized based off of component SEU responses and sensitivity dominance could be analyzed. The mission used the SEU data to determine components that require mitigation (based on mission requirements) and which type of mitigation would fulfill design specifications.

VI.   SUMMARY

The evolution of technology is causing potential complexity of FPGA designs to grow rapidly. This has impacted SEU test and analysis and SEU data extrapolation for mission survivability predictions. In order to keep up with technological advancements, the NEPP FPGA test guidelines manual is currently being updated. This document provides a synopsis of updates and new material.

VII.   REFERENCES

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