Power Integrity Analysis of Low Power SOC Design

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Abstract. With the development of process and design technology, the power integrity of low power SOC design meets new problems and challenges. Quantitative analysis is needed to guide the design of power-gating units for low-power SOC design, such as structure selection, the number and size confirmation, and placement optimization. Some new phenomena, such as rush current, rampup time, Power noise coupling and so on, needs to be analyzed and optimized. Static check, dynamic check and powerup analysis are needed to analyze the power performance of low power SOC design. In this paper, ANSYS Redhawk is used to analyze the power integrity of low-power design, and the power performance of low-power SOC design is obtained. Finally, the design of this paper meets the design performance requirements through chip test.

1. Introduction

With the reduction of the characteristic size of semiconductor and the improvement of integration, the leakage current plays more and more important role in the whole chip power consumption. For some specific applications, standby power consumption has become an important indicator of the chip. In order to reduce power consumption from all aspects and meet the challenges of low-power application scenarios, the design of this paper adopts low power design technology such as multi-voltage domain and power gating. For special low power design, under the condition of low power consumption, small size, the allowance for designers is also becoming smaller and smaller. Therefore, it is necessary to analyse quantitative of power integrity and reliability in the design of Low Power.

Power integrity analysis of low power SOC design includes: power-gating structure selection, quantity planning, location and the balance between rush current and ramp up time when powerup, considering power-gating module noise coupling to other always-on modules, calculating power switch actual working scenarios current, calculate the leakage current of power gating module in turn off state. This paper uses RedHawk designed by ANSYS to analyse the power integrity for low power design. Including power grid extraction for Low Power design, power-to-ground network robustness checking, power-to-ground network rule-based EM checking, as well as static and dynamic full-chip voltage drop analysis, power-gating module ramp up process and ramp down process key parameter analysis, and the power switch on-state maximum current analysis. Based on the above analysis, the designer can find the bottleneck of power network design in time to optimize the power plan and power gating design.

2. Redhawk Analysis Flow

RedHawk can simulate the transient power consumption as high as picosecond accuracy, and complete the power integrity analysis of the low power design of the whole chip in a fast and reasonable time. RedHawk considers the effects of on-chip and off-chip devices, SPICE simulation level standard cell model, capacitance load, on-chip package, parasitic power network parameters of PCB board, and so

on, which greatly improves the analysis accuracy of low-power design. The flow of power integrity analysis using Redhawk for low power design is shown in figure 1.

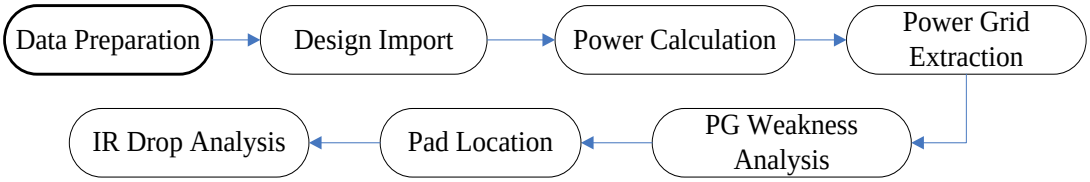

Figure 1. Power integrity analysis flow of Redhawk

2.1. Data Preparation

The input data files for power integrity analysis using Redhawk are all contained in the GSR (Global System Requirements) file, and the main input files are shown in figure 2.

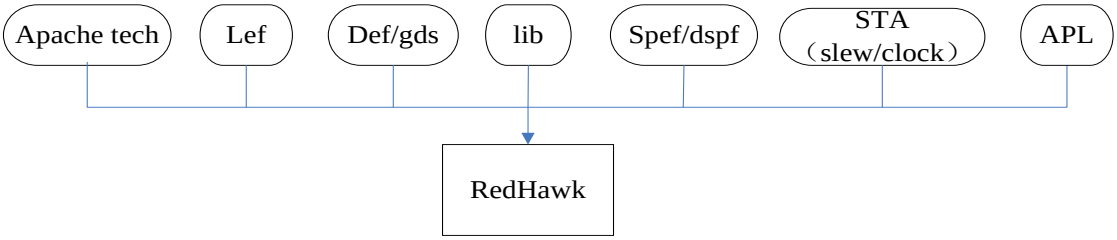

Figure 2. Input data of Redhawk

LIB and LEF file is standard format provided by process vendors.

Apache TECH file: A process file containing the description of wire information, usually provided by a process manufacturer, can also be converted to produce TECH FILE by rhtech command.

APL (Apache Power Library) file: It contains the current waveform, capacitance waveform and parasitic parameter information of the standard cell under different input transition time, output load and power supply voltage conditions using SPICE simulation. The way to generate APL files is shown in figure 3. The APL model files for low power design include current model of standard cell, CDEV model of standard cell, CDEV model of cap cell, APL PWL (piece-wise-linear) cap model of standard cell, APL PWL (piece-wise-linear) cap model of cap cell and power switch model.

DEF: Design Exchange Format, it contains the connection relationship of the circuit and the layout and routing information of the circuit. The DEF file is extracted by the physical designer after the layout and routing is completed.

PAD location file: The location definition information that contains the power integrity analysis is provided by the physical designer.

STA file: Contains the maximum and minimum transition time clock window information and clock network information, which is obtained by ATE engine, it is generated as shown in figure 4.

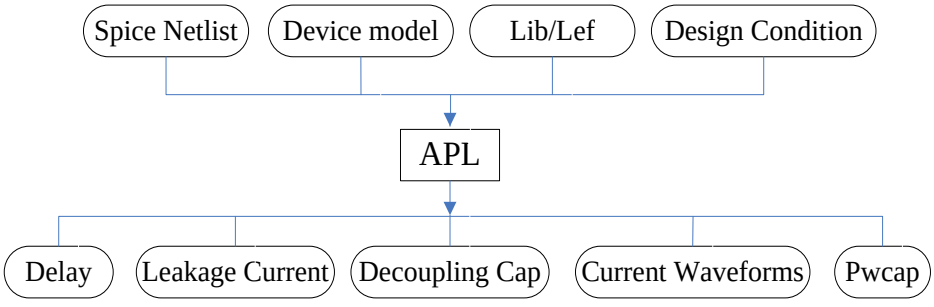

Figure 3. Generation and output of APL file

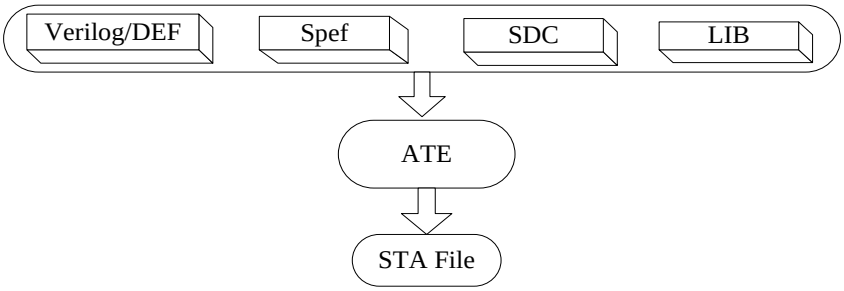

Figure 4. Generation method of STA file

2.2. Power Consumption Calculation

The power integrity analysis of low power SOC is based on the calculation of design power consumption. RedHawk can calculate the power consumption based on VCD waveform file and according to user defined toggle rate. Redhawk calculates power based on the principle shown in figure 5. Leakage power comes from the cell library, and internal power comes from the cell library lookup table. Switching power is calculated according to the toggle rate in the VCD waveform or the toggle rate set by the user.

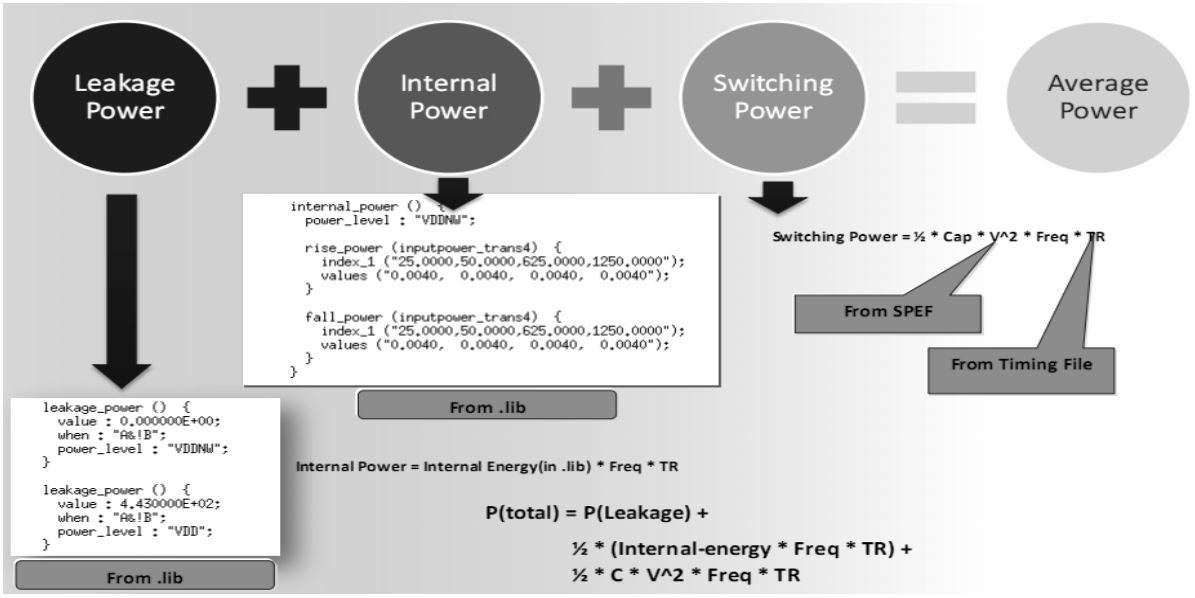

Figure 5. Power calculation principle

2.3. Power Network Extraction and Integrity Analysis

Based on the analysis of the power-to-ground network in the def data, the power-to-ground network is extracted into equivalent resistance, inductance and capacitance, etc., as shown in figure 6. According to the design power consumption calculation, the extracted network parameters of the circuit power supply, PAD location and other information are obtained, the power integrity analysis of the designed Static check, Dynamic check and PowerUp is completed.

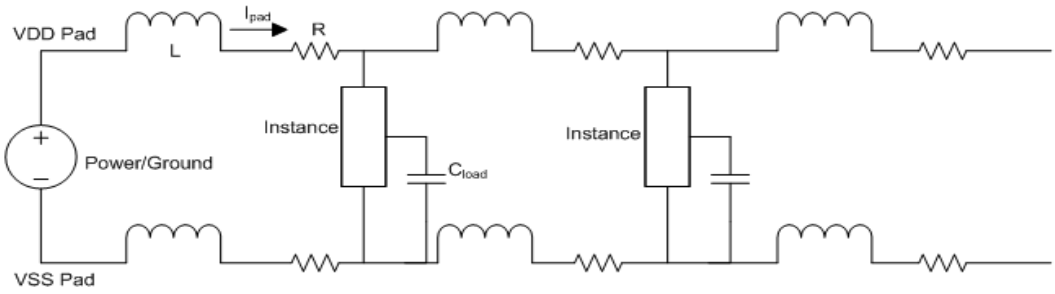

Figure 6. Power network extraction principle

3. Power Integrity Analysis of a Low Power Design

The design in this paper is a low power SOC chip, which is designed and manufactured in 55 nm process. Power gating and multi-voltage domain techniques are adopted. The design scale is about 3 million gates and the main clock frequency is 160MHz. It contains two voltage domains of 1.2V and 1.0V, the power gating region is in 1.2V and 1.0V voltage domains. The power gating area is connected by a single port power gating cell by a daisy chain. The voltage domain distribution is shown in figure 7. The connection of power gating cell is shown in figure 8.

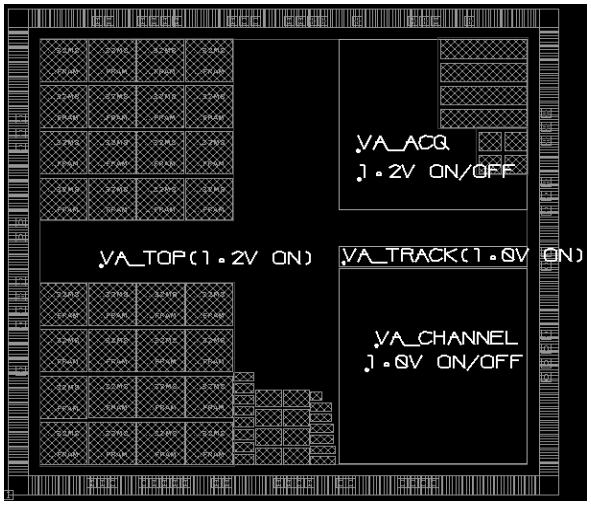

Figure 7. voltage domain distribution map

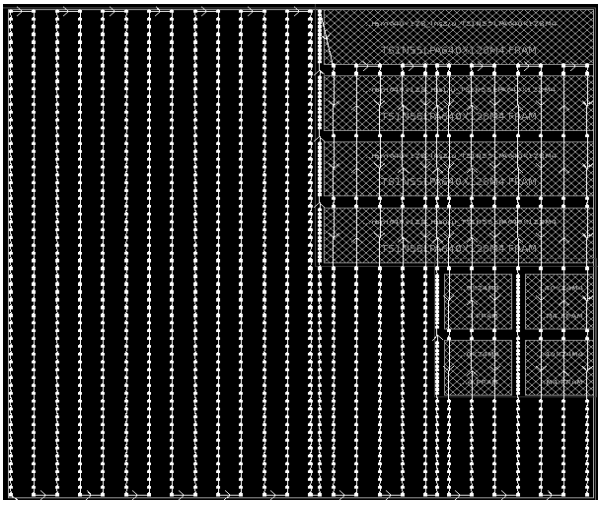

Figure 8. power gating cell connection of VA_ACQ

3.1. The Switch Model Generation of Power Gating Cell

For the power gating cell with a single control signal, the key configuration file content for generating the power switch model is shown in figure 9.

```
SWITCH_TYPE HEADER              ; the switch cell type: HEADER/FOOTER
EXT_PIN TVDD                    ; input POWER/GROUND pin of the switch cell
INT_PIN VDD                     ; output POWER/GROUND pin of the switch cell
GND_PIN_NAME VSS                ; GROUND/POWER pin of the switch cell
VDDVALUE 1.32
ON_STATE {
NSLEEPIN 1.32    }              ; ON State condition. NSLEEPIN is the control pin
OFF_STATE {
NSLEEPIN 0       }              ; OFF State condition.
POWER_UP {
NSLEEPIN 1.32    }              ; OFF State condition.
POWER_DOWN {
NSLEEPIN 0      }
CONTROL_PIN NSLEEPIN R F        ; Control pin function define
```

Figure 9. Configuration file of power switch model

3.2. The Switch Model of Power Gating Cell

In the power integrity analysis of a low power SOC with power gating cell, the equivalent circuit models of power gating cell during the modes of ON State, OFF State and Power Up are shown in figure 10, figure 11 and figure 12.

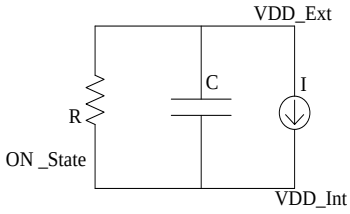

Figure 10. On state model

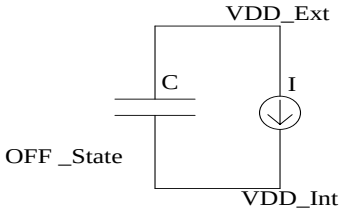

Figure 11. Off state model

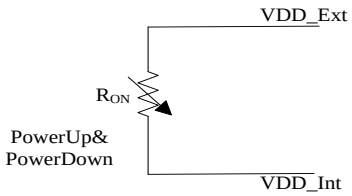

Figure 12. Powerup state model

Finally, the switch model content of the single port power gating cell used in this design is shown in figure 13.

```
SWITCH_CELL HDRSID1BWP12THVT {
   VDD 1.32 {
        SWITCH_TYPE: HEADER
        EXT_PIN: TVDD
        INT_PIN: VDD
        CTRL_PIN: NSLEEPIN R F
        ON:
                R 1249.54
                I 4.75514e-12
                C 1.29872e-15
                IDSAT 0.000295299
        OFF:
                C 5.52379e-16
                VI 1.32
                N_VO_I 12
                0       5.73225e-12
                0.22    1.7404e-12
                0.44    9.09633e-13
                0.66    6.62416e-13
                0.88    4.41468e-13
                1.1     2.20941e-13
                1.3068  1.34016e-14
   }
}
POWER_UP:
        VI 1.32
        N_VO_R 12
        0       4470.19
        0.22    3893.33
        0.44    3292.92
        0.66    2670.07
        0.88    2054.4
        1.1     1566.49
        1.3068  1251.58
POWER_DOWN:
        VI 1.32
        N_VO_R 12
        0       2.30276e+11
        0.22    6.32039e+11
        0.44    9.67423e+11
        0.66    9.96353e+11
        0.88    9.96675e+11
        1.1     9.95739e+11
        1.3068  9.84957e+11
```

Figure 13. Switch model of single port power gating cell

3.3. Power Integrity Analysis Results

The power integrity analysis result under the on state mode of Static check and Dynamic check and under the Powerup state of low power is carried out respectively. The results are shown in tables 1 and 2.

Table 1. Power performance in Static and Dynamic mode

	Worst Instance Drop	Worst Wire Drop	Worst Switch Drop	Peak Battery Current
Static Check	63mV	41mV	57mV	\
Dynamic Check	113mV	79mV	69mV	254mA

Table 2. Formatting sections, subsections and sub subsections.

	Peak Battery Current	Peak Rampup Current	Worst Rampup time	Max Differential Voltage	Worst Switch Current	Max Noise Voltage
Low Power Check	261mA	76mA	80.58ns	2.78mV	0.243mA	113.8mV

4. Conclusion

Power integrity analysis of low-power SOC can find the weak points in low power design, quickly locate the problem, facilitate the designer to improve the program, optimize the design, shorten the design cycle at the same time, improve the success rate of the chip. By increasing the power gating cell number and modifying the layout of the power gating cell in the physical design, can decrease the rush current and power noise coupling, but will increase the rampup time. So the designer must make a tradeoff between the rush current and rampup time in the low power SOC design. Finally, the design of this paper is verified by tape out and chip test. Through the chip test, the low power function is correct and the performance meets the design requirements.

5. References

[1] Chunzhang Chen, Xia Ai, Guowei Wang, *Physical design of digital integrated circuits*. Beijing: Science Press, 2008
[2] *RedHawk User Manual[M]*, ANSYS.2013
[3] *Synopsys Low-Power Flow User Guide[M]*, SYNOPSYS .2011