Design of PID Coprocessing Module for CPT Atomic Clock Control SoC

Kun Huang, Yiru Fu, Jun Deng, Keliu Hu and Tao Zhang

Sichuan Institute of Solid-State Circuits, China Electronics Technology Group Corp, Chongqing 400060, P. R. China
Email: hkof11@126.com

Abstract. The CPT (Coherent Population Trapping) atomic clock is very small because there is no microwave cavity. However, the circuit control system is becoming the constraint of further miniaturization of CPT atomic clock. The CPT atomic clock control SoC integrates control related circuit into a single chip. There are many control loops in the CPT atomic clock which require PID (Proportional-Integral-Derivative) algorithm. CPU in this SoC can not afford the computation of PID algorithm. So a PID coprocessing module is integrated into this SoC. The PID algorithm can be decomposed into multiply-add operations. The coprocessing module mainly consists of a multiply-add module. Compared with SoC without PID coprocessing module, SoC with this module can reduce the time of calculating PID algorithm to 24.808%, and the area consumption increases by only 8.89%.

1. Introduction

Atomic clocks are widely used in navigation, communication, missile, satellite positioning, astronomical observation, geodesy, precision instrument calibration, power grid regulation and high-speed traffic management and other fields. And in the past 50 years, it has become an indispensable device [1]. With the miniaturization of electronic devices, the miniaturization of atomic clocks is inevitable. The discovery of Coherent Population Trapping (CPT) phenomenon [2, 3] by Aletta in 1976 makes it possible to miniaturize atomic clocks. CPT atomic clock is a new type of frequency standard [4] which is based on the quantum interference phenomenon produced by the interaction between atom and coherent light. Because there is no microwave cavity needed by the traditional atomic clock, CPT atomic clock eliminates the cavity pulling shift effect on frequency standard, and is the only atomic clock that can be miniaturized in engineering at present. The US Kernco company successfully developed a chip scale CPT atomic clock in 2004.

The circuit control system of traditional CPT atomic clock usually includes ADC, DAC, FPGA, MCU and other circuits [5], but this discrete structure is difficult to further reduce the volume and power consumption of CPT atomic clock. Atomic clock control SoC integrates these circuits into one chip, which can reduce the area and power dissipation very well. After the first tape-out of the CPT atomic clock control SoC, the power and area of the circuit control system were reduced. The actual use found that the SoC can not precisely control the CPT atomic clock system. In the control system of CPT atomic clock, the temperature signal, laser demodulation signal and microwave demodulation signal need to be controlled by PID algorithm. There are many loops controlled by PID algorithm, and floating-point number is used in PID algorithm. CPU in this SoC has no floating-point unit, the PID operation is slow. A PID coprocessing module is added in the SoC to speed up the PID algorithm.

The PID algorithm can be decomposed into multiply-add operations [6]. The coprocessor is designed to be a multiply-add module and a bus interface module. The rest of the PID algorithm is

implemented by CPU. PID algorithm in this SoC is a process of software and hardware collaboration. A technology with reduced latency described in [7] is used in the multiply-add module. Simulation results show that the time of calculating PID algorithm is reduced to 24.808% comparing with anSoC with no coprocessing module, and the area consumption only increases by only 8.89%.

2. CPT Atomic Clock Control SoC

The system block diagram of CPT atomic clock is shown in Figure 1. The CPT atomic clock consists of two parts, the physical system and the circuit system. Physical systems include Vertical Cavity Surface Emitting Laser (VCSEL), wave plates, 87Rb vapour cell, etc. The circuit system includes amplifying circuit, electronic control system, temperature compensated crystal oscillator (TCXO), microwave source and Bias Tee etc.

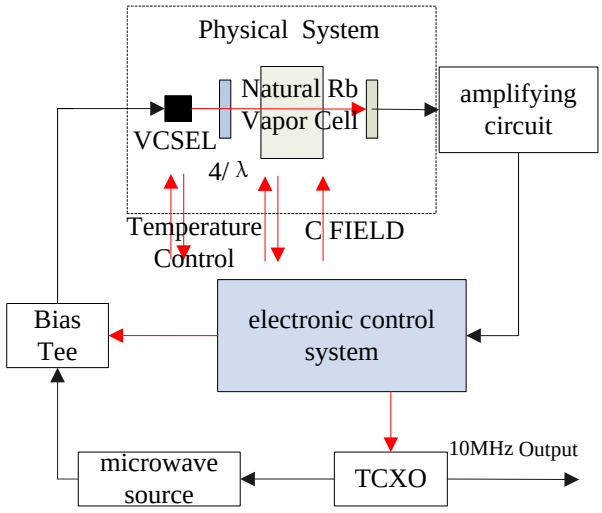

Figure 1. The system block diagram of CPT atomic clock.

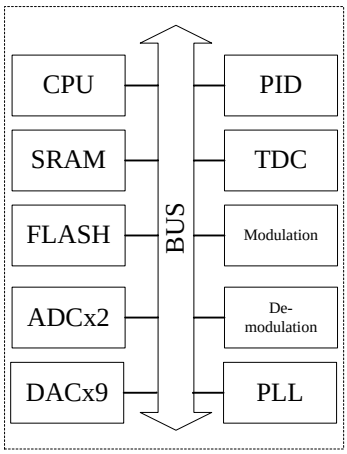

Figure 2. Atomic clock control SoC.

Atomic clock control SoC integrates the electronic control system into a single chip with hybrid SoC technology. It reduces the area and power consumption of the electronic control system, and improves its reliability.

As shown in Figure 2, this SoC integrates a Cortex-M0 CPU, 32k-Byte SRAM, FLASH, ADC, DAC, TDC, modulation module, demodulation module and PID coprocessing module. Cortex-M0 is selected for its excellent power performance. There are two ADC, one for temperature acquisition and the other for modulation signal acquisition. There are nine DAC, four for temperature control, four for modulation signal generation and one for C field control. The modulation module is used to generate signals needed by the laser frequency stabilization loop and the microwave frequency locked loop. The demodulation module is used to demodulate the corresponding signal. Four loops need to be controlled by the PID algorithm. They are VCSEL temperature loop, 87Rb vapor cell temperature loop, laser frequency stabilization loop and microwave frequency locked loop. The PID algorithm uses floating point numbers. For this CPU, the overall amount of computation is too large. To reduce the computation load, a PID coprocessing module is adopted.

3. PID Algorithm

The schematic diagram of the PID controller [6] is shown in Figure 3. The PID controller is linear controller. The error signal e(t) is the difference between reference input $R_{in}(t)$ and actual output $Y_{out}(t)$. The proportional, integral and derivative signals are summed to form the control signal u(t) applied to the plant model.

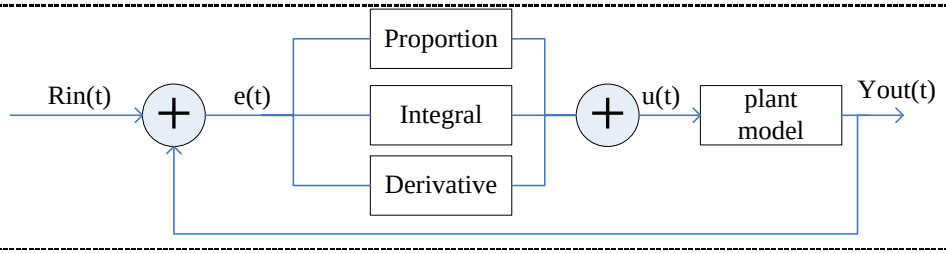

Figure 3. A typical PID control system

A mathematical description of the PID controller is,

$$u(t) = K_p[e(t) + \frac{1}{T_i}\int e(t)dt + T_d\frac{de(t)}{dt}] \tag{1}$$

Where u(t) is the control signal to the plant model, e(t) is the error signal, K_p is proportional gain, T_i is integral time constant and T_d is derivative time constant.

Digital system is not a continuous system. The integral and differential terms in formula (1) must be discretized. The discretized PID control expression is

$$u(k) = K_p[e_k + \frac{T}{T_i}\sum_{j=1}^{k} e_j + \frac{T_d}{t}(e_k - e_{k-1})] + u_0 \tag{2}$$

$$u(k) = K_p e_k + K_i\sum_{j=1}^{k} e_j + K_d(e_k - e_{k-1}) + u_0 \tag{3}$$

Where u(k) is the k-th control signal, e(k) is the k-th sampling error, K_i is integral coefficient, $K_i=K_p*T/T_i$, K_d is derivative coefficient, $K_d=K_p*T_d/T$.

From formula (3), the (k-1)-th sampling u(k-1) is

$$u(k-1) = K_p e_{k-1} + K_i\sum_{j=1}^{k-1} e_j + K_d(e_{k-1} - e_{k-2}) + u_0 \tag{4}$$

So Δu is

$$\Delta u = u(k) - u(k-1) = Ae_k + Be_{k-1} + Ce_{k-2} \tag{5}$$

Where $A = K_p+K_i+K_d$, $B = -K_p-2K_d$, $C = K_d$.

Compared with the conventional PID control algorithm, the incremental PID control algorithm has the following advantages: (1) Cumulative error is small. (2) No cumulative computation. (3) Small amount of calculation. In view of above advantages, this incremental PID algorithm is used to design the coprocessing module.

4. Coprocessing Module Design

From formula (5), the incremental PID control algorithm can be decomposed into simple multiply-add operations.

$$u(k) = \underrightarrow{u(k-1) + Ae_k + Be_{k-1} + Ce_{k-2}} \tag{6}$$

Through three multiply-add operations, the control signal u(k) can be easily calculated as shown in formula (6). The implement of the PID algorithm is that CPU controls the whole process and the coprocessing module performs multiply-add operations.

The coprocessing module includes bus interface and multiply-add module. In 2004, T.Lang put forward a floating point multiply add method with reduced latency [7]. As shown in figure 4, the main improvement is to put the normalization shifter ahead of addition, and combine addition and rounding. At present, most manufacturers adopt this technology in design and production. The design of coprecessing module also refers to this mothod.

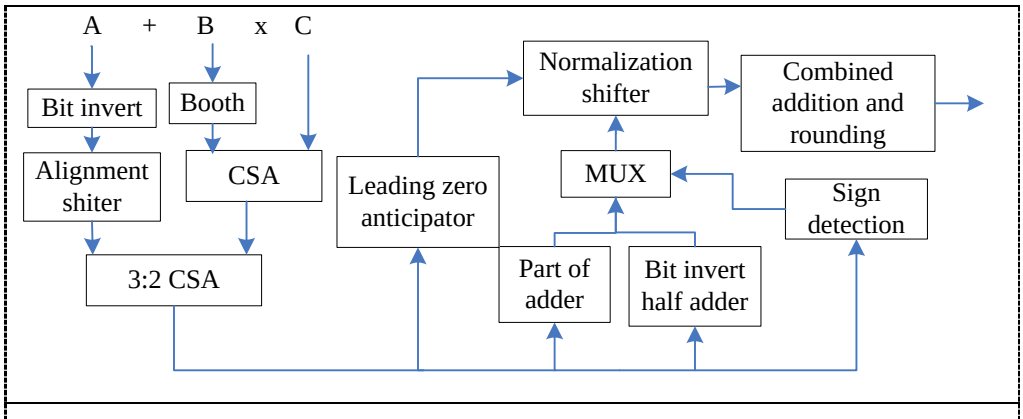

Figure 4. Scheme of Multiply-Add Operation

5. Simulation Results

To evaluate this coprocessing module, 3 versions of the atomic clock control SoC were proposed. A) SoC without coprocesssing module. B) SoC with this coprocessing module. C) SoC with a full PID coprocessing module. This full PID coprocessing module has completed all the operations in formula (6). This means that the PID algorithm is all implemented by hardware. CPU does not participate in the PID computation. VCS (an RTL simulator) is used to simulate a single PID computation time. Design-Compiler (synthesis tool) is used to evaluate the total area of SoC. And Power-Artist (power evaluator) is used to estimate the power consumption during a single PID computation. The SoC is running at 30MHz.

Table 1. Time, Area, Power and Energy of SoC.

	PID Computation Time	Total Cell Area	Power	Energy
SoC A	12500ns	645344	15.984mW	1.998e-7 J
SoC B	3101ns	702716	18.19mW	5.641e-8 J
SoC C	1251ns	1006577	21.085mW	2.638e-8 J

As shown in table 1, the PID computation time of SoC B is 24.808% of SoC A, and the PID computation time of SoC C is 10.008% of SoC A. Compare with SoC A, total cell area of SoC B has increased by 8.89%, power of SoC B has increased by 13.8%, total cell area of SoC C has increased by 55.98%, power of SoC C has increased by 31.91%. Although the power consumption of SoC B, C is higher than that of SoC A, the computation time of SoC B, C is shorter than SoC A, so the total energy of SoC B, C is less than that of SoC A. The energy of SoC B is 28.23% of SoC A. The energy of SoC C is 13.2% of SoC A. Although C has the shortest computation time, its area is too large to be accepted.

6. Conclusions

There are four loops in the CPT clock which need to be controlled by the PID algorithm, and the amount of computation required exceeds the processing capacity of the CPU. So a PID coprocessor module is added to assist the computation. If the PID algorithm is all implemented by hardware, the area is increased by 55.98%, which is unacceptable. Split the PID algorithm into 3 multiplicative operations. The coprocessing module completes the multiply-add operation, and the CPU completes

the rest. The simulation results show that the area of this method is only increased by 8.89%, and the computing time is reduced to 24.808% comparing with SoC without coprocessing module.

7. References

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