Research on Reconfigurable Instrument Technology of Portable Test System of Missiles

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Abstract. To solve the problem of low test efficiency and weak maneuverability of missiles, the reconfigurable instrument technology of missiles' portable test system is researched. In this paper, the realization plan based on PXI bus is proposed and key links of resource research is analyzed. Based on FPGA+DSP construction, the hardware circuit of the reconfigurable instrument is designed and the logic files are compiled. The research on the reconfigurable instrument technology can relieve the problem of low test efficiency and weak maneuverability of missiles effectively, and provide basis for further research of missiles' portable test systems.

1. Introduction

As the important maintenance equipment, automatic test system (ATS) takes charge of the function test and fault diagnosis of missiles in the whole life cycle, which is the guarantee for missiles to keep operational effectiveness normally, and plays a vital role in the formation and improvement of missiles' fighting capacity [1]. Nevertheless, the maintenance mode of missile ATE still exists many issues such as big scale test equipment, complexed maintenance procedure, low test efficiency, which has severely influence the maneuverability and flexibility of automatic test systems. To improve the maintenance ability of weapon equipment and satisfy the requirement of quick transfer for army, the problem of dig volume and weight for ATS is needed to be solved.

In recent years, the reconfigurable instrument technology has a rocketing development all of world and has a wide application in the ATS field [2-5]. Therefore, do research on the reconfigurable instrument technology is a portable way to improve the utilization ratio of instrument resources and achieve the portable test system of missiles.

In this paper, the realization plan based on PXI bus is proposed and key links of resource research is analyzed. Based on FPGA+DSP construction, the hardware circuit of the reconfigurable instrument is designed and the logic files are compiled. The research on the reconfigurable instrument technology can relieve the problem of low test efficiency and weak maneuverability of missiles effectively, and provide basis for further research of missiles' portable test systems.

2. Analysis of the reconfigurable instrument resource research

In general, ATS usually uses the "pile up mode" test method. Although this method can improve the collective effectiveness of all of test systems, the function redundancy is severe. And for specific test system, to achieve test requirements of UUT (Unite Under Test), the system will integrate all of functions, which results in the problem of big weight and volume. To solve these problems, there are

several keys must be taken into consideration. On the one hand, the realization of miniaturization and portability. In domestic, a set of automatic test system of missile is composed of computer, stimulation subsystem, switch subsystem, power subsystem, output equipment, common test port, test adapter and test accessory. As is shown in Figure 1. The whole system has a big scale and weak maneuverability. To reduce the volume and weight of the system, we should pay attention to big scale components like the test adapter and the switch subsystem. On the other hand, the choice of test bus. Test bus is the core of the whole ATS, the bus performance such as data throughput, transmission rate can affect the test accuracy of the system. In the test field, there are all kinds of test bus such as GPIB, VXI, PXI, LXI. Comparing to the other test bus, the PXI bus has advantages of high speed transmission rate and reliability, which is suitable to be selected as the test bus in the construction of the portable test system of missile.

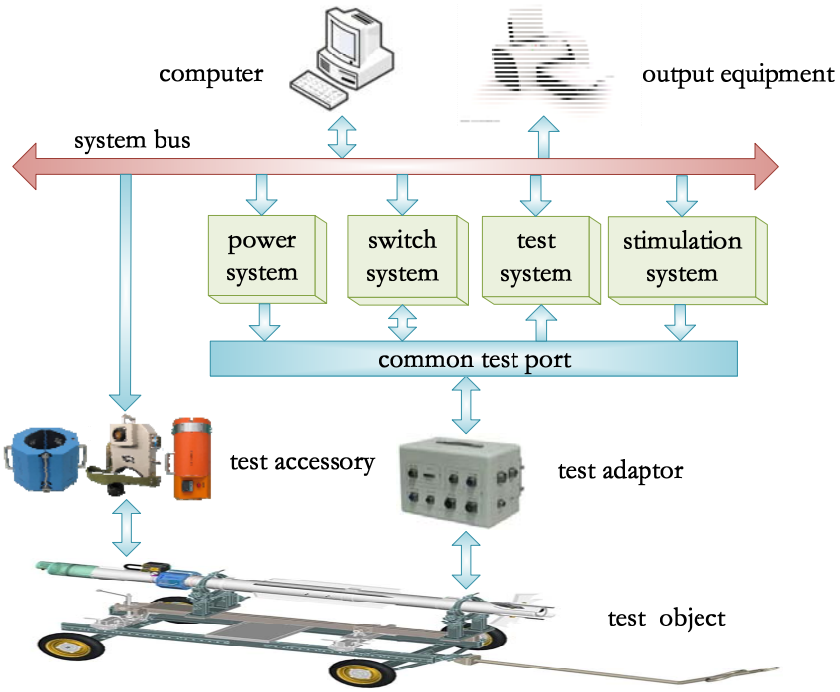

Figure 1. The composition of classic military ATS

3. The design of reconfigurable instrument resource

3.1. Overall design scheme

The whole system is composed of embedded computer, reconfigurable module and functional circuit module. As is shown in Figure 2. As the hardware basis of the reconfigurable function, the reconfigurable module contains FPGA and its configuration circuit, DSP, PXI port circuit and power transformation circuit [6-7]. The functional circuit module is composed of digital multimeter, AD, DA and counter. In the overall design scheme, the reconfigurable module and the functional circuit module are divided in order that when different PXI reconfigurable instrument needed to be design, users just need to design the different functional circuit board card according to different test requirements rather than redesign the reconfigurable module, which can improve the exploitation effectiveness and reduce cost.

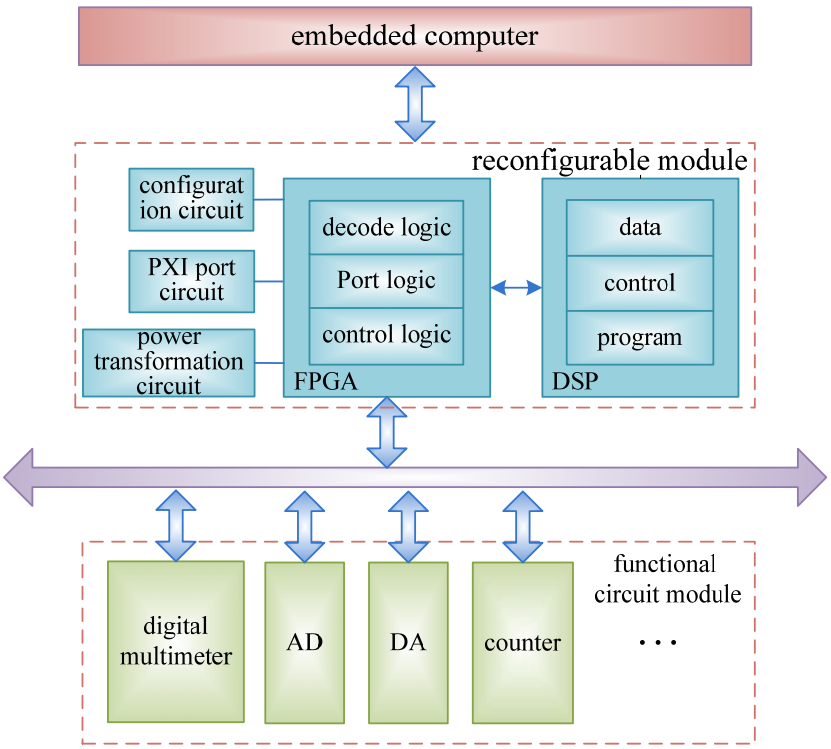

Figure 2. The overall design scheme of reconfigurable instrument

3.2. Hardware design

The main control module is shown in the Figure 3. Flash is the DSP memory used to store program. SDRAM is designed to expand DSP capacity and store data during the program running. EPCS is the serial memory designed to store the configuration files. DSP is used to realize the communication with upper computer, test data processing, control the read and write of FPGA reconfigurable files. FPGA is used to control the functional circuit module, realizing the interaction of test data and control command between FPGA and DSP by CPLD.

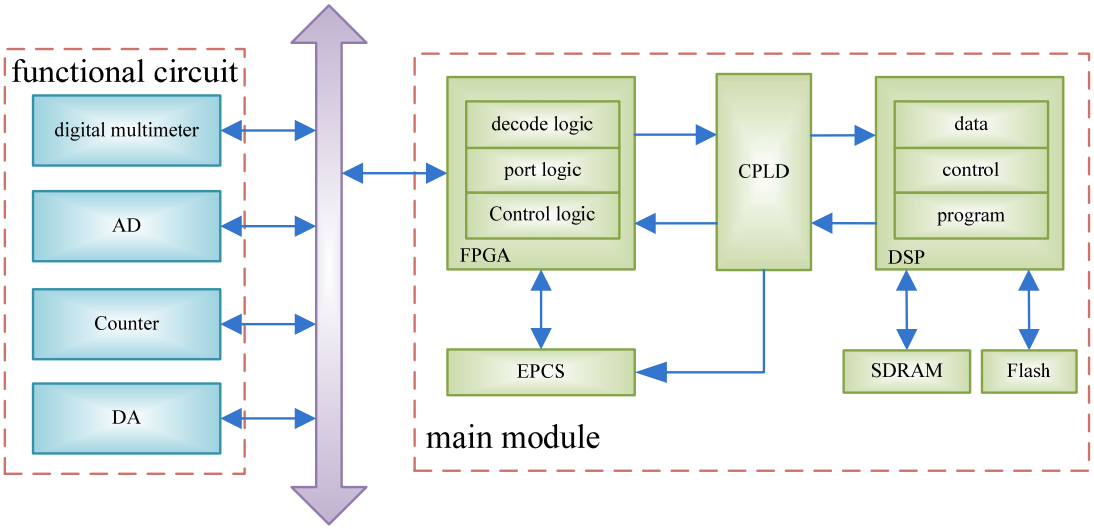

Figure 3. The main control module

TMS320C6201 is selected as the DSP chip. The connection between EMIF ports and SDRAM is shown in Figure 4. The 32bit data line of TMS320C6201 connect with two SDRAM chips directly. For TMS320C6201, the different memory unit is selected by enable signal BE [3:0]. The enable signal of SDRAM chip 1 is BE3 and BE2, and the enable signal of SDRAM chip 2 is BE0 and BE1. The connection between TMS320C6201 and Flash memory is shown in Figure 5. EMIF ports EA [21:2] of TMS320C6201connect with A [18:0] of MBM29LV800BA directly. EMIF ports ED [7:0] connect with DQ [7:0] of Flash directly.

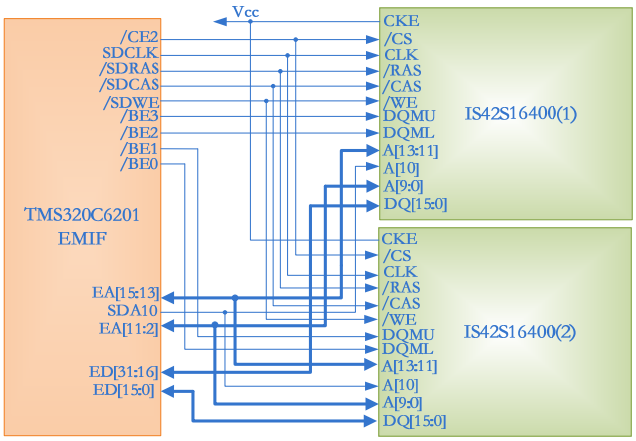

Figure 4. The connection between EMIF ports and SDRAM

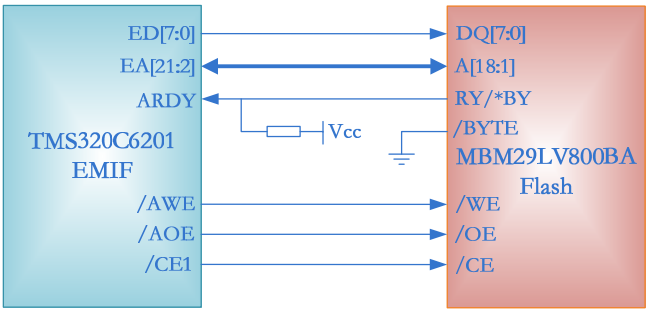

Figure 5. The connection between TMS320C6201 and Flash memory

Stable and reliable power supply unit is the importance insurance for the main control and functional circuit modules to work normally. DSP chip TMS320C6201 needs two kinds of power containing IO port power and chip inner power. The former requires 3.3V and the latter requires 2.5V. FPGA chip XC7A200T-2FBG676C needs three kinds of power containing chip inner power 1.0V, IO port voltage 3.3V and output drive voltage 2.5V. Integrating the other power supply requirements of functional circuit modules, the power finally contains ±12V, ±5V, 3.3V, 2.5V, 1.0V. As is shown in the Figure 6.

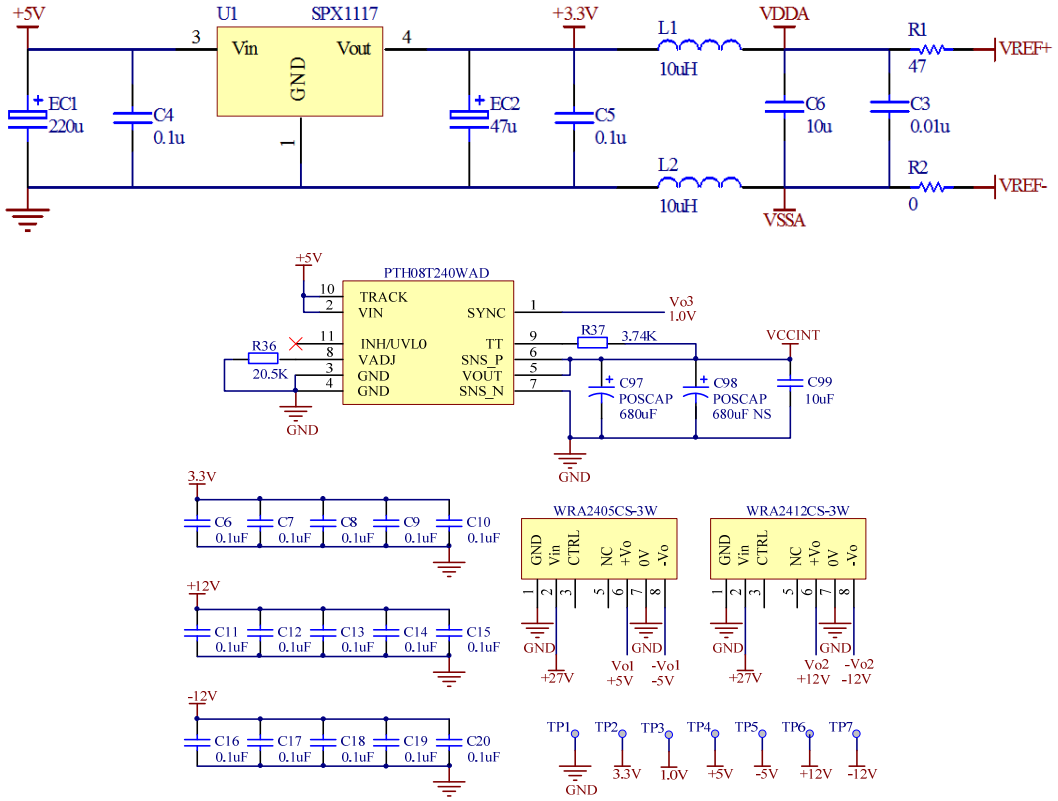

Figure 6. The power transmission circuit

3.3. *The reconfigurable logical files*

The reconfigurable instrument board cards integrate an ocean of test resources. In this paper, FPGA realizes the channel switch, functional circuit choice, read and write of register information according to the control command of DSP. The reconfigurable logic of FPGA analyzed by CPLD, which download new time and configuration data into EPCS. Then FPGA downloads new configuration files from EPCS and realizes the reconfigurable logic. In the design of the reconfigurable instrument, FPGA reconfigurable logics and reconfigurable channels realized based on Avalon bus. FPGA reconfigurable logical files are compiled by VHDL language, and BSF reconfigurable files are produced by QuartusII software. The reconfigurable files of digital multimeter, AD, DA and counter are shown in the Figure 7.

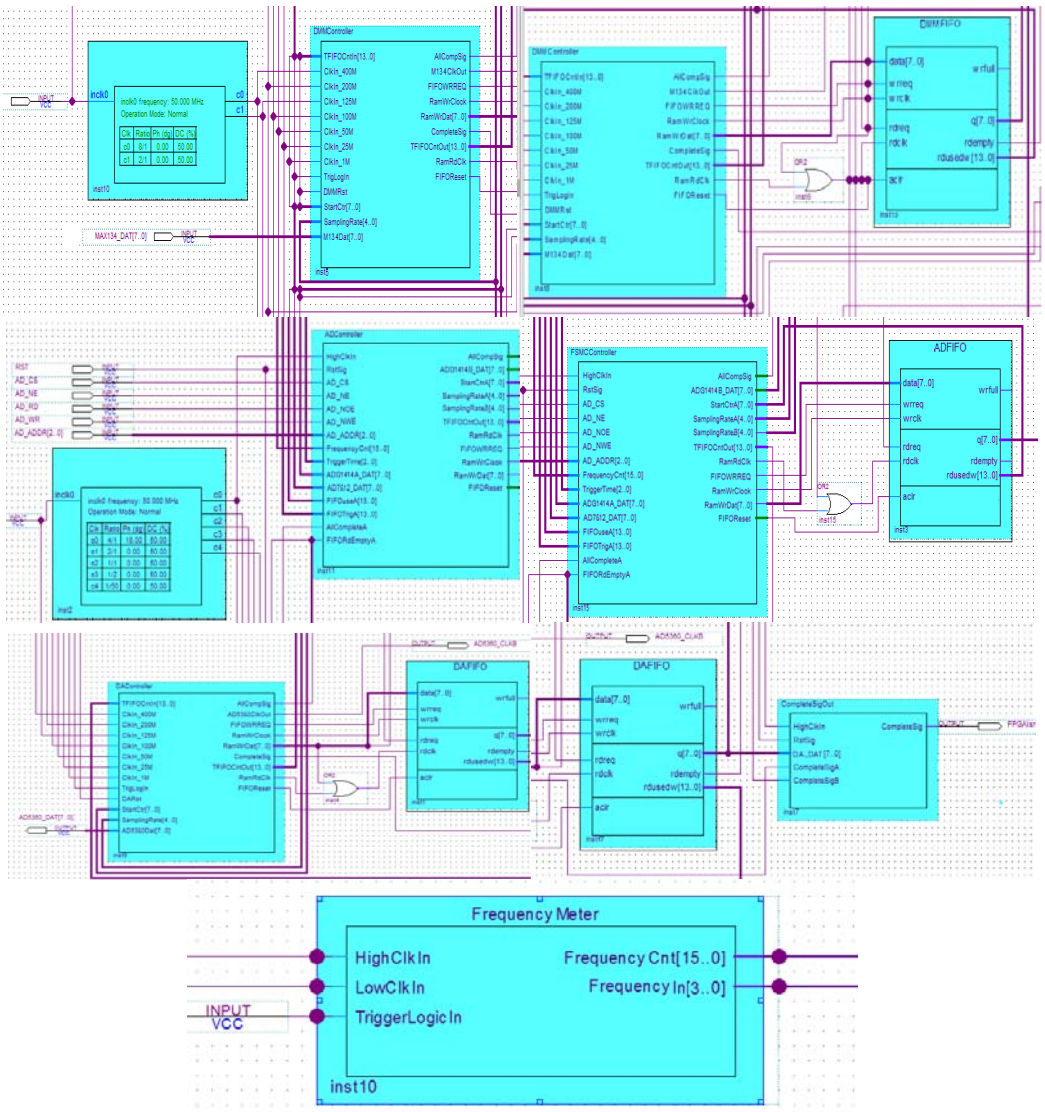

Figure 7. The reconfigurable files

4. Conclusion

Aiming at the problems that the FMECA of complexed weapon equipment is difficult to be quantified and the indicators are diverse, in this paper, a method to describe the fault criticality of missiles based on multi-level fuzzy comprehensive evaluation theory is proposed. We take a kind of complexed weapon equipment, a television guidance missile, as an example to establish factor sets, evaluation sets, weight sets, comprehensive evaluation based on multi-level fuzzy theory. Furthermore, a comprehensive evaluation indicator is proposed to quantitatively describe the fault criticality of missiles, which can provide basis for reliability research of the missile.

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