

Application of Cache Control Circuit in Radar Signal Replay System

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Abstract. This article studies the design ideas of the peripheral circuits related to radar signal playback. Mainly cache module and clock circuit. These peripheral circuits provide control logic and operating clock for the radar signal playback module. This design mainly focuses on DMA transmission, radar data extraction, and playback.

1. Introduction

The unit that performs the radar signal playback function in the system is a pulse radar playback board. The subject is designed to implement radar data extraction, radar signal playback, and peripheral circuit control by designing the FPGA internal ASIC circuit on the playback board. The entire circuit design is based on VHDL. The digital circuit design method, this part of the study is the core content and difficulties.

2. Division of system logic functions

This article mainly analyzes the pulse radar playback board from the perspective of logic function. The CPCI interface circuit mainly completes the task of reading radar data from the system memory via the PCI bus. This article uses a design method based on the IP core to design it. This part will be discussed in detail in Chapter 5, and the radar signal playback module. The three parts of the clock control circuit and the cache control circuit together constitute the system playback logic circuit, as shown in Figure 1.



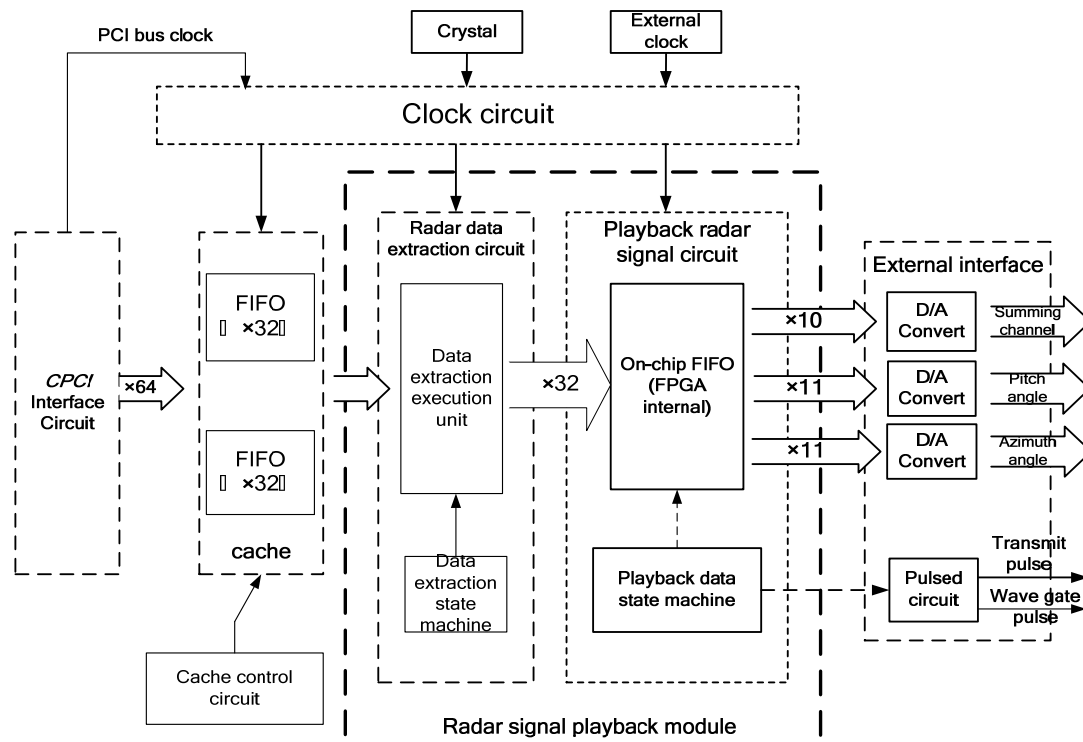


Figure 1. System logic circuit diagram

3. Cache Module Control

3.1. Read-write enable control

The PCI interface controller completes the data burst transmission through the DMA operation. After the system starts the playback operation, the PCI device will complete a DMA transfer first; write enough radar data into the high-speed buffer, and then the radar signal playback circuit. Whenever the "almost empty" flag of the cache module is activated, it indicates that the data in the cache module is about to be read, and the PCI host device will burst the next DMA transfer. This process will be performed in a loop until the data in the echo file is completely played back or the user interrupts the playback.

According to the above DMA transfer control flow, we know that the data written to the cache module is read from the bus by the PCI interface controller. Therefore, the write enable side of the FIFO is controlled based on the start timing of the DMA: as long as the PCI interface controller is performing a DMA transfer, the write enable of the FIFO is activated; when there is no data transfer on the LOCAL side of the PCI interface controller The FIFO write enable is inactive.

The read enable of the cache module is associated with the logic of the data extraction state machine and two situations need to be considered.

In the first case, the data extraction state machine extracts radar data in the first main pulse period in the radar echo file. When the user initiates playback, the system software generates a read and write control circuit that plays back the start signal and sends it to the cache module through the PCI bus. When the read/write control circuit detects this signal and judges that the "almost full" flag of the cache module is valid, the read enable of the cache module is activated, so that the data extraction state machine starts to read data from the cache module. If the first frame data extracted by the data extraction state machine has only one echo or no echo radar information in the main pulse period, the read/write control circuit cancels reading when the data extraction state machine extracts the header information and the frame data. Enabling the valid state; if the first frame of data has two echoes of

radar information in the main pulse period, the read/write control circuit needs to wait for the first information and the first two frames of data to be extracted before canceling the read enable.

In the second case, the data extraction state machine extracts radar data during and after the second main pulse period. Through analysis, the data extraction is always one frame ahead of the playback of the radar signal (only one echo or no echo in the main pulse period) or two frames (two echoes in the main pulse period). Can provide the necessary data for radar signal playback in time. According to this principle, we discuss in three situations:

(a). There is no echo in the main pulse period. Since no other pulse can be used as the trigger signal for the data extraction state machine after the synchronization pulse at this time, when the data playback state machine starts playing back the first synchronization pulse in the current main pulse cycle, the data extraction state machine starts to extract the next frame. The data, of course, is to activate the read enable of the cache module. When all radar data is extracted in the next main pulse cycle, the active state of the read enable terminal is cancelled;

(b). One echo in the main pulse period. In this case, when the data playback state machine starts playing back the IF echo signal, the data extraction state machine starts to start extracting the next frame of data. At this time, the read/write circuit activates the read enable function; when the data extraction state machine After the extraction of all radar data in the next main pulse period, the read enable is invalid;

(c). Two echoes within the main pulse period. This happens in the radar's "separation of blindness" and "disturbed distance" working states. When the data playback state machine starts playing back the second echo in the main pulse cycle, the read enable is effective, so that the data extraction state machine begins to extract the next frame of data. Since there are two echoes in this cycle, there must be only one echo or no echo in the next main pulse cycle. Therefore, when the next frame data is extracted, the read enable is invalid.

3.2. Full-air flag setting

The system starts DMA according to the state of the cache module's PAE. The average time for the radar signal playback circuit to read, process, and play back radar data within one main pulse period is $1/585 \text{ Hz} \approx 1.7 \text{ ms}$. In addition, due to non-real-time Windows operating system, the time interval for the system to allocate time slices for each task thread is up to about 20ms, that is, when the cache module is just in the "almost empty" state, the operating system may also be No time slice is allocated for the system control software, so that the next DMA cannot be started and the bus will not transmit data to the cache module. This period of time is about 20ms. Therefore, in order to ensure the continuity of the playback timing, the PAE must be selected so that the radar signal playback circuit does not read the cache module empty within 20 ms. It can be calculated that the size of a frame of data is 0.0305 MB , and the number of radar data frames that the radar signal playback circuit can process within 20ms is $N_{\text{frame}} = 20 \text{ ms} / 1.7 \text{ ms} \approx 12$. In addition, when there are two echoes within one main pulse cycle, the radar information in the main pulse cycle is using two frames of data for storage; the "nearly empty" flag of the cache module is set at a position where it can hold 24 frames, that is, $24 \times 0.0305 \text{ MB} \approx 0.8496 \text{ MB}$. For ease of calculation, the circuit takes a position of 1MB as a PAE. Since the cache module has a capacity of 4 MB, the amount of data transferred by one DMA is selected as $K_{\text{DMA}} = 4 \text{ MB} - 1 \text{ MB} = 3 \text{ MB}$, and the "almost full" flag of the cache module is set at 3 MB.

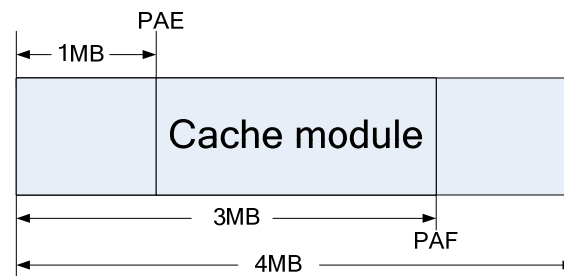


Figure 2. PAE and PAF selection

4. Distribution of clock circuits

There are three main clock sources on the board: the external clock interface, the on-board 200MHz crystal oscillator, and the 66MHz clock provided on the PCI bus. The external clock and 200MHz crystal oscillator are the system clocks, but they cannot be used as the clock source on the board at the same time. Users can use the clock selection circuit of the playback board to dynamically select one of them as the system clock. The 200MHz crystal oscillator is mainly used in system debugging. When the task is performed, the system mainly uses the external clock as the system clock.

There are 12 PLLs in Stratix II, among them there are four enhanced PLLs, and they are PLL5, PLL6, PLL11 and PLL12 respectively. The playback board's clock design uses three of the enhanced PLLs.

The CLK0 is a 66 MHz clock provided on the PCI bus, which is divided into two 66 MHz clocks by the PLL 12, all the way to provide a data synchronization clock for the PCI interface circuit, and the other way to provide a write clock for the cache module. Since the PCI interface controller reads the 66 MHz data on the bus and sends the data directly to the cache module, the process should be completed in synchronization with the same clock. Therefore, the two clocks require the same phase. CLK1 and CLK2 are obtained by an external clock or a 200MHz crystal oscillator through a clock selection splitter, and their clock frequency is 200MHz. CLK1 is divided into two 200MHz clocks through PLL6 as the read clock of the cache module and the data clock of the data extraction circuit, respectively. Since the data is read from the external FIFO into the FPGA, it is directly sent to the data extraction circuit for processing. Therefore, the frequency and phase of the two clocks are the same. CLK2 is divided into two 200MHz clocks through PLL5 as the data clock of the data playback circuit and the reference clock of AD9776. The frequency and phase of this clock are also the same. Here is a point: Since the delay information in the echo file is quantized by the 200MHz clock, the read clock of the cache module uses 200MHz. The 200 MHz read clock that is larger than 66 MHz is also considered here to avoid situations where the FIFO will be written full of lost data.

In Figure 3, CLK_SEL is the clock selection signal. When CLK_SEL is high, the external clock is selected as the system clock source. When CLK_SEL is low, the 200MHz crystal oscillator is selected as the system clock source. CLK_EN is the clock selection circuit enable terminal.

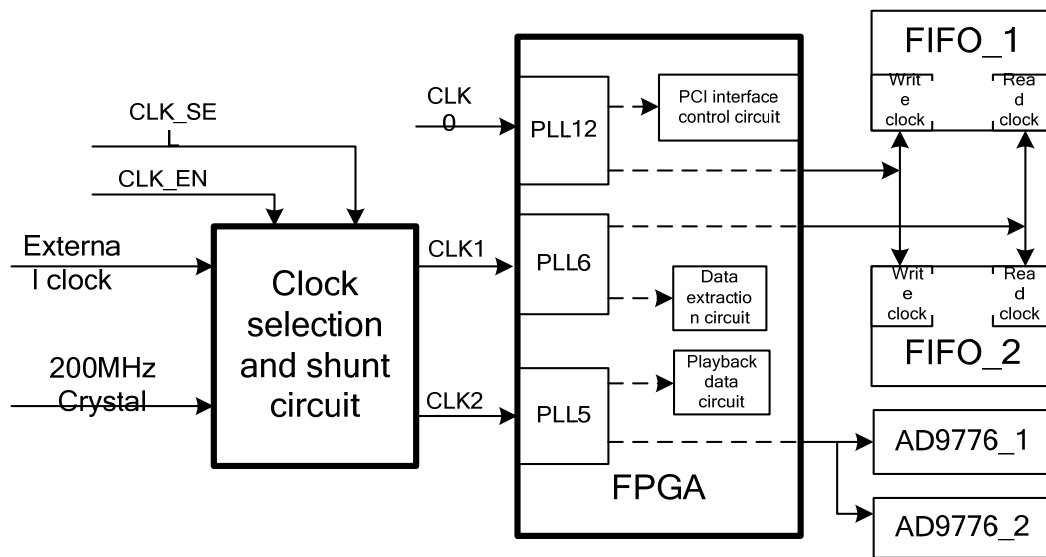


Figure 3. System clock circuit schematic

5. Summary

This paper mainly studies the design ideas of the peripheral circuits related to radar signal playback. From the cache module and the clock circuit are discussed in two aspects. The circuit is researched and designed from DMA transmission, radar data extraction and playback.

References

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