

Integration of hardware and software tools for VLSI SoC class design support

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Abstract. Design of radio-electronic equipment is connected with formation of the heterogeneous design environment that contains hard and soft solutions from different company. The heterogeneous design environment generates the set of problems. Most of them does not have unified information solutions, in particular, complexity of operating decisions- making and data transmission of design information. One of the well-known way to solve the problem is the integration and formation of unified information environment. The paper presents the method of integration of heterogeneous hardware and software design support tools of the radio-electronic equipment in the unified information environment. As an example, the stage of system design of the digital goniometric satellite navigation receiver using the Global Navigation Satellite System GLONASS is presented. For information exchange between elements of the information environment the transformer to the uniform data format on the basis of the XML language is used. The implementation of the automated workstation for the GNSS receiver design and testing is also considered.

1. Introduction

Production of the modern radio-electronic equipment is linked to continuous increase in the complexity of designed devices, strengthening the requirements for the technological process of semiconductor foundry and evolution of production methods and approaches. In designing of complex microelectronic systems project organizations and R&D centers widely apply such methodologies as the Silicon-on-a-Chip (SoC) and the Network-on-a-Chip (NoC). They focus on the pre-designed circuit cores (soft microprocessor cores, memory units, digital amplifiers, filters, etc.), that called Intellectual Property (IP) cores [1–3]. The concrete CAD (Computer-Aided Design) or CAPP (Computer-Aided Process Planning) system is used at every step of designing microelectronic devices. Based on this approach the heterogeneous information environment is formed, which influences efficiency of the design process. As the result, the heterogeneous information environment gives rise to a number of problems:

- There is not of a complete picture of the design process;
- It is impossible to analyze of the whole set of project information;
- It is difficult to make quick design decisions.

In radio-electronics production the following factors must be considered: frequent change of the nomenclature of products, release small-scale of a batch of products, frequently replacing each other, emergence of unscheduled production orders. In such conditions the heterogeneous design environment is characterized by wide range of the CAD and CAPP systems and other application programs from different company. It needs to be revised for purposes of effectiveness in the application information solutions.



One of the well-known way to solve the problem is the integration and formation of unified information environment. For this purpose hardware and software support tools combine into the single complex of uniform solutions using the unified format for data exchange or the universal format of Electronic Design Document (EDD) and formation of the Integrated Information Environment (IIE) [4, 5]. This approach already at the early design stages provides the formalization of interaction methods and protocols that significantly increases efficiency of information processing and facilitates decision-making during the design cycle.

2. Aim of the research

The aim of the work is increasing the quality of design process and tests of the radio-electronic equipment in production of Very-Large-Scale Integrated Circuits (VLSI) of the SoC class. This will be achieved by integration hardware and software used on various stages of the design process into the IIE structure.

The steps are presented below:

1. Carry out a research of all SoC design stages;
2. Formulate requirements to the uniform data exchange format according to used software and hardware;
3. Develop the necessary support tools for design tools integration into the IIE.

It should be noted that already known approaches in the field of the IIS organization are successfully applied for creation of flexible manufacturing systems in various fields of machine building, especially for the automated production management systems. However, at the same time, unified well-tested approaches, methods and recommendations that completely satisfied the needs of project organizations by design and small-scale production of the complex radio-electronic equipment are not known [6–9].

3. Integration of hardware and software design tools for VLSI SoC class

Consider the integration of software and hardware used in the design process of the digital receiver for the Global Navigation Satellite Systems GLONASS (GNSS receiver) with the measurement of movements around the yaw axis (Tait-Bryan angles). Such devices are intended with navigation signals (NS) from two or more navigation spacecraft (NSC, up to six), implemented on the basis of custom or semi-custom integrated circuits as the Uncommitted Logic Arrays (ULC) or the Programmable Logic Devices (PLD).

From the point of view on the design and testing process, the GNSS receiver can be represented as two components (figure 1):

- program simulator of navigation signals from spacecraft (1);
- structural units of the GNSS receiver (2).

The representation of the GNSS receiver includes following components [10, 11]:

- G_{1-6} — blocks of generation of information and frequency components according with the navigation signal from the spacecraft;
- SMA_{1-6} — blocks the navigation signal modulation and amplification onboard the spacecraft;
- PS_{1-6} — blocks of phase shift input according with the navigation signal and characteristics of the signal propagation medium;
- SCS — satellite constellation selector;
- NSR_{L1}, NSR_{L2} — navigation signal receivers for L1 and L2 frequencies;
- RPA — block of resolving phases ambiguity for the navigation signal;
- PSC — block of phase shifts computation for the navigation signal;
- UO — block for solving the system of equations for determination of movement values around yaw axis of a vehicle based on the computational values of the navigation signal phase shifts.

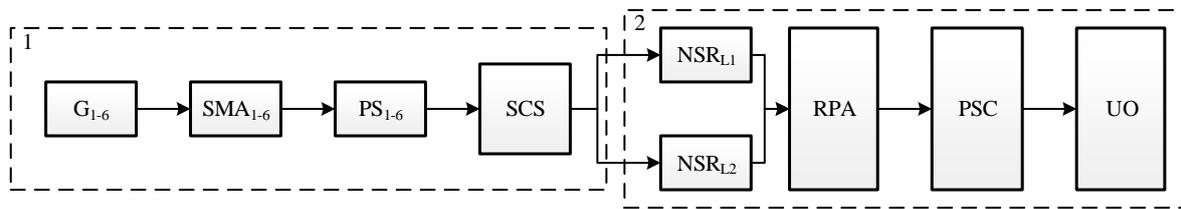


Figure 1. Schematic structure of the GNSS receiver structural organization.

In general, the process of SoC design includes the following stages: design on the system level, functional design, logic design, topological design, stage of verification and preparation for production [12] (figure 2). Consider the example of integration design tools for the design stage on the System Level (SL) of the GNSS receiver. Let’s make allowance that the integration methods for remaining stages of the whole design cycle are similar.

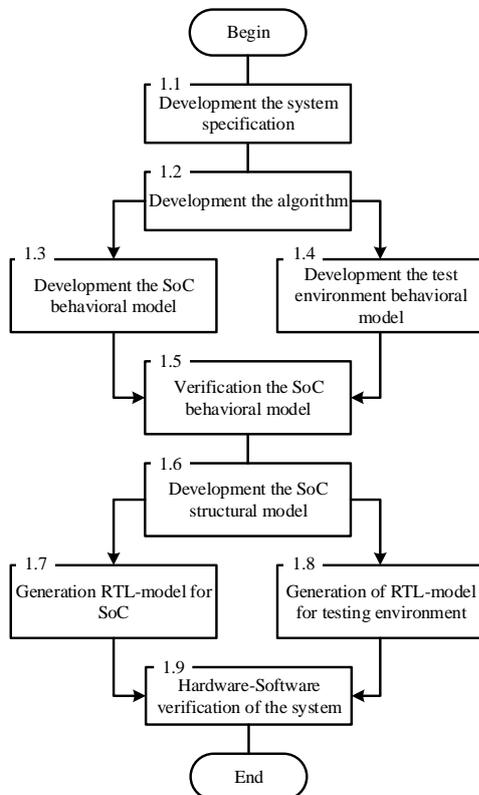


Figure 2. Block diagram for the System Level stage of the SoC design cycle.

The development of the SoC at the SL stage begins with requirement analysis and development of the system specification (1.1). The algorithm of the SoC functioning on the level of the mathematical description is developed on the basis of the system specification (1.2). On the basis of the algorithm the behavioral model of the SoC that reflects general principles of the system functioning is developed (1.3). The additional behavioral model of the testing environment is developed for more effective verification of the SoC behavioral model (1.4). After that the behavioral model of the SoC is verified (1.5). The structural model of the system on the functional block level is developed on the basis of the system model (1.6). This type of model makes possible to generate the code description of functional blocks into the description on the Register-Transferring Level (RTL) using standard hardware description languages like VHDL or Verilog HDL (1.7). The description of the testing environment is similarly generated (1.8). The received description of the structural model undergoes the procedure of hardware-software verification using hardware development kits constructed on the basis of PLD chips (1.9).

Electronic design documents created during the System Level stage can be presented in various formats depending on the software (table 1) used on the particular step.

Table 1. The list of software, used during the System Level stage.

Number of step	Software	Document format
1.1	MS Word	.doc,.docx
1.2	MATLAB, Maple, Enterprise Architect	.m,.ns,.msw,.eap
1.3	MATLAB, Simulink: Communications System	.m,.slx
1.4	Toolbox; DSP System Toolbox.	
1.5	MATLAB, Simulink: Simulink Control Design; Simulink Design Optimization; Simulink Design Verifier.	.html
1.6	MATLAB, Simulink: HDL Coder; Communications System Toolbox HDL Support.	.m,.slx
1.7	MATLAB, Simulink: HDL Workflow Advisor;	.m,.slx,.vhd,.html
1.8	HDL Code Generation.	
1.9	LabVIEW, ISE Design Suite, Vivado, ModelSim, MATLAB, Simulink: HDL Verifier; Instrument Control Toolbox.	.vhd,.xise,.ucf,.bit,.vi .mpf,.html,.xls,.xlsx

Design on the System Level is carried out by means of the software-controlled automated workstation for GNSS receiver design and testing which includes the appropriate equipment hardware and software units.

The hardware implementation of the automated workstation includes (figure 3):

- personal computer (1);
- development kit Nallatech Xtreme DSP Development Kit-IV (2) based on PLDs Xilinx Virtex-IV XC4VSX35-10FF668 and Virtex-II XC2V80-4CS144;
- arbitrary waveform generator GW Instek SFG-2108 (3);
- radio frequency combination analyzer Agilent N9914A FieldFox (4);
- digital oscilloscope LeCroy WaveRunner 64Xi (5).

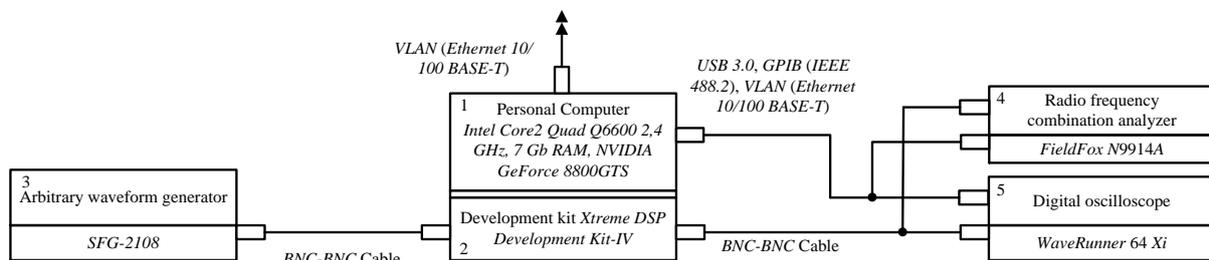


Figure 3. Schematic structure of the automated workstation hardware realization.

The following software is responsible for the interaction between the hardware components of the workstation:

- with the measuring equipment — the built-in modules of the LabVIEW and the Instrument Control Toolbox of the MATLAB/Simulink;

- with the development kit — the software DIMECheck and FUSE Probe from the kit's manufacturer.

The information exchange between hardware and software components as a part of the automated workstation is presented in figure 4.

The core of the workstation is the personal computer with software development tools deployed on it (6) including the application software (7) and the transforming module into the uniform format of the EDD (8) through which the interaction between the workstation and the Product Lifecycle Management (PLM) system (11) is carried out. The hardware tools include the measuring equipment (1) and the development kit (9).

The interaction between the software and the measuring equipment is carried out by the Virtual Instrument Software Architecture (VISA) standard (5) using the standardized input-output interface and supporting GPIB (2), USB 3.0 (3) and VLAN (4) interfaces. Interaction between the development kit and the software is carried out by the PCI Express input-output bus (10).

The PLM system is deployed on the basis of the system "Lotsman: PLM" (developer – ASCON, Saint Petersburg, Russia). In this software realization of the workstation open standards for data exchange based on the eXtended Markup Language (XML) are widely used as the unified format of EDD. The IP-XACT standard (IEEE 1685), which is an extension of the XML language for documentary block metadata used in processes of design and verification of microelectronic systems is applied.

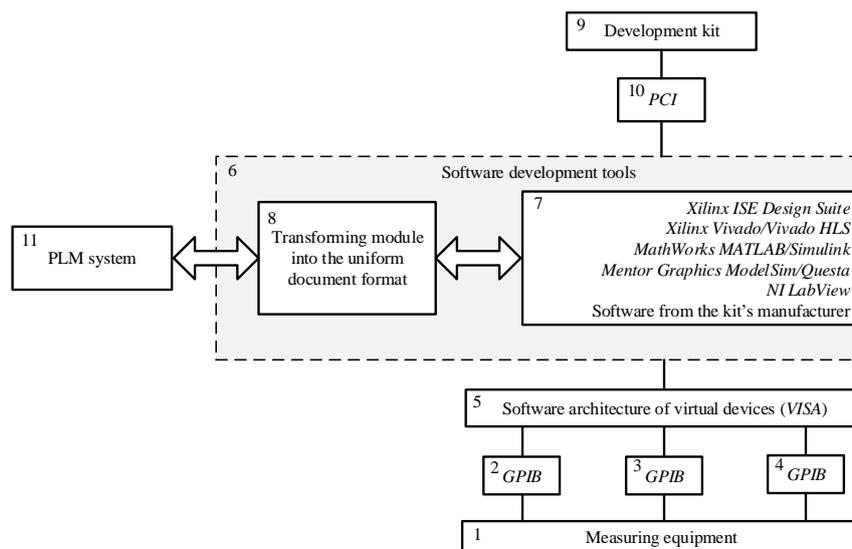


Figure 4. Schematic structure of the information interchange between the workstation's components.

The transforming module into the EDD is based on the C# language with using functions from the Tcl scripting language. The interaction of the module with the LabVIEW is carried out by means of the Model Interface Toolkit extension, with the MATLAB — with using of the built-in tools included in the Integrated Development Environment ActiveTcl. Interaction of the module with other software is carried out by built-in interpreters of the Tcl language that are included in the majority of existing CAD, CAPP and IDE systems used in radio-electronic industry. The developed automated workstation provides execution of design and testing processes of the digital GNSS receiver throughout all stages of the project cycle. At the same time automated recording of test results and formation of the required set of design documentation in electronic form is realized. The set of EDD is created using offered methods and algorithms has the required completeness and consistency.

This way, the automated workstation makes it possible to organize execution of design cycle processes of the radio-electronic equipment in the highly automated information environment,

accumulation of results, generated during various iterations of the design process and recording of test results. Accumulation and transmission of information are provided in standard markup formats – XML or XLS. The repository of information is implemented on the basis of the "Lotsman: PLM" system.

4. Conclusion

Design of modern radio-electronic devices is carried out in a complex information infrastructure, including CAD tools, libraries of logic elements, functional blocks, technological libraries, tools for correction a photomask, methods and means for preparation of products for industrial monitoring. The approaches for the integration of heterogeneous hardware and software demonstrated in this paper can be successfully used on different stages of the design and testing cycle.

In general, the design process of the unified information environment for support of design and testing processes of the radio-electronic equipment should be started with the determination of requirements to the unified format for data exchange and formalization of the design process stages. This allows to effectively combine heterogeneous hardware and software instruments into the IIE and, as a result, to increase effectiveness of the available instruments, to reduce the cost of refinement existing and the development of additional tools. This approach can be implemented in microelectronic design centers and factories which correspond to the current trend associated with the information integration and organization of "smart" foundry in high-tech areas of industry.

Acknowledgments

This work was supported by the Ministry of Education and Science of the Russian Federation in the framework of the Federal target program «Research and development of priority directions of development of the scientific-technological complex of Russia for 2014-2020» (agreement № 14.575.21.0142, unique ID project RFMEFI57517X0142).

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