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Development of a Wireless Dynamic Test Device for Low Strain Integrity Testing and Parallel Seismic Testing of Foundation Piles

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Abstract. The low strain integrity testing and the parallel seismic testing of foundation piles usually need dedicated instruments, respectively. The development of a wireless dynamic testing device based on Wi-Fi for foundation piles is introduced, which consists of a microcontroller with ADCs, a static RAM, a Wi-Fi transceiver module and other peripheral circuitries. The developed device features 16-bit dual-channel simultaneous sampling, variable trigger threshold and variable number of pretrigger samples, and it satisfies the requirements of both the low strain integrity testing and the parallel seismic testing of piles. A controlling computer should be present with the dynamic test device to conduct tests. Field tests were carried out on concrete bored piles with both test methods, and the test results have shown the functionality and reliability of the wireless dynamic test device.

1. Introduction

In civil engineering, good quality of foundation piles is essential for the safety of superstructures, however, piles are not readily available for visual inspection because they are often concealed in soil after construction. As a result, many non-destructive testing methods have been developed for the quality control/quality assurance of piles during construction, among which the low strain integrity test method[1] is a common and economical way to evaluate structural integrity of piles as well as to determine lengths of piles.

The low strain integrity test method is only applicable in the condition that the top of a pile is free and accessible, whereas the parallel seismic test method[2, 3] could be used to evaluate the quality or lengths of piles with superstructures as well as of the unknown or undocumented foundation piles, as actual conditions of piles are difficult to be extracted from low strain integrity test results in those scenarios.

The principles of both the aforementioned methods are on the basis of the theory of wave propagation in media. They involve measuring the time and the characteristics of elastic waves (mostly compressive waves) propagating through the pile or the surrounding soil. The compressive stress wave is generated by excitation on the top of a pile, usually by hand-held hammer blows.

Although the history of these methods is quite long, the instruments available nowadays on the market are usually dedicated to either the low strain integrity testing or the parallel seismic testing. In addition, these instruments are expensive. In fact, the underlying circuitries of these two kinds of

testing devices have a lot in common to some extent. So a dynamic test device supports both test methods is desirable and thus more cost-effective.

The major components of a common testing instrument include accelerometers, signal conditioning modules, a dynamic test device for signal recording and data processing and visualization equipment. The aim of this paper is to present the development of a wireless dynamic test device as well as field tests of both the low strain integrity testing and the parallel seismic testing conducted on concrete bored piles to verify the functionality and reliability of the device.

2. Hardware design

2.1. Overview of hardware of the dynamic test device

For a traditional dynamic test device used for the low strain integrity testing of piles, a single sampling channel is enough. However, at least two simultaneous sampling channels are necessary for the parallel seismic testing, due to the requirement that every first-peak arrival time of the stress waves from the excitation point on the pile to the accelerometer in the pipe since the time of excitation should be acquired accurately. The hardware block diagram of the dynamic test device is shown in figure 1.

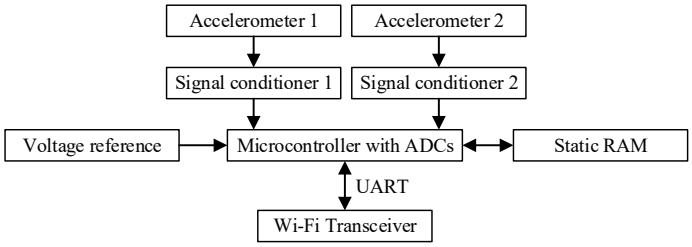


Figure 1. Hardware block diagram of the dynamic test device.

As in this device, a microcontroller with ADCs has the benefit to reduce the complexity of the hardware circuit as well as cut down the cost. An external precision voltage reference which has higher initial accuracy and lower temperature coefficient was selected instead of the microcontroller's internal voltage reference. Also, as the capacity of the on-chip memory for the storage of sampling data may not cover all the sample points for a single acquisition operation in practical applications, a high-capacity external memory is necessary. In addition, wireless communication which can eliminate the cable connection between the dynamic test device and the controlling computer could improve the testing efficiency in the field. Wi-Fi is a reasonable option, because it has been a standard feature of almost all laptop computers for a long time, thus there is no need to have a dedicated wireless communication adapter for the controlling computer.

2.2. Electronic circuit components

2.2.1. Microcontroller with ADCs. For the development in this paper, a C8051F060 of Silicon Labs which includes two 16-bit 1 Msps ADCs and a DMA interface was selected as the microcontroller. The C8051F060 is a fully integrated mixed-signal System-on-a-Chip MCU, its main highlighted features are as follows: high-speed pipelined 8051-compatible CIP-51 microcontroller core (up to 25 MIPS); in-system, full-speed, non-intrusive debug interface on-chip; 64 kB of in-system programmable flash memory; 4352 bytes of on-chip RAM; external data memory interface with 64 kB direct address space; UART serial interfaces implemented in hardware; five general purpose 16-bit timers; programmable counter/timer array with 6 capture/compare modules.

The two 16-bit ADCs and the DMA interface are the core for the implementation of signal sampling of the dynamic test device. As the dynamic test device requires high accuracy and high stability of the sampling clock, a 22.1184 MHz crystal is used with the external oscillator drive circuit to generate the system clock. Apart from this, the internal voltage references for ADCs and the on-chip XRAM are not used in this application.

2.2.2. External static RAM. The IDT71V124SA of Integrated Device Technology was selected as the external memory for samples storage. It is a 128k×8-bit high-speed static RAM, and it has an output enable pin which operates as fast as 5 ns, with address access times as fast as 10 ns available. As the direct address space of the external data memory interface of C8051F060 is 64 kB, a dedicated I/O pin should be used to help address the entire memory of IDT71V124SA by splitting the static RAM memory map into two 64 kB areas, if necessary.

2.2.3. External precision voltage reference. The LT1019CS8-2.5 of Linear Technology is a third generation bandgap voltage reference utilizing thin film technology and a greatly improved curvature correction technique. It has very low temperature coefficient (20 ppm/℃ max.) and tight initial output voltage tolerance (0.2% max.). The LT1019CS8-2.5 was used to generate the highly accurate and stable voltage reference for the two 16-bit ADCs and the two signal conditioners which convert the input signals to meet the input voltage range of the two ADCs.

2.2.4. Signal conditioners. The LT1806CS8 is a single low noise rail-to-rail input and output unity-gain stable operational amplifier which is optimized for low voltage, high performance signal conditioning systems. The signal conditioning circuitry for each input channel of ADC converts and shifts the voltage signal, which is the output from the dedicated signal conditioning module for the accelerometer, to meet the requirements of ADC input range.

2.2.5. Wi-Fi transceiver module. Various miniature Wi-Fi transceiver modules have become available on the market. To benefit from antennas with different gains, the module with the IPEX connector is preferable. The ESP-07S of Ai-Thinker was selected as the Wi-Fi transceiver module, which is based on the ESP8266 with highly competitive package size and ultra-low power technology. The ESP-07S communicates with the microcontroller C8051F060 via the UART serial port, and it could be configured with AT commands to automatically enter into the TCP client transparent communication mode whenever the module is powered on. So in effect the ESP-07S serves as a UART to Wi-Fi converter. This configuration can avoid dealing with the details of data transmission between the Wi-Fi module and the controlling computer manually.

3. Software design

The software of the dynamic test device consists of the data acquisition program for the microcontroller and the controlling program for the computer. The controlling program creates a TCP server after initialization. When the Wi-Fi connection between the computer and the dynamic test device is established, the Wi-Fi transceiver module which works as a TCP client will try to connect to the TCP server automatically. After the TCP connection has been established, it is ready for testing.

3.1. The program for the microcontroller

As the ESP-07S serves as a transparent UART to Wi-Fi bridge, the microcontroller can directly receive and send data via its UART port without knowing the existence of the Wi-Fi transceiver module. Therefore, the program for the microcontroller just initializes the system and configures the timers, the UART port, the 16-bit ADCs and the DMA interface, and then it goes into a loop of awaiting, parsing and executing of commands from the controlling computer. The variable trigger threshold is implemented with the ADC0 programmable window detector and software intervention. The program flowchart of the main loop of the program for the microcontroller is shown in figure 2.

3.2. The controlling program for the computer

The controlling program provides data acquisition control, data processing and visualization, and data management. The raw data of acceleration received from the dynamic test device is processed and converted to velocity data for analysis[4]. As integration is applied to obtain velocity from

acceleration[5, 6], it is important to remove the drift in the raw acceleration data to obtain correct velocity curves[7, 8]. The program flowchart of a single data acquisition is shown in figure 3.

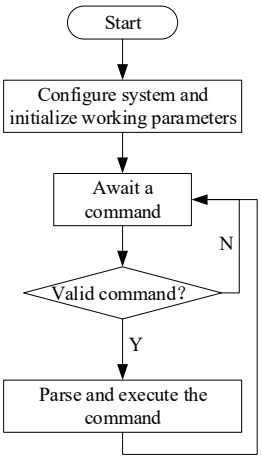


Figure 2. Flowchart of the main loop of the dynamic test device.

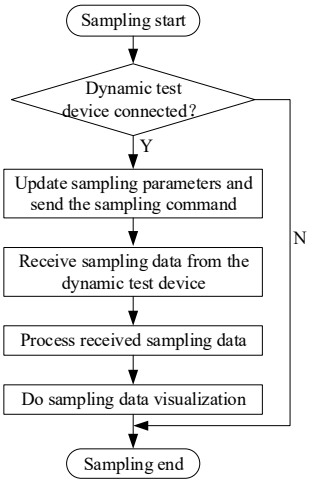


Figure 3. Flowchart of a single data acquisition.

4. Field tests and results

To test the functionality of the prototype of the wireless dynamic test device, both the low strain integrity test and the parallel seismic test were conducted on the exposed concrete bored piles in the field. The off-the-shelf charge output accelerometers and the dedicated signal conditioning modules were used in the tests. Besides, a generic laptop computer was used as the data processing and data visualization equipment, on which the controlling program ran.

4.1. Low strain integrity testing and results

The basic design specifications of the bored piles for low strain integrity testing were as follows: pile diameter, 900 mm; grade of concrete, C25. The surrounding soil was soft clay. The main parameters of the dynamic test device were set as follows: sampling frequency, 40 kHz; number of data points per acquisition, 1024.

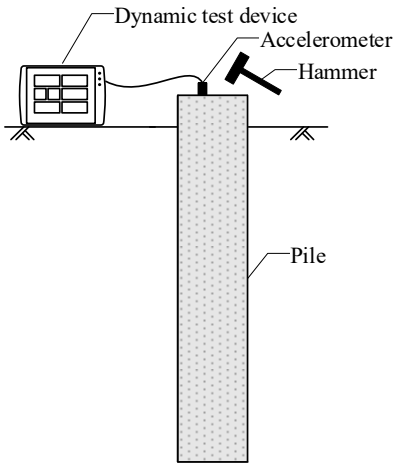
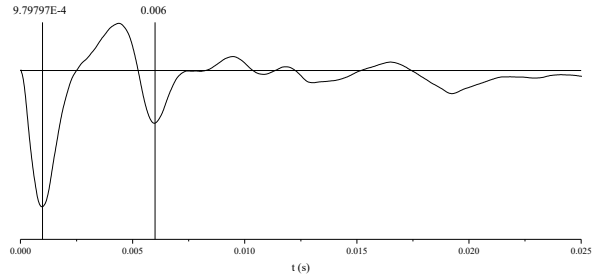
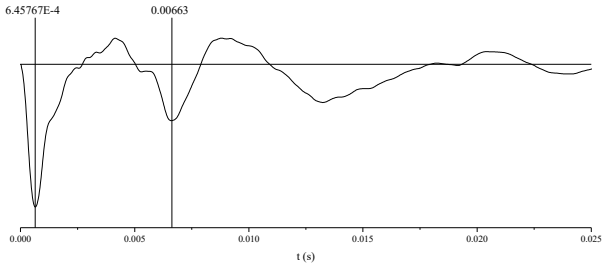


Figure 4. Schematic diagram of the low strain integrity testing.



(a) Pile length: 9.00 m, calculated pile length: 9.04 m.



(b) Pile length: 10.30 m, calculated pile length: 10.77 m.

Figure 5. Results of two low strain integrity tests.

As shown in figure 4, the charge output accelerator mounted on the top of the pile was connected to a charge amplifier; the output of the charge amplifier was connected to the signal input of the dynamic test device. The excitation was applied with a nylon hammer on the top of the pile. The hammer impact generates the compressive stress wave that travels down along the axis of the pile to the bottom where the wave is reflected back to the top of the pile. For each pile, several records were obtained with the same procedure. As the raw data collected was acceleration, the velocity was obtained by amplifying, filtering and integrating. Only the curve containing clear features was retained.

The test results of two different bored piles are shown in figure 5. As the reflected wave from the bottom of each pile is prominent, the length of pile can be obtained with the following equation:

$$L = cT/2 \quad (1)$$

where c is the wave velocity in the concrete medium, L the pile length below the accelerometer, T the time difference between the first and the reflected extremum. The calculation assumed the wave velocity of 3600 m/s.

4.2. Parallel seismic testing and results

The basic design specifications of the bored piles for parallel seismic testing were as follows: pile diameter, 900 mm; pile length, 9.0 m; grade of concrete, C25. The surrounding soil was soft clay. The inside diameter of the PVC pipe parallel with the pile was 58 mm, and the outside diameter was 68 mm. The bottom of the pipe was about 2 m below the bottom of the pile. The distance between the pile and the pipe was 350 mm. The main parameters of the dynamic test device were set as follows: sampling frequency, 80 kHz; number of data points per acquisition, 1024.

As shown in figure 6, the pipe parallel with the pile was filled full with clean water in advance. Then the probe, which was actually a charge output accelerator of high sensitivity, was put in

downward to the bottom of the pipe. The probe was made to be able to contact the inner wall of the pipe, thus ensuring good collection of the stress wave. Besides, another charge output accelerator mounted on the top of the pile was used to trigger the sampling operation.

The data acquisition was conducted from the bottom upward to the top of the pipe. When the probe rose and reached the position for sampling, a hard rubber mallet was used to hammer at the top of the pile to trigger the sampling. Within the 5.5 m below the top of the pile, data was collected at intervals of 0.5 m along the pipe, and the rest at intervals of 0.25 m.

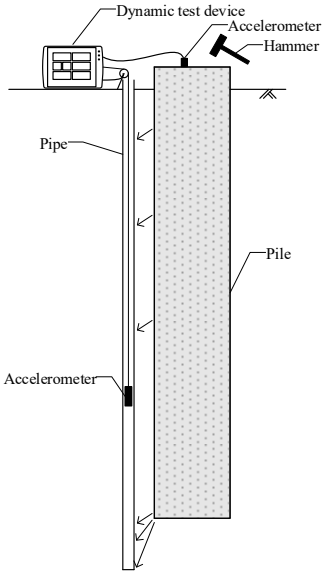


Figure 6. Schematic diagram of the parallel seismic testing.

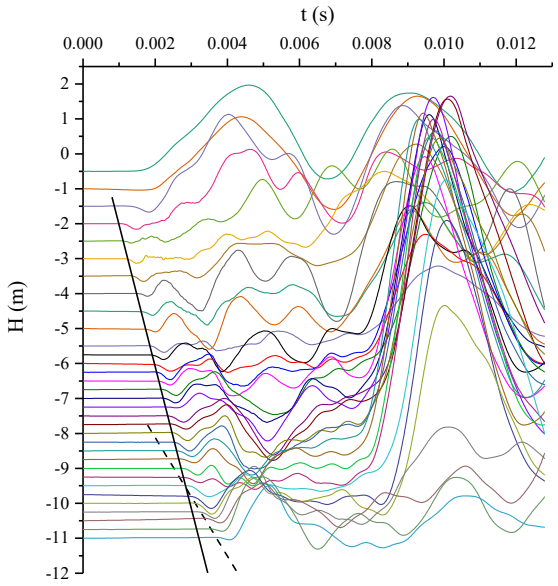


Figure 7. Time–depth curves of the parallel seismic test.

As shown in figure 7, the velocity curves obtained in the test are arranged according to their depths of acquisition. The times of arrival of the initial peak on the velocity curves and the depths of the velocity curves could be extracted and classified into two line groups: the upper line group and the lower line group. By fitting lines to these data points, the equations for the upper line and the lower line could be obtained as follows:

$$H = -4049.34t + 2.00 \quad (2)$$

$$H = -1696.59t - 4.72 \quad (3)$$

Therefore, the depth of intersection can be obtained, which is -9.57 m. When the distance between the pipe and the pile is short, the depth of the intersection point of the two lines could be taken as the position of the bottom of the pile[9], but it is slightly deeper than the actual position of the bottom of the pile[10, 11].

5. Conclusions

In this paper, the development of a wireless dynamic test device that supports both the low strain integrity test and the parallel seismic test of the foundations piles is presented, including the hardware design and the software design. The compact implementation of this device is based on the microcontroller with two simultaneous sampling 16-bit ADCs and the DMA interface, the standalone high-capacity static RAM, the external precision voltage reference, the Wi-Fi transceiver module and other peripheral circuitries. The device only handles the sampling and data transmission, whereas the controlling computer deals with the computationally intensive data processing and all the rest. The test results of the low strain integrity test and the parallel seismic test on concrete bored piles in the field showed the functionality and reliability of the developed device. And its low cost could make it a

competitive device as compared with those dedicated testing devices for the low strain integrity testing or for the parallel seismic testing available now on the market.

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