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Research and design of integral circuit for electronic current transformer

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Abstract. Aiming at the problem of serious magnetic saturation, small dynamic range and difficult digital processing of traditional electromagnetic current transformers, an electronic current transformer design method based on digital integrators is proposed. It includes selection of integral algorithm, determination of sampling rate and resolution, and structure design. Using the calibration test platform for system testing and analysis, the ratio error is less than ± 0.5%, the phase angle error is less than ± 20′, and the entire system achieves the 0.2 class accuracy. The test results show that the electronic current transformer is stable, reliable and accurate, and can meet the practical application requirements.

1. Introduction

With the development of computer digital communication technology, power systems have become increasingly demanding for measurement, protection, control, and data transmission intelligence as well as power grid security, reliability, and high-quality operation. Traditional electromagnetic current transformers had the disadvantages of high insulation requirements, serious magnetic saturation, small dynamic range, and difficulty in digitizing currents, which hindered the improvement of the automation level of the power system [1]. The new type of electronic current transformer based on Rogowski coil makes up for the defects of traditional transformer. The signal induced by the Rogowski coil needs to be processed by the integrator. So as a key link of the active current transformer, the performance of the integral circuit determines the spectrum range and response time of the signal [2]. The design of the integrator circuit directly affects the measurement accuracy of the transformer, and then affects the performance of the entire system. The excellent integrated circuit can broaden the dynamic range of the electronic current transformer based on Rogowski coil and improve its linearity and measurement accuracy [3].

In summary, this paper mainly discussed the design method of a digital integrator. It included the selection of integral algorithm, the determination of sampling rate and resolution, and the structural design. The research showed that the electronic current transformer composed of the integral circuit had stable and reliable working performance, high precision, effective design method, and could meet actual measurement requirements.

2. Design principle of digital integrator

2.1. Integral algorithm of digital integrator

Compared with the analog integrator, the digital integrator hardware circuit has a simple structure, and an appropriate integration algorithm can be used to implement the integration function according to different situations. The phase characteristics are excellent, the performance is stable, and it is not susceptible to outside interference, so the environmental adaptability and reliability can be greatly improved. Using numerical calculation theory to analyze its integration algorithm was as follows [4]. According to the general form of numerical quadrature, the Newton-Cotes quadrature formula was derived using the interpolation.

$$\int_a^b f(x)dx \approx \sum_{i=0}^{n} \lambda_i^n f(a + k\frac{b-a}{n}) \tag{1}$$

Where λ_i^n was the quadrature coefficient, and $\lambda_i^n = (b-a)\frac{(-1)^{n-i}h}{i!(n-i!)n}\int_0^n\left[\prod_{j=0}^{n}(t-j)\right]dt$.

When n=0, the cumulative quadrature formula was obtained according to Newton-Cotes quadrature formula.

$$\int_a^b f(x)dx \approx (b-a)f(a) \tag{2}$$

When n=1, the trapezoidal quadrature formula based on Newton-Cotes quadrature formula was:

$$\int_a^b f(x)dx \approx \frac{(b-a)}{2}[f(a) + f(b)] \tag{3}$$

When n=2, the parabolic quadrature formula (Simpsion quadrature formula) was obtained according to Newton-Cotes quadrature formula.

$$\int_a^b f(x)dx \approx \frac{(b-a)}{6}\left[f(a) + 4f\left(\frac{a+b}{2}\right) + f(b)\right] \tag{4}$$

When n=2, the Simpsion3/8 quadrature formula was obtained according to Newton-Cotes quadrature formula.

$$\int_a^b f(x)dx \approx \frac{(b-a)}{8}\left[f(a) + 3f\left(\frac{2a+b}{3}\right) + 3f\left(\frac{a+2b}{3}\right) + f(b)\right] \tag{5}$$

When n=2, the Cotes quadrature formula was obtained according to Newton-Cotes quadrature formula.

$$\int_a^b f(x)dx \approx \frac{(b-a)}{90}\left[7f(a) + 32f\left(\frac{3a+b}{4}\right) + 12f\left(\frac{a+b}{2}\right) + 32f\left(\frac{a+3b}{4}\right) + f(b)\right] \tag{6}$$

In order to solve the problem of convergence and stability of Newton-Cotes quadrature formula under multi-node conditions, usually the complex quadrature method was used to reduce the integration interval, so as to obtain an accurate integration result. That is, the Newton-Cotes quadrature formula was used to calculate each sub-interval after the integration interval was subdivided, and then the integral result was added to obtain the integral value of the entire interval.

In the case of the same integral interval, combining the accuracy requirements of the integration and the algorithm structure, we could analyze the above situations to obtain a conclusion. Accumulation method requires the largest number of sampling points and the smallest amount of calculation. The trapezoid formula is the second, and the Simpsion formula has the smallest number of sampling points and the largest amount of computation. Therefore, the digital integrator selected the trapezoidal formula algorithm [5].

2.2 Determination of sampling rate and resolution

When designed the digital integrator, it was necessary to determine the sampling rate and resolution requirements of the system to the analog-digital converter (ADC) so as to select the device [6]. The relationship between digital frequency ω and the number of sampling points N per unit period was as follows.

$$\omega = T\Omega = \frac{2\pi f}{f_s} = \frac{2\pi}{N} \tag{7}$$

Where f is the analog frequency and fs is the sampling frequency. When the analog signal was quantized, the error was called quantization error. Assuming that there was no such quantization error, the minimum number of sample points N necessary for the integration algorithm could be calculated under certain accuracy requirements to determine the minimum sampling rate required by the digital integrator.

The resolution of the ADC reflected the effect of quantization error on system accuracy. While the quantification process was a nonlinear process, deterministic analysis and statistical analysis were usually used to study its impact on the system. Determining the steady-state error of the trapezoidal

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formula using the deterministic analysis method was as follows.

$$\varepsilon_0 = \varepsilon \lim_{z\to 1} \frac{T(z+1)}{z-1} = \infty \tag{8}$$

In the absence of compensation link, quantization error might lead to steady-state output saturation of the system. Therefore, in order to ensure the accuracy and stability of the digital integrator, it is necessary to solve the problems such as DC offset, integral initial value and input saturation. For DC offset, consider adding a high-pass filter (HPF) between the integrator input and the ADC output, or set a DC compensator at the input of the integrator. For ADC saturation, consider using a multi-gain amplifier circuit or a high-resolution ADC.

3. The structure of the digital integrator

Digital integrators generally consist of digital circuits built from A/D converter chips and digital signal processors (DSP) or FPGA. Combined with its integral algorithm, the digital integrator was designed with the ADC-DSP-DAC scheme. The principle block diagram was shown in figure 1.

Figure 1.The principle block diagram of digital integrator based on ADC and DSP.

The function of the front end circuit was signal conditioning and low pass filtering. ADC used 16 bit analog-to-digital converter ADS8320, DSP adopted TMS320LF2407A of TI computer, DAC used 12 bit to analog converter TLU5616. The main function of the postposition circuit was to smooth the output of DAC. The sampling rate of the prototype was 40 kHz.

A digital integrator consisting of an A/D converter chip had a higher sampling rate than a digital integrating circuit composed of a voltage-to-frequency converter. It could achieve integral within larger bandwidth and lower power consumption, which was a good choice for electronic transformers with high efficiency and stability. Therefore, electronic transformers often use A/D converter type digital integrators. The voltage signal induced by Rogowski coil was generally small, and the integral operation was realized in the digital integrator after amplifying circuit processing and A/D conversion. It could be known from the working principle of the digital integrator that the error mainly depended on the selection of the integration algorithm and was insensitive to external interference.

4. System testing and analysis

In order to determine the design parameters, the electronic current transformer prototype composed of the digital integrator needed to be tested for accuracy. The prototype was placed at room temperature, and the accuracy test was carried out with the calibration test platform. The rated voltage was 110kV, rated current was 600 A (IN) and the rated secondary output was digital signal. Several current test points were selected in the range of (3%-120%) IN, and the ratio error and phase error curve of the electronic current transformer system were shown as figure 2 and figure 3.

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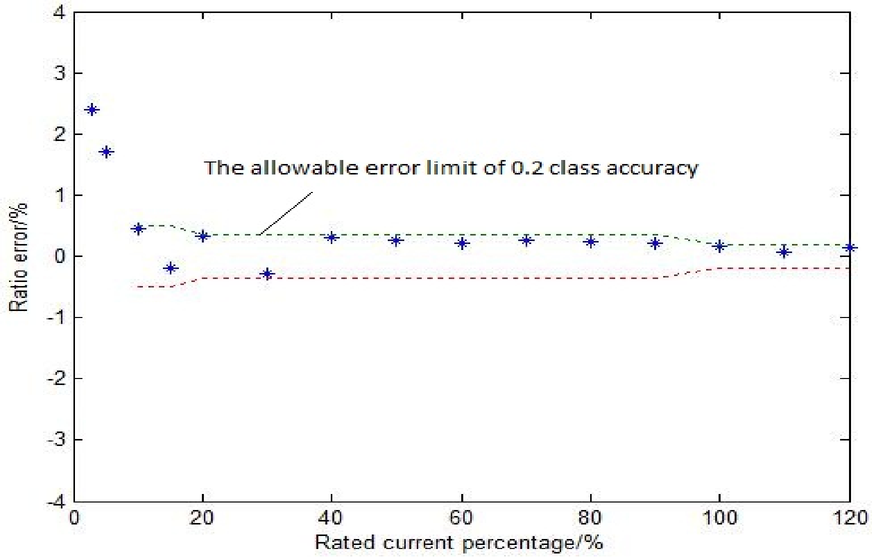

Figure 2.The ratio error curve of electronic current transformer.

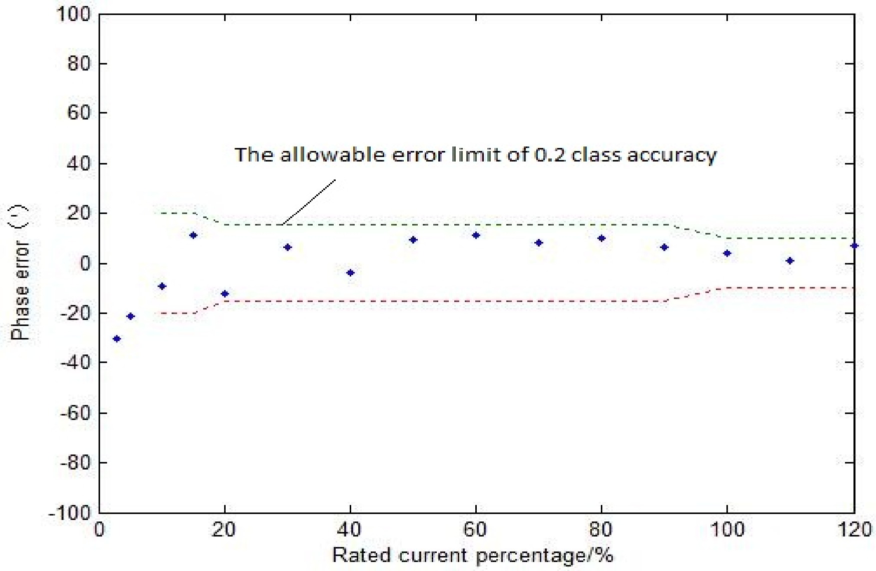

Figure 3.The phase error curve of electronic current transformer.

As shown in figure 2 and figure 3, the ratio error of the output current of the electronic current transformer in the range of (3%-120%) IN is less than that of the man 0.5%, the error of the phase error is less than the scholar 20', which meets the requirement of the 0.2 class accuracy.

5. Conclusions

This paper presented a design method of electronic current transformer based on digital integrator. It mainly discussed the integral algorithm and structure design of the digital integrator, and carried out system test and analysis with the calibration test platform. The test results show that the ratio error is less than ± 0.5%, the phase error is less than ± 20´, and the entire system achieves the 0.2 class accuracy and meets the actual application requirements.

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