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Low Power Wallace Tree Encoder For Flash ADC

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Abstract – Flash ADC is the fastest analog to digital converter. It is also known as parallel ADC. It consists of a resistor ladder, a comparator and an encoder circuit. The encoder circuit converts the thermometer code which is the output of comparator into binary code. The efficiency of encoder is very important. It should be capable of reducing the bubble errors and should dissipate low power. Wallace tree encoder is well efficient in reducing all the bubble errors. This paper proposes a low power Wallace tree encoder for Flash ADC. It is having a power dissipation of 939.43pW and delay of 5.38nS. The proposed encoder is implemented in 180nm CMOS technology with 1.8V supply voltage and was simulated using Mentor graphics.

1. Introduction

Most of the real world signals are analog in nature. They are difficult to store and even more difficult to process. So it becomes necessary to convert them into digital form. An analog to digital converter converts any analog signals into digital data, which makes it easier to store and process as well as more accurate and reliable. These ADCs vary in speed and performance. Flash ADC which is also called parallel ADC is best suited for high speed low resolution applications. It consists of a resistor ladder network, a comparator and an encoder circuit. For an N bit Flash ADC there are 2^N resistors and 2^N-1 comparators. The resistor ladder provides the reference voltage. The comparator compares the input voltage with the reference voltage. Each comparator produces a '1' when its analog input voltage is higher than the reference voltage applied to it. Otherwise the comparator output is '0'. Output of the comparator is a thermometer code. Thermometer code resembles the output of a thermometer. In thermometer code, a value representing number 'N' has the lowermost N bits as '1', others are '0'. Code consists of sequence of zeros followed by sequence of ones. There cannot be zero in between two ones. The encoder circuit converts the thermometer code to binary. Fig. 1 shows the block diagram of Flash ADC.

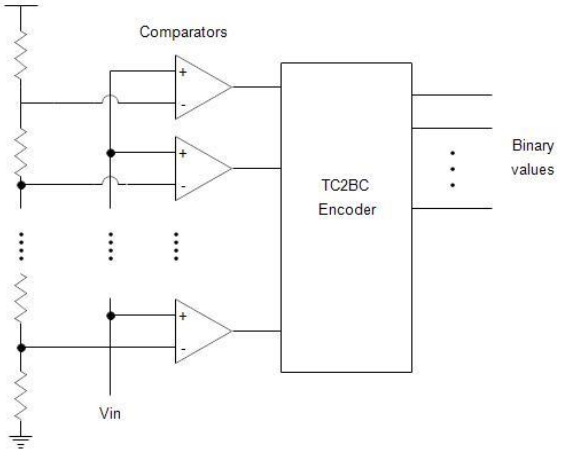

Fig. 1: Block diagram of Flash ADC

Encoder performance is very important for the design of Flash ADC. High speed encoders are used in Flash ADCs for applications such as disk drive read channels and UWB communication receivers involving medium to high resolution and high speed [1]. Normally the thermometer code consists of series of zeroes followed by ones. There should be only one transition. But in some cases zeroes come in between ones or vice versa. This condition is called bubble error. So while designing an encoder care should be taken to reduce this error. The basic building block of Wallace tree encoder is the full adder circuit. For the inputs 011 and 101 the sum and carry outputs are the same. 011 represent the normal thermometer code since there is only one transition and 101 represent the error condition. For both these input conditions output of the full adder remains the same. So even though bubble error exists in the input of Wallace tree encoder the output will not be affected.

Reference [2] gives a Wallace tree encoder with a power dissipation of 1.506nW and a power-delay product of 7.71aJ. This paper proposes a low power Wallace tree encoder by modifying the basic component i.e. full adder circuit. This circuit is having a power dissipation of 939.43pW and a power-delay product of 5.476aJ.

2. Wallace Tree Encoder

The Wallace tree encoder also called as ones counter is built with full adder cells. It counts the number of ones present at the output of comparator and represents them as binary code. Fig. 2 shows a 3 bit Wallace tree encoder with full adder as its basic cell. The full adders count the number of logic "1" at their input to give final binary output. The full adders are arranged to sum the inputs so as to form Wallace tree.

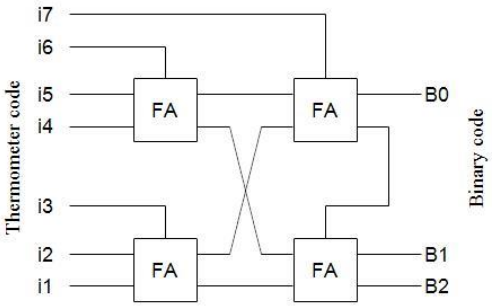

Fig. 2: 3-bit Wallace tree encoder

Even when bubble errors are present, this encoder converts output of comparator into correct binary output. Another advantage of this encoder is flexibility such that suitable topology can be selected according to speed and power requirements [5]-[7]. The number of full adder cells needed to implement an N bit encoder is given by the equation,

$$X_N = \sum_{i=1}^{N}(i-1).2\hat{}(N-i) \quad (1)$$

3. Wallace Tree Encoder Using 28T Full Adder

Reference [2] gives a 28 transistor full adder circuit as shown in fig. 3. The equations for sum and carry output is given as,

$$Sum = A\ xor\ B\ xor\ Cin \quad (2)$$

$$Cout = A.B + Cin\ (A\ xor\ B) \quad (3)$$

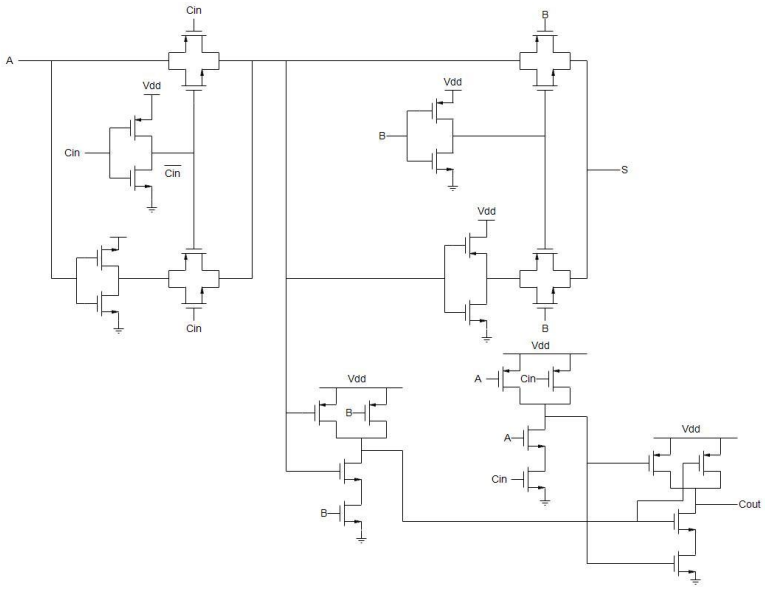

Fig. 3: Conventional 28T full adder

The conventional CMOS full adder shows robustness against voltage scaling and transistor sizing. The disadvantages are high input capacitance and requirement of buffers [3]. The schematic of Wallace tree encoder built using this 28T full adder is as shown in fig. 4.

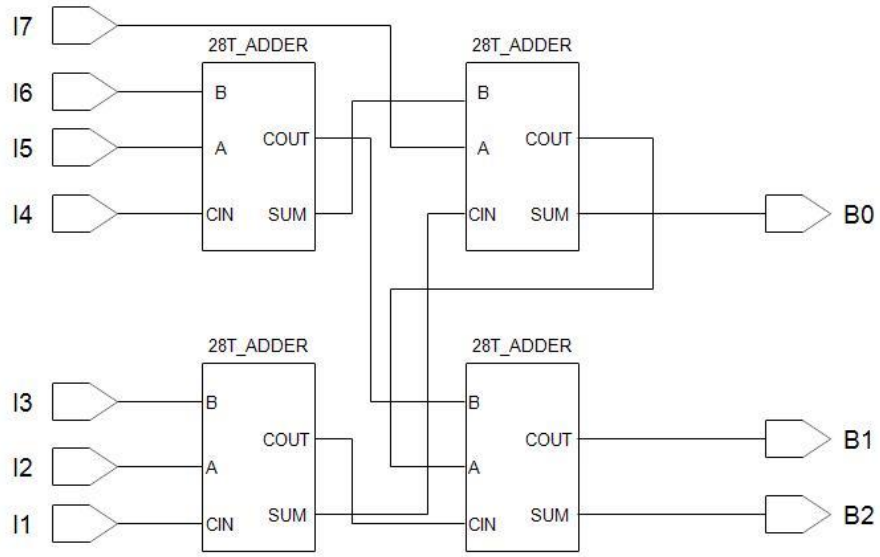

Fig. 4: Schematic of Wallace tree encoder using 28T full adder

The above circuit is simulated using Mentor graphics simulation tool. It gives a full swing output with a supply voltage of 1.8V. The simulation results show that this encoder circuit is having a delay of 5.12 nS and power dissipation of 1.506nW. In order to design a low power Flash ADC it is necessary to reduce the power dissipation of the encoder circuit. By changing the internal full adder circuit of this encoder a remarkable change in the power dissipation is observed.

4.Wallace Tree Encoder Using 14T Full Adder

A new full adder circuit using 14 transistors is proposed. Although the device count is very low, the circuit has full voltage swing in all nodes [4]. More than one logic style is employed for its implementation. It uses Ex-OR/ Ex-NOR module and transmission gate logic. 14 transistor full adder circuit is shown in fig. 5

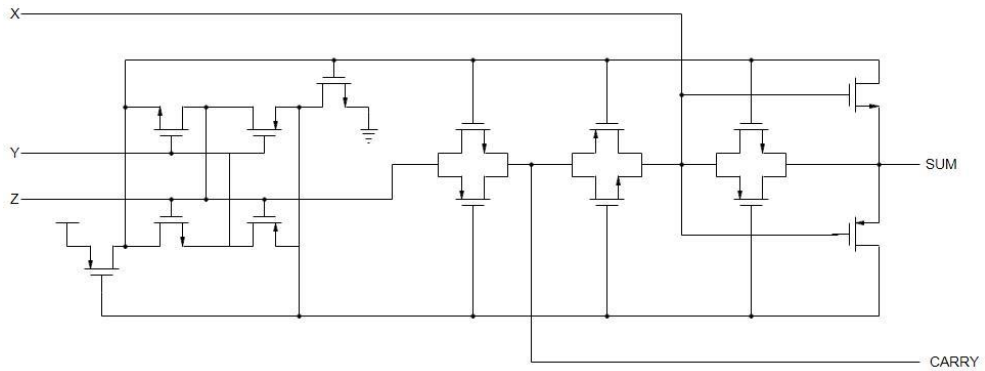

Fig. 5: Proposed 14T full adder

A low power encoder is designed using this full adder circuit and simulated using Mentor graphics tool. Fig. 6 shows the schematic of the encoder.

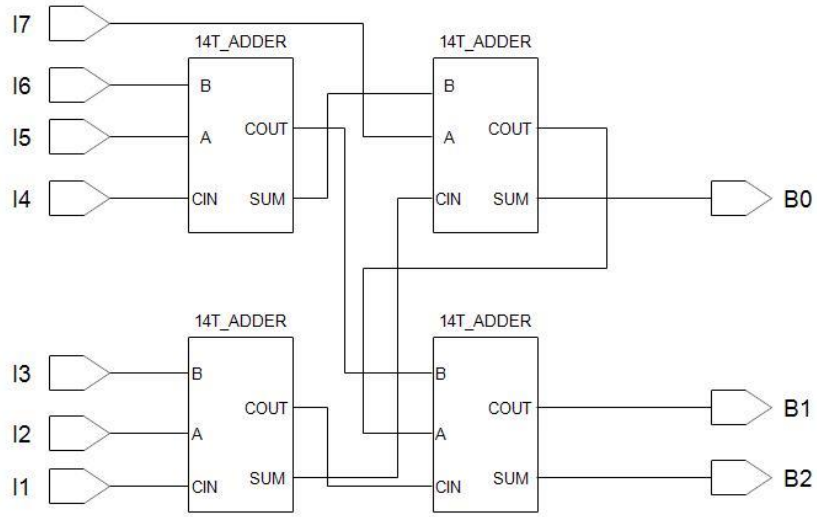

Fig. 6: Schematic of Wallace tree encoder using 14T full adder

This circuit is simulated using mentor graphics simulation tool in 180nm technology. It is having a delay of 5.83nS . Even though the delay of this circuit is slightly greater than that of the circuit shown in fig. 4 its power dissipation is very low. It is observed to be 939.43pW. Hence the overall power-delay product of this circuit is comparatively low.

5.Power Consumption And Delay Analysis

Wallace tree encoder circuit given in reference [2] which is constructed using 28T full adder is simulated using mentor graphics and results are compared with that of proposed encoder. The comparison is tabulated.

Table. 1 Comparison of power, delay and power delay product

Wallace tree encoder	Power Dissipation	Delay (nS)	PDP (aJ)
Using 28T full adder	1.506nW	5.12nS	7.71aJ
Using 14T full adder	939.43pW	5.83nS	5.47aJ

6.Conclusion

Thermometer code to binary code conversion in Flash ADC is done using suitable encoder circuits. Wallace tree encoder is capable of reducing all the bubble errors in the thermometer code and it provides a proper binary output. This paper proposes an efficient Wallace tree encoder which

dissipates less power. It has a power dissipation of 939.43pW which is comparatively less than previous designs. Hence the proposed encoder is well suitable for the design of low power Flash ADC.

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